Cryogenic CMOS Characterization for Quantum Computer Applications

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P.A. 't Hart

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Cryogenic CMOS Characterization

for Quantum Computing Applications

Cryogene CMOS Karakterisering voor Kwantumcomputer Applicaties

PROEFSCHRIFT

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van Rector Magnificus Prof.dr.ir. T.H.J.J. van der Hagen,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op maandag 21 november 2022
klokke 1230h

door

Pascal Alexander 't HART

Electrotechnisch ingenieur
geboren te Gouda.

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Chapter 1

Introduction

1.1 The Quest for Faster Computation

Humans in general are not optimized for carrying out repetitive tasks, such as those required in large calculations: our attention is nonlinear, time variant and subject to many external factors, making us inefficient and error prone. Since ancient times people have been looking for ways to automate these tasks and came up with solutions in the form of what nowadays would be called a computer. One of the first computers, the Antikythera mechanism, was based on pure mechanics and most likely used for calculations related to astronomy [1]. As time progressed, electromechanical computers emerged, such as the Bombe, which was built specifically for Enigma deciphering [2]. Later on, the vacuum tube was invented and even larger machines were built, capable of faster and more complex calculations. A prime example of such a machine is the Electronic Numerical Integrator and Computer (ENIAC), used in the development of thermo-nuclear weapons [3]. Finally, the transistor was invented, leading to the development of CMOS, which enabled the speed and level of integration required to build today's (super)computer. An interesting thing to note is that the driving force behind the development of faster and higher capacity computers is strongly coupled to mankind's favourite occupations: waging wars, optimizing financial gains and gaming.
Although modern data centers are quite impressive, both in terms of their size and computing power, a certain class of problems is intractable even for classical supercomputers. Searching large data sets, prime factorization, but also modeling of complex systems, such as those found in molecules or the weather, are either too computationally complex or require a prohibitive amount of time to complete. Quantum computation is a new computing paradigm that holds the promise of solving such problems [4, 5]. At the basis of the quantum computer lies the quantum bit (qubit), which, in addition to the '0' and '1' state of the classical bit, can assume a composite state that is a superposition of two base states denoted by

$|0\rangle$ and $|1\rangle$. The state of a qubit can thus be represented by $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$, where α and β are complex coefficients, satisfying the condition $|\alpha|^2 + |\beta|^2 = 1$. All possible states of the qubit lie on a unit sphere, also known as a Bloch sphere, with the $|0\rangle$ and $|1\rangle$ base states located at the north and south pole, respectively. The two poles are equivalent to the two states of the classical bit, while all the composite states between the poles are exclusively available in qubits. These superposition states allow the quantum computer to encode much more information per bit as compared to a classical computer. A second property specific to qubits is entanglement. When a change in one qubit affects other qubits in a predictable way, these qubits are said to be correlated or entangled. Specific quantum algorithms exploit the existence of these quantum effects, i.e., superposition and entanglement, to enable an exponential computational speed up compared to its classical counterpart.
In order for these quantum effects to arise, and for the quantum states to be detectable, the qubits typically need to be cooled down to extremely low temperatures in the range between 10 mK and 100 mK. In order to perform quantum computation, the state of the qubits needs to be controlled and read-out by classical electronics, capable of the generation and measurement of specific electrical signals. Since the qubit state deteriorates in time, after an interval known as decoherence time, the controller in addition to this sensing time constraint, has as additional task to correct the errors introduced in the qubit state due to decoherence (Quantum Error Correction, QEC) during calculations [6].

1.2 Cryo-CMOS as Quantum Computer Enabler

The quantum computers of today comprise only a few tens of qubits, which are directly connected to room-temperature equipment located outside of the cryogenic refrigerator. This equipment consists of large commercial, or custom made signal sources and digitizers. Wires carry the signals from the room-temperature electronics, through the refrigerator, to the qubits that sit at deep-cryogenic temperatures.
This is still a workable solution for the small number of qubits in a research setting. However, in order to run any useful quantum algorithm, thousands to even millions of physical qubits are required [6, 7], making this approach unfeasible. The current approach can be compared with connecting a mega-pixel CCD through meters-long interconnect to read-out circuits: this solution does not scale, consumes a prohibitive amount of space (both the wires in the fridge and the equipment outside of it), is extremely costly and poses many reliability issues.
A possible approach that tackles most of the above-mentioned challenges, is the implementation of the control and read-out electronics into an integrated circuit that can be placed close to the qubits. This forces the controller to operate at deep-cryogenic temperatures comparable to those of the qubits [8, 9, 10, 11, 12, 13].

Nanometer CMOS is the platform of choice for the cryo-controller by virtue of its high level of integration and maturity, enabling the complex circuits required for the generation, detection and processing of the electrical signals by the controller. The key features of CMOS that make it a perfect fit for this application are its high speed of operation required for handling the microwave signals, and its power efficiency, which is of prime importance for operating within the limited power budget of the refrigerator. Most importantly, CMOS was proven to operate reliably down to deep-cryogenic temperatures [14]. This opens up the possibility to co-integrate the controller and the solid-state qubits onto a single substrate, enabling a scalable quantum computer.
These CMOS properties enable the design of cryogenic circuits in theory; however, in practice, designers need additional information on the low-temperature behaviour of MOSFETs in order to design circuits that operate as intended in a cryogenic environment. This behaviour is captured in compact models, used for simulating the circuits to ensure that the specifications are met.

1.3 The Importance of Cryogenic Device Modeling

Device characteristics at cryogenic temperatures can deviate significantly from their room temperature behaviour. For example, the threshold voltage of a MOSFET can increase by more than 100 mV when it is cooled down to 4.2 K, as shown in this thesis. If a designer is not aware of this shift, circuits that work as intended at room temperature can potentially fail at deep-cryogenic temperatures due to the resulting change in bias points, or even due to devices that are unable to be switched on.
Device characterization is an indispensable step in building models for circuit designers. Foundries characterize their technology over the standard military temperature range (-55 to 125 °C) and generally do not supply compact models (yet) that are valid at deep-cryogenic temperatures.
Therefore, designers of cryogenic circuits have to rely on back-of-the-envelope calculations and must build in margins to allow for parameter shifts, as they are unable to fully simulate their designs with use of the existing electrical simulators. These margins cause circuits to most likely occupy more silicon area than required and thus operate at lower speeds and with increased power dissipation compared to an optimized circuit. As the power budget is severely limited, this is a very important challenge of (current) cryogenic circuit design. Worst of all, circuits deviating from the stringent specifications for quantum control can lead to lower fidelity of quantum operations [15].
In order to overcome these challenges, cryogenic device characterization needs to be carried out, to investigate and capture the impact of low temperatures on different device parameters. A convenient temperature to operate cryogenic circuits at, is that of liquid helium, which lies around 4.2 K. Therefore, most characterizations

are carried-out at this temperature. Effort was already devoted to characterization and modeling at these temperatures by other groups, see Chapter 2 for an extensive overview. However, not much attention was spent on the impact of these extreme temperatures on device matching and self-heating in advanced processes. The work presented in this thesis, therefore, focuses on the design and characterization of test chips in an advanced 40-nm process, and the subsequent modeling of device mismatch and self-heating at cryogenic temperatures.

1.4 Objective and Scope of This Thesis

The objective of this thesis is to gain more insight into cryogenic MOSFET behaviour, with the aim to build models to be used by circuit designers developing the cryogenic controller. These models involve the primary DC behaviour and secondary effects such as device matching and self-heating.
In order to attain this objective, multiple dedicated test structures were designed and fabricated in a 40-nm bulk CMOS process, which is the intended platform for the cryogenic controller. All measurements carried out and presented in this thesis were performed on these 40-nm bulk CMOS test structures. All characterizations were carried out at DC in the temperature range from 300 K down to 4.2 K.

1.5 Organisation of This Thesis

This thesis is organized as follows. Chapter 2 details the cryogenic device characterization and modeling of I_D-V_G and I_D-V_D curves measured on large arrays of MOSFETs. The tools available for cryogenic characterization of test samples are described, followed by a summary of the low-temperature impact on the most common MOSFET parameters. The chapter concludes with the DC modeling of a 40-nm bulk CMOS process, employing Artificial Neural Network training.
In Chapter 3 an extensive device mismatch study is presented of devices operated from 300 K down to 4.2 K. This chapter is split into two parts. The first part focuses on devices operated in the moderate- to strong-inversion regime, while the second part investigates specifically the matching behaviour of devices biased in the subthreshold regime. Models are presented able to predict drain-current mismatch in all regions of operation.
Chapter 4 presents an in-depth study on the self-heating of devices in a cryogenic environment. The channel temperature of a MOSFET as function of dissipated power and ambient temperature is extracted and modeled. To gain more insight into possible electro-thermal coupling between circuits, a spatial temperature profile up to 30 µm from the dissipating devices was measured.
Finally, conclusions are drawn and some suggestions for future work are given in Chapter 5.

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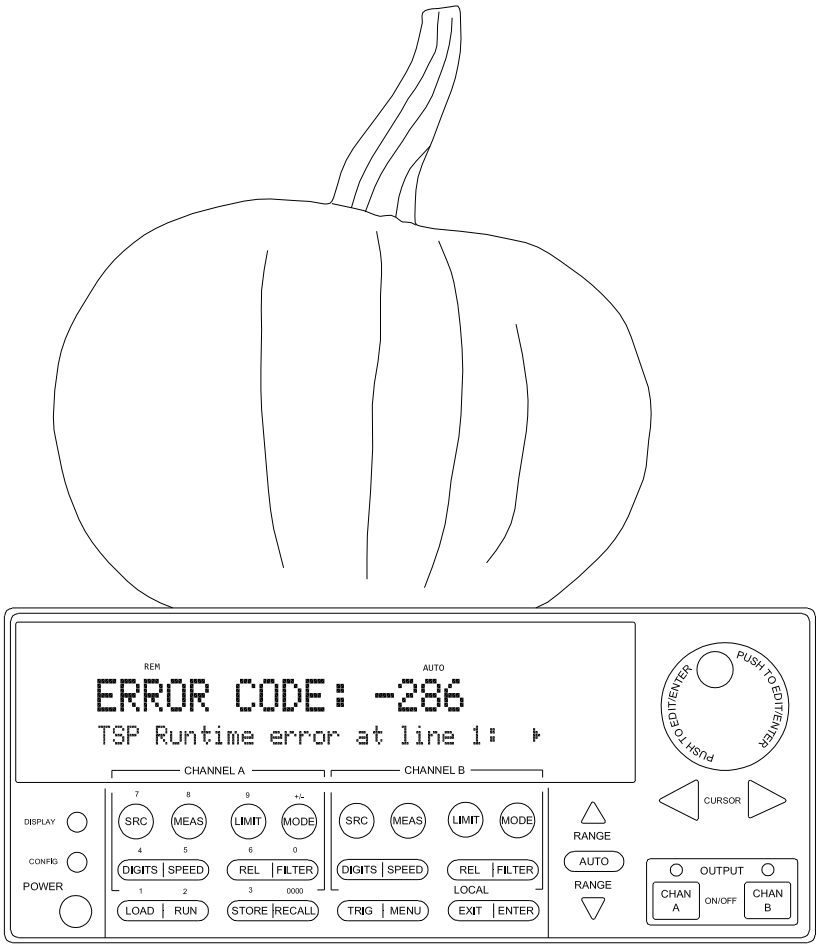
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Chapter 2

Cryogenic Device Characterization and Modeling

The introduction of CMOS in 1959 enabled many new applications that were previously unattainable with discrete components. Due to its power efficiency, high level of integration and maturity, CMOS enabled extreme miniaturization and integration onto a single die. In addition to these benefits over other technologies, CMOS was found to be suitable for operation in harsh environments, exhibiting radiation hardness [1, 2, 3] and the ability to operate at deep cryogenic temperatures, apparent from Fig. 1.

Interest in ultra-low temperature electronics is found in different niche areas. Electronics required to operate in space, for example, are subject to temperatures lying outside of the military temperature range (-55 to 125 °C) on both sides of this interval [3, 7, 1, 8]. Also here on Earth, observation of very distant objects in the solar system requires instrumentation able to detect signals with a very low signal-to-noise ratio. An approach to build such detectors is to cool them down to cryogenic temperatures in order to reduce their thermal noise [9]. Other applications for low-temperature electronics are found in experimental physics for sensors and sensor readout [10].

A relatively new application field for cryo-CMOS circuits is the control and readout of qubits in quantum processors, which is one of the main motivations behind this thesis [11]. As pointed out in Chapter 1, the availability of accurate device models that incorporate cryogenic device behaviour is paramount to ensure reliable circuit operation under these extreme conditions.

Therefore, this chapter starts with a description of the device behaviour of 40-nm bulk MOSFETs operated at deep-cryogenic temperatures, which needs to be

Parts of this chapter have been published in IEEE WOLTE14 [4] and IEEE JEDS [5, 6]

captured in the device models. In order to characterize devices at such low temperatures, special techniques are required, with the ones most commonly used briefly described in the first part of this chapter. The second part of this chapter describes a new modeling approach for the behaviour of 40-nm bulk-CMOS transistors.
This chapter is structured as follows. An overview of the state of the art of cryogenic MOSFET characterization is given in Section 2.1. Techniques for cooling devices to these extreme low temperatures are presented in Section 2.2, after which some of the most important cryogenic MOSFET effects are discussed in detail in Section 2.3. This chapter concludes in Section 2.4 with an Artificial-Neural-Network-based modeling approach of devices in the 40-nm process targeted in this thesis.

2.1 State-of-the-art of Cryogenic Device Characterization

Characterization of CMOS at deep-cryogenic temperatures dates back to the late 1960s [12]. Since that time many different technology nodes, ranging from 100 µm to 14 nm and including bulk, Fully-Depleted Silicon-On-Insulator (FDSOI) and FinFET, have been characterized from room temperature (RT) down to deep-cryogenic temperatures as low as 20 mK.
A graphical overview of these efforts is shown in Fig. 1, in which the technology and type of work (characterized/modeled) are indicated. A large increase in the number of published research in the past couple of years can be seen, mainly due to the renewed interest in cryogenic characterization and modeling fueled by the development of the quantum computer. Fast and complex circuits are required for this application and thus the focus of device characterization and modeling with the quantum computer in mind is geared towards advanced CMOS technologies. The technology targeted in this thesis is a 40-nm one, indicated by a red cross in Fig. 1.
In order to enable the characterization of devices at such low temperatures, dedicated (cryogenic) equipment is required. The most common techniques for cryogenic device characterization will be discussed in the next section.

2.2 Cryogenic Characterization Methods

This section gives a brief overview of three common techniques that enable cryogenic characterization available in the group where this research was carried out. They are presented in order of increasing cooling capability, cycle time, complexity and cost.

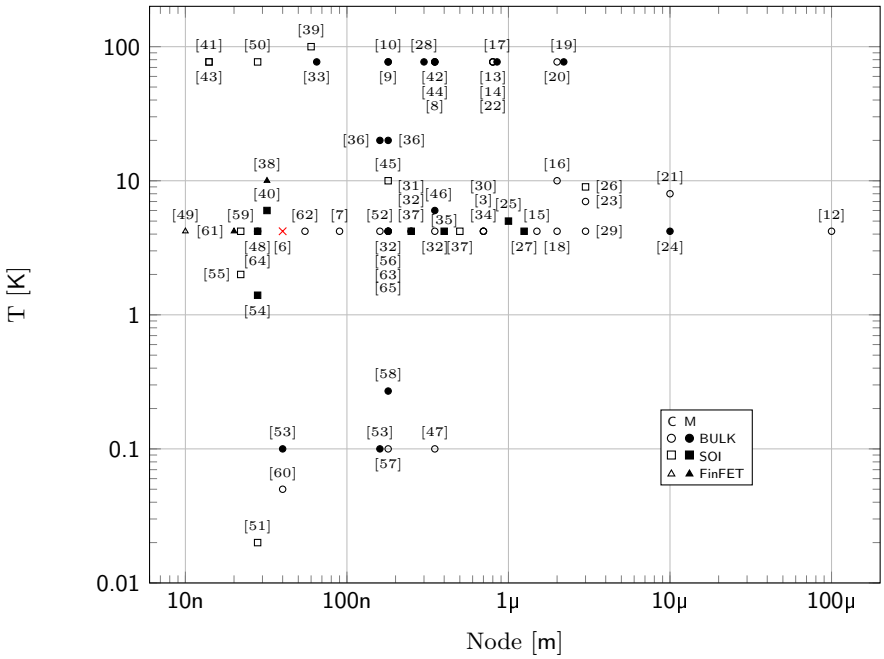

Figure 1: Overview of cryogenic MOSFET characterization (C) and modeling (M). Reference numbers reflect the publication date from oldest (low number) to most recent (high number). The work in this thesis is indicated by a red cross (×).

2.2.1 Dipstick

The dipstick is one of the most simple methods to cool samples down to 4.2 K based on cooling due to liquid helium or vapour. A typical dipstick is illustrated in Fig. 2. It consists of a stainless-steel pipe that carries interconnect wires between the sample holder at the cold end and the connection box at the room-temperature end. An airtight feed-through that mates with a Dewar containing liquid helium, in combination with the connection box, ensure as little helium loss to the environment as possible.

The sample temperature can be modulated in the range between approximately 250 K and 4.2 K by varying the height above the liquid helium level in the Dewar. It is measured by a cryogenic temperature sensor either clamped to the sample package or placed directly above the bare die.

As helium inevitably evaporates during storage, and especially during measurements, the setup is connected to a helium recovery system that collects, filters and re-liquifies the gas so it can be re-used in future experiments.

The samples to be characterized are mounted on a PCB placed in the sample

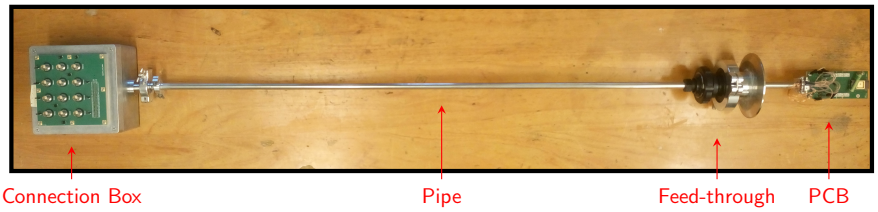

Figure 2: Photograph of the dipstick used in this work. Different parts are indicated.

holder, therefore, the dies need to be either mounted in a package (Ceramic DIP, CLCC, etc.) or glued and wirebonded directly on the PCB itself. This setup is limited to low-frequency characterization, in which no parasitic de-embedding and extensive impedance matching is required.
The main benefits of the dipstick are: it is cheap and can be built anywhere. Also, it allows for a fast cool-down, in the order of 10 minutes, and consumes little helium. Measurements can be taken continuously for 1-2 weeks at cryogenic temperatures without supervision. This is a big advantage, especially when measuring a large number of matched device pairs or large arrays. The cooling power at 4.2 K (when the sample is fully submerged in the liquid helium) lies around 1 W, depending on the geometry of the DUT. At higher power the helium starts to boil around the sample and the thermal contact worsens.
Some drawbacks of this technique are the lack of direct temperature control and temperature stability issues that can arise when the sample is in the helium vapour and the pressure of the recirculation system varies.

2.2.2 Cryogenic Probe Station

The cryogenic probe station solves some of the drawbacks of the dipstick, trading them off against increased cost and cycle time. The probe station shown in Fig. 3 left, consists of a vacuum chamber equipped with a looking glass and micro-meter actuated probe needle arms. A sample holder (chuck) is mounted in the center of the chamber, see Fig. 3 right, which is surrounded by multiple temperature and radiation shields, enabling the chuck to reach cryogenic temperatures by flowing helium through it. The temperature is controlled by integrated heater-diodes in the chuck.
Different types of needles can be mounted on the probe arms, such as DC needles (a single needle) and RF Ground-Signal-Ground (G-S-G) probes. The latter allow for precise impedance matching, required for high-frequency characterization.
One of the main benefits of the cryogenic probe station is the compatibility with on-wafer, high frequency characterization using G-S-G needles and a calibration substrate. Another benefit is the Proportional-Integral-Derivative (PID) temper-

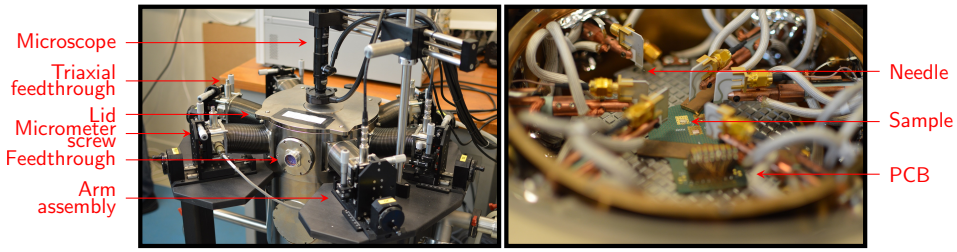

Figure 3: Photograph of the Lakeshore CPX cryogenic probe station used in this work. Different parts are indicated. *Left*: overview of the probestation. *Right*: detailed view of the vacuum chamber with DC needles, sample and chuck visible.

ature control, which can be varied between (theoretically) 1.2 K, by pumping on the helium exhaust, and 400 K.
Drawbacks are its high cost and complexity of operation. The helium consumption is large compared to a dipstick and the probestation can only cool down for a limited amount of time (approximately 7 to 10 h) due to the helium flow through the chuck which evaporates the helium in the Dewar. Moreover, constant supervision is required. The number of needles is typically limited to 6.

2.2.3 Dilution Refrigerator

When sub-Kelvin characterization is required, a dilution refrigerator is the logical choice for the job. A photo of a dilution refrigerator can be found in Fig. 4. It can readily be recognized that these machines require a lot of space and peripherals such as cooling water and high-capacity power connections. Indicated in the figure are the different stages, each with a decreasing temperature moving from top to bottom of the dilution refrigerator. During normal operation the different stages shown in Fig. 4 are enclosed in metal cans brought under high vacuum. The exact theory of operation of these refrigerators lies beyond the scope of this thesis, however, in short the operation relies on the dilution of He^3 with He^4, which is an endothermic process and thus removes heat from the fridge. The coldest part of the dilution fridge, the "cold finger" all the way at the bottom, can reach temperatures as low as 10 mK and has a cooling power of several µW at this temperature. The main benefit of the dilution refrigerator is its ability to cool samples to temperatures as low as 10 mK, a temperature unattainable with the other methods described above.
The main drawbacks are the cost, complexity (both in operation and experimental setup), the space it consumes and the cycle times, which lie in the order of a

week. The wiring can be complex and unreliable and is also limited in terms of connections. Also, the cooling power at the lowest temperatures is very limited, restricting characterizations to bias regimes that do not exceed that power budget.

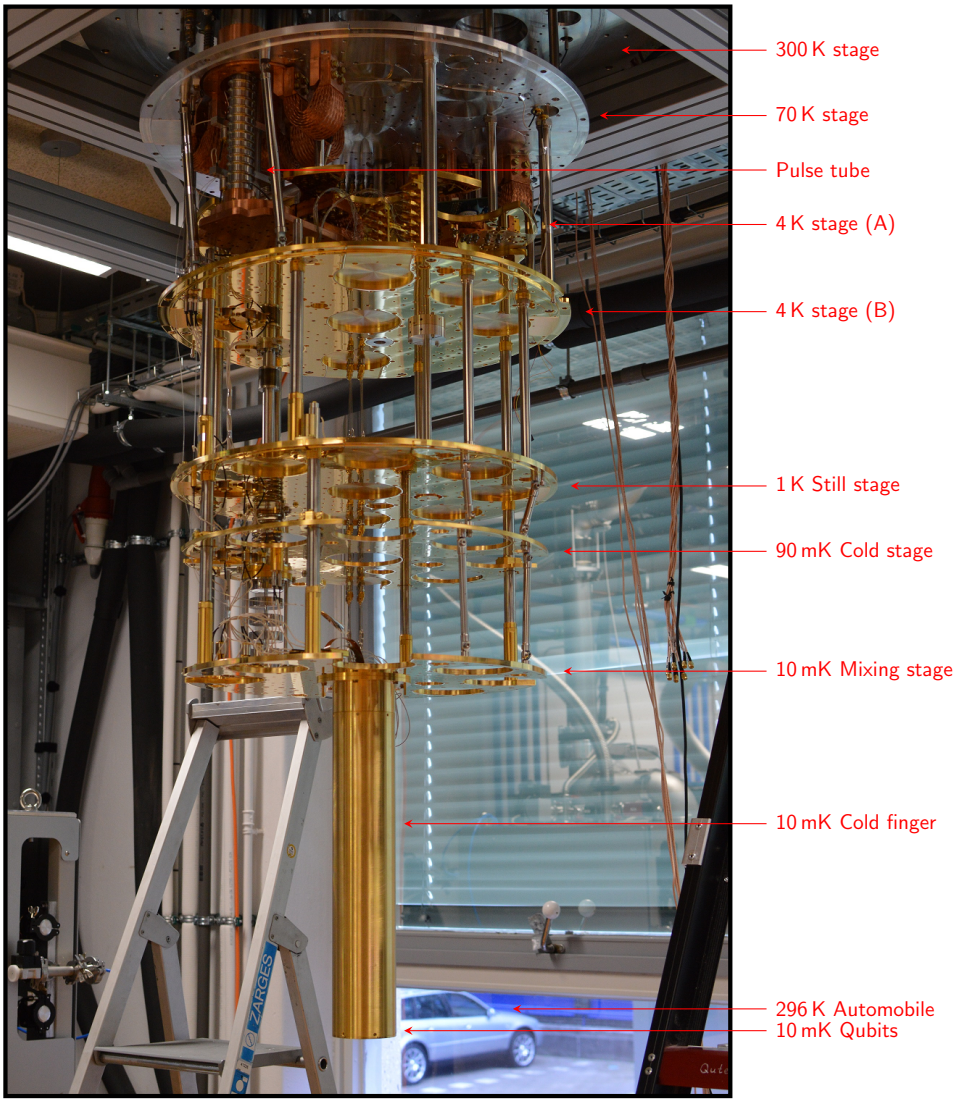

Figure 4: Photograph of an opened Bluefors XLD dilution refrigerator used in QuTech. The most important parts and their respective operating temperature are indicated.

2.3 Cryogenic MOSFET Behaviour

The first step towards device models able to accurately predict behaviour from RT down to deep-cryogenic temperatures, is the electrical characterization of devices over this temperature range. Many works have been published investigating MOSFET behaviour in different technologies at cryogenic temperatures as indicated in Fig. 1.

The most important curves in DC-MOSFET characterization are the drain current as a function of drain-source voltage (I_D-V_D curves) and drain current as a function of the gate-source voltage (I_D-V_G curves) shown in Fig. 5 and Fig. 6/7, respectively. The importance of accurate measurement of the drain current at different biases over temperature is immediately apparent, as many aspects of these curves change when deep-cryogenic temperatures are approached. For example, an increase in threshold voltage and mobility are both highlighted in Fig. 8, the former marked by a translation of the I_D-V_G curve along the V_{GS} axis and the latter by a multiplicative factor increasing the drain current for high V_{GS}, respectively.

The increased drain current at high $|V_{GS}|$ in Fig. 8 is related to the competing cryogenic effects of the threshold voltage and mobility increase. The improved mobility directly translates into an increased drain current, while the V_{TH} increase combats this effect by lowering the drain current, but to a lesser degree as seen in Fig. 8.

An interesting phenomenon, related to the interplay of the temperature sensitivity of the mobility and threshold voltage, is the Zero-Temperature-Coefficient (ZTC) bias point [66], indicated in Fig. 8. Depending on the operating regime, either V_{TH} (in moderate inversion) or β (in strong inversion) dominate the drain-current behaviour over temperature, and the cross-over point, where the two effects cancel each other out, is approximately temperature insensitive. Circuits exist that employ this bias point in order to generate a stable current/voltage reference over a wide temperature range [67].

The temperature sensitivity of the subthreshold slope SS can be observed in Fig. 8 by plotting the drain current on semi-logarithmic axes, the slope becoming steeper with decreasing temperatures.

From the measured drain-current data, the important modeling parameters previously mentioned can be extracted at different temperatures. A short description of their meaning, the method employed for their extraction and their behaviour over temperature is discussed in the following paragraphs.

2.3.1 Threshold Voltage

The threshold voltage V_{TH} is the V_{GS} value that marks the onset of significant drain-current flow, and is one of the core parameters of compact MOSFET models. The threshold voltage was extracted using the Extrapolation-in-Linear-Region method (ELR) [68] throughout this thesis, for its simplicity and its successful ap-

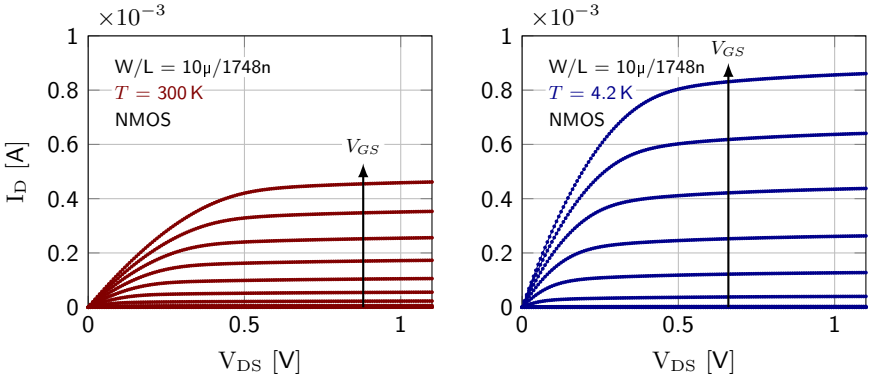

Figure 5: Typical I_D as a function of V_{DS} (I_D-V_D) curves for a 40-nm process characterized at room and cryogenic temperature. $V_{GS} = \{0, 0.1, 0.2, ..., 1.1\}$ V

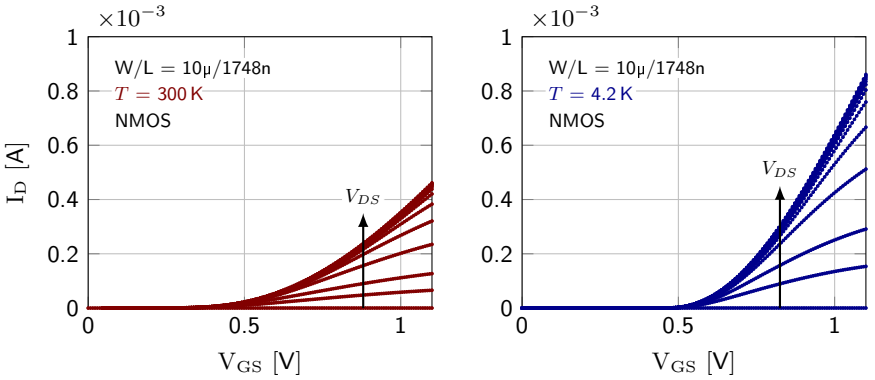

Figure 6: Typical I_D as a function of V_{GS} (I_D-V_G) curves for a 40-nm process characterized at room and cryogenic temperature (lin scale). $V_{DS} = \{0, 0.05, 0.1, 0.2, ..., 1.1\}$ V

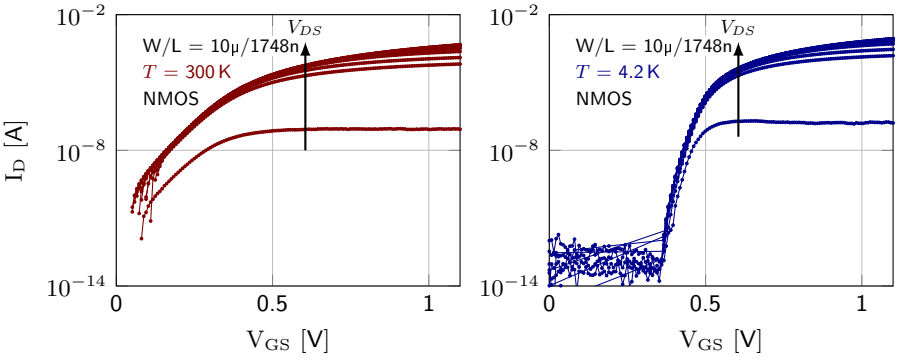

Figure 7: Typical I_D as a function of V_{GS} (I_D-V_G) curves for a 40-nm process characterized at room and cryogenic temperature (log scale). $V_{DS} = \{0, 0.05, 0.1, 0.2, ..., 1.1\}$ V

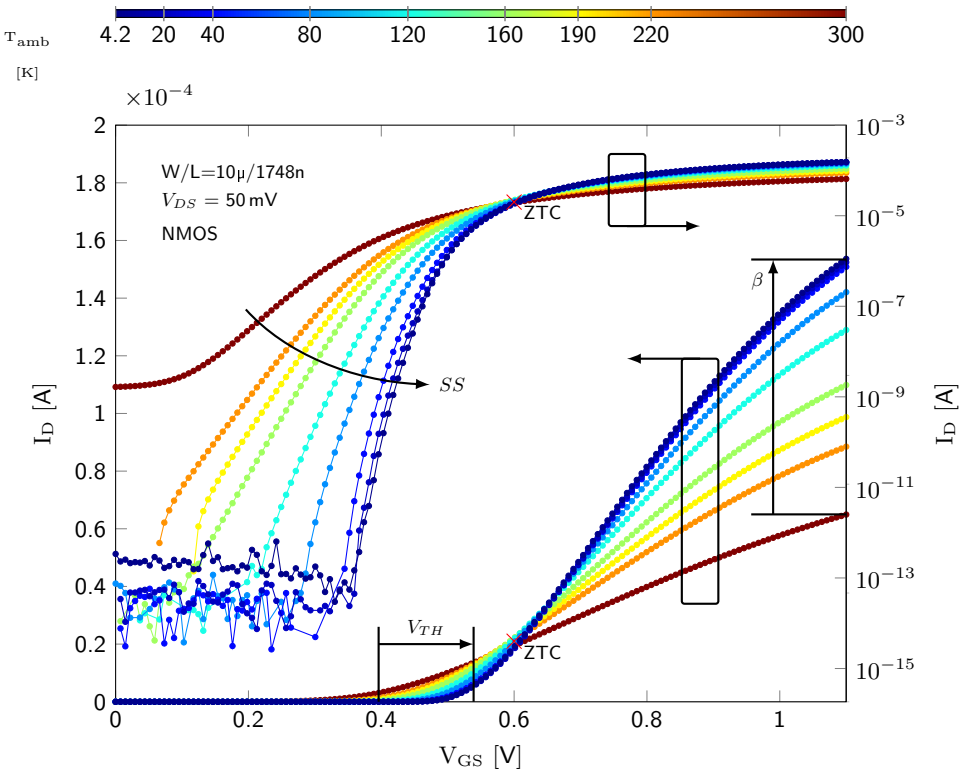

Figure 8: I_D vs V_{GS} (I_D-V_G) behaviour of a 40-nm process biased at $V_{DS} = 50\,\text{mV}$ as a function of temperature. The most important parameter shifts and the Zero Temperature Coefficient (ZTC) point are indicated by arrows and a red cross, respectively. $T = \{4.2, 20, 40, 80, 120, 160, 190, 220, 300\}$ K.

plicability in the mismatch study presented in Chapter 3.
The ELR method is based on the long-channel linear equation:

$$I_D = \beta \left((V_{GS} - V_{TH})\, V_{DS} - \frac{V_{DS}^2}{2} \right), \tag{2.1}$$

where β is the current factor ($\beta = \mu C_{OX} W/L$, with μ the carrier mobility, C_{OX} the gate-oxide capacitance and W and L the width and length of the MOSFET, respectively) and V_{TH} the threshold voltage. The threshold voltage is extracted by applying a first-order fit to the I_D-V_G data at the point of maximum transconductance, as shown in Fig. 9 left. The value of V_{TH} is found from the intercept

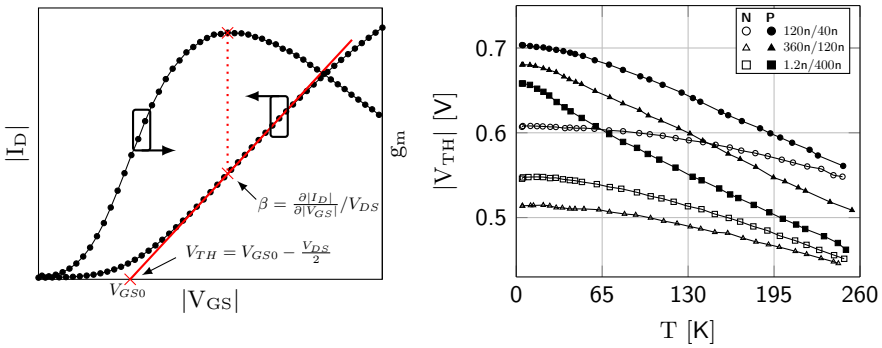

Figure 9: Threshold voltage extraction and behaviour. *Left*: schematic representation of the ELR threshold voltage extraction method. The capture of V_{TH} and β is indicated. *Right*: Extracted V_{TH} as a function of temperature for NMOS (N) and PMOS (P) device types and geometries.

with the V_{GS} axis by setting Eq. 2.1 equal to zero:

$$V_{TH} = V_{GS0} - \frac{V_{DS}}{2}. \tag{2.2}$$

The behaviour of the threshold voltage from RT down to 4.2 K of PMOS and NMOS devices with different geometries can be seen in Fig. 9 right, which shows a linear increase down to a temperature of 50 K, below which the threshold voltage starts to saturate. These curves are compatible with those found and modeled by other groups [46, 69]. Different explanations are given for the increase and saturation at deep cryogenic temperatures. In [46], the saturation is explained by carrier freeze-out and field-assisted ionization while [69] attributes these effects to the temperature dependence of the bulk Fermi potential and interface traps close to the band edge.
The implications of an increased threshold voltage for circuit design is a reduced headroom, complicating designs that employ techniques such as cascoding, requiring an increased V_{DD}. Although a higher threshold voltage in combination with the increased SS reduces static leakage on one hand, and thus power consumption in digital designs, it limits the operating speed on the other.

2.3.2 Mobility

A second important parameter in MOSFET compact models is the carrier mobility μ. In this thesis the exact value of the mobility is not extracted, as the current factor (β) can be directly extracted from measured data and it is β that is relevant for the mismatch modeling presented in Chapter 3. However, the extracted current

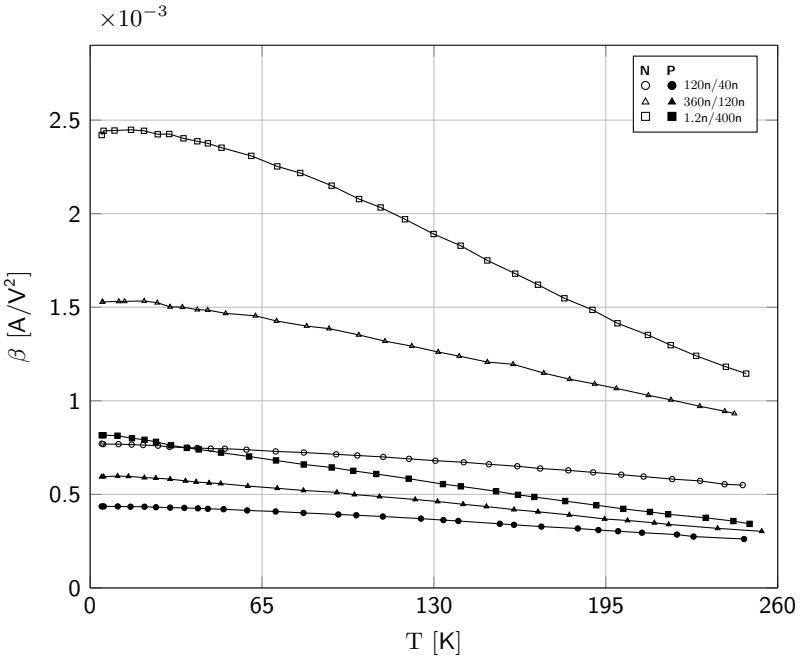

Figure 10: Current factor (β) as a function of temperature for NMOS (N) and PMOS (P) device types and geometries.

factor can still be used to study mobility as it is proportional to β:

$$\beta = \mu C_{OX} W/L, \tag{2.3}$$

in which μ represents the carrier mobility, C_{OX} the gate-oxide capacitance and W and L the width and length of the device, respectively. The latter three parameters are assumed to have negligible temperature dependence compared to μ.
The current factor is extracted from the slope of the first order fit of the I_D-V_G curve at maximum transconductance, see Fig. 9 left, the same fit employed for extraction of the threshold voltage in the previous paragraph:

$$\beta = \frac{\partial I_D}{\partial V_{GS}} / V_{DS}. \tag{2.4}$$

The behaviour of the current factor over the temperature range from RT down to 4.2 K for PMOS and NMOS devices of different sizes can be seen in Fig. 10. The mobility increase with temperature reduction is apparent with a saturating behaviour resembling that observed in the plots of the threshold voltage (Fig. 9) and subthreshold slope (Fig. 11).

The mobility improves down to a temperature of 40 K due to reduced phonon (lattice) scattering, below which Coulomb (impurity) scattering starts to dominate [70], similar to the impurity-limited resistance of metals at cryogenic temperatures, discussed in Section 4.4. Short devices exhibit a lower temperature dependence of β, as the halo implant increases the effective channel doping, reducing its temperature sensitivity [71].
From a circuit design perspective, the improved mobility observed at low temperatures results in more drain current for an equal overdrive compared to room temperature, resulting in faster switching.

2.3.3 Subthreshold Slope

The subthreshold slope SS is an important factor in low-power designs. Its inverse, the subthreshold swing, is defined as the V_{GS} increase required to raise the drain current by a decade for devices biased with V_{GS} below the threshold voltage. A steep subthreshold slope is preferred, as the MOSFET behaviour approaches the model of an ideal switch under this condition: a low-leakage "off" state and high-current "on" state selectable by a small change in V_{GS}, the latter enabling high switching speeds.
The carrier flow of MOSFETs biased in the subthreshold regime is diffusion-current driven and exponential in nature:

$$I_D \propto \exp\left(\frac{q(V_{GS} - V_{TH})}{nk_BT}\right), \tag{2.5}$$

with n the slope factor, k_B the Boltzmann constant, T the absolute temperature and q the electron charge.
The exponential regime can be clearly recognized in the I_D-V_G plot shown in Fig. 8. The subthreshold slope is extracted by finding the slope of a first-order fit in this regime:

$$SS = \frac{\partial V_{GS}}{\partial \log(I_D)}. \tag{2.6}$$

Combining Eq. 2.5 and Eq. 2.6 yields an expression for the theoretical subthreshold slope as a function of temperature:

$$SS(T) = \ln(10)\frac{nk_BT}{q}. \tag{2.7}$$

From Eq. 2.7, the subthreshold slope is expected to linearly improve with decreasing temperature, from a value around 60 mV/dec at RT to below 1 mV/dec at a temperature of 4.2 K. The extracted subthreshold slope as a function of temperature for NMOS devices with different geometries is shown in Fig. 11. The subthreshold slope exhibits the predicted linear behaviour down to 70 K, below which it starts to saturate to a value close to 20 mV/dec. The deviation from the

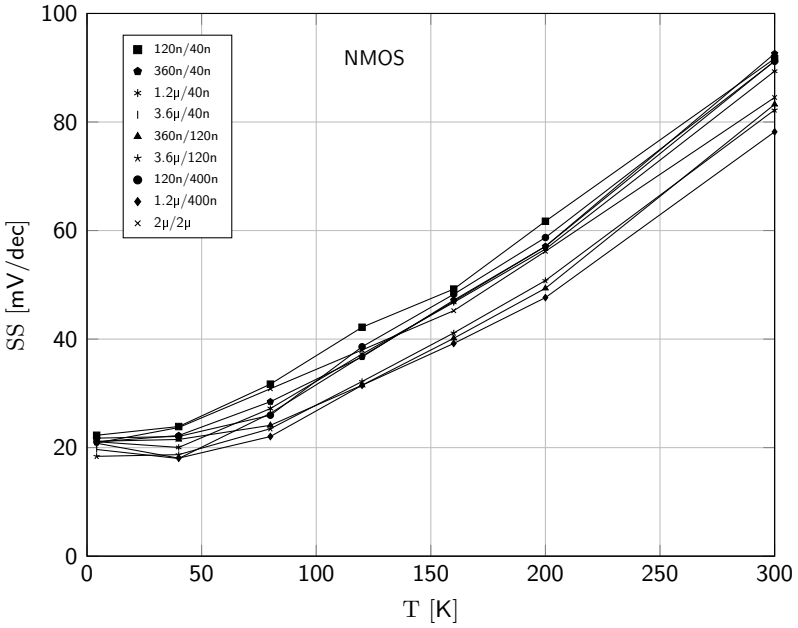

Figure 11: Subthreshold slope as a function of temperature for NMOS devices of different geometries.

model in Eq. 2.7 is in line with results found by others [15, 72, 53]. It was recognized by [72] that this saturation seems to be universally observed, irrespective of the device size or used technology (bulk, FDSOI, FinFET, etc.), which points to an intrinsic mechanism responsible for this effect. The subthreshold slope behaviour over temperature was successfully explained and modeled by taking the presence of band-tails into consideration [72], showing that in these cases an ideal switch cannot be obtained, even at deep-cryogenic temperatures.
For circuit designers, the steeper subthreshold slope at cryogenic temperatures means a more ideal switching behaviour of the devices. However, due to the saturation, much less improvement is actually gained if Eq. 2.7 is used as predictor. Analog designs can suffer from additional non-ideal subthreshold behaviour that perturbates the ideal exponential I-V relationship. These and other subthreshold effects are discussed in more detail in Chapter 3.

2.3.4 Kink Effect

The kink effect is the name given to the sudden jump in drain current observed in the saturation region of (in this case) MOSFETs, as shown in Fig. 12. The effect

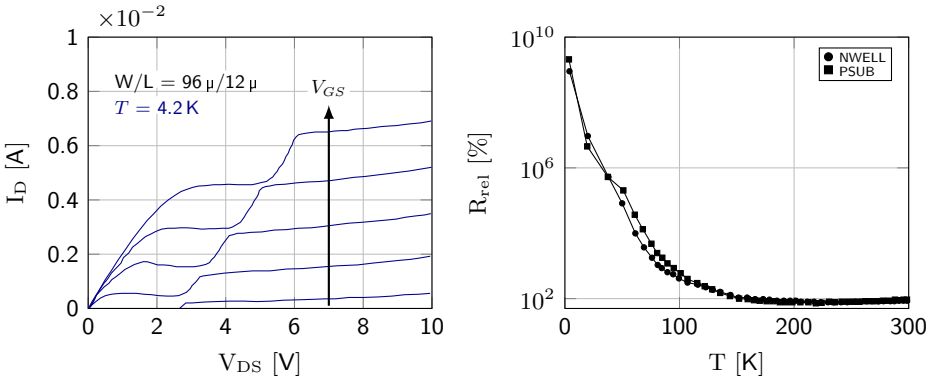

Figure 12: The kink-effect. *Left*: a typical example of the kink effect at cryogenic temperatures of a 3-µm technology, replotted from [73]. $V_{GS} = \{1, 2, ..., 5\}$ V. *Right*: the NWELL and PSUB resistance relative to its room temperature value as function of temperature of a 40-nm technology, replotted from [74].

presents itself only in mature technologies (feature size of 0.35 µm and above) operated at deep-cryogenic temperatures. It is also observed at RT in SOI technologies or when, for example, the substrate connection is severed in bulk devices. The occurrence of the kink has been known for many years and the first explanations date back to the early 1990s [73]. As V_{DS} is increased, the horizontal electric field in the channel exceeds a critical value at a certain point, at which charge carriers attain enough energy to create additional "excess" electron-hole pairs through impact ionization, see Fig. 13 left, which marks the onset of the kink as explained next. These excess carriers leave the device through the drain and source, respectively, and add to the main current. However, a fraction of the minority excess carriers flow through the substrate impedance. The voltage dropped over this impedance raises the local substrate potential in the vicinity of the channel, lowering the threshold voltage through the body effect and increases suddenly the drain current of the device. The kink saturates as V_{DS} is further increased, as the parasitic bulk-source diode becomes forward biased, diverting the substrate current, effectively clamping the substrate potential.
At RT, the substrate impedance is low and the modulation of the substrate potential near the channel by the substrate current is negligible. However, at low temperatures the substrate impedance increases dramatically as shown in Fig. 12 right. When the substrate starts to freeze-out at temperatures below 100 K, the effect of the substrate current becomes apparent.
The onset of the kink shifts to higher V_{DS} values with increasing V_{GS} as visible in Fig. 12 left. On one hand, the vertical electrical field in the channel increases with V_{GS}, increasing effects such as surface scattering which reduces carrier mobility. For carriers to attain enough energy for impact-ionization, a higher horizontal field

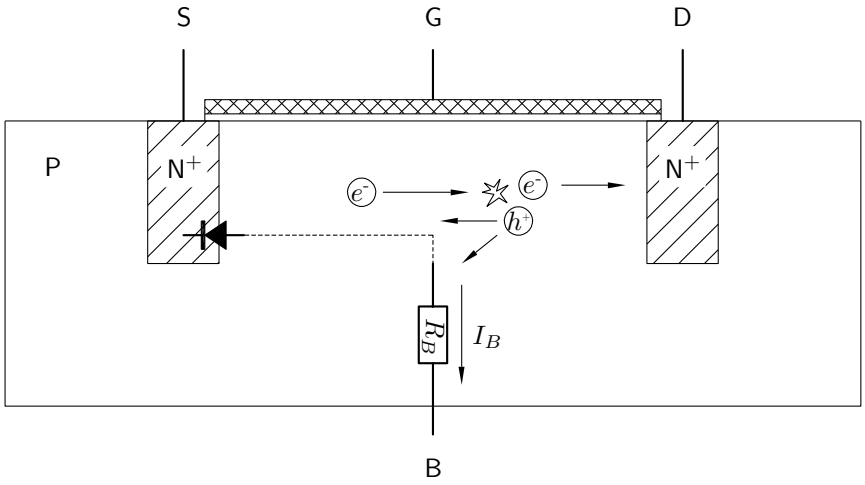

Figure 13: A schematic representation of the mechanism behind the kink-effect.

(V_{DS}) is thus required. On the other hand, this horizontal field reduces at higher V_{GS} by the increased distance between the pinch-off point and the drain.
The kink effect is mainly a problem in mature bulk technologies and is not observed in technologies with feature size below 0.35 µm. The effect is absent in these technologies due to the increased vertical field driven by geometrical scaling, which impedes impact ionization as discussed above. The formation of electron-hole pairs is further supressed by the scaling of the supply voltages. The kink effect has not been observed in the 40-nm processes characterized in this thesis and is thus not further discussed.

2.3.5 AC Behaviour

Although this thesis focuses on DC device characteristics, the ability to simulate dynamic behaviour in circuits is required and therefore the impact of low temperatures on RF characteristics are of interest. Some important parameters are summarized in this paragraph.
For example, the current-gain cutoff frequency f_T continuously improves with decreasing temperature, up to a factor of approximately 1.6 in nanometer bulk CMOS RF circuits operated at 4.2 K compared to those at 300 K [7]. The maximum oscillation frequency f_{max} improves down to 50 K, below which it flattens-out due to the saturation of the gate resistance (see also Chapter 4) which is the main parameter that determines f_{max} [7].

2.3.6 Noise

One of the reasons for cooling down sensitive circuits is to reduce their noise, a technique applied in, for example, circuits such as detectors/sensors for space observation. Thermal noise decreases dramatically when the ambient temperature is lowered from 300 K down to 4.2 K, however, a smaller noise reduction than the expected proportional decrease with temperature is found at cryogenic temperatures. This noise saturation has been attributed to shot noise starting to dominate at cryogenic temperatures [75, 76]. This excess noise requires more power to be burned in order to reach a certain specification, causing challenges in applications where power budgets are severely limited such as those cooled by dilution refrigerators. Another potential effect that can severely impact the noise performance of circuits is self-heating, extensively discussed in Chapter 4. Here it is shown that the channel temperatures in bulk CMOS devices can rise to up to 50 K (while in an ambient temperature of 4.2 K) already at low power levels ($<$1 mW), thus increasing thermal noise.

2.3.7 Device Mismatch

Device mismatch is the effect parameter variability (such as $\sigma_{\Delta V_T}$, $\sigma_{\Delta\beta/\beta}$ and $\sigma_{\Delta SS/SS}$) has on pairs of supposedly identical devices. It invalidates the assumption of perfectly matched devices, which many precision circuits base their operation on, necessitating the application of many circuit techniques to alleviate this problem. These techniques often result in designs requiring more silicon area and/or operate with increased power dissipation compared to the original design. Previous research (see Chapter 3) hints at an increased device mismatch at cryogenic temperatures, indicating a possible challenge for cryogenic high-precision circuit design. An in-depth study of device mismatch and the evaluation of the effectivity of dummy placement at deep-cryogenic temperatures is presented in Chapter 3.

2.3.8 Self-Heating

Self-heating occurs in (resistive) devices carrying an electric current, causing a local temperature increase due to Joule heating. As many device parameters exhibit a high temperature sensitivity, many undesired circuit effects can result, such as shifting of bias regimes, electro-thermal feedback loops and thermal runaway, i.e. a temperature rise that results in increased current, resulting in even more self heating, ultimately destroying the device.
Prior research (see Chapter 4) indicates a self-heating exacerbated at deep-cryogenic temperatures, with all its associated problems and challenges for cryogenic circuit design. Self-heating at cryogenic temperatures has therefore been extensively investigated, the methods and results presented in Chapter 4.

2.4 Cryogenic 40-nm MOSFET Modeling

Cryogenic device models are indispensable for the reliable design of circuits for cryogenic operation, as pointed out in Chapter 1. Device behaviour at these low temperatures can be quite different from its room temperature equivalent, caused by the large temperature sensitivity of device parameters, the most important ones discussed in the preceding paragraphs.
Much effort has already been devoted to the characterization and modeling of MOSFETs operated at cryogenic temperatures in many different technologies and feature sizes, see Section 2.1 (in particular Fig. 1), and the physics of cryo-CMOS devices is mostly understood [53, 77].
Despite all this work, there is not yet a consensus on a standard cryo-CMOS model, and it is unclear whether existing model extraction procedures can be effectively applied to cryogenic characteristics. As an alternative, the use of an Artificial Neural Network (ANN) and associated training (extraction) techniques is here proposed in collaboration with Keysight Technologies, to automatically construct cryo-CMOS simulation models without requiring any physics-based device model [78]. ANNs only require a discrete set of experimental data, e.g., $I_D = f(V_{GS}, V_{DS}, W, L, T)$ for a limited set of bias points. Since those data can be scattered (sampled without any gridding constraints over T, W, L and bias), significant cryogenic characterization effort can be saved. From these data, the ANNs that are automatically generated provide infinitely differentiable functions describing the device nonlinear current/voltage and charge/voltage relations, hence are well-suited for accurate analog-circuit simulations.
This section explores the potential of ANN models for cryo-CMOS devices by applying such modeling methodology to experimental data. After describing the basics of the ANN modeling flow for both the static and dynamic characteristics in Section 2.4.1, the measurement setup and test structures are presented in Section 2.4.2. Section 2.4.3 assesses the quality of the proposed model for a large number of cryo-CMOS devices. The performance of those models in predicting the behaviour of practical circuits is then benchmarked by comparing the simulations using the proposed models with the experimental data for a static circuit and with simulations using the foundry-provided model for a dynamic circuit, respectively.

2.4.1 ANN-based Modeling for Cryo-CMOS

ANNs are a powerful computational paradigm inspired by the human nervous system [79]. They have become mainstream tools of the artificial intelligence and machine learning communities. The Universal Approximation Theorem [79] proves that an ANN with at least one hidden layer with a sufficient number of univariate processing functions, or neurons, can arbitrarily fit any nonlinear function of any number of independent variables. ANN training is an automatic process of adjusting the internal weights and biases (parameters) of the ANN to enable the model

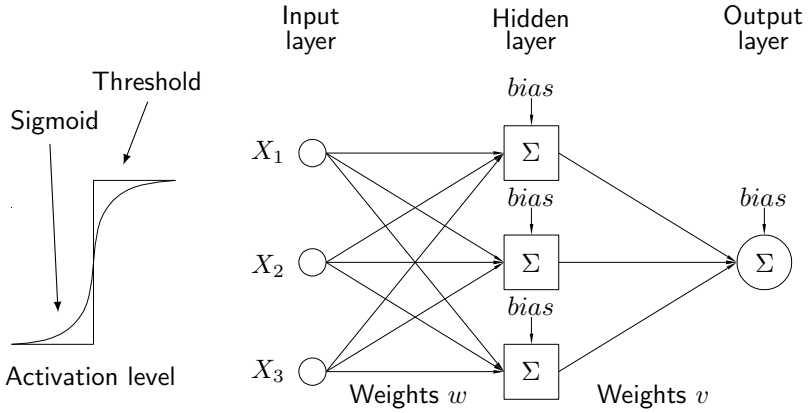

Figure 14: Schematic overview of the ANN structure illustrating the ANN layer structure and a plot of typical univariate neuron nonlinearity (sigmoid and threshold functions).

to match the training data. A typical single hidden layer structure is shown in Fig. 14, along with a plot of a typical univariate neuron nonlinearity, or threshold function. Mathematically this ANN can be represented by the following equation:

$$F(X_1, ..., X_N) = \sum_{i=1}^{L} v_i s \left(\sum_{k=1}^{N} w_{ki} x_k + a_i \right) + b_i, \tag{2.8}$$

in which v_i and w_{ki} are the weights, s the Sigmoid function and a_i and b_i are the biases.

Applying ANNs to device modeling is advantageous as there are no equation development or user-defined parameter extraction processes needed. The general modeling flow is shown in Fig. 15. Given the measured data, e.g., drain current from sampled bias points and over a wide range of temperatures and geometries (W/L), an ANN model is automatically trained (constructed).

Unlike drain currents that can be directly measured at different bias conditions and used to train ANN functions with standard techniques to produce voltage-controlled current source elements, the charge stored by device bias-dependent capacitances cannot be directly measured. Instead, the nonlinear charge functions (modeled by voltage-controlled nonlinear capacitors) can be generated by training ANNs to simultaneously fit the partial derivatives of the desired charge functions to bias-dependent capacitances (e.g. C_{GG} and C_{GD}) that can be obtained from S-parameter data [80]. This requires a unique kind of automated "Adjoint training" [78] that essentially performs line-integration of measured data and is illustrated in Fig. 16. This approach is generally superior to a direct numerical line-integration approach for several reasons, as described in [81]. The implementation in this work, however, ignores the effect of independently biasing internal

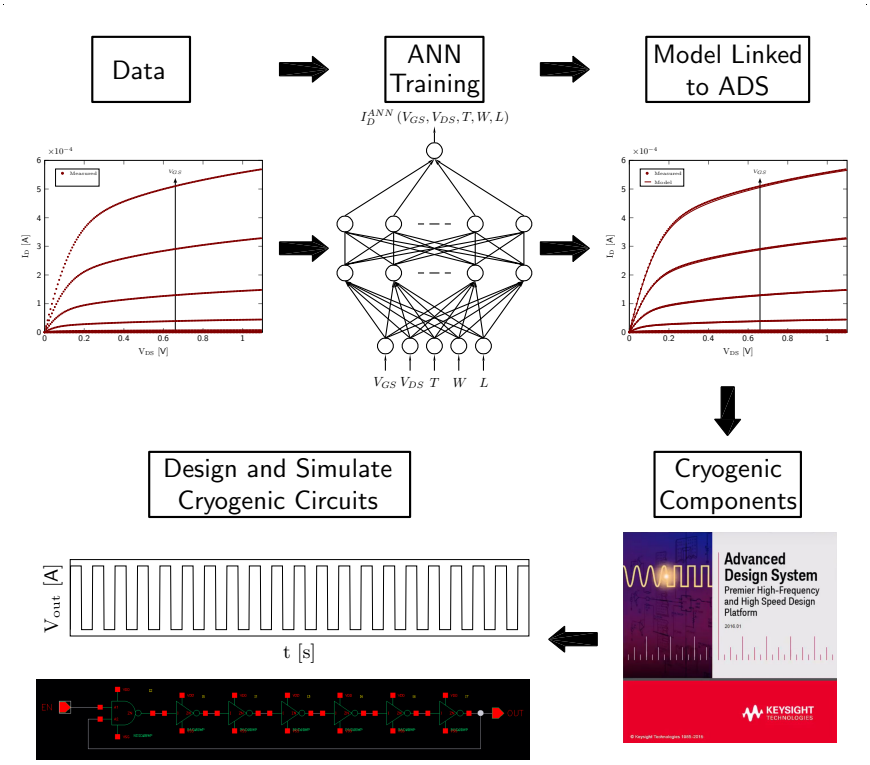

Figure 15: Modeling flow: Given the measured data, an ANN model is automatically trained (constructed). The trained model is easily linked to a circuit simulator, for high-level circuit simulation and design.

nodes (e.g. the bulk node), and effectively treats the device as having two independent terminal voltages, drain-source (V_{DS}) and gate-source (V_{GS}) voltages, assuming the bulk node to be tied to the source.

2.4.2 Characterization Structures and Measurement Setup

In order to measure $I_D = f(V_{GS}, V_{DS}, W, L, T)$ for many different geometries, device types (PMOS, NMOS), bias points and temperatures as training set for the ANN, dedicated test structures have been designed and manufactured in the TSMC 40-nm bulk CMOS process. Two test structures were available, one for NMOS types and one for PMOS types, each comprising an array of 400 devices with different device geometries ranging from minimum (W=120 nm, L=40 nm)

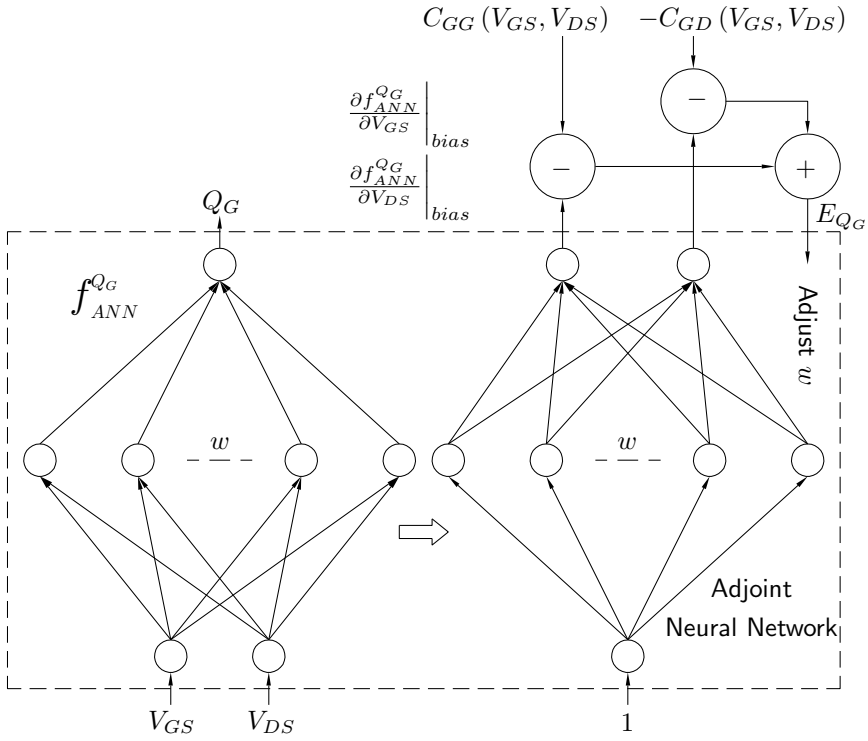

Figure 16: Adjoint ANN training of the model gate terminal charge function from C_{GG} and $-C_{GD}$ data. The Adjoint training method utilizes a more complicated ANN network, but ultimately returns an ANN model for the terminal charge Q_G (this figure) and similarly for Q_D, the drain charge, assuming a three-terminal device structure with the bulk node shorted to the source.

to large size (W=10 µm, L=10 µm), graphically summarized in Fig. 17 left. A diagram indicating the electrical connections and a chip micrograph can be found in Fig. 17 right and Fig. 18, respectively. All devices in the array share their drain and source connection, both wired in a Kelvin fashion to mitigate the effect of parasitic wire/interconnect resistance. Each device is individually selectable by connecting its gate to a common gate line through a pass gate controlled by a digital shift register, while all the other devices are shut off by connecting their gates to either V_{SS} or V_{DD} for NMOS or PMOS devices, respectively. The device bulk connection is tied to the appropriate rail.

The test dies were mounted in a Ceramic DIP (CERDIP) package, placed on a PCB at the end of a dipstick, as shown in Fig. 18. A set of relays allowed selection of either the NMOS of the PMOS array to mitigate undesired effects such

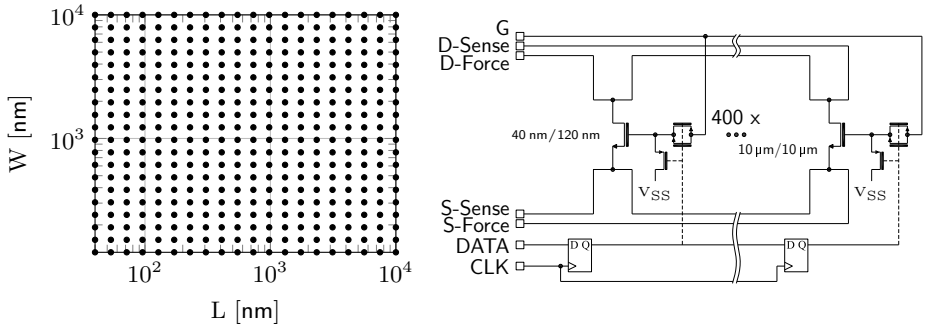

Figure 17: Test chip. *Left*: the available W/L combinations for both PMOS and NMOS devices. *Right*: schematic representation of the internal electrical connections to the NMOS array.

as leakage. The chip temperature was monitored by a Cernox temperature sensor brought in close thermal contact to the CERDIP package.
The electrical characterization was carried out by two Keithley 2636B Source Measurement Units (SMUs), measuring the drain current while sweeping both V_{GS} and V_{DS} over the range from 0 V to the nominal supply voltage ($V_{DD} = 1.1$ V), with V_S fixed at the bulk potential.
Although the data was acquired on a regular grid for V_{DS} and V_{GS}, this is not strictly necessary for the ANN training. For instance, the W and L of the 400 geometries are not linearly, but logarithmically scaled from 40 nm to 10 µm, in order to sample the region closer to the minimum size more accurately, since those devices are more relevant for circuit design and more significant variations in their electrical behaviour are expected.

2.4.3 Measurement Results and Model Validation

The ANN model was trained over the drain current data measured at 4.2 K, 100 K and 300 K, over a bias grid of 12 V_{DS} values by 151 V_{GS} values, and for the 400 geometries to learn the constitutive relation $I_D = f(V_{DS}, V_{GS}, W, L, T)$. The training required 24 hours on a 4-core intel i7 workstation with 32-GB RAM. The resulting model fitted the measured DC characteristics within a 1% RMS error.
Examples from a few selected devices and temperatures are shown in Fig. 19 and 20, demonstrating the quality and applicability of the resulting models.
To assess the ability of the ANN to model dynamic behaviour, a dynamic ANN model based on the quasi-static approach described in Section 2.4.1 was generated from S-parameters obtained from simulations using the foundry-provided models at 300 K (the foundry models are not valid at 4.2 K) and measured I-V data. These models were then benchmarked by simulating a 500 MHz inverter-based ring

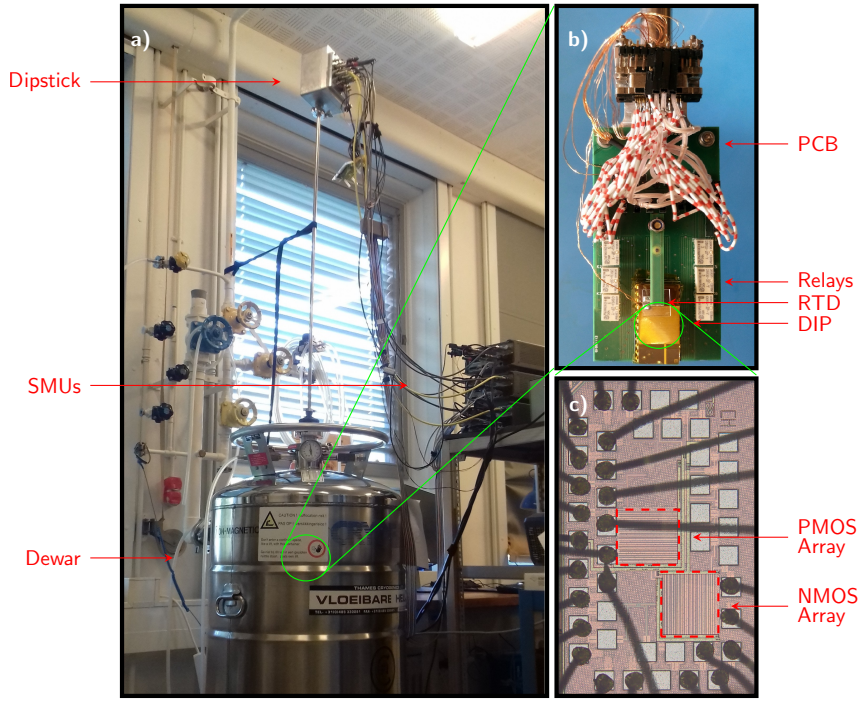

Figure 18: The measurement setup. a) Overview of the full dipstick setup. b) Detailed photograph of the PCB holding the sample. c) Die micrograph of the test chip.

oscillator employing 142 digital inverters and a NAND gate for start up. Although the dynamic model is limited to 300 K due to the present lack of measured cryogenic S-parameters, the oscillation frequency predicted by the ANN models for 300 K (525 MHz) accurately matched (within 6%) the predictions of the foundry-provided models (559 MHz).

2.4.4 Conclusion

These results demonstrate the utility of automatically generated ANN models for cryo-CMOS applications. By avoiding developing specific physics-based models and minimizing the required characterization data, the proposed modeling approach can significantly accelerate the development of the complex cryo-CMOS electrical interfaces for future large-scale quantum processors.

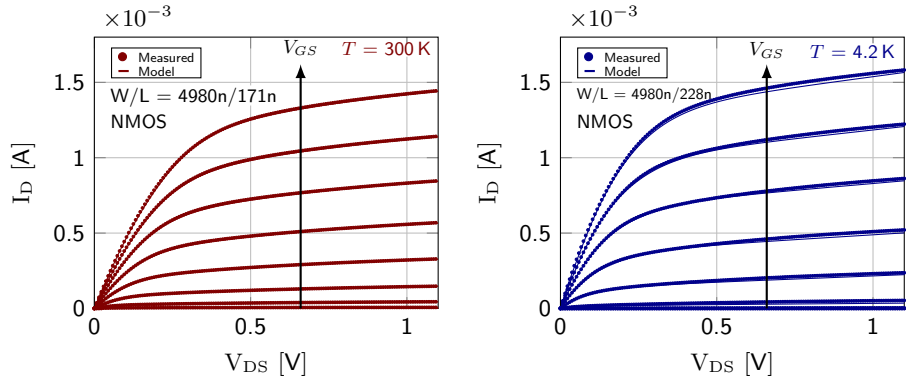

Figure 19: Measurements vs model: I_D-V_D plots of an NMOS device at room and cryogenic temperature, showing both measured data and the models generated by the ANN modeling flow. $V_{GS} = \{0, 0.1, 0.2, ..., 1.1\}$ V.

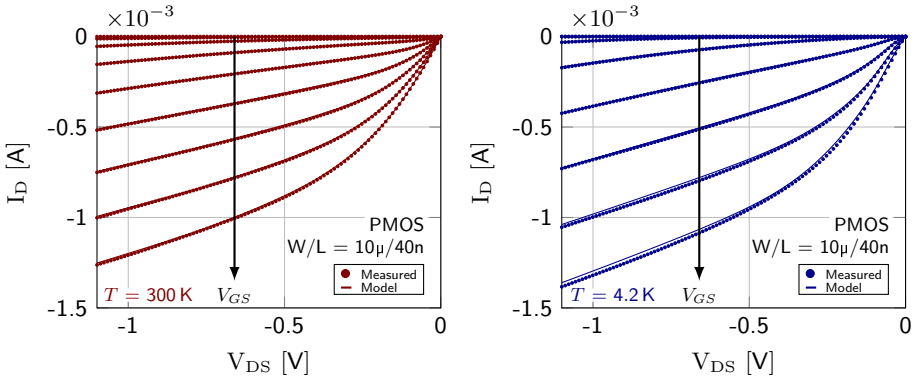

Figure 20: Measurements vs model: I_D-V_D plots of a PMOS device at room and cryogenic temperature, showing both measured data and the models generated by the ANN modeling flow. $|V_{GS}| = \{0, 0.1, 0.2, ..., 1.1\}$ V.

2.5 Conclusions

In this Chapter, an overview of previous cryogenic characterization and modeling efforts was presented, from which it can be concluded that the recent developments around quantum computing sparked a new interest in this niche field. Three common techniques that enable electrical characterization of test chips at temperatures as low as 100 mK were presented, highlighting both the benefits and drawbacks of each method.

Devices operated at these extreme low temperatures exhibit behaviour that can

deviate significantly from those observed at room temperature. The effect of temperature on the most important parameters that govern the cryogenic operation of MOSFETs, such as the threshold voltage, mobility and subthreshold slope, have been shown from experimental data and some background on the underlying physical mechanisms was given.
In order to bring this information to the circuit designers in the form of cryogenic DC models, which enable reliable cryogenic circuit design, this chapter concluded with the description of a successful DC-modeling flow based on ANN training.
In the following chapters, in-depth studies of more advanced DC effects, such as device matching and self-heating, are presented.

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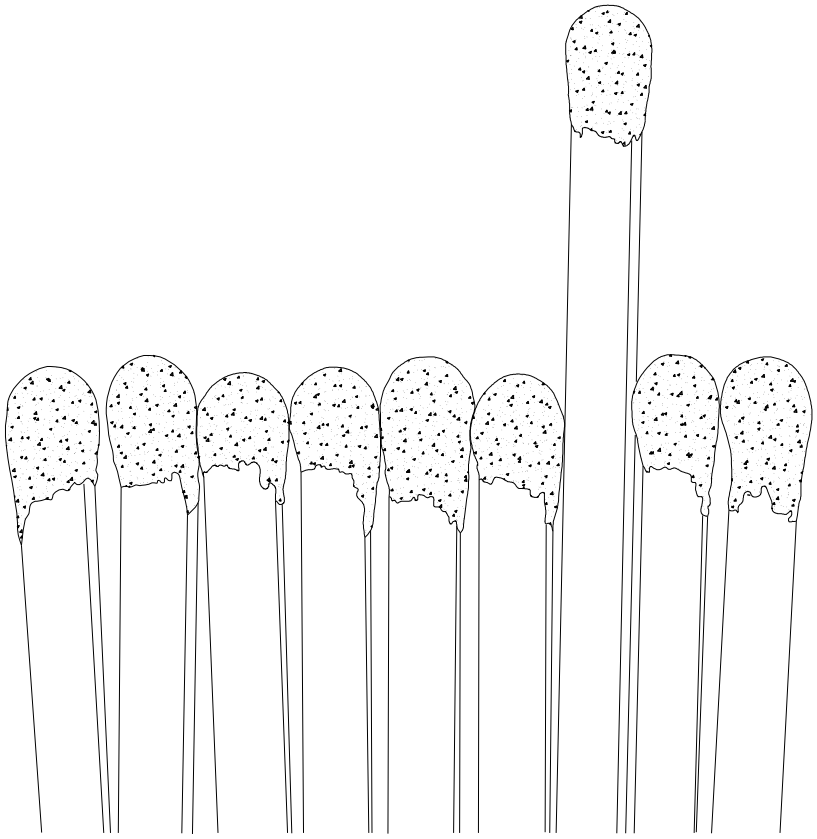

*Inspired by the work of Dr.ir. H.P. Tuinhout.

Chapter 3

Cryogenic Device Matching

3.1 Introduction

An important first step towards the reliable design of the cryogenic CMOS qubit controller introduced in Chapter 1 is the characterization and modeling of the low-temperature impact on MOSFET device parameters, such as shifts in threshold voltage, beta and subthreshold slope, as described in Chapter 2. However, in actual circuit designs, often not only the parameters of the individual MOSFETs are of importance, but also the performance of multiple devices combined needs to be taken into account. The operating principles of many of these circuits does not primarily rely on the behaviour of individual components, or their absolute parameter values, but rather on the behaviour of matched device pairs: devices that are assumed to be "perfectly" matched i.e., have equal threshold voltage, current gain, etc. over different bias conditions and ambient temperatures. In reality perfect matching is never achieved, therefore, knowledge of and the ability to simulate second-order effects such as device matching during the design phase are critical for proper circuit operation in the field.

If the two devices forming a matched pair are mismatched, they can severely limit the performance of the sensitive circuits they constitute. Examples of such circuits are current/voltage references, current mirrors and data converters, that form an integral part of the cryogenic controller.

The importance of mismatch is widely recognized and it was extensively investigated over the military temperature range (-55 to 125 °C) both in the strong-inversion operating region [3, 4, 5, 6, 7] and the subthreshold region [8, 9, 10, 11, 12, 13, 14]. These works indicate a degradation of matching as the operating temperature is reduced, which, when extrapolated, suggest mismatch effects should be exacerbated at cryogenic temperatures.

However, device mismatch at extremely low temperatures, in the range of 4.2 K, has not gained much attention up until now.

Parts of this chapter have been published in IEEE JEDS [1, 2]

The limited data published on cryogenic matching experiments confirms the above mentioned suspicion of increased mismatch at cryogenic temperatures. An increase in the variability of the current factor (β), the threshold voltage (V_{TH}) and the drain-current (I_D) for 0.5-µm Silicon on Sapphire (SOS) CMOS devices at LHT [15] and for 0.35-µm bulk CMOS devices at 5 K [16] was reported.
These works investigated mature processes and no work has been published focused on the cryogenic characterization of mismatch in an advanced nanometer CMOS technology, typically required in the interface for a quantum processor.
Therefore, a detailed matching study of 40-nm bulk CMOS devices at deep-cryogenic temperatures was carried out, whose methods and results are presented in this chapter. This chapter splits the mismatch studies into two main sections: strong inversion matching and subthreshold matching.
The first part of this chapter reports the characterization of NMOS and PMOS device pairs with 8 different geometries over the temperature range from RT down to Liquid Helium Temperature (LHT) manufactured in the STMicroelectronics 40-nm bulk CMOS technology. The variability of the device parameters relevant for strong-inversion mismatch analysis, i.e. β and V_{TH}, were extracted and their behaviour over temperature and device area was investigated, demonstrating that the Pelgrom rule [3] holds for nanometer CMOS down to LHT. With the use of these parameters, a drain-current mismatch ($\sigma_{\Delta I_D/I_D}$) model valid from moderate to strong inversion was validated against measurements.
Due to the limited cooling power of dilution refrigerators at deep-cryogenic temperatures, the power efficiency of the cryogenic controller is paramount. A very attractive way to minimize power consumption is to shift the operation of cryo-CMOS circuits from strong-inversion to the subthreshold region. The measurements presented in the first part of this chapter are limited to moderate/strong-inversion device operation. Therefore, new test chips were designed and fabricated to specifically investigate subthreshold device matching.
The second part of this chapter reports a study on subthreshold device mismatch of the TSMC 40-nm bulk CMOS technology. The behaviour of the subthreshold drain current is studied as a function of device geometry over the temperature range from Room Temperature (RT) down to LHT. In addition to the variability of threshold voltage and current factor, the subthreshold swing (SS) variability is specifically investigated for its impact on the subthreshold mismatch. Moreover, the validity of the Pelgrom area-scaling rule for these three parameters is again assessed at both room and cryogenic temperatures. Furthermore, a complete model of the drain-current mismatch is derived, valid from the subthreshold to the strong inversion regime over the full temperature range from 300 K down to 4.2 K, which is obtained by combining the Croon model [17] and the subthreshold mismatch model [11].
Finally, this chapter concludes with a short study of linear device arrays characterized at both RT and LHT, simulating the placement of different number of dummy devices. In order to improve matching of device pairs, dummy devices are routinely

placed adjacent to matched structures. Dummy devices mitigate undesired lithographic effects, mechanical stress and doping non-uniformity among the devices of the matched pair, thereby improving matching.
From the studies above, it is clear that matching deteriorates with decreasing temperature, however no information is gained about the effect and magnitude of mechanical stress at these temperatures. As complex integrated circuits consist of many layers of dissimilar materials, all with their individual Coefficient of Thermal Expansion (CTE), mechanical stress experienced by devices is expected to increase at extremely low temperatures.
Another important factor, directly applicable to circuit design, is the number of dummies required: it is not directly evident how many devices should be placed. For example, placing too few dummies results in a design that has sub-optimal performance, while placing too many wastes valuable chip area. In the final section of this chapter, measurements of linear device arrays at both RT and LHT are compared to answer these two questions. It is found that stress effects increase at cryogenic temperatures compared to RT and that only larger-than-minimum-size devices benefit from the placement of a limited amount of dummies.

This chapter is split into two main sections and structured as follows. The first part describes the strong-inversion matching study. In Section 3.2.1 and 3.2.2 a description of the experimental setup and of the parameter extraction algorithms is given, respectively. Section 3.2.3 details the methods employed for the strong-inversion mismatch analysis. The measurement results are presented in Section 3.2.4 and discussed in Section 3.2.5. Conclusions are drawn in Section 3.2.6.
The second part of this chapter presents the subthreshold matching study in detail. A description of the devices under test, the measurement setup and parameter extraction is given in Section 3.3.1 and 3.3.2. The mathematical foundations of the subthreshold and Croon models are established in Section 3.3.3. The measurement results are presented in Section 3.3.4 and discussed in Section 3.3.5. Finally, conclusions are drawn in Section 3.3.6.
The last part of this chapter is a study on stress effects and dummy placement at cryogenic temperatures presented in Section 3.4, using the linear device arrays described in Section 3.2.1.
This chapter concludes with Section 3.5.

3.2 Strong-Inversion Matching

This first part of this chapter contains the details of the strong-inversion matching study carried out on test structures designed in the STMicroelectronics 40-nm bulk CMOS process. The test dies specifically designed for this study contain both matched pair structures detailed in the following sections and the structures used for the mechanical stress and dummy placement study presented in Section 3.4.

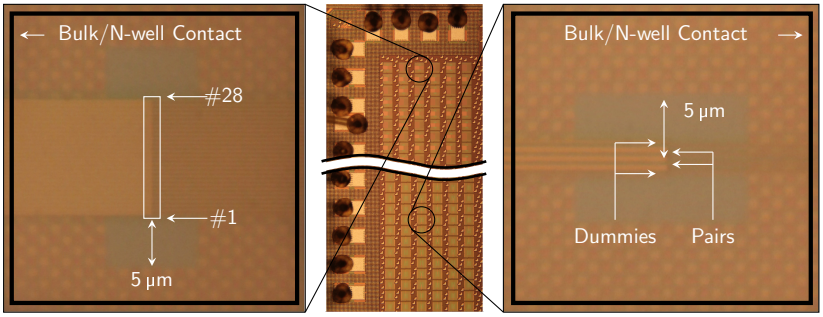

Figure 1: Die micrograph (*center*) with zoomed detail. *Left*: matched-device array; *right*: matched pair.

Both test structures are described in Section 3.2.1 for clarity, as some array devices also were employed to improve statistical estimators in the matched pair study.

3.2.1 Experimental Setup

Measurements were carried out on 3 dies manufactured in the STMicroelectronics 40-nm bulk CMOS process comprising low-threshold-voltage (LVT) 1.1-V NMOS and PMOS devices. The two types of test structures are highlighted in the die micrograph of Fig. 1: the device pairs, designed for mismatch characterization and the linear device arrays, targeted at mechanical stress effects and dummy placement.

All the devices share a common source connection while the drain and gate connections can be independently enabled by means of transmission gates, as depicted in the block diagram of Fig. 2. Each transmission gate can be individually enabled by a latched shift register, which is daisy-chained to form a chip-level shift register. The voltage drop across the cables, bondwires and transmission gates was compensated for by using Kelvin connections up to the source and drain diffusions of the devices.

Each die contains devices with 8 different geometries, as summarized in Fig. 3. For each geometry, 33 device pairs per die with dummies placed on both sides (to mitigate stress effects) were available. The linear arrays consist of 28 devices placed at the minimum allowable distance in a single row. No dummy transistors were placed adjacent to the first (device #1) and last device (device #28) in each array. A total of 9 arrays per die were available for each of the 3 array geometries represented in Fig. 3. Unless specifically mentioned, metal fillers were kept away further than 5 µm from the active devices in the pairs and arrays to minimize the effect of metal coverage, stress and asymmetries on device matching.

For the electrical characterization, Keithley 2636B Source Measurement Units (SMUs) were used to force voltages at the source, drain and gate terminals and

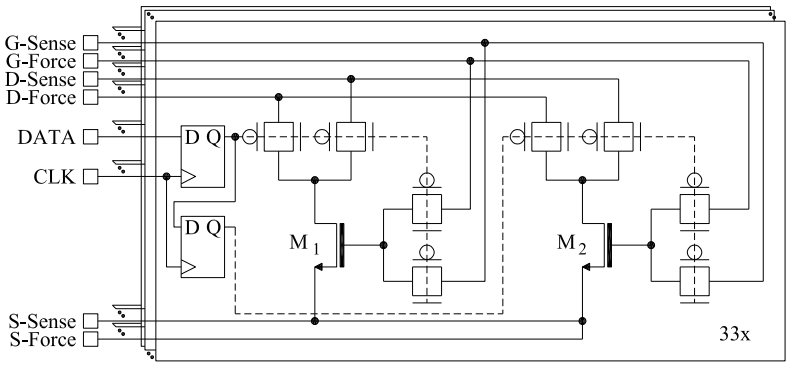

Figure 2: Simplified schematic of the circuit used to measure the matched pairs (M_1 and M_2). Arrays comprise 14 such circuits.

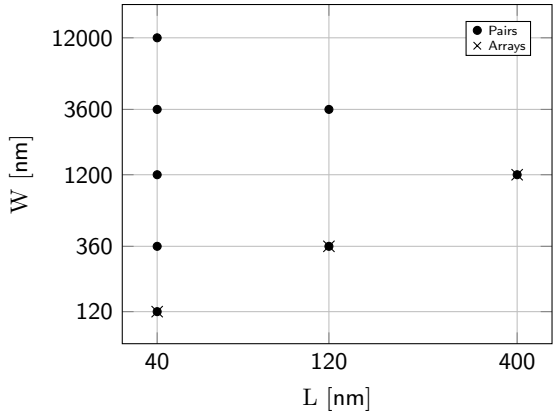

Figure 3: Device geometries available for mismatch and dummy/stress characterization.

record the drain current. To allow for the measurement of low currents, active guarding in combination with triaxial cabling was employed. In all the experiments, the drain current (I_D) as a function of gate voltage (V_G) was measured by electrically shorting the source voltage to the bulk, i.e. to 0 V for the NMOS and to 1.1 V for the PMOS and setting the drain-source voltage to $|V_{DS}| = 50$ mV and to $|V_{DS}| = 1.1$ V for operation in linear or saturation region, respectively.
All devices were measured sequentially in a 3-step procedure: 1) after selecting the target transistor by shifting the correct bit pattern into the shift register, the I_D-V_G curve is measured; 2) the same measurement is carried out a second time; 3) all devices are de-selected by shifting in an all-0 pattern and the measurement

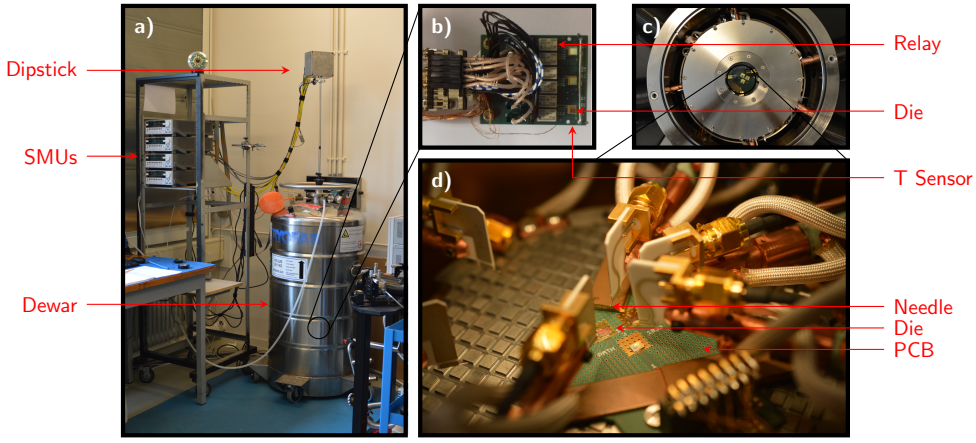

Figure 4: Measurement setup. a): dipstick; b) detail of PCB on the dipstick. The temperature sensor (Cernox RTD) is located on the opposite side of PCB. Relays used for die selection; c) cryogenic probestation; d) detail of the PCB in the cryogenic probestation.

is carried out a third time. The measurement in step 1 is the actual measurement used for the analysis, while the measurement in step 2 is done to check the Short-Time-Repeatability (STR) of the characterization, which is an indication of the reliability of the experiment and is used to guard against measurement errors due to bad contacts, sudden (unintended) temperature changes and interference. The STR is always below 0.2 % over the bias range, thus not significantly impacting measurement results. The measurement in step 3 quantifies the leakage current (∼200 nA @ 300 K) due to the large number (5136) of transmission gates connected in parallel and it is required to compensate for such leakage in order to extend the measurement range to lower current levels. Since the transmission-gate leakage is weakly bias- and temperature-dependent, a residual error remains after compensation. By discarding measured data for too low drain current, it was ensured that the leakage-induced error was always below 10 %.

Three dies were glued and wire-bonded to a PCB that was either placed in a Lakeshore CPX cryogenic probestation equipped with Lakeshore model-336 temperature controllers, or on a dipstick inserted into a Dewar containing liquid helium for cryogenic cooling, see Fig. 4. Ambient temperature was continuously monitored during the measurement, to ensure that the temperature had settled and that the temperature difference between the measurement of each device in a pair was below 5 mK.

From the measured I_D-V_G data, the threshold voltage (V_{TH}) and the current factor (β) were extracted via the maximum-G_m method [18]. Although the long-channel approximation used by this scheme may not be the most appropriate choice for

advanced technology nodes, it extracts the parameters at a point derived from the data itself, i.e. the bias point with the maximum transconductance G_m. This is an advantage over the other two well-known extraction methods, i.e. the constant current [18] and the 3-point [19] method, that either rely on an arbitrary target current or on multiple points chosen on the I_D-V_G curve. Moreover, since this work is mainly concerned with parameter mismatch, the extraction of the actual physical parameter value is of lesser importance. Mismatch is extracted accurately as long as the parameters are derived in a reliable and repeatable way for every device [20].
Following the extraction of V_{TH} and β for each pair, their mismatch (ΔV_{TH} and $\Delta\beta/\beta$) and their variability, i.e. their standard deviation $\sigma_{\Delta V_{TH}}$ and $\sigma_{\Delta\beta/\beta}$, are calculated from a sample size of 99 device pairs. The error bars in the following plots indicate 95% confidence intervals. Only for the geometries used for both the pairs and the arrays (see Fig. 3), a sample size of 351 is employed by also exploiting the devices in the array, thus resulting in a better statistical accuracy. For the arrays 27 devices per position were considered. The resulting $\sigma_{\Delta V_{TH}}$ and $\sigma_{\Delta\beta/\beta}$ are used as input to the Croon model to compute the drain-current mismatch $\sigma_{\Delta I_D/I_D}$ (see Section 3.2.3) [17].

3.2.2 Drain-Current Mismatch

When a single transistor pair (M_1, M_2) is considered, its drain-current mismatch can be defined as follows:

$$\frac{\Delta I_D}{\bar{I}_D} = \frac{2\,(I_{D_1} - I_{D_2})}{I_{D_1} + I_{D_2}}, \tag{3.1}$$

where the overbar is the average value operator and the subscript indicates the first or second device of a pair.
Two different types of mismatch can be distinguished: systematic and random mismatch.
Systematic mismatch arises from any asymmetry between the devices of a pair, e.g., when paired devices are (partially) covered by metal, have different proximity to wells or have their drain-current flowing in different directions. These sources of mismatch can be minimized by careful layout. Random mismatch can be mostly attributed to microscopic variations, e.g., Random Dopant Fluctuation (RDF), Line Edge Roughness (LER) / work function variation of the gate and Oxide Thickness Variation (OTV) [21], which are inevitably introduced during manufacturing and cannot be compensated at design time. In this work, care was taken to minimize any systematic mismatch in the device-pair structures, so as to accurately characterize the random mismatch. At the same time, the array structures are used to characterize some systematic effects.
As an example, the drain-current mismatch of 99 NMOS device pairs (W/L=360n/120n) measured at RT is plotted in Fig. 5, together with its ensemble

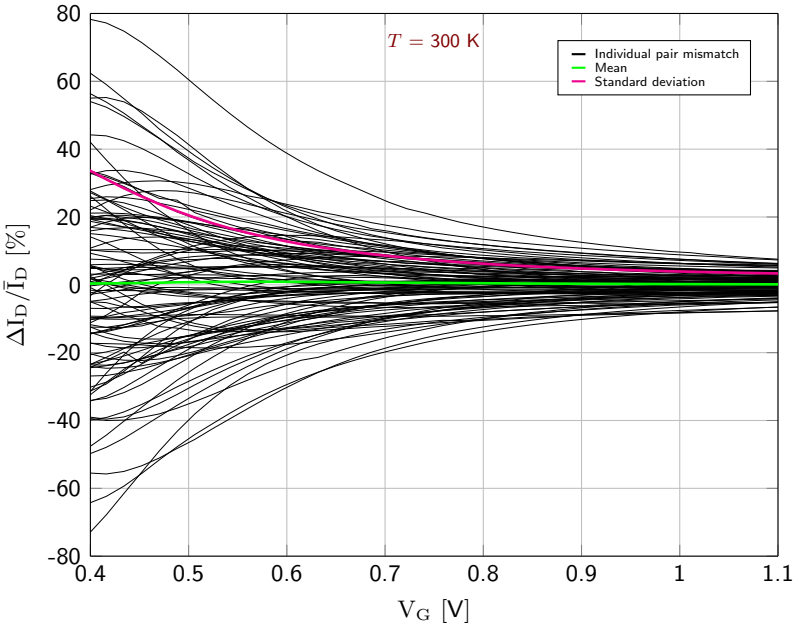

Figure 5: Drain-current mismatch per device pair for 99, W/L=360n/120n NMOS pairs. Ensemble mean (green) and standard deviation (magenta) indicated.

mean and standard deviation curves. The mean value of the drain-current mismatch is close to 0 over the full operating range, well within the margin of both the experimental and the statistical inaccuracy. This indicates a mismatch dominated by random, rather than systematic variation, thus validating the experimental approach. Similar considerations apply to the other geometries.

3.2.3 Strong-Inversion Mismatch Modeling

In order to provide designers of cryogenic circuits with the ability to predict device variability, the Croon model is used for drain-current mismatch [17]:

$$\sigma^2_{\Delta I_D/\bar{I}_D} = \sigma^2_{\Delta\beta/\bar{\beta}} + \left(\frac{g_m}{\bar{I}_D}\right)^2 \sigma^2_{\Delta V_{TH}}, \tag{3.2}$$

where σ is the standard deviation operator and g_m is the transconductance.
This model is based on a Taylor expansion of the drain current expressed as:

$$I_D = \beta f(V_{GS} - V_{TH}), \tag{3.3}$$

with $f(\cdot)$ an arbitrary function and $g_m = \partial I_D/\partial V_{GS}$.
The well-known area dependence of the threshold-voltage and current-factor vari-

ability is described by the Pelgrom rule [3]:

$$\sigma_{\Delta V_{TH}} = \frac{A_{VTH}}{\sqrt{WL}} \qquad \sigma_{\Delta\beta/\bar{\beta}} = \frac{A_{\beta}}{\sqrt{WL}}, \tag{3.4}$$

where A_{VTH} and A_{β} are technology-dependent factors and W and L are the active device width and length, respectively.
Eq. 3.11 and 3.12 were first validated with cryogenic measurements, after which the temperature dependent $\sigma_{\Delta V_{TH}}$ and $\sigma_{\Delta\beta/\bar{\beta}}$ interpolated from Eq. 3.12 were fed into Eq. 3.11 to form a full mismatch model.

3.2.4 Experimental Results

This Section describes the measured data and observations for device pairs. The extracted $\sigma_{\Delta V_{TH}}$ and $\sigma_{\Delta\beta/\bar{\beta}}$, are plotted as a function of device geometry for both RT and LHT in the Pelgrom plots in Fig. 6. The geometries have been grouped according to device length into 3 bins (L=40 nm, 120 nm and 400 nm) to highlight the length dependency of the A-factors.
Pelgrom's rule was fit to the measured data using a linear fitting weighted by the error bars. The resulting A_{VT} and A_{β} values are reported in Table 1 and 2. It can be concluded that variability of both parameters increases at LHT compared to RT and that Pelgrom's rule is valid at both temperatures with increased A-factors at cryogenic temperatures. The $\sigma_{\Delta V_{TH}}$ increase is statistically less significant if compared to $\sigma_{\Delta\beta/\bar{\beta}}$, as error bars in Fig. 6a and c are partially overlapping. This is reflected especially in the A_{VT} of the smallest geometry as can be seen in the confidence intervals reported in Table 1. If RT and LHT A-factors are compared by averaging their increase over the 3 geometries and 2 device types, it becomes clear that A_{β} shows the largest temperature variations ($+75\,\%$) with respect to A_{VT} ($+22\,\%$). The A-factor length dependency is particularly significant for β, increasing in value as devices become longer.
Mismatch fluctuation sweeps [7] for devices at different temperatures between LHT and RT are shown in Fig. 7 and Fig. 8. With these data, the performance of the measurement setup was assessed by comparing the standard deviation of the 300 K data with Monte Carlo simulations generated using the model provided by the foundry, which resulted in less than 13% deviation over the plotted range. Drain-current mismatch was found to increase with decreasing $|V_{GS}|$ for all temperatures. When temperature is decreased from RT to LHT, mismatch increases regardless of the operating regime, moderate or strong inversion. Over the reported temperature range, matching can deteriorate up to $10\times$ in moderate inversion, if evaluated at equal $|V_{GS}|$ (Fig. 7c). In all the 6 plots, the model in Eqn. 3.11 using the above-mentioned parameters ($\sigma_{\Delta V_{TH}}$ and $\sigma_{\Delta\beta/\bar{\beta}}$ in Fig. 6) is superimposed on the experimental data. The model is able to predict the measured data over all the measured geometries and temperatures by using the *unmodified*, extracted $\sigma_{\Delta V_{TH}}$ and $\sigma_{\Delta\beta/\bar{\beta}}$ values, without employing any fitting.

3.2.5 Discussion

The V_{TH} variability increase at cryogenic temperatures in Fig. 6a and c can be attributed to charge trapping in shallow traps at the Si/insulator interface, which due to the low carrier energy at LHT, remain trapped and perturb V_{TH} [15]. β variability increase can be attributed to the above mentioned shift from phonon-dominated scattering to impurity (dopant) scattering, which is a major contributor to mobility fluctuations [7]. It can be concluded from the data in Fig. 6 and Table 1 and 2 that mobility fluctuations are impacted at cryogenic temperatures much more strongly than threshold-voltage fluctuations.
The observed length dependency of the A-factor, visible in Fig. 6 and Table 1 and 2, can be attributed to halo/pocket implants employed to mitigate short-channel effects. Although these implants degrade matching because of RDF by increasing the doping concentration (RDF), this mechanism is not strongly concentration de-

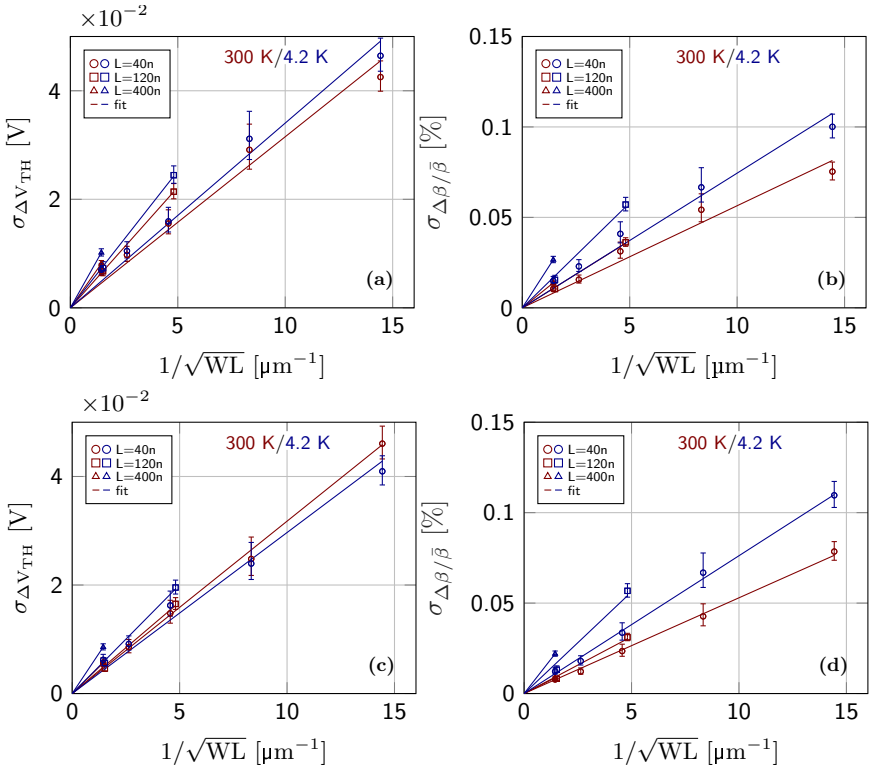

Figure 6: Pelgrom plots for V_{TH} and β with length dependency indicated by separate fitting for each length at RT (red) and LHT (blue). a), b) NMOS; c), d) PMOS. Error bars indicate 95% statistical confidence intervals.

Table 1: Threshold-voltage scaling factors as function of temperature and device length in [m], 95% confidence interval indicated.

T [K]	A_{VT} [mV · µm]					
	NMOS			**PMOS**		
	40n	**120n**	**400n**	**40n**	**120n**	**400n**
300	3.2 ±0.2	4.5 ±0.2	5.7 ±0.3	3.2 ±0.1	3.4 ±0.2	3.9 ±0.3
4.2	3.4 ±0.2	5.0 ±0.3	7.0 ±0.4	3.0 ±0.1	4.0 ±0.2	5.9 ±0.4

Table 2: β scaling factors as function of temperature and device length in [m], 95% confidence interval indicated.

T [K]	A_{β} [% µm]					
	NMOS			**PMOS**		
	40n	**120n**	**400n**	**40n**	**120n**	**400n**
300	5.6 ±0.2	7.4 ±0.4	9.5 ±0.5	5.3 ±0.3	6.3 ±0.3	6.0 ±0.4
4.2	7.4 ±0.3	11.6 ±0.7	18 ±1	7.6 ±0.4	11.3 ±0.6	15 ±1

pendent [21]. However, due to the strong control of device electrostatics in the heavily doped pockets, the area where fluctuation impact device behaviour is reduced, increasing mismatch [22]. The observed effects are in agreement with the data supplied by the foundry for RT.

The drain-current mismatch increase for lower $|V_{GS}|$ (Fig. 7 and Fig. 8), observed for all temperatures and devices, is due to the higher g_m/I_D when moving towards weak inversion (WI), which modulates the V_{TH} variability contribution in Eqn. 3.11. The increase of $\sigma_{\Delta I_D/\bar{I}_D}$ with decreasing temperature for a fixed V_{GS} bias is mainly caused by the V_{TH} increase (as discussed in Section 2.3.1), since a higher V_{TH} reduces the gate overdrive and shifts the device operating region towards WI, where drain-current mismatch is inherently larger, as explained above. As the subthreshold slope (SS) is enhanced at cryogenic temperatures [23], g_m/I_D is higher at lower temperature, thus increasing the impact of the $\sigma_{\Delta V_{TH}}$ term even more.

To investigate the effect of biasing and to indicate possible techniques that mitigate mismatch for cryogenic circuit design, $\sigma_{\Delta I_D/\bar{I}_D}$ has been plotted at two different g_m/I_D values as a function of temperature in Fig. 9. As the g_m/I_D term is kept constant, the only deterioration observed when the temperature is reduced from RT to LHT is caused by the temperature dependence of the parameter variability.

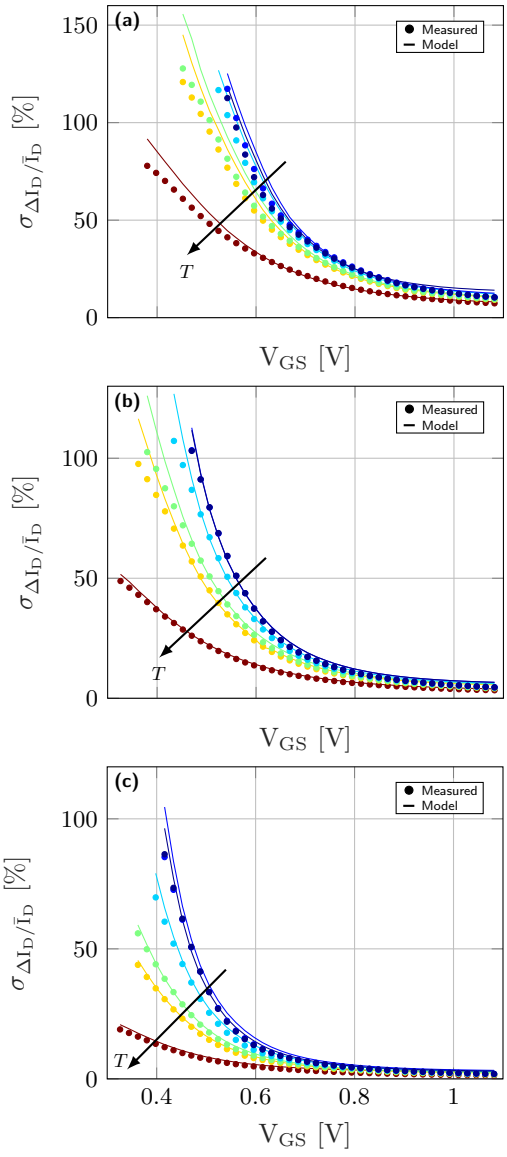

Figure 7: Drain-current mismatch for NMOS devices as a function of temperature (V_{DS} = 50 mV). T = 4.2, 40, 100, 150, 200 and 300 K. a) W/L=120n/40n; b) W/L=360n/120n; c) W/L=1.2µ/400n. Dots: measured data; lines: simplified Croon model as in Eq. 3.11.

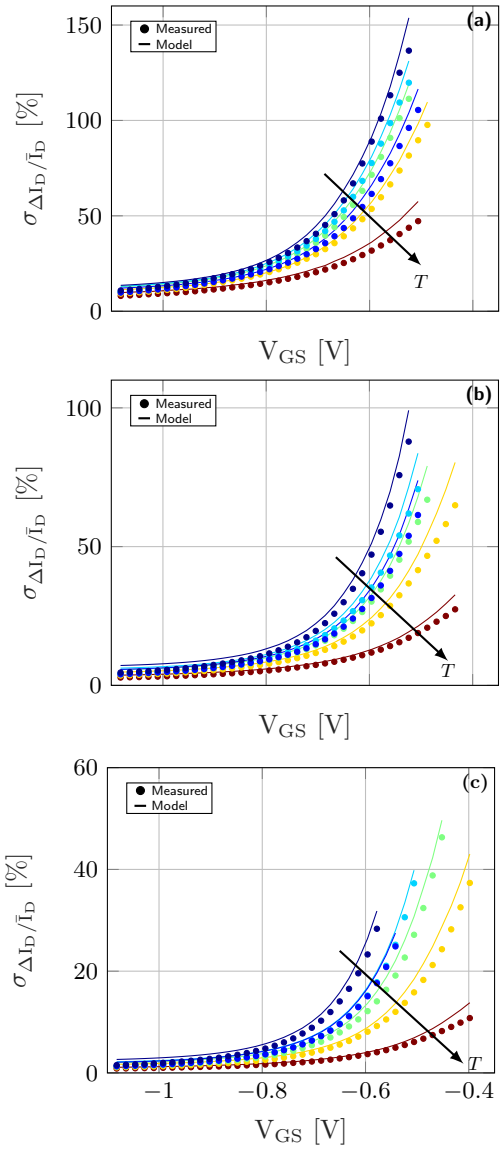

Figure 8: Drain-current mismatch for PMOS devices as a function of temperature ($|V_{DS}|$ = 50 mV). T = 4.2, 40, 100, 150, 200 and 300 K. a) W/L=120n/40n; b) W/L=360n/120n; c) W/L=1.2µ/400n. Dots: measured data; lines: simplified Croon model as in Eq. 3.11.

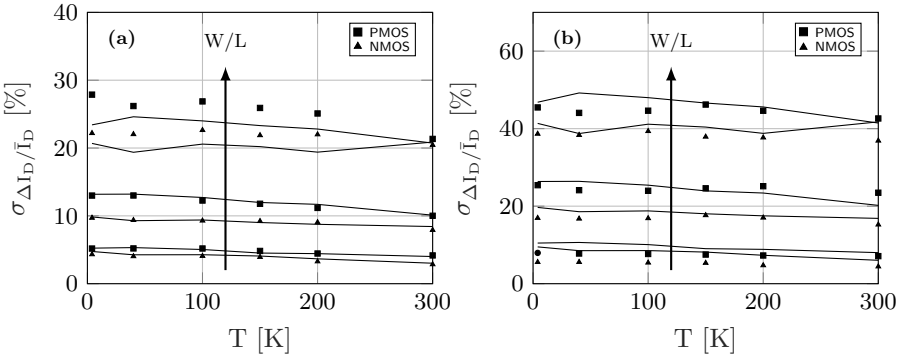

Figure 9: Drain-current mismatch as a function of temperature at a fixed g_m/I_D in saturation ($V_{DS} = 1.1\,\mathrm{V}$). a) $g_m/I_D = 5\,\mathrm{V}^{-1}$; b) $g_m/I_D = 10\,\mathrm{V}^{-1}$. Marks: measured data, lines: simplified Croon model as in Eq. 3.11. Arrow points in direction of decreasing W/L: 1.2µ/40n, 360n/120n and 120n/40n.

In these bias regions, it is mainly the V_{TH} variability that controls drain-current mismatch, which does not increase by more than 1.2×, in agreement with the extracted increase of $\sigma_{\Delta V_{TH}}$ over this temperature range.

3.2.6 Conclusion

The STMicroelectronics 40-nm bulk CMOS process was characterized over the temperature range from 300 K down to 4.2 K. The analysis of threshold-voltage and current-factor variability in matched device pairs showed that the Pelgrom scaling rule remains valid down to deep-cryogenic temperatures. The current-factor variability, and consequently the A-factors, increase at these low temperatures by ∼75 %, while the threshold-voltage variability remains substantially unaffected. The Croon model was successfully employed to accurately predict drain-current mismatch over the above-mentioned temperature range and for several device geometries. The availability of the presented mismatch data and model for such advanced nanometer CMOS process is crucial for the reliable design and operation of cryogenic circuits such as the cryogenic controller.
This study was however limited to strong-inversion device operation, which, as discussed in Section 3.1, is not the preferred operating and power regime for complex cryogenic circuits that have to operate within a tight thermal budget. Therefore, a complementary study was carried out for devices operating in the subthreshold region presented in the following section of this chapter.

3.3 Subthreshold Matching

This second part of this chapter describes the matching study on devices operating in the subthreshold region. This study was carried out on test structures fabricated in the TSMC 40-nm bulk CMOS technology, specifically designed to allow for the characterization of very small drain currents.

3.3.1 Experimental Setup

Two separate test chips were designed specifically to characterize subthreshold mismatch at cryogenic temperatures. Both chips were fabricated in the same 1.1-V 40-nm bulk CMOS process but in two different batches and comprise thin-oxide NMOS and PMOS devices with standard threshold voltage.
The first test chip (chip #1) enabled the characterization of three different device geometries laid out in a matched-pair configuration as indicated in Fig. 10a and Fig. 11. The results of the characterization of chip #1 have also been presented in [24]. A second test chip (chip #2, Fig. 10b) was designed to include 6 additional device geometries, as indicated in Fig. 11, thereby extending the scope of the work, e.g., to include mismatch dependency on device length.
A simplified circuit diagram of the NMOS array is shown in Fig. 12. A similar setup is adopted for PMOS devices. All devices (48 device pairs for each of the 3 geometries) share their drain and source terminals. When a device is selected, its gate is connected to a common bond pad through a transmission gate. When not selected, the gate is either connected to $\mathrm{V_{SS}}$ (for the NMOS) or $\mathrm{V_{DD}}$ (for the PMOS). Due to the higher threshold voltage at 4.2 K, the resistance of the transmission gate can significantly increase when biasing the device under test (DUT) in subthreshold. This, combined with the gate current of the DUT, caused the anomalous drain current behaviour reported in [24]. To overcome this limitation, the gate bias of the transmission gates was raised by 400 mV (up to 1.5 V) for all the characterization at 4.2 K, preventing the anomalous behaviour. The transmission gates are controlled by a latched shift register to enable automatic characterization. The potential of the N-well and of the substrate is fixed by contact rings biased at $\mathrm{V_{DD}} = 1.1\,\mathrm{V}$ and $\mathrm{V_{SS}} = 0\,\mathrm{V}$, respectively. Kelvin connections are made to the source and drain to mitigate the effect of series resistance in the measurement path, which is particularly important for the reliable extraction of device parameters in strong inversion where a non-negligible current is expected.
Chip #1 comprises one NMOS array and one PMOS array, each comprising 3 sets of 24 device pairs. Between the arrays, the shift register is daisy-chained and the gate pad is shared. Source and drain are routed to separate bond pads for each array, in order to minimize leakage. Chip #2 contains 3 NMOS arrays and 3 PMOS arrays. Their layout and connections are similar to those of chip #1. Device geometries with similar expected leakage were grouped in each array to increase the measurable subthreshold-current range.

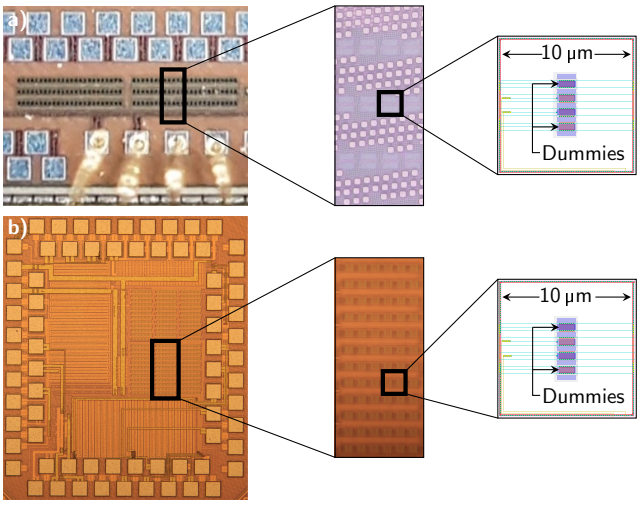

Figure 10: Micrograph of the chips used for mismatch characterization: a) chip #1 comprising 3 different device geometries (results also presented in [24]); b) chip #2 comprising an extended set of device geometries. Inset shows the layout details of the matched pairs.

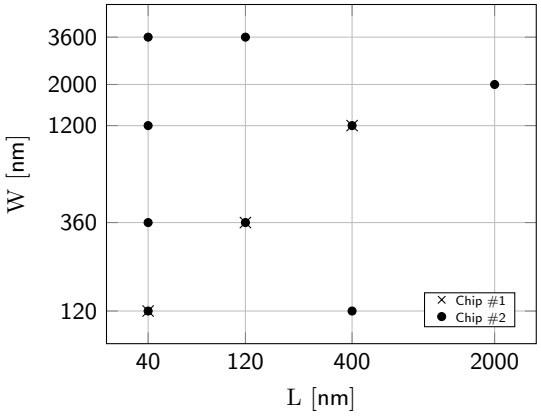

Figure 11: Device geometries available in the two test chips.

It should be noted that these chips were fabricated in a different 40-nm bulk CMOS process than the one reported in Section 3.2 and [25, 1], and that the test structures were redesigned. This was necessary to minimize leakage and consequently, enable accurate subthreshold-current measurement.
Care was taken to reduce the impact of systematic mismatch, edge effects and

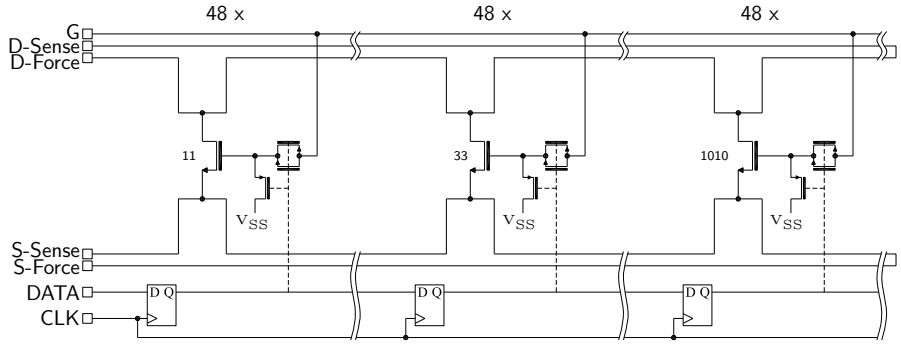

Figure 12: Simplified schematic of the NMOS mismatch characterization array of chip #1.

mechanical stress by placing the devices in each pair at minimum distance with symmetrical connections, by surrounding them with identical dummy devices and by keeping metallization further than 5 µm away from the active devices, as indicated in Fig. 10.

For the electrical characterization, two Keithley 2636B Source Measurement Units (SMUs) were connected to the samples by low-leakage triaxial guarded connections. The measurement setup did not limit the lowest measurable current of the instruments, which is in the range of 10 fA. Since the time required to characterize a single die exceeds 36 hours due to the long instrument settling times associated with the low current range, an automated setup with samples directly submerged into liquid Helium is preferred over a manual setup with a cryogenic probestation. Intermediate temperatures between LHT and RT were reached by positioning the sample at different heights in the Helium vapour inside a Helium Dewar.

For chip #1 and chip #2 a total of six dies (3 dies for chip #1; 3 dies for chip #2; 72 matched pairs per geometry) were characterized, both in the linear ($|V_{DS}|$ = 50 mV) and in the saturation region ($|V_{DS}|$ = 1.1 V) at RT and at LHT. In addition to these two temperatures, the devices on chip #2 were also measured at 100 K and a single device of each geometry was characterized at 9 temperature points from 300 K down to 4.2 K.

All devices were characterized sequentially in a 3-step procedure: 1) a single device is selected by loading the correct bit pattern into the digital interface; the drain current is measured as a function of gate-source voltage (V_{GS}) and recorded; 2) the first measurement is repeated, but with fewer V_{GS} bias points to save time; 3) all devices are deselected, and the measurement of the chip output is carried out a third time. Step 2 is employed to assess the Short Time Repeatability (STR) of the measurement setup, which is an indication of the reliability of the experi-

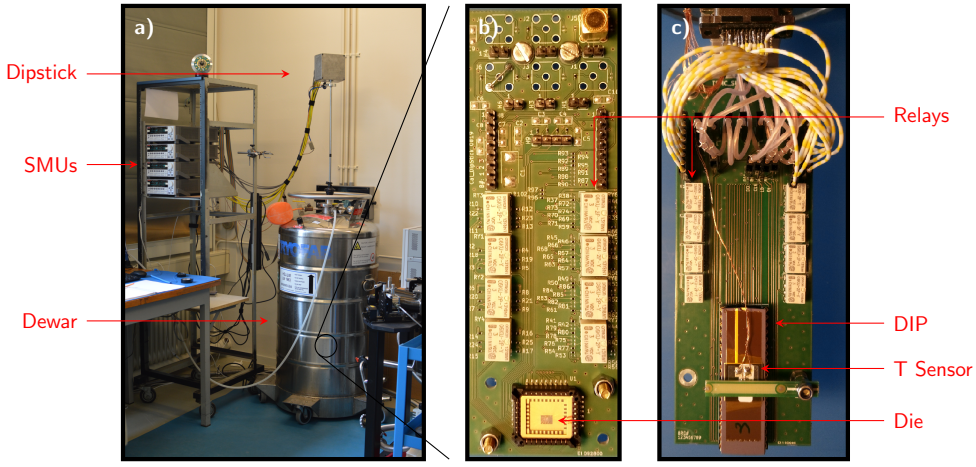

Figure 13: Measurement setup. a): dipstick and instruments; b) detail of the PCB designed for characterizing chip #1; c) detail of the PCB for characterizing chip #2.

ment and is used to guard against measurement error due to bad contacts, sudden (unintended) temperature changes and interference. The STR was always below 0.6 % over the bias range, thus not significantly impacting the measurement results. Step 3 characterizes the inevitable leakage of the array (∼4 nA at RT; < 10 fA at LHT). To extend the subthreshold range to lower currents, the leakage is subtracted from the value of I_D measured in step 1. This corrected data is then used for data analysis.

Since the leakage is weakly bias and temperature dependent, a residual error remains after compensation. Data were discarded for low current ranges, to ensure that this error is always below 10 %. The array data was validated against individual devices directly accessible via reserved bond pads in chip #1.

As shown in Fig. 13, the dies were either wire bonded to a CLCC (chip #1) or a DIP package (chip #2). These PCBs were mounted at the tip of a dipstick, which was inserted into a liquid Helium Dewar to reach cryogenic temperatures. The die temperature was continuously monitored with a Cernox temperature sensor. Temperature drift between the characterization of paired devices was below 10 mK at LHT, 1.1 K at RT and 0.3 K at 100 K. Due to a design error, the PMOS devices with W/L=120n/40n suffered from excess leakage current and are not included in the following analysis of subthreshold mismatch.

3.3.2 Parameter Extraction

The device parameters relevant for drain-current mismatch modeling in strong inversion, i.e. V_{TH} and β, were extracted from the I_D-V_G curves with the use of the Extrapolation-in-Linear-Region (ELR) method [18]. The ELR method was chosen for its reliability over the other two well-known methods, i.e. the constant current [18] and the 3-point [19] method, as it does not depend on arbitrarily chosen extraction points. Moreover, it was verified that the ELR results fit very well with the mismatch models employed in this work.
The subthreshold swing is an important device parameter in the subthreshold mismatch model. It is extracted by calculating the inverse slope of a line through two I_D points in the subthreshold regime:

$$SS^{-1} = \frac{|\log(I_{D_{hi}}/I_{D_{lo}})|}{V_{GS_{hi}} - V_{GS_{lo}}}, \tag{3.5}$$

where the 'hi' and 'lo' subscripts indicate a bias point at the edge between weak and moderate inversion and a bias point at the lowest current above the measurement limit, respectively.
As Drain Induced Barrier Lowering (DIBL) decreases the V_{TH} for devices in saturation, the value extracted by ELR in the linear regime will be over-estimated. Therefore, for these devices, the V_{TH} term in Eq. (3.9) is extracted with the use of the Extrapolation-in-Saturation-Region (ESR) method [18], which captures the impact of DIBL.

3.3.3 Subthreshold Mismatch Modeling

The subthreshold drain current is modeled by the simplified exponential equation:

$$I_D = I_0 e^{(V_{GS}-V_{TH})/SS}, \tag{3.6}$$

where I_0 is a temperature and geometry-dependent constant. Due to both the exponential nature and the increased I_D variability in this operating regime at cryogenic temperatures, Taylor expansion of Eq. (3.6) becomes impractical, thus making it more appropriate to use a logarithmic transform with base 10 [11, 8]:

$$\log(I_D) \propto \frac{1}{\ln(10)} \frac{V_{GS} - V_{TH}}{SS}. \tag{3.7}$$

If V_{TH} and SS are assumed to be the sources of variability, a first-order Taylor expansion of Eq. (3.7) yields:

$$\Delta \log(I_D) = \frac{1}{\ln(10)} \left[-\frac{1}{SS} \Delta V_{TH} - \frac{(V_{GS} - V_{TH})}{SS} \frac{\Delta SS}{SS} \right]. \tag{3.8}$$

The subthreshold drain-current mismatch can then be modeled by the variance of Eq. (3.8) as [11]:

$$\sigma^2_{\Delta \log I_D} = \frac{1}{\ln(10)^2}\left[\left(\frac{\sigma_{\Delta V_{TH}}}{\overline{SS}}\right)^2 + \left(\frac{V_{GS}-V_{TH}}{\overline{SS}}\frac{\sigma_{\Delta SS}}{\overline{SS}}\right)^2 + 2\frac{(V_{GS}-V_{TH})}{\overline{SS}^3}\sigma_{\Delta V_{TH}}\sigma_{\Delta SS}\rho_{\Delta V_{TH},\Delta SS}\right]. \quad (3.9)$$

Here the overline indicates the average value over all matched pairs with a given geometry and $\rho_{\Delta V_{TH},\Delta SS}$ is the correlation coefficient between ΔV_{TH} and ΔSS. This correlation was found to be statistically insignificant at RT, 100 K and LHT. Therefore, this term is ignored in the following analysis.
The drain-current mismatch over all temperatures in moderate to strong inversion is modeled by the Croon model [17], as such model has already been proven to apply at cryogenic temperatures in [1]. It can be shown that:

$$\sigma^2_{\Delta I_D/I_D} = \ln(10)^2\sigma^2_{\Delta \log I_D}, \quad (3.10)$$

therefore the Croon model is expressed as:

$$\sigma^2_{\Delta \log I_D} = \frac{1}{\ln(10)^2}\left[\sigma^2_{\Delta\beta/\beta} + \left(\frac{\bar{g}_m}{\bar{I}_D}\right)^2\sigma^2_{\Delta V_{TH}}\right], \quad (3.11)$$

where g_m is the transconductance of the devices. For the Croon model in Eq. (3.11), no correlation term is introduced, as it is typically neglected in moderate/strong inversion [1, 17].
The increased subthreshold mismatch resulting from the increased SS variability cannot adequately be modeled by Eq. (3.11), therefore the Croon model is only used outside the subthreshold region. In weak inversion, the subthreshold model of Eq. (3.9) is employed.
Pelgrom's scaling rule [3] is used to model the area dependency of $\sigma_{\Delta V_{TH}}$, $\sigma_{\Delta\beta/\beta}$ and $\sigma_{\Delta SS/SS}$:

$$\sigma_{\Delta V_{TH}} = \frac{A_{VT}}{\sqrt{WL}} \quad \sigma_{\Delta\beta/\beta} = \frac{A_\beta}{\sqrt{WL}} \quad \sigma_{\Delta SS/SS} = \frac{A_{SS}}{\sqrt{WL}} \quad (3.12)$$

where A_{VT}, A_β and A_{SS} are the threshold-voltage, current-factor and subthreshold-swing area-scaling parameters, respectively, and WL is the device active area. By combining Eq. (3.12) with (3.9) and (3.11), the drain-current mismatch for any device geometry can be computed.
Finally, it is important to note that the model parameters in Eq. (3.9) and (3.11) ($\sigma_{\Delta V_{TH}}$, $\sigma_{\Delta\beta/\beta}$ and $\sigma_{\Delta SS/SS}$) have not been selected to fit the proposed models to the measured data. Instead, the mismatch in each parameter (V_{TH}, β, SS) was

extracted from the I_D-V_G data of each pair and subsequently used to compute the respective standard deviation used in the models described by Eq. (3.9) and (3.11). This is a strong argument for the validity of the adopted model.

3.3.4 Experimental Results

Fig. 14 shows the I_D-V_G characteristics for 48 NMOS and PMOS devices from a single die at RT, 100 K and LHT. The temperature impact on the three relevant parameters can clearly be identified: V_{TH} increases ($V_{TH_{4.2K}} - V_{TH_{300K}} \approx 100\,\text{mV}$), mobility increases ($\beta_{4.2K}/\beta_{300K} \approx 2\times$) and SS decreases ($SS_{300K} \approx 90$ mV/dec $\rightarrow SS_{4.2K} \approx 20$ mV/dec), which is consistent with prior works [23, 26, 1].
To investigate the cryogenic subthreshold drain-current behaviour, additional measurements were carried out over a larger set of temperatures. Fig. 15a shows the I_D-V_G curves of a single W/L=1.2μ/40n NMOS device at intermediate temperatures between RT and LHT in steps of 40 K. It is clear from this plot that the SS decreases down to 40 K after which it starts to saturate.
To study the impact of device geometry on SS, Fig. 15b shows data at LHT for NMOS devices from all available geometries, demonstrating a very weak sensitivity to device geometry.
To assess the subthreshold drain-current variability for devices with equal geometry, the drain current of 10 NMOS devices with W/L=1.2μ/40n at T = 4.2 K, biased both in the linear ($V_{DS} = 50\,\text{mV}$) and saturation ($V_{DS} = 1.1\,\text{V}$) region, is reported in Fig. 15c. A slight V_{TH} decrease due to DIBL and a subthreshold current improvement can clearly be seen for the saturated devices with respect to those operated in the linear regime. The impact of the V_{TH} and SS variability on the subthreshold drain-current distribution is clearly visible in this plot.
To be complete, the temperature behaviour of the extracted SS for all 9 available NMOS geometries is shown in Fig. 15d. SS improves with decreasing temperature up to 4$\times$ from RT to LHT. At temperatures below 40 K, the slope saturates (see Fig. 15a). Similar curves are obtained for the PMOS devices.
To investigate subthreshold mismatch, $\Delta \log(I_D) = \log(I_{D1}) - \log(I_{D2})$ was computed for 72 device pairs at RT, 100 K and LHT, as plotted in Fig. 16. The combination of the increased V_{TH} and the steeper SS causes I_D to reach the instrument's current floor at a much higher V_{GS} at cryogenic temperatures compared to RT. The subthreshold mismatch is orders of magnitude higher at LHT compared to RT, which is attributed to an increased SS mismatch further exacerbated by the steeper subthreshold slope.
Pelgrom plots for $\sigma_{\Delta V_{TH}}$, $\sigma_{\Delta\beta/\beta}$ and $\sigma_{\Delta SS/SS}$ are shown in Fig. 17 and Fig. 18 for PMOS and NMOS, respectively. The linear fittings are inversely weighted with the 95 % confidence bounds, with the slopes representing the A-factors in Eq. (3.12). For both NMOS and PMOS devices, the Pelgrom rule is effective in modeling $\sigma_{\Delta V_{TH}}$ and $\sigma_{\Delta\beta/\beta}$ at RT, 100 K and LHT.
The $\sigma_{\Delta SS/SS}$ dependency on area plotted in Fig. 17c and Fig. 18c can be suc-

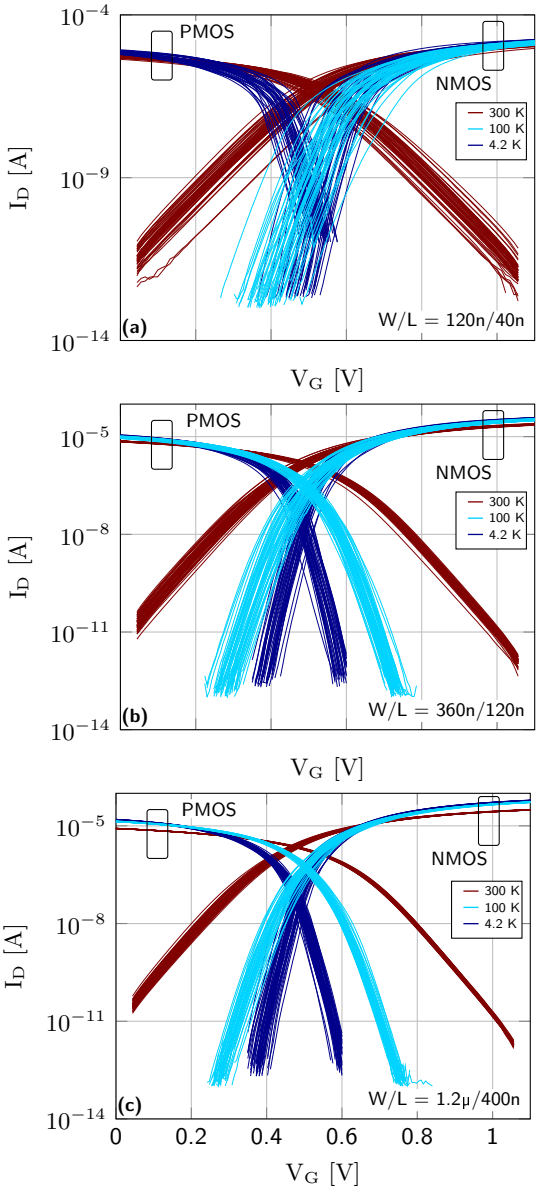

Figure 14: I_D-V_G curves for a single die (48 devices per geometry) at T = 300 K, 100 K and 4.2 K: a) W/L=120n/40n; b) W/L=360n/120n and c) W/L=1.2µ/400n. $|V_{DS}|$ = 50 mV. V_S = 0 V for NMOS and 1.1 V for PMOS, respectively.

cessfully modeled by the Pelgrom rule at RT, 100 K and LHT. Only devices with L=40n are shown in these plots for clarity.
The temperature and length dependency of the extracted A-factors is shown in Fig. 19 and Fig. 20 with error bars representing 95 % confidence intervals. For both NMOS and PMOS, A_{VT} shows a significant increase of $\sim$1.5$\times$ at LHT with respect to RT for L=400n, while no significant increase is observed for L=40n. A_β increases significantly over the same temperature range: $\sim$2$\times$ for N- and PMOS devices with L=40n and up to $\sim$4.2$\times$ for L=400n NMOS devices, respectively. For all lengths, A_{SS} significantly increases by $\sim$3$\times$ and $\sim$5$\times$ at 100 K compared to RT for NMOS and PMOS devices, respectively. Below 100 K, A_{SS} saturates or increases only slightly.

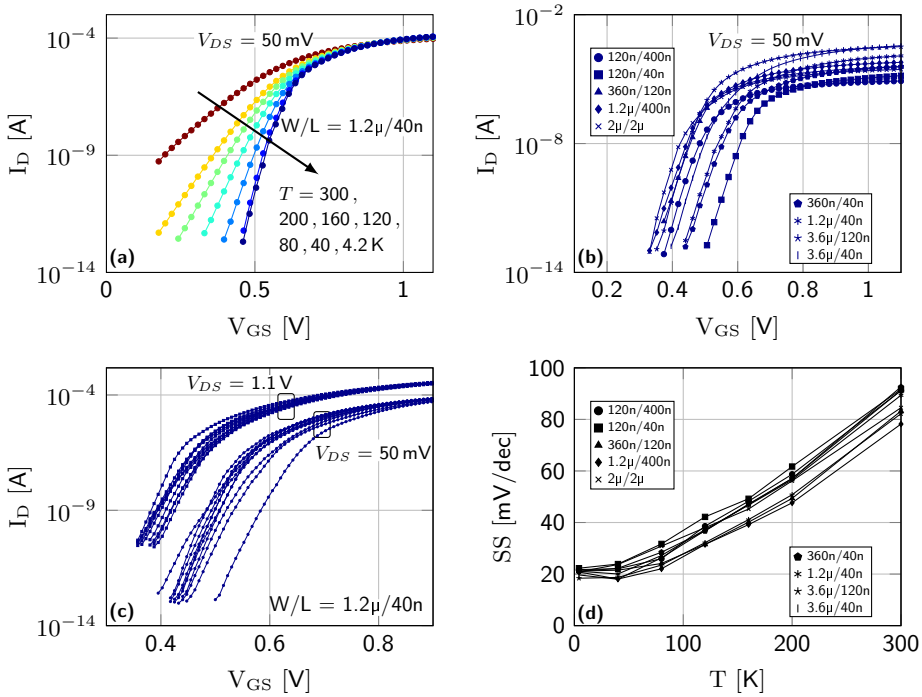

Figure 15: NMOS device behaviour over temperature: (a) I_D-V_G curves of a W/L=1.2µ/40n device; (b) $\mathrm{I_D - V_G}$ curves of all 9 geometries at T = 4.2 K; (c) I_D-V_G curves of 10 W/L=1.2µ/40n devices at T = 4.2 K and (d) extracted SS (V_{DS} = 50 mV) as function of temperature for all 9 geometries.

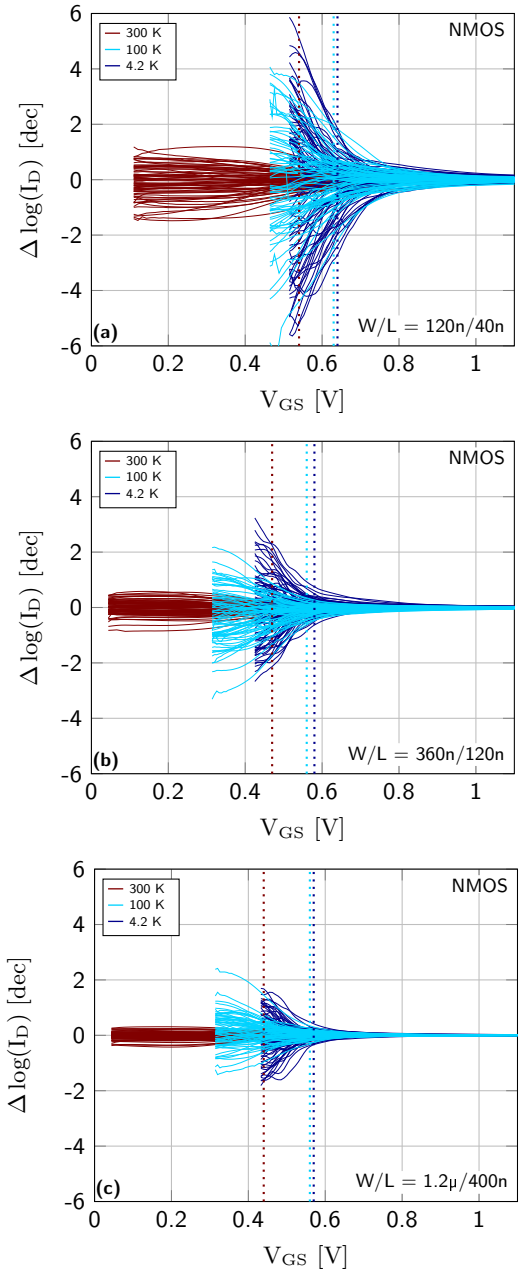

Figure 16: NMOS drain-current mismatch of 72 device pairs (3 dies) at T = 300 K, 100 K and 4.2 K: a) W/L=120n/40n; b) W/L=360n/120n and c) W/L=1.2µ/400n. V_{TH} marked by dashed lines. $V_{DS} = 50\,\text{mV}$.

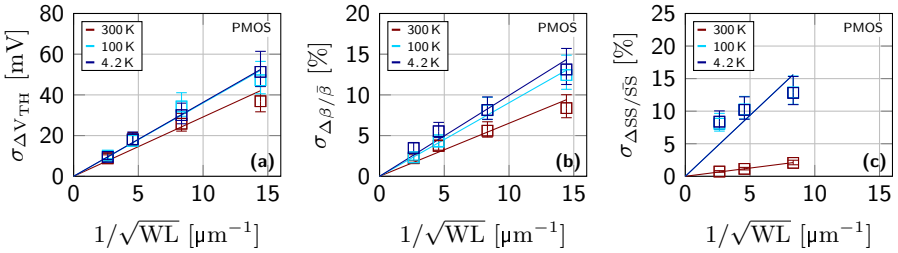

Figure 17: Pelgrom plots of PMOS with L=40n device length at T = 300 K, 100 K and 4.2 K for: (a) $\sigma_{\Delta V_{TH}}$; (b) $\sigma_{\Delta\beta/\beta}$ and (c) $\sigma_{\Delta SS/SS}$. 95% confidence intervals are shown.

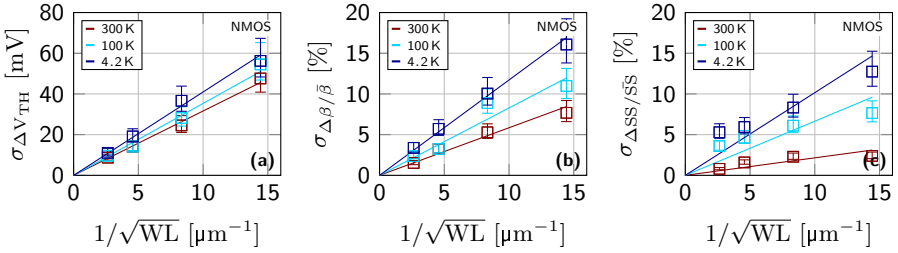

Figure 18: Pelgrom plots of NMOS with L=40n device length at T = 300 K, 100 K and 4.2 K for: (a) $\sigma_{\Delta V_{TH}}$; (b) $\sigma_{\Delta\beta/\beta}$ and (c) $\sigma_{\Delta SS/SS}$. 95% confidence intervals are shown.

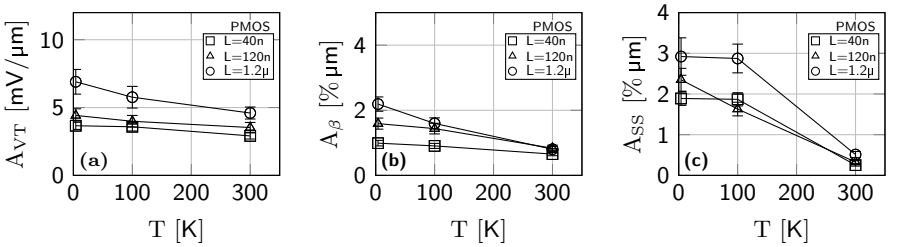

Figure 19: A-factors as a function of temperature for 3 different PMOS device lengths: a) A_{VT}; b) A_β and c) A_{SS}. 95% confidence intervals are shown.

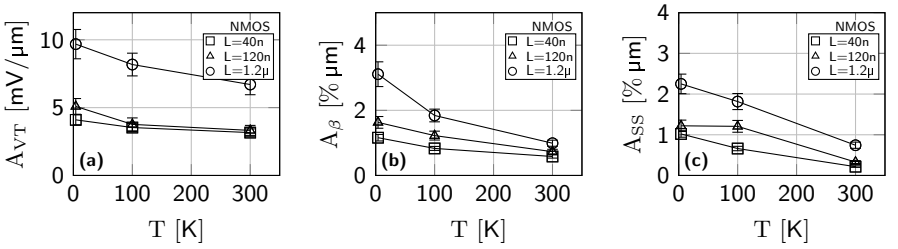

Figure 20: A-factors as a function of temperature for 3 different device NMOS lengths: a) A_{VT}; b) A_β and c) A_{SS}. 95% confidence intervals are shown.

Drain-current mismatch for devices operating in linear and saturation regions at various temperatures and geometries is plotted in Fig. 21, 22 and 23, together with the Croon and the subthreshold models of Eq. (3.9) and (3.11), respectively. It should be noted that the $\sigma_{\Delta V_{TH}}$, $\sigma_{\Delta\beta/\beta}$ and $\sigma_{\Delta SS/SS}$ used in these two equations are the same as reported for the Pelgrom plots and have been directly derived from the measurements and not by fitting the models. Only 3 of the 9 available geometries are shown here for brevity, but similar trends were observed in the omitted curves.

At 300 K, in Fig. 21, both the Croon and the subthreshold models are able to predict mismatch over the full bias range for both NMOS and PMOS and in all operating regimes. At RT, drain-current mismatch reaches a plateau in the subthreshold region due to the low variability of SS at RT.

Drain-current mismatch at 100 K, as plotted in Fig. 22, shows an increased subthreshold mismatch compared to RT. The Croon model is capable of fitting the

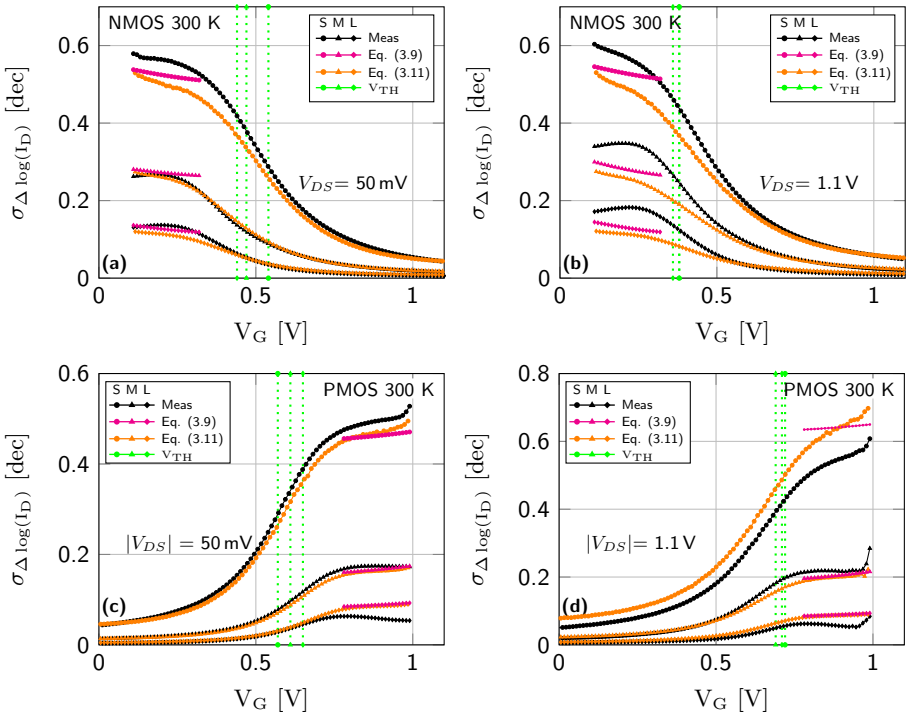

Figure 21: Drain-current mismatch as function of gate bias for 3 geometries at T = 300 K: S (W/L=120n/40n); M (W/L=360n/120n) and L (W/L=1.2µ/400n). V_{TH} and V_{DS} indicated in each figure. $V_S = 0$ V for NMOS and 1.1 V for PMOS.

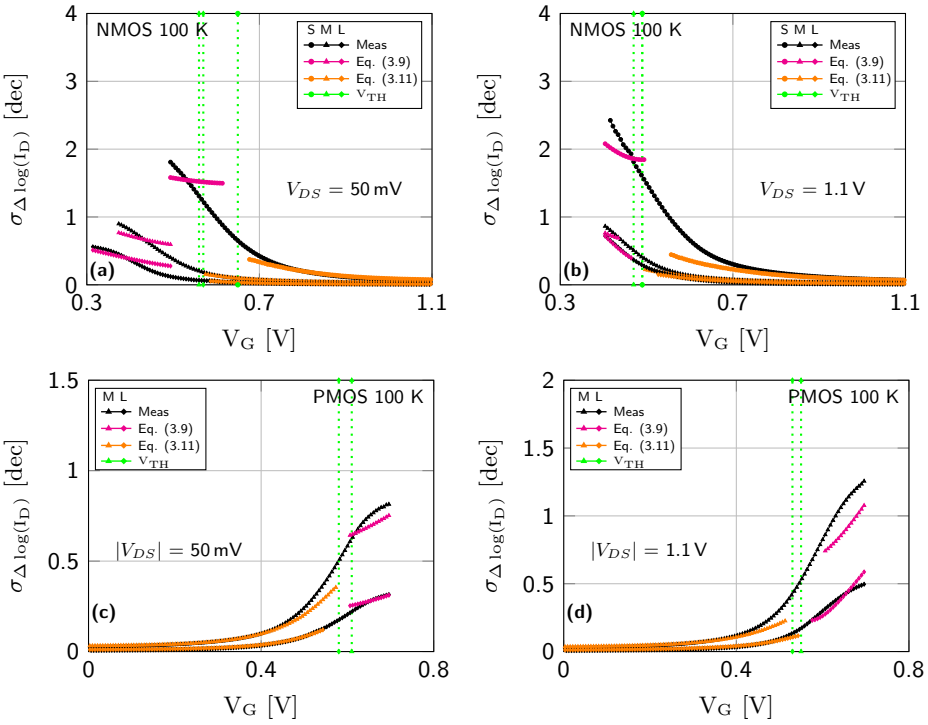

Figure 22: Drain-current mismatch as function of gate bias for 3 geometries at T = 100 K: S (W/L=120n/40n); M (W/L=360n/120n) and L (W/L=1.2µ/400n). V_{TH} and V_{DS} indicated in each figure. V_S = 0 V for NMOS and 1.1 V for PMOS.

data in strong to moderate inversion, but it ceases to be adequate in subthreshold. The subthreshold model is able to give a better prediction in this region.
In Fig. 23, the subthreshold mismatch at LHT increases further compared to 100 K, which is in line with the $\Delta \log(I_D)$ plots in Fig. 16 while the trend of the curves stays similar with those at RT and 100 K. The Croon model is again able to predict mismatch in strong to moderate inversion but the subthreshold model needs to be employed for weak inversion.

3.3.5 Discussion

Unless the gate voltage of the transmission gate is raised as explained in Section 3.3.1, pronounced discontinuities in the SS can be observed. While these large anomalies are not visible in the plots nor in the subthreshold characteristics of bare, pad accessible devices, very subtle deviations from ideal exponential

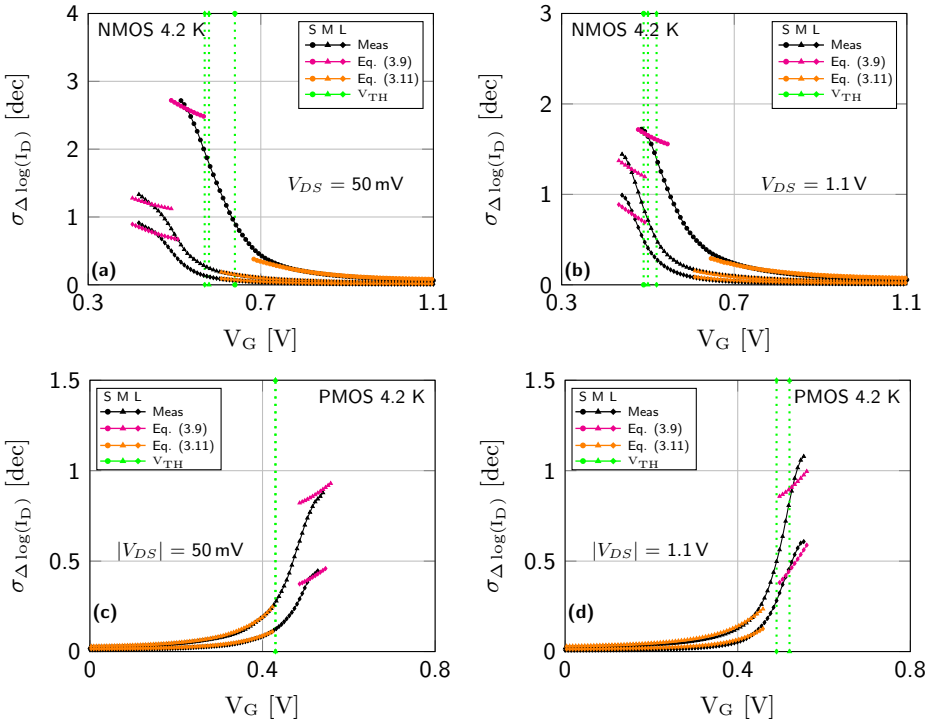

Figure 23: Drain-current mismatch as function of gate bias for 3 geometries at T = 4.2 K: S (W/L=120n/40n); M (W/L=360n/120n) and L (W/L=1.2µ/400n). V_{TH} and $|V_{DS}|$ indicated in each figure. $V_S = 0\,\mathrm{V}$ for NMOS and 1.1 V for PMOS.

behaviour were still observed in a part of the device population at LHT, in both multiplexed and bare structures.

Deviations from ideal subthreshold behaviour have already been described in other publications. In cryogenically cooled 22-nm FDSOI [27] these effects were attributed to resonant electron/hole tunneling through a Quantum Dot (QD). Subthreshold humps in [9, 28] were shown to be caused by STI bumps in the channel edge, locally modulating barrier heights. Unexpected changes in subthreshold slope at cryogenic temperatures have also been explained by a V_{GS} dependency of the threshold voltage caused by freeze-out of dopants [29, 28, 30, 31]. The cause of oscillations in the subthreshold region observed by [32, 33, 34, 35, 36] is identified as resonant electron/hole tunneling through electronic states of defects, such as dopant atoms coupled to the diffusions.

As the mechanisms behind these effects are random (e.g. QDs, STI bumps,

dopants), they have the potential to severely impact subthreshold matching.
In this work, the extraction of SS was not hampered by subthreshold non-idealities, as the deviations where minute and, furthermore, the fitting of SS filters out small local variations resulting in Pelgrom-like behaviour down to 4.2 K (Fig. 17c and 18c). Moreover, subthreshold matching was not significantly deteriorated by any of these effects as the simple subthreshold model, which only takes the extracted SS variability into account, is able to fit the data quite well.
The observed length dependency of $\sigma_{\Delta V_{TH}}$ and $\sigma_{\Delta\beta/\beta}$ (see Fig. 17 and 18) is compatible with prior results presented in [1].
Based on the A-factors for L=40n, for which the largest amount of geometries are available and, hence the highest accuracy is reached, it can be concluded that A_{VT} has no statistically significant variation with temperature, while A_β and A_{SS} increase significantly from RT to LHT.
As highlighted in Section 3.3.4, the Croon model is able to accurately predict mismatch in moderate to strong inversion at all temperatures and bias conditions, as also demonstrated in [1], while the subthreshold model must be adopted in weak inversion. Although the models and the experimental data already show good agreement when using $\sigma_{\Delta V_{TH}}$, $\sigma_{\Delta\beta/\beta}$ and $\sigma_{\Delta SS/SS}$ extracted from the measurements, as described above, an even smaller discrepancy is obtained when *fitting* the models described in Eq. (3.9) and (3.11) with the experimental data, as shown in Fig. 24.

3.3.6 Conclusion

This section describes the characterization and modeling of the subthreshold device mismatch of CMOS devices at cryogenic temperatures. Mismatch increases

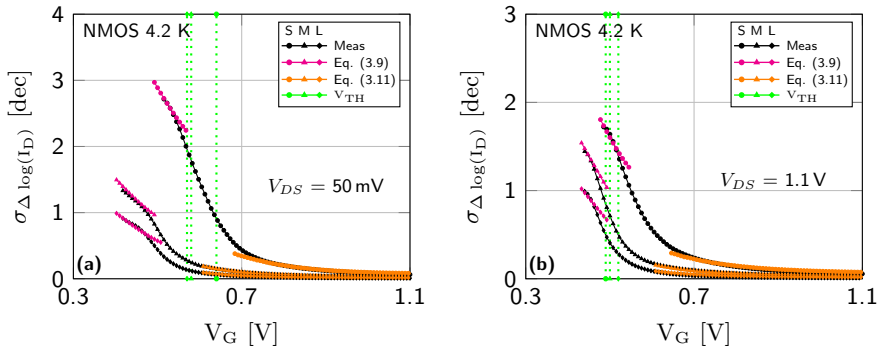

Figure 24: Drain-current mismatch modeled using the Croon and the subthreshold model and tuning $\sigma_{\Delta SS/SS}$ and $\sigma_{\Delta V_{TH}}$ for the best fit between experimental data and models: a) V_{DS} = 50 mV; b) V_{DS} = 1.1 V.

at cryogenic temperatures in all operating regions and, in particular, subthreshold matching deteriorates by more than several orders of magnitude. As the Croon model does not take subthreshold-swing variability into account, a specific subthreshold model is shown to adequately model mismatch in the weak-inversion region at these temperatures. Improving matching by increasing the device area as predicted by Pelgrom rule proves to be valid at cryogenic temperatures in all operating regions including subthreshold. As a result, the proposed mismatch models can become an essential tool for the design of the cryo-electronics that will enable scalable quantum computers.

3.4 Stress Effects and Dummy Placement

This final section describes the experiments carried out on the array structures present on the 40-nm bulk CMOS test chip described in Section 3.2.1.
In the previous two sections it was shown that matching deteriorates at cryogenic temperatures compared to RT in all operating regimes, which brings up the question: how can matching be improved under these extreme conditions?
Dummy devices (see also Section 3.1) are routinely placed adjacent to sensitive matched structures to mitigate undesired lithographical and mechanical-stress effects, and improve the overall geometrical symmetry of structures, reducing device mismatch. At deep-cryogenic temperatures many electrical and mechanical parameters shift significantly from their RT values and the effectiveness of this method is not directly evident. It is therefore worthwhile to investigate the effect of dummy devices on parameter variability/shift at these low temperatures. This is especially interesting, as an increase in mechanical-stress-induced mismatch can be expected due to a significant thermal expansion/contraction at very low temperatures [37].

3.4.1 Experimental Setup and Results

For this experiment I_{DSAT}, V_{TH} and β were extracted from devices placed in linear arrays. These arrays emulate the placement of increasingly more dummies for devices closer to the center of the array. In order to characterize the effect of these dummies, I_{DSAT} is measured as a function of device position in the array, since it is directly observable and it is an important parameter for circuit designers. To shine more light on the underlying mechanisms that cause these changes, V_{TH} and β are also extracted as a function of device position in the array.
The array layout, electrical connections and available device geometries have been described in Section 3.2.1. The parameters V_{TH} and β were extracted employing the maximum-$\mathrm{G_m}$ method [18], as per the strong-inversion matching study. The maximum drain current, I_{DSAT}, has been measured at maximum gate and drain drive: $I_{DSAT} = I_D|_{|V_{GS}|,|V_{DS}|=1.1\,\mathrm{V}}$.
In Fig. 25 and Fig. 26, I_{DSAT} is plotted as a function of device position for NMOS and PMOS devices. The values at RT and LHT are normalised to the corresponding median value to enable a comparison between the two temperatures. A variability increase for both NMOS and PMOS devices can be recognized by elongated error bars, both when temperature and the device area are decreased. Considering the NMOS devices in Fig. 25, the effect of array position starts to become significant only for large devices, while it is overshadowed by random mismatch for smaller devices. A significantly larger I_{DSAT} for the two outer devices (position #1 and #28) can be seen in Fig. 25c, although a clear temperature dependence is not visible.
Compared to NMOS, the PMOS devices in Fig. 26 exhibit larger and opposite

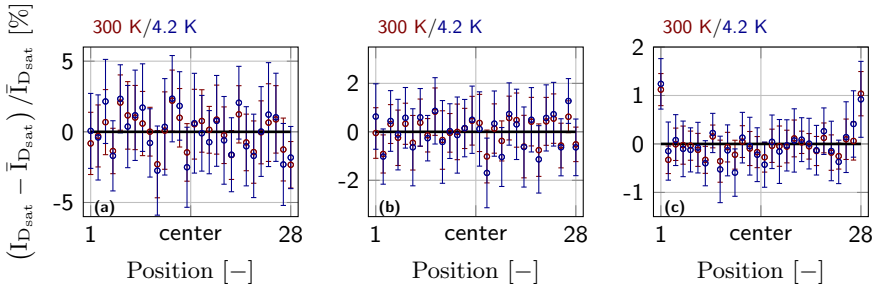

Figure 25: Relative $I_{D_{sat}}$ $(I_D|_{V_{DS}=V_{GS}=1.1\,\mathrm{V}})$ values as a function of device position for NMOS devices at RT (red) and LHT (blue): a) W/L=120n/40n; b) W/L=360n/120n and c) W/L=1.2µ/400n. Zero deviation emphasized by the black lines and error bars indicate 95% confidence intervals. Note that y-axes are not equally scaled.

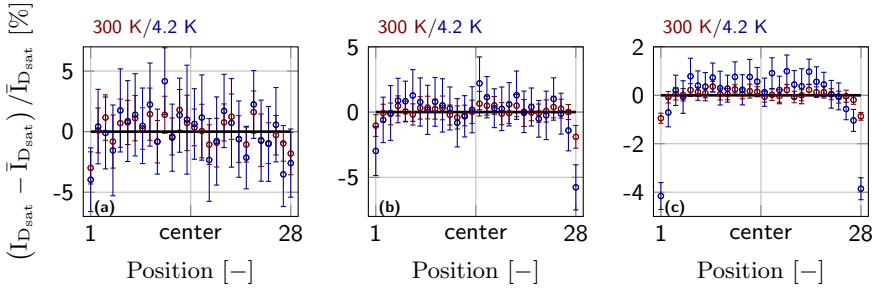

Figure 26: Relative $I_{D_{sat}}$ $(I_D|_{V_{DS}=V_{GS}=1.1\,\mathrm{V}})$ values as a function of device position for PMOS devices at RT (red) and LHT (blue): a) W/L=120n/40n; b) W/L=360n/120n and c) W/L=1.2µ/400n. Zero deviation emphasized by the black lines and error bars indicate 95% confidence intervals. Note that y-axes are not equally scaled.

sensitivity to placement in the array. Significant I_{DSAT} changes are visible in the outer devices for both medium (Fig. 26b) and large sizes (Fig. 26c) at both RT and LHT. When the structures are cooled down to LHT, I_{DSAT} of these outer devices changes by a factor of approximately 2 compared to RT. A statistically significant deviation of the drain current of the outer device is also visible for the small devices (Fig. 26a), but to a lesser extent.

To gain more insight into the physical mechanisms at play, the extracted (normalised) V_{TH} and β are plotted at both RT and LHT for both NMOS and PMOS devices in Fig. 27 and Fig. 28.

These devices show an average V_{TH} increase of ∼100 mV for NMOS and ∼180 mV for PMOS devices, respectively, and a β improvement by a factor of 1.3 to 1.5 at LHT compared to RT, depending on geometry.

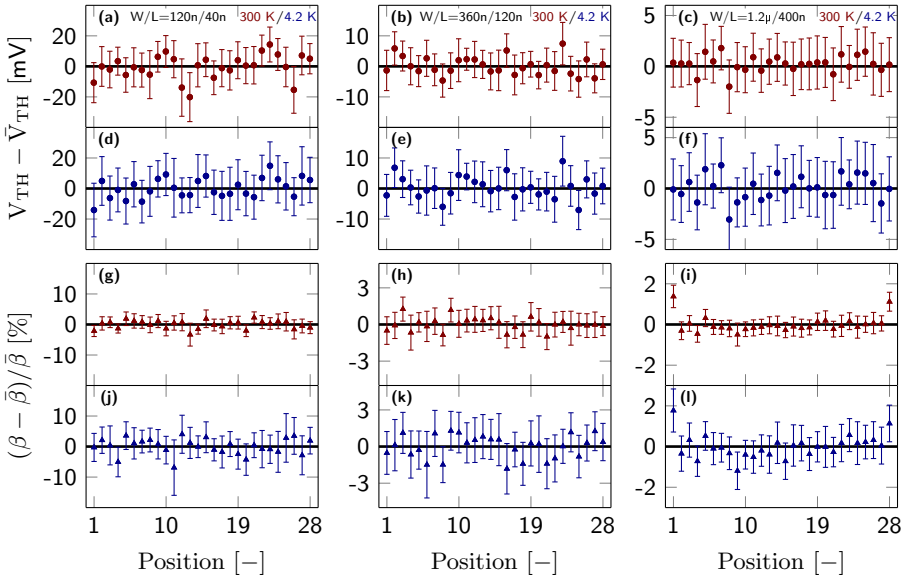

Figure 27: Normalised V_{TH} (circle) and β (triangle) as a function of device position for NMOS devices at RT (red) and LHT (blue). First column: W/L=120n/40n; second column: W/L=360n/120n; third column: W/L=1.2µ/400n. Error bars indicate 95% confidence intervals.

Starting with RT data, the small and medium NMOS devices shown in Fig. 27a, b, g and h do not exhibit significant changes at the edge of the array. For the largest geometry, a significant 1% increase in β can be observed at device positions #1 and #28 in Fig. 27i, while the V_{TH} is not affected. Similar results are found for NMOS arrays cooled down to LHT in Fig. 27.

PMOS devices start to show very significant sensitivity to array position for geometries larger than W/L=360n/120n, as plotted in Fig. 28. Considering minimum-size devices at RT, only device position #1 (Fig. 28g) shows a clear deviation from the median, while this is not the case for LHT (Fig. 28j) or other positions. Therefore this is not considered a dummy effect. The medium and large geometries at RT exhibit a significant β decrease ($\sim$1 %) in positions #1 and #28 as seen in Fig. 28h and i. The effect is stronger at LHT (Fig. 28k and l), where β decreases with $\sim$3.3 % for the outermost devices. For these positions there is also a slight V_{TH} increase, especially for the largest device with an increase of $\sim$2 mV at RT and $\sim$3 mV at LHT.

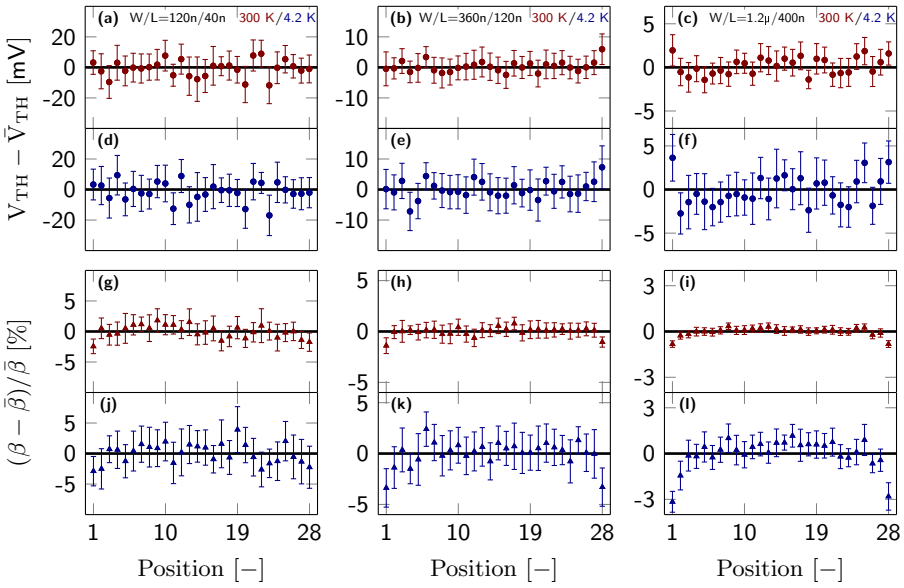

Figure 28: Normalised V_{TH} (circle) and β (triangle) as a function of device position for PMOS devices at RT (red) and LHT (blue). First column: W/L=120n/40n; second column: W/L=360n/120n; third column: W/L=1.2µ/400n. Error bars indicate 95% confidence intervals.

3.4.2 Discussion

The sensitivity of I_{DSAT} to dummy placement in Fig. 25 and Fig. 26 is found to be opposite for NMOS and PMOS. This points to an effect of piezo-resistive origin, whose coefficients have typically different signs for n- and p-type silicon [38]. The effect alters mobility as a function of mechanical stress originating from, for example, Shallow Trench Isolation (STI) surrounding each device. The effect of STI stress on MOSFETs has been known for years [39] and has been widely reported as compressive in nature, enhancing hole- and deteriorating electron-mobility [40, 41]. However, an increase in NMOS and decrease in PMOS I_{DSAT} observed in these measurements is opposite to what is typically reported. The piezo-resistive effect is highly anisotropic, resulting in changes in electron- or hole-mobility with any combination of sign, depending on crystal, device-current and stress orientation [42]. Unfortunately, the device orientation with respect to the crystal for the transistor pairs/arrays is not known. Additionally, prior works also report deviations from the often encountered compressive, longitudinal (i.e., parallel to device current), uni-axial stress. In [37] it is shown that apart from the longitudinal stress component also the transverse component needs to be taken into account, which, if compressive, can degrade PMOS mobility. In [43], PMOS insensitivity to STI

stress is reported, which was attributed to the wafer crystal orientation. The device arrays characterized in this work are placed in a rectangular STI cut-out. The large aspect ratio of the cut-out, could potentially lead to compressive transverse, and tensile longitudinal stress for the outer devices. This is different from single devices surrounded by STI and could also explain the difference observed here.
Another factor that has been shown to impact MOSFET mobility is metal coverage [44]. The reported mobility shifts as a result of metal-1 coverage (M1) are compatible with the results presented in this work. The devices in the interior of the array are impacted by the inevitable source/drain M1 interconnect of the two neighboring devices, while the two outer devices only encounter the effect of metal coverage from one neighboring device, thus also explaining the mobility shifts observed.
Apart from the mobility change, V_{TH} is also found to shift for the outer most devices in Fig. 28c and f, which can also be attributed to mechanical stress, as also reported in [37] and [43].
A practical guideline for circuit designers is that dummies can mitigate such effects, but no more than one dummy device on each side is required. Furthermore, the beneficial effect of such dummy is only significant for large devices for which device mismatch is not overpowering the stress effects.

3.4.3 Conclusion

Measurements on linear arrays of transistors uncovered a systematic mismatch related to device placement at the array edges, which was attributed to mechanical stress. It was shown as a countermeasure that, when random mismatch is not overshadowing such an edge effect, placing dummy devices at the array edge can alleviate such effect.

3.5 Conclusions

For the reliable cryogenic operation of certain precision circuits, such as ADCs, DACs and references, models that extend beyond the DC behaviour presented in the previous chapter are required during their design. The operation of such circuits is often based on matched device pairs and thus models incorporating accurate data on device matching at cryogenic temperatures are indispensable.
In this chapter, statistical data and models describing device matching in all MOSFET operating regimes, from subthreshold to strong-inversion, were presented. The Pelgom scaling-model was shown to be valid down to temperatures of 4.2 K and the drain-current matching was successfully predicted using two simple models. It was shown that device matching deteriorates at cryogenic temperatures compared to room temperature, with, in particular, a large increase of mismatch in the subthreshold regime caused by an exacerbated subthreshold-slope variability.

Effects like these can be mitigated by means of increased device size as per the Pelgrom scaling-rule, however, additional techniques like dummy device placement can be employed. It was shown that mechanical-stress induced parameter changes are amplified at very low temperatures and that placing a limited number of dummy devices can be beneficial.
These models and data allow circuit designers to make better and more informed choices concerning device geometry and placement during design time, improving overall circuit performance, (area) efficiency and yield.

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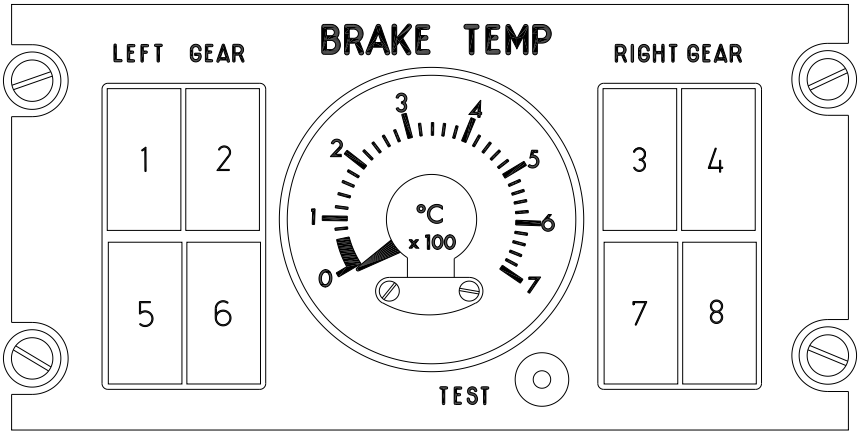
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Chapter 4

CMOS Self-Heating at Cryogenic Temperatures

4.1 Introduction

In Chapter 2 it has been shown that core device parameters, such as threshold voltage, mobility and subthreshold slope can shift significantly from their RT values at low ambient temperatures (T_{amb}). Other important phenomena that should be taken into consideration when designing cryogenic circuits, such as device matching and dummy placement, were similarly found to be temperature dependent in Chapter 3. The incorporation of device temperature in compact models extended to the cryogenic environment is thus paramount to guarantee reliable circuit simulations and hence, robust circuit operation under these conditions.
However, self-heating can raise the device temperature (T_{chan}) significantly above T_{amb}. This effect is amplified at cryogenic temperatures, as thermal properties of silicon, such as thermal conductivity (K_{th}), vary almost over 1.5 orders of magnitude in the temperature range from room temperature down to 4.2 K, as shown in Fig. 1.
This effect has actually been observed in a cryo-CMOS microwave driver for spin qubits operating at $T_{amb} = 3$ K. From measurements of on-chip temperature sensors, it was inferred that the chip was subjected to self-heating exceeding 10 K for a dissipated power above 400 mW [3].
Self-heating does not only impact the characteristics of the device itself, it can also propagate through the surrounding silicon forming thermal feedback loops with neighboring devices [4]. While this can be already critical in electronic cryogenic circuits, it will become crucial in future system-on-chip (SoC), integrating both electronics and qubits, which are extremely sensitive to any thermal crosstalk [5].

Parts of this chapter have been published in IEEE JEDS [1]

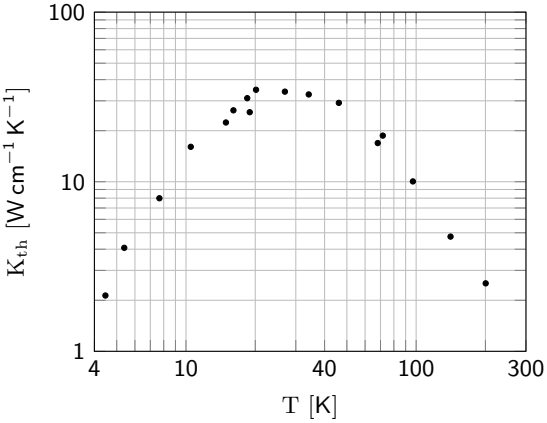

Figure 1: Thermal conductivity of silicon over temperature, replotted from [2].

Therefore, this chapter is devoted to an investigation of the actual device temperature as a function of ambient temperature and dissipated power in order to add this thermal information to the modeling flow.
Self-heating at room temperature has received much attention in literature, specifically focused on silicon-on-insulator (SOI) technologies as the buried oxide (BOX) poses a thermal impedance 2 orders of magnitude higher compared to that of bulk silicon at this temperature [2, 6].
Far less attention was devoted to studies on self-heating at cryogenic temperatures. Early work dates back to the beginning 1970s [7] and has been extended more recently by investigations on bulk MOSFETs [7, 8, 9, 4, 10], resistors [11, 12] and SOI [13, 14]. Self-heating was investigated both by measurements of the device temperature itself [13, 14, 12] and by placing temperature sensors in the vicinity of on-chip heaters [4, 11, 15, 16, 17, 12]. All these works show that self-heating is exacerbated at cryogenic temperatures and that the effect is highly dependent on device geometry (size, aspect ratio) and power density. This variability is clearly observed in recent cryo-CMOS integrated circuits for qubit interfacing, as SH ranged from 1 to 3 K in a 40-nm bulk-CMOS high-speed ADC with low power density [18] to more than 10 K in a 22-nm FinFET microwave driver [3]. As device geometry and power density differ considerably between advanced bulk CMOS nodes and the previously studied mature technologies, it is necessary from a modeling perspective to characterize self-heating on devices better resembling those employed in practical cryo-CMOS designs [19, 18, 20, 21], both in geometry and power density. Understanding the impact of self-heating is especially crucial for the cryo-CMOS low-noise amplifiers (LNA) necessary for the detection of the weak signals from quantum processors, as an increase of the device temperature of only a few Kelvin can strongly affect the noise performance, e.g., in a thermal-noise-limited amplifier in which the noise is directly proportional to the device temperature.

In this chapter, the effects of self-heating on the device itself and on the surrounding silicon are characterized and modeled using a typical NMOS device similar to the ones found in cryogenic circuits.
This chapter is structured as follows: Section 4.2 describes the test chip, measurement setup and the device calibration. Section 4.3 presents the measurement results, which are discussed and modeled in Section 4.4. Finally, conclusions are drawn in Section 4.5.

4.2 Test Structures and Measurement Setup

A test chip was taped-out, specifically designed for the characterization of self-heating at deep-cryogenic temperatures. The chip was manufactured in the TSMC 40-nm bulk-CMOS process. Fig. 2 and Fig. 3e show a simplified overview of the test structures and a die micrograph, respectively.
Three NMOS devices are employed as heaters (H1, H2 and H3), formed by a 5 fingered device with fingers measuring $W/L = 12\,\mu m/40\,nm$ each, individually selectable (separated gates and drains) and able to dissipate $\approx 7\,mW$ of power (P_H). The gates of the two MOSFETs separating H1 and H3 from H2 are connected to $\mathrm{V_{SS}}$ in order to electrically isolate the heaters from each other (Fig. 2 top). The center heater (H2) has additional connections available, enabling the measurement of the gate resistance, further discussed in Section 4.2.1. The choice for NMOS over a PMOS device was motivated by its higher current driving capability (and thus power), as no significant thermal differences are expected between both types. In addition to the MOSFETs, a linear array comprising 52 diodes, whose functionality was investigated in a previous feasibility study, is placed perpendicular to the channel, along a line through the center of the heaters (Fig. 2 top). These diodes act as temperature sensors, enabling the detection of the spatial thermal profile in the heaters' vicinity, further discussed in Section 4.2.2.

4.2.1 Gate Test Structure

To enable T_{chan} characterization through a range of T_{amb}, gate thermometry is employed, in which the calibrated temperature dependence of the gate resistance (R_G, see Section 4.2.4) is used as a temperature sensor [14, 22]. Kelvin connections to both top (V_{GT}, I_{GT}) and bottom (V_{GB}, I_{GB}) side of the H2 gate are therefore available to mitigate the impact of temperature dependence of back-end metals and parasitics on the resistance measurement (see Fig. 2).
The assumption was made that the gate and the channel are tightly thermally coupled, since only a thin ($< 3\,nm$) insulating layer separates them, similar to other works [10, 14, 23, 24]: $T_G \approx T_{chan}$.

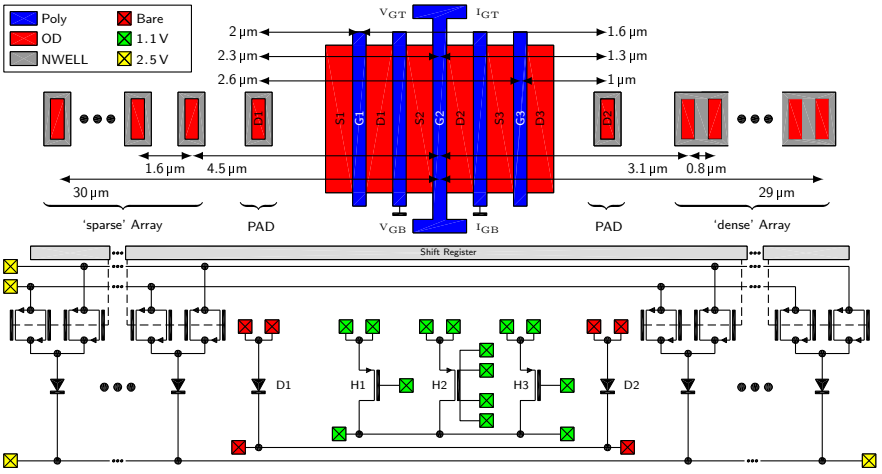

Figure 2: Simplified layout (top) and schematic overview (bottom) of the gate and diode test structures. H2 has Kelvin connections to its gate, comprising the V_{GT}, I_{GT}, V_{GB} and I_{GB} contacts. D1 and D2 are the two pad-accessible diodes (PAD). The different bond pad voltage domains are indicated. All digital blocks have been omitted for clarity.

4.2.2 Diode Test Structures

For the measurement of the thermal profile around the heaters, the substrate temperature is sensed by measuring the calibrated thermal dependency of the voltage drop (V_A) across P^+/NWELL silicon diodes operated at a constant current I_0. A graphical representation of this structure can be seen in Fig. 2, comprising pad-accessible diodes and a multiplexed diode array.

Pad-accessible diodes: two diodes (D1 and D2 in Fig. 2) are placed in close vicinity to the heaters (one on each side), with connections directly available via bond pads, to measure the substrate temperature at small distances from the heaters with high spatial resolution (300 nm). Different combinations of heaters (H1/H2/H3) and diodes (D1/D2) allow for a total set of 6 distances: $d = \{1, 1.3, 1.6, 2, 2.3, 2.6\}$ µm.
Because of the direct connection to the pads, these diodes have been used as benchmark to verify the correct operation of the pass gates in the multiplexed diode array.

Multiplexed diode array: a multiplexed array comprising 50 diodes to characterize the substrate temperature over larger distances, up to 30 µm from the heaters, enables automatic characterization. Thick-oxide pass gates were employed to allow the diode potential to rise above the nominal supply voltage (1.1 V), required as

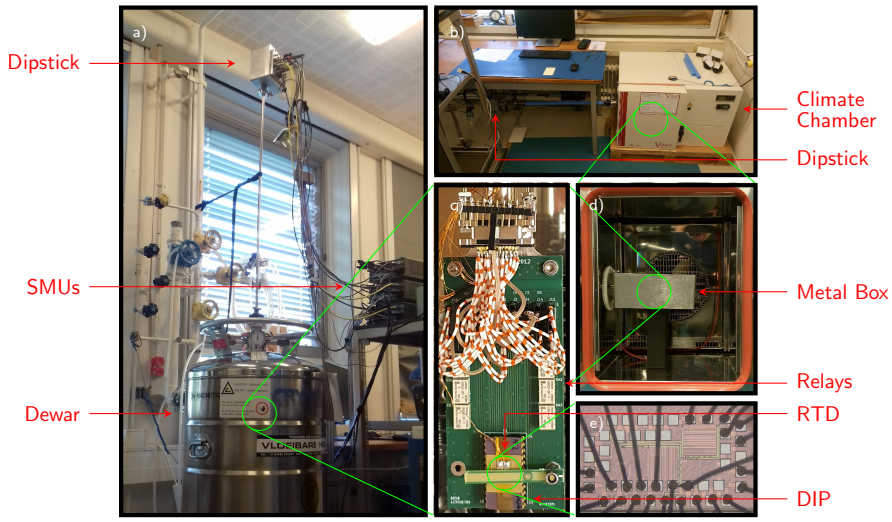

Figure 3: Measurement setup: a) dipstick in LHe Dewar; b) dipstick in climate chamber; c) PCB at the end of the dipstick; d) climate chamber internal view; e) die micrograph.

$V_A|_{I_0}$ increases with decreasing temperature.
An array was placed on both sides of the heaters. The 'dense' array (Fig. 2 top right) comprises diodes placed at the minimum allowed distance, resulting in a spatial resolution of 0.8 µm and is used for the actual measurements. The 'sparse' array (Fig. 2 top left) is a copy of the 'dense' array with every other device removed, resulting in less contact/metal density compared to the latter array. By comparing the results from the two arrays, it can be verified if the metal/contact density significantly impacts the thermal profile due to heat-leakage via the biasing metal lines.

4.2.3 Measurement Setup

A photographic overview of the measurement setup can be seen in Fig. 3. The dies were glued and wire-bonded to ceramic DIP packages, which were fitted in a socket on a PCB mounted at the end of a dipstick (Fig. 3c). The PCB contains relays, enabling different configurations to be switched in and out during characterization. A Cernox type Resistance Temperature Detector (RTD) clamped to the package was used to measure T_{amb}.
Measurements at $T_{amb} \geq$ RT were carried out by inserting the end of the dipstick into a Vötsch VTM7004 climate chamber (Fig. 3b). The PCB inside the climate chamber was enclosed by a metal box to improve thermal stability, thus reducing

temperature drift/gradients over time (Fig. 3d).
The dipstick was inserted into a Dewar containing LHe for the cryogenic measurements (Fig. 3a). The height of the sample above the LHe level modulates T_{amb}.
Electrical characterization was carried out by 3 Keithley 2636B SMUs.

4.2.4 Calibration

The temperature characteristics of both the gate resistor and the silicon diodes need to be calibrated before they can serve as temperature sensors. During calibration, the parameters of interest (R_G and $V_A|_{I_0}$) as a function of T_{amb} are characterized while T_{amb} is slowly varied with all heaters disabled.
For $T_{amb} \geq$ RT, the climate chamber is used to generate a slowly varying T_{amb}: after warming up to $\approx$ 350 K, the climate chamber is switched off and allowed to (slowly) cool down while calibration takes place. Cryogenic calibration was carried out by manually lowering the dipstick into the Dewar, cooling down the sample.

Diode Calibration: for the 2 pad-accessible diodes, the I_A-V_A curves are measured as a function of T_{amb}. Deviation from ideal exponential behaviour at cryogenic temperatures can be observed in Fig. 4, left. From these curves, V_A as a function of T_{amb} is subsequently extracted by a horizontal cut along the line $I_A = I_0$ as indicated in the figure. As recording the full I_A-V_A characteristics for all 50 diodes in the array would take a prohibitive amount of time, V_A is directly measured by forcing $I_A = I_0$ for these devices. Since there is some variability present among different diodes, all diodes need to be calibrated individually, see Fig. 4, right.
An example of a diode calibration curve and the resulting temperature sensitivity can be observed in Fig. 5 top and bottom, respectively. The minimum measurable channel temperature change ΔT_{min} was calculated as per [14] to be 0.05 K and 2 K at $T_{amb} = 50$ K and 11 K, respectively.
The de-facto standard value (for commercial diode temperature sensors) of $I_0 =$ 10 µA was used for $T_{amb} \geq$ RT. To increase the sensitivity at deep-cryogenic temperatures, the current bias was reduced to $I_0 = 1$ µA for $T_{amb} < 300$ K. The temperature drift (T_{drift}) was monitored and the calibration was repeated in case of excessive values. The maximum temperature drift (T_{drift}) during a single I_A-V_A characterization was 0.6 K ($T_{amb} \geq$ RT) and 1 K ($T_{amb} <$ RT).

Gate Calibration: R_G is measured by setting $V_{GB} = 0$ V and simultaneously sweeping V_{GT} from 0 to 50 mV, see Fig. 2, while recording the gate resistor current (I_G). Note that V_D was left open to avoid any current and consequent heating in the device. R_G is extracted from the slope of a first-order fit of the I_G-V_{GT} characteristic. The full gate calibration curve can be observed in Fig. 5 top. The maximum T_{drift} during a single R_G characterization was 0.25 K ($T_{amb} \geq$ RT) and 0.4 K ($T_{amb} <$ RT). The gap between 220 K and 300 K results from limitations in the minimum and maximum attainable temperature of the climate chamber and

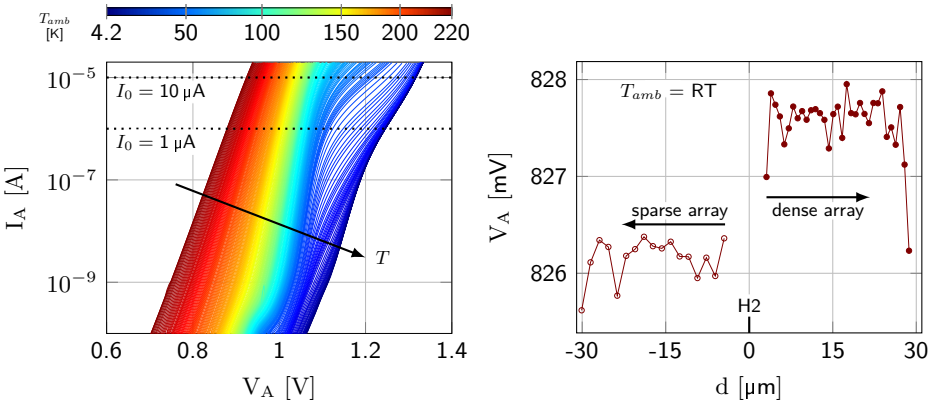

Figure 4: left) I_A-V_A curves of pad-accessible diode D1 at ambient temperatures (T_{amb}) ranging from 220 K down to 4.2 K. The two horizontal cuts along $I_A = I_0$, from which the calibration curves are extracted, are indicated. right) Voltage drop (V_A) measured at $I_0 = 10\,\mu A$ for diodes in the 'dense' (filled dots) and 'sparse' (open dots) array operated at RT with $P_H = 0$ as a function of distance from center heater (d).

LHe Dewar, respectively.

4.3 Experimental Results

This section presents the measurement results, focusing on the experimental methods and discussing data validity. In-depth analysis and discussion of the reported data is given in Section 4.4.

4.3.1 Gate-resistance Measurements

In the first step of the T_{chan} characterization, the sample is brought to the target T_{amb} by placing it at a certain height above the LHe level, or for RT measurements, by keeping it inside the (switched-off) climate chamber. When T_{amb} stays within $\pm$ 0.2 K of the set point, thermalization is assumed and different power levels are dissipated in the center heater (P_{H2}) by stepping V_D in a staircase pattern: V_D = {0, 0.05, 0.1, ..., 1.1} V, while V_{GB} and V_{GT} are both set to 1.1 V. Following each step in V_D, a 10 s delay was added to allow the structure to reach thermal equilibrium. V_{GT} is subsequently swept from 1.1 to 1.15 V, while both I_D and I_G are recorded. Finally, the routine described above is repeated for multiple T_{amb}. R_G is extracted from the I_G-V_{GT} data as per the calibration routine described in Section 4.2.4. The T_{chan} is inferred from these extracted R_G values by local interpolation of the calibration curve (Fig. 5 top) around that operating point.
As one side of the gate (V_{GT}) experiences a voltage change of 50 mV during mea-

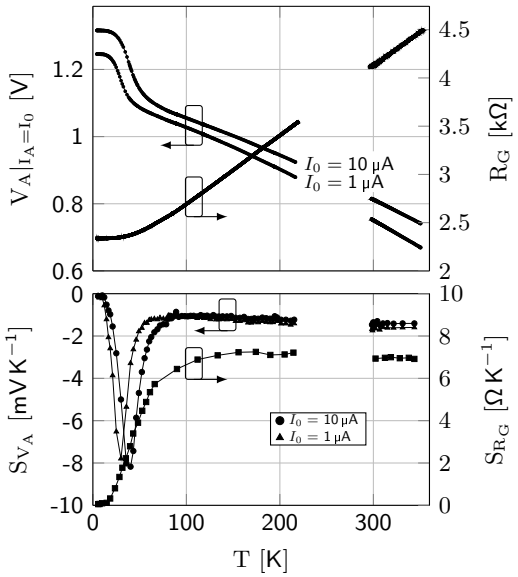

Figure 5: Calibration details. Top) calibration curves for the gate resistance (R_G) and the voltage drop across one of the pad-accessible diodes (V_A), the latter extracted at two different I_0 values, see also Fig. 4. Bottom) temperature sensitivity of the gate resistance (S_{R_G}) and diode voltage (S_{V_A}) as a function of temperature (T) extracted from the calibration curves.

surement, I_D increases slightly. The dissipated power is therefore calculated using the mean I_D, $P_{H2} = V_D \cdot \bar{I}_D$, resulting in a maximum error of 2.5 % in power.
The absolute T_{chan} as a function of P_{H2} for different T_{amb} is plotted in Fig. 6. The channel self-heating, ΔT_{chan}, is derived from these data by subtracting the extracted temperature at $P_{H2} = 0$ for each T_{amb} from the corresponding curve, as shown in Fig. 7. As the temperature sensitivity of R_G drops to very low values for $T_{chan} < 11$K, the RTD temperature reading was used for compensation instead of $T_{chan}|_{P_{H2}=0}$ for these curves.
In order to protect against sudden temperature changes in the helium vapour (caused by varying pressure in the building's helium recovery system), the T_{amb} readings of the RTD are monitored: measurements are discarded when T_{drift} exceeds ± 0.5 K during a gate measurement at a single V_D set point. In addition, these readings are also cross-checked with the extracted $T_{chan}|_{P_{H2}=0}$ as an additional safeguard.

4.3.2 Diode Measurements

The diode characterization is very similar to that of the gate (Section 4.3.1); however, apart from H2, in this case, H1 and H3 can additionally be used as heaters.

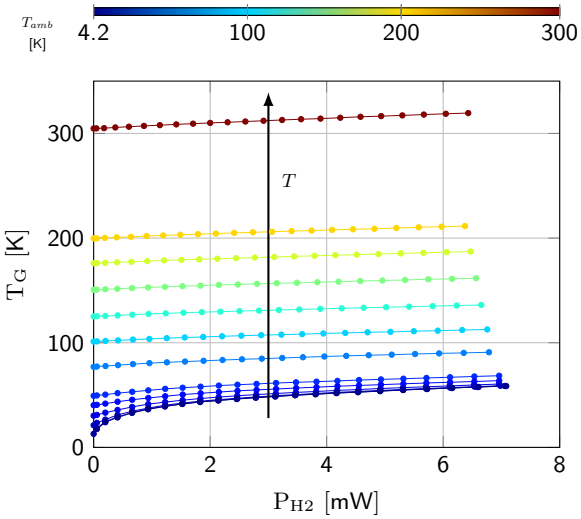

Figure 6: Absolute channel temperature (T_G) as a function of dissipated heater power (P_{H2}) at different ambient temperatures: T_{amb} = {4.2, 10, 20, 30, 40, 50, 75, 100, 125, 150, 175, 200, 300} K.

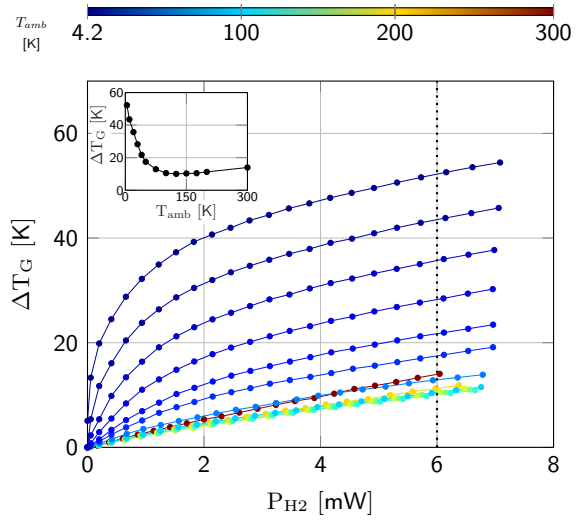

Figure 7: Channel self-heating (ΔT_G) as a function of dissipated heater power (P_{H2}) for different ambient temperatures (T_{amb}). Inset indicates interpolated SH at fixed heater power (P_{H2} = 6 mW, see dashed line) as a function of T_{amb}. Plot derived from data in Fig. 6.

The characterization and analysis of the diode measurements can again be split into two groups:

Pad-accessible diodes: T_{amb}, power dissipation and thermalization are handled as per the gate measurements. For each V_D set point, V_A is swept while I_A and I_D are recorded. These data are collected for all 6 combinations of H1, H2 or H3 with D1 or D2 over all T_{amb} targets. From the I_A-V_A data, $V_A|_{I_A=I_0}$ is extracted in the same manner as during diode calibration and the diode temperature (T_D) is inferred with the use of the individual diode calibration curves (Fig. 5 top).
The absolute T_D for T_{amb} = RT and 4.2 K as a function of the enabled heater and the heater power can be seen in Fig. 8.
Finally, the substrate heating (Fig. 9) is calculated by compensating each absolute temperature curve in Fig. 8 with the corresponding temperature extracted at $P_{Hn} = 0$, identical to the procedure followed in the channel SH analysis, while for $T_{amb} < 10$ K the temperature reading of the RTD was used.

Multiplexed diode array: the measurement and analysis of the diode array follow the same routine as the pad-accessible diodes described above; however, due to the large number of devices (50), resulting in an increased measurement time, some adaptions were implemented to mitigate long-term T_{drift}: since sub-µm resolution is not required, only H2 was enabled; V_A of each diode is directly measured by forcing $I_A = I_0$ and the number of V_D set points was reduced to the set V_D = {0, 0.1, 0.2, ..., 1.1} V. With these measures in place, characterization of the full array still consumes a considerable amount of time, therefore T_{drift} needs to be taken into account.
Long-term temperature drift is only present for samples in helium vapour, caused by time-varying pressure in the building's helium recovery system.
To further minimize T_{drift} impact, each diode in an array is fully characterized over all V_D set points (power levels), before switching to adjacent devices. During characterization of a single diode, T_{drift} is assumed to be small (comparable to that of the pad-accessible diodes) as the characterization time is relatively short: $\approx$ 115 s. However, there is still a long-term T_{drift} present between diode measurements, since a full array characterization takes $\approx$ 97 min. Therefore, the same compensation employed in the channel and pad-accessible diode characterization is applied here, which in this case, additionally auto-zeros the drift component between individual diode measurements.
The long-term drift is assumed to be small enough to maintain T_{amb}, however, large enough to distort the SH measurement, the effect of which is dependent on the height above the LHe. During the full array characterization, the RTD readings are therefore used to guard against too large short- and long-term T_{drift}. The allowed short-term drift (during single-diode measurements) is as per the pad-accessible diode characterization, while the long-term drift must stay within $\pm$0.5 K of the target T_{amb} for the data not to be discarded.

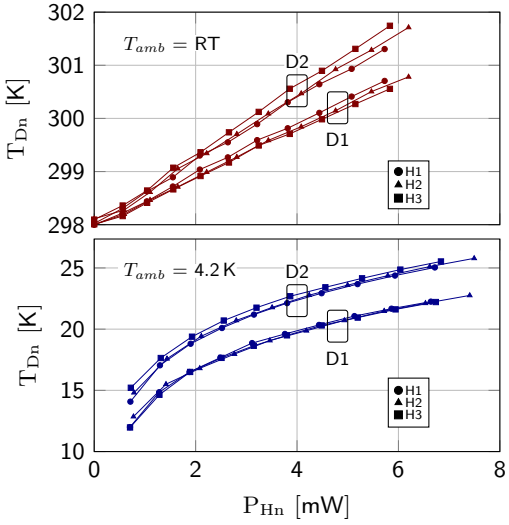

Figure 8: Absolute diode temperature (T_{Dn}) measured with all 6 heater/diode combinations as a function of heater power (P_{Hn}) at both T_{amb} = RT (top) and 4.2 K (bottom). At 4.2 K for P_{Hn} below 700 µW, readings are discarded due to limited temperature sensitivity, as explained in Section 4.4.1.

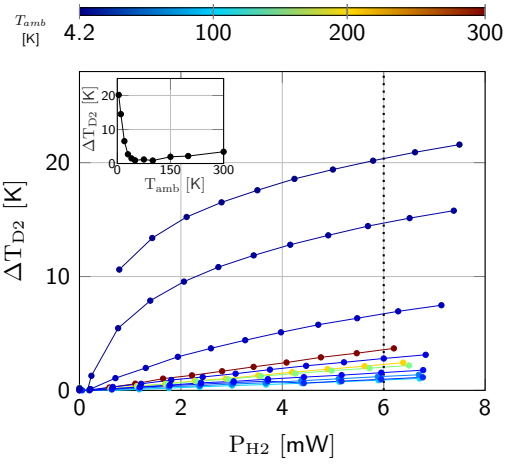

Figure 9: Diode temperature rise (ΔT_{D2}) of D2 as a function of heater power (P_{H2}) at different ambient temperatures: $T_{amb} = \{4.2, 10, 20, 30, 40, 50, 75, 100, 150, 200, 300\}$ K. Inset indicates interpolated temperature rise at fixed heater power ($P_{H2} = 6$ mW, see dashed line) as a function of T_{amb}.

Extracted absolute substrate temperatures as a function of distance for $P_{H2} = 0$ and $P_{H2} = 6.3\,\text{mW}$ measured at $T_{amb} = \text{RT}$ are plotted in Fig. 10.
Substrate heating as a function of distance at $P_{H2} = 6\,\text{mW}$ measured at different T_{amb} can be observed in Fig. 11. The corresponding measured temperatures of the pad-accessible diodes and the channel have been added to the figure.
The temperature profiles associated with different heater powers at a fixed T_{amb} = 160 K are plotted in Fig. 12, exemplifying the effect of T_{drift} on a single diode measurement.

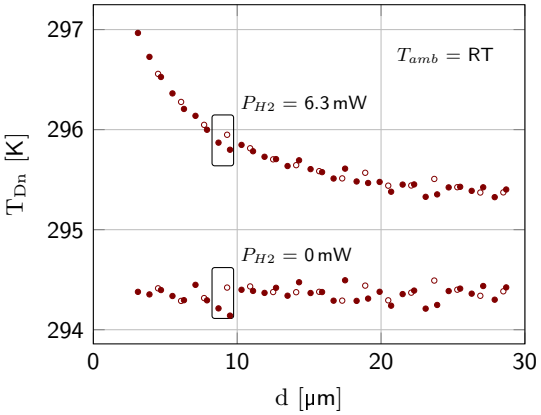

Figure 10: Substrate temperature measured by the diode arrays (T_{Dn}) as a function of distance from the center heater (d) at low ($P_{H2} = 0$) and high ($P_{H2} = 6.3\,\text{mW}$) heater power at $T_{amb} = \text{RT}$. Data from the 'dense' (filled dots) and 'sparse' (open dots) arrays have been overlaid.

4.4 Self-Heating: Discussion, Modeling and Take-Aways

4.4.1 Diode-Based Temperature Sensing

Deviation from exponential behaviour in cryogenically operated diodes shown in Fig. 4, are compatible with previous observations in literature [25, 26]. The sharp V_A increase for $T_{amb} < 50\,\text{K}$ can be attributed to carrier freeze-out [26, 27, 28], also present in diodes specifically designed for cryogenic temperature sensing [29]. Consistently and significantly lower $V_A|_{I_0=const}$ were found for diodes in the 'sparse' array compared to the 'dense' array as indicated in Fig. 4. Most likely these differences can be ascribed to a combination of two effects: 1) diodes in the 'dense' array lie in a single continuous NWELL, while each 'sparse' diode sits in its own

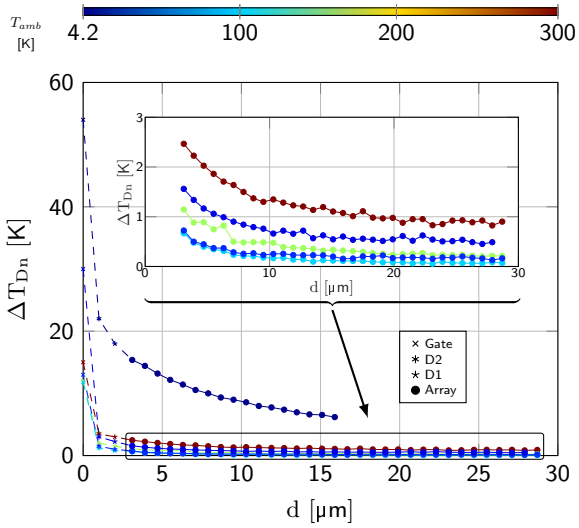

Figure 11: Substrate heating (ΔT_{Dn}) measured by the 'dense' array as a function of distance from the center heater (d) at high heater power ($P_{H2} = 6.3\,\text{mW}$) and different ambient temperatures: $T_{amb} = \{4.2, 30, 50, 100, 160, 300\}$ K. Data from the gate and pad-accessible diode structures are also plotted. The inset indicates a zoomed-in plot of the diode array measurements with the 4.2 K curve omitted for increased visibility.

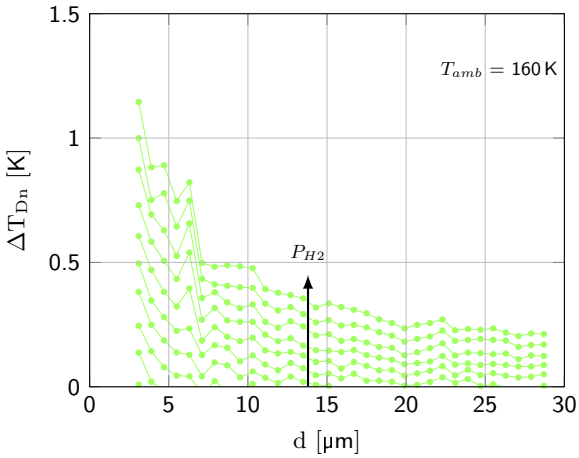

Figure 12: Substrate heating measured by the 'dense' array (ΔT_{Dn}) as a function of distance to the center heater (d) at different heater power levels: $P_{H2} = \{0.6, 1.2, 1.7, 2.3, 3.0, 3.6, 4.3, 5.0, 5.8, 6.6\}$ mW. $T_{amb} = 160\,\text{K}$. Only curves corresponding to P_{H2} values causing significant heating are shown.

well. This causes differences in doping densities, and subsequent electrical characteristics, through the Well Proximity Effect (WPE) [30]. 2) the different Shallow Trench Isolation (STI) widths between diodes in the two arrays cause different mechanical stress to be present, altering the carrier transport parameters through the piezo-junction effect [31].
The calibration curves of V_A and R_G in Fig. 5 show a near-constant temperature sensitivity of $-1.2\,\mathrm{mV/K}$ and $0.18\,\%/\mathrm{K}$ for $T_{amb} > 50\,\mathrm{K}$, respectively. Freeze-out causes a large increase in V_A sensitivity below this temperature, however, sensitivity drops to a very low value for $T_{amb} < 10\,\mathrm{K}$, compatible with measurements in [28]. I_0 was reduced to $1\,\mu\mathrm{A}$ during cryogenic measurements to mitigate the latter effect [25], the value being a trade-off between improved sensitivity and increased impact of array leakage at deep-cryogenic temperatures [32]. The temperature sensitivity of R_G decreases to a value close to zero for $T_{amb} < 11\,\mathrm{K}$, in-line with metal-like behaviour [33]. For $T_{amb} > 50\,\mathrm{K}$, carrier transport is limited by phonon scattering, exhibiting a positive temperature coefficient (PTC), while below this temperature transport becomes increasingly limited by impurity scattering, which being temperature independent, prevents further resistance decrease.
Due to the diminishing temperature sensitivity of both the diodes and gate resistance, the reading of T_D and T_G have been excluded for temperatures below 10 K and 11 K, respectively. However, due to the rapid temperature increase to values above 10 K already at low P_H for $T_{amb} = 4.2\,\mathrm{K}$, this results in the loss of only a small part of the data (see Fig. 6 and 8).
SH due to biasing of the temperature sensors (inducing a power dissipation below $8\,\mu\mathrm{W}$) is insignificant for the range of interest ($P_H > 1\,\mathrm{mW}$), as it has been simulated in COMSOL to cause a SH below 20 mK in the diodes.

4.4.2 Channel Temperature Sensing

From the T_{chan} measurements in Fig. 6, an agreement between the RTD temperature reading and extracted $T_{chan}|_{P_{H2}=0}$ was found, indicating the correct operation of the setup through the full temperature range. Larger SH at equal P_{H2} can be observed for lower temperatures in Fig. 7: $\Delta T_{chan} \approx 14\,\mathrm{K}$ (RT) vs $\Delta T_{chan} \approx 52\,\mathrm{K}$ (4.2 K) at $P_{H2} = 6\,\mathrm{mW}$. For $T_{amb} < 100\,\mathrm{K}$, ΔT_{chan} is highly non-linear with respect to dissipated power, resulting in large SH for low P_{H2} in this temperature range, also observed by [16] and [10]. As shown in the inset of Fig. 7, the SH behaviour from RT down to 4.2 K for a given P_{H2} shows a decrease down to 125 K, below which its effect starts to increase again, exhibiting a dramatic increase below $T_{amb} = 75\,\mathrm{K}$. This behaviour hints to a temperature-dependent R_{th}, with a minimum at $\approx 100\,\mathrm{K}$, also shown in other works [16, 12]. Previously reported values of the minimum lie between 77 K and 250 K and have been attributed to the impact of parasitic R_{th} (package, glue, etc.) dominating at these low temperatures in bulk CMOS [12]. Although the adopted test setup does not exactly reproduce prior work's experimental conditions, e.g., the chips are in direct contact

of gaseous/liquid Helium unlike the vacuum environment used in [12], the shift in the minimum from the expected value is attributed to the parasitic thermal resistance of the measurement setup. A more precise estimation of the effect of R_{th} may require additional experimental effort and its outside the scope of this work. The crowding of T_{chan} between 40 K and 60 K for deep-cryogenic temperatures, visible in Fig. 6 for heating power above 1 mW, is a direct consequence of this R_{th} behaviour: below the R_{th} minimum, R_{th} has a negative temperature coefficient (NTC), which impedes SH more and more as T_{chan} approaches the minimum. The implications of this observed effect are further discussed in Section 4.4.5.
Comparing the SH magnitude extracted in this work with literature, much higher SH was found in SOI technology at comparable power densities [14]. As the main R_{th} in such technology is determined by SiO_2, which exceeds that of Si by ≈ 2 orders of magnitude, a large difference in SH is expected. Regarding bulk technology, in which no BOX exists, the geometry and area of MOSFET devices significantly impact SH. Far lower SH was observed in a large square heater in bulk technology [12], which has significantly more enclosing area and hence a much lower R_{th} to the surrounding silicon compared to the wide/short devices measured in this work. Also, the power density is orders of magnitude less compared to that in this work. The values published on a bulk device with an aspect ratio better resembling the structures characterized in this work, but with much larger W and L, show a slightly smaller SH effect. The structure in question had $\approx 100\times$ larger area [4] and considerably lower power densities. The preliminary work done by [10] shows values that compare very well with the measurements presented here, although no geometrical details are given.
These results stress the importance of geometry on SH, which is why in this work a transistor geometry comparable to the ones employed in practical cryo-CMOS circuits was chosen.

4.4.3 Spatial Thermal Measurements

Observations in line with the previous two sections can be made for the pad-accessible diodes. Both diodes show a smaller ΔT_D compared to the ΔT_{chan} at identical conditions, as the effect of heating falls off rapidly with a $1/d^n$-law (with d the distance to the heater and n a factor between 1 and 2): at $T_{amb} = 4.2$ K, 30 K less ΔT_D was measured 1 µm from the heater compared to ΔT_{chan} itself, see Fig. 8 and 9. Again, larger ΔT_D at cryogenic temperatures compared to RT was observed: $\Delta T_D \approx 3.5$ K (RT) vs $\Delta T_{diode} \approx 21$ K (4.2 K) at $P_H = 6$ mW, measured at 1 µm from the heater.
All 6 diode/heater combinations are distinguishable at both RT and 4.2 K in Fig. 8, with $T_{D2} > T_{D1}$, as D2 is closer to the heater than D1. The ΔT_D as a function of the enabled heater is flipped between D1 and D2, reflecting the mirror symmetry of the structure (see Fig. 2 top).
In Fig. 9, a similar behaviour as in the T_{chan} measurements can be observed in the

pad-accessible diodes below 30 K. The inset clearly shows the same behaviour: a decreasing ΔT_D with decreasing T_{amb} with a minimum at $\approx$ 100 K, which compares well with the channel measurement.
Additional cryogenic effects were observed in the heaters, see Fig. 8. At $T_{amb} =$ 4.2 K, the power in H1-H3 increases by 17 % to 20 % at equal bias conditions compared to RT, attributed to the improved mobility, resulting in an increased I_D and P_H. At equal T_{amb}, H2 was able to dissipate consistently more power compared to H1 and H3. H2 is effectively shielded from STI stress by adjacent devices (H1 and H3), which alters carrier transport parameters (and thus I_D and P_H) through the piezo-resistive effect [31].
Another interesting observation on the SH structure is the heat propagation from the heaters to the 'dense' and 'sparse' diode arrays. As seen in Fig. 10, there is good agreement between the T_D in both arrays, indicating no significant effects of metal/STI density on the thermal transport for these measurements, as was described in Section 4.2.2. The readings at $P_{H2} = 0$ correlate well with the RTD readings and an agreement within $\pm$0.25 K between both 'dense' and 'sparse' diodes was found at both low and high P_{H2}; the latter indicates a stable T_{amb} and a successful calibration. The temperature mismatch between the two arrays is mainly due to the large time span between individual measurements, as each array is fully characterized before switching to the other. Compatibility of the array data with both channel and pad-accessible diode measurements can be seen, the shape corresponding to simulations shown by [12].
The substrate ΔT falls off with the distance d from the heater for all measured T_{amb}, following a similar shape to ΔT measured at RT, see Fig. 11. At $T_{amb} =$ 4.2 K, the observable d range is limited as the substrate temperature drops below 10 K for $d >$ 15 µm, as discussed previously. The ΔT_D evolution over T_{amb} matches the pad-accessible diode data, e.g. a minimum at $\approx$ 100 K. At T_{amb} = 4.2 K severe substrate heating was observed, as much as 7 K, measured 15 µm from the heater dissipating $P_{H2} =$ 6.5 mW.
Substrate heating at $T_{amb} =$ 160 K as a function of P_{H2} (Fig. 12) uncovers detectable substrate heating 30 µm from the heater at $P_{H2} >$ 3.6 mW, while negligible heating is observed at $P_{H2} \leq$ 0.6 mW. A 0.1 K short-term T_{drift} is visible, impacting the diode measurement at $d =$ 6.3 µm.

4.4.4 Ultra-Wide-Temperature Self-Heating Model

In order to make the IC design work-flow cryo-SH aware, SH was modeled via a similar approach as in [14], but for bulk CMOS. First, the differential thermal resistance ($R^*_{th} = d\Delta T_{chan}/dP_H$) has been calculated from data in Fig. 7, and plotted as a function of absolute channel temperature ($T_{chan} = T_{amb} + \Delta T_{chan}$) in Fig. 13. The extracted R^*_{th} at $T_{amb} <$ 50 K partially overlap, proving the validity of the measured channel SH. Since SH in bulk is far less pronounced compared to SOI, and even less at higher temperatures, the T_{chan} range for $T_{amb} >$ 50 K is limited

and gaps appear in the R^*_{th} curve. The previously discussed minimum and rapid increase in SH at deep-cryogenic temperatures are also reflected in this curve. The shape of the R^*_{th} curve, and in particular the deviation from the expected R^*_{th} valley around 40 K, is compatible with the one shown in [12]. This curve illustrates that a single function is able to describe the complete R^*_{th} behaviour of this structure over the full temperature range from RT down to 4.2 K, and can thus be employed to model SH over P_H and T_{amb}. As the data at deep-cryogenic temperatures are similarly shaped to those in [14], but deviates at higher temperatures (containing a minimum, not monotonically decreasing), R^*_{th} was split into two regions, only to aid fitting. For $T_{chan} \leq 70$ K Eq. (4.1) [14] was used:

$$R^*_{th} = \frac{R^*_{th0}}{1 + \left(\frac{T}{T_0}\right)^n}, \tag{4.1}$$

where R^*_{th}, n and T_0 are fitting parameters, the first being geometry dependent whose modeling is beyond the scope of this work. For $T_{chan} > 70$ K a simple parabolic function was fitted to the data to capture the minimum and the PTC behavior, both shown in Fig. 13. Finally, these two fitted functions and Eq. (4.2) [14] were used to predict SH as a function of T_{amb} and P_H.

$$P = \int_0^{\Delta T} \frac{d\Delta T'}{R^*_{th}(T_{amb} + \Delta T')} \tag{4.2}$$

The resulting models for various T_{amb} are plotted in Fig. 14. These plots show that the very simple Eq. (4.2) is capable of successfully predicting SH over the full T_{amb} range from 4.2 K up to RT, including both the linear and square-root-like behaviour, with < 3 K error in the 0 to 7 mW P_H range.

4.4.5 Self-Heating Impact on Cryo-CMOS Circuits

While the cryo-SH data and modeling presented above could enable the next steps in reliable cryo-CMOS design, conclusions on the impact of circuit behaviour can already be drawn. Although SH is indeed severe for T_{amb} below 50 K (see Fig. 7), T_{chan} will not exceed an absolute temperature above 60 K even for a dissipated power of a few mW's, due to the minimum in the thermal resistance, as clearly highlighted by replotting the data from Fig. 6 in Fig. 15. Since the key transistor parameters, such as threshold voltage, current factor and subthreshold slope, as well as passive-device characteristics, such as R_G (see Fig. 5), show little variation at temperatures below 50 K [34, 35], SH would not significantly impact the circuit bias conditions and its dynamic performance, causing a relative temperature insensitivity in this regime. This effect can also explain the absence of the negative output conductance characteristic of self-heating in cryo-CMOS devices [36].

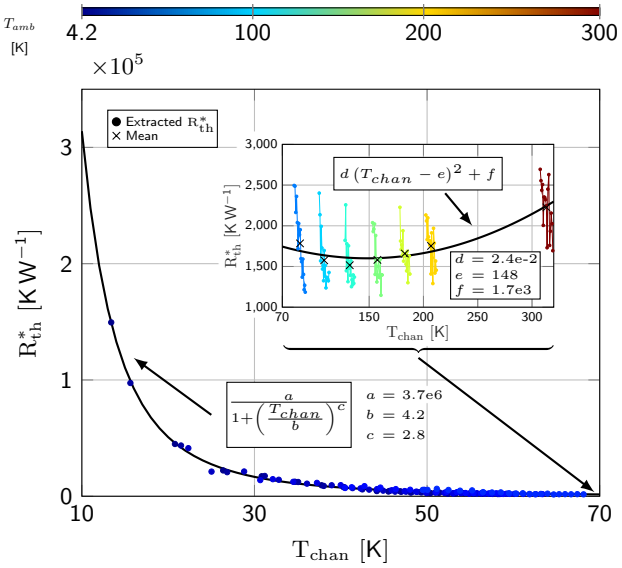

Figure 13: Extracted differential thermal resistance (R^*_{th}) as a function of channel temperature (T_{chan}) derived from data shown in Fig. 6. Data from different ambient temperatures (T_{amb}) are indicated by colors. The inset shows the extracted data at T_{chan} $>$ 75 K for visibility. Fitting parameter values are indicated in the figure.

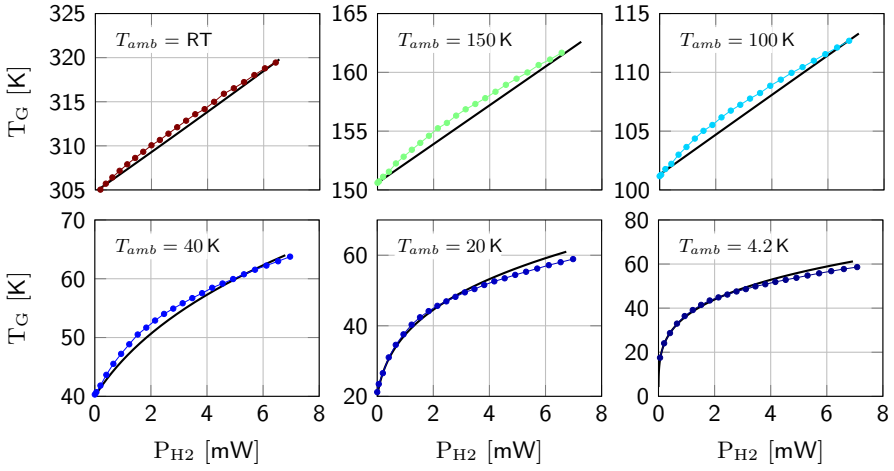

Figure 14: Absolute gate temperature (T_G) as a function of heater power (P_{H2}) at different ambient temperatures (T_{amb}). Model prediction (solid lines) vs measured data (dotted lines). Note: y-axes not equally scaled.

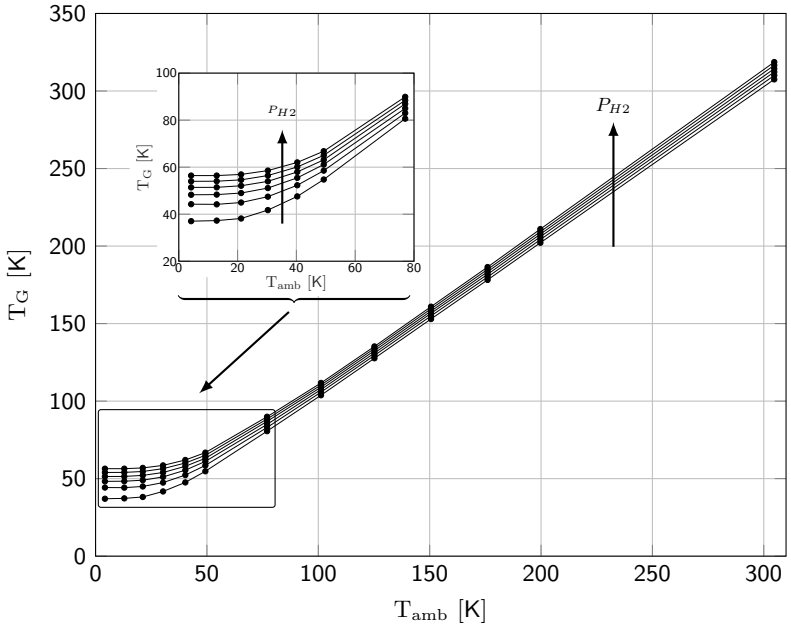

Figure 15: Gate temperature (T_G) as a function of ambient temperature (T_{amb}) for different H2 power levels: $P_{H2} = \{1, 2, ..., 6\}$ mW. These data are interpolations based on data shown in Fig. 6. A zoomed-in plot of the saturation region is shown in the inset.

However, the increase in circuit temperature by tens of degree Kelvin above T_{amb} can significantly degrade the noise performance for a thermal-noise-limited circuit, although it is still unclear whether temperature-independent shot-noise may be the main limitation in transistor's noise performance at deep-cryogenic temperatures [37]. Moreover, since the exact position of the thermal-resistance minimum cannot be fully attributed to the thermal properties of silicon, but heavily depends on the die thermalization, such as the package, the T_{chan} may vary due different positions on the die or boundary conditions of the die with the surrounding enclosure. Devices at tens of µm distance from each other can still experience significant thermal cross-talk at deep-cryogenic temperatures even at moderate power levels ($P > 4$ mW) within at least a radius of 30 µm (see Fig. 11 and 12). This directly translates into layout guidelines to properly space power-hungry devices from noise-sensitive circuits and precision circuits for which matching is a major consideration.

4.5 Conclusions

A 40-nm CMOS test structure was fabricated and characterized for a comprehensive evaluation of self-heating in bulk CMOS technology in the ambient temperature range from 300 K down to 4.2 K. The temperature rise was measured both in the MOSFET channel through the change in the gate resistance, and in the surrounding silicon substrate by a linear array of diodes operating as sensors.
Severe self-heating was observed at deep-cryogenic ambient temperatures, resulting in a channel temperature rise exceeding 40 K for a dissipated power of only 2 mW at a 4.2 K ambient temperature. Although the thermal conductivity of silicon is relatively low at very low temperatures, the absolute channel temperature does not exceed 60 K even for significantly higher power, due to the thermal resistance for a typical MOSFET, which has minimum above 70 K. This effect was confirmed by extracting the device thermal resistance from measured data at different temperatures and modeling it with a simple analytical expression able to predict channel temperatures over the full ambient temperature range from deep-cryogenic to room temperature.
The spatial propagation of SH results in a rise in substrate temperature detectable and quantifiable at a distance of 30 µm from the heater.
The thorough characterization of nanometer bulk-CMOS devices at cryogenic temperatures is of paramount importance for the design of the integrated control electronics for quantum processors. For achieving first-time-right silicon, it is imperative to simulate the circuit at the actual operating temperature rather than assume the ambient temperature. Towards that goal, the results and modeling presented in this chapter will contribute towards the full self-heating-aware IC design-flow required for the reliable design and operation of cryo-CMOS circuits.

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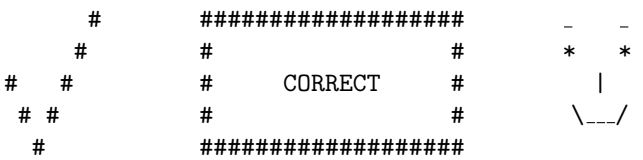
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Chapter 5

Conclusion

5.1 Research Overview and Contributions

Quantum computers promise a solution to certain problems intractable by classical computers. By doing so, quantum computation has the potential to induce a revolution that, without a doubt, will significantly change the world we live in. However, the actual implementation of such a device is still in its infancy, as state-of-the-art setups only comprise a few qubits, while thousands to even millions are required to tackle any useful problem.

The number of qubits is currently limited due to many difficulties of which the interconnect bottleneck is one. For correct operation, the qubits typically need to be cooled down to deep-cryogenic temperatures in the order of 10 mK to 100 mK in dilution refrigerators, which can accommodate only a finite number of physical interconnects from the qubits on the inside to the control electronics located on the outside of the refrigerator.

A possible solution that relaxes this constraint is the integration of the electronics currently located at room temperature, into a qubit controller chip operating at deep-cryogenic temperatures placed in close vicinity of the qubits itself. This would enable a scalable quantum computer, capable of executing actual quantum algorithms.

Apart from constraints, such as speed and power dissipation, one of the most important demands for the electronics in this application is its ability to be fully operational at a temperature of 4.2 K. Electronics operated at deep-cryogenic temperatures are nothing new. In fields like experimental particle physics, space exploration and observation, examples of such electronics exist. However, to meet the specifications required for qubit control, modern technology nodes such as 40-nm CMOS are required, for which not much cryogenic research has been carried-out.

Circuit designers that target cryogenic environments, require compact models enabling them to accurately simulate the functionality and behaviour of circuits at

cryogenic temperatures, to ensure reliable and optimal operation at these extreme conditions. The work contained in this thesis is centered around this goal: collect data and model the behaviour of devices operated at cryogenic temperatures through extensive characterization.
In this work, over 6000 devices were characterized in the temperature range between 300 K and 4.2 K, resulting in the following main contributions:

- It was shown that an Artificial-Neural-Network-based model flow is able to accurately generate cryogenic DC device models from measured data.
- Drain-current mismatch was characterized and modeled in the temperature range from 300 K down to 4.2 K in all bias regimes from subthreshold to strong-inversion.
- The temperature rise of both the channel and the surrounding silicon substrate of a MOSFET due to self-heating was characterized, and the former was modeled in the temperature range from 300 K down to 4.2 K.

By measuring I_D-V_D and I_D-V_G relationships of devices over different ambient temperatures, many parameters of interest were shown to change with decreasing temperatures. For example, comparing data measured at room temperature with those measured at 4.2 K the following was found: threshold voltage increased by approximately 100 mV, mobility increased by a factor of 2 and the subthreshold swing decreased to a value close to 20 mV/dec, depending on geometry.
From characterization of an array comprising devices with 400 distinct geometries over the temperature range between room temperature and 4.2 K, a large dataset was collected and fed into an ANN developed by Keysight Laboratories. It was shown that this modeling flow is able to automatically and successfully compile a DC model, with even sparse datasets (i.e. not regularly sampled in W, L, V_{GS}, V_{DS} and/or T). This modeling flow has the potential to accelerate development of cryogenic models and thus the design of cryogenic electronics for qubit interfacing.
Looking beyond single devices and more towards actual circuits, other additional DC effects become important. One of the effects that was extensively investigated in this work was drain-current mismatch in device pairs. It was found that the Pelgrom scaling rules for the threshold voltage, current factor and subthreshold slope remain valid down to 4.2 K. In the moderate to strong-inversion region an increase of drain-current mismatch was found with decreasing temperature. This increase was attributed to an increased current-factor variability (by 75 %) while the threshold-voltage variability remained substantially unaffected by temperature. The Croon model was successfully employed to predict drain-current mismatch for different device geometries over the full cryogenic ambient temperature range.
Since the power efficiency of qubit interfacing circuitry is paramount, an additional matching study was performed specifically aimed at subthreshold device operation. Cryogenic drain-current matching was found to deteriorate by several orders of

magnitude in this regime, mainly due to the large increase of subthreshold-slope variability at low temperatures. The subthreshold drain-current mismatch was successfully predicted by a specific subthreshold model. These two models combined, allow circuit designers to choose device operating regions and sizes to match the specification, without compromising area or speed.
All the models mentioned above have the device temperature as primary input. Especially for devices that dissipate significant power, the assumption that the device temperature is equal to the ambient temperature becomes invalidated due to self-heating. It is therefore important to accurately characterize and model self-heating, and use it as input to the DC and mismatch models to improve their accuracy.
Characterization of dedicated test structures uncovered severe self-heating at deep-cryogenic temperatures. A channel temperature rise of 40 K already at power levels of 2 mW was measured at 4.2 K. At higher dissipated powers, an absolute channel temperature not exceeding 60 K was found, due to the temperature dependence of the thermal resistance, which has minimum above 70 K. The channel temperature as a function of ambient temperature and dissipated power was successfully modeled with the use of the extracted device thermal resistance, able to accurately predict the channel temperature over the full ambient temperature range, from deep cryogenic to room temperature.
The effect of the heater was detectable and quantifiable at distances up to 30 µm from the heater.

5.2 Future Work

The work presented in this thesis was carried out while cryo-CMOS circuits were being taped-out in parallel. Direct applicability to circuit design was thus urgent, and the main target of the research. This work is therefore by no means complete and many aspects are left to be investigated. Some ideas for future research are summarized below:

- The work presented in this thesis mainly revolves around device characterization, and less around the physical modeling of cryogenic effects. The availability of cryogenic device mismatch and self-heating models is already very useful for circuit designers for the purpose of validation, however, an understanding of the physical mechanisms behind these effects can lead to more elaborate design rules. These rules enable designers of cryogenic precision circuits to circumvent problems associated with these cryogenic effects in an early design phase.

- This thesis focused on device characterization at temperatures down to 4.2 K, while current qubits operate at much lower temperatures, in the order of tens to hundreds of milli-Kelvins. Although it is expected that the control

electronics will not operate at these extreme low temperatures due to the severely limited power budget at the milli-Kelvin stage of a dilution refrigerator, characterization of device mismatch and variability at these extremes could still gain new and valuable data. Continuing on the remarks made in the previous point, these data could shine more light on the physical causes of increased cryogenic device variability.

- Related to the previous point, strong magnetic fields are often present in the vicinity of qubits to ensure their proper operation. Electrical transport properties are known to be altered by these fields through, for example, the Hall-effect. Therefore, not only the temperature, but also the effect of orientation and magnitude of these magnetic fields on MOSFETs and other components could be investigated.

- It is known that device self-heating is highly dependent on device geometry. The self-heating research presented in this thesis regards only a single device geometry. Repeating the same experiments on devices with different W and L could give additional insight into device geometries that are less susceptible to this effect, enabling circuit designers to make better informed choices to mitigate self-heating already during the circuit design.

- Employing ANNs for the "automatic" generation of cryogenic models is a very attractive scheme. In particular the ability of these networks to cope with sparse data (sampled without any gridding constraints over T, W/L and bias) has the potential to save a lot of valuable measurement time, as cryogenic characterization on average is more time consuming compared to those in the military temperature range. The data collected in this work has a fine gridding in all the previously mentioned parameters which was subsequently used for the ANN training. However, it remains unknown how much of this data was redundant for the purpose of modeling, in other words: how much data is actually required for successful model extraction using ANNs? Answering this question could significantly speed up the time required to characterize and model a technology at cryogenic temperatures.

In conclusion, it can be stated that cryogenic models are an absolute requirement when a cryogenically operated technology is pushed to its limits. This work is only a small step into that direction, and many, many, hours will need to be spend in the lab, evaporating the limited supply of helium for a machine that either solves or creates mankind's biggest problems.

Publications

Journals

P. A. 't Hart, M. Babaie, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and Modeling of Mismatch in Cryo-CMOS," *IEEE Journal of the Electron Devices Society (JEDS)*, vol. 8, pp. 263–273, 2020.

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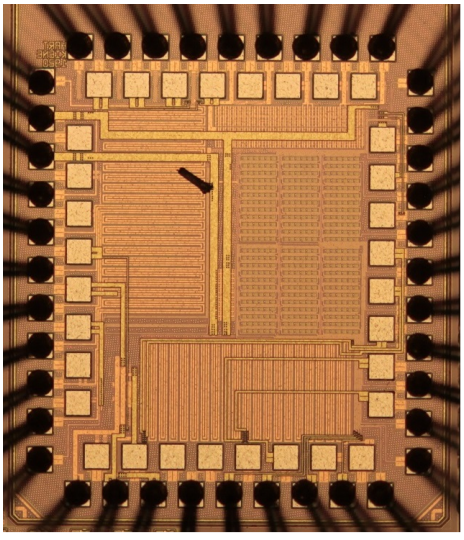

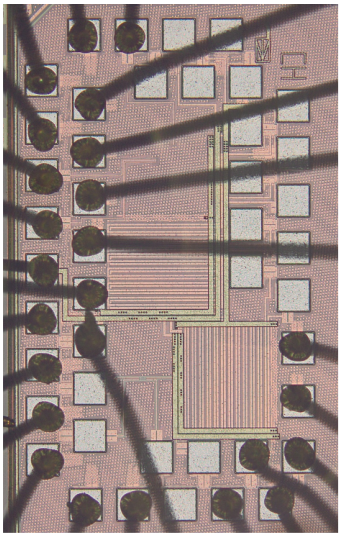

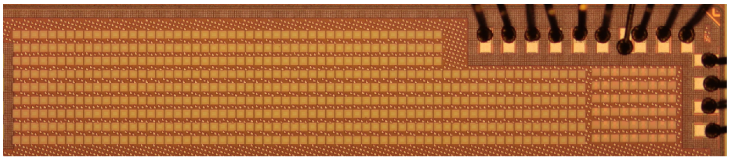

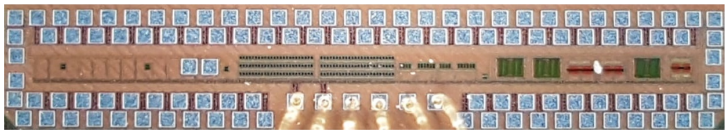

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Summary

Quantum computation has the potential to solve a certain class of problems intractable by today's classical computers, by virtue of the exponential speed-up it offers compared to its classical counterpart. Some examples of the problems this new computing paradigm promises to solve are simulation of complex molecules, enabling the manufacture of new materials and breaking specific encryption algorithms. The quantum computer attains its enormous computing power by employing quantum bits (qubits) instead of classical bits. In addition to the binary state of the classical bit (i.e. '1' and '0'), the qubit, which is based on quantum effects, can assume any linear combination of these states, and can therefore exploit quantum phenomena such as entanglement and superposition.

These quantum effects are very delicate and only emerge at deep-cryogenic temperatures, typically between 10 mK and 100 mK, at which thermal noise is low enough for the effects not to be scrambled. Qubits therefore 'live' in dilution refrigerators that can attain such extreme low temperatures.

To excecute quantum algorithms, the qubits need to be controlled: the initial state must be set and the result of the calculation needs to be read-out. Currently, this control is realized by rack-mounted classical electronics operated at room temperature, that connect to the qubits by long cables in the dilution refrigerator. While this approach works in an academic setting with only a few qubits, severe problems will be encountered when the number of qubits are scaled up to the millions necessary for executing any useful quantum algorithm. Problems associated with cable reliability, heat load and physical size, make this approach impractical.

To tackle this problem, an integrated controller is proposed that harnesses all the functionality of the room temperature control electronics in a silicon die placed in close vicinity to the actual qubits, and hence itself needs to operate at deep cryogenic temperatures. CMOS is the technology of choice for this controller for its speed, energy efficiency and proven cryogenic operation.

Many device parameters are known to change significantly compared to their room temperature value when devices are operated in a cryogenic environment. For example, the threshold voltage increases, mobility improves and the subthreshold slope becomes steeper at deep-cryogenic temperatures. For the reliable design of cryogenic circuits (Cryo-CMOS), precise knowledge of these parameter shifts and

the ability to simulate circuits at cryogenic ambient temperatures during the circuit design phase is indispensable.
Therefore, this work focuses on the characterization of devices over the temperature range from room temperature down to liquid helium temperature (4.2 K). Dedicated test chips were designed to characterize behavioural changes exhibited by devices operated at extremely low temperatures. From these measurement data, models were compiled able to predict this cryogenic device behaviour. In addition to the DC modeling of I_D-V_G and I_D-V_D data, important secondary effects that impact precision-analog circuits such as device mismatch and self-heating were extensively characterized and modeled.
In the strong-inversion region, the main sources of device mismatch, threshold-voltage and current-factor variability, were shown to follow the Pelgrom rule down to a temperature of 4.2 K. The Croon model was successfully employed to predict drain-current mismatch in the temperature range between room temperature and 4.2 K.
Matching in the subthreshold region was found to deteriorate by several orders of magnitude due to increased subthreshold-swing variability at deep-cryogenic temperatures. Since the Croon model does not take this variability source into account, a specific subthreshold model was shown to be required and able to adequately model drain-current mismatch in this region at cryogenic temperatures.
Self-heating was found to be exacerbated at deep-cryogenic temperatures, raising the local chip temperature significantly, exceeding 40 K for a dissipated power of 2 mW at 4.2 K. This effect was successfully modeled using a simple analytical expression, by extraction of the device thermal resistance at different ambient temperatures. Moreover, the spatial propagation of self-heating was found to be detectable and quantifiable at a distance of 30 µm from the heat source.
It was shown that these two effects need to be taken into account when designing cryogenic circuits, as they can lead to large deterioration of performance at low temperatures.
The characterization and modeling contained in this thesis aids the design of cryogenic circuits that form the first steps towards a scalable and practical quantum computer, capable of executing actual quantum algorithms.

Samenvatting

Kwantumcomputers hebben de potentie om een bepaalde set problemen op te lossen, die te complex zijn voor hedendaagse klassieke computers, dankzij de exponentieel hogere snelheid die hij bezit in vergelijking met zijn klassieke tegenhanger. Problemen die dit nieuwe computerparadigma belooft op te lossen zijn bijvoorbeeld de simulatie van complexe moleculen, waardoor nieuwe materialen kunnen worden gemaakt, en het kraken van specifieke coderingsalgoritmen. De kwantumcomputer behaalt zijn enorme rekenkracht door gebruik te maken van kwantumbits (qubits) in plaats van klassieke bits. Naast de binaire toestand van de klassieke bit (d.w.z. '1' en '0'), kan de qubit, die op kwantumeffecten is gebaseerd, elke lineaire combinatie van deze toestanden aannemen en daarom fenomenen zoals verstrengeling en superpositie benutten.

Deze kwantumeffecten zijn zeer delicaat en worden alleen zichtbaar op diep-cryogene temperaturen, die meestal tussen 10 mK en 100 mK liggen, waarbij de thermische ruis laag genoeg is om de effecten niet te verstoren. Qubits 'leven' daarom in dilution refrigerators die zulke extreem lage temperaturen kunnen bereiken.

Om kwantumalgoritmen uit te kunnen voeren, moeten de qubits worden aangestuurd: het moet mogelijk zijn om de begintoestand in te stellen en het resultaat van de berekening moet kunnen worden uitgelezen. Momenteel wordt deze besturing gerealiseerd door klassieke elektronica die zich op kamertemperatuur bevindt te verbinden via lange kabels in de dilution refrigerator met de qubits. Hoewel deze benadering werkt in een academische setting met slechts een paar qubits, zullen er zich ernstige problemen voordoen wanneer het aantal qubits wordt opgeschaald naar de miljoenen die nodig zijn voor het uitvoeren van een nuttig kwantumalgoritme. Problemen die verband houden met betrouwbaarheid van kabels, warmtebelasting en fysieke afmetingen maken deze aanpak onpraktisch.

Om dit probleem op te lossen, is een geïntegreerde controller voorgesteld die alle functionaliteit van de elektronica die zich nu op kamertemperatuur bevindt, te combineren in een chip die fysiek bij de qubits wordt geplaatst, en dus op diep cryogene temperaturen moet kunnen werken. CMOS is de technologie bij uitstek voor deze controller vanwege zijn snelheid, energie-efficiëntie en bewezen cryogene werking.

Van veel component eigenschappen is bekend dat ze significant veranderen in cryo-

gene omgevingstemperaturen in vergelijking met hun normale waarde op kamertemperatuur. Zo neemt de drempelspanning toe, verbetert de mobiliteit en wordt de subdrempel helling steiler bij diep cryogene temperaturen. Voor het betrouwbaar ontwerpen van cryogene schakelingen (Cryo-CMOS) is nauwkeurige kennis van deze verandering in eigenschappen en de mogelijkheid om deze bij cryogene omgevingstemperaturen te simuleren, tijdens de ontwerpfase, onontbeerlijk.
Daarom richt dit werk zich op de karakterisering van componenten op temperaturen van kamertemperatuur tot dat van vloeibaar helium (4.2 K). Speciale testchips zijn ontworpen om veranderingen in eigenschappen te karakteriseren die worden vertoond bij extreem lage temperaturen. Met behulp van deze meetgegevens zijn modellen geconstrueerd die dit cryogene gedrag kunnen voorspellen. Naast de DC-modellering van I_D-V_G en I_D-V_D data, werden belangrijke secundaire effecten die van invloed zijn op analoge precisieschakelingen, zoals componentmismatch en zelfverwarming, uitgebreid gekarakteriseerd en gemodelleerd.
In het sterke inversie gebied is aangetoond dat de hoofdoorzaken van mismatch, de variabiliteit van de drempelspanning en stroom factor, zich volgens de Pelgrom regel gedragen tot een temperatuur van 4.2 K. Het Croon model is gebruikt om de drainstroommismatch tussen kamertemperatuur en 4.2 K correct te voorspellen.
Matching in het subdrempel gebied bleek te verslechteren met tientallen malen als gevolg van verhoogde subdrempel helling variabiliteit bij diep cryogene temperature. Aangezien het Croon model geen rekening houdt met deze bron van variabiliteit, bleek het nodig te zijn om een specifiek subdrempelmodel te gebruiken om adequaat drainstroommismatch te modelleren in deze regio bij cryogene temperaturen.
Zelfverwarming bleek te verergeren bij diep cryogene temperaturen. De lokale chiptemperatuur werd met meer dan 40 K verhoogd voor een gedissipeerd vermogen van 2 mW bij een omgevingstemperatuur van 4.2 K. Dit effect werd met succes gemodelleerd met een eenvoudige analytische expressie, door extractie van de thermische weerstand van het component bij verschillende omgevingstemperaturen. Bovendien bleek de propagatie van zelfverwarming detecteerbaar en meetbaar op een afstand van 30 µm van de warmtebron.
Met de laatste twee effecten moet rekening worden gehouden bij het ontwerpen van cryogene schakelingen, aangezien deze kunnen leiden tot een grote verslechtering van de prestaties bij cryogene temperaturen.
De karakterisering en modellering in dit proefschrift dragen bij aan het ontwerp van cryogene schakelingen die de eerste stappen vormen naar een schaalbare en praktische kwantumcomputer, die in staat is om daadwerkelijke nuttige kwantumalgoritmen uit te voeren.

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After completing my Master's program, I was absolutely certain that I would never stay for a PhD. Well... It took me 2.5 years, 2 South-Africans and many, many, ASMs to realize that a PhD might not be so bad after all.
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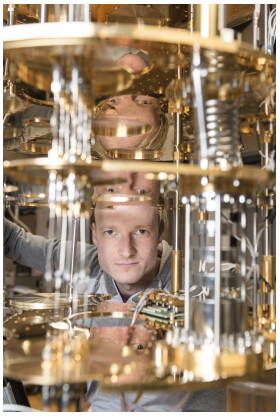
About the Author



P.A. 't Hart was born in Gouda, The Netherlands. He obtained both his BSc and MSc degree in microelectronics at TU Delft. For his master's thesis project he characterized the piezo-junction effect in bipolar transistors with both the Electronic Components, Materials and Technology department (ECTM) and the Electronic Instrumentation Laboratory. The project was in collaboration with Cypress Semiconductor, where he did an internship at their Lynnwood facility taping out and characterizing dedicated test structures for IC packaging research. He received the MSc in Electrical Engineering from the TU Delft in 2014.

In 2017 he joined the group of Edoardo Charbon and Fabio Sebastiano as a PhD candidate, characterizing and modeling MOSFETs operated at cryogenic temperatures. The core of the work done lies with device mismatch and variability. During these initial measurements, the test setups and knowledge applied in the other topics, such as DC-characterization and self-heating, were developed. This thesis is the result of all these efforts combined.
Besides his academic activities, he has many years of experience in flight simulation, interfacing and repairing instruments and other avionics. His interests lie especially in reverse engineering of mil-spec electronics, electronics design in general, rowing and home improvement.

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