Design and Simulation of a Superconducting Qubit

Master's Thesis

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Design and Simulation of a Superconducting Qubit

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Abstract

Quantum bits (qubits) are regarded as the building blocks of a quantum computer, which have significant implications in quantum information science. The superconducting qubit is a solid platform for quantum computing, where the Transmon qubit based on the Josephson junction or the SQUID structure is widely designed and researched. Microwave design and electromagnetic simulation of a superconducting qubit is a crucial way to determine and enhance the qubit performance in reality. The geometry of a superconducting qubit structure should be optimized to achieve the desired equivalent capacitance and consequently the resonant frequency through the external magnetic flux adjustment. In this thesis, a special superconducting qubit for lower energy loss named 'Pokemon' qubit is analyzed, with the role of different capacitance geometry in the qubit studied. This thesis also presented a comparative analysis between the in-plane capacitive structure and the flip-chip capacitance. The results pave the way for future modular quantum processing units utilizing flip-chip technology.

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Chapter 1

Introduction

1.1 Background

Quantum computing is a cutting-edge and rapidly evolving technology that leverages the principles of quantum mechanics to solve complex problems more efficiently than classical computing [2]. Compared with classical computers that may face limitations when processing large-scale data, quantum computers utilize quantum bits (qubits) existing in superposition and entanglement states to process certain types of computations much faster [3], which makes the technology increasingly attractive to global scientists and engineers.

The core of quantum computing is the qubit, which can exist in a superposition state of 0 and 1 and form strong correlations with other qubits through quantum entanglement. Among various qubit implementation schemes, superconducting qubits as artificial atoms are one of the most commonly used qubits due to their good controllability and scalability [4–6]. They have advanced significantly in gate functionality during the last ten years, making them a viable option for creating quantum computers [7]. These qubits are based on superconducting circuits and utilize the nonlinear effects of Josephson junctions (JJ) to construct circuit elements capable of representing quantum states. Transmon qubits are unique superconducting qubits with extensive application [4], which has a Superconducting Quantum Interference Device (SQUID) structure inside the qubit, controlled by external magnetic field [8]. The Starmon and the Pokemon qubits are types of Transmon qubits designed at QuTech for surface code. These qubits are design to allow high speed gate connection to its four nearest neighbors.

The manufacturing process of superconducting qubits is compatible with traditional microelectronic technology, which allows large-scale integration on chips using standard lithographic techniques [9], thereby promoting the scalability of quantum computers. With advancements in fabrication, superconducting qubit performance and controllability have improved significantly (particularly with the efforts

of companies like Google and IBM)[10], making quantum computers more stable and running quantum algorithms more effectively.

However, superconducting quantum bits still face numerous technical challenges. For example, the coherence time of superconducting quantum bits is relatively shorter than qubits in natural atoms [11], which means that the superconducting qubits are more sensitive to energy loss, noise, and environmental interference. Moreover, matching the frequency of quantum bits with that of the drive signal is also an issue. Specifically, the resonance frequency is crucial for quantum bit state control, which directly affects the operational precision, speed, and accuracy of quantum computing. Therefore, how to design and determine the resonant frequency of quantum bit circuits and improve the qubit lifetime should be considered.

1.2 Motivation

As mentioned in the earlier section, the performance of quantum bits largely depends on the qubit resonant frequency. When the resonant frequency of quantum bits precisely matches the drive signal frequency, the rapid and accurate state transitions, as well as the quantum computing efficiency can be ensured. Specifically, in quantum computing, it is typically necessary to apply microwave pulses or other types of electromagnetic signals to control the state of quantum bits [11] (e.g., exciting quantum bits from the ground state to the excited state), and for each quantum bit, it has a 'natural frequency,' also known as the resonant frequency, which determines how the qubit responds to external drive signals. For example, if a microwave pulse with a frequency of f_0 is applied, and the qubit's resonance frequency is also f_0, the pulse's energy will be maximally transferred to the quantum bit, causing the quantum bit's state to change precisely and efficiently. This means quantum operations can be completed in a short time with fewer errors through the computational process.

Similar to an LC resonant circuit, the resonant frequency of a superconducting qubit is controlled by adjusting the values of the equivalent capacitance and inductance in the circuit. For a Transmon qubit, its simplest equivalent circuit can be modeled as an equivalent capacitor and a nonlinear inductor in parallel, where the nonlinear inductance originates from the SQUID structure in the Transmon qubit controlled by an external magnetic field, and the equivalent capacitance depends on the design and structure of the qubit circuit [4]. Therefore, it is essential to determine the equivalent capacitance of a superconducting qubit to adjust the resonant frequency. Only with a known capacitance value of a qubit circuit with a specific structure, the desired resonant frequency can be obtained by adjusting the nonlinear inductance, thereby controlling the operational state of the quantum bit.

On the other hand, energy loss in superconducting qubits is a significant issue

in quantum computing. Energy loss typically manifests as a reduction in the coherence time of the quantum bit [12], leading to information loss and error accumulation during quantum computing. Therefore, designing a quantum bit with lower energy loss is crucial for improving its performance (longer coherence time), enabling reliable quantum computing over extended periods, and advancing quantum computing from theory to practical application.

Above all, the motivation of this thesis is to analyze and simulate a higher-performance (lower-loss) superconducting qubit and explore how the equivalent capacitance varies with the geometric shape of the internal capacitance in the qubit and its effect on the resonant frequency using electromagnetic simulation software (CST Microwave Studio). Through this work, it is hoped to provide new insights for the development of superconducting qubits.

1.3 Thesis Contributions

Analysis of a new type of Transmon qubit: With the motivation illustrated above, this thesis investigates a new type of Transmon qubit circuit, named the 'Pokemon qubit', designed at QuTech to ensure that it retains the essential features of a Transmon qubit while addressing the critical issue of energy loss in superconducting qubits with smoother capacitor structures. The primary goal of the Pokemon qubit is to improve the coherence time and overall performance of the qubit by minimizing energy dissipation. This advancement makes the Pokemon qubit more suitable for practical use in quantum computing applications where long operational times are essential.

Theoretical derivation of the equivalent capacitance: With the design of the Pokemon qubit, the qubit circuit structure is analyzed and simplified. The key aspect of the circuit design is to determine the equivalent capacitance for the resonant frequency calculation. This thesis provides a detailed derivation of the equivalent capacitance expression, which is crucial for accurately calculating the resonant frequency and ensuring that the qubit is tuned to operate at its optimal frequency, thus improving quantum computing performance.

Electromagnetic (EM) simulation analysis: To validate the theoretical design, this thesis utilizes CST Microwave Studio, a powerful electromagnetic simulation tool, to model the qubit's behavior and simulate its performance under various configurations. This tool allows for precise visualization of how changes in the physical shape and size of the components within the qubit circuit affect its equivalent capacitance and, consequently, its resonant frequency. The simulations provide valuable insights into the impact of the qubit's geometric structure on its performance, offering guidance for further optimization.

By combining theoretical analysis and electromagnetic simulations, this thesis

aims to demonstrate how the Pokemon qubit can achieve lower energy loss and how its equivalent capacitance is affected by the inner superconductor geometries. These insights are intended to contribute to the ongoing development of superconducting qubits.

1.4 Thesis Outline

This thesis focuses on the microwave analysis and simulation of the Pokemon qubit, with its context outlined in the following chapters. Chapter 2 introduces several related previous works in the field of superconducting qubits research. In Chapter 3, the concepts and the work principle of the superconducting qubits are introduced in detail, and the methodologies of this thesis are specifically introduced in Chapter 4, including the capacitor models, typical Transmon qubit models with the equivalent capacitance of the Pokemon qubit derived, and the simulation methods used for this thesis work. Chapter 5 then illustrates the detailed simulation of the capacitor models and the Pokemon qubit, and studies how the equivalent capacitance value changes with the geometries. Finally, Chapter 6 gives the conclusions of this thesis.

Chapter 2

Literature Review

Superconducting quantum bits, as the core components of quantum computing, have received extensive research and application in recent years, particularly in the optimization and performance enhancement of quantum hardware. Researchers have advanced quantum computing by continuously optimizing the design, control, and manufacturing technologies of superconducting quantum bits.

Research on superconducting qubits began in the 1990s and has evolved with the introduction of different types of qubit designs. Cooper pair box (CPB) quantum bits are one of the early implementations of superconducting quantum bits, typically used in conjunction with superconducting quantum interference devices (SQUIDs). Bouchiat and Vion first described the basic principles of CPB qubits and demonstrated how to implement qubits using Josephson junctions in superconducting circuits in 1998 [13]. The article demonstrated the quantum coherence of a single Cooper pair box and discussed its potential in quantum computing. Currently, the main types of superconducting qubits include Transmon qubits, Flux qubits, and Phase qubits. Among these, Transmon qubits have become one of the most widely used superconducting qubits due to their strong noise resistance and long coherence time. Koch and his colleagues proposed the Transmon qubit in 2007 and demonstrated its significant structural advantages over traditional superconducting qubits (like CPB) [4]. The design principle of Transmon involves balancing the parameters of capacitance and inductance to achieve the desired resonance frequency. The most distinctive feature of Transmon qubits is that improves coherence time and noise resistance by increasing capacitance and reducing the impact of charge noise on qubit performance, which lays the foundation for the development of superconducting qubits. Clarke and Wilhelm reviewed the basic principles of superconducting qubits and provides an overview of their development in 2008 [11]. It introduced the role of Josephson junctions, the working principle of SQUIDs (superconducting quantum interference devices) and their role in superconducting qubits, compared the principles of different types of superconducting qubit circuits (including flux qubits,

charge qubits, and phase qubits), and illustrated the coupling between qubits.

Coherence time is one of the most critical performance metrics in quantum computing [11]. As superconducting qubits began to evolve, Devoret and Schoelkopf noted that energy loss and environmental noise are the primary factors affecting the coherence time of superconducting qubits [12]. They analyzed the quantum dynamics and error rates in these systems and emphasized the importance of reducing energy loss in superconducting qubits, which is directly linked to decoherence, a major obstacle to maintaining the coherence of quantum states. In recent years, through material improvements and circuit design optimizations, the coherence time of superconducting qubits has seen significant improvements. Lupascu and his colleagues proposed methods to mitigate energy loss and enhance qubit performance by improving materials and designs [14], further contributing to the reliability of quantum computing. Despite these advancements, McRae et al. measured material losses in superconducting microwave resonators in 2020, identifying two-level systems (TLS) and non-equilibrium quasi-particles as the primary energy loss mechanisms, and proposed methods to improve material and interface processing [15]. Jayaraman investigated the loss and decoherence mechanisms in silicon-based superconducting circuits, and discussed the effect of material defects, surface spins, and TLS on the energy loss [16]. These researches contribute to long-term qubit operation.

In the study of superconducting qubits, how to precisely control the resonant frequency of the qubits is another important issue. A. Blais and his colleagues introduced the qubit manipulation using microwave pulses that is essential qubit state control [17]. The match conditions between the resonant frequency of the superconducting qubit and the drive signal frequency are important to the qubit performance. Precisely matched frequencies can lead to maximally transferred pulse energy and better computing efficiency. Wallraff et al. discussed methods for controlling and reading out superconducting qubits, they performed dispersion measurements of quantum bit states by non-resonantly coupling quantum bits to transmission line resonators and probing the transmission spectrum of the resonators and achieved relatively long coherence time [18].

Electromagnetic simulation technology is widely applied in the design and optimization of superconducting qubits. Amini and Mallahzadeh have proposed a new simulation model that enables traditional full-wave simulation software (such as HFSS and CST Microwave Studio) to accurately simulate the electromagnetic behavior of superconducting circuits. They replaced the superconducting film with an equivalent thin layer of appropriate impedance, which ensured to obtain the behavior of superconducting microwave components [19]. Saslow and Wong utilized HFSS to simulate a flip-chip-inspired structure, analyzed the key quantum metrics such as resonance modes, quality factors, and decoherence times, and explored the influence of the dielectric layer losses on quantum bit performance [20].

Recent studies have pushed the boundaries of quantum computing. The development of superconducting qubits has seen significant performance improvement, but key challenges like energy loss, coherence time, and frequency control still need to be advanced through circuit design. More research is needed to fully realize the potential of large-scale and efficient quantum computing.

Chapter 3

Superconducting Qubits

In this chapter, the theoretical concepts of the superconducting qubit are introduced. Generally speaking, a superconducting qubit is an artificial atom consisting of a nonlinear oscillator that mimics the non-equidistant energy levels in a natural atom. The following sections in this chapter introduce the superconducting qubit with the general mathematical expression of its state given, and compare energy levels between each state of a linear LC oscillator with those of the Josephson Junction, which is the basic component of quantum bits. A commonly used qubit, the Transmon Qubit, is introduced in the end of this chapter.

3.1 Quantum bits (Qubits)

Qubit, short for "quantum bit", is a basic unit of quantum information and computing. Unlike the classical bit in conventional computing which only exists in one of the two states (i.e., 0 or 1), a qubit can exist in a superposition of both states simultaneously. Quantum information is stored in the states. Mathematically, the general state $|\psi\rangle$ of a qubit can be expressed as a linear combination of two basis states [21]

$$|\psi\rangle = \alpha_0|0\rangle + \alpha_1|1\rangle \tag{3.1}$$

where the notation '$|\rangle$' is the 'Dirac' natation for quantum states, and α_0 and α_1 are two complex numbers satisfying $|\alpha_0|^2 + |\alpha_1|^2 = 1$, said to be the amplitudes, with $|\alpha_0|^2$ and $|\alpha_1|^2$ representing the probabilities of measuring the state $|0\rangle$ and state $|1\rangle$ respectively.

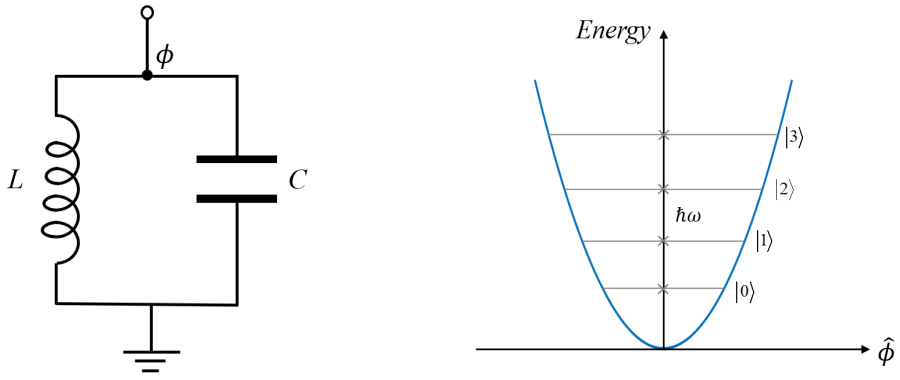
Another characteristic of the quantum bit is the entanglement. For multiple qubits, they can be entangled to each other regardless of their distance, which means that the state of a qubit may depend on another qubit's state.

3.2 Superconducting Qubits

A superconducting qubit is one of the most commonly used types of qubit artificially designed using circuits made from superconducting materials, whose electrical resistance can reach zero when operating at cryogenic temperature, allowing coherent quantum behaviors. Compared with natural atoms like trapped ions [22–25] and neutral atoms [26–29], whose states are represented by intrinsic energy levels or degrees of freedom (e.g., electron spin states) of the atoms, superconducting qubits introduce a nonlinear inductor to construct an artificial atom with non-equidistant energy levels similar to those of the natural atom. Although natural atoms have relatively longer coherence time than that of the superconducting qubits due to the weak interaction with the environment [27, 30], the interaction between qubits is slow, leading to hard controls [31]. In contrast, superconducting qubits are easier to integrate into a chip, allowing better scalability, tunability, and controllability [4–6, 32], which makes them possible to be engineered for desired characteristics and support quantum computing with promising platforms.

3.3 LC Oscillator

The main principle of a superconducting qubit is to utilize a two-level quantum system which can be realized by quantizing the circuit using the quantum mechanical features of superconducting circuits. A parallel LC oscillator consisting of a capacitor C in parallel with an inductor L is first considered (Fig.3.1a), where the oscillating angular frequency is $\omega = \frac{1}{\sqrt{LC}}$.



(a) LC oscillator diagram

(b) Energy potential for the circuit

Figure 3.1: LC Harmonic oscillator

The Lagrangian $\mathcal{L}$ of the LC circuit can be expressed through equation 3.2 [33–35]

$$\mathcal{L} = T - U = \frac{1}{2}C\dot{\Phi}^2 - \frac{1}{2L}\Phi^2, \tag{3.2}$$

where $T = \frac{1}{2}C\dot{\Phi}^2$ is the electrical (kinetic) energy of the capacitor, and $U = \frac{1}{2L}\Phi^2$ is the magnetic (potential) energy of the inductor. Φ and $\dot{\Phi}$ represent the node flux and its time derivative on the top node respectively.

The Hamiltonian $\mathcal{H}$ of the LC oscillator system can be derive through the Legendre transformation and the generalized momenta Q that represents the charge magnitude on the capacitor plates [36]

$$Q = \frac{\partial \mathcal{L}}{\partial \dot{\Phi}} = C\dot{\Phi}, \tag{3.3}$$

which leads to the Hamiltonian [3, 37]

$$\mathcal{H} = \frac{Q^2}{2C} + \frac{\Phi^2}{2L}. \tag{3.4}$$

The system can then be quantized by replacing Q by the quantum operator $\hat{Q}$, and Φ by $\hat{\Phi}$, which satisfy the commutation relation [36, 38]

$$[\hat{\Phi}, \hat{Q}] = i\hbar\mathbb{1}. \tag{3.5}$$

The annihilation operator $\hat{a}$ can be derived through the quantum operators $\hat{\Phi}$ and $\hat{Q}$:

$$\hat{a} = \frac{1}{\sqrt{2L\hbar\omega}}\hat{\Phi} + i\frac{1}{\sqrt{2C\hbar\omega}}\hat{Q}, \tag{3.6}$$

with $\omega = 1/\sqrt{LC}$ being the resonant frequency.
Based on the bosonic commutation relations that the annihilation $\hat{a}$ and creation $\hat{a}^\dagger$ satisfy [39]:

$$[\hat{a}, \hat{a}^\dagger] = \mathbb{1}, \tag{3.7}$$

the quantized flux $\hat{\phi}$ and charge $\hat{Q}$ can be expressed as: [33, 36, 40]

$$\hat{\Phi} = \sqrt{\frac{\hbar Z_0}{2}}(\hat{a}^\dagger + \hat{a}) = \Phi_{zpf}(\hat{a}^\dagger + \hat{a}), \tag{3.8}$$

$$\hat{Q} = i\sqrt{\frac{\hbar}{2Z_0}}(\hat{a}^\dagger - \hat{a}) = iQ_{zpf}(\hat{a}^\dagger - \hat{a}), \tag{3.9}$$

where $Z_0 = \sqrt{L/C}$ is the characteristic impedance of the oscillator, and the coefficients

$$\Phi_{zpf} = \sqrt{\frac{\hbar}{2C\omega}} = \sqrt{\frac{\hbar Z_0}{2}}, \quad Q_{zpf} = \sqrt{\frac{\hbar C\omega}{2}} = \sqrt{\frac{\hbar}{2Z_0}} \tag{3.10}$$

are the zero point fluctuations (zpf) of the flux and charge variable respectively.

Thus, the quantum Hamiltonian can be rewritten with the above definitions as:

$$H = \hbar\omega\left(\hat{a}^\dagger\hat{a} + \frac{1}{2}\right), \tag{3.11}$$

with the eigenstate satisfying $\hat{a}^\dagger\hat{a}|n\rangle = n|n\rangle$ ($n = 0, 1, 2...$ [39], the LC circuit thus produces discrete energy levels spaced equally by $\hbar\omega$, shown in Fig.3.1b. The problem of this LC circuit is the poor distinction of energy levels (the energy differences between each state are equal), which makes it impossible to generate and control reliable qubits.

3.4 Josephson Junction and Cooper Pair Box

As mentioned that, the distinguishable energy gaps between quantum states should be realized in a system to construct and control reliable qubits. The nonlinearity of a circuit element is consequently introduced to achieve the addressable two-level system. Compared with the harmonic oscillator which is composed of a linear inductor L and a capacitor C in parallel, the unharmonic oscillator can achieve nonlinearity by replacing the linear inductor L by an ideal nonlinear inductor, which is the Josephson Junction (JJ), first introduced by Brian Josephson in 1962 [41] and widely used for implementing different kinds of superconducting qubits, such as Transmon, flux, and phase qubits.

Figure 3.2 shows the structure of a Josephson junction, which is formed by two superconductors through a thin insulating layer with an appropriate thickness of typically 2-3 nm, allowing the Cooper-pair electrons to tunnel across the junction. The circuit symbol of JJ is also shown in Fig.3.2, which is composed by its own capacitance C_J and a junction in parallel only accounting for the Josephson potential. It can be seen that the parallel structure uses a junction to replace the linear inductor in the LC resonator (Fig.3.1a) to obtain a nonlinear system, which is the so-called Cooper pair box (CPB).

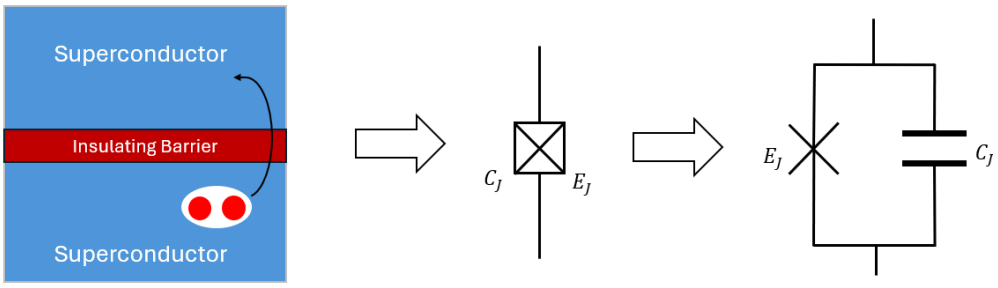


Figure 3.2: Structure and symbol of the Josephson Junction (Cooper pair box)

For Josephson Junction, there are 2 main equations illustrating its working principles. First, a supercurrent i_b is generated by the flow of the Cooper-pair electrons, expressed by the first Josephson relation [42]

$$i_b = I_c \sin\varphi, \tag{3.12}$$

where φ is the superconducting phase difference, and $I_c > 0$ is the critical (maximum) current that the junction can support [34].
The second Josephson relation reads the superconducting voltage v_b cross the junctions

$$v_b = \frac{\Phi_0}{2\pi}\frac{d\varphi}{dt}, \tag{3.13}$$

where $\Phi_0 = h/2e$ is the superconducting flux quantum. Thus, the phase difference φ can also be re-written through Equation 3.13 and the relationship $\dot{\Phi}_b = v_b$ as:

$$\varphi = \frac{2\pi}{\Phi_0}\Phi_b. \tag{3.14}$$

Through Equation 3.12 and 3.13, the relationship between v_b and i_b can then be derived:

$$\frac{di_b}{dt} = I_c\cos\varphi\cdot\frac{d\varphi}{dt} = I_c\cos\varphi\cdot\frac{2\pi v_b}{\Phi_0}, \tag{3.15}$$

i.e.,

$$v_b = \frac{\Phi_0}{2\pi I_c\cos\varphi}\frac{di_b}{dt} = L_J\frac{di_b}{dt}, \tag{3.16}$$

where L_J is the defined Josephson inductance which satisfies $v_b = L_J\frac{di_b}{dt}$. Thus, L_J can be illustrated in Equation 3.17, from which can be seen that the inductance is non-linear.

$$L_J = \frac{\Phi_0}{2\pi I_c\cos\varphi} \tag{3.17}$$

Using Equation 3.12 and 3.13, the energy stored in the Josephson junction is given by

$$\int_t v_b i_b \, dt = -\frac{\Phi_0 I_c}{2\pi} \cos\varphi = -E_J \cos\varphi = -E_J \cos\left(\frac{2\pi}{\Phi_0}\Phi_b\right), \tag{3.18}$$

with the Josephson energy

$$E_J = \frac{\Phi_0 I_c}{2\pi}. \tag{3.19}$$

From the circuit diagram of a Cooper pair box (unharmonic oscillator) shown in Figure 3.3a, where the shunting capacitance C_J in parallel represents the intrinsic capacitance of the Josephson Junction, the Lagrangian $\mathcal{L}$ of the CPB can then be expressed by Equation 3.20 with the top node flux defined as ϕ and the bottom node on the ground, similar to that illustrated in Section 3.3:

$$\mathcal{L} = \frac{1}{2} C_J \dot{\Phi}^2 + E_J \cos\varphi = \frac{1}{2} C_J \dot{\Phi}^2 + E_J \cos\left(\frac{2\pi}{\Phi_0}\Phi\right). \tag{3.20}$$

For a quantized system, the quantum Hamiltonian can be represented as [36]:

$$H = \frac{\hat{Q}^2}{2C_J} - E_J \cos\left(\frac{2\pi}{\Phi_0}\hat{\Phi}\right), \tag{3.21}$$

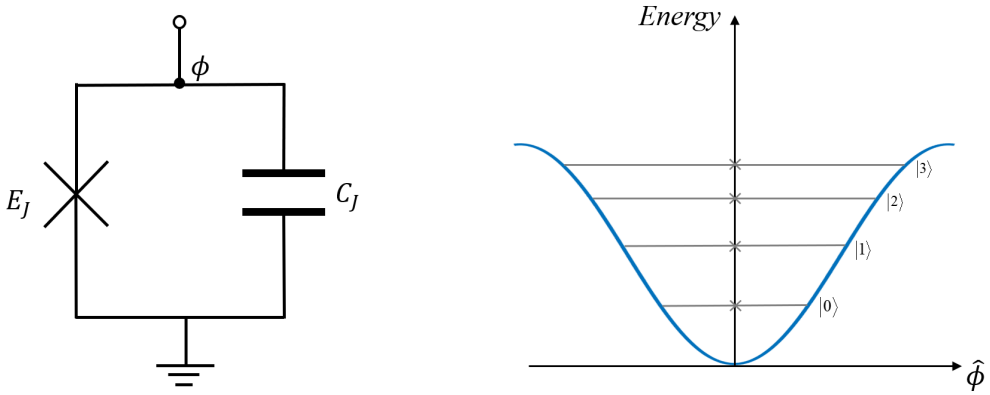
where $\hat{Q} = C\dot{\Phi}$ and $[\hat{\Phi}, \hat{Q}] = i\hbar\mathbb{1}$, same as that illustrated in Section 3.3.
By introducing dimensionless flux and charge variables ϕ and q where

$$\phi = \frac{2\pi\Phi}{\Phi_0}, \quad q = \frac{Q}{2e}, \tag{3.22}$$

with $\Phi_0 = \frac{h}{2e}$, the rescaled quantum operators $\hat{\phi}$ and $\hat{q}$ satisfying $[\hat{\phi}, \hat{q}] = i\mathbb{1}$ can be used to rewrite the Hamiltonian as [3, 36]:

$$H = 4E_C \hat{q}^2 - E_J \cos\hat{\phi}, \tag{3.23}$$

where $E_C = \frac{e^2}{2C_J}$ is the charging energy in the capacitor.



(a) Cooper pair box

(b) Energy potential for CPB

Figure 3.3: Unharmonic Oscillators

Figure 3.3b shows the energy levels of different eigenstates for a Cooper pair box. Compared with the harmonic oscillator using linear circuit elements (Fig.3.1b), whose energy level separations are known to be exactly equidistant, the unharmonic oscillator (CPB) with a nonlinear inductor (Josephson junction) leads to non-equidistantly spaced energy levels, shown as a 'cos()' function. It can be seen that the separation of the energy levels in nonlinear circuits becomes closer for higher excited states, which limits the system's dynamics to only two Qubit states, and thus ensures a stable and reliable two-level system.

Usually the capacitance C_J in a cooper pair box is small, thus the Hamiltonian is dominated mainly by the charging energy E_C, i.e., $E_J/E_C < 1$, which makes the CPB very sensitive to charge fluctuations, leading to bad stability.

3.5 Transmon Qubit

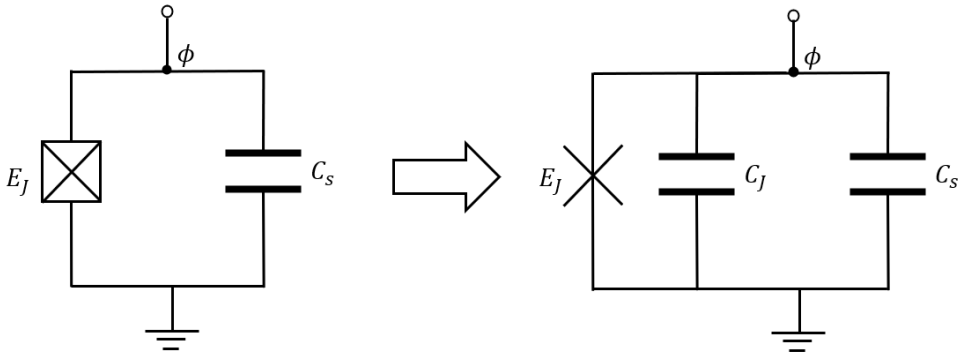


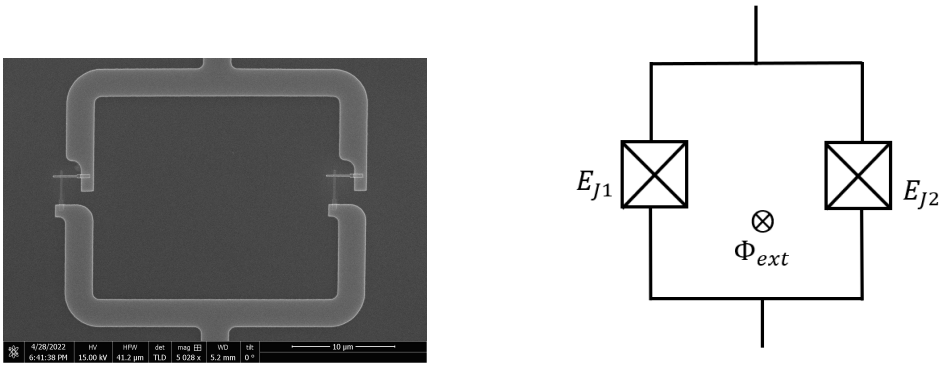
Figure 3.4: Structure of the Transmon qubit

To suppress the sensitivity to the charge fluctuations and the charge dispersion, the ratio E_J/E_C should be increased to $E_J/E_C >> 1$. One method is to shunt a necessary large capacitor $C_S >> C_J$ [4] to increase the total capacitance $C_\Sigma = C_J + C_S$ and thus decrease the charging energy $E_C = \frac{e^2}{2C_\Sigma}$, which is referred to as a Transmon qubit circuit, shown in Figure 3.4.

The quantum Hamiltonian expression is similar to that of the CPB, with C_J replaced by the total capacitance C_Σ, which also leads to non-equidistant energy levels as a 'cos()' function. Compared to the Cooper Pair Box, the Transmon qubit is less sensitive to the charge noise with better stability, however, it should be noted that the energy levels become more equidistant than the CPB without shunting capacitors, which may make the two-level system less stable and lead to leakage outside the preferred computational states, thus choosing a reasonable C_S value for a Transmon qubit should be considered.

3.6 DC SQUID and Tunable Transmon Qubit

To control the qubit frequency flexibly, a structure containing two parallel Josephson junctions in a loop with some flux threaded through the loop is used, which is the DC Superconducting Quantum Interference Device (SQUID), shown in Figure 3.5, where Φ_{ext} is the external magnetic flux into the loop.



(a) A SQUID device from Ref.[43] (b) SQUID electric circuit

Figure 3.5: SQUID structure

The Josephson energy of the DC SQUID can be expressed in Equation 3.24 [4],

$$E_J = E_{J\Sigma}\cos\left(\frac{\pi\Phi_{ext}}{\Phi_0}\right)\sqrt{1+d^2\tan^2\left(\frac{\pi\Phi_{ext}}{\Phi_0}\right)} \tag{3.24}$$

where $d = \frac{E_{J2}-E_{J1}}{E_{J2}+E_{J1}}$, and $E_{J\Sigma} = E_{J1} + E_{J2}$.

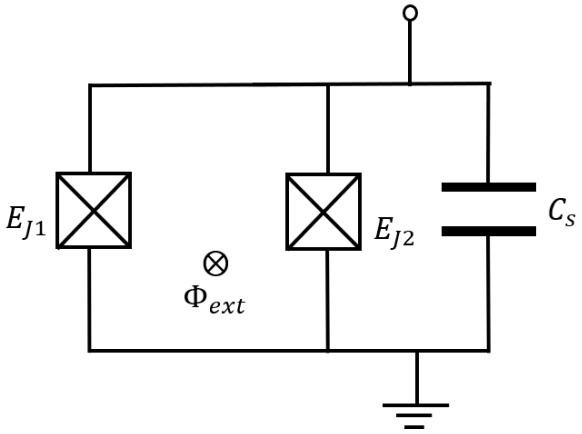


Figure 3.6: Circuit structure of a tunable Transmon qubit

Unlike the Transmon qubit consisting of a large capacitance shunting a single Josephson junction which cannot conveniently tune the qubit frequency, a tunable Transmon qubit shunting a SQUID instead of a single JJ can be used to control the qubit frequency by tuning the magnetic flux Φ_{ext} threaded through the SQUID loop, shown in Figure 3.6. To be more specific, the DC SQUID in the Transmon qubit can be regarded as a 'tunable' single Josephson junction whose effective inductance varies with the applied external flux Φ_{ext} as [34]

$$L_{\text{SQUID}}(\Phi_{ext}) = \frac{\Phi_0}{4\pi I_c \cos\left(\frac{\pi\Phi_{ext}}{\Phi_0}\right)}. \tag{3.25}$$

Although a single Josephson junction possesses a non-linear inductor as that illustrated in Equation 3.17, the phase φ is determined by the current and voltage in the junction, which makes it a dynamical variable of the quantum circuit. Therefore, the inductance of a single JJ is not a directly controllable parameter: varying it would require perturbing the quantum state of the system. In contrast, the external magnetic flux in Equation 3.25 is an experimentally tunable parameter, which can be adjusted continuously and reversibly without disturbing the quantum state of the qubit. Thus, by tuning the magnetic flux, the inductance of the SQUID structure can be adjusted, which consequently controls the qubit resonance frequency.

Chapter 4

Methodology

In this chapter, the methodology of this thesis is presented. Based on the Transmon qubits illustrated in Chapter 3, which are mainly composed by a capacitor and a non-linear inductor, this chapter first discusses and compared the capacitor models, including the flip-chip capacitor and the in-plane capacitor. Then, typical Transmon qubits like the Starmon qubit and the Pokemon qubit are introduced, with their circuit structures, main component functions, and characteristics compared. The circuit model of the Pokemon qubit investigated in this thesis is analyzed and simplified, and its equivalent capacitance is derived for resonant frequency calculations. Additionally, the simulation approach employed in this work is described, detailing the simulation settings, primary functions, and representative simulation results obtained using CST Microwave Studio.

4.1 Capacitor Models

Capacitance is the ability of an object to store the electric charge. It is measured by the change in charge in response to a difference in electric potential, expressed as the ratio of them, i.e.,

$$C = \frac{q}{V}, \tag{4.1}$$

where q is the charge held, and V is the electric potential.

Theoretically, the capacitance between two conductors depends on the geometry, the opposing surface area, the conductor distance, and the permittivity of the material, independent of the potential difference V between conductors and the total charge q on them.

4.1.1 Flip-Chip Capacitor Model

A flip-chip capacitor is consist with 2 conductor pads in parallel. Figure 4.1 shows a simple system consisting of two identical rectangular plates with their area A, placed in a medium with its permittivity ε, the capacitance can be theoretically calculated through Equation 4.2.

$$C = \varepsilon \frac{A}{d}, \tag{4.2}$$

where d is the distance between the two capacitors.

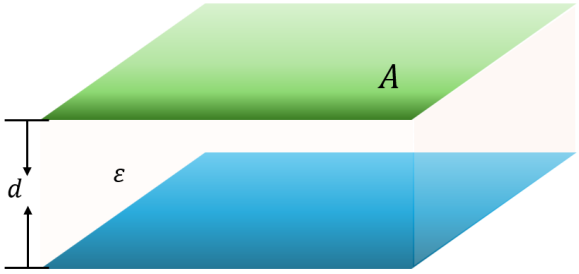


Figure 4.1: Flip-chip capacitor model

Typically, due to process limitations, the minimum spacing distance between the two conductor planes is about 1 micrometer.

4.1.2 In-plane Capacitor Model

Compared with the flip-chip capacitor where the conductors are in different planes, the in-plane capacitor consists of conductors with distance in the same plane. A simple in-plane conductor model (in-plane parallel plate capacitor) is shown in Figure 4.2, where two rectangular plates with distance d are placed in the same plane on a substrate.

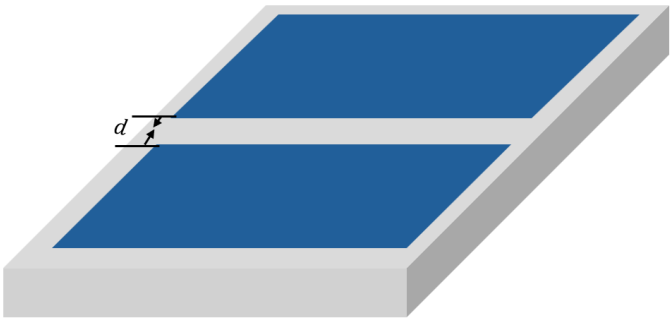


Figure 4.2: Parallel plate capacitor

Another common type of in-plane capacitor is the interdigitated capacitor, and it has a higher quality factor than the parallel plate capacitor with its structure shown in Figure 4.3. From the figure, it can be seen that the interdigitated capacitor is composed of two interleaved conductors with gap G in the same plane on a substrate, where each conductor consists several micro-strip lines (fingers) with finger length l and finger width w [44]. The spacing distances d between each two adjacent fingers are the same, with total n fingers. The capacitor dimension (maximum distance between the two conductors) is a. In this capacitor, it is assumed that only the coupling between adjacent fingers is considered and the number of fingers can be large [45–49].

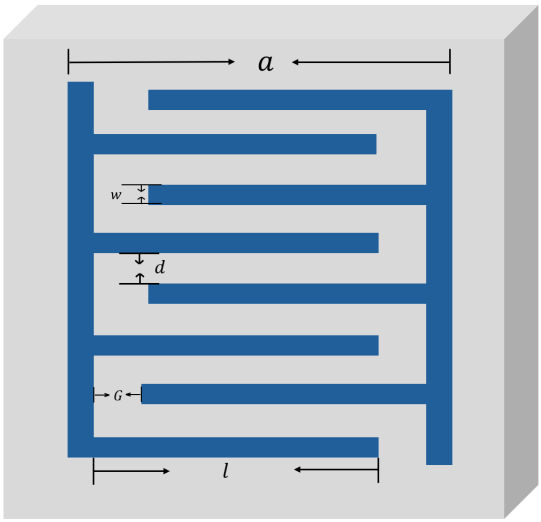


Figure 4.3: Interdigitated capacitor model

The total interdigitated capacitance can be expressed generally through the elliptic integrals (K) [50]:

$$C_{\mathrm{IDC}} = \varepsilon_0 \varepsilon_{\mathrm{r}} \frac{K(k_0')}{K(k_0)} (n-1) l \tag{4.3}$$

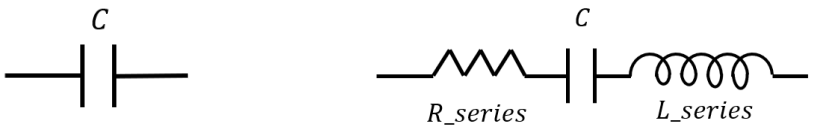
where ε_0 is the permittivity in the free space, ε_{r} is the permittivity of the dielectric layer, k_0 is the modulus of the elliptic integrals [51] defined by the finger width w and the space between the fingers d, and $k_0' = (1-k_0^2)^{1/2}$.

In [52], one expression of the IDC capacitance value was derived based on the parameters in Figure4.3:

$$C_{\mathrm{IDC}} = \varepsilon_0 \varepsilon_{\mathrm{r}} \frac{(2l - a + 2w) t_0}{d} (2n-1), \tag{4.4}$$

where t_0 is the thickness of the electrodes (the conductors).

It should be noticed that, in practical scenarios, especially at high frequencies, the geometric inductance of the IDC should be considered. It is crucial to consider the inductor connected in series with the capacitor. The equivalent models of a capacitor under low frequencies (ideal model) and high frequencies are shown in Figure 4.4. Another important issue should be considered is, the self-resonance of the capacitor should be avoid, the operating frequency range should be away from the resonant frequency caused by the capacitor and the geometric inductor. Therefore, although Equation 4.4 shows the capacitance value increases with the finger length, the geometric inductance is also proportional to the length, which is unwanted and should be avoided, making the design of the interdigitated capacitor complex.

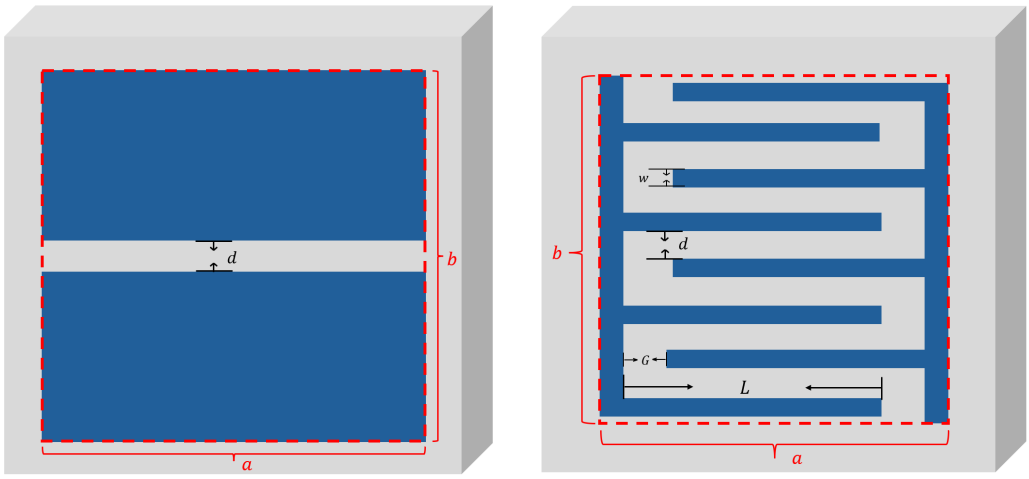


(a) Ideal capacitor

(b) Real capacitor at high frequencies

Figure 4.4: Sketch of the capacitor model

4.1.3 2D Footprint Area



(a) 2D footprint sketch for the in-plane parallel plate capacitor

(b) 2D footprint sketch for the interdigitated capacitor

Figure 4.5: 2D footprint sketch for in-plane capacitors

The 2D footprint area refers to the projected area that a circuit structure occupies when viewed from above on a flat, i.e., it represents the total surface area that the object (for example, a capacitor) covers on the substrate or any other surface. It is important for the chip design and packaging, which determines how much space a capacitor or a qubit will occupy on a wafer.

Thus, for the flip-chip capacitor, its 2D footprint area is equal to the area of one chip. For two rectangular pads in parallel shown in Figure 4.1, the 2D footprint area is the area of the rectangular plate (i.e., A). As for the in-plane capacitors (in-plane parallel plate capacitors, and interdigitated capacitors), the 2D footprint is outlined by the red dotted line, shown in Figure4.5, and the area can be expressed as the product of a and b, (i.e., $a * b$).

4.2 Typical Transmon Qubits

4.2.1 Starmon Qubit

Starmon qubit is a SQUID-based Transmon qubit based on circuit quantum electrodynamics, with its structure shown in Figure 4.6 [53]. From this figure, it can be seen that the Starmon qubit is a seven-port Transmon qubit, connecting to four bus resonators in the corners of the qubit, a microwave-drive line on the top, a readout resonator at the bottom, and a flux-bias line at right.

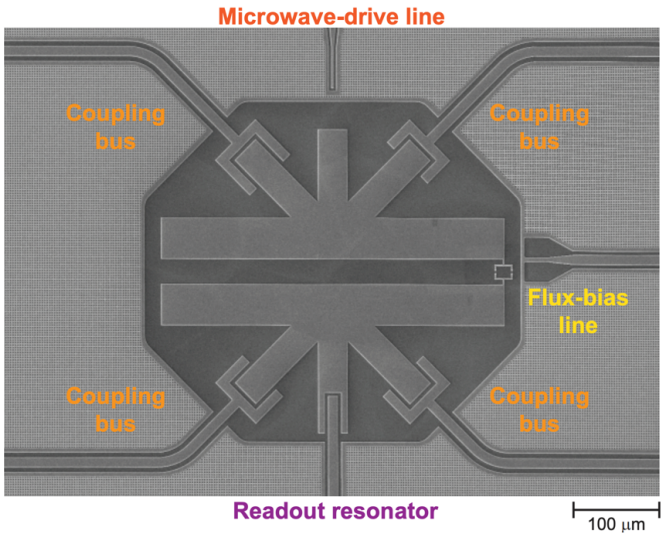


Figure 4.6: Starmon qubit circuit diagram. Adapted from[1].

4.2.2 Pokemon Qubit

It can be seen that the shape of a conductor or resonator in the Starmon qubit has sharp corners, which means that the electric field tends to concentrate more at those points, i.e., the field strength is higher near sharp points or edges. The bad effect of this shape is that it leads to increased dielectric losses at the interface layers between the superconductor and the silicon substrate and thus more energy dissipation, directly decreasing the qubit's coherence time which is critical for maintaining the qubit's quantum state.

To suppress this effect, a new Transmon qubit, named 'Pokemon Qubit' was designed and experimentally studies at QuTech in 2019. This qubit contains smoother corners, which reduce the energy loss around the corners and may have longer coherence time than Starmon qubits. This thesis work mainly focuses on the microwave analysis and simulation of the Pokemon Qubit.

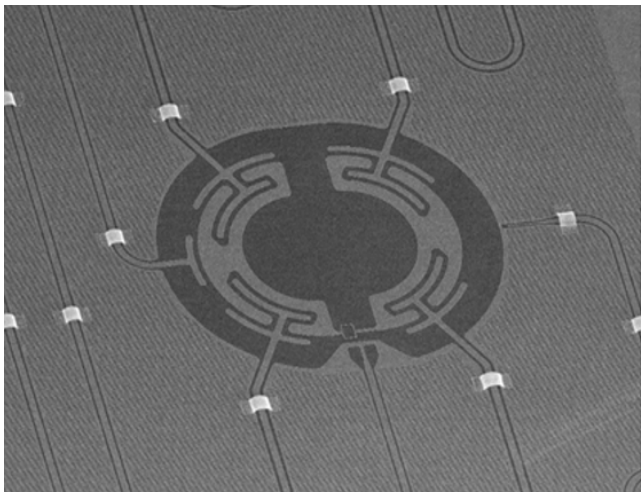
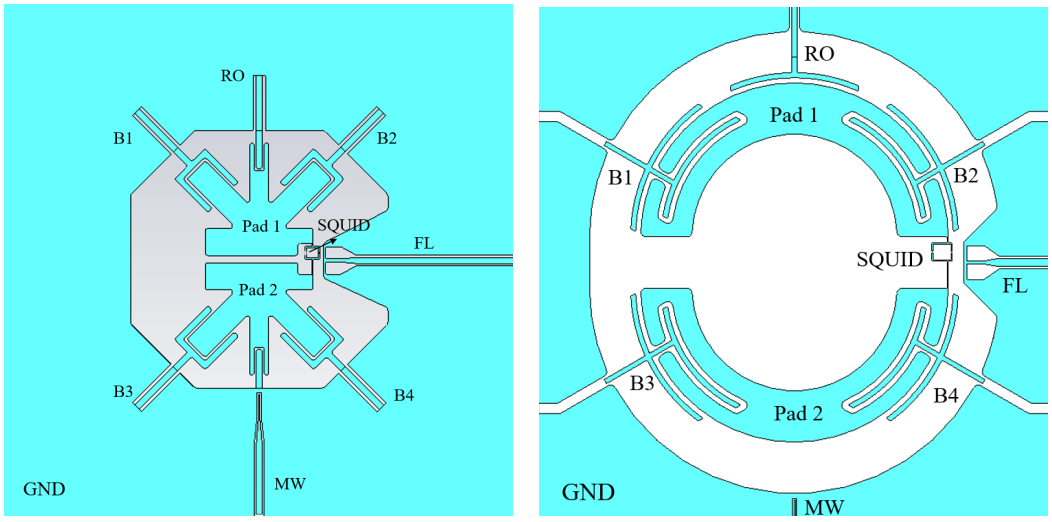


Figure 4.7: Fabricated Pokemon qubit model at QuTech

4.2.2.1 Pokemon Qubit Components and Functions

Figure 4.8a and 4.8b compared the qubit circuit structures of the Starmon qubit and the Pokemon qubit, from which can be seen that the main components of the Pokemon qubit are similar to those of the Starmon, i.e., the Pokemon qubit also has seven ports with similar functions to that in the Starmon qubit. It can be seen that both of them are surrounded by a ground plane (GND), consisting of 4 bus resonators ($B1 \sim B4$), a readout line (RO) on the top, a microwave drive line resonator (RO) at the structure bottom, a flux line (FL) at right, 2 in-plane pads (Pad 1, 2), and a superconducting quantum interference device (SQUID) structure. The lines are all coplanar waveguides. To be more specific, in Figure 4.8b, 4 buses are used to couple with other neighboring qubits, the microwave drive line is for controlling

the qubits state, and the flux line applies a magnetic field to the SQUID to tune the effective inductance, thus can change the qubit resonate frequency. As illustrated in the previous section, two in-plane metal plates separated by a distance form an in-plane capacitor, which means that the Pokemon qubit has a complex structure consisting of several series and parallel capacitors.



(a) Starmon Qubit (b) Pokemon Qubit

Figure 4.8: Typical Transmon Qubits

4.2.2.2 Pokemon Qubit Circuit Model

As illustrated in Subsection 4.2.2.1, the Pokemon circuit model is composed by several capacitors. Based on the structures, the circuit structure of the Pokemon qubit is modeled in Figure 4.9, where c_R is form by the readout line (RO) and Pad 1, c_{mw} is formed by the microwave drive line (MW) and Pad 2, c_{b1} and c_{b2} are formed by Pad 1 and the bus resonator on the structure top (B1 and B2), and c_{b3} and c_{b4} are formed by Pad 2 and the bus resonator B3 and B4 at the bottom. C_t is the capacitor generated by the two in-plane pads (Pad 1 and 2), and c_{g1} and c_{g2} are the capacitors formed by the superconducting Pad 1 (or 2) and the ground (GND). Also, there is a capacitor c_{gli} ($i = 1,2,3,4$) between the i-th bus resonator and the ground. Usually, these capacitors have much greater values than the capacitors formed by the buses and the pads, i.e., $c_{gli} \gg c_{bi}$ ($i = 1,2,3,4$).

In application, the resonant frequency is determined by the equivalent capacitor in parallel with the inductor of the SQUID structure tuned by the flux line, where the two end points of the parallel connection are point a and point b. Thus, the derivation of the equivalent capacitance between point a and b is essential for the subsequent determination of the qubit resonance frequency.

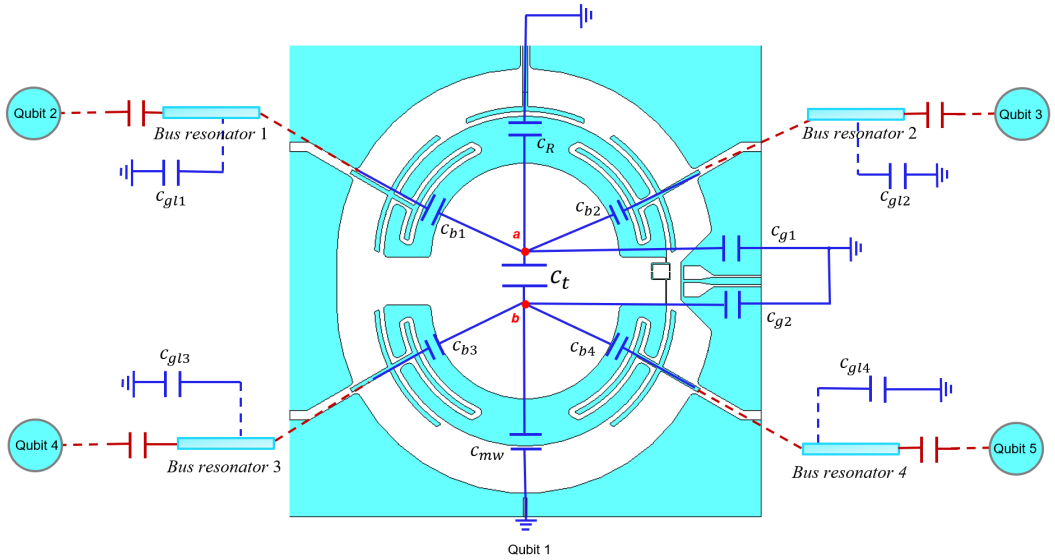


Figure 4.9: Pokemon Qubit Circuit Structure

To derive the equivalent capacitance between the two points, the relationship between c_{gli} and c_{bi} can be utilized to simplified the circuit model. Specifically, when two capacitors are in series, then the much smaller capacitance dominates. Take c_{gl1} and c_{b1} as an example, the total capacitance of the two in-series capacitors is:

$$c_{series} = \frac{c_{gl1} \cdot c_{b1}}{c_{gl1} + c_{b1}} \tag{4.5}$$

Divide both the numerator and denominator by c_{gl1}, then:

$$c_{series} = \frac{c_{b1}}{1 + \frac{c_{b1}}{c_{gl1}}}. \tag{4.6}$$

When $c_{gl1} \gg c_{b1}$, $\frac{c_{b1}}{c_{gl1}}$ is almost equal to zero, i.e., $\frac{c_{b1}}{c_{gl1}} \to 0$, which is negligible in Equation 4.6. Then, the total capacitance value of two capacitors in series with one of them much larger than the other can be simplified as:

$$c_{series} \approx \frac{c_{b1}}{1+0} \approx c_{b1} \tag{4.7}$$

Figure 4.10 shows the relationship between the total capacitor and the ratio of c_{gl1} to c_{b1}. It can be seen that, when $c_{gl1} \geq 300 c_{b1}$ (meaning that c_{gl1} is much larger than c_{b1}), the total capacitance value C_{total} is almost the same as that of the smaller one (c_{b1}), consist with the characteristic that illustrated above through the formula approximation and derivation.

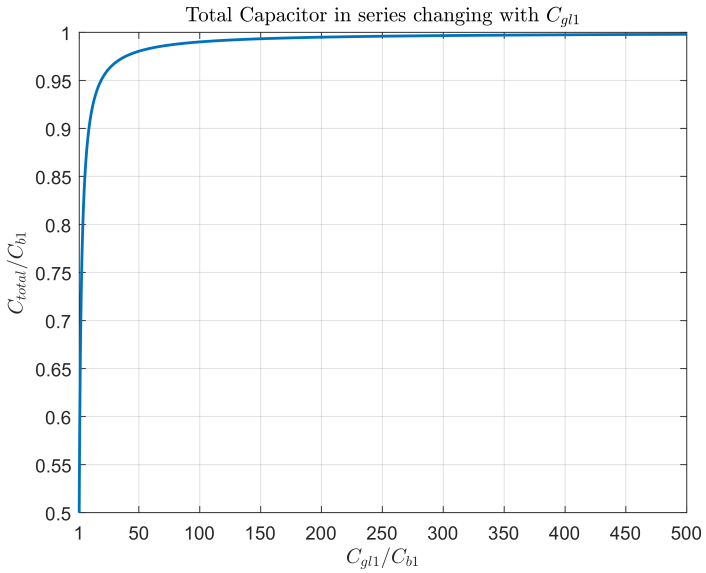


Figure 4.10: Capacitors in series

Based on this feature, the simplified circuit model is shown in Figure 4.11, where now c_{bi} $(i = 1,2,3,4)$ directly connects with the ground.

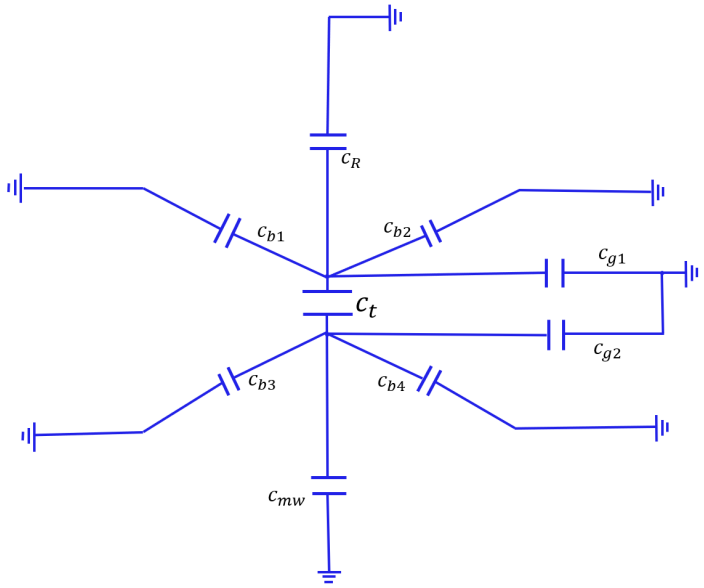


Figure 4.11: Simplified Pokemon Qubit Circuit Model

It can be seen that, c_{b1}, c_{b2}, and c_R are in parallel, between point a and GND. Similarly, c_{b3}, c_{b4}, and c_{mw} are also in parallel, between point b and GND. Using

the equation for calculating total capacitance with n capacitors in parallel,

$$C_{parallel} = \sum_{i=1}^{n} C_{pi} \quad (i = 1, 2, ...n), \tag{4.8}$$

where C_{pi} is the i-th capacitor in parallel. Then, the shunted capacitors on top can be expressed as:

$$c_{eq1} = c_{b1} + c_{b2} + c_R; \tag{4.9}$$

Similarly, the shunted capacitors at the bottom can also be expressed through Equation 4.8 as:

$$c_{eq2} = c_{b3} + c_{b4} + c_{mw}. \tag{4.10}$$

Figure 4.12 shows the equivalent circuit model of the Pokemon qubit, from which can be seen that the parallel capacitors formed by c_{eq1} and c_g1 are connected in series with the parallel capacitors formed by c_{eq2} and c_g2, with the series-equivalent capacitor shunted with C_t.

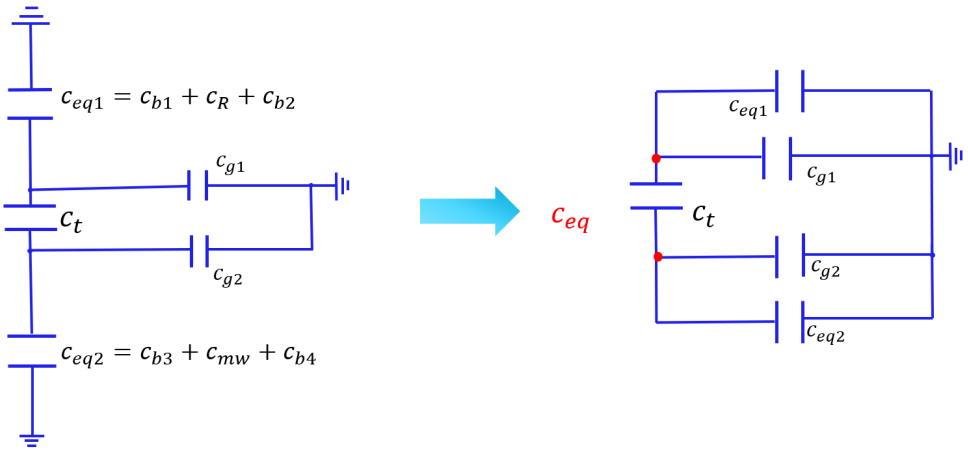


Figure 4.12: Equivalent Pokemon Qubit Circuit Model

When two capacitors C_{s1} and C_{s2} are connected in series, the equation of the total capacitance can be expressed as:

$$C_{series} = \frac{C_{s1} \cdot C_{s2}}{C_{s1} + C_{s2}}. \tag{4.11}$$

Utilize the equation above, the series-equivalent capacitor in the qubit circuit model in Figure 4.12 can be expressed as:

$$
\begin{aligned}
c_{eq3} &= \frac{(c_{eq1}+c_{g1})\cdot(c_{eq2}+c_{g2})}{(c_{eq1}+c_{g1})+(c_{eq2}+c_{g2})} \\
&= \frac{(c_{b1}+c_{b2}+c_R+c_{g1})\cdot(c_{b3}+c_{b4}+c_{mw}+c_{g2})}{(c_{b1}+c_{b2}+c_R+c_{g1})+(c_{b3}+c_{b4}+c_{mw}+c_{g2})}.
\end{aligned}
\tag{4.12}
$$

This series-equivalent capacitance is connected in parallel with C_t. Then, the parallel-equivalent capacitor formed by c_{eq3} and C_t is the total equivalent capacitor C_{eq} lumped with the SQUID inductor in the Pokemon qubit circuit, i.e.,

$$
\begin{aligned}
C_{eq} = c_{eq3} + C_t &= \frac{(c_{eq1}+c_{g1})\cdot(c_{eq2}+c_{g2})}{(c_{eq1}+c_{g1})+(c_{eq2}+c_{g2})} + C_t \\
&= \frac{(c_{b1}+c_{b2}+c_R+c_{g1})\cdot(c_{b3}+c_{b4}+c_{mw}+c_{g2})}{(c_{b1}+c_{b2}+c_R+c_{g1})+(c_{b3}+c_{b4}+c_{mw}+c_{g2})} + C_t
\end{aligned}
\tag{4.13}
$$

4.3 Simulation Methods

Simulation design is crucial for any complex qubit design and helpful for optimizing multiple quantum bits for different frequencies, which enables a deep understanding of circuit characteristics that are difficult to obtain through measurement or intuition alone. To realize the full-wave EM simulation of the capacitors and the Pokemon qubit, this thesis utilize CST Microwave Studio (CST) for qubit characteristics analysis.

There are two main methods used in CST for Pokemon qubit simulation: frequency domain simulation (RF simulation), and electrostatic simulation (ES simulation), under high and low frequency respectively. The following subsections compare the two simulation methods, with their theory principles, essential settings, and the main simulation results illustrated.

4.3.1 Electrostatic (ES) Simulation

ES simulation is under low-frequency (DC), which means that the circuit characters do not change with the frequency. The purpose of the ES simulation is to compute static electric fields (E-fields) due to DC voltages or charge distributions, used for static charge distribution analysis and capacitance value extraction. This simulation based one of the Maxwell's equation (Poisson's equation):

$$
\nabla \cdot (\varepsilon \nabla V) = -\rho, \tag{4.14}
$$

where ρ is the charge density, ε is the permittivity, and V is the voltage. From the equation, it can be seen that the simulator is time- and frequency- independent.

Figure 4.13 shows the simulation tab of the electrostatic simulation, where the electric potentials for each conductor should be defined manually for capacitor matrix calculation. The voltage values of two conductors spacing with distance should not be equal.

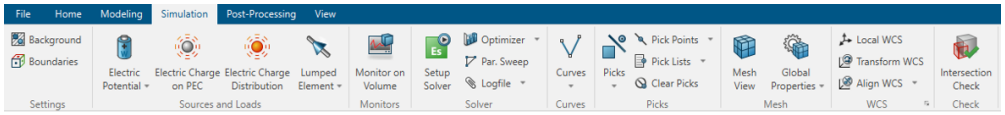


Figure 4.13: ES Simulation tab in CST

With the voltages defined in the ES solver, the capacitance values of each 2 separate pads can be simulated and calculated by the software. The results are shown as the form of a capacitance matrix, which can be imputed in a specific equation to calculate the desired equivalent capacitance.

4.3.2 Frequency Domain (RF) Simulation

The frequency domain simulation is under high-frequency, which means the electromagnetic field propagation and scattering are considered. The RF solver computes steady-state sinusoidal electromagnetic field solutions at specific frequency points, leading to frequency-dependent circuit characters. Compared with the time-domain solver in high-frequency simulation, the frequency domain solver can achieve more accurate results under a very narrow frequency range. The RF simulation based on the two frequency-domain Maxwell's equations:

$$\nabla \times \mathbf{E} = -j\omega\mu\mathbf{H} \tag{4.15}$$

$$\nabla \times \mathbf{H} = j\omega\varepsilon\mathbf{E} + \mathbf{J}, \tag{4.16}$$

where E is the electric field strength, H is the magnetic field strength, J is the current density, ε is the permittivity, and μ is the permeability.

The simulation tab of the frequency domain solver is shown in Figure 4.14. It can be seen that for the RF simulation, the frequency range must be defined, different from the ES solver. With the defined frequencies, the simulation results are shown in each frequency point, i.e., they change with the frequency.

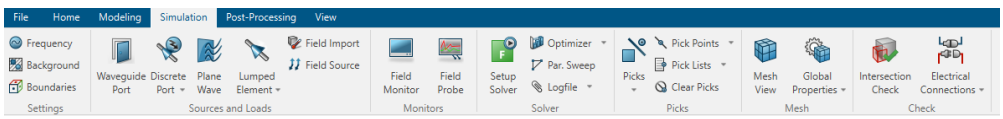


Figure 4.14: RF Simulation tab in CST

Another important setting for the frequency-domain simulation is to insert ports to evaluate the characteristics based on the S-parameter. There are two types of ports: discrete ports and waveguide ports. A waveguide port is used for analyzing signals transmitting through a waveguide such as the coplanar ones. It is a special type of port designed to simulate an infinitely impedance-matched waveguide connected at the other end, thereby minimizing reflections. Discrete ports are inserted wherever it does not make sense to use a waveguide port. It can be used for frequency-domain capacitance estimation through post-processing. Another application of the discrete port is to use it as an alternative to Josephson junctions, which cannot be accurately modeled and simulated using CST Studio. Therefore, using discrete ports allows the inductor to be connected after finite element simulation (in the schematic simulation) to scan the frequency of the quantum bit and find resonant frequencies.

An important output of the RF simulation is the S-parameter, from which the resonant frequency can be determined. To be more specific, S-parameter is usually used to define the wave behavior in a multi-port electric network, which can describe the energy flow in the system. For example, in a 2-port network, the S-parameter is defined as:

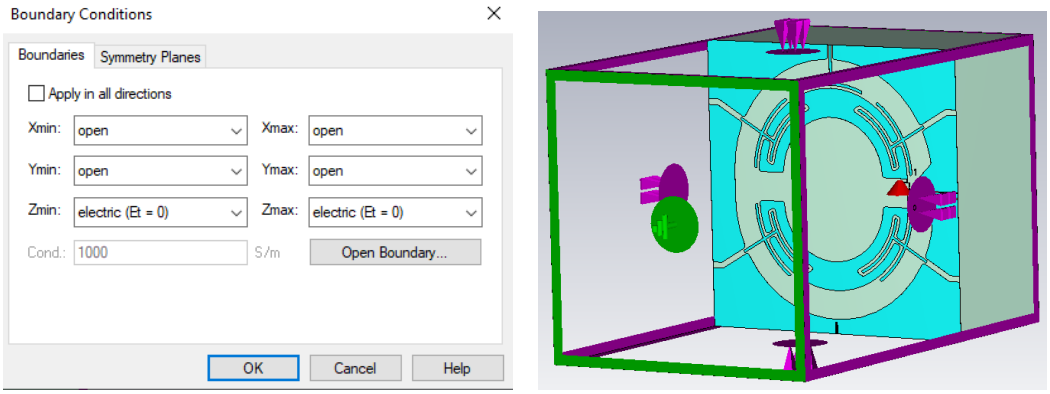
$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}, \tag{4.17}$$

where a_i represents the inserted port and b_i represents the output port ($i = 1,2$). S_{11} is a commonly used parameter which represents the input reflection coefficient in Port 1.

With only one port inserted for simulation, the S-parameter result is S_{11}. From the variation trend of S_{11} with frequencies, the resonance frequency can be defined where S_{11} reaches its minimum value, meaning that the system is well-matched with minimal reflection energy. This will be illustrated in detail in Section 5.2.

4.3.3 General Settings

Both of the two simulation methods should include the background and boundary conditions determined by the circuit chip surroundings, for accurate simulation results. In practice, there is always a metal layer suspended above the qubit circuit with a gap, thus the boundary condition used for this thesis simulation is set in Figure 4.15a, with the schematic diagram shown in Figure 4.15b.



(a) Boundary Condition Settings (b) Boundary Sketch

Figure 4.15: Boundary Conditions used in this thesis

Choosing the correct mesh settings is also crucial for simulation accuracy in both solvers, including choosing reasonable initial mesh and convergence criteria for mesh adaptation.There should be at least two mesh cells side by side in every structure.

It should be noticed that, CST Microwave Studio and similar simulation software cannot fully simulate superconducting materials. Therefore, a surface impedance model is used to simulate superconducting materials [54]. In this model, the resistivity is set to $R = 10^{-18}$ Ω, which is extremely close to zero while avoiding floating-point errors. The reactance value increases linearly with frequency, with $X = 2\pi fL$, where L is typically chosen to be 0.75 pH. The parameter settings of this surface impedance material are shown in Figure 4.16.

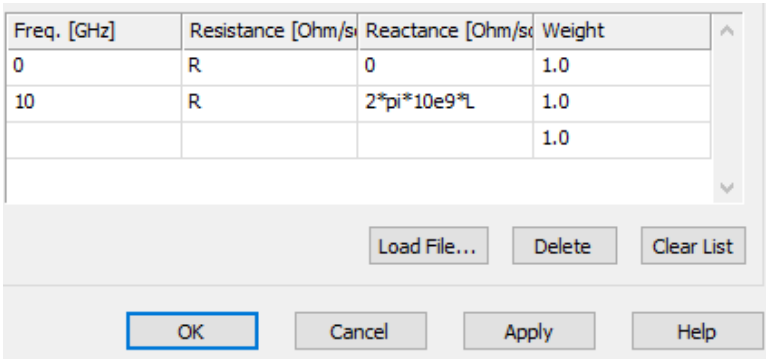


Figure 4.16: Surface Impedance Material Settings in CST

Chapter 5

Simulation

In this chapter, the capacitor models including flip-chip capacitor and the in-plane capacitor models are first simulated in CST Microwave studio, where the in-plane capacitor includes the gap capacitor and the interdigitated capacitor that are illustrated in Chapter 4. Then, Pokemon Qubit models are simulated and analyzed in CST Microwave Studio using both frequency domain simulation and electrostatic simulation, with their typical outputs illustrated. In the last part of this chapter, the role of the capacitor geometries in the qubit is analyzed by doing parameter sweeps.

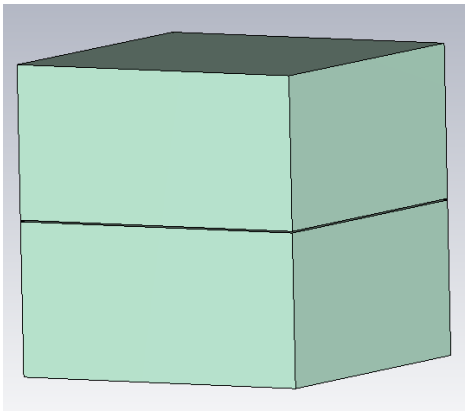
5.1 Capacitor Model Simulation

5.1.1 Flip-Chip Capacitor Simulation

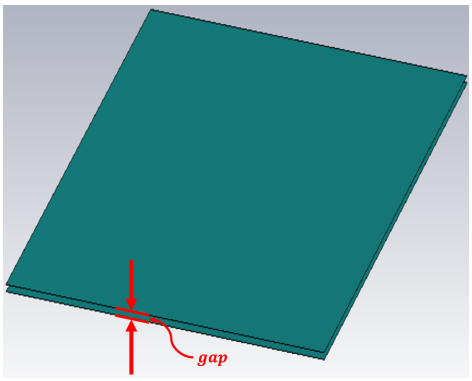
In this section, a flip-chip model is built in CST under the electrostatic (ES) simulation, shown in Figure 5.1, where Figure 5.1b shows the model outlook without the substrates. The two superconducting plates are made of the surface impedance material that illustrated in Section 4.3, placed on a silicon substrate of 2 mm $\times$ 2 mm $\times$ 1 mm. The substrate material is made of loss-free silicon with a permittivity of $\varepsilon = 11.45$.

The relationship between the total capacitance and the gap distance is first evaluated. For this simulation, each plate of the capacitor is a square, i.e., the length and width of the superconducting pads are equal to 1 mm, which means the 2D footprint area of the flip-chip capacitor is $1\,\text{mm}^2$. The gap range between the two plates is from $1\,\mu\text{m}$ to $10\,\mu\text{m}$ with a step of $0.5\,\mu\text{m}$. The set range is based on the fabrication ability in practice, where the minimum gap distance between pads in a flip-chip capacitor should be larger than $1\,\mu\text{m}$. The capacitance values for each condition can be obtained through the capacitance matrix result obtained from the electrostatic simulation. Figure 5.2 shows how the total capacitance of the flip-chip capacitor changes with the distance, from which it can be seen that the capacitance

is inversely proportional to the gap or in other words the vertical distance between the chips.



(a) Flip-chip capacitor model



(b) Flip-chip capacitor (Substrate is hidden for easier visualization)

Figure 5.1: Flip-chip capacitor model in CST

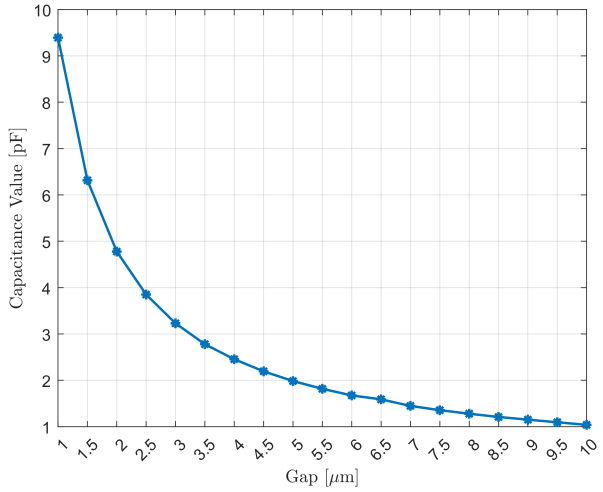


Figure 5.2: Flip-chip capacitance v.s. gap

In addition, the relationship between the flip-chip capacitance and the 2D footprint area is investigated under the RF simulation in CST, where the frequency range of the simulation is between 0.1 and 0.4 GHz, and the 2D area is changed by the variation of the side length *Cond_L* of the plate (square). For different 2D footprint areas, the gap in the capacitor is fixed at 10 µm. Figure 5.3 and 5.4 show the simulation results of the flip-chip capacitance varying with the frequency for different 2D footprint area, where it can be seen that the capacitance value increases with larger 2D footprint area (increasing *Cond_L*).

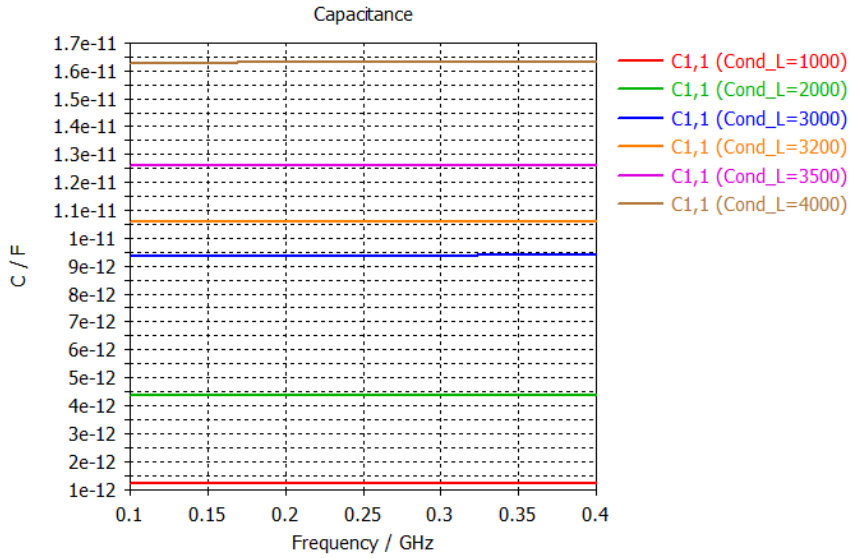


Figure 5.3: Flip-chip capacitance v.s. frequency for $Cond\_L = 1 \sim 4$ mm

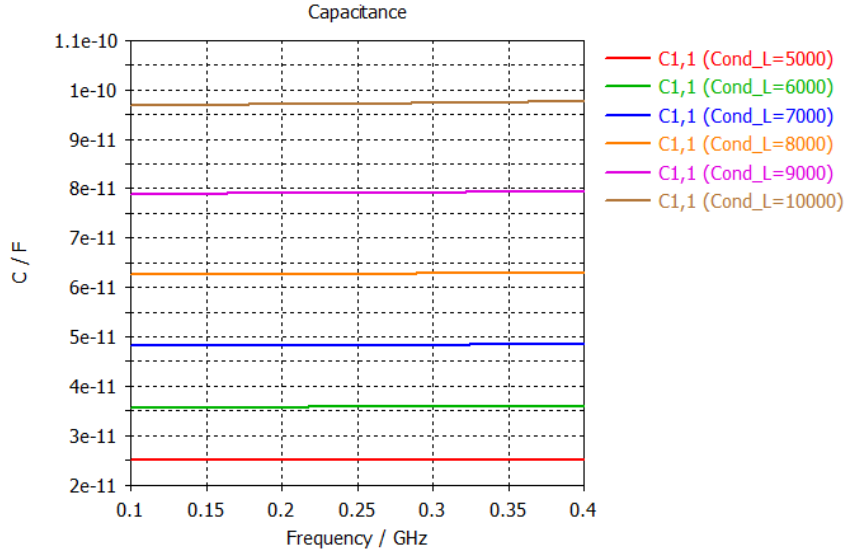


Figure 5.4: Flip-chip capacitance v.s. frequency for $Cond\_L = 5 \sim 10$ mm

5.1.2 In-Plane Capacitor Simulation

In this section, two types of in-plane capacitors are simulated, analyzed, and compared, which are the in-plane parallel plate capacitor and the interdigitated capacitor.

5.1.2.1 Parallel Plate Capacitor

In this part, two identical rectangular superconducting plates with a gap are placed in the same plane on a substrate in CST, where the substrate is made of loss-free silicon with a size of 2 mm $\times$ 2 mm $\times$ 1 mm and the permittivity of $\varepsilon = 11.45$. The superconducting material is the surface impedance model as illustrated in Section 4.3. The 3D model built in CST is shown in Figure 5.5.

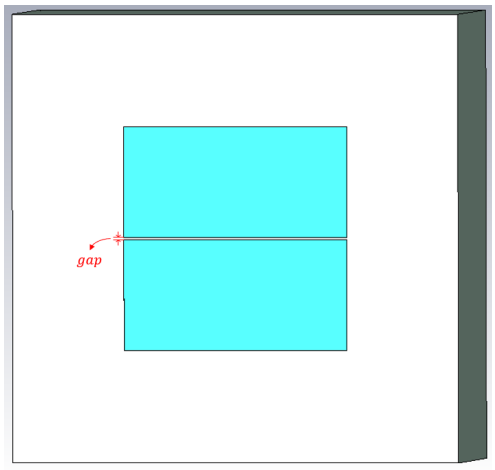


Figure 5.5: In-plane parallel plate capacitor model in CST

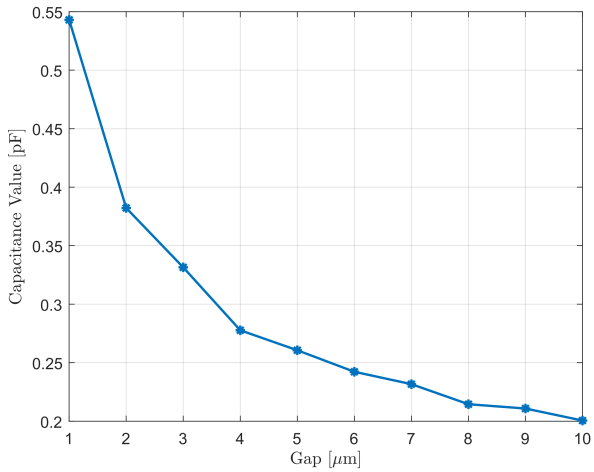


Figure 5.6: In-plane parallel plate capacitance v.s. gap

Similar to the flip-chip capacitor, the relationship between the gap and the total capacitance is first researched through ES simulation. The 2D footprint area is a square with its side length equal to 1 mm, making the area remain at 1 mm^2. The gap

range in the in-plane capacitor is also between 1 µm to 10 µm, where gap $\geq$ 1 µm is the limit of fabrication. The simulation results from the capacitance matrix in CST are plotted in Figure 5.6 through MATLAB, where it can be seen that the total capacitance of the in-plane parallel plate capacitor decreases with longer spacing distance.

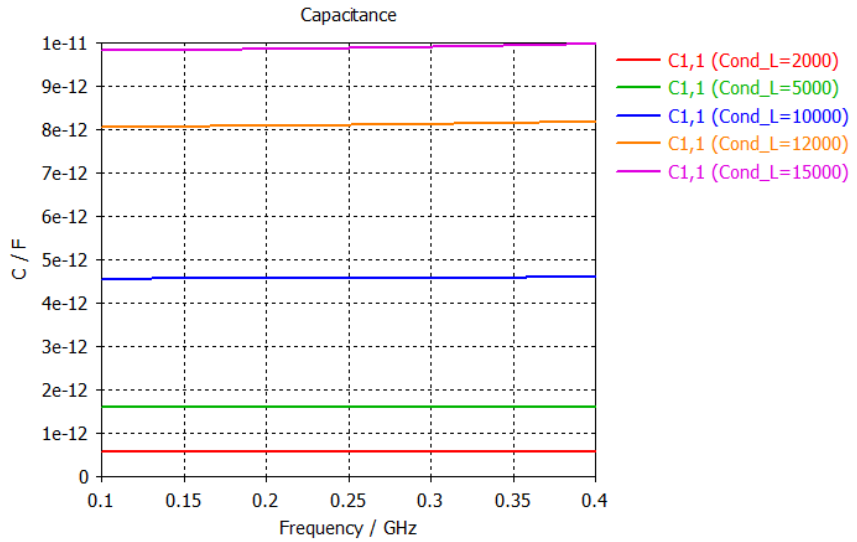


Figure 5.7: Parallel plate capacitance v.s. frequency for $Cond\_L = 2 \sim 15$ mm

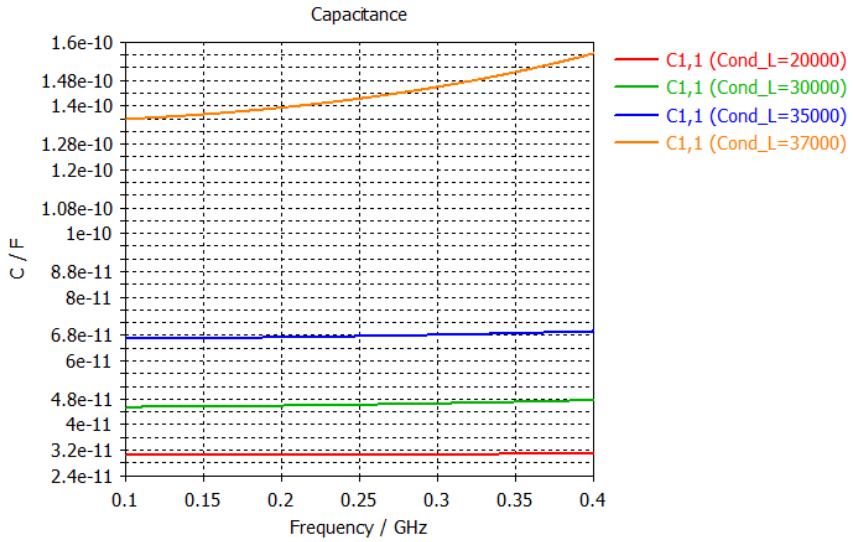


Figure 5.8: Parallel plate capacitance v.s. frequency for $Cond\_L = 20 \sim 37$ mm

The relationship between the in-plane parallel plate capacitance and the 2D footprint area is then evaluated under the RF simulation in CST, with the frequency

range between 0.1 and 0.4 GHz, and the 2D area is changed by the variation of the side length *Cond_L*. The gap in the capacitor is fixed at 10 µm for different areas. Figure 5.7 and 5.8 show the simulation results of the in-plane parallel plate capacitance varying with the frequency for different 2D footprint area, from which it can be seen that the capacitance increases with the 2D footprint area, similar to that demonstrated in the flip-chip capacitors.

The comparison between the flip-chip capacitor and the in-plane parallel plate capacitor is also discussed using the simulation results in the previous sections, where the gap distance for the two types of capacitor is 10 µm. The capacitance value for each 2D footprint area is chosen at 0.25 GHz. Figure 5.9 shows the comparison between the flip-chip capacitor and the in-plane capacitor, where the simulated capacitance results are shown in a limited range between 1 pF and 50 pF (1 pF = 10^{-12} F). Besides the relationship between the capacitance and the area that has been discussed, it can be seen that, for the same area value, the flip-chip capacitance value is much larger than that of the in-plane gap capacitor. This phenomenon paves a possible way of using flip-chip technology to achieve higher capacitance values under a fixed 2D footprint area.

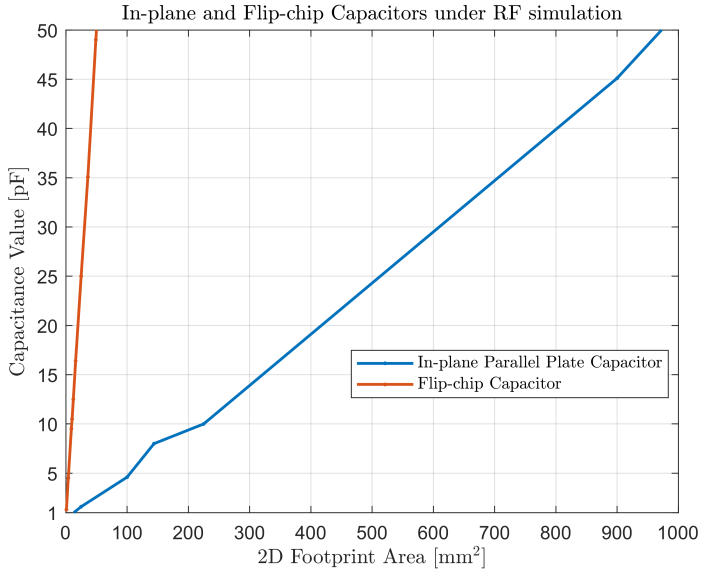


Figure 5.9: Comparison between flip-chip and in-plane parallel plate capacitors

5.1.2.2 Interdigitated Capacitor

Another type of in-plane capacitor, the interdigitated capacitor, is discussed in this sub-section, with its built structure and its parameters shown in Figure 5.10. In Figure 5.10, '*Cond_L*' and '*Cond_w*' are the length and width of the 2D footprint of the interdigitated capacitor, which define the area of the 2D footprint. The length of each finger in the capacitor is the same, represented by '*finger_L*', and '*finger_w*' is the width of each finger. '*gap*' represents the distance between adjacent fingers, and the space at the end of the fingers between two conductors is represented by '*dis_gap*'. The total number of fingers is represented by '*N*'.

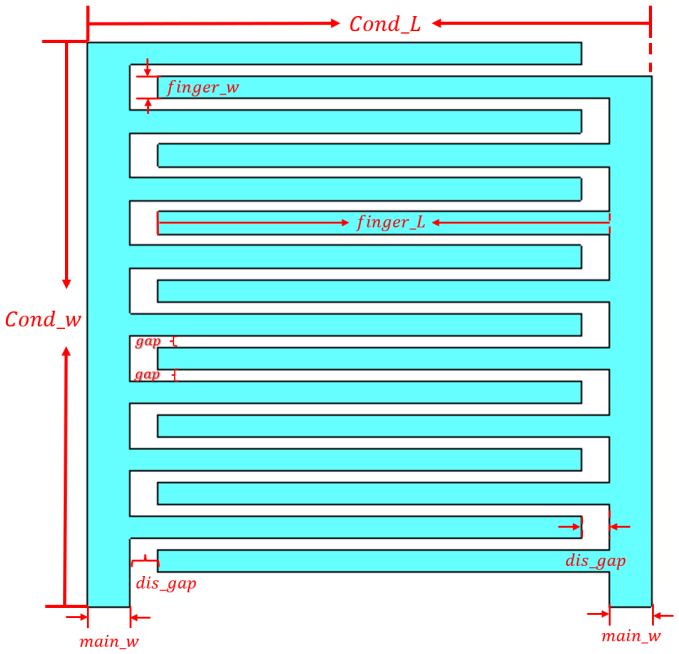
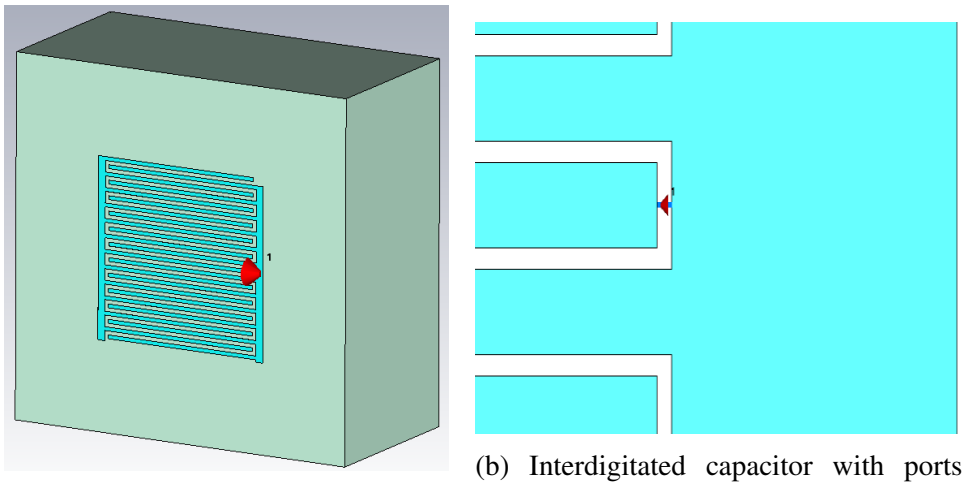


Figure 5.10: Interdigitated capacitor diagram

The interdigitated capacitor is designed using the surface impedance model as a superconducting material, fabricated on a silicon substrate with a permittivity of 11.45. The complete 3D model of the capacitor built in CST Microwave Studio is shown in Figure 5.11a. Due to the long and thin fingers in the interdigitated capacitor, the geometric inductance determined by the conductor shape should not be ignored. Thus in this section, the capacitance value of the interdigitated capacitor is simulated and compared under both electrostatic (ES) and high-frequency (RF) simulations in CST, where the latter (RF simulation) considers the inductive effect at high frequencies while the former (ES simulation) does not. As illustrated in section 4.3, the capacitor values can be derived through the obtained capacitor matrix with the voltages of each conductor defined under the ES simulation, while for the RF

simulation, a discrete port should be input between the two conductors to evaluate the capacitance value, shown in Figure 5.11.

In the following parts, the effect of each parameter (*finger_w*, *gap*, and *finger_L*) on the interdigitated capacitance under fixed 2D footprint area is first studied, after which the relationship between the 2D footprint area and the capacitance value is evaluated.



(a) Interdigitated capacitor with ports

(b) Interdigitated capacitor with ports (Zoomed)

Figure 5.11: Interdigitated capacitor model with ports built in CST

Parameter Sweep under Fixed 2D Footprint Area

In this section, the 2D footprint area of the interdigitated capacitor is fixed at 1 mm^2 (*Cond_L* = *Cond_w* = 1 mm), i.e., the dimension of the capacitor is unchanged for the following simulation. The capacitor is fabricated on a silicon substrate of 2 mm × 2 mm × 1 mm. The influences of the finger length *finger_L*, finger width *finger_w*, gap between adjacent fingers *gap* on the total interdigitated capacitance are discussed. Due to the fact that the 2D footprint area is fixed, either changing *finger_w* or *gap* thereby change the number of fingers *N*.

Finger Width

The influence of the finger width on the total interdigitated capacitor under fixed 2D footprint area is first evaluated, where the range of the finger width is between 10 µm and 40 µm with a step of 5 µm. The gap between adjacent fingers is fixed at *gap* = 20 µm, the finger length is *finger_L* = 800 µm, and the distance at the end of the finger *dis_gap* = 50 µm.

Figure 5.12 shows the relationship between the total capacitance and the finger width under the high frequency simulation (RF simulation) in CST, where the frequency range is between 0.1 GHz and 1.2 GHz. It can be seen that, with its dimension fixed, the total capacitance of an interdigitated capacitor increases as the finger width becomes shorter.

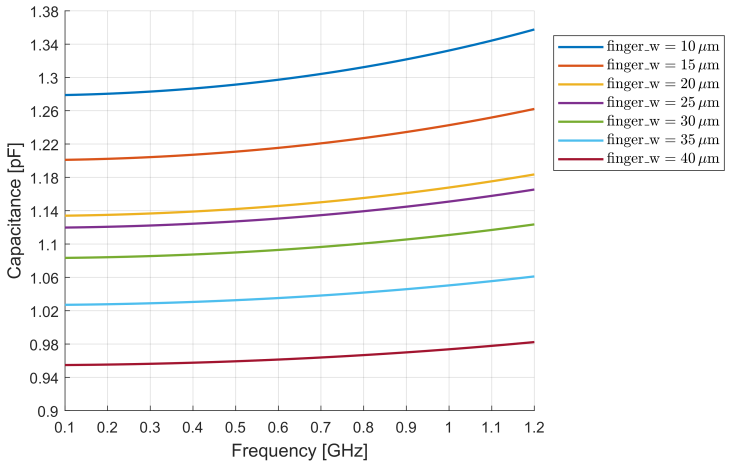


Figure 5.12: Capacitance v.s. frequency for different finger width

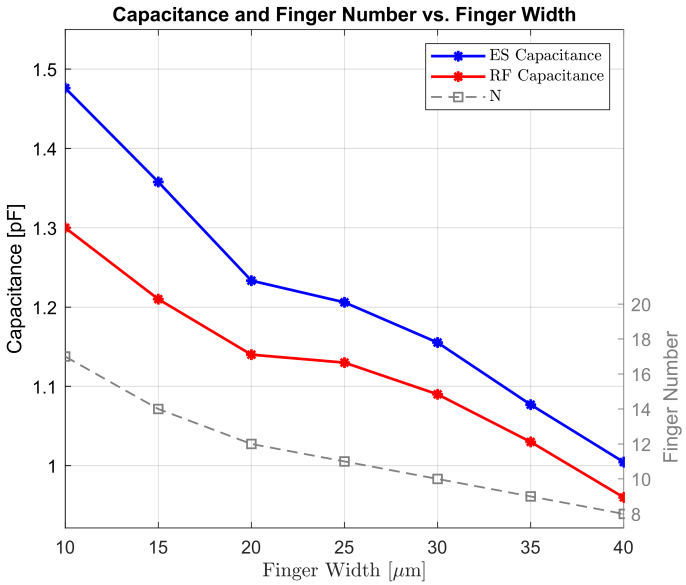


Figure 5.13: Interdigitated capacitance v.s. finger width

Figure 5.13 plots the relationship between the finger width and the total capacitance value under electrostatic (ES) simulation, and compares it with that under

RF simulation, where for ES simulation, each value for a specific finger width is obtained through the capacitance matrix, while the capacitance value for RF simulation is selected at 0.6 GHz. The number of fingers versus the finger width is also plotted in Figure 5.13, from which it can be seen that the number of fingers decreases with larger width due to the fixed 2D footprint area. It can also be noticed that, the varying trends of the total interdigitated capacitance under both ES and RF simulation are the same, i.e., the capacitance value decreases with the finger width under a fixed area, which can be explained by the decreasing number of the fingers in the capacitor. From Figure 5.13, it can also be seen that the simulation result values for the RF simulation are smaller than those under the ES simulation. This is due to the geometric inductance determined by the long and thin fingers in the shape of the interdigitated capacitor, which is considered in the RF simulation, thus lowering the equivalent capacitance value. In practice, the inductive effect at high frequencies should be considered, thus the values obtained from RF simulation are more reliable.

Gap

The influence of the gap distance between adjacent fingers on the total interdigitated capacitor under fixed 2D footprint area is evaluated in this part, where the range of the gap is between 5 µm and 25 µm with a step of 5 µm. The width of fingers is fixed at $finger\_w$ = 20 µm, the finger length is $finger\_L$ = 800 µm, and the distance at the end of the finger dis_gap = 50 µm.

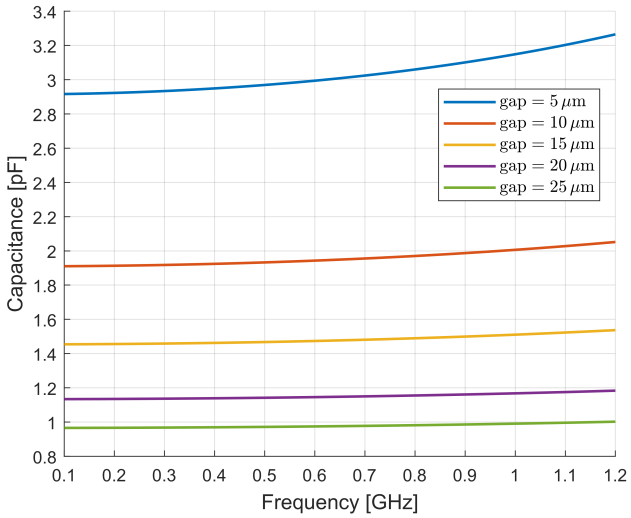


Figure 5.14: Capacitance v.s. frequency for different gap

Figure 5.14 shows the relationship between the total capacitance and the gap distance under the high frequency simulation (RF simulation) in CST, with the same frequency range between 0.1 GHz and 1.2 GHz as that in the previous part. It can be seen that, with the capacitor dimension fixed, the total interdigitated capacitance increases when the gap distance is reduced.

As illustrated previously, the variations of the gap also consequently change the finger number N, influencing the capacitance values. Figure 5.15 shows how the total capacitance under both the ES and RF simulations and the number of fingers change with the gap distance between fingers. Similar to that illustrated previously, the total interdigitated capacitance value for each gap under ES simulation is obtained from the capacitance matrix, and the value for RF simulation is selected at 0.6 GHz. It can be seen that for both the RF and ES simulation, the total capacitance decreases with larger gap distance, which is mainly caused by the decreasing number of fingers when increasing the gap distance under a fixed 2D footprint area. In Figure 5.15, it can also be seen the same phenomenon as that in Figure 5.13, where for the same gap value, the capacitance obtained from RF simulation is smaller than that under the ES simulation, caused by the considered geometric inductance in RF simulation that is illustrated previously.

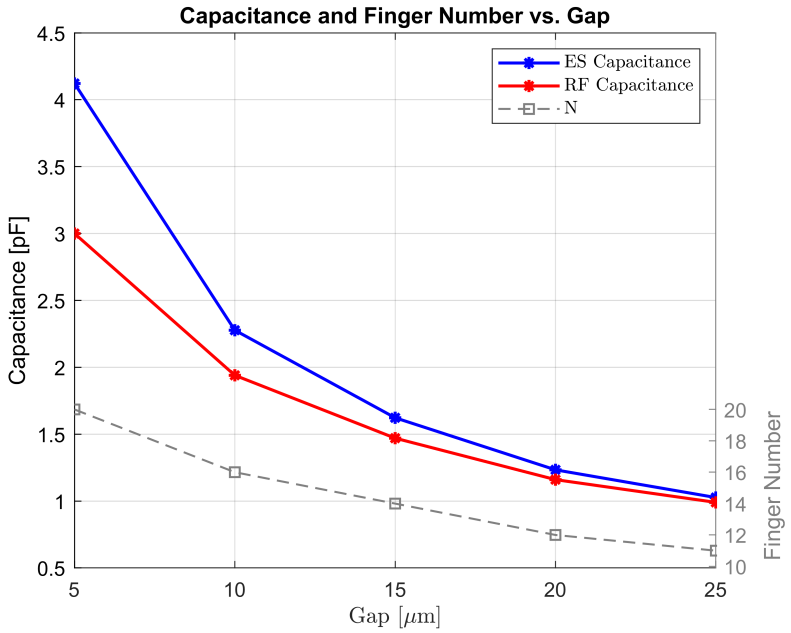


Figure 5.15: Interdigitated capacitance v.s. gap

Finger Length

The influence of the finger length on the total interdigitated capacitor under fixed 2D footprint area is evaluated in this part, where the range of the finger length is between 600 µm and 850 µm with a step of 50 µm. The width of fingers is fixed at *finger_w* = 20 µm, the gap between adjacent fingers is *gap* = 20 µm, and the distance at the end of the finger *dis_gap* = 50 µm. Different from the previous two discussions, due to unchanged finger width and gap distance, the number of fingers under this simulation does not change.

Figure 5.16 shows the relationship between the total capacitance and the finger length under the high frequency simulation (RF simulation) in CST, with the frequency range between 0.1 GHz and 1.2 GHz. It can be seen that, with other parameters and the capacitor dimension fixed, the total interdigitated capacitance increases with the finger length.

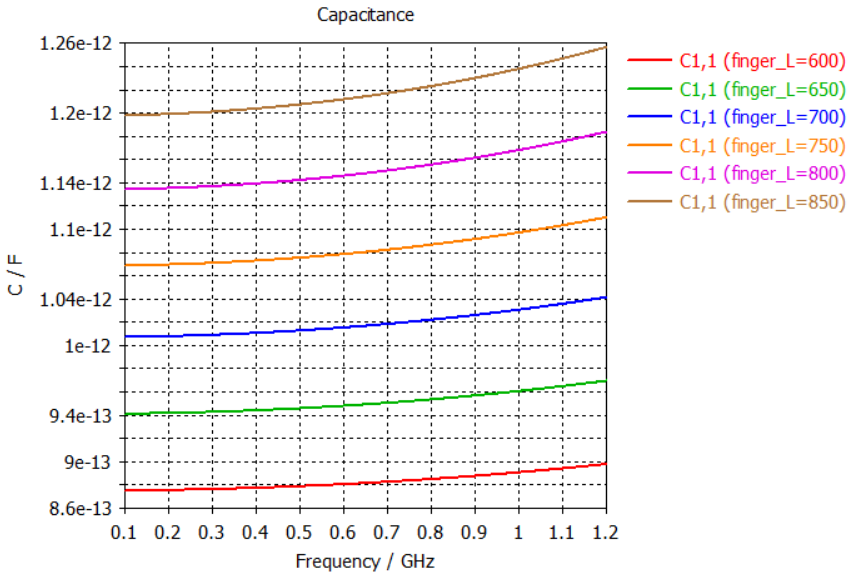


Figure 5.16: Capacitance v.s. frequency for different finger length

Figure 5.17 compares the relationship between the finger length and the total capacitance value under electrostatic (ES) simulation and RF simulation, where each capacitance value for a specific finger length is obtained through the capacitance matrix in ES simulation and selected at 0.6 GHz under RF simulation. It can be noticed that, the varying trend of the total interdigitated capacitance under RF simulation is the same as that under ES simulation, i.e., the capacitance value increases with the finger length under a fixed area, while for RF simulation, each capacitance result under RF simulation is smaller than that under ES simulation with the same

parameter settings due to the geometric inductance, as that explained in the previous part.

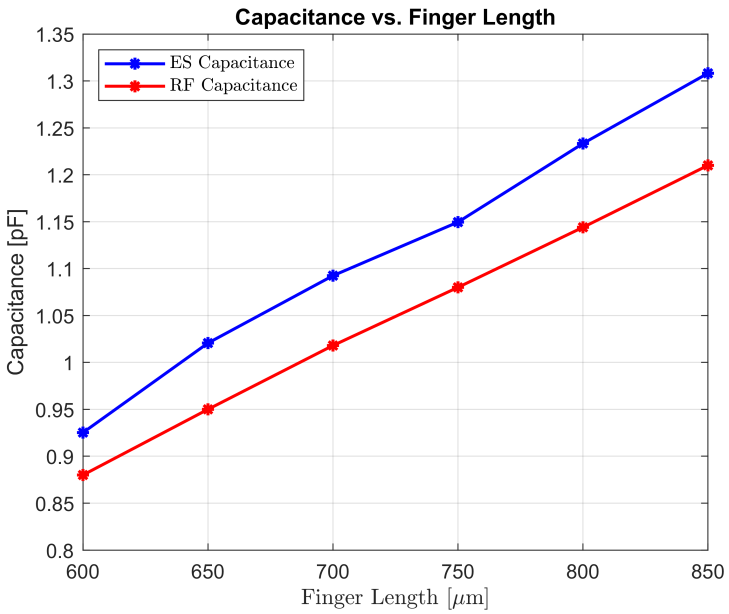


Figure 5.17: Capacitance v.s. finger length

Changing 2D Footprint Area

In this section, the 2D footprint area is changed to evaluate how it influences the total capacitance. For each interdigitated capacitor with different 2D footprint area, it is scaled uniformly by changing the length of the 2D footprint (*Cond_L*), while keeping the internal parameters in the same proportion. To be more specific, $gap = dis\_gap = finger\_w = 0.5main\_w$, and $Cond\_L = Cond\_w$, thus the variation of the 2D footprint area is caused by changing the value of *Cond_L*.

Figure 5.18 shows the relationship between the total capacitance and the 2D footprint length (i.e., *Cond_L*) under the high frequency simulation (RF simulation) in CST, where *Cond_L* is in the range of 1 mm to 6 mm with a step of 1 mm, i.e., the 2D footprint area is between 1 mm^2 and 36 mm^2. The frequency range for simulation is between 0.1 GHz and 0.4 GHz. It can be seen that, the total interdigitated capacitance increases with the 2D footprint area of the capacitor.

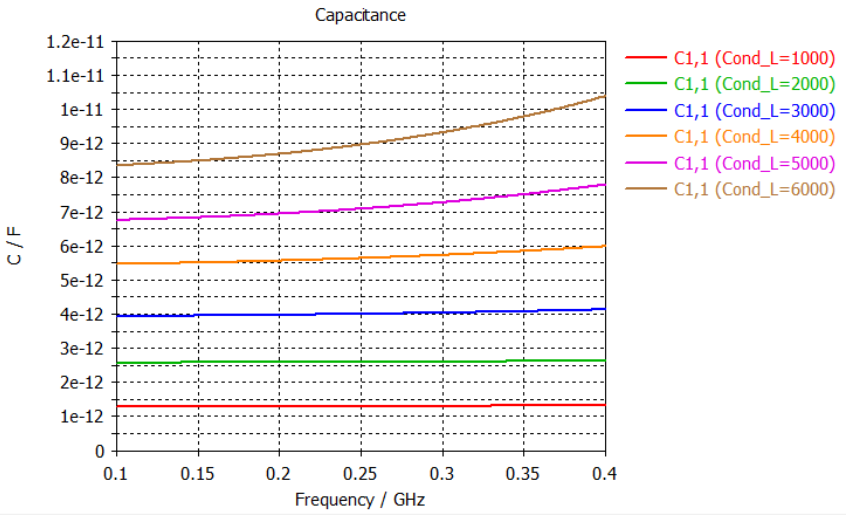


Figure 5.18: Capacitance v.s. frequency for different *Cond_L*

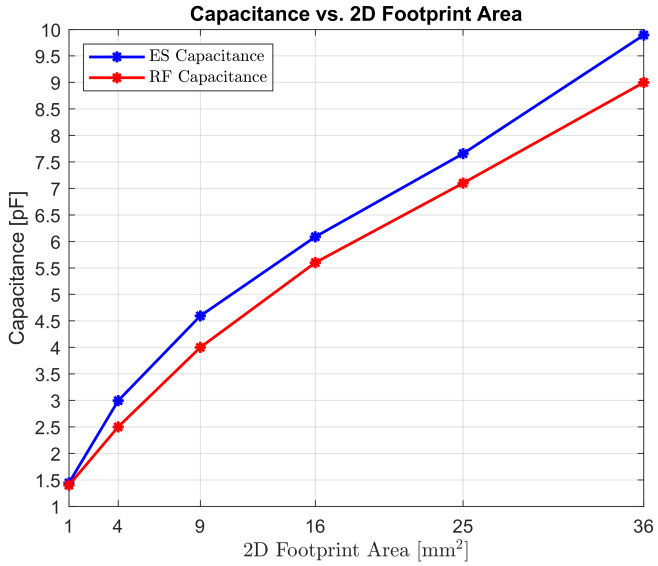


Figure 5.19: Capacitance v.s. finger length

Figure 5.18 compares the relationship between the 2D footprint area and the total capacitance value under electrostatic (ES) simulation and RF simulation, where the area is calculated through $(Cond\_L)^2$, and each capacitance value for a specific finger length is obtained through the capacitance matrix in the ES simulation and selected at 0.25 GHz under RF simulation. It can be noticed that, for both ES and RF simulations, the interdigitated capacitance value increases with the 2D footprint area, but the RF simulation results are lower than that from the ES simulation,

caused by the geometric inductance. It can also be seen that the difference between these two types of simulations becomes larger as the 2D footprint area increases. This is because the geometric inductance is proportional to the geometric length, and increasing the 2D footprint area means longer finger length, thus the inductive effect of the fingers on the total capacitance value becomes more obvious with increasing area.

The comparison between the flip-chip capacitor and the interdigitated capacitor is discussed in the following section. Each capacitance value under a specific 2D footprint area is simulated in the RF solver in CST for both capacitors, which is more realistic in practice. The simulation results for the two capacitors are plotted in Figure 5.20, where the gap distance in the flip-chip capacitor is 10 µm, while for the interdigitated capacitor, the 2D footprint area is changed by different *Cond_L* values with the same proportion of the internal parameters in the capacitor. Because the geometric inductance in the interdigitated capacitor is proportional to the geometric length, the dimension of the capacitor cannot be too large (which means that the finger length of the interdigitated capacitor is too large, leading to a great inductive characteristic or even self-resonating), the 2D footprint area of this capacitor is limited in the range of 1 to 36 mm^2. The simulated capacitance results for the two types of capacitors are shown in a range between 1 pF and 9 pF. It can be seen that both of the two capacitors increase with larger 2D area, and the capacitance value under the flip-chip technology is still larger than that using the in-plane technology (interdigitated capacitor) for the same 2D footprint area.

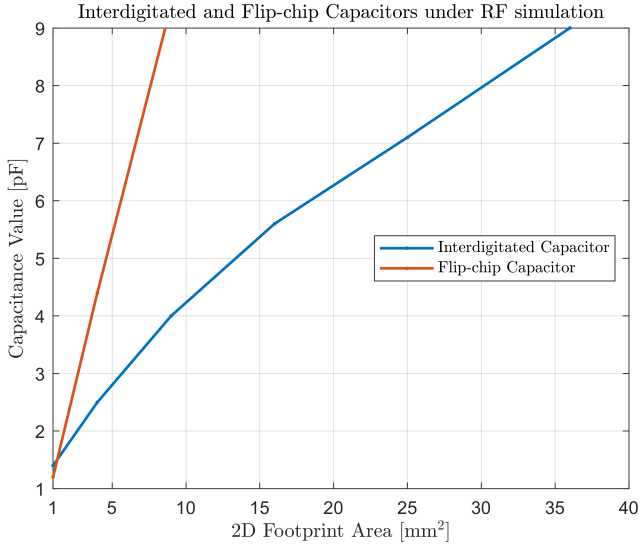


Figure 5.20: Comparison between flip-chip and interdigitated capacitors

Besides the comparison of the above two types of capacitors, Figure 5.21 also

adds the parallel plate capacitance value versus its 2D footprint area under the RF simulation, shown by the gray dotted line, and compares with the interdigitated capacitor and the flip-chip capacitor, where the gap in the parallel plate capacitor is also 10 µm. It can be seen that although the interdigitated capacitor, which is a type of in-plane capacitor, still has a smaller capacitance value than the flip-chip capacitor under the same 2D footprint area, the capacitance difference between these two capacitors is smaller than the difference between the parallel plat capacitor and the flip-chip capacitor.

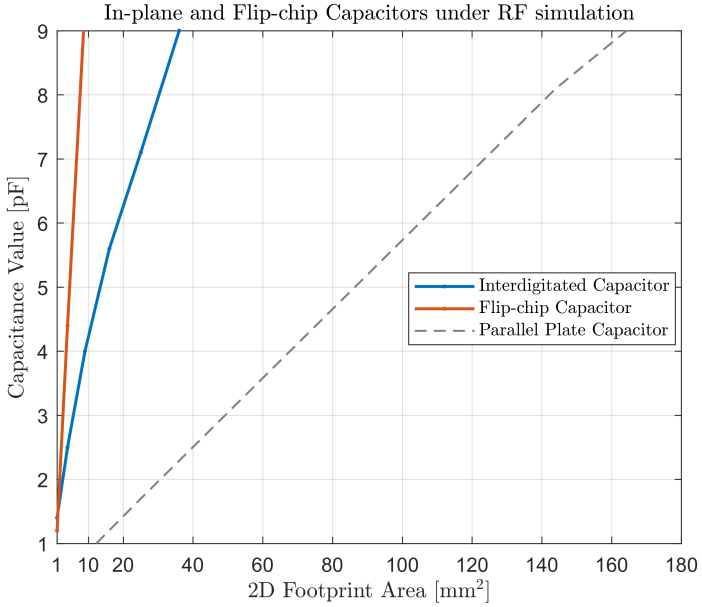


Figure 5.21: Comparison between flip-chip and in-plane capacitors

In summary, although using the interdigitated capacitor increases the capacitance value for the in-plane technologies with fixed 2D footprint area, due to the geometric inductance limit proportional to geometric length, interdigitated capacitors still cannot reach a higher value than using the flip-chip technology under the same area. Thus, the flip-chip technology provides much larger capacitance values for a given fixed 2D footprint than using the in-plane technology to design a qubit, which not only leads to less capacitance energy in the qubit and makes the qubit more stable due to being less sensitive to the charge fluctuations, but also increases the scalability for the integration of qubits on chips, paving a possible way for future modular quantum processing units utilizing this technology.

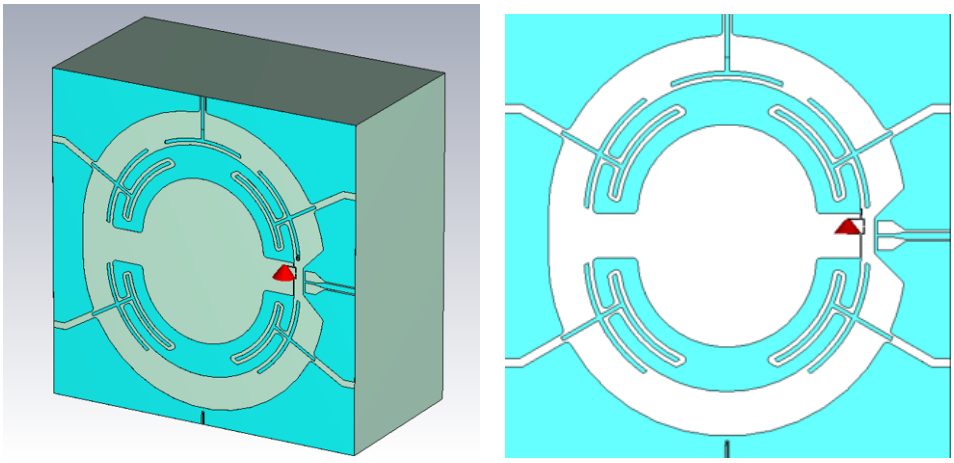
5.2 Pokemon Qubit Simulation

5.2.1 Pokemon qubit simulation with two solvers

In this section, the Pokemon qubit is simulated and compared through both RF and ES simulation, where in both simulations, the superconducting plates forming a Pokemon qubit structure are placed on a 1000 µm × 1000 µm × 525 µm silicon block in CST. Figure 5.22a shows the 3D outlook of the Pokemon qubit built in the frequency domain solver in CST.

5.2.1.1 Frequency domain simulation

In this project for the Pokemon qubit simulation, one discrete port is inserted in the SQUID structure to analyze the equivalent capacitor value of the qubit, shown in Figure 5.22b.



(a) Pokemon qubit 3D structure in RF solver

(b) Discrete port imputed in Pokemon qubit

Figure 5.22: Pokemon qubit model with ports in CST

3D Simulation

In 3D simulation, as illustrated above, a discrete port is inserted in the SQUID structure, and the capacitance of the port can be simulated and calculated by CST to evaluate the equivalent capacitor of the Pokemon qubit over the set frequency range (2 GHz $\sim$ 8 GHz). The result is shown in Figure 5.23, where the capacitance is between 80 fF $\sim$ 88 fF (1 fF = 10^{-15} F).

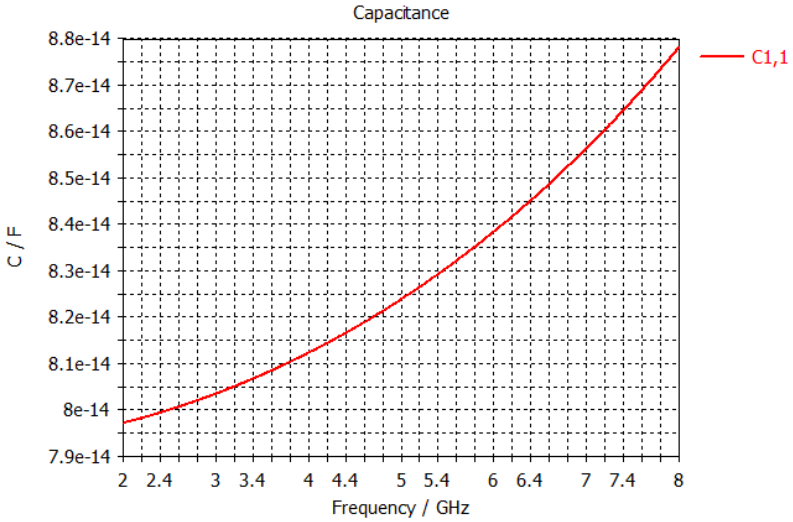


Figure 5.23: Equivalent capacitance result under RF simulation

Schematic Simulation

Apart from the 3D simulation in the frequency domain, schematic simulation is an easy and fast way to analyze the qubit characteristics. The 3D model of the Pokemon qubit under the schematic simulation is shown in Figure 5.24, where the port is connected to a 30 nH inductance, meaning that the equivalent capacitor of this port is lumped with this inductor.

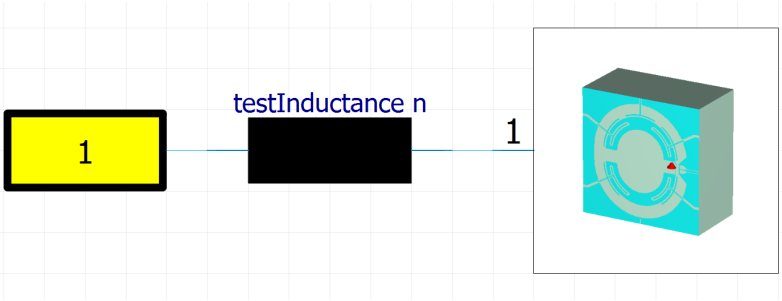


Figure 5.24: Schematic Simulation Circuit Diagram

The S-parameter result versus frequencies for this schematic simulation is shown in Figure 5.25, where the horizontal axis is set to a frequency range of 3 to 4.5 GHz. From the figure, it can be seen that the resonant frequency is about $f_0 \approx 3.24$ GHz.

As illustrated in Section 3.3, the resonant frequency of a LC oscillator can be calculated through:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}. \tag{5.1}$$

With the capacitance results in Figure5.23 and the known inductor value, the theoretical resonant frequency is

$$f_0 = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{30\times10^{-9}\times8.05\times10^{-14}}} = 3.24 \text{ GHz}, \tag{5.2}$$

which is almost consistent with the simulated result in the S-parameter in Figure 5.25.

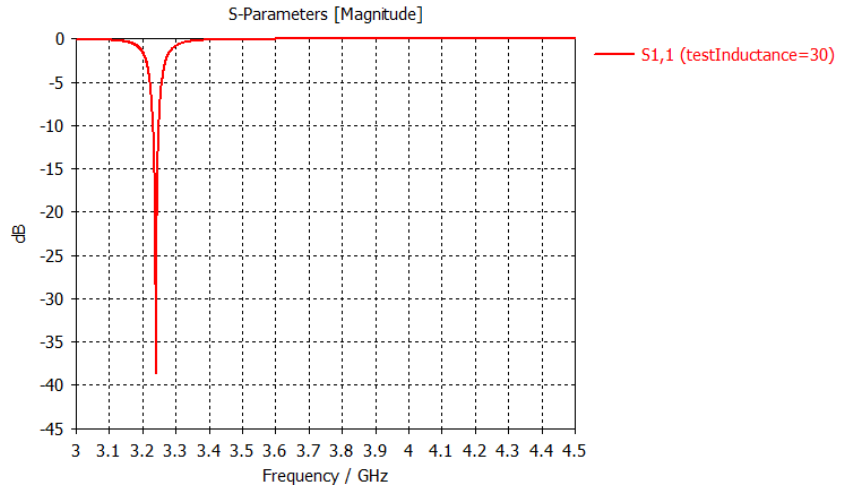


Figure 5.25: S-Parameter Values under Schematic simulation

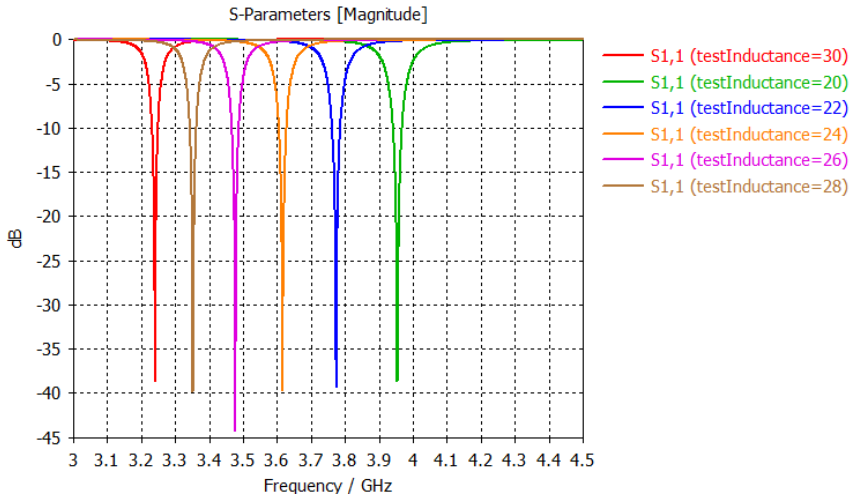


Figure 5.26: S-Parameter under L Sweep

Furthermore, the inductor value in the schematic simulation is swept between 20 nH and 30 nH with a step of 5 nH, resulting in six S-parameter curves shown in Figure 5.26, and the resonant frequencies for each inductor lumped with the equivalent capacitor in the Pokemon qubit can consequently be obtained.

From Figure 5.26, it can be seen that the resonant frequency decreases with increasing inductance. This changing phenomenon of the resonant frequency can be easily explained through Equation 5.1, which means that it is possible to achieve the desired resonant frequency by changing the inductance of the SQUID structure (i.e., tuning the external magnetic field through the flux lines, as that illustrated in section 3.6) with a known qubit structure (i.e., a known capacitance value). In this way, a frequency-tunable quantum platform is designed. Frequency tuning is used to bring two qubits close in frequency to entangle them and de-tune the frequency when entanglement is not desired.

5.2.1.2 Electrostatic Simulation (ES)

As for the electrostatic simulation, the geometry parameter setting of the Pokemon qubit circuit in this simulation is the same as that in the RF simulation, but for this scenario, it is necessary to define the voltage values of each superconducting plate for capacitance calculation. The voltage settings are shown in Figure 5.27. With the defined voltages, the capacitance matrix results are actually shown in Table 5.1.

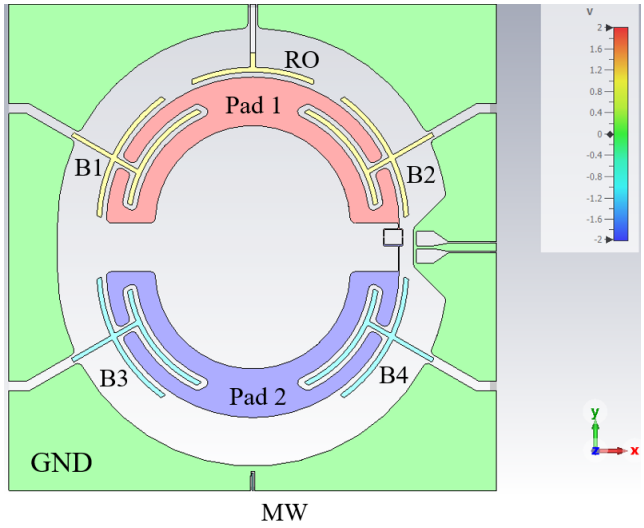


Figure 5.27: Voltage Definition for ES Simulation

Using the theoretical expression of the equivalent capacitance in Equation 4.13 and the table below, the calculated capacitance value in the ES solver is approximately 99.86 fF, almost aligns with, but has about $10 \sim 20$ fF larger than that in

the RF solver. The reason is the same as that illustrated in Section 5.1.2.2, where the geometric inductance due to the geometry and the kinetic inductance due to the superconducting material are considered in the RF simulation, which lowers the equivalent capacitance value, while the equivalent circuit model only considers the capacitive components from the ES simulation which are not affected by those inductors.

Table 5.1: Capacitor Matrix under ES Simulation

	bus1 (fF)	bus2 (fF)	bus3 (fF)	bus4 (fF)	ground (fF)	mw (fF)	pad1 (fF)	pad2 (fF)	read (fF)
bus1	5.034	0.092	0.329	0.043	17.767	0.0005	58.533	1.236	0.491
bus2	0.092	5.015	0.042	0.212	18.541	0.0004	58.688	1.230	0.487
bus3	0.319	0.042	5.342	0.095	17.932	0.005	1.216	58.918	0.030
bus4	0.043	0.212	0.095	5.061	18.721	0.005	1.029	59.060	0.027
ground	17.767	18.541	17.932	18.721	144.498	7.024	41.486	49.328	19.874
mw	0.0005	0.0004	0.005	0.005	7.024	0.084	0.004	0.086	0.0001
pad1	58.533	58.688	1.216	1.029	41.486	0.004	30.612	12.764	22.867
pad2	1.236	1.230	58.918	59.060	49.328	0.087	12.764	32.810	0.253
read	0.491	0.487	0.030	0.027	19.874	0.0001	22.867	0.253	3.480

5.2.2 Capacitance Optimization under Parameter Sweeps

In this section, the role of the capacitor geometries inside the Pokemon qubit is analyzed.

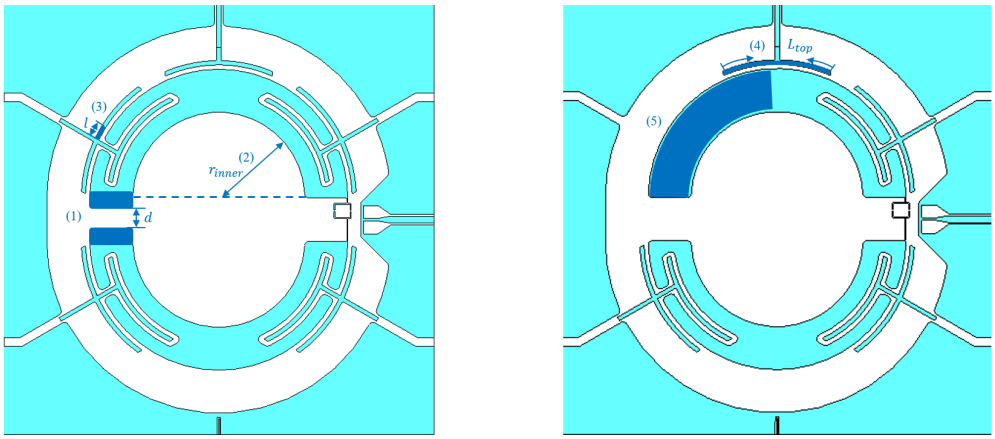


Figure 5.28: Analyzed parts for parameter sweeps

Specifically, five parts of the qubit are simulated through parameter sweeps, shown in Figure 5.28, where the first analysis is for the pad distance d between

Pad 1 and Pad 2, the second analysis is to evaluate the influence of the inner radius r_{inner} of Pad 1 and 2 on the total equivalent capacitor, the third and fourth analysis is to find how the arm length of the bus resonator (Bus 1) and the readout line influences the equivalent capacitor respectively, and the last scenario is to evaluate the capacitance result when removing Bus 1 (i.e., the c_{b1} value in Equation 4.13 is equal to 0). For each scenario, the Pokemon qubit model is simulated both in the RF and ES solvers.

5.2.2.1 Pad Distance

When the distance d between the two pads changes, it is obvious that almost all the capacitance values in Equation 4.13 change, making it difficult to evaluate the total trend of the equivalent value C_{eq} versus d. In both ES and RF simulations, the pad distance d is swept in the range of $20 \sim 80$ μm with a step of 10 μm.

Figure 5.29 shows the parameter sweep results for different d between 20 to 80 μm with a step of 10 μm under the frequency domain simulation, where the frequency range is between 4 GHz and 8 GHz, from which it can be seen that the total equivalent capacitance increases with decreasing distance d between the two superconducting pads.

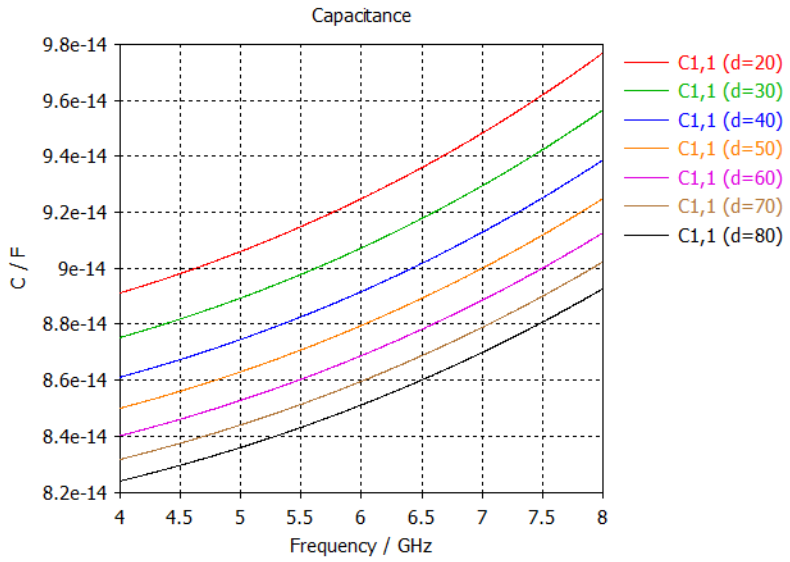


Figure 5.29: C_{eq} changing under d sweep with RF Simulation

The electrostatic simulation of the qubit is also analyzed under each distance value d the same as in the RF simulation, with each theoretical equivalent capacitance C_{eq} for a specifically defined distance d calculated through the obtained capacitor matrix from CST (Ref.C) and the mathematical expression in Equation 4.13.

The relationship between the distance and the total capacitance value is plotted in Figure 5.30 through MATLAB, from which it can be seen that C_{eq} decreases with d, consistent with that in the RF simulation. It can also be seen that, the capacitance value obtained from the RF simulation for each distance d is smaller than that under the ES simulation, which is the same phenomenon as that illustrated previously, due to the inductive characteristic at high frequencies.

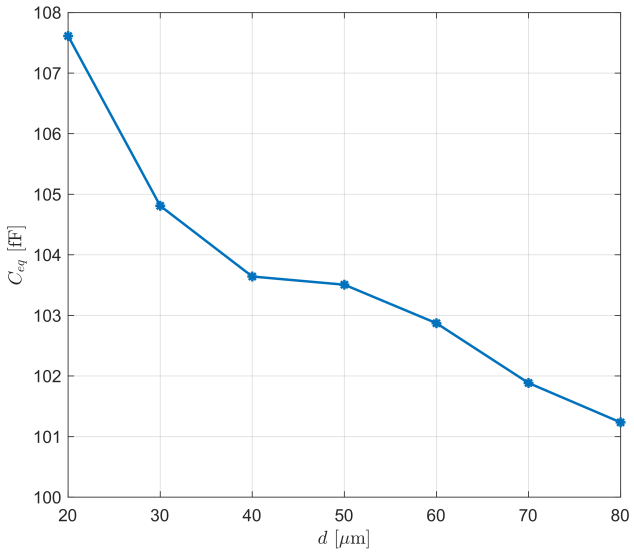


Figure 5.30: Equivalent Capacitance C_{eq} v.s. d under ES Simulation

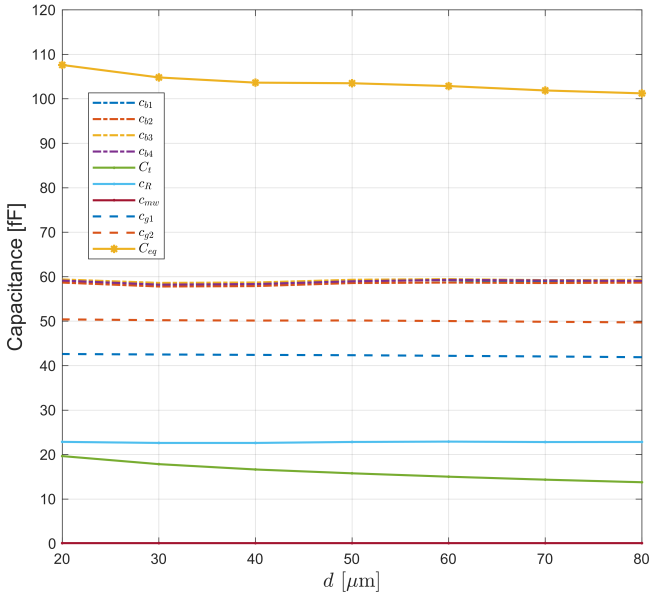


Figure 5.31: Capacitors v.s. d under ES Simulation

Figure 5.31 also shows how each capacitor in the Pokemon qubit circuit changes with the pad distance d. It can be seen that the capacitors formed by the bus resonators and the pads (c_{bi}, $i = 1,2,3,4$) have relatively larger values than other capacitor components in the qubit, while the capacitor formed by the microwave driveline and Pad 2 is very small, nearly equal to zero. Furthermore, the capacitor C_t formed by Pad 1 and Pad 2 changes most when d varies, and it has the same trend as the total equivalent capacitor C_{eq}, which means that the variation of C_{eq} is dominantly affected by C_t.

5.2.2.2 Inner Pad Radius

In this part, the influence of the inner radius r_{inner} of Pad 1 and Pad 2 is evaluated under both the RF and ES simulation. Similarly to that illustrated in the previous section, all the capacitance values in Equation 4.13 change when the inner radius value changes, which means that the changing trend of the equivalent capacitance cannot be easily estimated by the theoretical expression. In the following ES and RF simulations, the inner radius r_{inner} of the two pads is swept in the range of $100 \sim 200$ μm with a step of 20 μm.

Figure 5.32 shows the parameter sweep results for different r_{inner} between 100 to 200 μm under the frequency domain simulation, where the frequency range is between 4 GHz and 8 GHz. It can be seen that the total equivalent capacitance increases with decreasing inner radius r_{inner} of Pad 1 and Pad 2. Due to the unchanged outer radius, decreasing the inner radius will increase the area of the two pads, which means the total equivalent capacitance increases with the area of Pad 1 and Pad 2.

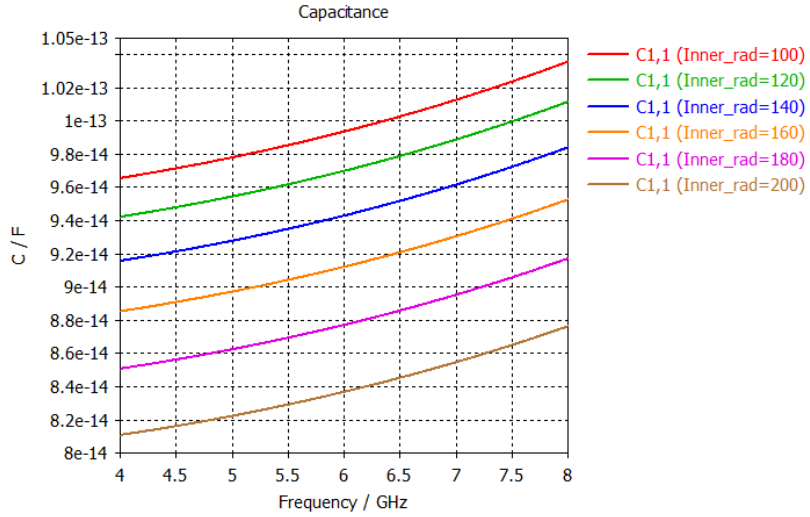


Figure 5.32: C_{eq} changing under r_{inner} sweep with RF Simulation

The electrostatic simulation of the qubit is also analyzed under each radius value r_{inner} the same as in the RF simulation, where the equivalent capacitance C_{eq} for each r_{inner} is calculated theoretically through the capacitance matrix obtained from CST simulation (Ref.C)and the mathematical expression in Equation 4.13. The relationship between the inner radius and the total capacitance value is plotted in Figure 5.33 through MATLAB, from which it can be seen that C_{eq} decreases with the inner radius r_{inner}, i.e., increases with the pad area, consistent with that in the RF simulation, and for each inner radius value r_{inner}, the ES simulation result value is larger than that under the RF simulation.

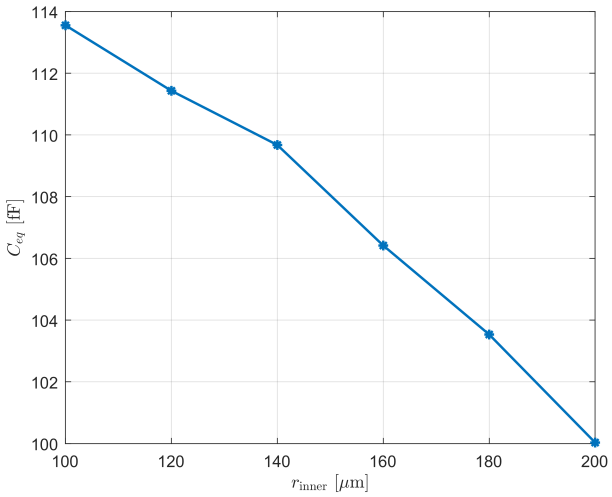


Figure 5.33: C_{eq} v.s. inner radius r_{inner} under ES Simulation

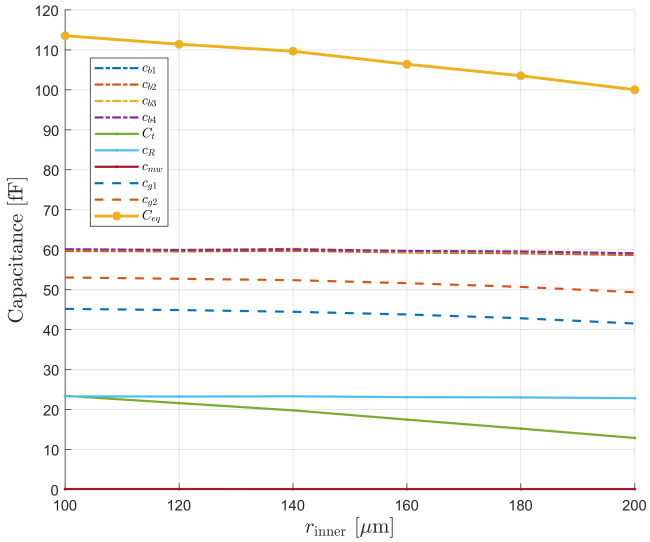


Figure 5.34: Capacitors v.s. inner radius r_{inner} under ES Simulation

Figure 5.34 also shows how each capacitor in the Pokemon qubit circuit changes with the inner radius r_{inner}. Similarly as that shown in Figure 5.31, in this simulation result, it can be seen that the capacitors formed by the bus resonators and the pads have relatively larger values than others, while the capacitor c_{mw} formed by the microwave driveline and Pad 2 is nearly equal to zero. Furthermore, although the variation of the areas of the two pads affects all formed capacitors in the qubit structure, there is the most obvious change in the capacitor C_t formed by Pad 1 and Pad 2, with the same trend as that of the equivalent capacitance, meaning that C_t dominantly affects C_{eq}.

5.2.2.3 Arm Length of Bus Resonator

In this part, the arm length l of the bus resonator 1 (Bus 1) is swept, with its role analyzed through the same method as that illustrated in the above section. In the electrostatic simulation, the capacitance c_{b1} formed by Bus 1 and Pad 1 and the total equivalent capacitance C_{eq} are simulated in CST (Ref.C) and calculated through Equation 4.13 for each arm length value, where the arm length l is from 38 μm to 108 μm. Figure 5.35 shows the ES simulation results. It can be seen that the total capacitance almost remains, with slight increase when extending the arm length, which means that the impact of the arm length l is very tiny.

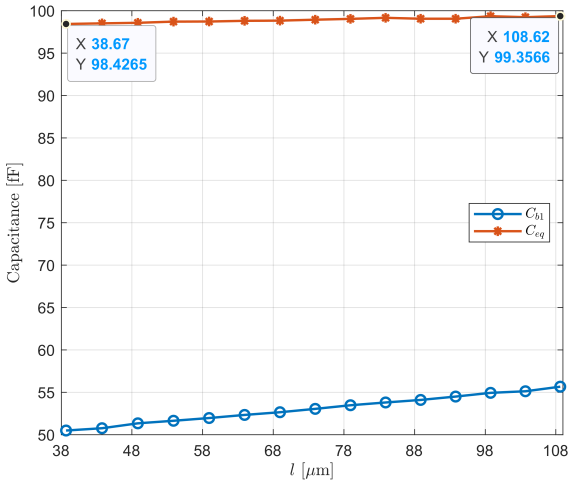


Figure 5.35: C_{eq} and c_{b1} v.s. bus arm length l under ES Simulation

The RF simulation results for $l = 63.94,\ 83.9,\ 103.69$ μm are shown in Figure 5.36, where the results are zoomed around the 6 GHz frequency value. It can be seen that the difference between the three curves is tiny. Specifically, the capacitance difference between the Pokemon qubits when $l = 103.69$ μm and $l = 63.94$ μm is 0.02 pF, extremely smaller than the equivalent capacitance values of the two qubits around 6 GHz, which are nearly the same, with the value about 83 pF.

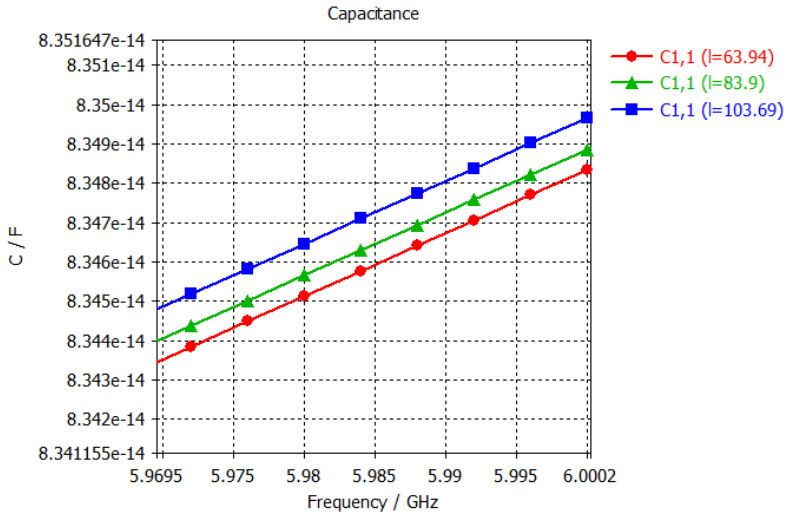


Figure 5.36: C_{eq} changing under the arm length l sweep with RF Simulation

5.2.2.4 Arm Length of Readout Line

In this part, the role of arm length L_{top} of the readout line is analyzed through both the RF and ES simulation. The swept range is between 100 μm and 200 μm with a step of 20 μm. The capacitance c_R formed by the top readout line and Pad 1 and the total equivalent capacitance C_{eq} change with the shape of the readout line.

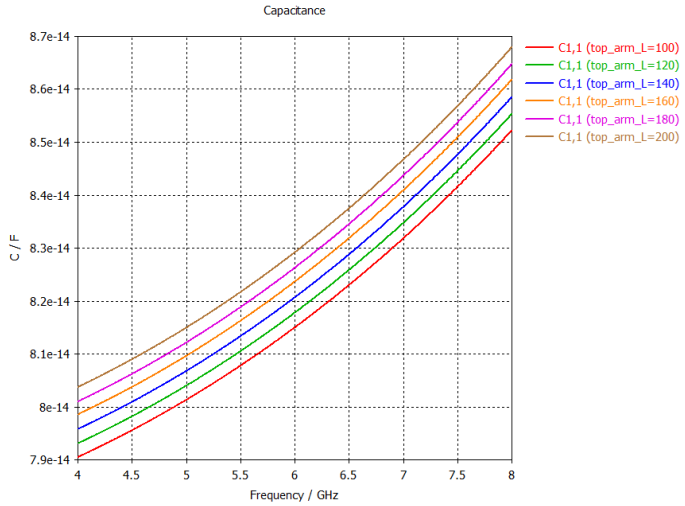


Figure 5.37: C_{eq} changing under the readout length L_{top} sweep with RF Simulation

Figure 5.37 shows the relationship between the total equivalent frequency and the frequency across different arm length, under high-frequency simulation. It can be seen that the capacitance value become larger when the arm length of the readout

line increases. Figure 5.38 shows the static capacitance values of C_{eq} and c_R versus the arm length under the ES simulation, where the result for each length is calculated through the obtained capacitance matrix in CST (Ref.C). It can be seen that both c_R and C_{eq} increase with the arm length, consistent with that in the RF simulation.

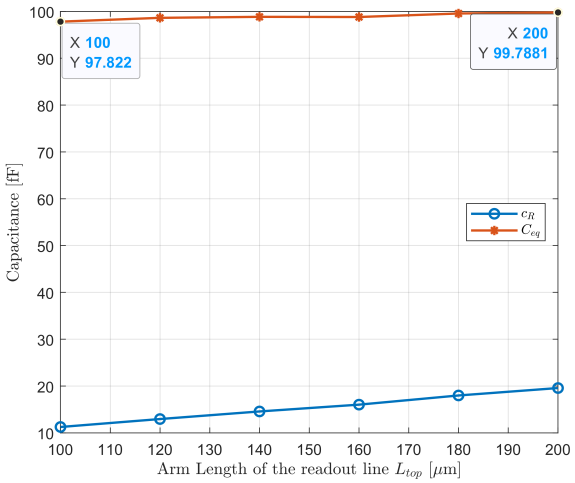


Figure 5.38: C_{eq} and c_R v.s. readout arm length L_{top} under ES Simulation

5.2.2.5 Capacitor Removement

In this part, there is no longer a bus resonator (Bus 1) in the top-left corner of the qubit, with other 3 buses remained.

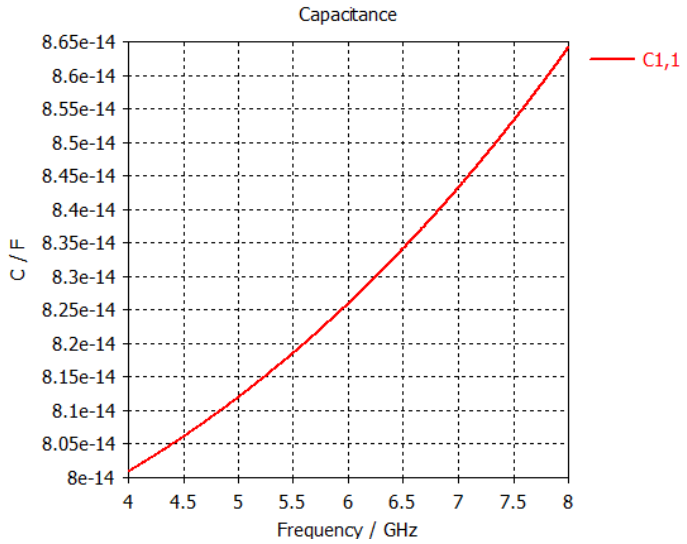


Figure 5.39: Capacitance value when removing C_{b1} under RF Simulation

The RF simulation result is shown in Figure 5.39, where the frequency is between 4 GHz and 8 GHz, and the total equivalent capacitance is about $80.27 \sim 86.62$ fF, lower than that in Section 5.2.1.1 (for the frequency range between 4 GHz and 8 GHz,the capacitance value under RF simulation in Section 5.2.1.1 is about $81.3 \sim 87.7$ fF), which can be easily explained through Equation 4.13 when $c_{b1} = 0$.

Table 5.2: Capacitor Matrix under ES Simulation when removing Bus 1

	/	bus2 (fF)	bus3 (fF)	bus4 (fF)	ground (fF)	mw (fF)	pad1 (fF)	pad2 (fF)	read (fF)
/	/	/	/	/	/	/	/	/	/
bus2	/	5.014	0.043	0.213	18.541	0.0004	58.587	1.231	0.487
bus3	/	0.043	5.358	0.095	18.005	0.005	1.436	58.848	0.031
bus4	/	0.213	0.095	5.066	18.755	0.005	1.063	59.059	0.028
ground	/	18.541	18.005	18.755	145.747	6.478	50.444	49.550	20.097
mw	/	0.0004	0.005	0.005	6.478	0.086	0.004	0.088	0.0002
pad1	/	58.587	1.436	1.063	50.444	0.004	34.345	13.665	23.246
pad2	/	1.231	58.848	59.059	49.550	0.088	13.665	32.858	0.256
read	/	0.487	0.031	0.028	20.097	0.0002	23.246	0.256	3.501

The capacitance matrix result in the ES simulation of the Pokemon qubit is shown in Table 5.2, and the theoretical value of the equivalent capacitance is calculated to be $C_{eq} \approx 87.584$ fF through Equation 4.13, which is about $1 \sim 7.6$ fF larger than the RF result without considering geometric and kinetic inductance in the circuit, also consistent with that illustrated in the previous sections.

Chapter 6

Conclusion

6.1 Conclusions

In this thesis, a novel superconducting qubit for lower loss energy and longer coherence time named 'Pokemon qubit' is analyzed, with its structure compared with that of a typical superconducting qubit (Starmon qubit). The theoretical working principle of the Transmon qubit (which is a type of a superconducting qubit) is first introduced, with the working principle of its important components such as Josephson junctions and the SQUID structure introduced. The circuit model of the Pokemon qubit is then derived and simplified, with its total equivalent capacitance for determining the resonant frequency is mathematical expressed in Equation 4.13.

Two main technologies for designing a capacitance model are introduced and compared, which are the flip-chip capacitor and the in-plane capacitor respectively. It can be seen that, under the same 2D footprint area, the flip-chip capacitance has a larger value than the in-plane capacitance, which can be used to increase the capacitance values under a fixed 2D footprint area. The in-plane capacitance can be increased through introducing a different geometry structure (like the interdigitated capacitance illustrated in this thesis) under the same 2D footprint area for in-plane technology. It can be seen that by using the interdigitated capacitor rather than the simple in-plane parallel plate capacitor, the capacitance value increases obviously with fixed 2D area. Specifically, for the interdigitated capacitor with a fixed 2D footprint area, by increasing the number of fingers (both by decreasing the finger width and the gap with unchanged area) and the finger length, the capacitance value will increase. It should also be noticed that in practical high-frequency systems, the geometric inductive influence of the superconducting fingers should be considered, which means that the equivalent total capacitance value can be smaller than that in the static system. The inductive characteristic of the superconducting plates may even lead to negative capacitance results or self-resonating under RF simulations in CST, which should be considered and avoided in the capacitor design.

The role of the superconducting qubit geometry of the Pokemon qubit on the total equivalent capacitance is then considered and simulated under two types of simulation, i.e., electrostatic simulation (ES simulation) and high-frequency domain simulation (RF simulation), where the equivalent capacitance value of the Pokemon qubit can be obtained through post-processing S-parameter result in RF simulation and through the capacitance matrix in ES simulation. For the frequency-domain simulation, using the schematic simulation is an easy and fast way to analyze the qubit resonant frequency for the qubit design. Five main parameters of the qubit geometry are swept with their influence analyzed. In general, the total capacitance value of the Pokemon qubit is determined by all the components in the qubit structure. To be more specific, the total capacitance increases when the area of the two main pads in the qubit center (Pad 1 and Pad 2) becomes larger, either by decreasing the distance of the two pads or by shortening the inner radius of the two pads. The equivalent capacitance also increases with the arm length of the bus resonator and the readout line, and this is because the increased arm length makes the corresponding capacitance larger, which contributes to an increase in the total equivalent capacitance. If one bus resonator is removed, only remaining other three buses, the total capacitance value will decrease. These analyses and simulations of capacitance are useful practice in determining the required lumped inductor value in the SQUID structure by tuning the external magnetic flux to achieve the desired resonant frequency of the qubit.

6.2 Future work

In the future, one possible exploration is to design more high-performance superconducting qubits to reduce the energy loss and extend the coherence time of the qubit. This improvement can be achieved by optimizing the geometry of the qubit (similar to the method used in this thesis) and its surrounding circuit to suppress dielectric and surface losses, or by engineering materials with lower intrinsic dissipation.

Another possible research area can focus on the combination of the flip-chip technology and the typical superconducting qubit design. Due to the higher capacitance value by using the flip-chip technology under a fixed 2D footprint area, and lower energy loss of the improved qubit structure (Pokemon qubit) for the SQUID-based Transmon qubit design, future research could combine the two technologies to design a flip-chip Transmon qubit for desired higher capacitance values (if needed) with lower energy loss for reliable quantum computing.

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Appendix A

Symbols

In this appendix, the overview of frequently used symbols and nomenclature in this thesis are given below.

List of constants

h (resp. $\hbar$)	Planck constant resp. reduced Planck constant: $\hbar = h/2\pi$
e	Electron charge
Φ_0	Superconducting flux quantum: $\Phi_0 = \dfrac{h}{2e}$
ε_0	Permittivity of the free space

List of symbols

i	Imaginary unit
$\|\psi\rangle$	Quantum state
ω	Angular frequency
$\mathcal{L}$	Lagrangian
T	Kinetic energy
U	Potential energy
$\mathcal{H}$	Classical Hamiltonian
H	Quantum Hamiltonian
C	Capacitance

L	Inductance
Z_0	Characteristic impedance
Φ	Flux
$\dot{\Phi}$	Time derivative of the flux
ϕ	Reduced (dimensionless) flux: $\phi = \frac{2\pi\Phi}{\Phi_0} = \frac{2e\Phi}{\hbar}$
φ	Phase in $[0, 2\pi)$
$\hat{\Phi}$	Quantized flux
$\hat{\phi}$	Quantized dimensionless flux
Q	Charge
q	Reduced (dimensionless) charge: $q = \frac{Q}{2e}$
$\hat{Q}$	Quantized charge
$\hat{q}$	Quantized dimensionless charge
$\hat{a}$	Annihilation
$\hat{a}^\dagger$	Creation
E_C	Charging energy associated with a capacitance C: $E_C = \frac{e^2}{2C}$
E_L	Inductive energy associated with an inductance L: $E_L = \frac{\Phi_0^2}{4\pi^2 L}$
I_c	Critical current
E_J	Josephson energy associated with a Josephson junction: $E_J = \frac{\Phi_0 I_c}{2\pi}$
L_J	Josephson inductance associated with a Josephson junction: $L_J = \frac{\Phi_0^2}{4\pi^2 E_J}$
v_b	Voltage in time domain
i_b	Current in time domain
$\mathbb{1}$	The identity matrix/operator
ε_r	Relative permittivity

Appendix B

Abbreviations

This appendix details some abbreviations used in this thesis writing.

List of abbreviations

Qubit(s)	Quantum bit(s)
SQUID(s)	Superconducting Quantum Interference Device(s)
CPB	Cooper pair box
TLS	Two-level systems
JJ	Josephson Junction
EM simulation	Electromagnetic simulation
IDC	Interdigitated Capacitor
GND	Ground plane
RO line	Readout line
MW drive line	Microwave drive line
ES simulation	Electrostatic simulation
RF simulation	Frequency domain simulation

Appendix C

Capacitance matrix results in CST

This appendix shows the capacitance matrix results for the Pokemon qubit under electrostatic simulation with different parameters in Section 5.2.2 in Chapter 5.

Capacitance matrix for different pad distance *d* in 5.2.2.1

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
mw	pad1	pad2	read		
bus1	5.112314e-15 F	8.844768e-17 F	2.503411e-16 F	3.950279e-17 F	1.750872e-14 F
	4.512940e-19 F	5.923376e-14 F	1.325341e-15 F	4.888550e-16 F	
bus2	8.844768e-17 F	5.008355e-15 F	3.932471e-17 F	2.127393e-16 F	1.855018e-14 F
	4.455365e-19 F	5.868346e-14 F	1.243506e-15 F	4.878045e-16 F	
bus3	2.503411e-16 F	3.932471e-17 F	5.145416e-15 F	9.154797e-17 F	1.763740e-14 F
	4.915599e-18 F	1.310082e-15 F	5.937781e-14 F	2.745483e-17 F	
bus4	3.950279e-17 F	2.127393e-16 F	9.154797e-17 F	5.058259e-15 F	1.875191e-14 F
	4.922001e-18 F	1.043348e-15 F	5.912790e-14 F	2.737867e-17 F	
ground	1.750872e-14 F	1.855018e-14 F	1.763740e-14 F	1.875191e-14 F	1.438660e-13 F
	6.634064e-15 F	4.262099e-14 F	5.041230e-14 F	1.995107e-14 F	
mw	4.512940e-19 F	4.455365e-19 F	4.915599e-18 F	4.922001e-18 F	6.634064e-15 F
	8.550276e-17 F	3.981999e-18 F	8.929383e-17 F	1.481171e-19 F	
pad1	5.923376e-14 F	5.868346e-14 F	1.310082e-15 F	1.043348e-15 F	4.262099e-14 F
	3.981999e-18 F	3.143030e-14 F	1.965787e-14 F	2.285827e-14 F	
pad2	1.325341e-15 F	1.243506e-15 F	5.937781e-14 F	5.912790e-14 F	5.041230e-14 F
	8.929383e-17 F	1.965787e-14 F	3.360825e-14 F	2.634885e-16 F	
read	4.888550e-16 F	4.878045e-16 F	2.745483e-17 F	2.737867e-17 F	1.995107e-14 F
	1.481171e-19 F	2.285827e-14 F	2.634885e-16 F	3.475371e-15 F	

Figure C.1: Capacitance matrix for $d = 20\,\mu\text{m}$

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground	mw	pad1	pad2	read
bus1	5.114349e-15 F	8.841025e-17 F	2.532808e-16 F	3.959115e-17 F	1.737987e-14 F	4.518590e-19 F	5.835625e-14 F	1.315211e-15 F	4.862126e-16 F
bus2	8.841025e-17 F	4.996133e-15 F	3.940864e-17 F	2.117672e-16 F	1.839731e-14 F	4.431310e-19 F	5.780308e-14 F	1.238453e-15 F	4.849128e-16 F
bus3	2.532808e-16 F	3.940864e-17 F	5.147996e-15 F	9.150641e-17 F	1.751107e-14 F	4.893201e-18 F	1.297559e-15 F	5.861011e-14 F	2.752860e-17 F
bus4	3.959115e-17 F	2.117672e-16 F	9.150641e-17 F	5.045701e-15 F	1.859012e-14 F	4.879088e-18 F	1.039857e-15 F	5.821873e-14 F	2.727537e-17 F
ground	1.737987e-14 F	1.839731e-14 F	1.751107e-14 F	1.859012e-14 F	1.438352e-13 F	6.250539e-15 F	4.250907e-14 F	5.021872e-14 F	1.969669e-14 F
mw	4.518590e-19 F	4.431310e-19 F	4.893201e-18 F	4.879088e-18 F	6.250539e-15 F	8.537230e-17 F	3.952144e-18 F	8.825511e-17 F	1.474667e-19 F
pad1	5.835625e-14 F	5.780308e-14 F	1.297559e-15 F	1.039857e-15 F	4.250907e-14 F	3.952144e-18 F	3.138501e-14 F	1.784750e-14 F	2.261644e-14 F
pad2	1.315211e-15 F	1.238453e-15 F	5.861011e-14 F	5.821873e-14 F	5.021872e-14 F	8.825511e-17 F	1.784750e-14 F	3.355589e-14 F	2.620657e-16 F
read	4.862126e-16 F	4.849128e-16 F	2.752860e-17 F	2.727537e-17 F	1.969669e-14 F	1.474667e-19 F	2.261644e-14 F	2.620657e-16 F	3.466598e-15 F

Figure C.2: Capacitance matrix for $d = 30\,\mu\text{m}$

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground	mw	pad1	pad2	read
bus1	5.128089e-15 F	8.870468e-17 F	2.581957e-16 F	3.983170e-17 F	1.739870e-14 F	4.577614e-19 F	5.833884e-14 F	1.304595e-15 F	4.865892e-16 F
bus2	8.870468e-17 F	5.000270e-15 F	3.969790e-17 F	2.120150e-16 F	1.839524e-14 F	4.459849e-19 F	5.789323e-14 F	1.237979e-15 F	4.854798e-16 F
bus3	2.581957e-16 F	3.969790e-17 F	5.166391e-15 F	9.183747e-17 F	1.755019e-14 F	4.931008e-18 F	1.288210e-15 F	5.869753e-14 F	2.777185e-17 F
bus4	3.983170e-17 F	2.120150e-16 F	9.183747e-17 F	5.048199e-15 F	1.859118e-14 F	4.905711e-18 F	1.039363e-15 F	5.835115e-14 F	2.730452e-17 F
ground	1.739870e-14 F	1.839524e-14 F	1.755019e-14 F	1.859118e-14 F	1.439021e-13 F	6.283828e-15 F	4.241729e-14 F	5.013977e-14 F	1.966394e-14 F
mw	4.577614e-19 F	4.459849e-19 F	4.931008e-18 F	4.905711e-18 F	6.283828e-15 F	8.578820e-17 F	3.960701e-18 F	8.882168e-17 F	1.484736e-19 F
pad1	5.833884e-14 F	5.789323e-14 F	1.288210e-15 F	1.039363e-15 F	4.241729e-14 F	3.960701e-18 F	3.131617e-14 F	1.664622e-14 F	2.261978e-14 F
pad2	1.304595e-15 F	1.237979e-15 F	5.869753e-14 F	5.835115e-14 F	5.013977e-14 F	8.882168e-17 F	1.664622e-14 F	3.348223e-14 F	2.611510e-16 F
read	4.865892e-16 F	4.854798e-16 F	2.777185e-17 F	2.730452e-17 F	1.966394e-14 F	1.484736e-19 F	2.261978e-14 F	2.611510e-16 F	3.467976e-15 F

Figure C.3: Capacitance matrix for $d = 40\,\mu\text{m}$

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
mw	pad1	pad2	read		
bus1	5.154562e-15 F	8.911131e-17 F	2.644097e-16 F	4.014359e-17 F	1.754498e-14 F
	4.557183e-19 F	5.915635e-14 F	1.296002e-15 F	4.892801e-16 F	
bus2	8.911131e-17 F	5.002732e-15 F	3.996209e-17 F	2.122193e-16 F	1.849776e-14 F
	4.397646e-19 F	5.858244e-14 F	1.239156e-15 F	4.866828e-16 F	
bus3	2.644097e-16 F	3.996209e-17 F	5.186550e-15 F	9.210293e-17 F	1.769518e-14 F
	4.862060e-18 F	1.279163e-15 F	5.930581e-14 F	2.808324e-17 F	
bus4	4.014359e-17 F	2.122193e-16 F	9.210293e-17 F	5.053414e-15 F	1.870806e-14 F
	4.832770e-18 F	1.038739e-15 F	5.897103e-14 F	2.736127e-17 F	
ground	1.754498e-14 F	1.849776e-14 F	1.769518e-14 F	1.870806e-14 F	1.440384e-13 F
	6.695734e-15 F	4.235107e-14 F	5.015698e-14 F	1.989563e-14 F	
mw	4.557183e-19 F	4.397646e-19 F	4.862060e-18 F	4.832770e-18 F	6.695734e-15 F
	8.488554e-17 F	3.887110e-18 F	8.743624e-17 F	1.468145e-19 F	
pad1	5.915635e-14 F	5.858244e-14 F	1.279163e-15 F	1.038739e-15 F	4.235107e-14 F
	3.887110e-18 F	3.123245e-14 F	1.579213e-14 F	2.284074e-14 F	
pad2	1.296002e-15 F	1.239156e-15 F	5.930581e-14 F	5.897103e-14 F	5.015698e-14 F
	8.743624e-17 F	1.579213e-14 F	3.341443e-14 F	2.607498e-16 F	
read	4.892801e-16 F	4.866828e-16 F	2.808324e-17 F	2.736127e-17 F	1.989563e-14 F
	1.468145e-19 F	2.284074e-14 F	2.607498e-16 F	3.475410e-15 F	

Figure C.4: Capacitance matrix for $d = 50\,\mu\text{m}$

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
mw	pad1	pad2	read		
bus1	5.179609e-15 F	8.963660e-17 F	2.721620e-16 F	4.059604e-17 F	1.762028e-14 F
	4.665351e-19 F	5.921861e-14 F	1.285425e-15 F	4.909829e-16 F	
bus2	8.963660e-17 F	5.015339e-15 F	4.040435e-17 F	2.131142e-16 F	1.856393e-14 F
	4.464077e-19 F	5.869474e-14 F	1.240049e-15 F	4.883971e-16 F	
bus3	2.721620e-16 F	4.040435e-17 F	5.212073e-15 F	9.275665e-17 F	1.776996e-14 F
	4.936614e-18 F	1.268706e-15 F	5.946002e-14 F	2.846237e-17 F	
bus4	4.059604e-17 F	2.131142e-16 F	9.275665e-17 F	5.065581e-15 F	1.878212e-14 F
	4.914185e-18 F	1.039226e-15 F	5.929117e-14 F	2.747160e-17 F	
ground	1.762028e-14 F	1.856393e-14 F	1.776996e-14 F	1.878212e-14 F	1.441379e-13 F
	6.958844e-15 F	4.220607e-14 F	5.003355e-14 F	1.999164e-14 F	
mw	4.665351e-19 F	4.464077e-19 F	4.936614e-18 F	4.914185e-18 F	6.958844e-15 F
	8.568623e-17 F	3.916645e-18 F	8.884551e-17 F	1.489840e-19 F	
pad1	5.921861e-14 F	5.869474e-14 F	1.268706e-15 F	1.039226e-15 F	4.220607e-14 F
	3.916645e-18 F	3.112948e-14 F	1.503486e-14 F	2.292417e-14 F	
pad2	1.285425e-15 F	1.240049e-15 F	5.946002e-14 F	5.929117e-14 F	5.003355e-14 F
	8.884551e-17 F	1.503486e-14 F	3.331134e-14 F	2.598372e-16 F	
read	4.909829e-16 F	4.883971e-16 F	2.846237e-17 F	2.747160e-17 F	1.999164e-14 F
	1.489840e-19 F	2.292417e-14 F	2.598372e-16 F	3.481181e-15 F	

Figure C.5: Capacitance matrix for $d = 60\,\mu\text{m}$

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground	mw	pad1	pad2	read
bus1	5.195953e-15 F	8.984764e-17 F	2.801392e-16 F	4.089817e-17 F	1.760246e-14 F	4.750798e-19 F	5.884592e-14 F	1.272122e-15 F	4.889794e-16 F
bus2	8.984764e-17 F	5.010477e-15 F	4.074117e-17 F	2.124876e-16 F	1.851890e-14 F	4.492399e-19 F	5.858049e-14 F	1.237150e-15 F	4.866389e-16 F
bus3	2.801392e-16 F	4.074117e-17 F	5.234829e-15 F	9.302566e-17 F	1.773910e-14 F	4.973888e-18 F	1.254401e-15 F	5.923032e-14 F	2.876538e-17 F
bus4	4.089817e-17 F	2.124876e-16 F	9.302566e-17 F	5.060690e-15 F	1.874236e-14 F	4.938380e-18 F	1.036065e-15 F	5.914576e-14 F	2.740021e-17 F
ground	1.760246e-14 F	1.851890e-14 F	1.773910e-14 F	1.874236e-14 F	1.441645e-13 F	6.553125e-15 F	4.206523e-14 F	4.987001e-14 F	1.991749e-14 F
mw	4.750798e-19 F	4.492399e-19 F	4.973888e-18 F	4.938380e-18 F	6.553125e-15 F	8.639283e-17 F	3.921151e-18 F	8.928778e-17 F	1.500308e-19 F
pad1	5.884592e-14 F	5.858049e-14 F	1.254401e-15 F	1.036065e-15 F	4.206523e-14 F	3.921151e-18 F	3.103027e-14 F	1.436272e-14 F	2.281965e-14 F
pad2	1.272122e-15 F	1.237150e-15 F	5.923032e-14 F	5.914576e-14 F	4.987001e-14 F	8.928778e-17 F	1.436272e-14 F	3.322052e-14 F	2.580005e-16 F
read	4.889794e-16 F	4.866389e-16 F	2.876538e-17 F	2.740021e-17 F	1.991749e-14 F	1.500308e-19 F	2.281965e-14 F	2.580005e-16 F	3.474113e-15 F

Figure C.6: Capacitance matrix for $d = 70\,\mu m$

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus	4	ground	mw	pad1	pad2	read
bus1	5.228378e-15 F	9.039408e-17 F	2.906121e-16 F	4.1373	57e-17 F	1.766567e-14 F	4.781672e-19 F	5.882227e-14 F	1.260599e-15 F	4.901806e-16 F
bus2	9.039408e-17 F	5.011703e-15 F	4.120374e-17 F	2.1264	41e-16 F	1.854597e-14 F	4.458653e-19 F	5.866835e-14 F	1.235091e-15 F	4.877537e-16 F
bus3	2.906121e-16 F	4.120374e-17 F	5.264367e-15 F	9.3397	13e-17 F	1.781920e-14 F	4.938475e-18 F	1.242057e-15 F	5.929970e-14 F	2.924462e-17 F
bus4	4.137357e-17 F	2.126441e-16 F	9.339713e-17 F	5.0599	83e-15 F	1.871822e-14 F	4.893875e-18 F	1.034511e-15 F	5.905417e-14 F	2.746253e-17 F
ground	1.766567e-14 F	1.854597e-14 F	1.781920e-14 F	1.8718	22e-14 F	1.442963e-13 F	6.779024e-15 F	4.189714e-14 F	4.971782e-14 F	1.993769e-14 F
mw	4.781672e-19 F	4.458653e-19 F	4.938475e-18 F	4.8938	75e-18 F	6.779024e-15 F	8.558446e-17 F	3.863947e-18 F	8.865623e-17 F	1.493070e-19 F
pad1	5.882227e-14 F	5.866835e-14 F	1.242057e-15 F	1.0345	11e-15 F	4.189714e-14 F	3.863947e-18 F	3.089940e-14 F	1.377984e-14 F	2.283645e-14 F
pad2	1.260599e-15 F	1.235091e-15 F	5.929970e-14 F	5.9054	17e-14 F	4.971782e-14 F	8.865623e-17 F	1.377984e-14 F	3.310186e-14 F	2.568706e-16 F
read	4.901806e-16 F	4.877537e-16 F	2.924462e-17 F	2.7462	53e-17 F	1.993769e-14 F	1.493070e-19 F	2.283645e-14 F	2.568706e-16 F	3.480242e-15 F

Figure C.7: Capacitance matrix for $d = 80\,\mu m$

Capacitance matrix for different inner radius r_{inner} in 5.2.2.2

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
mw	pad1	pad2	read		
bus1	4.779320e-15 F	5.729369e-17 F	2.742251e-16 F	2.138829e-17 F	1.745929e-14 F
	3.449507e-19 F	5.974033e-14 F	1.301685e-15 F	4.652250e-16 F	
bus2	5.729369e-17 F	4.517022e-15 F	2.129561e-17 F	1.742185e-16 F	1.823005e-14 F
	3.063895e-19 F	5.967364e-14 F	1.267072e-15 F	4.617569e-16 F	
bus3	2.742251e-16 F	2.129561e-17 F	4.811174e-15 F	5.971984e-17 F	1.760670e-14 F
	4.583798e-18 F	1.288127e-15 F	5.999498e-14 F	1.986700e-17 F	
bus4	2.138829e-17 F	1.742185e-16 F	5.971984e-17 F	4.560026e-15 F	1.839480e-14 F
	4.537301e-18 F	1.080613e-15 F	6.011265e-14 F	1.769851e-17 F	
ground	1.745929e-14 F	1.823005e-14 F	1.760670e-14 F	1.839480e-14 F	1.408910e-13 F
	6.888767e-15 F	4.518019e-14 F	5.304703e-14 F	1.983996e-14 F	
mw	3.449507e-19 F	3.063895e-19 F	4.583798e-18 F	4.537301e-18 F	6.888767e-15 F
	8.243650e-17 F	4.024503e-18 F	9.332994e-17 F	9.984520e-20 F	
pad1	5.974033e-14 F	5.967364e-14 F	1.288127e-15 F	1.080613e-15 F	4.518019e-14 F
	4.024503e-18 F	3.640748e-14 F	2.341642e-14 F	2.328499e-14 F	
pad2	1.301685e-15 F	1.267072e-15 F	5.999498e-14 F	6.011265e-14 F	5.304703e-14 F
	9.332994e-17 F	2.341642e-14 F	3.849856e-14 F	2.518869e-16 F	
read	4.652250e-16 F	4.617569e-16 F	1.986700e-17 F	1.769851e-17 F	1.983996e-14 F
	9.984520e-20 F	2.328499e-14 F	2.518869e-16 F	3.282735e-15 F	

Figure C.8: Capacitance matrix for r_{inner} = 100 µm

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
mw	pad1	pad2	read		
bus1	4.816535e-15 F	5.941693e-17 F	2.762344e-16 F	2.300715e-17 F	1.745913e-14 F
	3.563789e-19 F	5.957990e-14 F	1.292160e-15 F	4.651182e-16 F	
bus2	5.941693e-17 F	4.552204e-15 F	2.290798e-17 F	1.762890e-16 F	1.823230e-14 F
	3.171528e-19 F	5.958501e-14 F	1.260285e-15 F	4.623188e-16 F	
bus3	2.762344e-16 F	2.290798e-17 F	4.847554e-15 F	6.192485e-17 F	1.758923e-14 F
	4.587630e-18 F	1.280145e-15 F	5.987424e-14 F	2.061971e-17 F	
bus4	2.300715e-17 F	1.762890e-16 F	6.192485e-17 F	4.594865e-15 F	1.840818e-14 F
	4.540742e-18 F	1.074561e-15 F	5.993564e-14 F	1.841555e-17 F	
ground	1.745913e-14 F	1.823230e-14 F	1.758923e-14 F	1.840818e-14 F	1.412351e-13 F
	6.797069e-15 F	4.488976e-14 F	5.271323e-14 F	1.980094e-14 F	
mw	3.563789e-19 F	3.171528e-19 F	4.587630e-18 F	4.540742e-18 F	6.797069e-15 F
	8.283404e-17 F	4.015259e-18 F	9.226012e-17 F	1.042000e-19 F	
pad1	5.957990e-14 F	5.958501e-14 F	1.280145e-15 F	1.074561e-15 F	4.488976e-14 F
	4.015259e-18 F	3.585421e-14 F	2.160080e-14 F	2.324058e-14 F	
pad2	1.292160e-15 F	1.260285e-15 F	5.987424e-14 F	5.993564e-14 F	5.271323e-14 F
	9.226012e-17 F	2.160080e-14 F	3.790196e-14 F	2.520802e-16 F	
read	4.651182e-16 F	4.623188e-16 F	2.061971e-17 F	1.841555e-17 F	1.980094e-14 F
	1.042000e-19 F	2.324058e-14 F	2.520802e-16 F	3.293160e-15 F	

Figure C.9: Capacitance matrix for r_{inner} = 120 µm

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
mw	pad1	pad2	read		
bus1	4.875511e-15 F	6.282290e-17 F	2.803306e-16 F	2.529341e-17 F	1.753933e-14 F
	3.666574e-19 F	5.985829e-14 F	1.284314e-15 F	4.683031e-16 F	
bus2	6.282290e-17 F	4.611306e-15 F	2.523417e-17 F	1.796445e-16 F	1.833487e-14 F
	3.272188e-19 F	5.972623e-14 F	1.255994e-15 F	4.651945e-16 F	
bus3	2.803306e-16 F	2.523417e-17 F	4.914434e-15 F	6.539288e-17 F	1.774425e-14 F
	4.552535e-18 F	1.271660e-15 F	6.021146e-14 F	2.181351e-17 F	
bus4	2.529341e-17 F	1.796445e-16 F	6.539288e-17 F	4.650585e-15 F	1.849501e-14 F
	4.493376e-18 F	1.066055e-15 F	6.010028e-14 F	1.950223e-17 F	
ground	1.753933e-14 F	1.833487e-14 F	1.774425e-14 F	1.849501e-14 F	1.417341e-13 F
	6.990220e-15 F	4.445837e-14 F	5.237030e-14 F	1.989286e-14 F	
mw	3.666574e-19 F	3.272188e-19 F	4.552535e-18 F	4.493376e-18 F	6.990220e-15 F
	8.180345e-17 F	3.928109e-18 F	9.032394e-17 F	1.085850e-19 F	
pad1	5.985829e-14 F	5.972623e-14 F	1.271660e-15 F	1.066055e-15 F	4.445837e-14 F
	3.928109e-18 F	3.507190e-14 F	1.978642e-14 F	2.329773e-14 F	
pad2	1.284314e-15 F	1.255994e-15 F	6.021146e-14 F	6.010028e-14 F	5.237030e-14 F
	9.032394e-17 F	1.978642e-14 F	3.716128e-14 F	2.537331e-16 F	
read	4.683031e-16 F	4.651945e-16 F	2.181351e-17 F	1.950223e-17 F	1.989286e-14 F
	1.085850e-19 F	2.329773e-14 F	2.537331e-16 F	3.320063e-15 F	

Figure C.10: Capacitance matrix for r_{inner} = 140 µm

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
mw	pad1	pad2	read		
bus1	4.958246e-15 F	6.819433e-17 F	2.861792e-16 F	2.883850e-17 F	1.751162e-14 F
	3.944279e-19 F	5.932286e-14 F	1.269378e-15 F	4.705553e-16 F	
bus2	6.819433e-17 F	4.691639e-15 F	2.872117e-17 F	1.851521e-16 F	1.829257e-14 F
	3.527889e-19 F	5.931440e-14 F	1.243735e-15 F	4.680424e-16 F	
bus3	2.861792e-16 F	2.872117e-17 F	4.990364e-15 F	7.070276e-17 F	1.767329e-14 F
	4.626765e-18 F	1.253169e-15 F	5.948560e-14 F	2.355555e-17 F	
bus4	2.883850e-17 F	1.851521e-16 F	7.070276e-17 F	4.731309e-15 F	1.849000e-14 F
	4.570129e-18 F	1.054951e-15 F	5.968334e-14 F	2.116546e-17 F	
ground	1.751162e-14 F	1.829257e-14 F	1.767329e-14 F	1.849000e-14 F	1.423622e-13 F
	6.444239e-15 F	4.378102e-14 F	5.161644e-14 F	1.979808e-14 F	
mw	3.944279e-19 F	3.527889e-19 F	4.626765e-18 F	4.570129e-18 F	6.444239e-15 F
	8.255141e-17 F	3.919040e-18 F	9.011553e-17 F	1.181740e-19 F	
pad1	5.932286e-14 F	5.931440e-14 F	1.253169e-15 F	1.054951e-15 F	4.378102e-14 F
	3.919040e-18 F	3.398030e-14 F	1.747468e-14 F	2.308573e-14 F	
pad2	1.269378e-15 F	1.243735e-15 F	5.948560e-14 F	5.968334e-14 F	5.161644e-14 F
	9.011553e-17 F	1.747468e-14 F	3.609154e-14 F	2.541367e-16 F	
read	4.705553e-16 F	4.680424e-16 F	2.355555e-17 F	2.116546e-17 F	1.979808e-14 F
	1.181740e-19 F	2.308573e-14 F	2.541367e-16 F	3.353278e-15 F	

Figure C.11: Capacitance matrix for r_{inner} = 160 µm

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
mw	pad1	pad2	read		
bus1	5.099395e-15 F	7.688861e-17 F	2.987483e-16 F	3.412600e-17 F	1.764644e-14 F
	4.341790e-19 F	5.908769e-14 F	1.256530e-15 F	4.791955e-16 F	
bus2	7.688861e-17 F	4.817141e-15 F	3.398524e-17 F	1.949759e-16 F	1.842204e-14 F
	3.890975e-19 F	5.913244e-14 F	1.237912e-15 F	4.751875e-16 F	
bus3	2.987483e-16 F	3.398524e-17 F	5.129703e-15 F	7.959547e-17 F	1.779363e-14 F
	4.741536e-18 F	1.238136e-15 F	5.941121e-14 F	2.626689e-17 F	
bus4	3.412600e-17 F	1.949759e-16 F	7.959547e-17 F	4.860061e-15 F	1.860071e-14 F
	4.686464e-18 F	1.042332e-15 F	5.954889e-14 F	2.364735e-17 F	
ground	1.764644e-14 F	1.842204e-14 F	1.779363e-14 F	1.860071e-14 F	1.433378e-13 F
	6.570212e-15 F	4.284470e-14 F	5.069223e-14 F	1.989173e-14 F	
mw	4.341790e-19 F	3.890975e-19 F	4.741536e-18 F	4.686464e-18 F	6.570212e-15 F
	8.366171e-17 F	3.876404e-18 F	8.923037e-17 F	1.312084e-19 F	
pad1	5.908769e-14 F	5.913244e-14 F	1.238136e-15 F	1.042332e-15 F	4.284470e-14 F
	3.876404e-18 F	3.253405e-14 F	1.522390e-14 F	2.303466e-14 F	
pad2	1.256530e-15 F	1.237912e-15 F	5.941121e-14 F	5.954889e-14 F	5.069223e-14 F
	8.923037e-17 F	1.522390e-14 F	3.468534e-14 F	2.548215e-16 F	
read	4.791955e-16 F	4.751875e-16 F	2.626689e-17 F	2.364735e-17 F	1.989173e-14 F
	1.312084e-19 F	2.303466e-14 F	2.548215e-16 F	3.408101e-15 F	

Figure C.12: Capacitance matrix for r_{inner} = 180 µm

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
mw	pad1	pad2	read		
bus1	5.306216e-15 F	9.157474e-17 F	3.188734e-16 F	4.246400e-17 F	1.778917e-14 F
	5.026938e-19 F	5.866362e-14 F	1.239450e-15 F	4.913423e-16 F	
bus2	9.157474e-17 F	5.013936e-15 F	4.229233e-17 F	2.120456e-16 F	1.854898e-14 F
	4.524515e-19 F	5.867051e-14 F	1.232097e-15 F	4.871677e-16 F	
bus3	3.188734e-16 F	4.229233e-17 F	5.342005e-15 F	9.460437e-17 F	1.796527e-14 F
	5.023997e-18 F	1.219270e-15 F	5.899990e-14 F	3.028157e-17 F	
bus4	4.246400e-17 F	2.120456e-16 F	9.460437e-17 F	5.060304e-15 F	1.872640e-14 F
	4.959930e-18 F	1.031078e-15 F	5.909923e-14 F	2.739642e-17 F	
ground	1.778917e-14 F	1.854898e-14 F	1.796527e-14 F	1.872640e-14 F	1.445075e-13 F
	6.740818e-15 F	4.151736e-14 F	4.933631e-14 F	1.995816e-14 F	
mw	5.026938e-19 F	4.524515e-19 F	5.023997e-18 F	4.959930e-18 F	6.740818e-15 F
	8.728258e-17 F	3.868560e-18 F	8.932059e-17 F	1.519582e-19 F	
pad1	5.866362e-14 F	5.867051e-14 F	1.219270e-15 F	1.031078e-15 F	4.151736e-14 F
	3.868560e-18 F	3.064604e-14 F	1.286678e-14 F	2.284125e-14 F	
pad2	1.239450e-15 F	1.232097e-15 F	5.899990e-14 F	5.909923e-14 F	4.933631e-14 F
	8.932059e-17 F	1.286678e-14 F	3.283365e-14 F	2.531821e-16 F	
read	4.913423e-16 F	4.871677e-16 F	3.028157e-17 F	2.739642e-17 F	1.995816e-14 F
	1.519582e-19 F	2.284125e-14 F	2.531821e-16 F	3.475555e-15 F	

Figure C.13: Capacitance matrix for r_{inner} = 200 µm

Capacitance matrix for different bus arm length l in 5.2.2.3

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
mw	pad1	pad2	read		
bus1	4.300638e-15 F	7.264377e-17 F	2.959289e-16 F	3.636422e-17 F	1.455068e-14 F
	4.413041e-19 F	5.048385e-14 F	1.125214e-15 F	2.976859e-16 F	
bus2	7.264377e-17 F	5.009432e-15 F	4.237523e-17 F	2.123013e-16 F	1.851123e-14 F
	4.514099e-19 F	5.841762e-14 F	1.229112e-15 F	4.864722e-16 F	
bus3	2.959289e-16 F	4.237523e-17 F	5.338664e-15 F	9.464078e-17 F	1.790067e-14 F
	5.008759e-18 F	1.230392e-15 F	5.883682e-14 F	3.066002e-17 F	
bus4	3.636422e-17 F	2.123013e-16 F	9.464078e-17 F	5.061848e-15 F	1.871817e-14 F
	4.948837e-18 F	1.033140e-15 F	5.900552e-14 F	2.756698e-17 F	
ground	1.455068e-14 F	1.851123e-14 F	1.790067e-14 F	1.871817e-14 F	1.447980e-13 F
	6.545839e-15 F	4.353051e-14 F	4.933299e-14 F	2.000980e-14 F	
mw	4.413041e-19 F	4.514099e-19 F	5.008759e-18 F	4.948837e-18 F	6.545839e-15 F
	8.668822e-17 F	3.888616e-18 F	8.940177e-17 F	1.525517e-19 F	
pad1	5.048385e-14 F	5.841762e-14 F	1.230392e-15 F	1.033140e-15 F	4.353051e-14 F
	3.888616e-18 F	3.124445e-14 F	1.281373e-14 F	2.294655e-14 F	
pad2	1.125214e-15 F	1.229112e-15 F	5.883682e-14 F	5.900552e-14 F	4.933299e-14 F
	8.940177e-17 F	1.281373e-14 F	3.280785e-14 F	2.543983e-16 F	
read	2.976859e-16 F	4.864722e-16 F	3.066002e-17 F	2.756698e-17 F	2.000980e-14 F
	1.525517e-19 F	2.294655e-14 F	2.543983e-16 F	3.493568e-15 F	

Figure C.14: Capacitance matrix for $l = 38.67\,\mu m$

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
mw	pad1	pad2	read		
bus1	4.343177e-15 F	7.326785e-17 F	2.969740e-16 F	3.663840e-17 F	1.466382e-14 F
	4.368453e-19 F	5.075478e-14 F	1.131848e-15 F	3.009442e-16 F	
bus2	7.326785e-17 F	5.008084e-15 F	4.232662e-17 F	2.123045e-16 F	1.850500e-14 F
	4.436244e-19 F	5.840092e-14 F	1.229042e-15 F	4.867159e-16 F	
bus3	2.969740e-16 F	4.232662e-17 F	5.336525e-15 F	9.457837e-17 F	1.790387e-14 F
	4.925028e-18 F	1.227969e-15 F	5.892739e-14 F	3.063913e-17 F	
bus4	3.663840e-17 F	2.123045e-16 F	9.457837e-17 F	5.062716e-15 F	1.872787e-14 F
	4.860162e-18 F	1.033446e-15 F	5.904316e-14 F	2.757528e-17 F	
ground	1.466382e-14 F	1.850500e-14 F	1.790387e-14 F	1.872787e-14 F	1.447957e-13 F
	6.456797e-15 F	4.342631e-14 F	4.935221e-14 F	1.996940e-14 F	
mw	4.368453e-19 F	4.436244e-19 F	4.925028e-18 F	4.860162e-18 F	6.456797e-15 F
	8.529764e-17 F	3.820790e-18 F	8.759255e-17 F	1.500130e-19 F	
pad1	5.075478e-14 F	5.840092e-14 F	1.227969e-15 F	1.033446e-15 F	4.342631e-14 F
	3.820790e-18 F	3.121974e-14 F	1.281548e-14 F	2.293477e-14 F	
pad2	1.131848e-15 F	1.229042e-15 F	5.892739e-14 F	5.904316e-14 F	4.935221e-14 F
	8.759255e-17 F	1.281548e-14 F	3.280323e-14 F	2.544918e-16 F	
read	3.009442e-16 F	4.867159e-16 F	3.063913e-17 F	2.757528e-17 F	1.996940e-14 F
	1.500130e-19 F	2.293477e-14 F	2.544918e-16 F	3.493960e-15 F	

Figure C.15: Capacitance matrix for $l = 43.76\,\mu m$

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
mw	pad1	pad2	read		
bus1	4.390025e-15 F	7.406166e-17 F	2.987151e-16 F	3.692627e-17 F	1.482342e-14 F
	4.459625e-19 F	5.133299e-14 F	1.137523e-15 F	3.043387e-16 F	
bus2	7.406166e-17 F	5.012432e-15 F	4.239948e-17 F	2.124481e-16 F	1.852066e-14 F
	4.501920e-19 F	5.846310e-14 F	1.230024e-15 F	4.869824e-16 F	
bus3	2.987151e-16 F	4.239948e-17 F	5.338699e-15 F	9.460063e-17 F	1.793001e-14 F
	4.981734e-18 F	1.228634e-15 F	5.881808e-14 F	3.063862e-17 F	
bus4	3.692627e-17 F	2.124481e-16 F	9.460063e-17 F	5.061671e-15 F	1.872017e-14 F
	4.928898e-18 F	1.032865e-15 F	5.893228e-14 F	2.755704e-17 F	
ground	1.482342e-14 F	1.852066e-14 F	1.793001e-14 F	1.872017e-14 F	1.447658e-13 F
	6.854957e-15 F	4.334536e-14 F	4.933843e-14 F	2.004681e-14 F	
mw	4.459625e-19 F	4.501920e-19 F	4.981734e-18 F	4.928898e-18 F	6.854957e-15 F
	8.657503e-17 F	3.870981e-18 F	8.888470e-17 F	1.520227e-19 F	
pad1	5.133299e-14 F	5.846310e-14 F	1.228634e-15 F	1.032865e-15 F	4.334536e-14 F
	3.870981e-18 F	3.119377e-14 F	1.280940e-14 F	2.293356e-14 F	
pad2	1.137523e-15 F	1.230024e-15 F	5.881808e-14 F	5.893228e-14 F	4.933843e-14 F
	8.888470e-17 F	1.280940e-14 F	3.280214e-14 F	2.542499e-16 F	
read	3.043387e-16 F	4.869824e-16 F	3.063862e-17 F	2.755704e-17 F	2.004681e-14 F
	1.520227e-19 F	2.293356e-14 F	2.542499e-16 F	3.493107e-15 F	

Figure C.16: Capacitance matrix for $l = 48.83\,\mu m$

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
mw	pad1	pad2	read		
bus1	4.424353e-15 F	7.462218e-17 F	2.996374e-16 F	3.716194e-17 F	1.493908e-14 F
	4.439727e-19 F	5.163435e-14 F	1.141954e-15 F	3.070607e-16 F	
bus2	7.462218e-17 F	5.013890e-15 F	4.241354e-17 F	2.125175e-16 F	1.853459e-14 F
	4.458822e-19 F	5.849730e-14 F	1.230305e-15 F	4.870172e-16 F	
bus3	2.996374e-16 F	4.241354e-17 F	5.338449e-15 F	9.469505e-17 F	1.790343e-14 F
	4.945905e-18 F	1.227935e-15 F	5.895622e-14 F	3.062616e-17 F	
bus4	3.716194e-17 F	2.125175e-16 F	9.469505e-17 F	5.065204e-15 F	1.872391e-14 F
	4.893696e-18 F	1.032835e-15 F	5.909679e-14 F	2.756694e-17 F	
ground	1.493908e-14 F	1.853459e-14 F	1.790343e-14 F	1.872391e-14 F	1.447561e-13 F
	6.682598e-15 F	4.327420e-14 F	4.933574e-14 F	2.000894e-14 F	
mw	4.439727e-19 F	4.458822e-19 F	4.945905e-18 F	4.893696e-18 F	6.682598e-15 F
	8.546900e-17 F	3.832476e-18 F	8.847038e-17 F	1.504452e-19 F	
pad1	5.163435e-14 F	5.849730e-14 F	1.227935e-15 F	1.032835e-15 F	4.327420e-14 F
	3.832476e-18 F	3.116425e-14 F	1.280908e-14 F	2.292873e-14 F	
pad2	1.141954e-15 F	1.230305e-15 F	5.895622e-14 F	5.909679e-14 F	4.933574e-14 F
	8.847038e-17 F	1.280908e-14 F	3.281677e-14 F	2.542904e-16 F	
read	3.070607e-16 F	4.870172e-16 F	3.062616e-17 F	2.756694e-17 F	2.000894e-14 F
	1.504452e-19 F	2.292873e-14 F	2.542904e-16 F	3.492543e-15 F	

Figure C.17: Capacitance matrix for $l = 53.88\,\mu m$

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
	mw	pad1	pad2	read	
bus1	4.473211e-15 F	7.535782e-17 F	3.011647e-16 F	3.745131e-17 F	1.510901e-14 F
	4.445348e-19 F	5.195713e-14 F	1.147823e-15 F	3.115126e-16 F	
bus2	7.535782e-17 F	5.012738e-15 F	4.240743e-17 F	2.124519e-16 F	1.853036e-14 F
	4.432532e-19 F	5.848113e-14 F	1.229572e-15 F	4.872523e-16 F	
bus3	3.011647e-16 F	4.240743e-17 F	5.342214e-15 F	9.468208e-17 F	1.793373e-14 F
	4.918736e-18 F	1.227525e-15 F	5.895508e-14 F	3.063627e-17 F	
bus4	3.745131e-17 F	2.124519e-16 F	9.468208e-17 F	5.063948e-15 F	1.873715e-14 F
	4.860945e-18 F	1.032831e-15 F	5.897248e-14 F	2.757311e-17 F	
ground	1.510901e-14 F	1.853036e-14 F	1.793373e-14 F	1.873715e-14 F	1.447533e-13 F
	6.403297e-15 F	4.318062e-14 F	4.932646e-14 F	2.000901e-14 F	
mw	4.445348e-19 F	4.432532e-19 F	4.918736e-18 F	4.860945e-18 F	6.403297e-15 F
	8.498051e-17 F	3.809612e-18 F	8.782434e-17 F	1.496083e-19 F	
pad1	5.195713e-14 F	5.848113e-14 F	1.227525e-15 F	1.032831e-15 F	4.318062e-14 F
	3.809612e-18 F	3.113671e-14 F	1.280630e-14 F	2.293193e-14 F	
pad2	1.147823e-15 F	1.229572e-15 F	5.895508e-14 F	5.897248e-14 F	4.932646e-14 F
	8.782434e-17 F	1.280630e-14 F	3.280394e-14 F	2.542639e-16 F	
read	3.115126e-16 F	4.872523e-16 F	3.063627e-17 F	2.757311e-17 F	2.000901e-14 F
	1.496083e-19 F	2.293193e-14 F	2.542639e-16 F	3.492864e-15 F	

Figure C.18: Capacitance matrix for $l = 58.92\,\mu m$

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
	mw	pad1	pad2	read	
bus1	4.517165e-15 F	7.605397e-17 F	3.024458e-16 F	3.774666e-17 F	1.523996e-14 F
	4.511731e-19 F	5.232305e-14 F	1.153859e-15 F	3.153406e-16 F	
bus2	7.605397e-17 F	5.010703e-15 F	4.241427e-17 F	2.124705e-16 F	1.853409e-14 F
	4.467560e-19 F	5.838183e-14 F	1.229389e-15 F	4.872752e-16 F	
bus3	3.024458e-16 F	4.241427e-17 F	5.342504e-15 F	9.478883e-17 F	1.791589e-14 F
	4.961233e-18 F	1.226697e-15 F	5.899954e-14 F	3.063425e-17 F	
bus4	3.774666e-17 F	2.124705e-16 F	9.478883e-17 F	5.065020e-15 F	1.874248e-14 F
	4.903624e-18 F	1.032796e-15 F	5.909035e-14 F	2.758295e-17 F	
ground	1.523996e-14 F	1.853409e-14 F	1.791589e-14 F	1.874248e-14 F	1.447401e-13 F
	6.664020e-15 F	4.309898e-14 F	4.931681e-14 F	2.000196e-14 F	
mw	4.511731e-19 F	4.467560e-19 F	4.961233e-18 F	4.903624e-18 F	6.664020e-15 F
	8.572315e-17 F	3.838107e-18 F	8.842004e-17 F	1.508314e-19 F	
pad1	5.232305e-14 F	5.838183e-14 F	1.226697e-15 F	1.032796e-15 F	4.309898e-14 F
	3.838107e-18 F	3.110572e-14 F	1.280233e-14 F	2.293498e-14 F	
pad2	1.153859e-15 F	1.229389e-15 F	5.899954e-14 F	5.909035e-14 F	4.931681e-14 F
	8.842004e-17 F	1.280233e-14 F	3.280239e-14 F	2.542751e-16 F	
read	3.153406e-16 F	4.872752e-16 F	3.063425e-17 F	2.758295e-17 F	2.000196e-14 F
	1.508314e-19 F	2.293498e-14 F	2.542751e-16 F	3.492433e-15 F	

Figure C.19: Capacitance matrix for $l = 63.94\,\mu m$

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
mw	pad1	pad2	read		
bus1	4.555793e-15 F	7.659899e-17 F	3.030667e-16 F	3.796754e-17 F	1.536799e-14 F
	4.423129e-19 F	5.264093e-14 F	1.158168e-15 F	3.193807e-16 F	
bus2	7.659899e-17 F	5.008139e-15 F	4.231143e-17 F	2.122672e-16 F	1.852483e-14 F
	4.357114e-19 F	5.843283e-14 F	1.228991e-15 F	4.865617e-16 F	
bus3	3.030667e-16 F	4.231143e-17 F	5.333022e-15 F	9.455483e-17 F	1.790490e-14 F
	4.817108e-18 F	1.224808e-15 F	5.887321e-14 F	3.058432e-17 F	
bus4	3.796754e-17 F	2.122672e-16 F	9.455483e-17 F	5.063740e-15 F	1.874654e-14 F
	4.787114e-18 F	1.032512e-15 F	5.899661e-14 F	2.756839e-17 F	
ground	1.536799e-14 F	1.852483e-14 F	1.790490e-14 F	1.874654e-14 F	1.447541e-13 F
	6.668853e-15 F	4.303498e-14 F	4.934413e-14 F	2.001043e-14 F	
mw	4.423129e-19 F	4.357114e-19 F	4.817108e-18 F	4.787114e-18 F	6.668853e-15 F
	8.371810e-17 F	3.743071e-18 F	8.610948e-17 F	1.471482e-19 F	
pad1	5.264093e-14 F	5.843283e-14 F	1.224808e-15 F	1.032512e-15 F	4.303498e-14 F
	3.743071e-18 F	3.109083e-14 F	1.280532e-14 F	2.293325e-14 F	
pad2	1.158168e-15 F	1.228991e-15 F	5.887321e-14 F	5.899661e-14 F	4.934413e-14 F
	8.610948e-17 F	1.280532e-14 F	3.280231e-14 F	2.542162e-16 F	
read	3.193807e-16 F	4.865617e-16 F	3.058432e-17 F	2.756839e-17 F	2.001043e-14 F
	1.471482e-19 F	2.293325e-14 F	2.542162e-16 F	3.493738e-15 F	

Figure C.20: Capacitance matrix for $l = 68.95\,\mu m$

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
mw	pad1	pad2	read		
bus1	4.608216e-15 F	7.756784e-17 F	3.052609e-16 F	3.829852e-17 F	1.555167e-14 F
	4.520458e-19 F	5.303829e-14 F	1.164661e-15 F	3.254143e-16 F	
bus2	7.756784e-17 F	5.015103e-15 F	4.244751e-17 F	2.125908e-16 F	1.854052e-14 F
	4.423075e-19 F	5.850859e-14 F	1.230249e-15 F	4.879957e-16 F	
bus3	3.052609e-16 F	4.244751e-17 F	5.348523e-15 F	9.478804e-17 F	1.795830e-14 F
	4.910986e-18 F	1.226577e-15 F	5.895909e-14 F	3.069015e-17 F	
bus4	3.829852e-17 F	2.125908e-16 F	9.478804e-17 F	5.064486e-15 F	1.874401e-14 F
	4.852336e-18 F	1.032546e-15 F	5.906789e-14 F	2.760416e-17 F	
ground	1.555167e-14 F	1.854052e-14 F	1.795830e-14 F	1.874401e-14 F	1.446981e-13 F
	6.827837e-15 F	4.290453e-14 F	4.930439e-14 F	2.005481e-14 F	
mw	4.520458e-19 F	4.423075e-19 F	4.910986e-18 F	4.852336e-18 F	6.827837e-15 F
	8.479468e-17 F	3.794408e-18 F	8.766202e-17 F	1.494233e-19 F	
pad1	5.303829e-14 F	5.850859e-14 F	1.226577e-15 F	1.032546e-15 F	4.290453e-14 F
	3.794408e-18 F	3.105356e-14 F	1.280247e-14 F	2.293149e-14 F	
pad2	1.164661e-15 F	1.230249e-15 F	5.895909e-14 F	5.906789e-14 F	4.930439e-14 F
	8.766202e-17 F	1.280247e-14 F	3.280833e-14 F	2.545272e-16 F	
read	3.254143e-16 F	4.879957e-16 F	3.069015e-17 F	2.760416e-17 F	2.005481e-14 F
	1.494233e-19 F	2.293149e-14 F	2.545272e-16 F	3.498206e-15 F	

Figure C.21: Capacitance matrix for $l = 73.94\,\mu m$

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
mw	pad1	pad2	read		
bus1	4.656413e-15 F	7.840554e-17 F	3.063543e-16 F	3.861872e-17 F	1.569356e-14 F
	4.574937e-19 F	5.346453e-14 F	1.170831e-15 F	3.310450e-16 F	
bus2	7.840554e-17 F	5.013729e-15 F	4.243131e-17 F	2.127256e-16 F	1.854636e-14 F
	4.446302e-19 F	5.851126e-14 F	1.230422e-15 F	4.885526e-16 F	
bus3	3.063543e-16 F	4.243131e-17 F	5.343915e-15 F	9.478062e-17 F	1.795691e-14 F
	4.932837e-18 F	1.225010e-15 F	5.896351e-14 F	3.066842e-17 F	
bus4	3.861872e-17 F	2.127256e-16 F	9.478062e-17 F	5.066691e-15 F	1.875191e-14 F
	4.881098e-18 F	1.032782e-15 F	5.912638e-14 F	2.762961e-17 F	
ground	1.569356e-14 F	1.854636e-14 F	1.795691e-14 F	1.875191e-14 F	1.446969e-13 F
	6.533471e-15 F	4.281273e-14 F	4.933055e-14 F	2.007602e-14 F	
mw	4.574937e-19 F	4.446302e-19 F	4.932837e-18 F	4.881098e-18 F	6.533471e-15 F
	8.518624e-17 F	3.812592e-18 F	8.825014e-17 F	1.502069e-19 F	
pad1	5.346453e-14 F	5.851126e-14 F	1.225010e-15 F	1.032782e-15 F	4.281273e-14 F
	3.812592e-18 F	3.101819e-14 F	1.279440e-14 F	2.294522e-14 F	
pad2	1.170831e-15 F	1.230422e-15 F	5.896351e-14 F	5.912638e-14 F	4.933055e-14 F
	8.825014e-17 F	1.279440e-14 F	3.280617e-14 F	2.545841e-16 F	
read	3.310450e-16 F	4.885526e-16 F	3.066842e-17 F	2.762961e-17 F	2.007602e-14 F
	1.502069e-19 F	2.294522e-14 F	2.545841e-16 F	3.498592e-15 F	

Figure C.22: Capacitance matrix for $l = 78.93\,\mu m$

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
mw	pad1	pad2	read		
bus1	4.690648e-15 F	7.902414e-17 F	3.071268e-16 F	3.884371e-17 F	1.579543e-14 F
	4.622250e-19 F	5.379150e-14 F	1.173803e-15 F	3.353513e-16 F	
bus2	7.902414e-17 F	5.013606e-15 F	4.243140e-17 F	2.126665e-16 F	1.855888e-14 F
	4.472089e-19 F	5.853460e-14 F	1.230097e-15 F	4.882340e-16 F	
bus3	3.071268e-16 F	4.243140e-17 F	5.344344e-15 F	9.484997e-17 F	1.795434e-14 F
	4.958380e-18 F	1.225474e-15 F	5.909248e-14 F	3.064399e-17 F	
bus4	3.884371e-17 F	2.126665e-16 F	9.484997e-17 F	5.069120e-15 F	1.876749e-14 F
	4.908290e-18 F	1.032858e-15 F	5.920469e-14 F	2.761142e-17 F	
ground	1.579543e-14 F	1.855888e-14 F	1.795434e-14 F	1.876749e-14 F	1.447108e-13 F
	6.755238e-15 F	4.273941e-14 F	4.932774e-14 F	2.004932e-14 F	
mw	4.622250e-19 F	4.472089e-19 F	4.958380e-18 F	4.908290e-18 F	6.755238e-15 F
	8.597898e-17 F	3.833493e-18 F	8.840986e-17 F	1.510299e-19 F	
pad1	5.379150e-14 F	5.853460e-14 F	1.225474e-15 F	1.032858e-15 F	4.273941e-14 F
	3.833493e-18 F	3.099756e-14 F	1.279860e-14 F	2.294091e-14 F	
pad2	1.173803e-15 F	1.230097e-15 F	5.909248e-14 F	5.920469e-14 F	4.932774e-14 F
	8.840986e-17 F	1.279860e-14 F	3.279583e-14 F	2.542972e-16 F	
read	3.353513e-16 F	4.882340e-16 F	3.064399e-17 F	2.761142e-17 F	2.004932e-14 F
	1.510299e-19 F	2.294091e-14 F	2.542972e-16 F	3.495007e-15 F	

Figure C.23: Capacitance matrix for $l = 83.90\,\mu m$

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground	mw	pad1	pad2	read
bus1	4.732811e-15 F	7.974068e-17 F	3.075663e-16 F	3.905883e-17 F	1.593799e-14 F	4.614653e-19 F	5.409154e-14 F	1.178134e-15 F	3.404609e-16 F
bus2	7.974068e-17 F	5.011056e-15 F	4.238454e-17 F	2.123650e-16 F	1.852264e-14 F	4.439090e-19 F	5.840940e-14 F	1.229470e-15 F	4.867230e-16 F
bus3	3.075663e-16 F	4.238454e-17 F	5.340387e-15 F	9.468322e-17 F	1.790829e-14 F	4.926628e-18 F	1.223241e-15 F	5.892000e-14 F	3.054166e-17 F
bus4	3.905883e-17 F	2.123650e-16 F	9.468322e-17 F	5.063051e-15 F	1.872499e-14 F	4.870542e-18 F	1.031725e-15 F	5.898092e-14 F	2.752730e-17 F
ground	1.593799e-14 F	1.852264e-14 F	1.790829e-14 F	1.872499e-14 F	1.446639e-13 F	6.475486e-15 F	4.266132e-14 F	4.930921e-14 F	1.996284e-14 F
mw	4.614653e-19 F	4.439090e-19 F	4.926628e-18 F	4.870542e-18 F	6.475486e-15 F	8.509433e-17 F	3.806479e-18 F	8.801602e-17 F	1.495876e-19 F
pad1	5.409154e-14 F	5.840940e-14 F	1.223241e-15 F	1.031725e-15 F	4.266132e-14 F	3.806479e-18 F	3.097502e-14 F	1.278567e-14 F	2.291691e-14 F
pad2	1.178134e-15 F	1.229470e-15 F	5.892000e-14 F	5.898092e-14 F	4.930921e-14 F	8.801602e-17 F	1.278567e-14 F	3.280503e-14 F	2.537474e-16 F
read	3.404609e-16 F	4.867230e-16 F	3.054166e-17 F	2.752730e-17 F	1.996284e-14 F	1.495876e-19 F	2.291691e-14 F	2.537474e-16 F	3.486605e-15 F

Figure C.24: Capacitance matrix for $l = 88.86\,\mu m$

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground	mw	pad1	pad2	read
bus1	4.781464e-15 F	8.061516e-17 F	3.082916e-16 F	3.934485e-17 F	1.609008e-14 F	4.681973e-19 F	5.448740e-14 F	1.183134e-15 F	3.476370e-16 F
bus2	8.061516e-17 F	5.008967e-15 F	4.233098e-17 F	2.121380e-16 F	1.849616e-14 F	4.472516e-19 F	5.830690e-14 F	1.228806e-15 F	4.862844e-16 F
bus3	3.082916e-16 F	4.233098e-17 F	5.333906e-15 F	9.453382e-17 F	1.788941e-14 F	4.962754e-18 F	1.221387e-15 F	5.879337e-14 F	3.050591e-17 F
bus4	3.934485e-17 F	2.121380e-16 F	9.453382e-17 F	5.059483e-15 F	1.870115e-14 F	4.905461e-18 F	1.030825e-15 F	5.899146e-14 F	2.751144e-17 F
ground	1.609008e-14 F	1.849616e-14 F	1.788941e-14 F	1.870115e-14 F	1.446429e-13 F	6.485470e-15 F	4.256399e-14 F	4.932036e-14 F	1.995875e-14 F
mw	4.681973e-19 F	4.472516e-19 F	4.962754e-18 F	4.905461e-18 F	6.485470e-15 F	8.571352e-17 F	3.835679e-18 F	8.886633e-17 F	1.507654e-19 F
pad1	5.448740e-14 F	5.830690e-14 F	1.221387e-15 F	1.030825e-15 F	4.256399e-14 F	3.835679e-18 F	3.094426e-14 F	1.277343e-14 F	2.288556e-14 F
pad2	1.183134e-15 F	1.228806e-15 F	5.879337e-14 F	5.899146e-14 F	4.932036e-14 F	8.886633e-17 F	1.277343e-14 F	3.280647e-14 F	2.536950e-16 F
read	3.476370e-16 F	4.862844e-16 F	3.050591e-17 F	2.751144e-17 F	1.995875e-14 F	1.507654e-19 F	2.288556e-14 F	2.536950e-16 F	3.486701e-15 F

Figure C.25: Capacitance matrix for $l = 93.81\,\mu m$

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
mw	pad1	pad2	read		
bus1	4.828218e-15 F	8.150551e-17 F	3.104061e-16 F	3.965418e-17 F	1.626215e-14 F
	4.665343e-19 F	5.492722e-14 F	1.189884e-15 F	3.550315e-16 F	
bus2	8.150551e-17 F	5.016212e-15 F	4.245665e-17 F	2.126487e-16 F	1.856800e-14 F
	4.435887e-19 F	5.862810e-14 F	1.231325e-15 F	4.882604e-16 F	
bus3	3.104061e-16 F	4.245665e-17 F	5.345138e-15 F	9.479082e-17 F	1.796397e-14 F
	4.924521e-18 F	1.222380e-15 F	5.906100e-14 F	3.062993e-17 F	
bus4	3.965418e-17 F	2.126487e-16 F	9.479082e-17 F	5.064528e-15 F	1.875284e-14 F
	4.869649e-18 F	1.031166e-15 F	5.912146e-14 F	2.759235e-17 F	
ground	1.626215e-14 F	1.856800e-14 F	1.796397e-14 F	1.875284e-14 F	1.446778e-13 F
	6.612474e-15 F	4.246425e-14 F	4.933358e-14 F	2.008517e-14 F	
mw	4.665343e-19 F	4.435887e-19 F	4.924521e-18 F	4.869649e-18 F	6.612474e-15 F
	8.495410e-17 F	3.795040e-18 F	8.786892e-17 F	1.496452e-19 F	
pad1	5.492722e-14 F	5.862810e-14 F	1.222380e-15 F	1.031166e-15 F	4.246425e-14 F
	3.795040e-18 F	3.090556e-14 F	1.279033e-14 F	2.294474e-14 F	
pad2	1.189884e-15 F	1.231325e-15 F	5.906100e-14 F	5.912146e-14 F	4.933358e-14 F
	8.786892e-17 F	1.279033e-14 F	3.280062e-14 F	2.543704e-16 F	
read	3.550315e-16 F	4.882604e-16 F	3.062993e-17 F	2.759235e-17 F	2.008517e-14 F
	1.496452e-19 F	2.294474e-14 F	2.543704e-16 F	3.496153e-15 F	

Figure C.26: Capacitance matrix for $l = 98.76\,\mu\text{m}$

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
mw	pad1	pad2	read		
bus1	4.865497e-15 F	8.218507e-17 F	3.104987e-16 F	3.987953e-17 F	1.636124e-14 F
	4.618862e-19 F	5.511480e-14 F	1.193224e-15 F	3.612854e-16 F	
bus2	8.218507e-17 F	5.010922e-15 F	4.234518e-17 F	2.123861e-16 F	1.851071e-14 F
	4.368797e-19 F	5.842716e-14 F	1.229124e-15 F	4.873797e-16 F	
bus3	3.104987e-16 F	4.234518e-17 F	5.335214e-15 F	9.453268e-17 F	1.790224e-14 F
	4.838578e-18 F	1.220248e-15 F	5.884741e-14 F	3.050805e-17 F	
bus4	3.987953e-17 F	2.123861e-16 F	9.453268e-17 F	5.062139e-15 F	1.872549e-14 F
	4.793744e-18 F	1.031340e-15 F	5.902511e-14 F	2.754290e-17 F	
ground	1.636124e-14 F	1.851071e-14 F	1.790224e-14 F	1.872549e-14 F	1.446718e-13 F
	6.499335e-15 F	4.238664e-14 F	4.940276e-14 F	1.994625e-14 F	
mw	4.618862e-19 F	4.368797e-19 F	4.838578e-18 F	4.793744e-18 F	6.499335e-15 F
	8.366264e-17 F	3.741600e-18 F	8.649147e-17 F	1.471664e-19 F	
pad1	5.511480e-14 F	5.842716e-14 F	1.220248e-15 F	1.031340e-15 F	4.238664e-14 F
	3.741600e-18 F	3.089212e-14 F	1.277545e-14 F	2.289361e-14 F	
pad2	1.193224e-15 F	1.229124e-15 F	5.884741e-14 F	5.902511e-14 F	4.940276e-14 F
	8.649147e-17 F	1.277545e-14 F	3.278177e-14 F	2.537538e-16 F	
read	3.612854e-16 F	4.873797e-16 F	3.050805e-17 F	2.754290e-17 F	1.994625e-14 F
	1.471664e-19 F	2.289361e-14 F	2.537538e-16 F	3.488537e-15 F	

Figure C.27: Capacitance matrix for $l = 103.69\,\mu\text{m}$

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
	mw	pad1	pad2	read	
bus1	4.913590e-15 F	8.305416e-17 F	3.117629e-16 F	4.017279e-17 F	1.652817e-14 F
	4.782024e-19 F	5.565253e-14 F	1.198215e-15 F	3.700170e-16 F	
bus2	8.305416e-17 F	5.011027e-15 F	4.237113e-17 F	2.125055e-16 F	1.853702e-14 F
	4.497940e-19 F	5.847741e-14 F	1.230018e-15 F	4.869128e-16 F	
bus3	3.117629e-16 F	4.237113e-17 F	5.338779e-15 F	9.467989e-17 F	1.792007e-14 F
	4.987407e-18 F	1.220648e-15 F	5.892448e-14 F	3.050194e-17 F	
bus4	4.017279e-17 F	2.125055e-16 F	9.467989e-17 F	5.063684e-15 F	1.874244e-14 F
	4.934059e-18 F	1.031387e-15 F	5.908339e-14 F	2.753409e-17 F	
ground	1.652817e-14 F	1.853702e-14 F	1.792007e-14 F	1.874244e-14 F	1.446418e-13 F
	6.616141e-15 F	4.229948e-14 F	4.931370e-14 F	2.005875e-14 F	
mw	4.782024e-19 F	4.497940e-19 F	4.987407e-18 F	4.934059e-18 F	6.616141e-15 F
	8.633998e-17 F	3.849096e-18 F	8.910042e-17 F	1.515149e-19 F	
pad1	5.565253e-14 F	5.847741e-14 F	1.220648e-15 F	1.031387e-15 F	4.229948e-14 F
	3.849096e-18 F	3.086240e-14 F	1.278256e-14 F	2.286328e-14 F	
pad2	1.198215e-15 F	1.230018e-15 F	5.892448e-14 F	5.908339e-14 F	4.931370e-14 F
	8.910042e-17 F	1.278256e-14 F	3.280563e-14 F	2.536320e-16 F	
read	3.700170e-16 F	4.869128e-16 F	3.050194e-17 F	2.753409e-17 F	2.005875e-14 F
	1.515149e-19 F	2.286328e-14 F	2.536320e-16 F	3.487064e-15 F	

Figure C.28: Capacitance matrix for $l = 108.62\,\mu m$

Capacitance matrix for different readout arm length L_{top} in 5.2.2.4

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
	mw	pad1	pad2	read	
bus1	5.327294e-15 F	9.307636e-17 F	3.194441e-16 F	4.270469e-17 F	1.786080e-14 F
	4.939342e-19 F	5.883939e-14 F	1.238513e-15 F	1.932895e-16 F	
bus2	9.307636e-17 F	5.032284e-15 F	4.253670e-17 F	2.124854e-16 F	1.860416e-14 F
	4.443762e-19 F	5.863354e-14 F	1.231221e-15 F	1.910379e-16 F	
bus3	3.194441e-16 F	4.253670e-17 F	5.342687e-15 F	9.453237e-17 F	1.792915e-14 F
	4.924735e-18 F	1.224988e-15 F	5.886917e-14 F	1.708734e-17 F	
bus4	4.270469e-17 F	2.124854e-16 F	9.453237e-17 F	5.056792e-15 F	1.871167e-14 F
	4.859436e-18 F	1.036384e-15 F	5.888119e-14 F	1.547156e-17 F	
ground	1.786080e-14 F	1.860416e-14 F	1.792915e-14 F	1.871167e-14 F	1.448720e-13 F
	6.571759e-15 F	4.420424e-14 F	4.931757e-14 F	1.570968e-14 F	
mw	4.939342e-19 F	4.443762e-19 F	4.924735e-18 F	4.859436e-18 F	6.571759e-15 F
	8.495162e-17 F	3.823113e-18 F	8.795146e-17 F	8.497790e-20 F	
pad1	5.883939e-14 F	5.863354e-14 F	1.224988e-15 F	1.036384e-15 F	4.420424e-14 F
	3.823113e-18 F	3.149538e-14 F	1.282617e-14 F	1.124820e-14 F	
pad2	1.238513e-15 F	1.231221e-15 F	5.886917e-14 F	5.888119e-14 F	4.931757e-14 F
	8.795146e-17 F	1.282617e-14 F	3.281228e-14 F	1.425387e-16 F	
read	1.932895e-16 F	1.910379e-16 F	1.708734e-17 F	1.547156e-17 F	1.570968e-14 F
	8.497790e-20 F	1.124820e-14 F	1.425387e-16 F	2.099075e-15 F	

Figure C.29: Capacitance matrix for $L_{top} = 100\,\mu m$

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
mw	pad1	pad2	read		
bus1	5.333934e-15 F	9.322687e-17 F	3.203338e-16 F	4.276955e-17 F	1.794992e-14 F
	5.033701e-19 F	5.923505e-14 F	1.241105e-15 F	2.192632e-16 F	
bus2	9.322687e-17 F	5.045345e-15 F	4.263395e-17 F	2.133399e-16 F	1.870521e-14 F
	4.529807e-19 F	5.909587e-14 F	1.235910e-15 F	2.167013e-16 F	
bus3	3.203338e-16 F	4.263395e-17 F	5.351357e-15 F	9.471514e-17 F	1.807148e-14 F
	5.007253e-18 F	1.225941e-15 F	5.929789e-14 F	1.884889e-17 F	
bus4	4.276955e-17 F	2.133399e-16 F	9.471514e-17 F	5.067606e-15 F	1.882290e-14 F
	4.918970e-18 F	1.036884e-15 F	5.926785e-14 F	1.707566e-17 F	
ground	1.794992e-14 F	1.870521e-14 F	1.807148e-14 F	1.882290e-14 F	1.448523e-13 F
	7.444514e-15 F	4.384404e-14 F	4.942627e-14 F	1.636983e-14 F	
mw	5.033701e-19 F	4.529807e-19 F	5.007253e-18 F	4.918970e-18 F	7.444514e-15 F
	8.740971e-17 F	3.880597e-18 F	8.876022e-17 F	9.539382e-20 F	
pad1	5.923505e-14 F	5.909587e-14 F	1.225941e-15 F	1.036884e-15 F	4.384404e-14 F
	3.880597e-18 F	3.136400e-14 F	1.287087e-14 F	1.294641e-14 F	
pad2	1.241105e-15 F	1.235910e-15 F	5.929789e-14 F	5.926785e-14 F	4.942627e-14 F
	8.876022e-17 F	1.287087e-14 F	3.281685e-14 F	1.573477e-16 F	
read	2.192632e-16 F	2.167013e-16 F	1.884889e-17 F	1.707566e-17 F	1.636983e-14 F
	9.539382e-20 F	1.294641e-14 F	1.573477e-16 F	2.288291e-15 F	

Figure C.30: Capacitance matrix for L_{top} = 120 µm

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
mw	pad1	pad2	read		
bus1	5.327048e-15 F	9.293144e-17 F	3.199655e-16 F	4.269306e-17 F	1.792701e-14 F
	4.889229e-19 F	5.914501e-14 F	1.239432e-15 F	2.465823e-16 F	
bus2	9.293144e-17 F	5.040381e-15 F	4.257784e-17 F	2.131826e-16 F	1.869097e-14 F
	4.406210e-19 F	5.899301e-14 F	1.234596e-15 F	2.435391e-16 F	
bus3	3.199655e-16 F	4.257784e-17 F	5.349118e-15 F	9.459391e-17 F	1.803003e-14 F
	4.874865e-18 F	1.225563e-15 F	5.921743e-14 F	2.056248e-17 F	
bus4	4.269306e-17 F	2.131826e-16 F	9.459391e-17 F	5.064266e-15 F	1.880175e-14 F
	4.812502e-18 F	1.036220e-15 F	5.920038e-14 F	1.861436e-17 F	
ground	1.792701e-14 F	1.869097e-14 F	1.803003e-14 F	1.880175e-14 F	1.448144e-13 F
	7.464256e-15 F	4.349512e-14 F	4.942393e-14 F	1.701396e-14 F	
mw	4.889229e-19 F	4.406210e-19 F	4.874865e-18 F	4.812502e-18 F	7.464256e-15 F
	8.441427e-17 F	3.775727e-18 F	8.705701e-17 F	1.009248e-19 F	
pad1	5.914501e-14 F	5.899301e-14 F	1.225563e-15 F	1.036220e-15 F	4.349512e-14 F
	3.775727e-18 F	3.125450e-14 F	1.286595e-14 F	1.456519e-14 F	
pad2	1.239432e-15 F	1.234596e-15 F	5.921743e-14 F	5.920038e-14 F	4.942393e-14 F
	8.705701e-17 F	1.286595e-14 F	3.282363e-14 F	1.716828e-16 F	
read	2.465823e-16 F	2.435391e-16 F	2.056248e-17 F	1.861436e-17 F	1.701396e-14 F
	1.009248e-19 F	1.456519e-14 F	1.716828e-16 F	2.471265e-15 F	

Figure C.31: Capacitance matrix for L_{top} = 140 µm

Capacitance Matrix (lumped):

	bus1	bus2	bus3	bus4	ground
mw	4.839269e-19 F	4.355802e-19 F	4.828646e-18 F	4.779323e-18 F	6.546320e-15 F
pad1	5.879052e-14 F	5.876017e-14 F	1.221623e-15 F	1.034997e-15 F	4.312745e-14 F
pad2	1.238028e-15 F	1.231371e-15 F	5.896802e-14 F	5.917008e-14 F	4.934581e-14 F
read	2.769299e-16 F	2.740418e-16 F	2.230097e-17 F	2.021430e-17 F	1.749879e-14 F
bus1	5.321013e-15 F	9.256156e-17 F	3.195824e-16 F	4.271582e-17 F	1.786875e-14 F
bus2	9.256156e-17 F	5.027764e-15 F	4.249623e-17 F	2.128313e-16 F	1.862015e-14 F
bus3	3.195824e-16 F	4.249623e-17 F	5.344112e-15 F	9.466881e-17 F	1.795626e-14 F
bus4	4.271582e-17 F	2.128313e-16 F	9.466881e-17 F	5.068147e-15 F	1.879493e-14 F
ground	1.786875e-14 F	1.862015e-14 F	1.795626e-14 F	1.879493e-14 F	1.447755e-13 F
mw	4.839269e-19 F	4.355802e-19 F	4.828646e-18 F	4.779323e-18 F	6.546320e-15 F
pad1	5.879052e-14 F	5.876017e-14 F	1.221623e-15 F	1.034997e-15 F	4.312745e-14 F
pad2	1.238028e-15 F	1.231371e-15 F	5.896802e-14 F	5.917008e-14 F	4.934581e-14 F
read	2.769299e-16 F	2.740418e-16 F	2.230097e-17 F	2.021430e-17 F	1.749879e-14 F

Figure C.32: Capacitance matrix for $L_{top} = 160\,\mu m$

Capacitance Matrix (lumped):

	bus1	bus2	bus3	bus4	ground
mw	4.842326e-19 F	4.359795e-19 F	4.821393e-18 F	4.760758e-18 F	7.080892e-15 F
pad1	5.907346e-14 F	5.909068e-14 F	1.223563e-15 F	1.034574e-15 F	4.272371e-14 F
pad2	1.239344e-15 F	1.233791e-15 F	5.935778e-14 F	5.945055e-14 F	4.941720e-14 F
read	3.177688e-16 F	3.150377e-16 F	2.435366e-17 F	2.205045e-17 F	1.830523e-14 F
bus1	5.326135e-15 F	9.251225e-17 F	3.203558e-16 F	4.269813e-17 F	1.794789e-14 F
bus2	9.251225e-17 F	5.033080e-15 F	4.255901e-17 F	2.131355e-16 F	1.868364e-14 F
bus3	3.203558e-16 F	4.255901e-17 F	5.351653e-15 F	9.477096e-17 F	1.805933e-14 F
bus4	4.269813e-17 F	2.131355e-16 F	9.477096e-17 F	5.066343e-15 F	1.879396e-14 F
ground	1.794789e-14 F	1.868364e-14 F	1.805933e-14 F	1.879396e-14 F	1.447388e-13 F
mw	4.842326e-19 F	4.359795e-19 F	4.821393e-18 F	4.760758e-18 F	7.080892e-15 F
pad1	5.907346e-14 F	5.909068e-14 F	1.223563e-15 F	1.034574e-15 F	4.272371e-14 F
pad2	1.239344e-15 F	1.233791e-15 F	5.935778e-14 F	5.945055e-14 F	4.941720e-14 F
read	3.177688e-16 F	3.150377e-16 F	2.435366e-17 F	2.205045e-17 F	1.830523e-14 F

Figure C.33: Capacitance matrix for $L_{top} = 180\,\mu m$

Capacitance Matrix (lumped):

---

	bus1	bus2	bus3	bus4	ground
mw	pad1	pad2	read		
bus1	5.322066e-15 F	9.227983e-17 F	3.200766e-16 F	4.267143e-17 F	1.791697e-14 F
	4.924601e-19 F	5.901358e-14 F	1.239700e-15 F	3.611152e-16 F	
bus2	9.227983e-17 F	5.030283e-15 F	4.252155e-17 F	2.131006e-16 F	1.868980e-14 F
	4.433488e-19 F	5.901098e-14 F	1.233990e-15 F	3.587333e-16 F	
bus3	3.200766e-16 F	4.252155e-17 F	5.348404e-15 F	9.474109e-17 F	1.803684e-14 F
	4.912715e-18 F	1.221360e-15 F	5.934460e-14 F	2.619868e-17 F	
bus4	4.267143e-17 F	2.131006e-16 F	9.474109e-17 F	5.066501e-15 F	1.879521e-14 F
	4.847436e-18 F	1.033058e-15 F	5.942574e-14 F	2.373145e-17 F	
ground	1.791697e-14 F	1.868980e-14 F	1.803684e-14 F	1.879521e-14 F	1.446902e-13 F
	7.203248e-15 F	4.234043e-14 F	4.942002e-14 F	1.876272e-14 F	
mw	4.924601e-19 F	4.433488e-19 F	4.912715e-18 F	4.847436e-18 F	7.203248e-15 F
	8.523699e-17 F	3.783881e-18 F	8.758779e-17 F	1.288966e-19 F	
pad1	5.901358e-14 F	5.901098e-14 F	1.221360e-15 F	1.033058e-15 F	4.234043e-14 F
	3.783881e-18 F	3.087414e-14 F	1.283325e-14 F	1.956653e-14 F	
pad2	1.239700e-15 F	1.233990e-15 F	5.934460e-14 F	5.942574e-14 F	4.942002e-14 F
	8.758779e-17 F	1.283325e-14 F	3.281530e-14 F	2.186783e-16 F	
read	3.611152e-16 F	3.587333e-16 F	2.619868e-17 F	2.373145e-17 F	1.876272e-14 F
	1.288966e-19 F	1.956653e-14 F	2.186783e-16 F	3.063712e-15 F	

Figure C.34: Capacitance matrix for L_{top} = 200 µm