Structured design of an external NMOS based Linear Voltage Regulator for automotive applications

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By

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Abstract

The electronization of automobiles is considered to be a revolution in automotive technology development progress. System level integrated circuits are needed to simplify the automotive electronics design and increase the reliability of automobiles.

In this thesis, a prototype of a linear voltage regulator is designed for system level integration. Instead of a conventional Internal PMOS or NMOS linear regulator topology, an external NMOS transistor produced by NXP is chosen as the pass device on considerations of certain commercial application. The parasitic inductance and capacitors of PCB traces and packaging are both modeled and calculated. The requirement differences of internal and external NMOS linear regulators are compared. This external NMOS transistor complicates the high-frequency design of this voltage regulator. The development of frequency compensation strategies as well as their implementation is the core of this work. Based on transistor models made by the author and the Root-Locus analysis method, the effectiveness of conceptual active compensation is examined in this thesis, and a passive frequency compensation scheme is proposed. This proposed scheme is not only able to accommodate the wide variation of load capacitor (470nF to 47µF) and the wide variation of load current (0 to 250mA) but also able to be compatible with the external NMOS. The effectiveness of passive frequency compensation is examined by both Root Locus analysis and transistor level simulation. The over-current protection of the NMOS linear regulator is also designed, which is realized by applying another current regulation loop to the voltage regulator. This voltage regulator is able to maintain a constant output current around 400mA in over-current protection scenario. The regulator quiescent current is 10µA, the output voltage accuracy is ±2%.

At the end of this thesis, the performance aspects are discussed and analyzed, and the influence of parasitic PCB trace and packaging is examined.

Acknowledgements

Two and a half years ago, I came to Netherlands with my passion and love for learning. I know that without the support of others, it would not be possible for me to reach this stage.

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1 Introduction

The year 1886 is regarded as the birth year of the modern car. In that year, German inventor Karl Benz built the Benz Patent-Motorwagen [1], this invention has changed human society to a large extent. With the development of electronic technology, electronic devices embedded in automobiles have shown significant advantages in aspects of controllability, comfortability, and safety. The first electronic devices were used to control engine functions and were referred to as engine control units (ECU) [2]. As electronic controls began to be used for more automotive applications, the acronym ECU took on the more general meaning of "electronic control unit" [3]. In this thesis, we will discuss salient points of the power supply design for automotive vehicles and focus on the design of a voltage regulator with an external NMOS transistor.

1.1 Project motivation

A modern automotive vehicle is not only a huge mechanical system but also a complex electrical system. A modern car may have up to 100 ECU's and a commercial vehicle up to 40 [4], such as airbag control unit, body control module, engine control unit, brake control module and so on. As in any other electrical systems in other domains, power management is an extremely important part of the automotive electrical system.

Figure 1-1 shows a simplified power management system in a car. This system handles the battery charging through a generator (stator and rectifier). The generator voltage control is used to regulate the generator output voltage to 12V. The battery is supplying power to separate electronic control units (ECUs) and other electric modules [5].

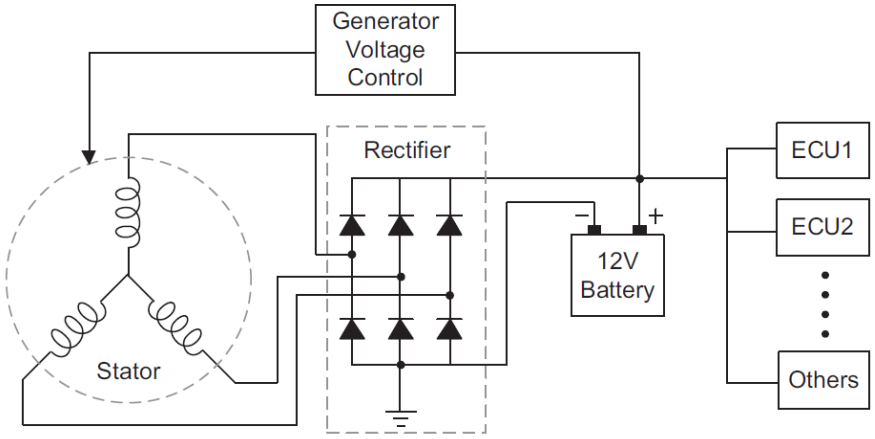


Figure 1-1 A simplified automotive power management system [5]

An example of an ECU is shown in Figure 1-2. It consists of power management in ECU, and also data transmitting and receiving (CAN [6] and LIN [7]), micro-controlling, sensing and actuation modules. The power of ECU is supplied by a typical value 12V lead-acid battery. Normally, many electronic devices inside the ECU need lower voltage than this battery supply. Therefore, a power management module with DC voltage conversion is essential. In the ECUs, the micro-controller is the central processing unit, sensors and actuators are required for the transfer between electronic and other different domains.

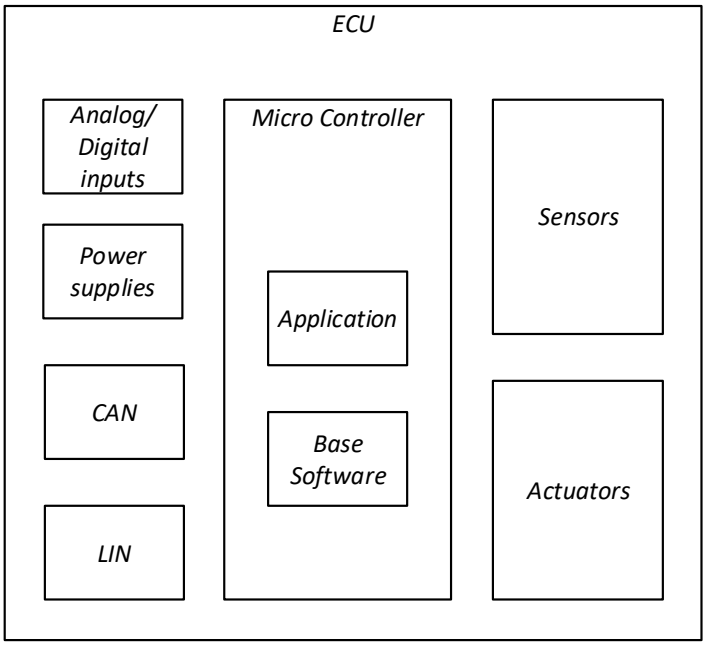


Figure 1-2 A typical ECU diagram

Figure 1-3 shows the basic topology of the voltage regulator used in this thesis. The following design is based on this topology. Part of this regulator is on-chip and the pass device needs to be off-chip. Principally, this is a negative feedback voltage amplifier that amplifies the reference voltage and is capable of sourcing

large current to a load. The pass transistor passes the current from the car battery to the load, the pass device can be either NMOS or PMOS. In this design, the external NMOS is an essential component because smaller silicon area and less heat dissipation are required, another advantage of the external power transistor is the flexibility to populate it or not, so the pass device will be NMOS. It is driven by the controller in such a way that the load voltage is maintained at its desired value under varying load conditions and over a wide battery voltage range. The external NMOS is supplied by the battery in the car and the controller is supplied by a 10V voltage, which is output voltage value of a Charge Pump in this Micro-Controller. Importantly, the dash lines mean the last stage of the controller can be either common source or common drain stage, which will be discussed in Section 6.3. The external transistor has been chosen as BUK9Y29-40E by NXP. In this Micro-Controller, the distance between pass device and on-chip circuit can be as long as 20cm on the PCB board, which means the PCB trace connecting the external transistor and the on-chip part can be the same length, so the influence of PCB trace and packaging needs to be modeled and tested in this design. Generally, a high-performance low-dropout voltage regulator with external NMOS transistor needs to be designed, the main performance aspects are:

i. Quiescent power consumption
ii. Accuracy of the load voltage
iii. Static and dynamic load regulation
iv. Static and dynamic line regulation
v. Over current protection
vi. Minimum drop-out voltage
vii. Ability to handle a large range of load capacitance

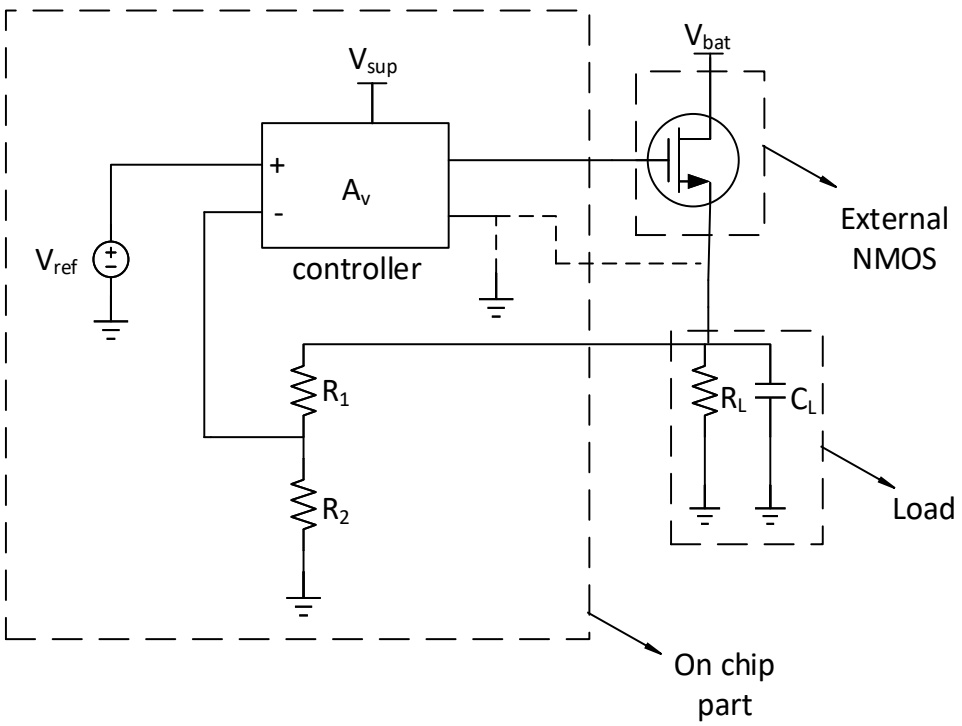


Figure 1-3 Schematic diagram of basic topology in this design

1.2 Organization of this thesis

In Chapter 2, the requirements of this voltage regulator are discussed.

In Chapter 3, the technology used in this design is introduced. This technology is from the previous Freescale.

In Chapter 4, the characteristic of the power MOSFET and the motivation of the modified EKV model are discussed.

In Chapter 5, the parasitics induced by PCB and packaging are modeled. The PCB and Packaging parasitic are considered as design risk in the beginning of this project.

In Chapter 6 and Chapter 7, specifically, the design of this voltage regulator is presented. The design approach, design considerations and the design of the controller are discussed in Chapter 6. The transistor sizing, small signal analysis of this voltage regulator, compensation schemes are discussed in Chapter 7. The implementation of over current protection circuit, floating current sources, floating voltage sources, and current dump path are also written in this Section.

In Chapter 8, the performance of this voltage regulator is evaluated and summarized.

Finally, Chapter 9 presents conclusions of this thesis and gives suggestions for future work.

2 Requirements

Table 2-1 shows the required specifications of this LDO. The details and numbers are explained in the following part.

symbol	parameter	condition	min	typ	max	unit
V_{IN}	Regulator Input Voltage	.	5.5	.	40	V
V_{OUT}	Output Voltage	$I_{out} = 10\mu A$ to 250mA	4.9	5	5.1	V
$V_{out\text{-}load}$	Dynamic Load Regulation	.	-2	.	2	%
$t_{stabilized}$	output voltage within 0.5% after load step	.	.	.	1	ms
$V_{out\text{-}line}$	Dynamic Line Regulation	.	-2	.	2	%
I_q	Quiescent Current (w/o band-gap)	$I_{out} = 0$ to 10µA Temp $\leq 85°C$	.	.	10	µA
$I_{q'}$	Current Consumption (w/o band-gap)	$I_{out} \geq 1mA$	.	.	$1.3\% \cdot I_{out}$	µA
C_L	External Output Capacitor		0.47	.	47	µF
I_{out}	Maximum Load Current		.	.	250	mA

Table 2-1 Specifications form of voltage regulator

2.1 Static state specifications

The drop-out voltage, quiescent current, line regulation, load regulation, and temperature drift are five major static state specifications, which will be discussed in detail in this Chapter.

2.1.1 Drop-out voltage

Linear regulators are also classified as low or high dropout (LDO or HDO), which refers to the minimum voltage dropped across the circuit, in other words, the minimum difference between the unregulated input supply and the regulated output voltage under the condition that the regulator can still maintain the regulation function within specs. Linear regulators with dropout voltages below 600 mV belong to the

low-dropout class. In our design, the drop-out voltage should be 0.5V because the lowest value of the battery in the car is 5.5V and the output voltage of this regulator is 5V.

2.1.2 Quiescent current

The quiescent current is defined as the current consumed by the control circuits of the linear voltage regulator. In the case of linear regulators, quiescent-current flow I_q and the voltage difference between the unregulated supply V_{in} and regulated output V_{out} limit power-efficiency performance to considerably lower levels,

$$\eta_{lin-reg} = \frac{I_{load}V_{out}}{(I_{load} + I_q)V_{in}}$$

In which I_{load} is the load current and quiescent current I_q flows to ground, not the load. The maximum quiescent current requirement in this LDO is defined as 10μA.

2.1.3 Line regulation

Line regulation (LNR) performance, is a dc parameter and it refers to output voltage variations arising from dc changes in the input supply, in other words, to the low-frequency supply gain of the circuit. In our project, the output voltage should be in the range from 4.9V to 5.1V under the variation of regulator input voltage from 5.5V to 40V [8].

2.1.4 Load regulation

DC voltage variations in the output resulting from dc changes in load current define load regulation (LDR) performance, which ultimately constitutes an ohmic voltage drop, that is, a linearly load-dependent voltage drop at the output of the regulator. In our design, the output voltage should be in the range from 4.9V to 5.1V under the variation of regulator load current from 0A to 250mA [8].

2.1.5 Temperature drift

In more generalized terms, any variation in the reference propagates to the output of the regulator through the equivalent voltage gain of the regulator. Linear regulator temperature coefficient (TC) is defined as the percentage of output voltage variation in response to temperature change which has a unit of %/°C. It can be expressed as:

$$TC = \frac{1}{V_{out}}\left(\frac{dV_{out}}{dT}\right) \approx \frac{1}{V_{out}}\left(\frac{\Delta V_{out}}{\Delta T}\right) = \frac{(\Delta V_{ref} + \Delta V_{os})\left(\frac{V_{out}}{V_{ref}}\right)}{V_{out}\Delta T} = \frac{1}{\Delta T}\left(\frac{(\Delta V_{ref} + \Delta V_{os})}{V_{ref}}\right)$$

In which ΔV_{ref} and ΔV_{os} are the temperature-induced variations of the reference voltage V_{ref} and input-referred offset voltage V_{os} and ΔT the corresponding change in temperature. In our design, the output voltage should be in the range from 4.9V to 5.1V under the variation of temperature from -40°C to 175°C.

2.2 Specifications of dynamic behavior

The abilities of the linear regulator in response to supply voltage and load current transient variation are two major dynamic state specifications, which will be introduced in detail in this part.

2.2.1 Line transient response

Line transient response is the output voltage variation in response to the suddenly changing of the supply voltage. The most important parameters that describe the line transient response including the settling time of the output voltage when line variation happens, and overshoot/undershoot peak of the output voltage. In our design, the output voltage of this LDO should be in the range from 4.9V to 5.1V in response to the line step variation from 5.5V to 40V or from 40V to 5.5V. The rise time and fall time are defined in the test bench.

2.2.2 Load transient response

Load transient response is defined as the linear regulator's ability to regulate the output voltage during fast load transients. In practical cases, the circuit loaded by a linear regulator can be dynamic (e.g. a micro-controller operating at several tens of MHz), the load current variation is fast and unpredictable. This requirement rules the overshoot, undershoot amplitude and also the settling time of the output voltage when supply variation happens. Similar to the line transient response specs, the output voltage of this LDO should be in the range from 4.9V to 5.1V in response to the load step variation from 100µA to 250mA or from 250mA to 100µA in a certain time, which is defined in the test bench.

2.3 Differences in requirements with the last generation LDO in NXP

The last generation LDO comprises an internal NMOS transistor, instead of an external transistor in the product of this generation. The selected BUK transistor is a high current MOSFET designed with a low R_{DSon}. The characteristics of this device are not optimized for this application. The BUK transistor is always working in the weak inversion, which is not modeled in the SPICE model of this BUK. The existence of this BUK transistor increases the difficulty in designing a stable voltage regulator because of trans-conductance variation and its huge parasitic capacitance. And the existence of the huge input capacitance puts severe requirements on the current drive capability of the driving stage. Some detailed characteristics of this BUK transistor are described in Section 4.1.

As stated in Section 1.1, the existence of PCB and Packaging has to be modeled and analyzed in this design.

In addition, as stated in Section 1, this LDO is supposed to be able to handle a larger range of load capacitance and load current.

3 Technology

In the beginning of this design, the ABCD9 of NXP is the technology process supposed to be used, but we transferred to the technology named SMOS10HV of Freescale because of the merging case of NXP and Freescale. The IC process SMOS10HV, which released in 2014 by Freescale, aiming at highly integrated Automotive and Industrial applications, will be introduced in this Chapter.

SMOS10HV is a 130nm process, the process architecture of SMOS10HV is not included in this thesis because of the confidential reason. Each component is surrounded on all sides by hard ground plane, and each component or group of components is surrounded by oxide isolation. In addition, there is no parasitic components to substrate and the EPI process is simple [9].

The key technology features of SMOS10HV are:

1. Fully dielectric isolated technology platform.
2. High-density logic, which is 130nm.
3. High voltage Power MOSFETs > 90V.
4. Eliminates substrate injection and device cross-talk.
5. Dual polarity isolation (+90V to -40V).
6. High-temperature operation (low leakage).
7. High level of Latch-up immunity.

4 Models

4.1 Power MOSFET characteristics

For commercial reasons, a 40V Automotive MOSFET of NXP is selected as the external pass device in this design, whose graphic symbol is shown in Figure 4-1.

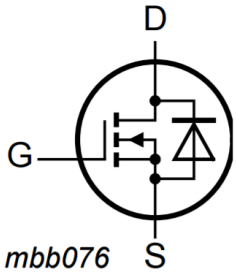


Figure 4-1 Graphic symbol of the external NMOS

From datasheet of BUK9Y29-40E, the transfer characteristics are shown in figure 4-2. The full load current is 250mA, so this BUK transistor is always working in its weak inversion region.

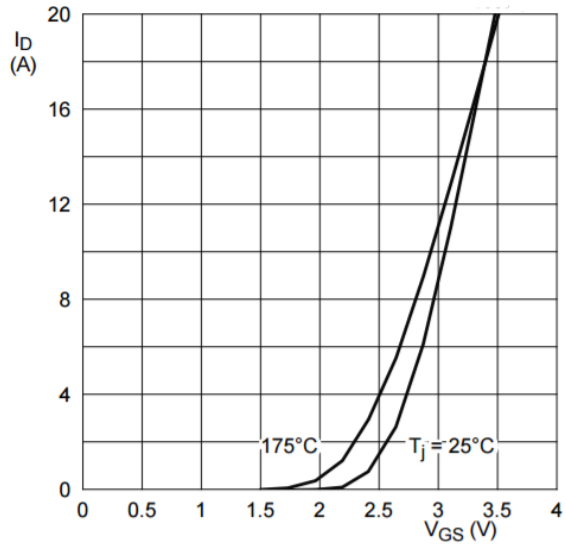


Figure 4-2 Transfer characteristics; drain current as a function of gate-source voltage; typical values; V_{DS}=10V

This BUK transistor has its own SPICE model available, which is a level 3 SPICE MOSFET model. It is predictable that this model is not qualified enough because the weak inversion region is not modeled continuously, which is the region that we are really interested in this design. To sum up, the model of this BUK is potential design risk in this design.

4.2 SLiCAP models

The analyses of dynamic behavior are essential in order to design a stable voltage regulator. In Cadence, you need schematics including biasing before you can do analyses of the dynamic behavior and it can be extremely cumbersome if you want to have Root Locus plots. There is a software designed for analog circuit design named SLiCAP, which supports the design method in which the level of complexity of small signal models at subsequent stages of the design can be chosen differently. These models are based on device parameters and operating conditions. These conditions do not need to be fixed by biasing circuits. These models are based on the EKV model [10], which includes all the operating regions of transistors and yields a detailed expression of g_m over wide current range. All the detailed physical parameters are acquired by fitting the g_m vs I_d plots and F_T vs I_d plots of transistors in Cadence and SLiCAP. The detailed procedures of fitting are shown in Appendix 10.1.

5 PCB and Packaging modeling

5.1 PCB

For the PCB trace connecting the on-chip controller and the external NMOS, a finite element approximation can be applied, with this approximation method, we model a trace with length X into N Sections of a unit length. The first procedure should be determining unit length inductance and capacitance, then the T- or π-network can be used to model the PCB trace [11], Concatenating N Sections to make trace with length X is the last step to finish the PCB model.

There are some advantages of this method: it is a simple scalable model and not much effort needed to extract unit length characteristics for a certain trace geometry. This method is suitable up to several GHz, depending on unit size. In our case, the frequency content of Low Dropout Regulator is far below several GHz.

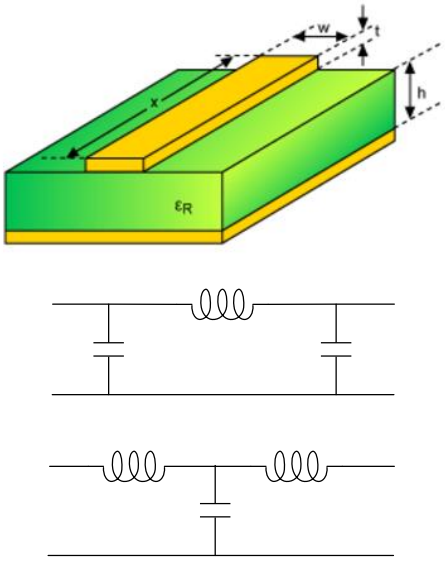


Figure 5-1 π and T model of PCB trace

5.1.1 Unit inductance and capacitance

We can use one or two of the formulas below to calculate the unknown L and C [11]:

$$C_0 = \frac{2.64 \cdot 10^{-11}(\varepsilon_r + 1.41)}{\ln\left[\frac{5.98H}{0.8W + T}\right]}$$

$$Z_0 = \frac{87}{\sqrt{1.41 + \varepsilon_r}} \ln\left(\frac{5.98H}{0.8W + T}\right)$$

$$L_0 = {Z_0}^2 C_0$$

In the conventional PCB industry, T is the trace thickness and T can be 18μm, 35μm and 70μm, W is the width of the trace and can vary from 25μm to 660μm, H is the height of dielectric above the return plane, which is in the range of 100μm to 1.6mm. The W and H follow the rule $0.1 < \frac{W}{H} < 3$ for the manufacturing requirement. In order to find the worst and typical case for this project, the calculated values of width are taken as 25μm, 70μm, 150μm, 300μm and 660μm.

The form in Appendix 10.3 shows the results of the unit inductance and unit capacitance in the PCB model (the first form shows the results followed the situation W/H = 0.1 and all the other rules, the second form shows the results followed the situation W/H = 3 and all the other rules).

The table of unit capacitance and unit inductance calculation can be found in Appendix 10.3. The worst case of the unit length inductance is $8.3 \cdot 10^{-7}$ H/m. Hence, for the 20cm PCB trace, the inductance is 166nH. The worst case of the unit length capacitance is $2.17 \cdot 10^{-10}$ F/m. Hence, for the 20cm PCB trace, the capacitance value is 43.4pF. For convenience of the following design, we should also choose a typical trace dimension value, The column with black shading in Appendix 10.3 is chosen as the typical value because this dimension is common in the industry application.

5.2 Packaging

The package model contains three main Sections [12]:

1. (Coupled) bond wires, modeled as four RLCK π Sections.
2. Lead fingers, modeled as capacitance to ground and between leads.
3. PCB solder pads, modeled as capacitance to ground.

The analytical model can be used in the design exploration phase to run simulations with varying bond wire length, pitch and height.

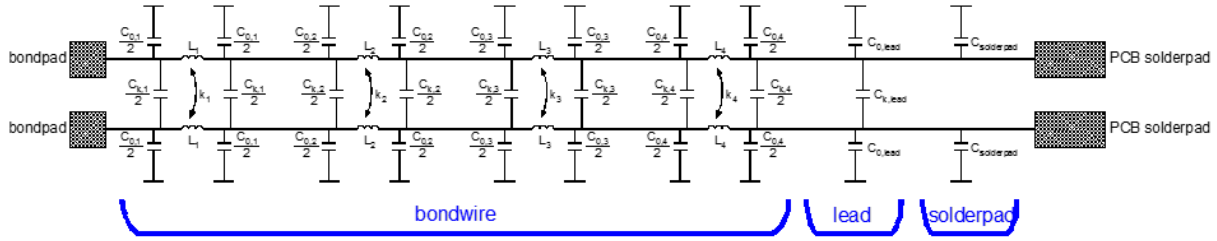


Figure 5-2 Packaging model diagram

5.2.1 Bond wire

In integrated circuit industry, diameter of bond wire is 20-25 µm, length of bond wire is 1-4 mm.

We take the diameter 20 µm and length 2 mm, and under room temperature, the resistivity of Gold is $2.44 \cdot 10^{-8}\ \Omega \cdot m$.

$$R = \rho_{Au} \cdot \frac{l}{\pi r^2} = 0.155\Omega$$

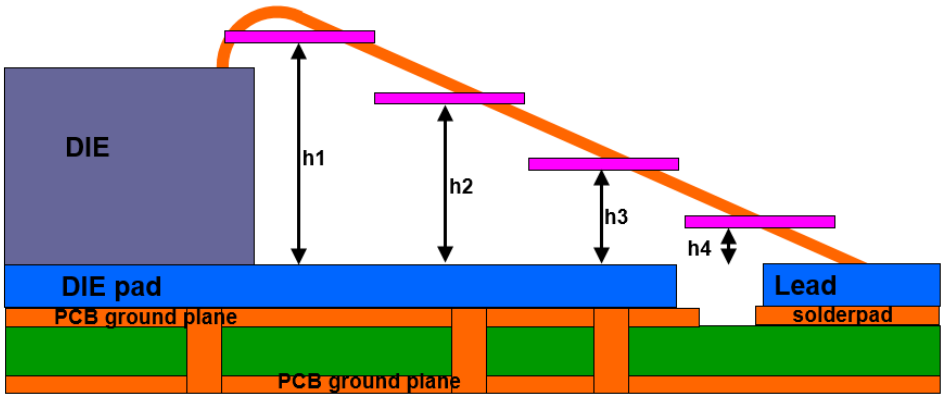


Figure 5-3 bond wire model

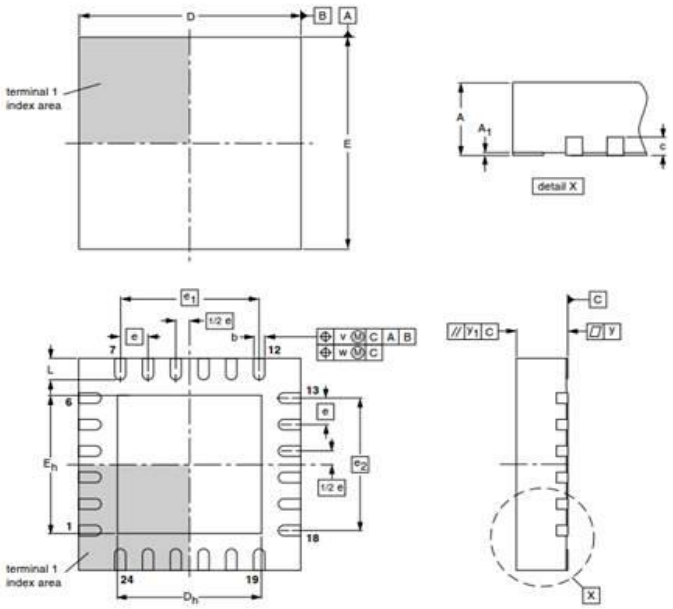
In the bond wire model, each bond wire is split into 4 segments, for each segment the RLCK values are calculated, the height above the ground plane at the die side and the PCB side are required as inputs, the height for the 2 intermediate segments is interpolated.

We take the common values of the h_1, h_2, h_3, and h_4 in the industry area, which are 200µm, 300µm, 400µm, 500µm. Similarly, we take the inductance values of each segment, which are 0.46nH, 0.44nH, 0.41nH, 0.37nH respectively, and the capacitance values of each segment, which are 0.024pF, 0.025pF, 0.027pF, 0.03pF respectively.

The sum of self-capacitance and mutual-capacitance {calculation in Appendix} of the bond wire are much smaller compared with the capacitance of PCB trace (100-300 times). In the design procedure, the bond wire capacitance can be neglected.

5.2.2 Lead

For the leads we use the package geometry information to calculate the parallel-plate capacitance.



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.75 2.45	4.1 3.9	2.75 2.45	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Figure 5-4 lead diagram and dimension

The distance between the lead and die-pad is in the range of 100µm to 500µm. The lead height is 0.2mm, the lead width is 0.3mm, and the lead Length is 0.5mm. According to equation below:

$$C_{0,lead} = \frac{\varepsilon_r \varepsilon_0 hw}{d}$$

In which h is the lead height and w is the lead width, d is the distance between the lead and the die pad. $C_{0,\ lead}$ =7.08 · 10-15 F (take the value of distance as 300µm). This capacitance is small enough to be neglected in the design and test procedures.

5.2.3 Solder Pads

For the solder pads, we use the PCB stack up and geometry information to calculate the parallel-plate capacitance. The solder pad to ground plane capacitance can be calculated from the area. Normally, the distance between the solder pad and ground plane varies from 100µm—5mm. Take the pad width and height values from the dimension figure we used in the previous lead frame part. The width and length are 2.75mm and 4.1mm respectively.

$$C = \frac{\varepsilon_r \varepsilon_0 wl}{d}$$

In which the w is the lead width, l is the lead length and d is the distance between the solder pads and the ground plane. This value should be taken into account in the design procedure when it is big enough, so in the design, we take the worst case which is 4pF.

5.2.4 Modeling Conclusion

Parameters will be taken into account in the design:

1. RLC of the PCB trace.
2. The capacitance of the solder pad.

6 Conceptual design

6.1 Design approach

In this design, a structured step by step design method is followed [13]. Principally, this voltage regulator can be designed as a negative feedback amplifier with external transistor. The on-chip circuit controls the external transistor, and in this report, the on-chip amplifier and external transistor are together called as the controller. During this step by step method, we will design and verify various performance aspects of this controller. The outlines of the design procedures are:

1. Consider the design requirements in this voltage regulator to find a more orthogonal design method.
2. Design the main configuration of the controller, based on the driving requirement of external transistor and driving requirement of stages in the controller.
3. Transistor sizing of the controller.
4. Stability analysis based on the basic configuration of this voltage regulator. The linear simulator SLiCAP is used to help this analysis.
5. If this regulator is unstable, then the frequency compensation of this regulator needs to designed
6. After the stability of this regulator is achieved in SLiCAP, test the stability by load transient and line transient simulations in Cadence, and also check the other performances by load transient and line transient simulations.
7. Design and Implement the other details of this voltage regulator according to the design requirements, e.g. Biasing circuit, over current protection, floating source implementation.
8. Test the whole design in Cadence.

6.2 Design considerations

6.2.1 Power consumption

The minimum values of the feedback resistors are determined by the quiescent current requirement. In the meanwhile, the maximum values of the feedback resistors are determined by the noise requirement.

Principally, part of the quiescent current budget is distributed on the feedback resistors, in this design, as a starting point, 1μA budget is distributed on the feedback resistors, the other 9μA are distributed on the circuit except the feedback resistors.

6.2.2 Noise

The output noise is an important specification when the voltage regulator is driving a noise sensitive Analog/RF block, for example a high-quality audio circuit or an RF transceiver. The noise coming from the voltage regulator will degrade the loading circuit performance. In this design, the noise requirements is included in the output voltage accuracy requirement, which means the output voltage should be in the range from 4.9V to 5.1V including the noise influence. The noise of a voltage regulator consists of two main parts: feedback elements noise, voltage regulator circuit noise. For a well-designed voltage regulator, the main contribution of noise should be the first stage of the regulator circuit. In fact, the first stage is input differential pair, however, given the truth that the noise evaluation of input differential pair is much more complex than the noise evaluation of a single properly biased MOSFET, and the noise evaluation result can be transferred to input differential pair, evaluation of the MOSFETS in the voltage regulator can be represented by a properly biased single MOSFET. If we use $\overline{V_{dp}^2}$ to represent the input equivalent voltage noise generator of a differential pair and $\overline{V_i^2}$ to represent the input equivalent voltage noise generator of a single properly biased MOSFET in the differential pair, the relation between $\overline{V_{dp}^2}$ and $\overline{V_i^2}$ is:

$$\overline{V_{dp}^2} = 2\overline{V_i^2}$$

Figure 6-1 shows the test set up circuit for noise measurement, in which the transistor is the input stage transistor, the noise contribution of the feedback resistors R1 and R2 are accounted for as if their parallel connection is in series with the reference voltage source, the current source represents the quiescent current in this transistor, which depends on the quiescent current distribution in this voltage regulator, the value of this current is set as 3μA in this measurement. The reason for the value of this quiescent current can be found in Chapter 7. The size of MOSFET is chosen as the smallest one because it can offer the largest possible noise than larger size. However, in this schematic, the value of the voltage source VDC needs to be accurate enough to match the value of this quiescent current, which is not easy because of the nonlinear relation between them in the MOSFET. Therefore, the set-up schematic is optimized as Figure 6-2, in which the right voltage value of V_{DC} can be achieved because of the control loop, In addition, in order to investigate the noise in input stage accurately, the capacitor C_{large} is set as a large capacitor which can eliminate the noise coming from the loop.

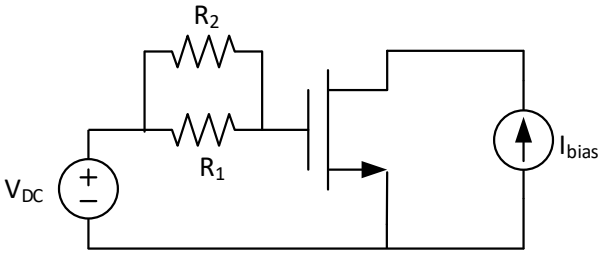


Figure 6-1 A test set up circuit for noise measurement

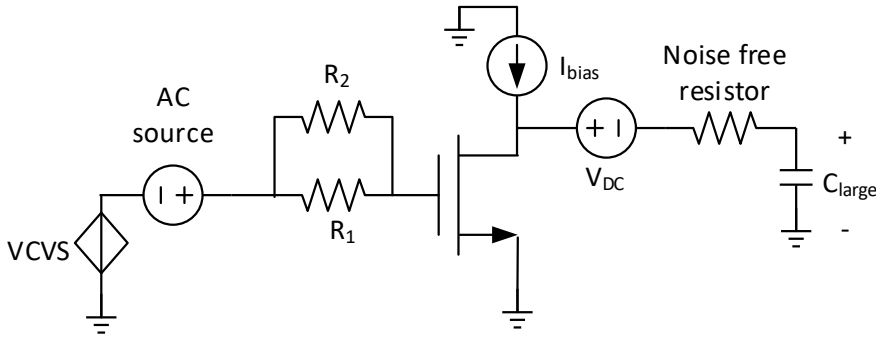


Figure 6-2 Improved test set up circuit for noise measurement

The input equivalent noise in this case is shown in Figure 6-3. When the frequency is smaller than 1KHz, the noise is mainly contributed by $1/f$ noise of MOSFET, when the frequency is larger than 1KHz, the thermal noise becomes dominant. From Figure 6-4, we can know the integrated noise from 1Hz to 1MHz is 123μV_{rms}. Comparing with the input voltage (1.2V), this integrated noise value will not influence the output accuracy, in conclusion, the noise influence on output accuracy can be neglected in this design.

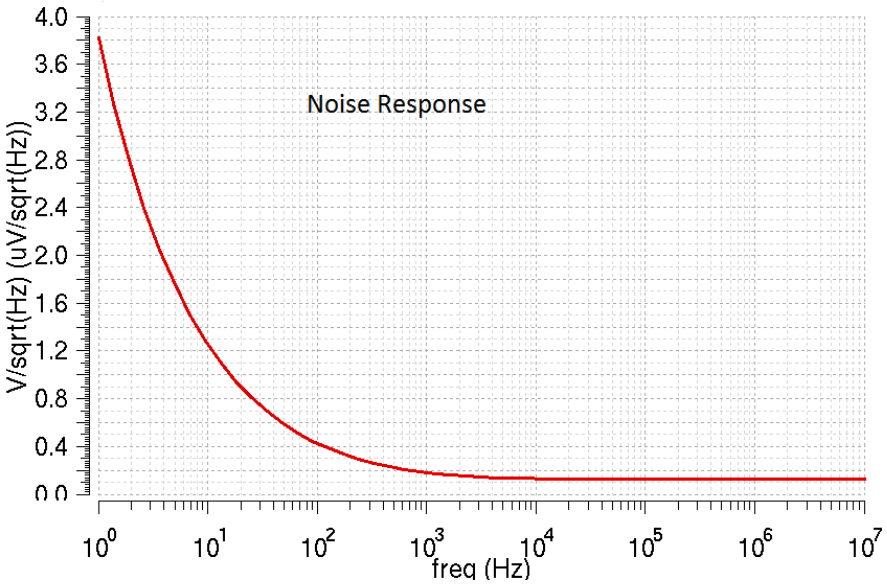


Figure 6-3 Source referred noise spectrum density

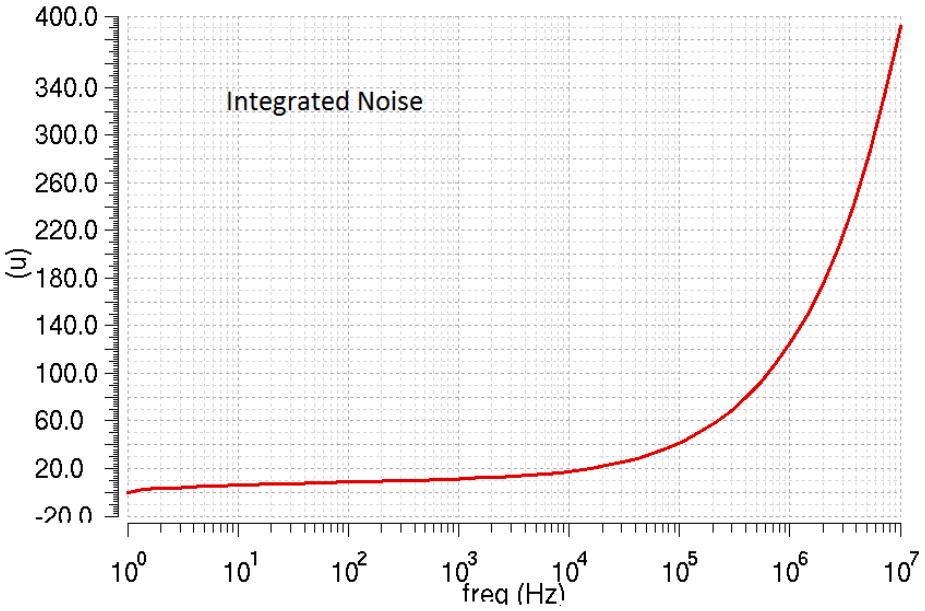


Figure 6-4 Source referred integrated noise

6.2.3 Large signal dynamic behavior

In this design, minimum driving current of each stage is determined by stabilized time after load step. Specifically, the driving current for BUK transistor is critical to ensure sufficient fast settling before output voltage going out of required range. Similarly, the driving current for the other stages is also critical to fast settling of next stage.

6.2.4 Small signal dynamic behavior

As stated before, the design of the small signal stability is the core work of this project. The voltage regulator should be stable with the load current and capacitor variation.

6.3 Design of the architecture of controller

From the view of top level, the DC output impedance of the voltage regulator is important because if load variation happens, the output voltage error is proportional to the DC output impedance. As Figure 6-5 shows, the controller and BUK transistor can be regarded as a block in order to get the value of the DC output impedance, the trans-conductance of this block is represented as g_m.

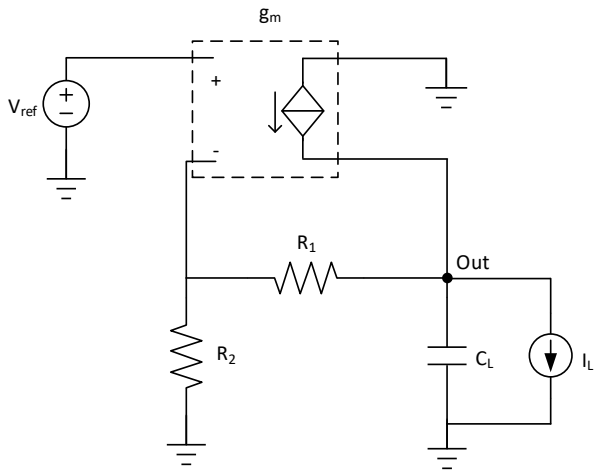


Figure 6-5 simplified 1-stage voltage regulator

Basically, the output impedance holds the expression:

$$Z_{out} = \frac{dV_{out}}{dI_{out}}$$

Output impedance expression can be found as:

$$Z_{out} = \frac{R_1 + R_2}{\left(\frac{s(C_L R_1 + C_L R_2)}{R_2 g_m + 1} + 1\right)(R_2 g_m + 1)}$$

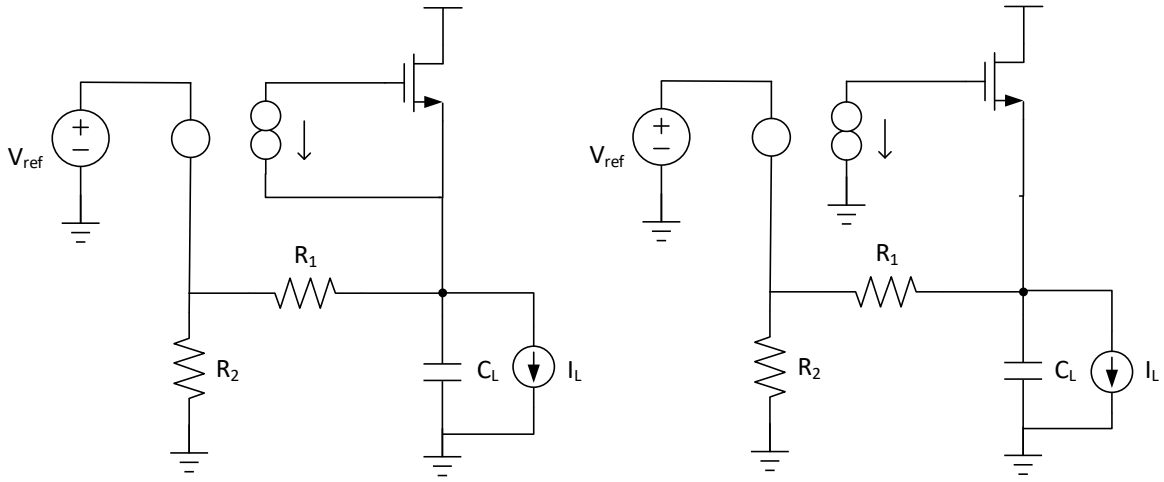
From equation above, the DC output impedance is:

$$R_{out} = \frac{R_1 + R_2}{R_2 g_m + 1}$$

In this simple 1-stage system, if less than 0.5% output error after load step is demanded, the output impedance should be lower than 0.1Ω. Therefore, according to equation above, the g_m should be large enough to ensure low output impedance, which means g_m should be larger than 41.76S.

A single-stage solution is not feasible, a multi-stage controller is required in this project, because the external NMOS is an essential component, but with only external NMOS, the four-terminal controller is not feasible.

In this design, the external NMOS transistor needs to be included as pass device, in the rest part, the controller can be implemented ideally if there is nullor in nature. There are two options of implementation shown in Figure 6-6 [13].



(a) Common source configuration (b) Common drain configuration

Figure 6-6 LDO with common drain or common source configuration controller

When the regulator is in quiescent scenario, if the load variation happens, the load capacitor will discharge with the current of 250mA, the output voltage will drop and reach its maximum allowable drop of 0.1V (instead of 0.2V to keep some margin for other error sources) within a short time, before which the regulator has to be able to respond. Based on the basic expression:

$$t = \frac{C_L V_{error}}{I_{Step}}$$

In which t is the time, C_L is the load capacitor, V_{error} is the maximus output voltage error we can accept in this design. I_{step} is the maximum load current step, which is 250mA.

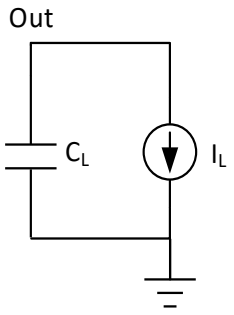


Figure 6-7 discharging schematic diagram on load capacitor with maximum load step

From equation above, the time to reach the voltage drop limitation is 188ns. Before this time the external NMOS input capacitance must be charged and this requires a large enough driving current. The delta V_{gs} required to drive external NMOS from a few µAmps to 250mAmps can be simulated as shown in Figure 6-8.

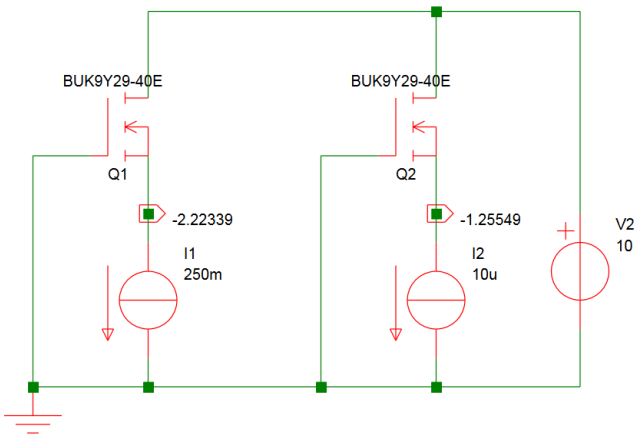
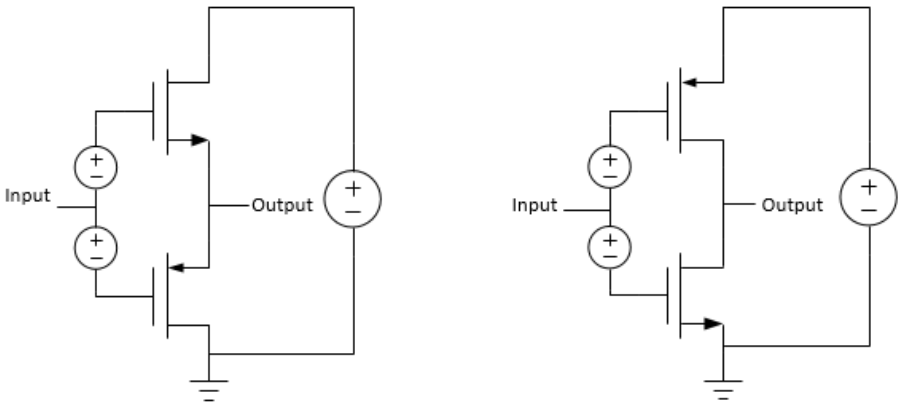


Figure 6-8 simulation schematic set up to derive delta V_{gs}

ΔV_{gs} is 1V, take the largest C_{gs} value from product datasheet, which is 500pF and according to equation below, we know the design information that required driving current I_{drive} for BUK transistor is 3.5mA.

$$I_{drive} = \frac{C_{gs}\Delta V_{gs}}{t}$$

As discussed in the above part, the gate driving current for BUK transistor needs to be as large as 3.5mA, this value is far larger than the required quiescent current. In this product, the quiescent current needs to be below 10μA, which means the controller must have current amplification ability. This huge difference between quiescent current and driving current requirement gives the motivation to use the class AB stage in the controller [14]. There are two implementation options for class AB stage, common source configuration and common drain configuration. This is shown in Figure 6-9:



(a) Common drain configuration (b) Common source configuration

Figure 6-9 common drain and common source configuration for class AB stage

The advantage of common source configuration is the voltage gain it can provide. The drawback of common source configuration is the larger output impedance and the difficulty on biasing this stage. For now, the common source configuration is preferred to be as a starting point, the biasing technique of common source class AB stage is shown in Figure 6-10.

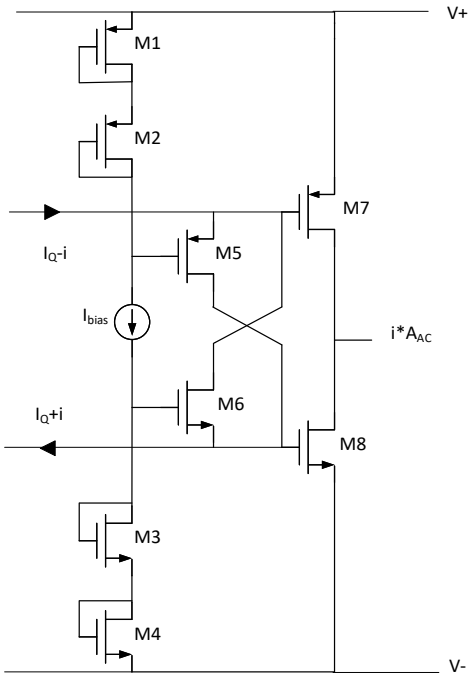


Figure 6-10 Model-based class AB biasing technique

This biasing technique is based on the method named model-based biasing technique, in this biased push-pull stage, M_3, M_4, M_6, M_8 & M_1, M_2, M_5, M_7 are two trans-linear loops, there is equations:

$$V_{gs5} + V_{gs7} = V_{gs1} + V_{gs2}$$

$$V_{gs6} + V_{gs8} = V_{gs3} + V_{gs4}$$

In which V_{gsi} represents the gate source voltage of M_i.

According to the technology used in this design, the supply voltage for the controller is 10V, and the BUK transistor is supplied by the car battery. If the BUK transistor stage is in common source configuration, then the charge pump must provide +5V (power supply for the class AB stage) on top of the output voltage of the regulator. This will cause a difficulty at start-up period. Therefore, the common drain configuration of BUK transistor is selected is this design.

If the impedance of wiring and battery is too large, then the proper implementation of BUK transistor's common drain configuration can be influenced. In order to solve this problem, an AC decoupling capacitor C_{dec} is added as Figure 6-11 shows, C_{dec} should be large enough to reduce this effect, and the value of this AC decoupling capacitor can be decided after the simulation in Chapter 8.

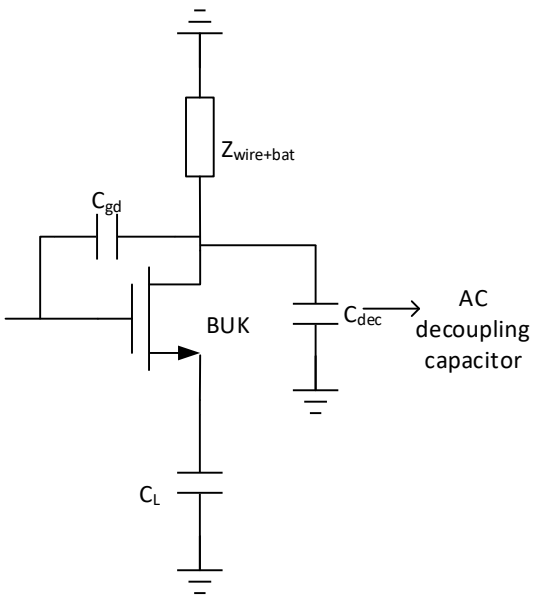


Figure 6-11 Schematic of AC decoupling capacitor implementation

With the input differential pair as first stage, the common source class AB stage as second stage, and the common drain BUK transistor as third stage, the structure of this voltage regulator can be decided as shown in Figure 6-12.

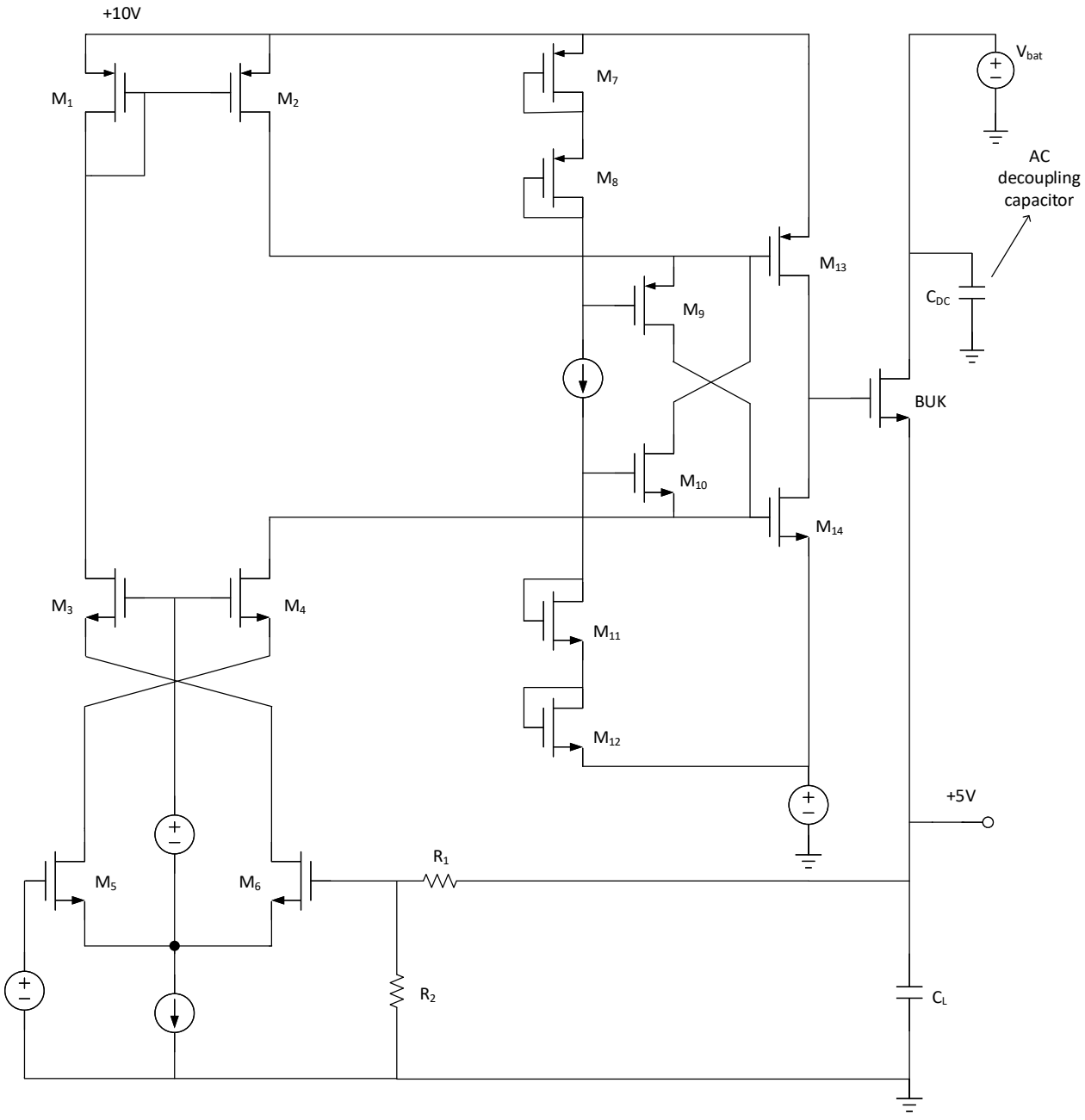


Figure 6-12 Schematic of voltage regulator before frequency compensation

In this design, the input pair transistors (M_5 and M_6) are low voltage transistors for better matching. The cascode transistors (M_3 and M_4) are there to increase the output impedance of this stage. M_1 and M_2 implement -1 current gain. M_7 to M_{12} are biasing transistors for class AB stage. M_9 and M_{10} can be considered as common gate stages to drive the output transistors of the class AB stage. M_{13} and M_{14} are the sourcing and sinking transistor in class AB stage, respectively.

For this voltage regulator, the test cases of load current step variation can be from 10µA to 250mA or from 250mA to 10µA. However, the external BUK transistor is only able to source current to the load,

which means when the load current suddenly reduces to 10μA from 250mA, the BUK transistor current and load current difference will charge the load capacitor, making the output voltage higher than the nominal value. In this scenario, the output voltage reduces only by the discharging path composed by R_1+R_2 and C_L, Since R_1, R_2, C_L are all in relative large values. The discharging time constant can be quite long (τ = 0.43s in this design).

To solve this problem, a current sink path should be added, the current sink circuit should be active only when the load current varies from high to low. In other cases, the current sink path should not draw any quiescent current from the voltage regulator. Figure 6-13 shows one possible current sink path solution. The node connected to the gate of BUK is named as IN_{BUK}, the common node of feedback resistor R_1 and R_2 is named IN_{diff}. The detailed implementation of this current sink path is discussed in Section 7.6.

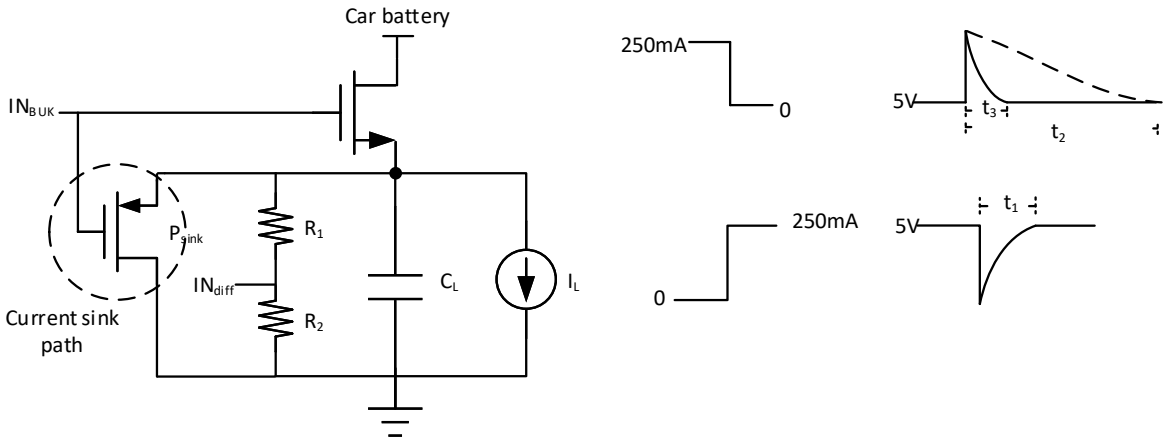


Figure 6-13 one possible solution of current sink path

In a sudden decrease of the load current, t_2 in Figure 6-13 shows the settling time without current sink path, t_3 shows the settling time with current sink path.

7 Detailed design

7.1 Transistor sizing in class AB stage

As shown in Section 6.3, the class AB stage should be capable of sourcing or sinking 3.5mA to the BUK transistor. For the best speed, the transistors in class AB stage should be as small as possible but kept large enough to supply the sourcing and sinking current within the available drive voltage range.

Leaving some headroom for driving current, the size of transistors with which can supply 3.5mA current in 3.3V gate source voltage are selected.

The gate-source voltage versus drain current plots of properly biased M_7 and M_8 (refer to figure 6-10) are shown in Figure 7-1 and Figure 7-2, M_7 is the PMOS sourcing FET in class AB, M_8 is the NMOS sinking FET in class AB stage:

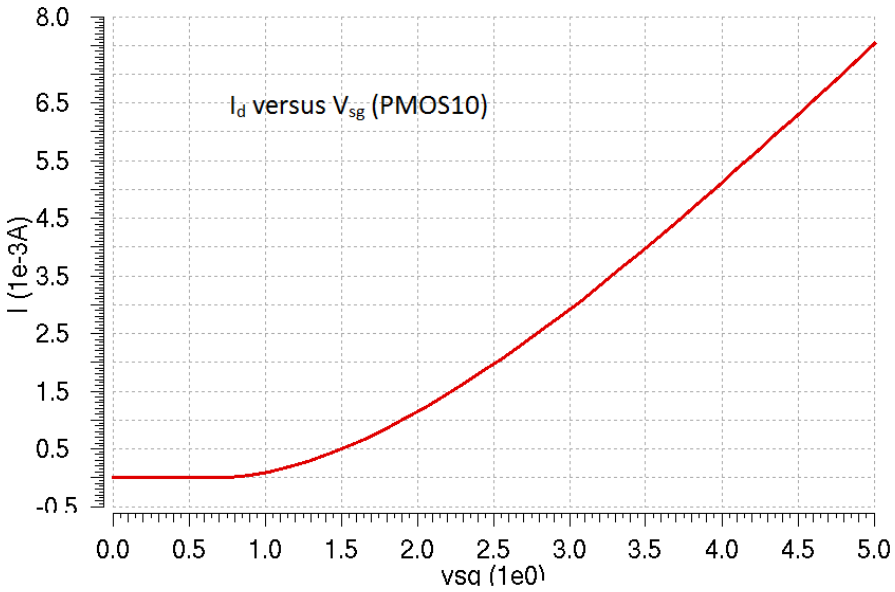


Figure 7-1 I_d vs V_{sg} of sourcing PMOS in class AB stage

As Figure 7-1 shows, PMOS with width of 45µm and NMOS with width of 15µm can supply enough current with 3.3V gate source voltage, they are qualified candidates for this class AB stage.

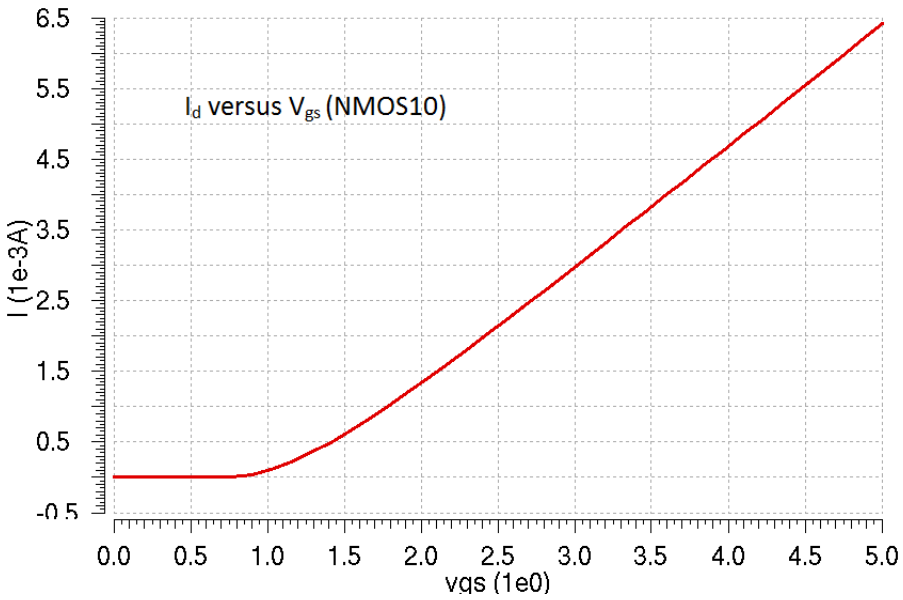


Figure 7-2 I_d vs V_{sg} of sinking NMOS in class AB stage

Moreover, considering the fact that the NMOS and PMOS transistor with minimum width can supply enough driving current for M_7 and M_8, M_5 and M_6 in Figure 6-10 will be designed as minimum size transistor. And according to the trans-linear equation in Section 6.3, the size of M_1, M_2 and M_3, M_4 can be determined. Specifically, M_1 will be designed as the same size with M_7, M_2 will be minimum size transistor. Similarly, M_3 will be designed as the same size with M_8, and M_4 will be the minimum size transistor.

7.2 Small signal analysis

In the previous part, the ideal transfer of this voltage regulator is designed based on the nullor property of the controller, however, the performance of this voltage regulator will be influenced adversely by the non-ideal behavior of the controller. The analysis of this influence is based on the asymptotic gain model [15].

Specifically speaking, the structured design approach followed in this thesis, is essentially a two-steps design approach. There are two steps to design this voltage regulator:

1. The design of the ideal gain.
2. The design of a controller that provides a sufficiently large loop gain over the operating range of interest.

With the asymptotic gain model, the source to load transfer can be written as:

$$A_f = A_{f\infty}\frac{-L}{1-L} + \frac{\rho}{1-L}$$

In which $A_{f\infty}$ is the asymptotic gain value, L is loop gain of the feedback amplifier, ρ is the direct transfer from source to load. The asymptotic gain model is a representation of the gain of negative feedback

amplifiers given by the asymptotic gain relation. In this design, the asymptotic gain model method is chosen as the design method, because it makes the design can be done in two independent steps with properly chosen loop gain reference and it completely characterizes feedback amplifiers, including loading effects and the properties of amplifiers and feedback networks. If the loop gain reference variable is selected properly, hence the asymptotic gain $A_{f\infty}$ equals the ideal gain A_i of a negative feedback amplifier and the source to load transfer can be expressed as:

$$A_f = A_i \frac{-L}{1-L}$$

Where the expression $\frac{-L}{1-L}$ is defined as servo function, which is uniquely defined by the loop gain.

In the following part, we will use the asymptotic gain model to design the high frequency behavior of the regulator. To this end, we need to evaluate the loop gain and the servo function, especially the poles and zeros. This is done with the aid of the small signal equivalent circuit, which is shown in Figure 7-3.

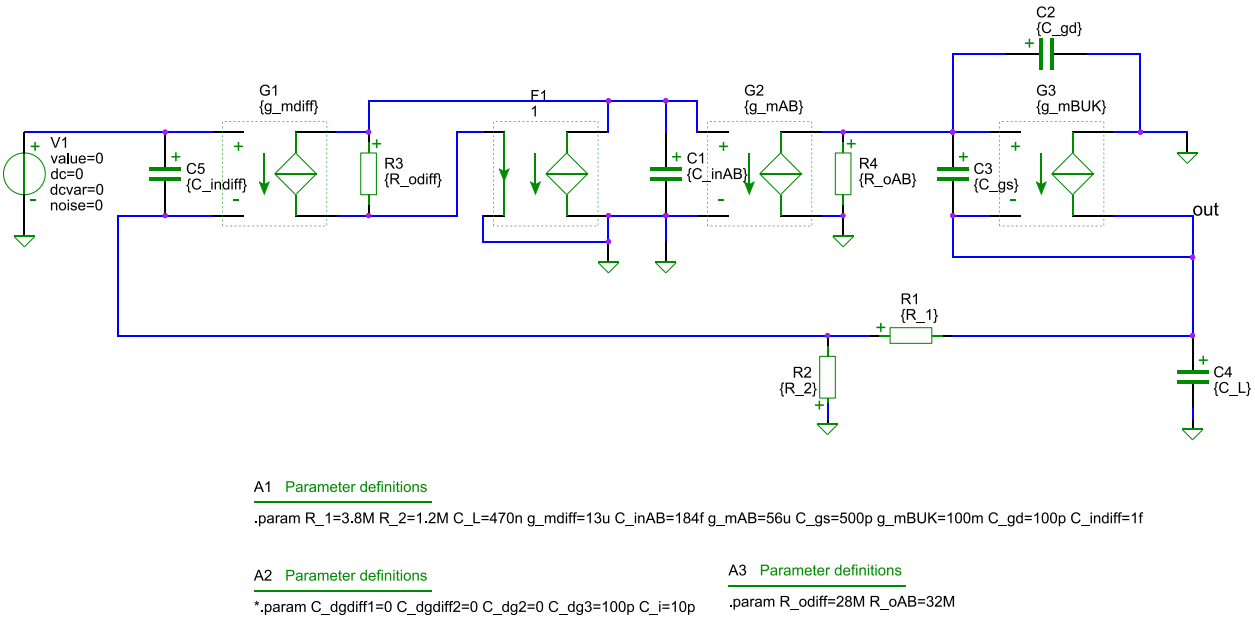


Figure 7-3 Small signal equivalent circuit of voltage regulator

In Figure 7-3, C_{indiff} is the input capacitance of the input differential pair, g_{mdiff} is the trans-conductance of first stage, R_{odiff} is the output resistance of first stage, C_{inAB} is the input capacitance of class AB stage, g_{mAB} is the trans-conductance of the class AB stage, R_{oAB} is the output resistance of class AB stage, C_{gs} is the gate source capacitance of the BUK transistor, C_{gd} is the gate drain capacitance of the BUK transistor, g_{mBUK} is the trans-conductance of the BUK transistor. C_L is the load capacitor, R_1 and R_2 are the feedback resistors.

The practical component parameters are summarized in the table below:

Symbol	Parameter	Symbol	Parameter

g_{mdiff}	13µS	R_{odiff}	28MΩ
C_{inAB}	184fF	g_{mAB}	56µS
R_{oAB}	32MΩ	C_{gs}	500pF
C_{gd}	100pF	g_{mBUK}	100mS
R_1	3.8MΩ	R_2	1.2MΩ
C_{indiff}	1fF	C_L	470nF

Table 7-1 Practical component parameters in small signal equivalent circuit

In Figure 7-3, G_1 is chosen as the loop gain reference, the symbolic loop gain expression is calculated in SLiCAP. The MATLAB codes and the symbolic loop gain expression are shown in Appendix 10.2. In the denominator, the coefficient of the highest order of s is $C_{\mathrm{inAB}}R_{\mathrm{odiff}}(C_LC_{\mathrm{gd}}C_{\mathrm{indiff}}R_1R_2R_{\mathrm{oAB}} + C_LC_{\mathrm{gs}}C_{\mathrm{indiff}}R_1R_2R_{\mathrm{oAB}} + C_{\mathrm{gd}}C_{\mathrm{gs}}C_{\mathrm{indiff}}R_1R_2R_{\mathrm{oAB}})$, which indicates the achievable bandwidth of this voltage regulator is:

$$\sqrt[n]{1/\left(C_{\mathrm{inAB}}R_{\mathrm{odiff}}\left(C_LC_{\mathrm{gd}}C_{\mathrm{indiff}}R_1R_2R_{\mathrm{oAB}} + C_LC_{\mathrm{gs}}C_{\mathrm{indiff}}R_1R_2R_{\mathrm{oAB}} + C_{\mathrm{gd}}C_{\mathrm{gs}}C_{\mathrm{indiff}}R_1R_2R_{\mathrm{oAB}}\right)\right)}$$

Where n is the order number of the negative feedback amplifier.

The numeric values of poles and zeros of loop gain are shown in Table 7-2.

	Real part	Imaginary part	magnitude	Q
P_1	-50.11	0.0	50.11	-
P_2	-5601.0	0.0	5601.0	-
P_3	-61788.0	0.0	61788.0	-
P_4	-1.745e8	0.0	1.745e8	-
Z_1	-3.183e7	0.0	3.183e7	-

Table 7-2 Numeric values of poles and zeros of loop gain

According to the values in Table 7-2, and the value of DC loop gain, which is -1.565e5, this is a third order system, p_4 is a non-dominant pole and Z_1 is a non-dominant zero.

The bandwidth ω_n of a negative feedback amplifier with an n-th order Butterworth characteristic can be obtained as:

$$\omega_n = \sqrt[n]{\left|(1 - L_{DC}) \prod_{i=1}^{n} P_i\right|}$$

In this certain case, the value of L_{DC} is -1.565e5, this negative feedback amplifier is a 3-order amplifier, so the achievable bandwidth is 140 KHz, which is far more than required for a settling time of 1ms.

In order to investigate the high frequency behavior of this voltage regulator in the whole load current range, the transistor level small signal circuit is built, as shown in Figure 7-4. As stated in Chapter 4, the modified EKV model is used in this transistor level equivalent circuit. The modeling procedures and the related physical parameters in the model file of these transistors are shown in Appendix 10.1.

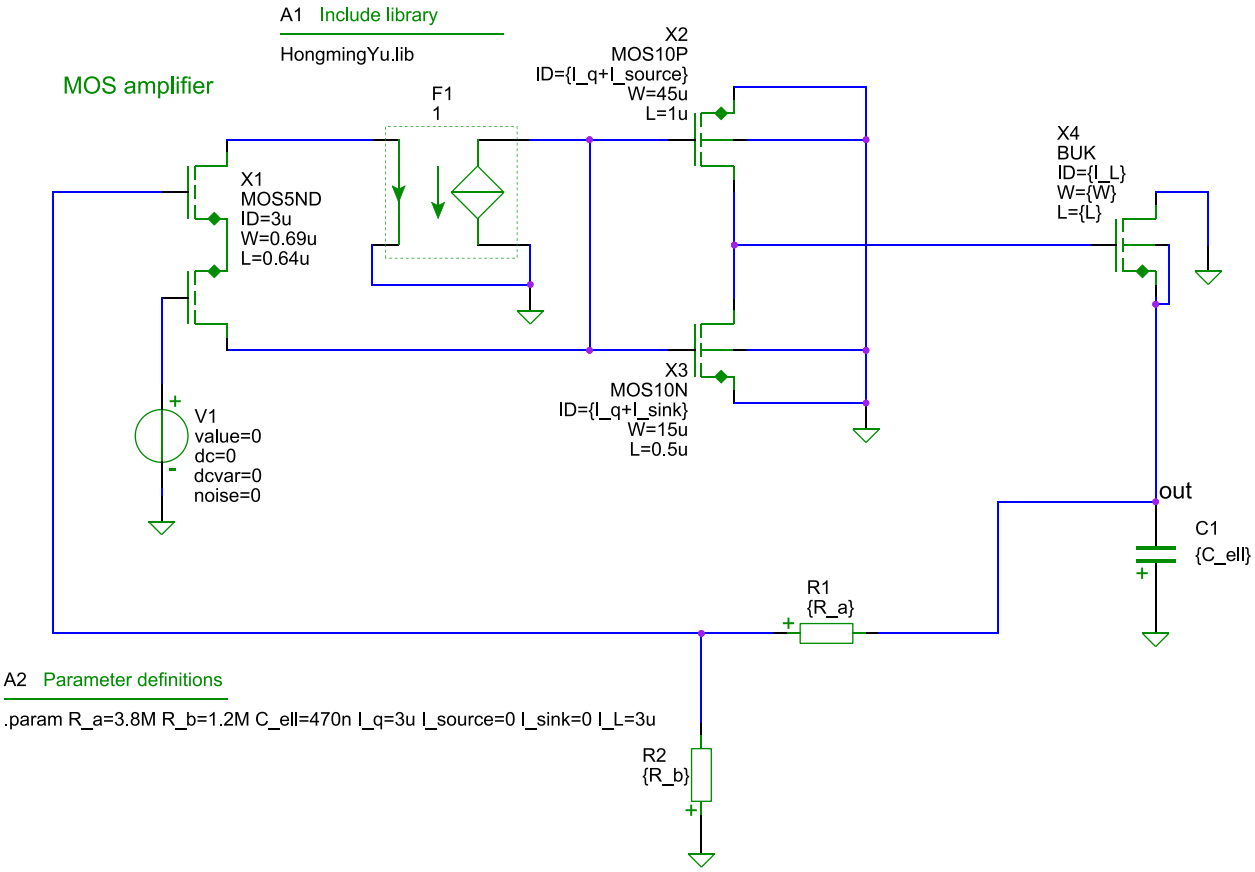


Figure 7-4 Transistor level small signal modeling circuit

The poles movement of this regulator with the load current are shown in Figure 7-5 and Figure 7-6, the stepping range of load current is from 10μA to 250mA.

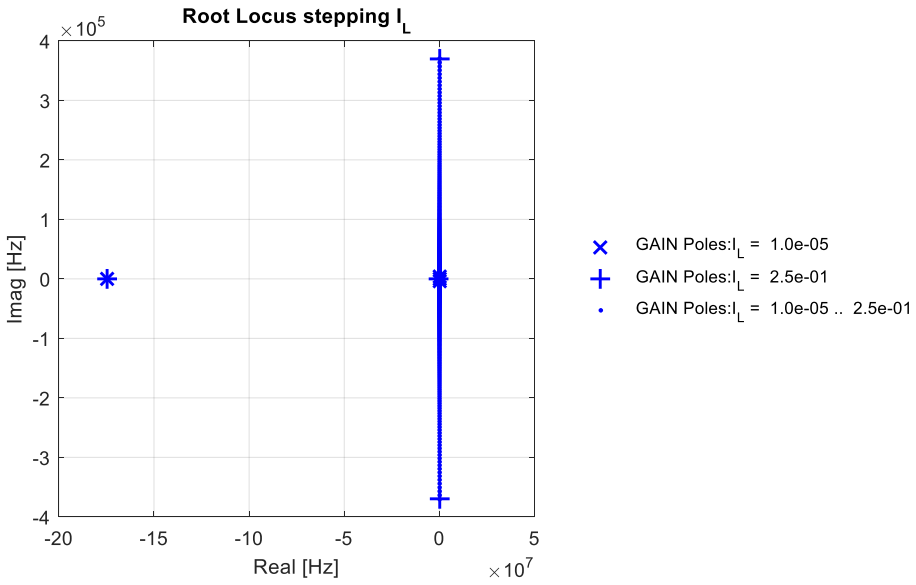


Figure 7-5 Root Locus plot with the load current as the Root Locus variable-1

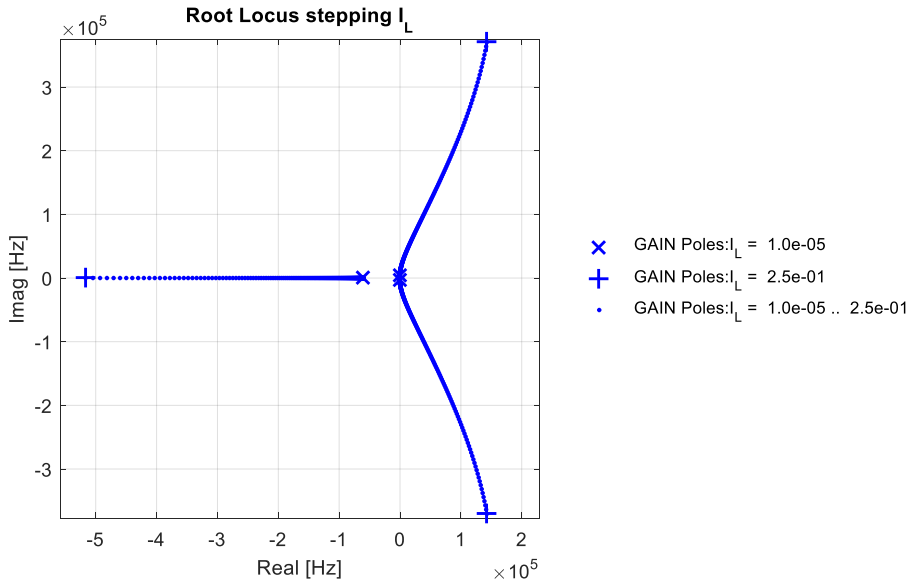


Figure 7-6 Root Locus plot with the load current as the Root Locus variable-2

From Figure 7-5 and Figure 7-6, it can be seen that there are poles moving to RHP with the load current variation, which indicates this voltage regulator is unstable over the interested operating range.

7.3 High frequency compensation

As stated in Chapter 2, the frequency compensation scheme needs to be designed. Principally, this is a negative feedback amplifier with all-pole loop gain, in which there are three poles:

$$L(s) = L_{DC}\frac{1}{(1-\frac{s}{p_1})(1-\frac{s}{p_2})(1-\frac{s}{p_3})}$$

In which L_{DC} is the DC loop gain value. P_1, P_2 and P_3 are three dominant poles in this negative feedback amplifier.

Basically, frequency compensation of this voltage regulator aims to put the poles in Butterworth positions. The dynamic part of a servo function with Butterworth transfer $F_3(s)$ can be written as:

$$F_3(s) = \frac{1}{1+\frac{2s}{\omega_h}+\frac{2s^2}{\omega_h^2}+\frac{s^3}{\omega_h^3}}$$

In which ω_h is the -3dB low pass cut-off frequency.

Then we can know the expression of the servo function is:

$$F_3(s) = \frac{-L_{DC}}{1-L_{DC}}\frac{1}{1-s\frac{p_1p_2+p_1p_3+p_2p_3}{(1-L_{DC})p_1p_2p_3}+s^2\frac{p_1+p_2+p_3}{(1-L_{DC})p_1p_2p_3}-s^3\frac{1}{(1-L_{DC})p_1p_2p_3}}$$

These three poles will be in Butterworth position if:

$$p_1p_2+p_1p_3+p_2p_3 = 2\omega_h^2$$

$$p_1+p_2+p_3 = -2\omega_h$$

Where $\omega_h = \sqrt[3]{|(1-L_{DC})p_1p_2p_3|}$.

Conceptually, this negative feedback loop can be compensated with two phantom zeros. After inserting two phantom zeros in the loop, the transfer function of the loop gain will be:

$$L(s) = L_{DC}\frac{(1-\frac{s}{z_1})(1-\frac{s}{z_2})}{(1-\frac{s}{p_1})(1-\frac{s}{p_2})(1-\frac{s}{p_3})}$$

Now the question for designing is the appropriate value of these two zeros to make the compensation. These three poles will be in Butterworth position if:

$$p_1p_2 + p_1p_3 + p_2p_3 - L_{DC}p_1p_2p_3 = 2\omega_h^2$$

$$p_1 + p_2 + p_3 - \frac{p_1p_2p_3L_{DC}}{z_1z_2} = -2\omega_h$$

where $\omega_h = \sqrt[3]{|(1 - L_{DC})p_1p_2p_3|}$.

Therefore, the values for the product and the sum of the inserting zeros are:

$$z_1z_2 = \frac{\omega_h^3}{p_1 + p_2 + p_3 + 2\omega_h}$$

$$z_1 + z_2 = \frac{p_1p_2 + p_1p_3 + p_2p_3 - 2\omega_h^2}{p_1 + p_2 + p_3 + 2\omega_h}$$

The values of inserting zeros can be calculated from the product and the sum of the inserting zeros:

$$z_1 = \frac{1}{2}(z_1 + z_2) + \frac{1}{2}\sqrt{(z_1 + z_2)^2 - 4z_1z_2}$$

$$z_2 = \frac{1}{2}(z_1 + z_2) - \frac{1}{2}\sqrt{(z_1 + z_2)^2 - 4z_1z_2}$$

With the data of the poles in Table 7-2, the frequency of these two zeros are about 2000(1+j) Hz and 2000(1-j) Hz.

7.3.1 Conceptual compensation with a controlled source

Conceptually, the most straightforward implementation of inserting two zeros is adding a controlled source in the feedback network with a second order differentiating transfer. The values of two zeros can be calculated according to Section 7.2, the position of zeros is 2000(1+j) Hz and 2000(1-j) Hz. Figure 7-7 shows in which way the second order Ideal differentiator (without adding extra poles) is inserted in this negative feedback amplifier.

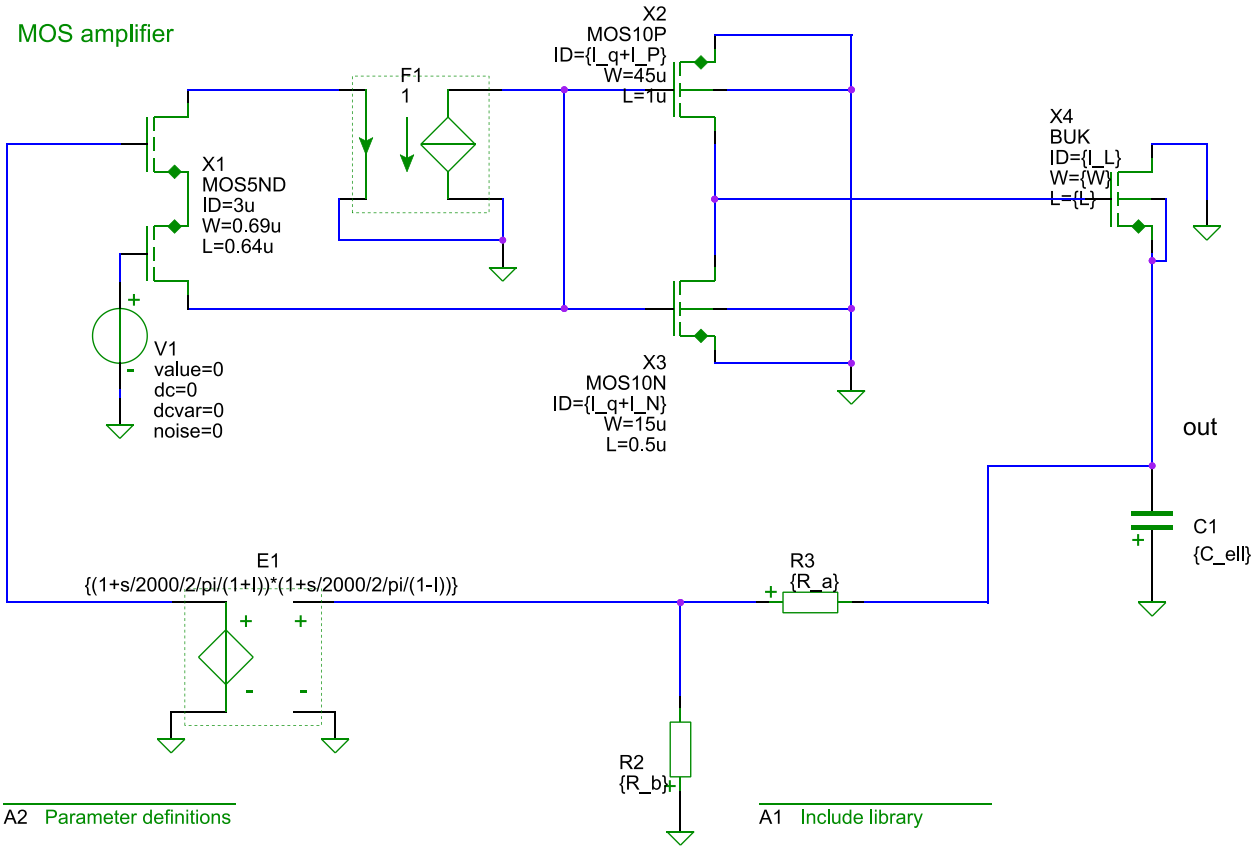


Figure 7-7 Transistor level small signal equivalent modeling circuit with conceptual ideal active compensation

The Root Locus plots with the load current as Root Locus variable are shown in Figure 7-8 and Figure 7-9 for this conceptual phantom zero compensation.

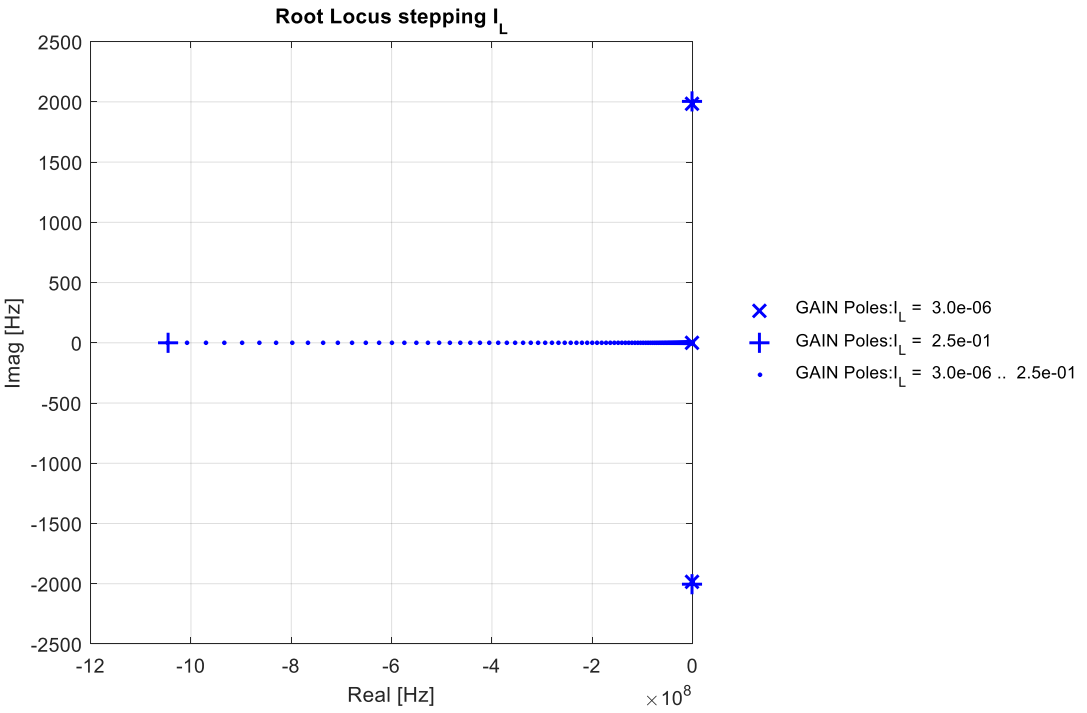


Figure 7-8 Transistor level small signal circuit Root Locus plots with the load current as Root Locus variable-1

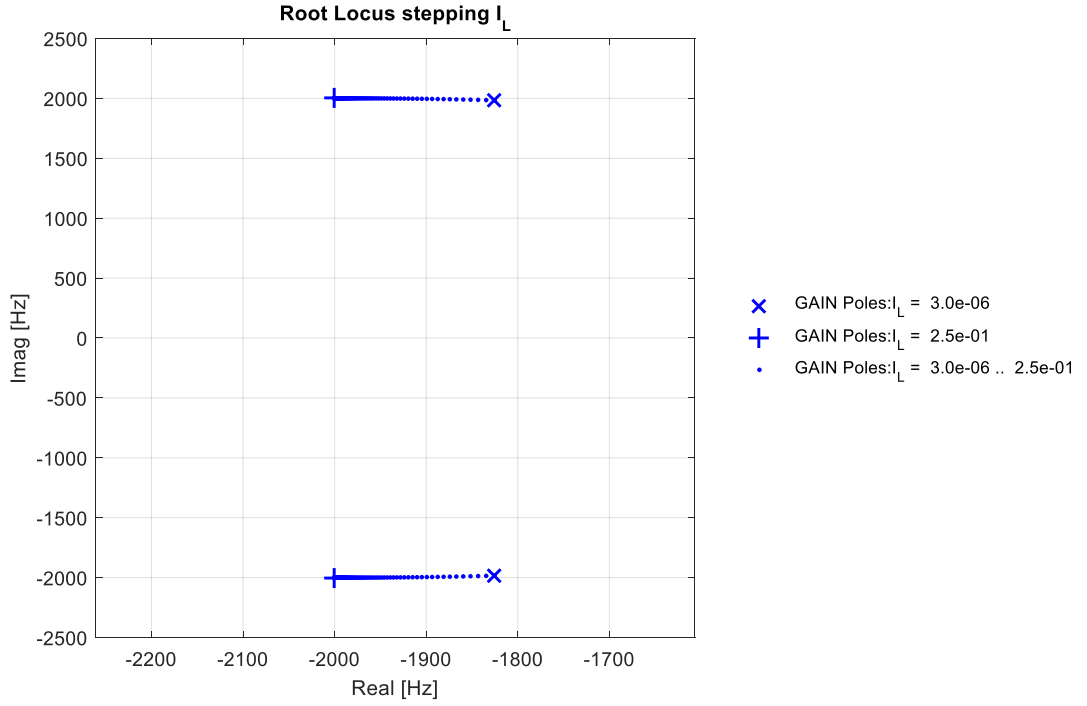


Figure 7-9 Transistor level small signal circuit Root Locus plots with the load current as Root Locus variable-2

From the Root Locus plots with load current as Root Locus variable, it can be seen that the dominant poles are in Butterworth positions after this conceptual compensation. Until now, this active compensation concept has acceptable effectiveness if the variation of sourcing and sinking current in class AB stage is neglected.

In order to further investigate the effectiveness of this active conceptual compensation, the sourcing and sinking current are chosen as Root Locus variables at different certain load current scenario. Because when PMOS in class AB stage sourcing current for BUK transistor, the NMOS in class AB stage is in quiescent scenario, similarly, when the NMOS in class AB sinking current, the PMOS in class AB stage is in quiescent scenario. The variation range of sourcing current and sinking current is from 3µA to 3.5mA.

When the class AB stage is sourcing, the Root Locus plots at different load current with the sourcing current as Root Locus variable are shown in Figure 7-10 and Figure 7-11.

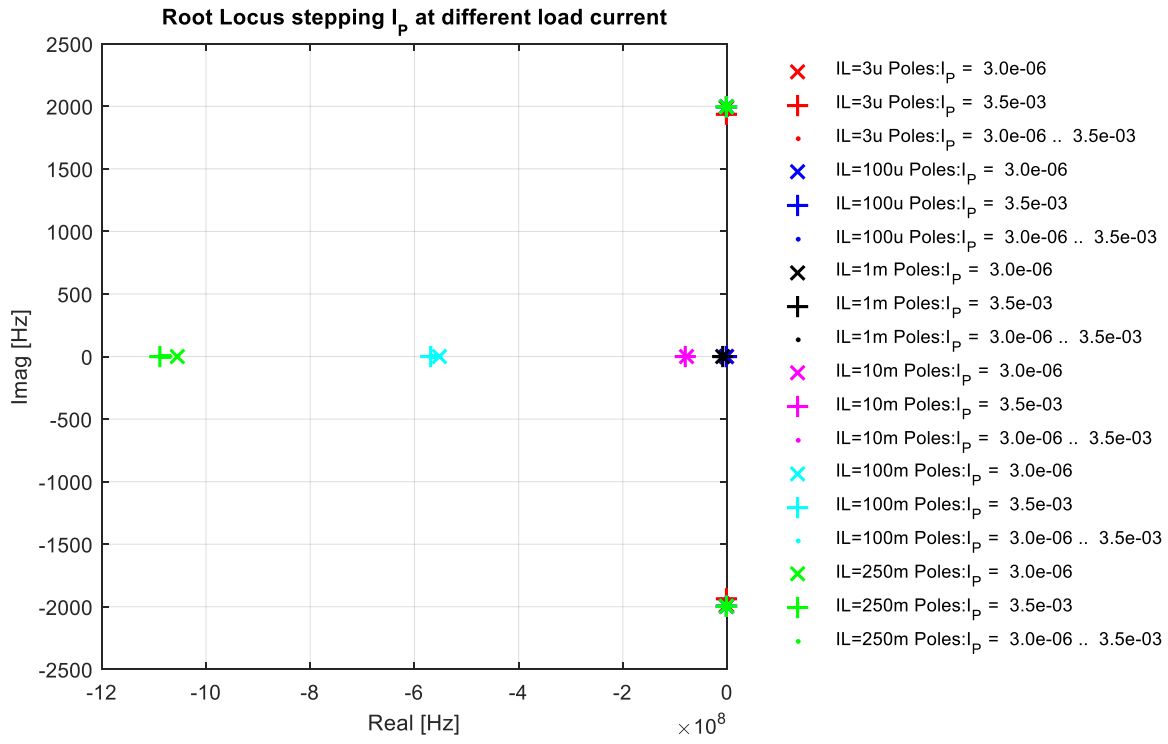


Figure 7-10 Root Locus plots with I_P as Root Locus variable at different load current-1

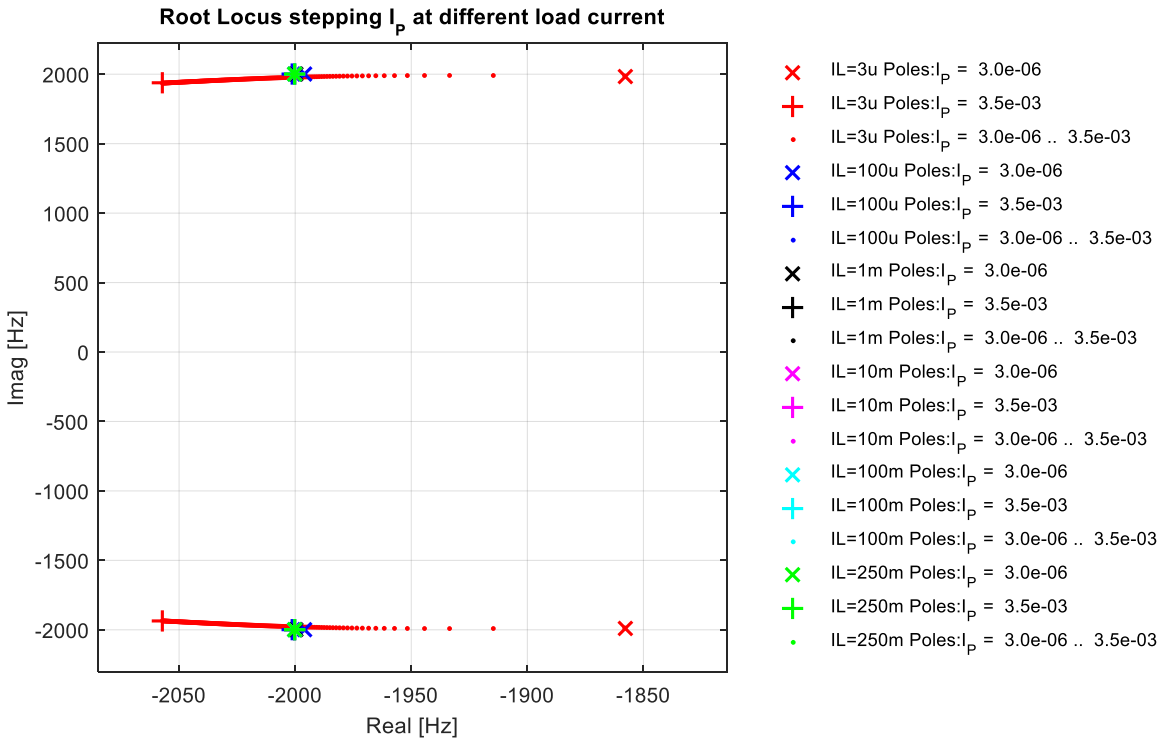


Figure 7-11 Root Locus plots with I_P as Root Locus variable at different load current-2

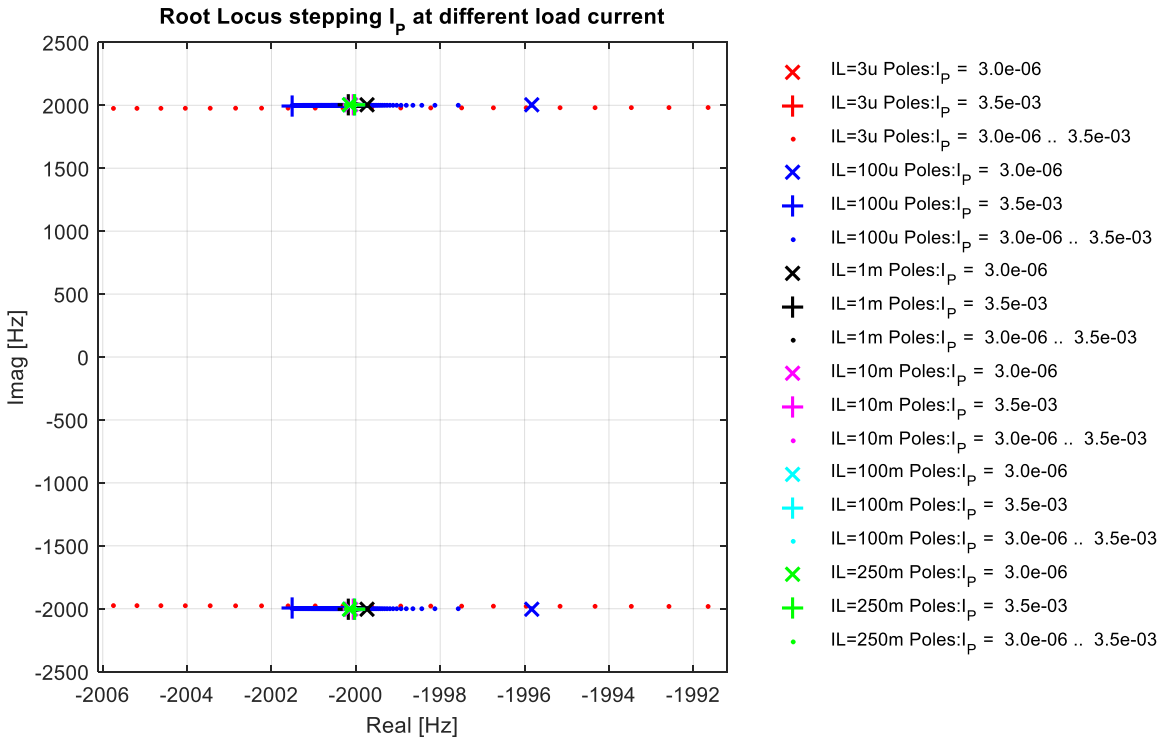


Figure 7-12 Root Locus plots with I_P as Root Locus variable at different load current-3

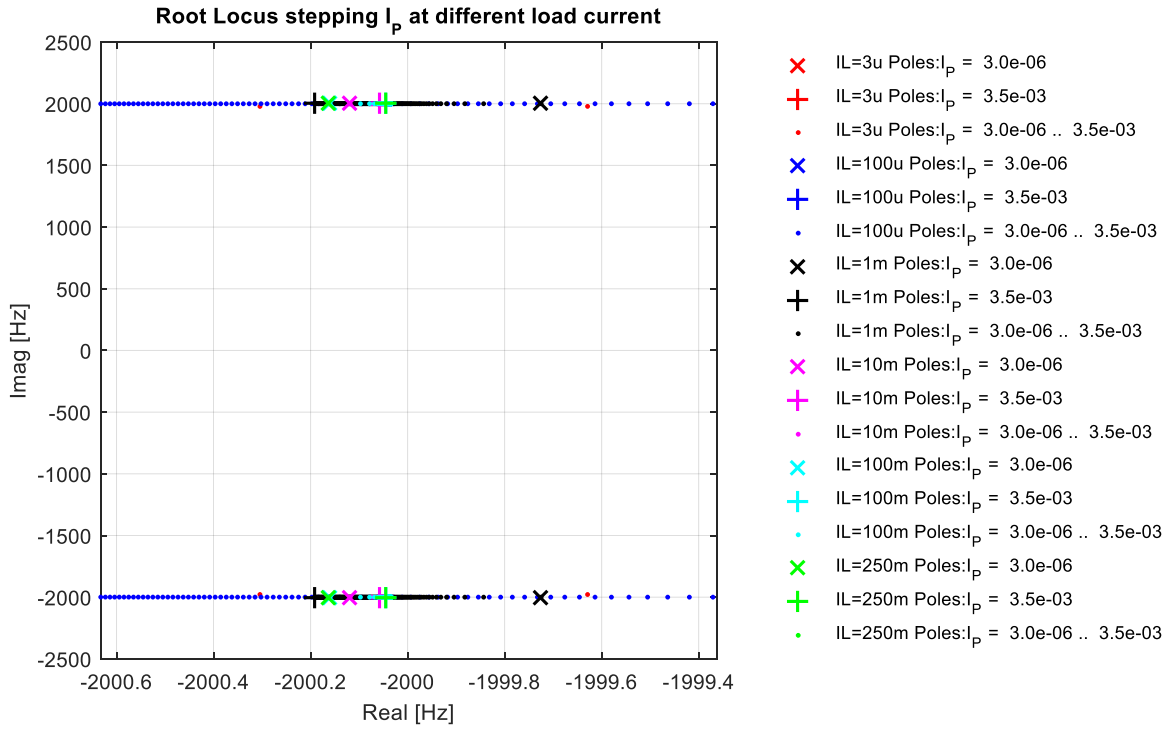


Figure 7-13 Root Locus plots with I_P as Root Locus variable at different load current-4

It can be seen that the active compensation with ideal differentiator, which has no extra poles added, works effectively in the whole load current range.

However, due to natural speed limitations, the implementation of differentiators will add poles thereby reducing the effectiveness of these two zeros. The effect of these additional poles should be verified before implementation.

As explained above, these phantom zeros would result in an infinite gain of those controlled sources for $j\omega \rightarrow \infty$, which is unphysical. At least three poles need to be added in the loop associated with two phantom zeros in differentiator implementation. We can assume the situation that these three poles are on the positions around 100MHz to test the feasibility of real differentiator compensation implementation. The schematic of this situation is shown in Figure 7-14, the transfer function change is made in the voltage controlled voltage source:

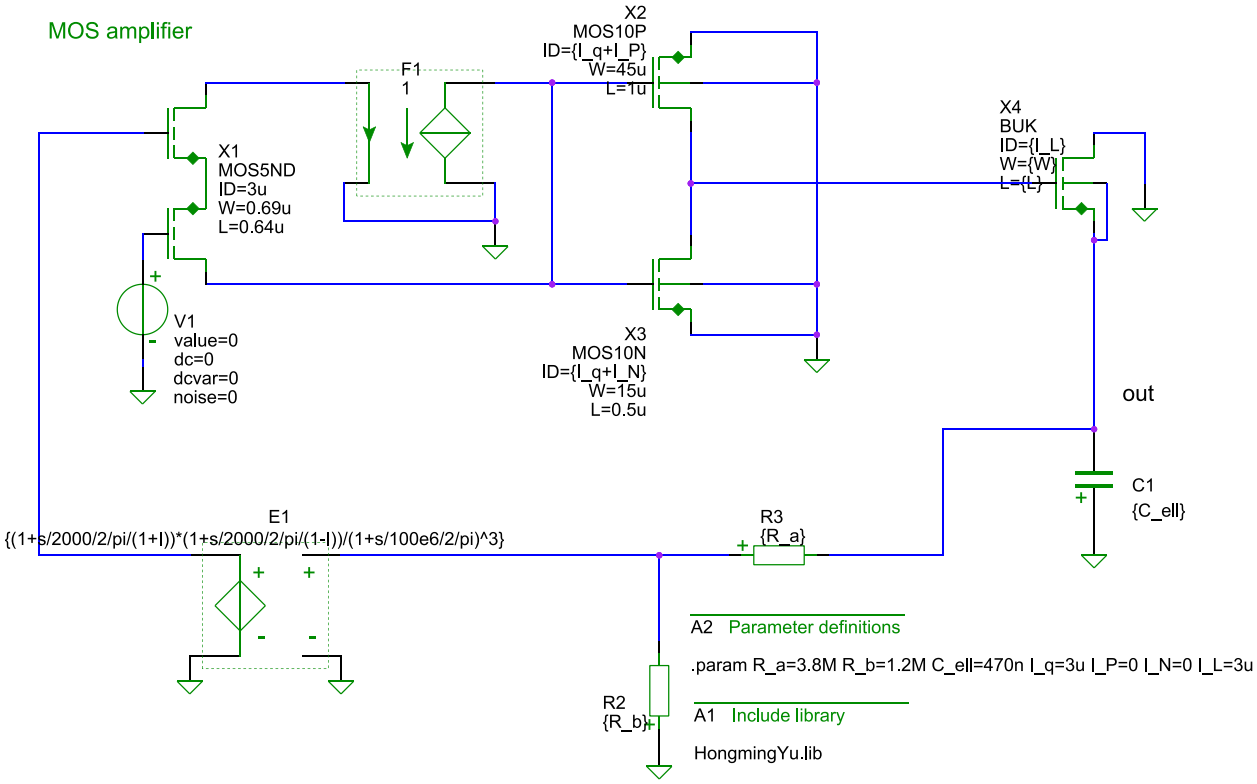


Figure 7-14 Transistor level small signal equivalent modeling circuit with conceptual non-ideal active compensation

The feasibility of this non-ideal active compensation scheme can be investigated further by Root Locus plots with the load current as the Root Locus variable. The Root Locus plots are shown in Figure 7-15.

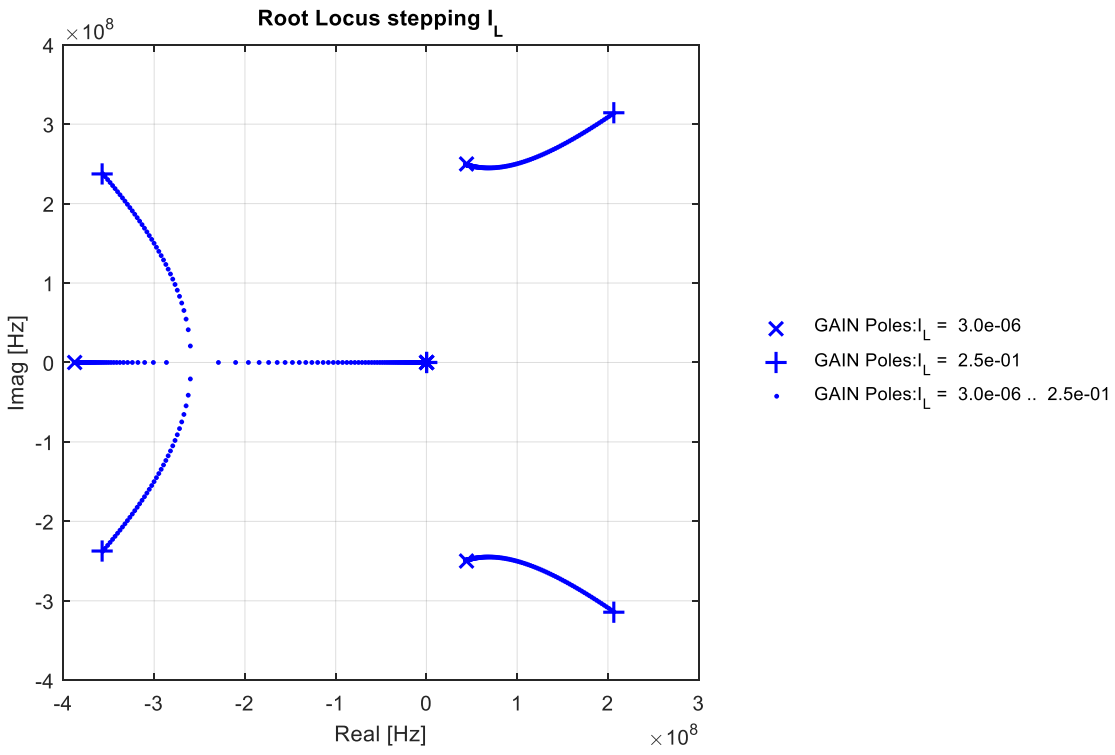


Figure 7-15 Root Locus plots with load current as Root Locus variable when the conceptual non-ideal active compensation implemented

It can be seen that this active compensation cannot be implemented. In the next Section, we will investigate other compensation techniques.

7.4 Compensation with passive components

As stated before, the active frequency compensation is not realistic in this design. Furthermore, in this negative feedback amplifier, the only possible location to generate complex zero passively is in the load. The implementation method is to put an inductor and a resistor in series with the load capacitor. However, the values of inductor and resistor will be out of the acceptable range if we want to have complex zero in the desired frequency, for example, the inductor value will be 0.266Hs and the resistor will be 1.06kΩ if the complex zero located at $2000(1\pm j)$Hz is demanded for frequency compensation.

If we are not aiming to the Butterworth characteristic of poles, then another straightforward method to make the regulator stable is adding two real phantom zeros in the loop. This method can be implemented by generating a phantom zero in the feedback network and another zero in the load. However, this turns out to be not effective enough because it is impossible to keep the regulator stable over the huge load current range. The implementation method of inserting two real phantom zeros is shown in Figure 7-16.

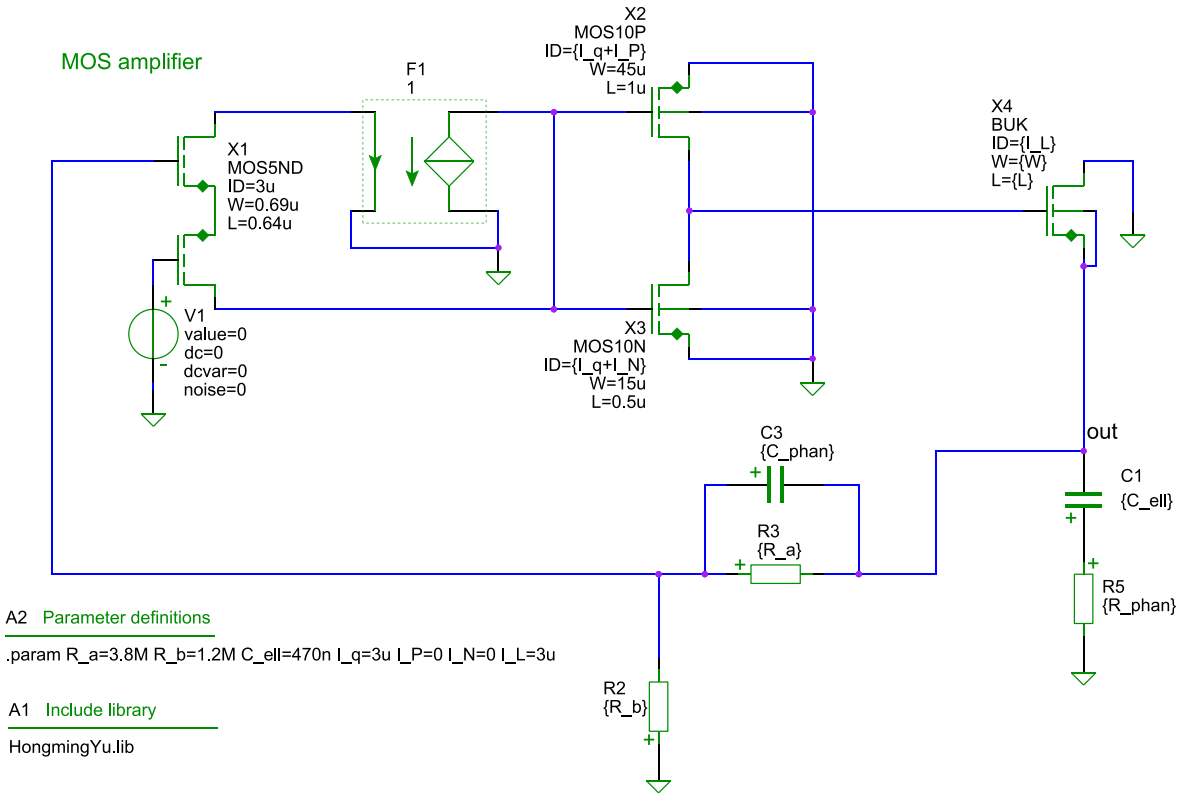


Figure 7-16 Small signal equivalent modeling circuit with two real phantom zeros implementation

From the Root Locus plots with load current as Root Locus variable, which are shown in Figure 7-17 and Figure 7-18, the method of inserting two phantom zeros is not capable of stabilizing this voltage regulator.

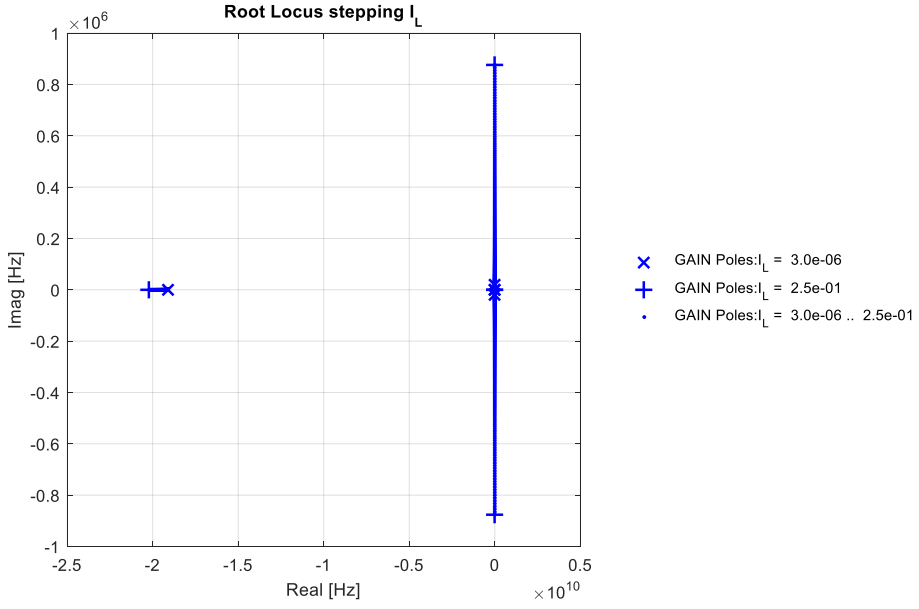


Figure 7-17 Root Locus plot with load current as the Root Locus variable of two real phantom zeros implementation-1

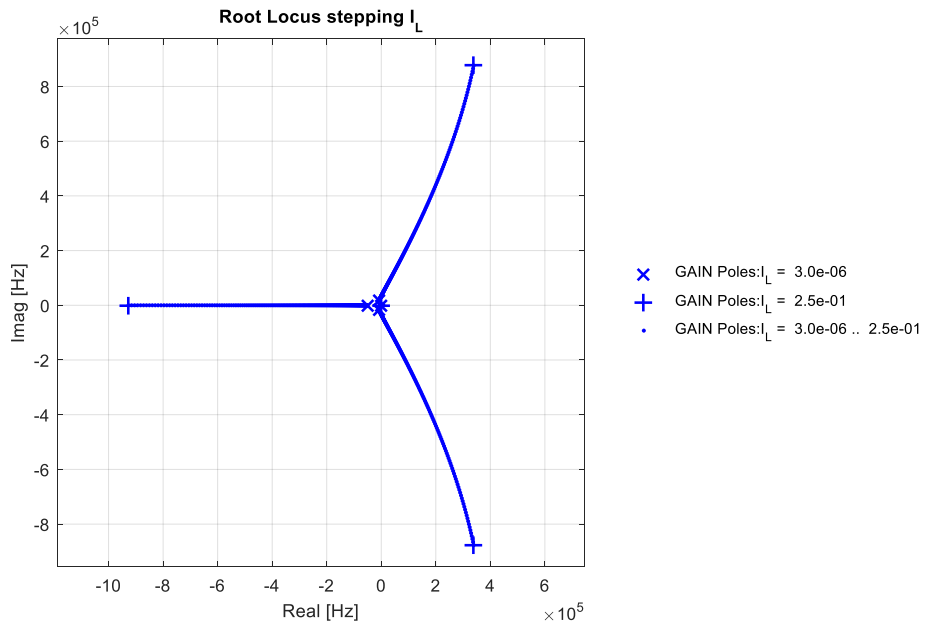


Figure 7-18 Root Locus plot with load current as the Root Locus variable of two real phantom zeros implementation-2

Basically, the BUK transistor stage can be seen as a voltage follower. In order to deal with many poles and their locations variation in this circuit (both dominant and non-dominant poles), a compensation method called Nested loop control seems a more promising approach for this design [16].

The idea of Nested loop control is to construct the controller from local feedback stages that have a well-designed frequency behavior. A classical PID controller can be seen as a form of Nested loop control [17].

As Figure 7-19 shows, we can turn the Amplifier (Amp) into an integrator by adding the capacitor C_{int}, while the common drain BUK stage can be regarded as a local feedback voltage follower. A stable regulator may be obtained in this way because the controller in this case is a single pole one. However, the loop gain of this BUK stage is not very large at low load currents. Hence, its pole may still be dominant.

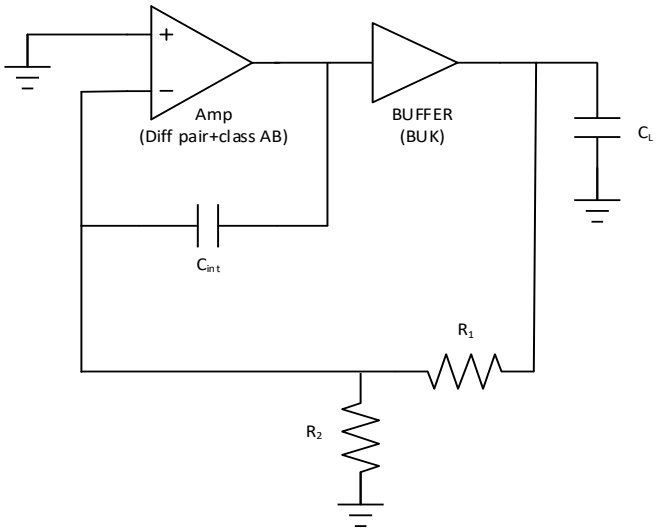


Figure 7-19 Schematic diagram of the integrator configuration

Because the loop gain of the BUK stage is limited, there is capacitive load for the integrator (apart from C_{gd}). We can establish a phantom zero both in the integrator and in the BUK stage by inserting a series resistor between the output of the integrator and the input of the BUK stage. This has been shown in Figure 7-20. This resistor:

1. Creates some degree of freedom to use C_{gd} as a compensation capacitor. This has been illustrated in Figure 7-20.
2. Isolates the BUK from the integrator.
3. Improves the stability of the integrator

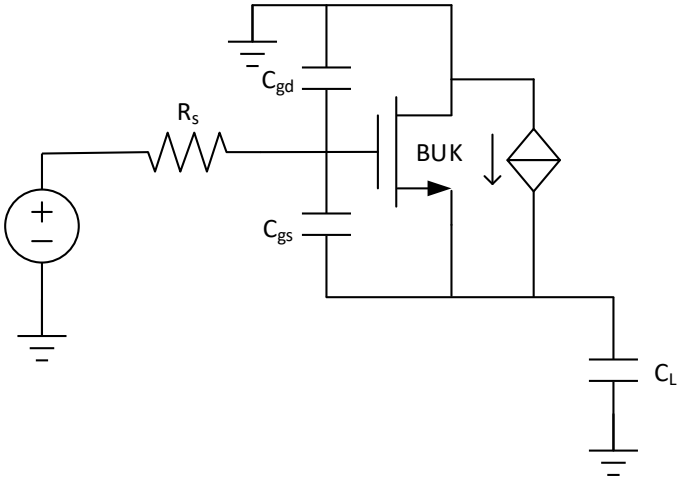


Figure 7-20 Schematic diagram of adding R_s

Point 2 and 3 have been illustrated in Figure 7-21, Z_L represents the load of the integrator, which is capacitive. The existence of R_s isolates the complex capacitive load and also creates a phantom zero in the integrator.

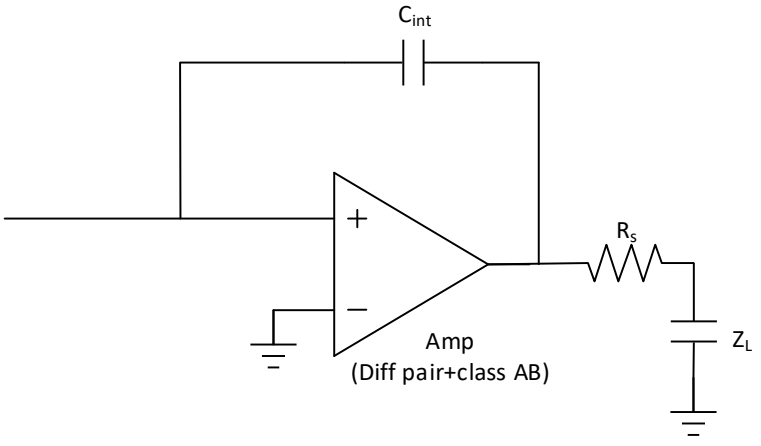


Figure 7-21 The implementation of R_s

In order to determine the value of R_s, the Root Locus analysis with R_s as Root Locus variable has been performed. The Figure 7-22 and Figure 7-23 are the Root Locus plots when the load current is 10μA, the Figure 7-24 and Figure 7-25 are the Root Locus plots when the load current is 250mA.

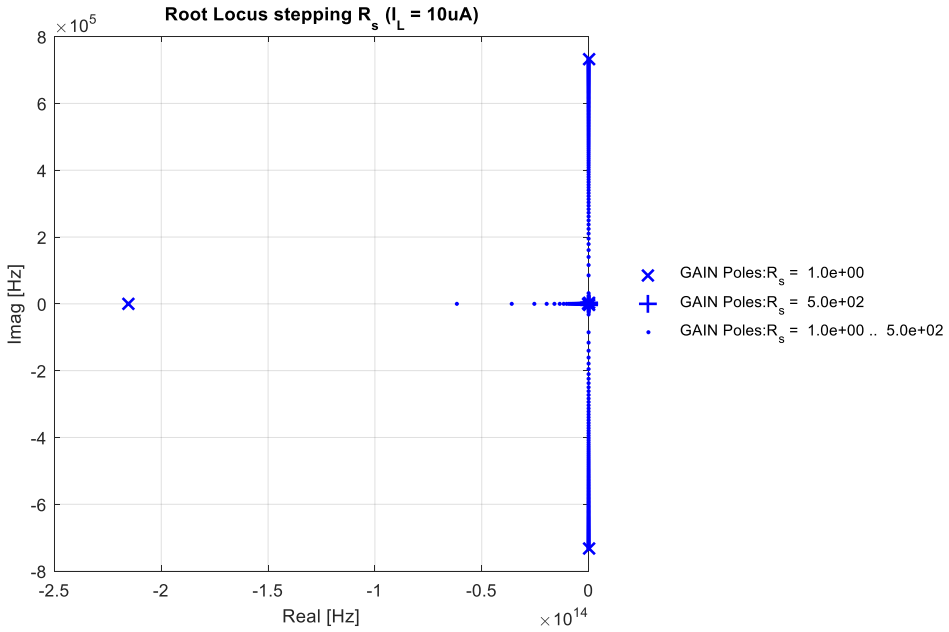


Figure 7-22 Root Locus plot with R_s as Root Locus variable when the load current is 10μA-1

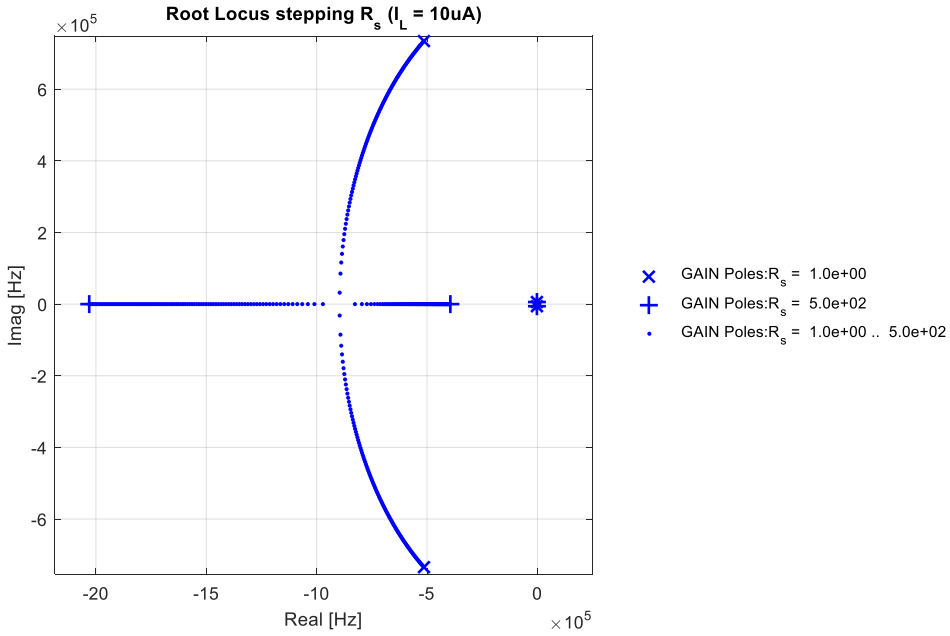


Figure 7-23 Root Locus plot with R_s as Root Locus variable when the load current is 10μA-2

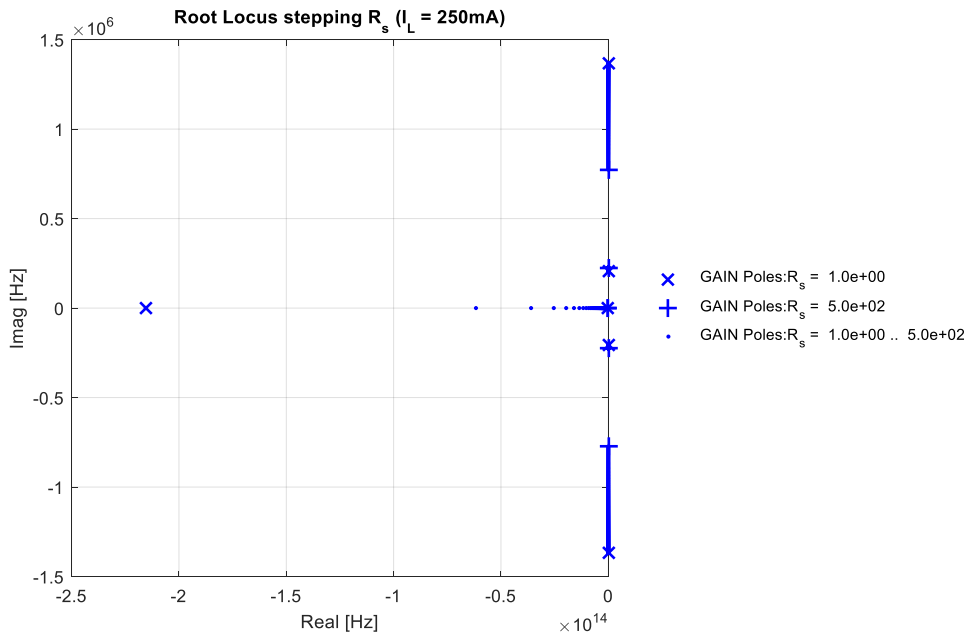


Figure 7-24 Root Locus plot with R_s as Root Locus variable when the load current is 250mA-1

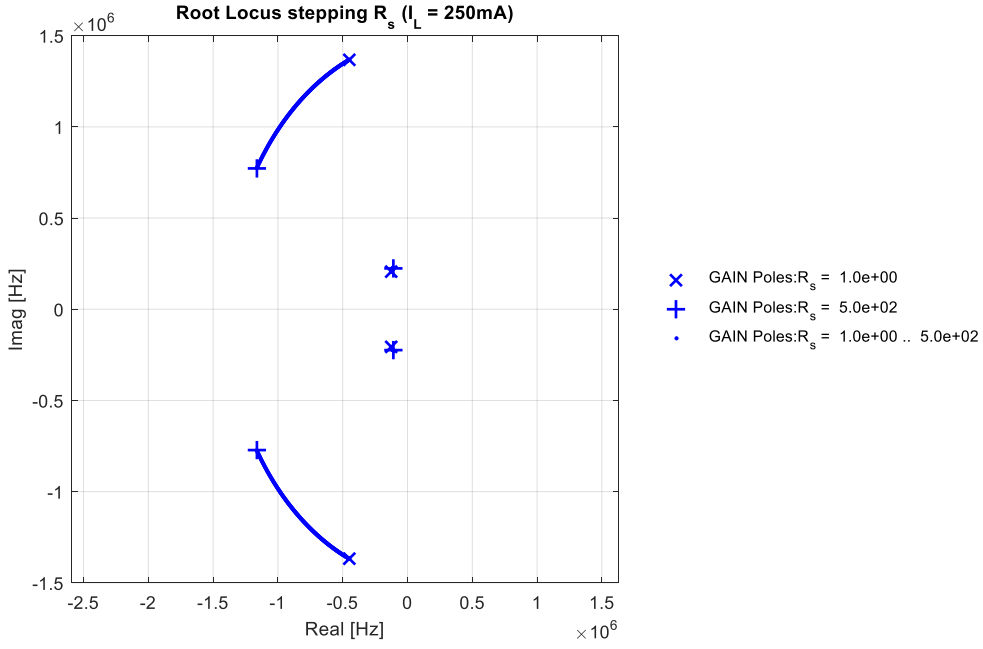


Figure 7-25 Root Locus plot with R_s as Root Locus variable when the load current is 250mA-2

From Figure 7-24 and Figure 7-25, the value of the resistor R_s is determined as 200Ω because the position of dominant poles will be manipulated into Butterworth position when R_s is around 200Ω.

As Figure 7-26 shows, according to the transfer of an integrator, a load step will result in a slope signal driving the BUK transistor. The BUK transistor might not be able to correct this load step fast enough. This problem can be solved by speeding up the integrator. There are basically two methods for improvement:

1. Make the value of the feedback resistors smaller to have smaller time constant of the integrator.
2. Put the series capacitor and resistor in parallel with R_1 to have fast enough response without turning non-dominant poles into dominant poles.

The method 1 is not a good candidate because of the quiescent current requirement, the method 2 is applied in this design.

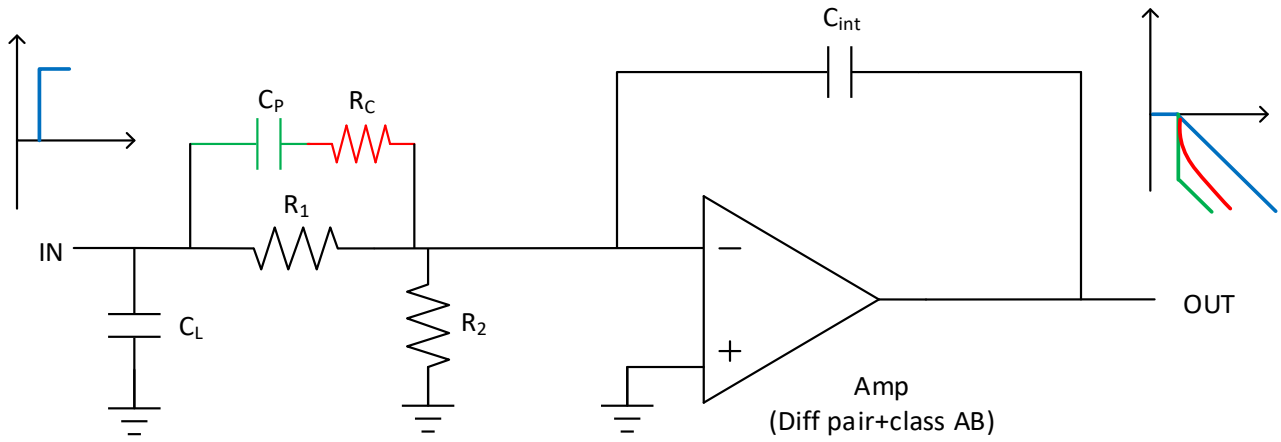


Figure 7-26 Schematic diagram of modified implementation of the integrator configuration

In order to have as fast response as possible, the value of C_P will be designed as large as possible. The C_P implements a phantom zero in the overall loop. It increases the high frequency loop gain thereby possibly converting non-dominant poles into dominant ones. This adverse effect of C_P can be prevented by inserting R_C in series with C_P. The value of R_C will be designed as small as possible, such as to keep the voltage regulator stable. The optimized value of C_P and R_C are found as 0.5pF and 50kΩ based on the Root Locus technique.

Actually, the current sensing resistor introduced in over current protection Section is also helping the frequency behavior by limiting the variation of the trans-conductance of the BUK transistor. The complete circuit of this passive compensation scheme is shown in Figure 7-27.

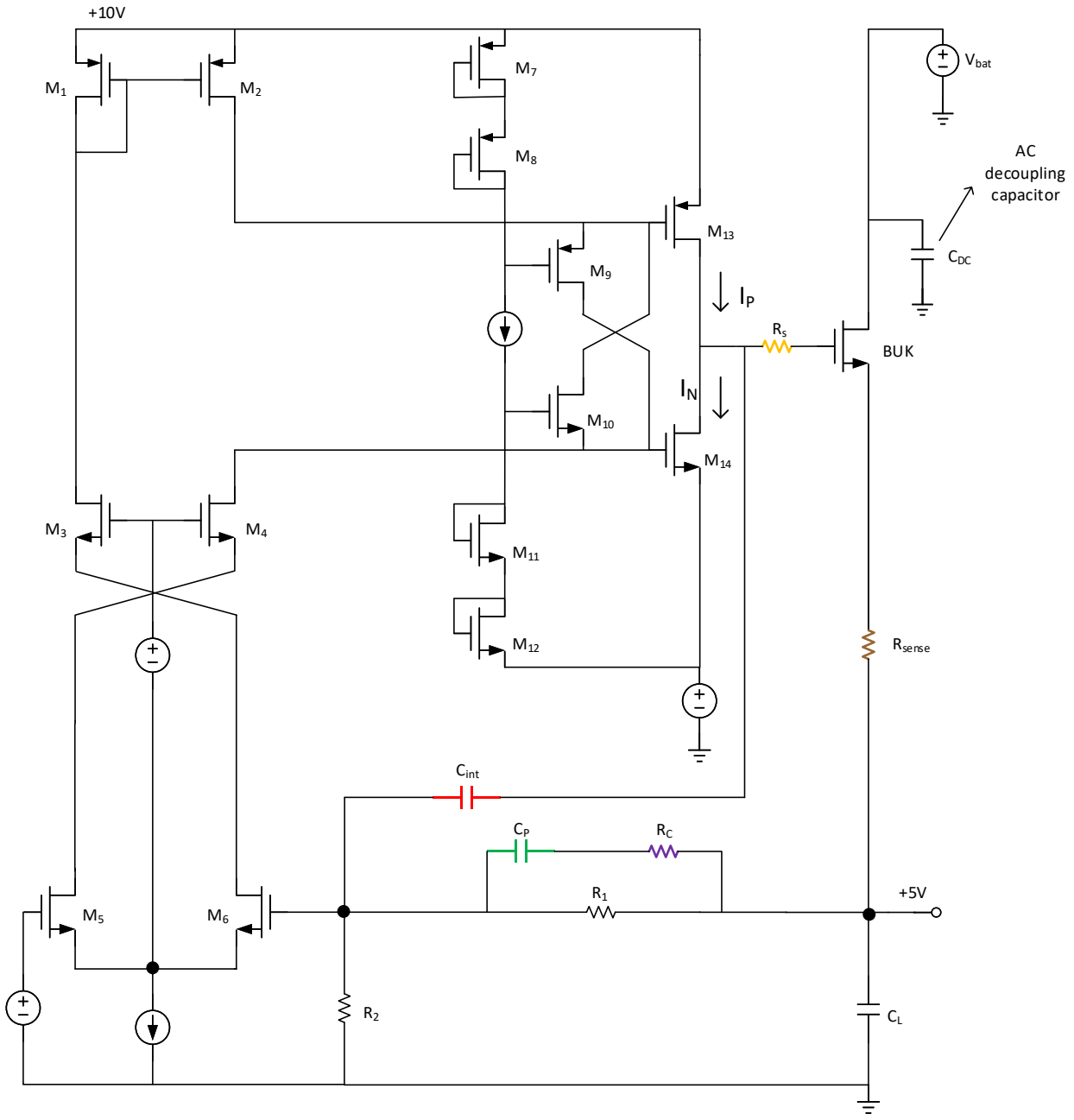
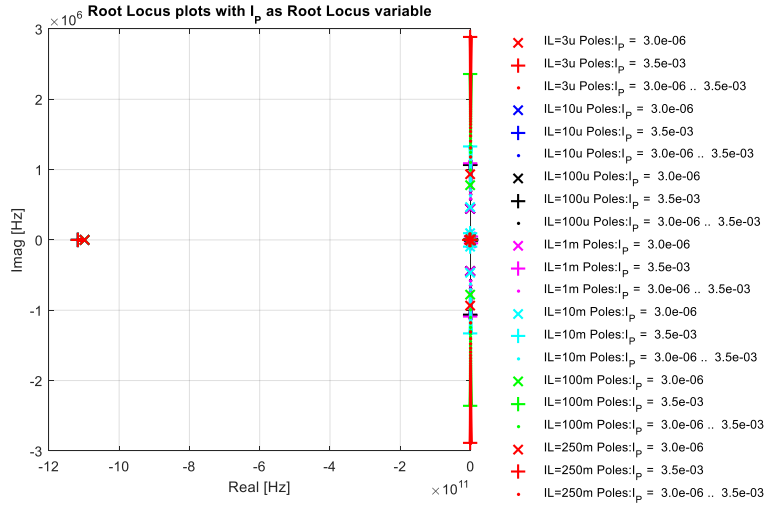
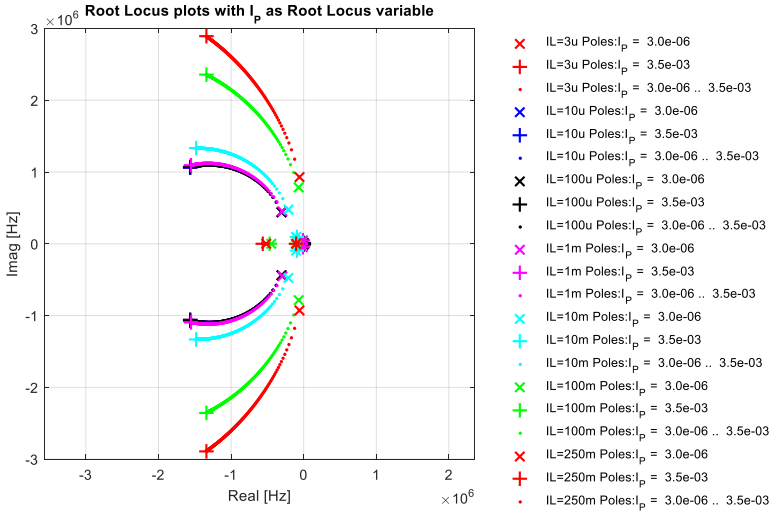
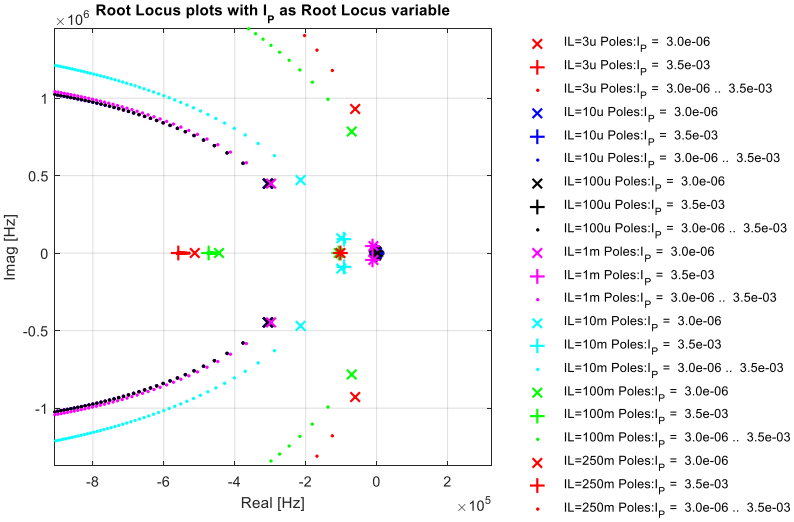


Figure 7-27 the complete circuit of this passive compensation scheme

As Figure 7-28 and Figure 7-29 show, the effectiveness of this passive compensation can be verified by the Root Locus plots with the sourcing current I_P and the sinking current I_N as the Root Locus variable at different load current scenarios.


Root Locus plots with I_P as Root Locus variable
×10^6
Imag [Hz]
Real [Hz]
×10^11
IL=3u Poles:I_P = 3.0e-06
IL=3u Poles:I_P = 3.5e-03
IL=3u Poles:I_P = 3.0e-06 .. 3.5e-03
IL=10u Poles:I_P = 3.0e-06
IL=10u Poles:I_P = 3.5e-03
IL=10u Poles:I_P = 3.0e-06 .. 3.5e-03
IL=100u Poles:I_P = 3.0e-06
IL=100u Poles:I_P = 3.5e-03
IL=100u Poles:I_P = 3.0e-06 .. 3.5e-03
IL=1m Poles:I_P = 3.0e-06
IL=1m Poles:I_P = 3.5e-03
IL=1m Poles:I_P = 3.0e-06 .. 3.5e-03
IL=10m Poles:I_P = 3.0e-06
IL=10m Poles:I_P = 3.5e-03
IL=10m Poles:I_P = 3.0e-06 .. 3.5e-03
IL=100m Poles:I_P = 3.0e-06
IL=100m Poles:I_P = 3.5e-03
IL=100m Poles:I_P = 3.0e-06 .. 3.5e-03
IL=250m Poles:I_P = 3.0e-06
IL=250m Poles:I_P = 3.5e-03
IL=250m Poles:I_P = 3.0e-06 .. 3.5e-03


Root Locus plots with I_P as Root Locus variable
×10^6
Imag [Hz]
Real [Hz]
×10^6
IL=3u Poles:I_P = 3.0e-06
IL=3u Poles:I_P = 3.5e-03
IL=3u Poles:I_P = 3.0e-06 .. 3.5e-03
IL=10u Poles:I_P = 3.0e-06
IL=10u Poles:I_P = 3.5e-03
IL=10u Poles:I_P = 3.0e-06 .. 3.5e-03
IL=100u Poles:I_P = 3.0e-06
IL=100u Poles:I_P = 3.5e-03
IL=100u Poles:I_P = 3.0e-06 .. 3.5e-03
IL=1m Poles:I_P = 3.0e-06
IL=1m Poles:I_P = 3.5e-03
IL=1m Poles:I_P = 3.0e-06 .. 3.5e-03
IL=10m Poles:I_P = 3.0e-06
IL=10m Poles:I_P = 3.5e-03
IL=10m Poles:I_P = 3.0e-06 .. 3.5e-03
IL=100m Poles:I_P = 3.0e-06
IL=100m Poles:I_P = 3.5e-03
IL=100m Poles:I_P = 3.0e-06 .. 3.5e-03
IL=250m Poles:I_P = 3.0e-06
IL=250m Poles:I_P = 3.5e-03
IL=250m Poles:I_P = 3.0e-06 .. 3.5e-03


Root Locus plots with I_P as Root Locus variable
×10^6
Imag [Hz]
Real [Hz]
×10^5
IL=3u Poles:I_P = 3.0e-06
IL=3u Poles:I_P = 3.5e-03
IL=3u Poles:I_P = 3.0e-06 .. 3.5e-03
IL=10u Poles:I_P = 3.0e-06
IL=10u Poles:I_P = 3.5e-03
IL=10u Poles:I_P = 3.0e-06 .. 3.5e-03
IL=100u Poles:I_P = 3.0e-06
IL=100u Poles:I_P = 3.5e-03
IL=100u Poles:I_P = 3.0e-06 .. 3.5e-03
IL=1m Poles:I_P = 3.0e-06
IL=1m Poles:I_P = 3.5e-03
IL=1m Poles:I_P = 3.0e-06 .. 3.5e-03
IL=10m Poles:I_P = 3.0e-06
IL=10m Poles:I_P = 3.5e-03
IL=10m Poles:I_P = 3.0e-06 .. 3.5e-03
IL=100m Poles:I_P = 3.0e-06
IL=100m Poles:I_P = 3.5e-03
IL=100m Poles:I_P = 3.0e-06 .. 3.5e-03
IL=250m Poles:I_P = 3.0e-06
IL=250m Poles:I_P = 3.5e-03
IL=250m Poles:I_P = 3.0e-06 .. 3.5e-03

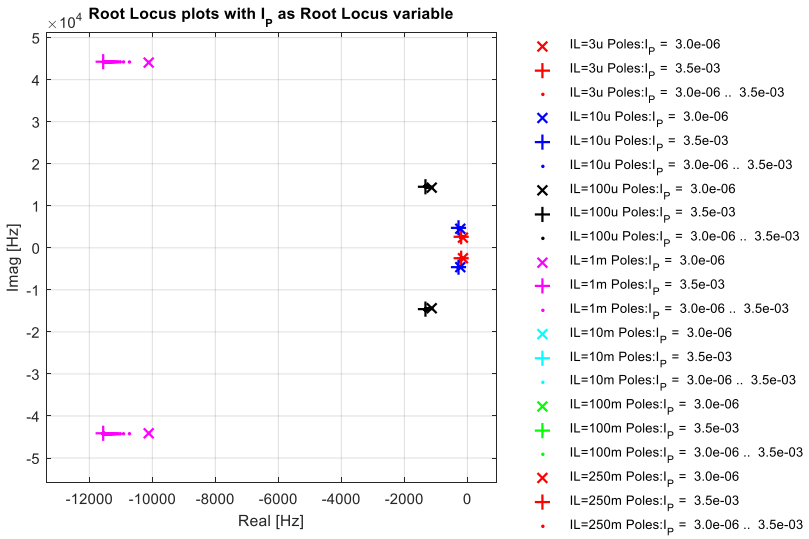
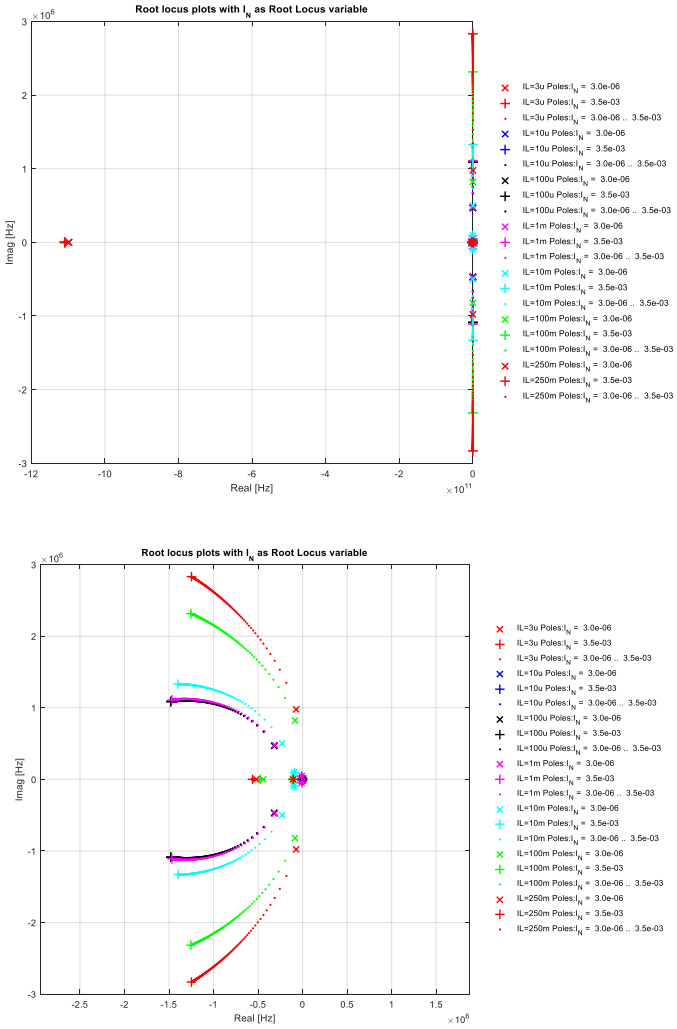


Figure 7-28 Root Locus plots with I_P as Root Locus variable at different load current scenarios



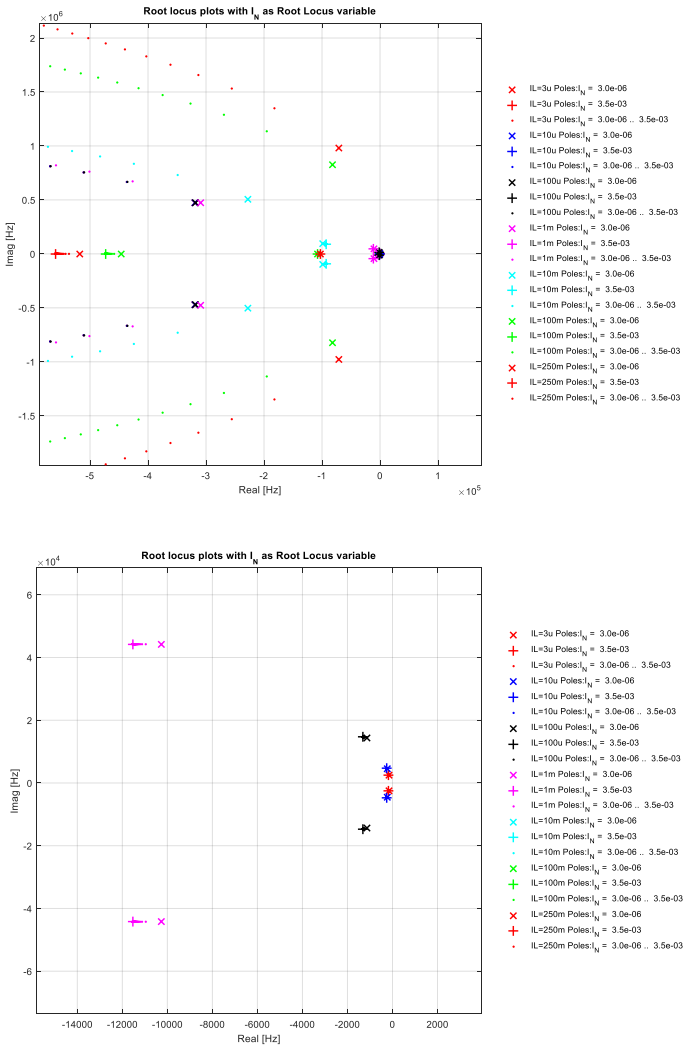


Figure 7-29 Root Locus plots with I_N as Root Locus variable at different load current scenarios

From Figure 7-28 and Figure 7-29, it can be concluded that this passive compensation scheme probably is capable of stabilizing this voltage regulator. The effectiveness of this compensation scheme is further verified in Cadence environment in Chapter 8.

7.5 Over current protection

The voltage regulator should have the over-current protection (OCP) function to protect itself from overload current damage, because current above limitation may cause the BUK transistor heating up which reduces its lifetime and may result in device failure. In real applications, the over-current scenario could be caused by the over power demand from the load. In this case, the voltage regulator should be kept at some constant output current to drive the loading circuit, which is 400mA is this design. This feature prevents the loading circuit from resetting if the over power demand only lasts a short period of

time. The basic method of overcurrent protection is shown in Figure 7-30, when the voltage regulator is operating in over current protection mode, the main voltage regulation loop is disabled because all the driving current for the BUK transistor is conducted to ground through M_{OCP}. The current sensing block senses the exact value of the output current, the over current control block controls M_{OCP}. If the load current is below the current limit (400mA), the current I_{OCP} is near 0, which adds no effect on the voltage regulation loop. If the load current exceeds 400mA, the over current control block will drive M_{OCP} into conduction, redirecting the driving current for BUK transistor to ground.

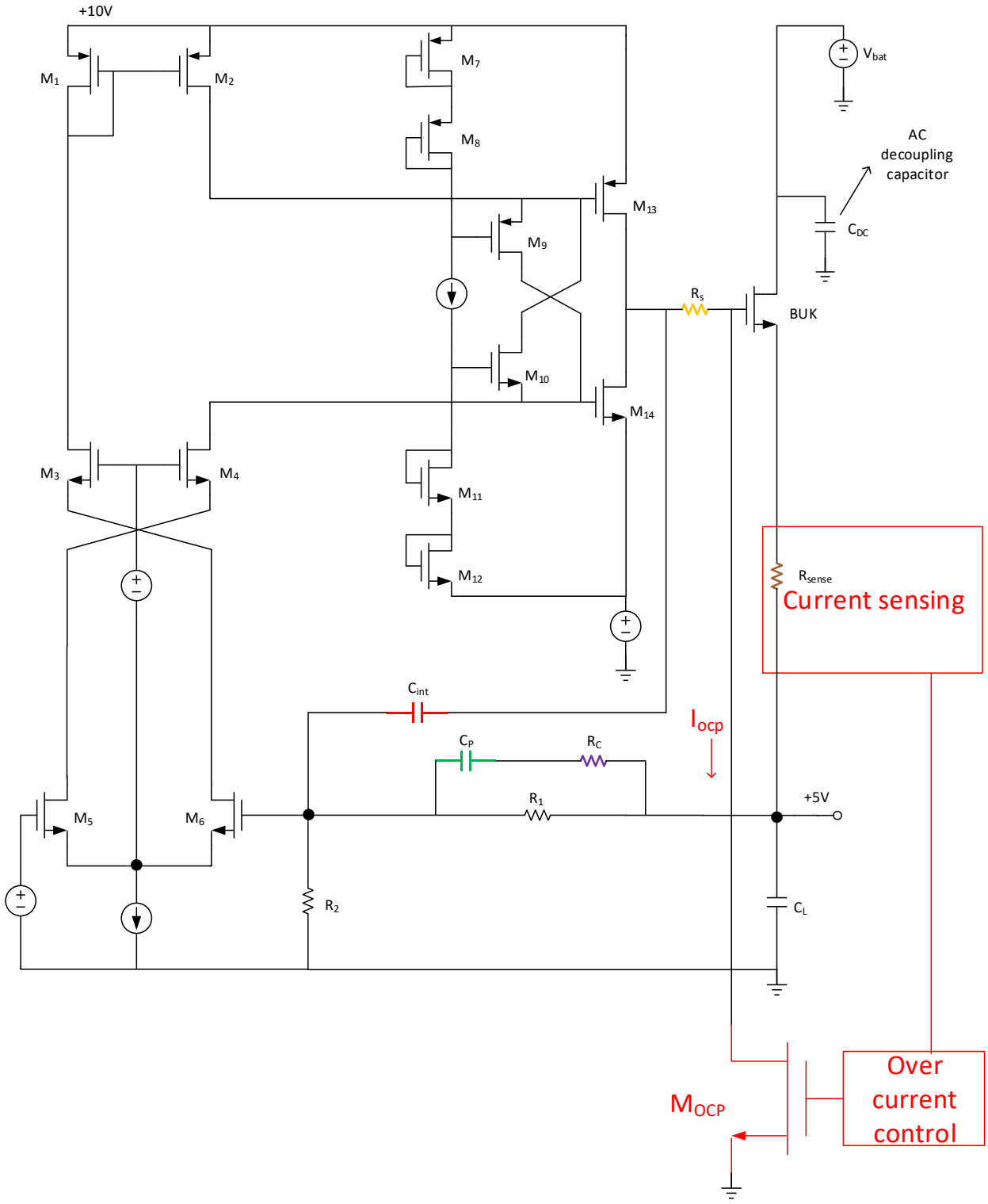


Figure 7-30 the block level schematic diagram of over current protection

The detailed transistor level implementation is shown in Figure 7-31, M_A and M_B form a PMOS current mirror which mirrors out the load current flowing through R_{sense}, I_{bias2} and R_{bias} compose a voltage reference, the current flowing through M_B and M_D is the control current of M_{OCP}. The stability and the

other performance evaluations of this current regulator should be taken care of, they are tested in Chapter 8.

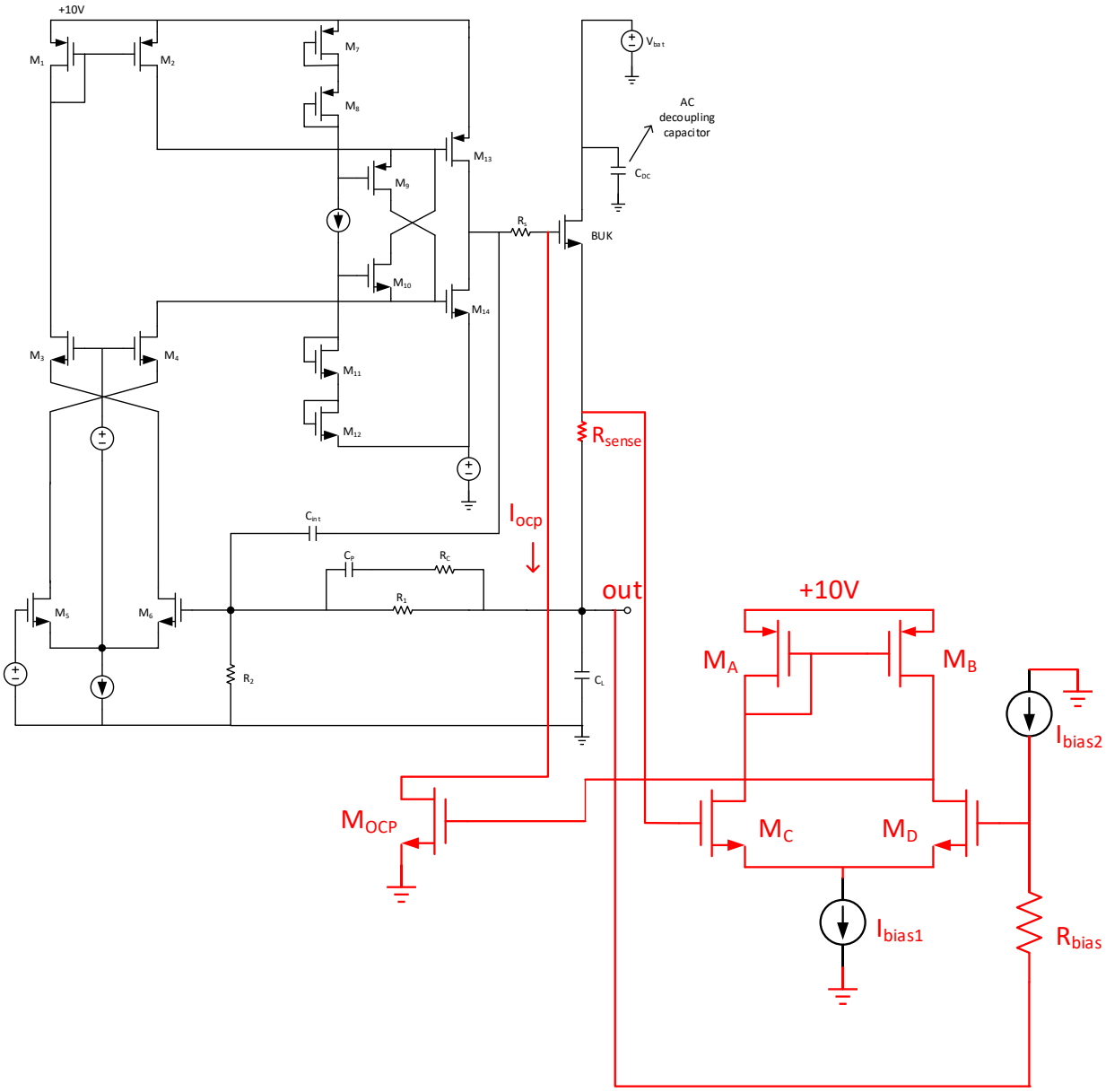


Figure 7-31 the detailed transistor level implementation of over current protection

7.6 Current dump path

As discussed in Chapter 6, when the load current suddenly increases from low to high, the BUK transistor is able to source current to the load, however, when the load current suddenly decreases from high to low, there is no current sink path except for the feedback resistor path, and the current sink capability of feedback resistors is too low. If we do not have extra current dump path, when the load current decreases

from high to low, the BUK transistor current and load current difference will charge the output capacitor, making the output voltage higher than the nominal value.

To solve this problem, a current dump path should be added. The current dump circuit should be active only when the load current varies from high to low. In other cases, the current sink path should not draw any quiescent current from the voltage regulator. Figure 7-32 shows one possible implementation of this current dump path.

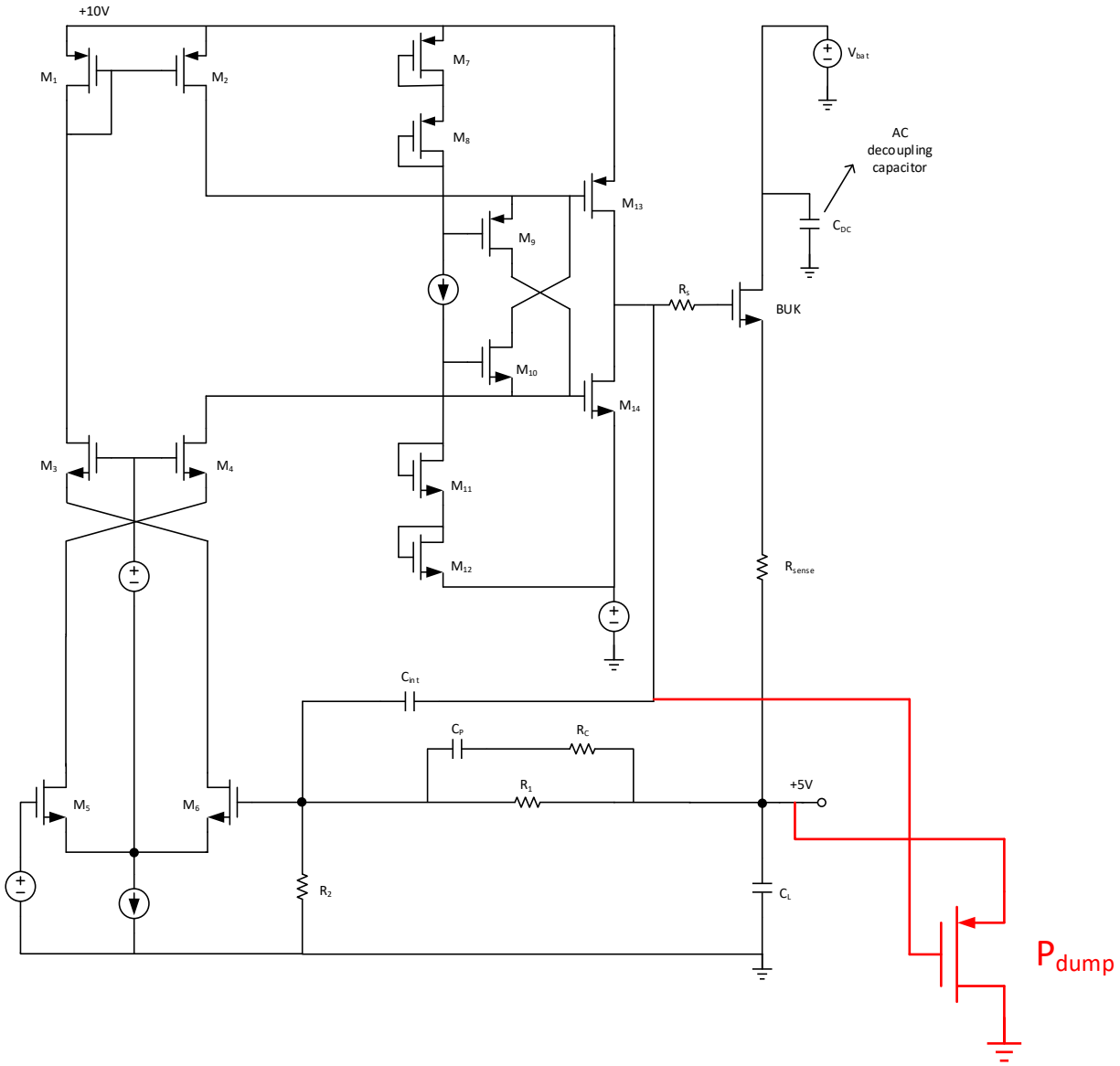


Figure 7-32 the transistor level implementation of current damp transistor

7.7 Floating sources

Because of the limited quiescent current budget in this design, the floating current source and floating voltage source are required in this voltage regulator. The conceptual implementation of floating sources in this regulator is discussed in this Section.

The implementation of floating current source is achieved by a pair of scaling current mirror and a resistor, the transistor level implementation is shown in Figure 7-33.

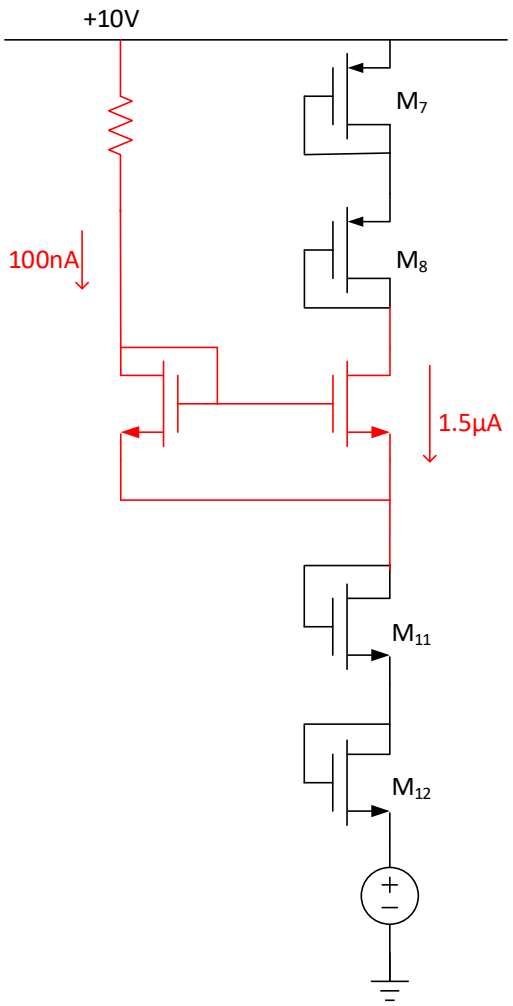


Figure 7-33 Transistor level implementation of floating current source

The implementation of floating voltage source is achieved by diode connected transistors and current source with minus node connected to ground. The transistor level implementation of floating voltage source is shown in Figure 7-34.

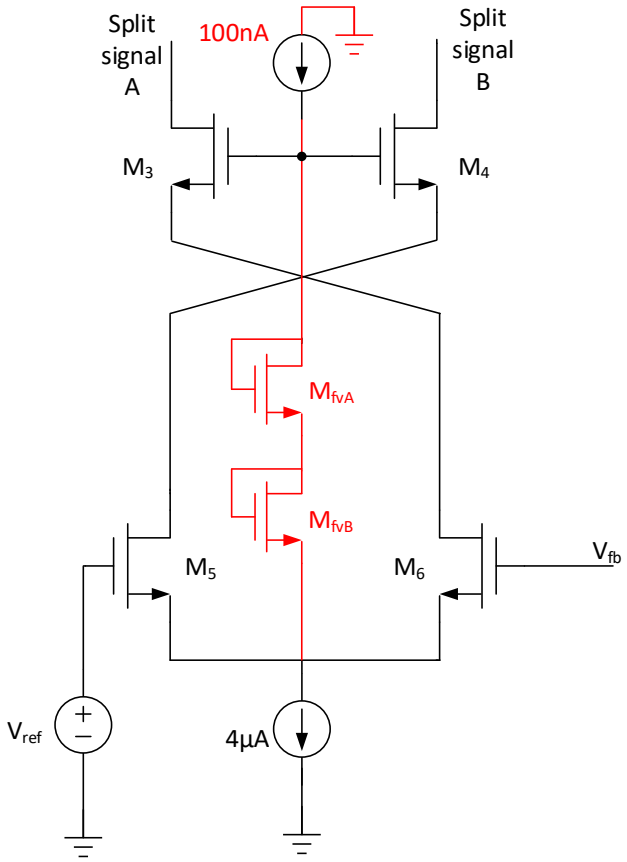


Figure 7-34 Transistor level implementation of floating voltage source

8 Performance evaluations

In this Chapter, the performance of this voltage regulator will be presented and summarized.

8.1 Static performance

8.1.1 Dropout region

From Figure 8-1, it shows that the regulator is functional around 5.3V when the regulator is in full load current scenario, which makes low drop-out regulation available.

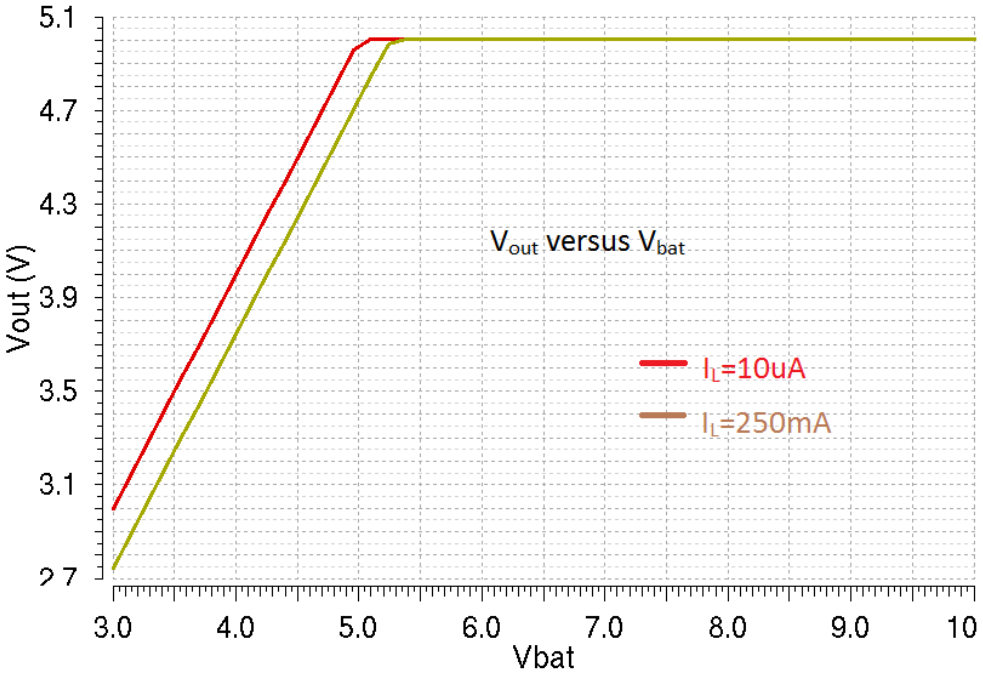


Figure 8-1 V_{out} versus V_{bat}

8.1.2 Quiescent current and current efficiency

The quiescent current I_q of this voltage regulator is 10.5μA, it should be noted that the band-gap circuit quiescent current is excluded.

The full load current of this regulator is 250mA, the overall current efficiency is defined as:

$$\eta_{current} = \frac{I_{load}}{I_{load} + I_q} \cdot 100\%$$

Therefore, the current efficiency of this regulator is 99.996%.

The distribution of quiescent current is shown in Figure 8-2.

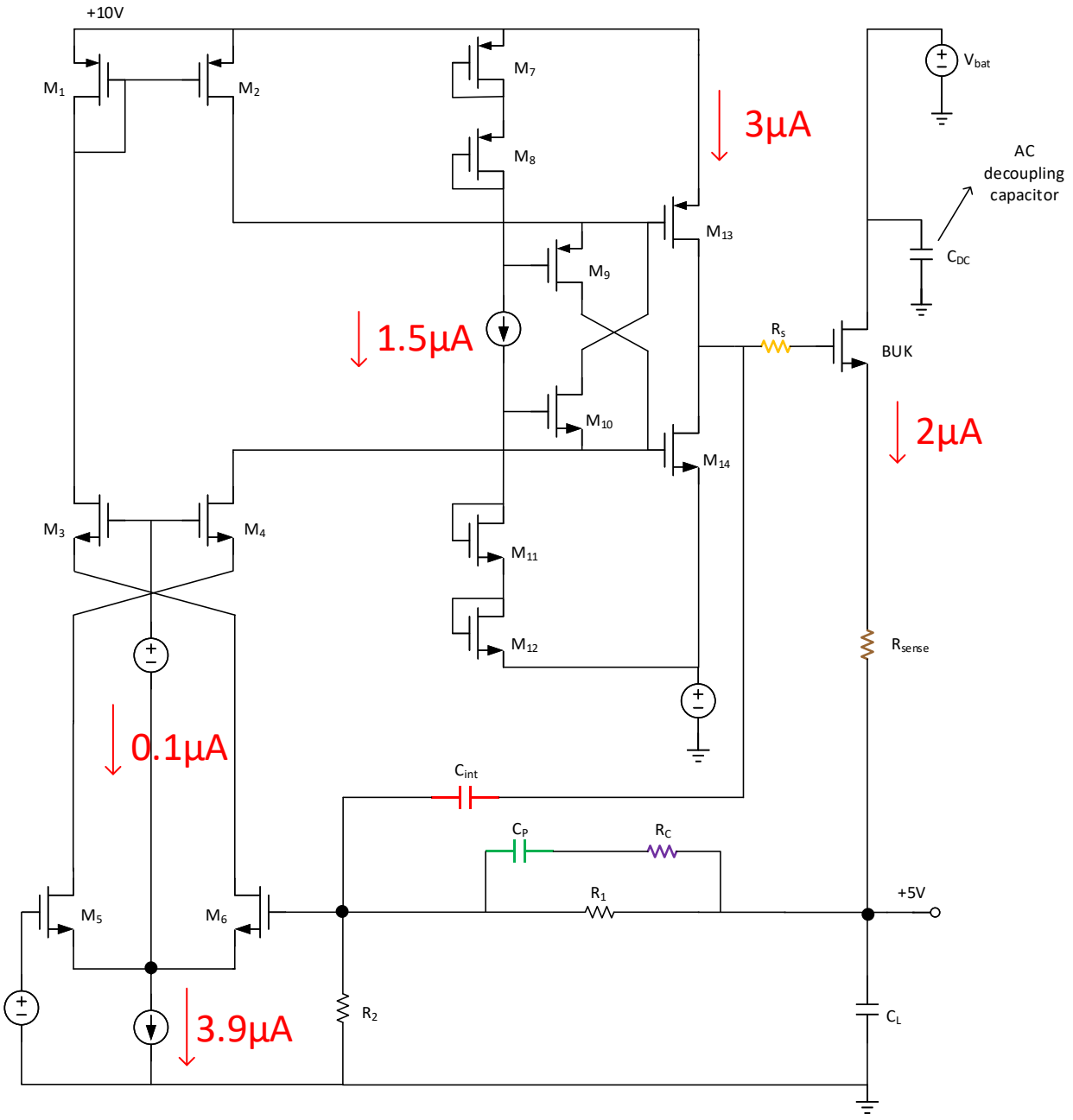


Figure 8-2 The schematic showing the quiescent current distribution

8.1.3 Static output voltage accuracy

The static output voltage accuracy of the voltage regulator is presented in this subSection. Figure 8-3 shows the line regulation performance.

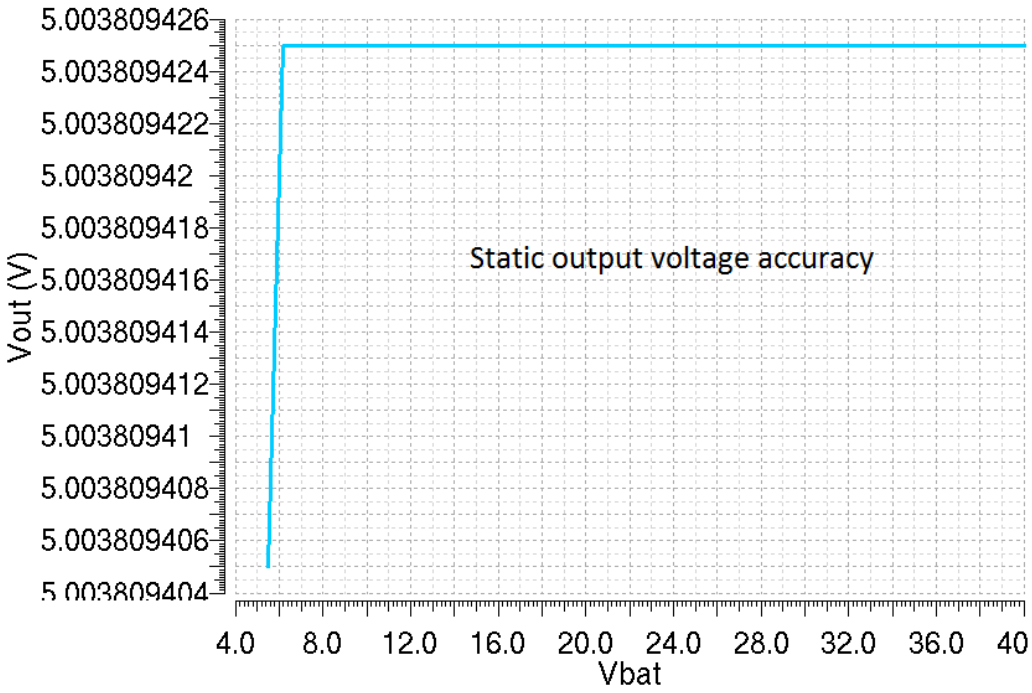


Figure 8-3 Static line regulation (I_L = 250mA)

Figure 8-3 shows the load regulation performance. The output voltage becomes more accurate as the load current increases. The reason is the loop gain of this voltage regulator increases as the load current increases. From Figure 8-4, the maximum inaccuracy is around 4mV. This inaccuracy is a consequence of biasing errors.

In practical cases, the mismatch between transistors and passive components also contributes to the output voltage inaccuracy. This inaccuracy can be solved to some extent by trimming of the feedback resistors during the chip fabrication.

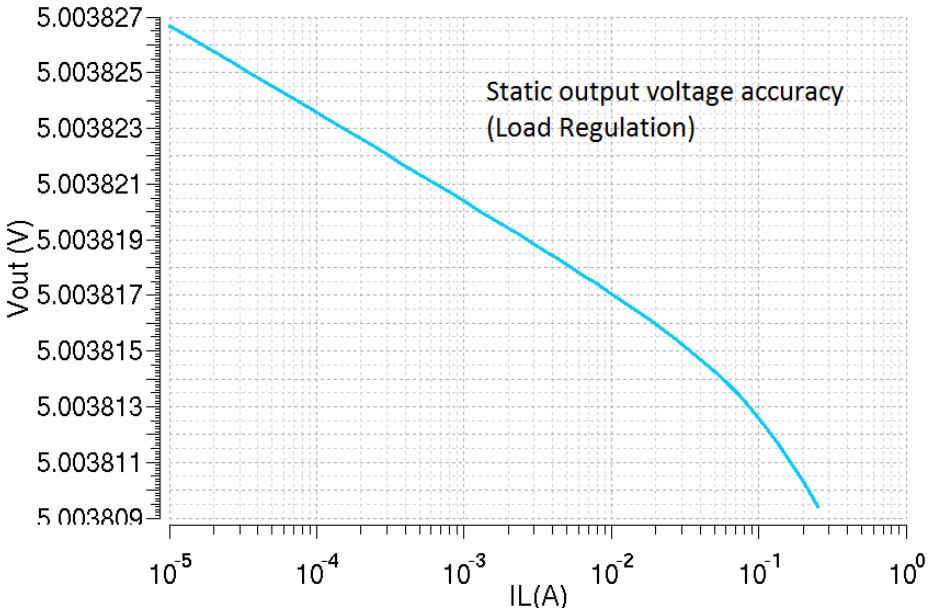


Figure 8-4 Static load regulation (V_{bat} = 12V)

8.2 Small signal stability

In order to further investigate the system stability in Cadence and also investigate the suitability of this modified EKV model for small signal analysis, the Bode plots generated in Cadence (based on BSIM model) and the Bode plots generated in SLiCAP (based on modified EKV model) are both discussed in this Section.

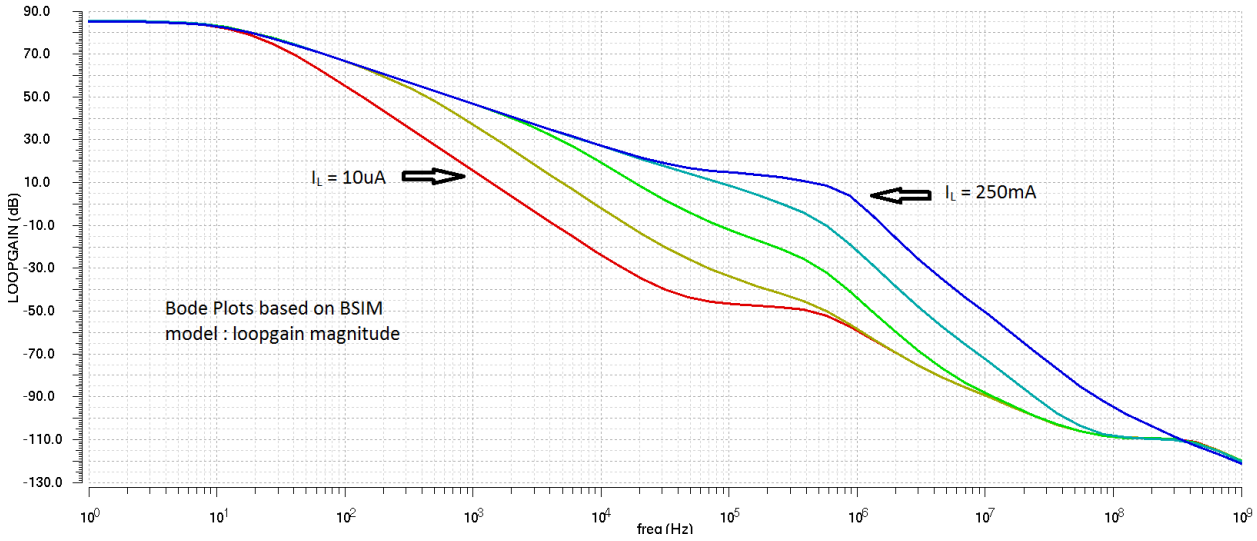


Figure 8-5 Bode plots of loop-gain magnitude based on BSIM model

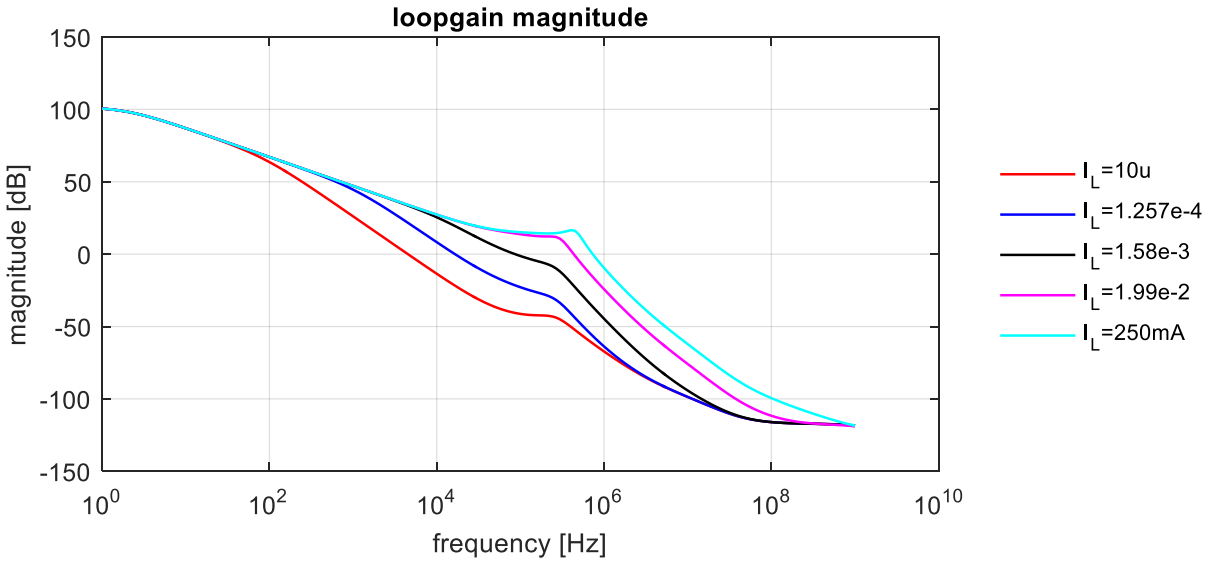


Figure 8-6 Bode plots of loop-gain magnitude based on modified EKV model

From the Figure 8-5, Figure 8-6, Figure 8-7 and Figure 8-8, it can be seen that the AC behavior of this voltage regulator based on different models matches with 10% error of unity gain frequency when the load current is high, and matches with 30% error of unity gain frequency when the load current is below 10mA. The AC behavior difference between these two models are mainly contributed by the different model of BUK transistor, which is a level-3 (without weak inversion region modeled) model in Cadence and a modified EKV model in SLiCAP (with weak inversion region modeled).

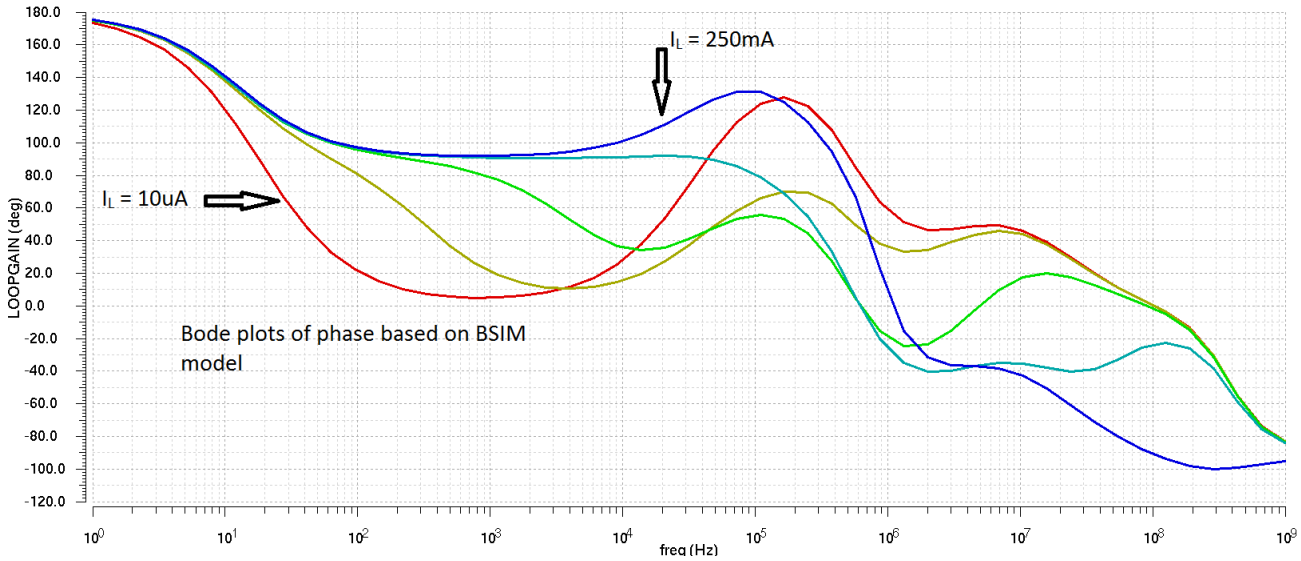


Figure 8-7 Bode plots of phase based on BSIM model

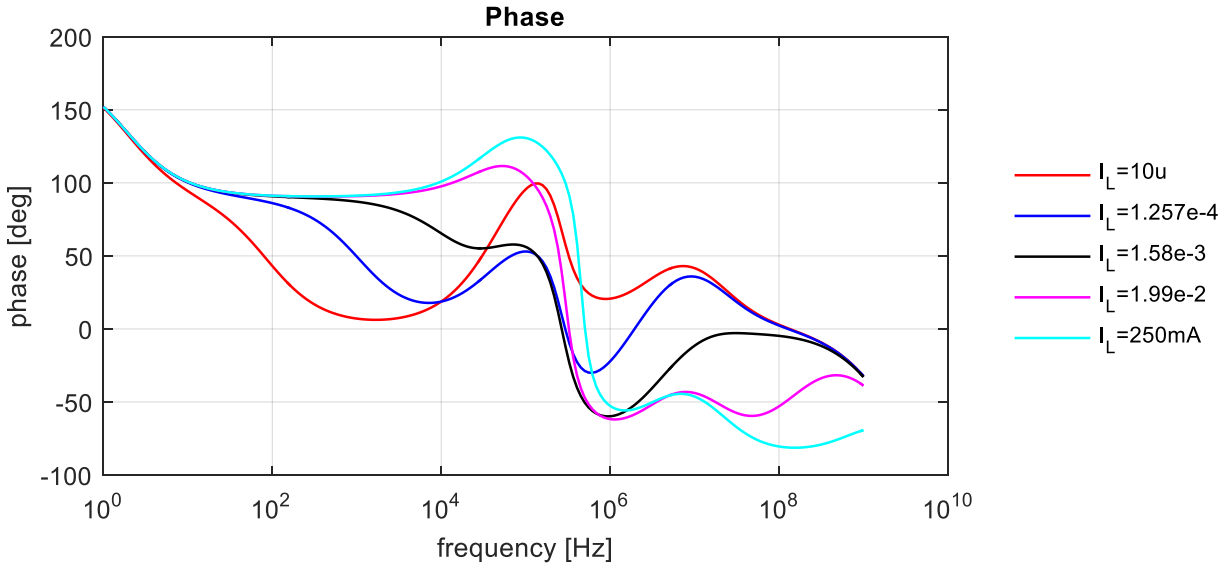


Figure 8-8 Bode plots of phase based on modified EKV model

From Figure 8-5 and Figure 8-7, it can be seen that this voltage regulator is stable in the whole load current scenarios. Although the system shows under-damped behavior (for the phase margin is low) in low load current scenario, the regulator output voltage variation due to load current step in this range is not critical. The reason for that is small current variation can be immediately compensated by the charge stored on the external load capacitor.

8.3 Dynamic performance

8.3.1 Line transient response

The low battery line transient response is shown in Figure 8-9. It can be seen that the output voltage variation is within the specification.

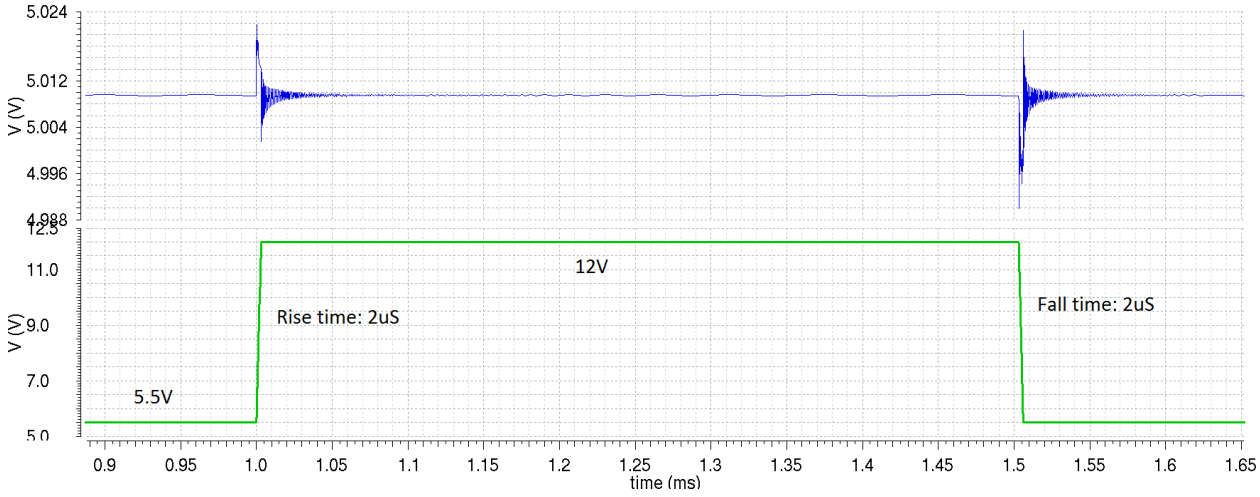


Figure 8-9 Line transient response of low battery variation

The high voltage line transient response is shown in Figure 8-10. It can be seen that as the NMOS pass transistor goes into saturation region, the ringing time of output voltage is reduced.

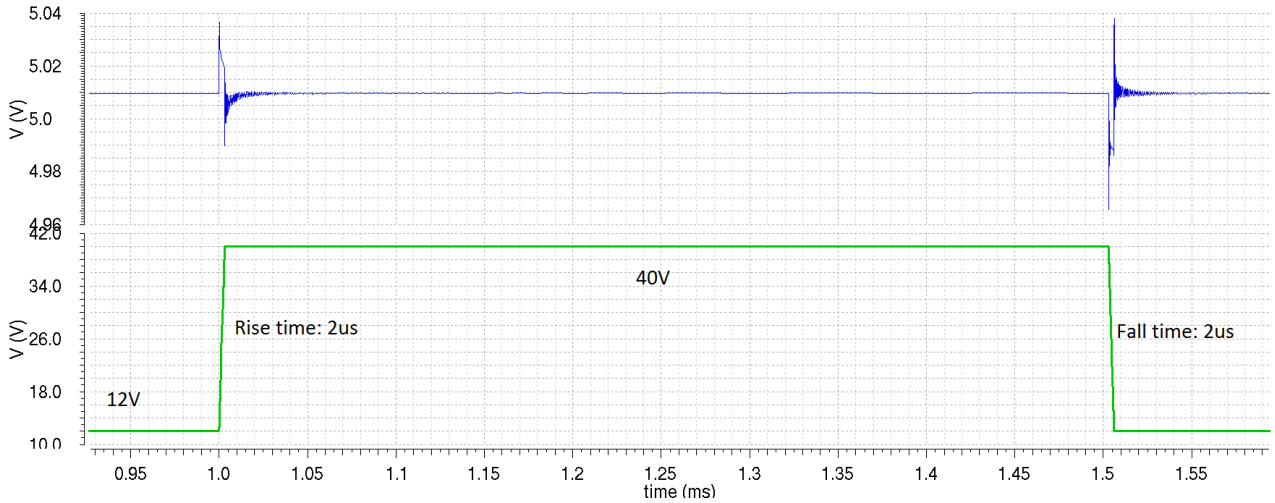


Figure 8-10 Line transient response of high battery variation

8.3.2 Load transient response

The load transient response for V_{bat} = 12V is shown in Figure 8-11, it can be found that the V_{out} variation is around $\pm 100mV$.

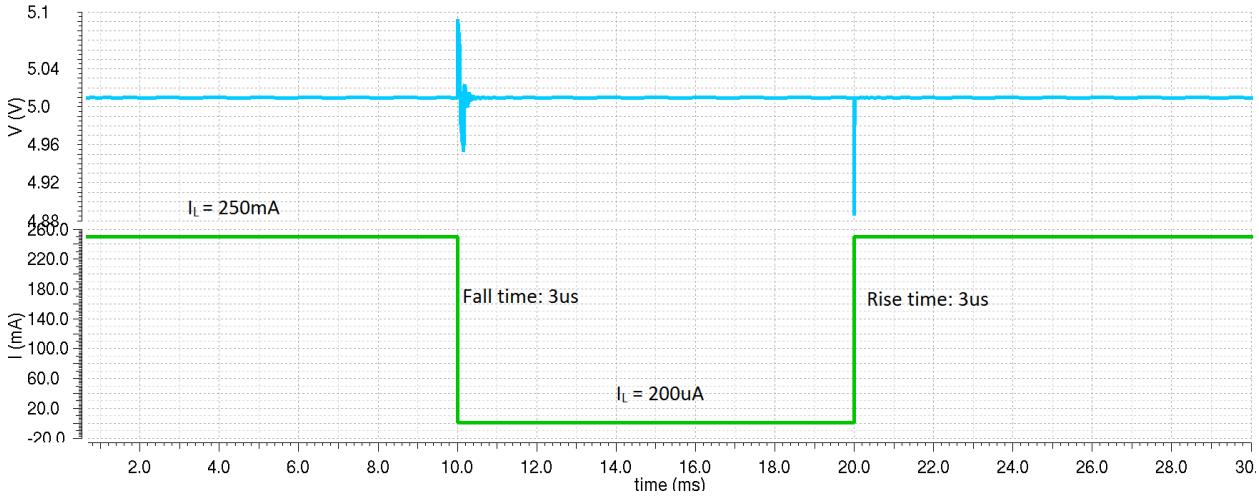


Figure 8-11 Load transient response (V_{bat} = 12V)

It is necessary to check if the low current region gives any critical error to this regulator, the low current load transient response is shown in Figure 8-12.

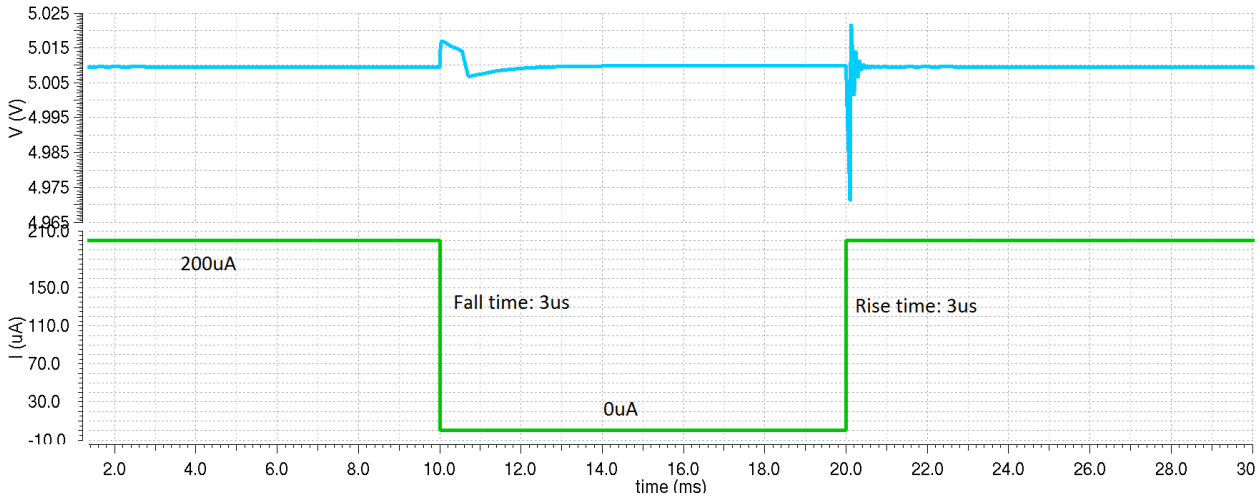


Figure 8-12 Low current load transient response (V_{bat} = 12V)

8.3.3 Over current protection performance

According to the requirement of this voltage regulator, the over current protection circuit should work when the load current comes to 400mA. The over current protection function is tested, the output current is shown in Figure 8-13.

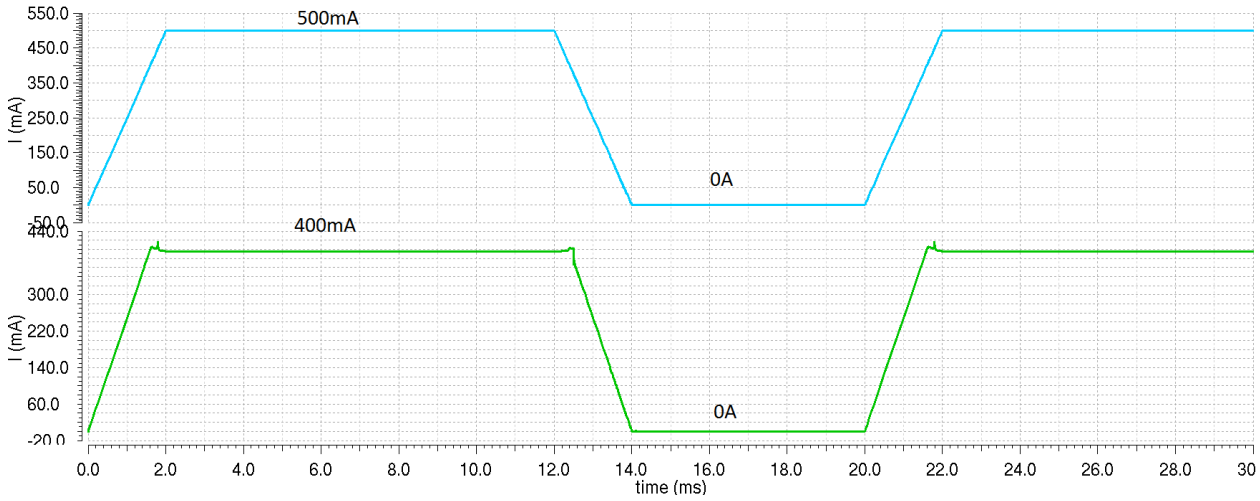


Figure 8-13 Over current protection transient behavior

8.3.4 External load capacitor scaling

As stated in Chapter 2, the compatibility of load capacitor with different sizing is required. Figure 8-14 and Figure 8-15 show the load transient response with different size of load capacitor.

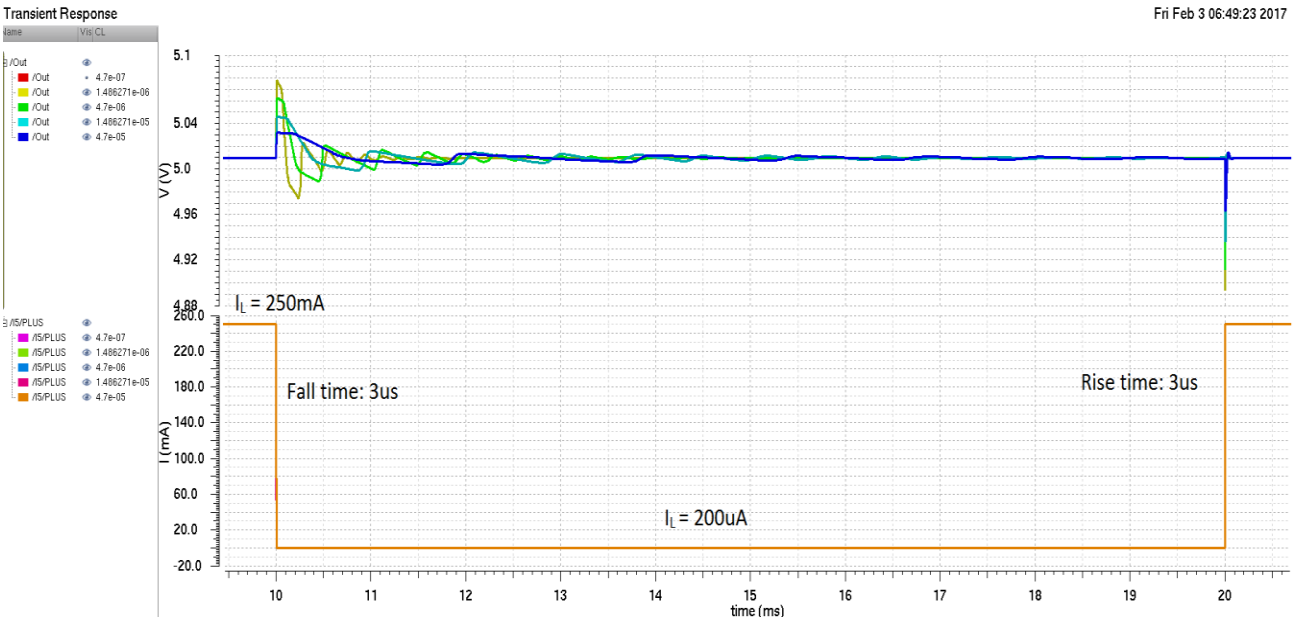


Figure 8-14 Load transient response with different size of load capacitor (V_{bat} = 12V)

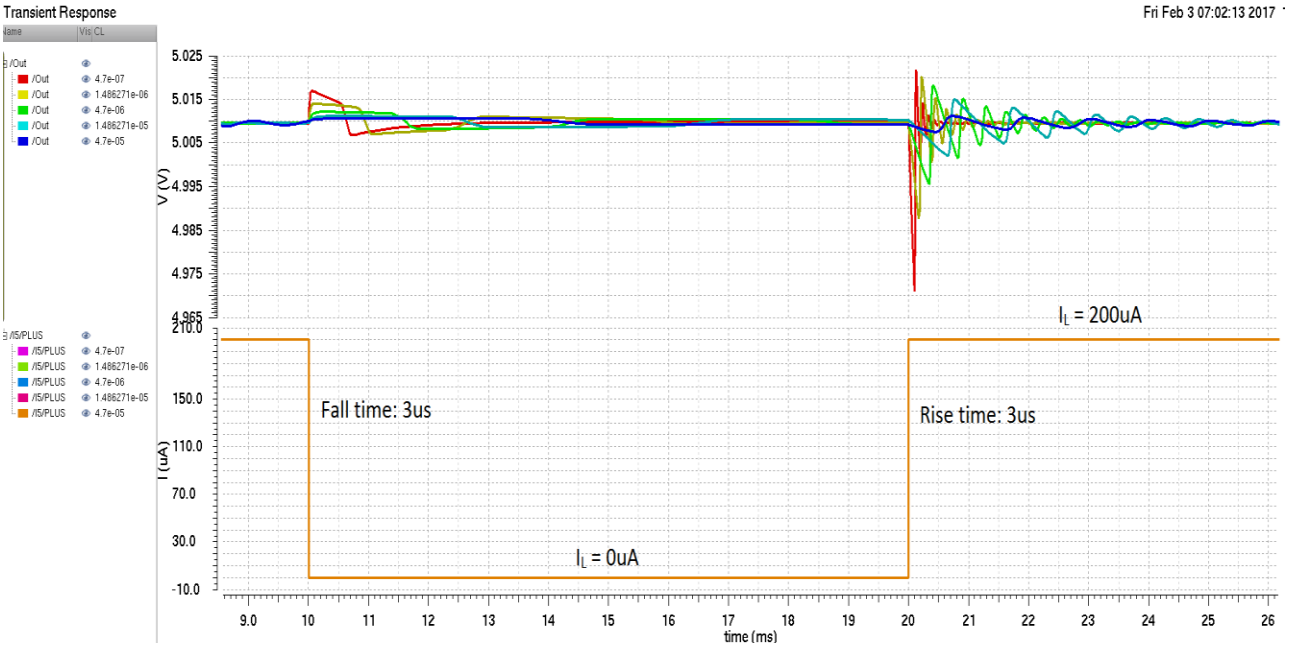


Figure 8-15 Low current load transient response with different size of load capacitor (V_{bat} = 12V)

8.3.5 Overall performance summary

Table 8-2 shows the overall performance summary of this voltage regulator. The numbers in brackets are the required value in the beginning of this project.

symbol	parameter	condition	min	typ	max	unit
V_{IN}	Regulator Input Voltage	.	5.5(5.5)	.	40(40)	V
V_{OUT}	Output Voltage	I_{out} = 10μA to 250mA	4.9(4.9)	5	5.1(5.1)	V
$V_{out\text{-}load}$	Dynamic Load Regulation	.	-2(-2)	.	2(2)	%
$t_{stabilized}$	output voltage within 0.5% after load step	.	.	.	0.2(1)	ms
$V_{out\text{-}line}$	Dynamic Line Regulation	.	-1(2)	.	1(2)	%
I_q	Quiescent Current (w/o band-gap)	I_{out} = 0-10μA Temp ≤ 85°C	.	≈10.5μA (10 μA)		μA
$I_{q'}$	Current Consumption (w/o band-gap)	$I_{out} \geq$ 1mA		≈10.5μA (1.3% · I_{out})		μA
η	Current efficiency (w/o band-gap)	.	.	99.996% in any scenario (99.9% in zero-load scenario, 98.7% in full-load scenario)	.	.
C_L	External Output Capacitor		0.47(0.47)	.	47(47)	μF
I_{out}	Load Current		.	250(250)	400(400)	mA
Overall Performance	With PCB & Packaging parasitic			✓		

Table 8-1 Overall performance summary of this voltage regulator

9 Conclusions and future work

In this thesis, a voltage regulator with external NMOS pass device is presented. Based on the development of modified EKV model and the asymptotic gain model, the small signal behavior is accurately analyzed. The feasibility of conceptual active compensation is tested, and an effective passive compensation scheme is proposed. The effectiveness of this compensation is verified by both Root Locus analysis and Cadence simulation.

This voltage regulator is able to keep ±2% output voltage accuracy. The current efficiency of this voltage regulator is 99.996%. The typical output current is 250mA and the maximum output current can be 400mA. The load capacitor of this voltage regulator can be scaled from 470nF to 47µF. The influence of PCB and Packaging parasitic is modeled, calculated and tested in this design, the overall performance of this voltage regulator will not be influenced by these parasitic inductors and capacitors.

Due to the time limit, measurement results of this voltage regulator test-chip is not included in this thesis. Beside the silicon verification of this work, from design perspective of view, the future work can be done in five aspects:

i. The consideration of replacing this BUK transistor with a proper one for this design.
ii. Make the value of C_{int} adaptively scaling with load current to have better transient performance.
iii. The feasibility of replacing this BUK transistor with internal power NMOS transistor.
iv. Adding ESD protections and over voltage protections.
v. Trimming can be implemented on the feedback resistors R_1 and R_2 to minimize the output voltage spread.

10 Appendix

10.1 Appendix A: Fitting of modified EKV model

In order to create the best matching on frequency behavior of the BSIM model and the EKV model, the fitting is based on the g_m versus I_d plot and the F_T versus I_d plot, because F_T and g_m are main parameters that related to the frequency behavior of transistors. the g_m versus I_d plots based on different types of model are The F_T versus I_d plots based on different types of model are shown in Figure 10-1 and Figure 10-2. The plots are all results after fitting.

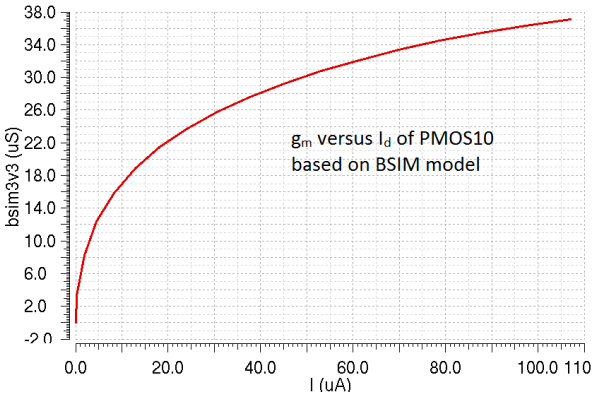


Figure 10-1 gm versus Id of PMOS10 based on BSIM model

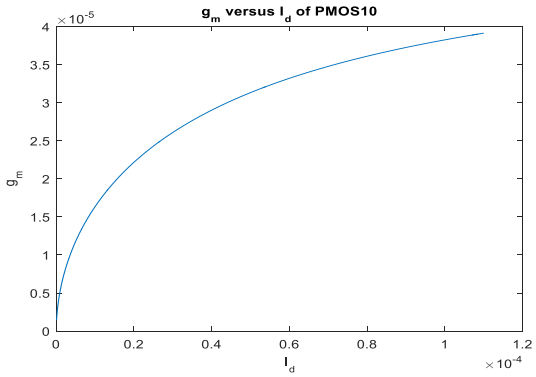
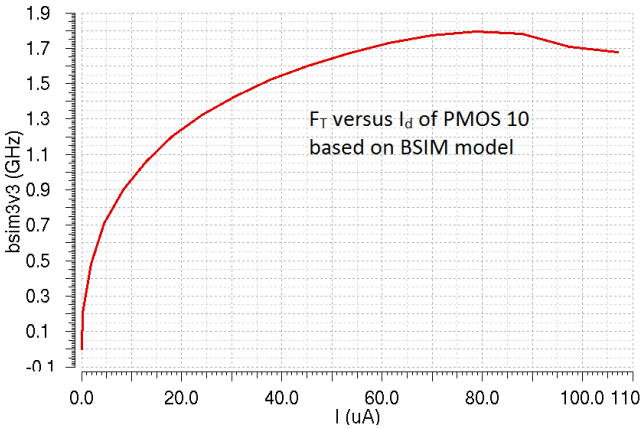


Figure 10-2 gm versus Id of PMOS10 based on modified EKV model



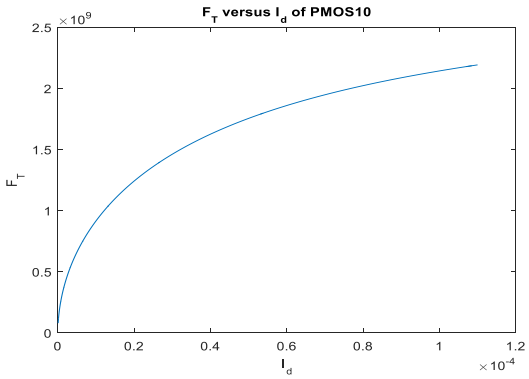


Figure 10-3 FT versus Id of PMOS10 based on BSIM model

Figure 10-4 FT versus Id of PMOS10 based on modified EKV model

All the transistors used in the small signal analysis are modeled in the same way, including the BUK transistor.

The MATLAB codes for this fitting are:

```
clear all

slicap();

makeNetlist('buktest','buktest');

errors = checkCircuit('buktest');

% all parameters should have numeric values!

defPar('ID',0);

stepVar('ID');

stepStart('0.1u');

stepStop('110u');

stepNum(500);

stepMethod('log');

Step('true');

pars = getStepParams({'ID','FT_X1'});

plot(pars.ID, pars.FT_X1);

stophtml();
```

The final model file of the modified EKV model is:

```
* Sub circuits for corresponding gSchem and LTspice symbols

.subckt ABCD 1 2 3 4 at={at} bt={bt} ct={ct} dt={dt}
N1 1 5 3 7
E1 7 8 1 2 {at}
H1 8 4 6 5 {bt}
G1 3 4 1 2 {ct}
F1 3 4 2 6 {dt}
.ends

.subckt O_dcvar 1 2 4 COMMON
+ sib={sib}
+ sio={sio}
+ svo={svo}
+ iib={iib}
Ib 1 5 I dc={iib} dcvar={sib^2}
F1 2 COMMON 5 COMMON 1
Io 1 2 I dcvar={sio^2}
Vo 1 3 V dcvar={svo^2}
N1 4 COMMON 3 2
.ends

.subckt O_noise 1 2 4 COMMON sv={sv} si={si}
N1 4 COMMON 3 2
V1 1 3 V noise={sv}
I1 1 2 I noise={si}
.ends

.subckt N_noise 1 2 4 COMMON sv={sv} si={si}
N1 4 COMMON 3 2
V1 1 3 V noise={sv}
I1 1 2 I noise={si}
.ends

.subckt N_dcvar 1 2 4 6 COMMON
+ sib={sib}
+ sio={sio}
+ svo={svo}
+ iib={iib}
Ib 1 5 I dc={iib} dcvar={sib^2}
F1 2 COMMON 5 COMMON 1
Io 1 2 I dcvar={sio^2}
Vo 1 3 V dcvar={svo^2}
N1 4 6 3 2
```

```
.ends

.subckt BUK drain gate source bulk ID={ID}
M1 drain gate source bulk BUK
.model BUK M
+ cgs    = {c_gs}
+ gm     = {g_m}
+ cdg    = {c_dg}
+ gb     = {(N-1)*g_m}

.param
+ KP     = 40.5
+ g_m    = {ID/(N*U_T*sqrt(IC+0.5*sqrt(IC)+1))}
+ c_gs   = 498p
+ c_dg   = 100p
+ U_T    = 25.6m
+ N      = 1.4
+ IC     = {2*ID/KP/((2*N*U_T)^2)}
+ FT     = {g_m/(c_gs+c_dg)/2/pi}
.ends

.subckt NMOS_ANA drain gate source bulk W={W} L={L} ID={ID}
M1 drain gate source bulk NMOS_ANA
.model NMOS_ANA M
+ cgs    = {c_gs}
+ gm     = {g_m}
+ go     = {g_o}
+ cdg    = {c_dg}
+ gb     = {(N-1)*g_m}

.param
+ IC_CRIT = {1/(8*(N*U_T)^2*(Theta+1/L/E_CRIT))}
+ g_m    = {ID/(N*U_T*sqrt(IC*(1+IC/IC_CRIT)+0.5*sqrt(IC*(1+IC/IC_CRIT))+1))}
+ g_o    = {ID/VAL/L}
+ c_gs   = {W*L*C_0 + C_O*W}
+ c_dg   = {C_O*W}
+ U_T    = 25.6m
+ Theta  = 0.28
+ E_CRIT = 3M
+ N      = 1.043
+ IC     = {ID*L/W/I_0}
+ VAL    = 80M
+ I_0    = {2*N*mu_0*C_0*U_T^2}
+ mu_0   = 34.6m
```

```
+ C_0     = {8.85p * 3.9 / TOX}
+ C_O     = 473p
+ TOX     = 3.49n
+ FT      = {g_m/(c_gs+c_dg)/2/pi}
.ends

.subckt MOS5N drain gate source bulk W={W} L={L} ID={ID}
M1 drain gate source bulk MOS5N
.model MOS5N M
+ cgs     = {c_gs}
+ gm      = {g_m}
+ go      = {g_o}
+ cdg     = {c_dg}
+ gb      = {(N-1)*g_m}

.param
+ IC_CRIT = {1/(8*(N*U_T)^2*(Theta+1/L/E_CRIT))}
+ g_m     = {ID/(N*U_T*sqrt(IC*(1+IC/IC_CRIT)+0.5*sqrt(IC*(1+IC/IC_CRIT))+1))}
+ g_o     = {ID/VAL/L}
+ c_gs    = {W*L*C_0 + C_O*W}
+ c_dg    = {C_O*W}
+ U_T     = 25.6m
+ Theta   = 0.28
+ E_CRIT  = 5.6M
+ N       = 1.1
+ IC      = {ID*L/W/I_0}
+ VAL     = 66.6M
+ I_0     = {2*N*mu_0*C_0*U_T^2}
+ mu_0    = 53m
+ C_0     = {8.85p * 3.9 / TOX}
+ C_O     = 463.7p
+ TOX     = 13.1n
+ FT      = {g_m/(c_gs+c_dg)/2/pi}
.ends

.subckt MOS5P drain gate source bulk W={W} L={L} ID={ID}
M1 drain gate source bulk MOS5P
.model MOS5P M
+ cgs     = {c_gs}
+ gm      = {g_m}
+ go      = {g_o}
+ cdg     = {c_dg}
+ gb      = {(N-1)*g_m}
```

```
.param
+ IC_CRIT = {1/(8*(N*U_T)^2*(Theta+1/L/E_CRIT))}
+ g_m     = {ID/(N*U_T*sqrt(IC*(1+IC/IC_CRIT)+0.5*sqrt(IC*(1+IC/IC_CRIT))+1))}
+ g_o     = {ID/VAL/L}
+ c_gs    = {W*L*C_0 + C_O*W}
+ c_dg    = {C_O*W}
+ U_T     = 25.6m
+ Theta   = 0
+ E_CRIT  = 25M
+ N       = 1.06
+ IC      = {ID*L/W/I_0}
+ VAL     = 127.5M
+ I_0     = {2*N*mu_0*C_0*U_T^2}
+ mu_0    = 9.5m
+ C_0     = {8.85p * 3.9 / TOX}
+ C_O     = 289p
+ TOX     = 13.3n
+ FT      = {g_m/(c_gs+c_dg)/2/pi}
.ends

.subckt MOS10N drain gate source bulk W={W} L={L} ID={ID}
M1 drain gate source bulk MOS10N
.model MOS10N M
+ cgs     = {c_gs}
+ gm      = {g_m}
+ go      = {g_o}
+ cdg     = {c_dg}
+ gb      = {(N-1)*g_m}

.param
+ IC_CRIT = {1/(8*(N*U_T)^2*(Theta+1/L/E_CRIT))}
+ g_m     = {ID/(N*U_T*sqrt(IC*(1+IC/IC_CRIT)+0.5*sqrt(IC*(1+IC/IC_CRIT))+1))}
+ g_o     = {ID/VAL/L}
+ c_gs    = {W*L*C_0 + C_O*W}
+ c_dg    = {C_O*W}
+ U_T     = 25.6m
+ Theta   = 0.28
+ E_CRIT  = 3.4M
+ N       = 1.0999
+ IC      = {ID*L/W/I_0}
+ VAL     = 148M
+ I_0     = {2*N*mu_0*C_0*U_T^2}
+ mu_0    = 41.5m
+ C_0     = {8.85p * 3.9 / TOX}
```

```
+ C_O     = 1.2n
+ TOX     = 13.5n
+ FT      = {g_m/(c_gs+c_dg)/2/pi}
.ends

.subckt MOS10P drain gate source bulk W={W} L={L} ID={ID}
M1 drain gate source bulk MOS10P
.model MOS10P M
+ cgs     = {c_gs}
+ gm      = {g_m}
+ go      = {g_o}
+ cdg     = {c_dg}
+ gb      = {(N-1)*g_m}

.param
+ IC_CRIT = {1/(8*(N*U_T)^2*(Theta+1/L/E_CRIT))}
+ g_m     = {ID/(N*U_T*sqrt(IC*(1+IC/IC_CRIT)+0.5*sqrt(IC*(1+IC/IC_CRIT))+1))}
+ g_o     = {ID/VAL/L}
+ c_gs    = {W*L*C_0 + C_O*W}
+ c_dg    = {C_O*W}
+ U_T     = 25.6m
+ Theta   = 0
+ E_CRIT  = 25M
+ N       = 1.1
+ IC      = {ID*L/W/I_0}
+ VAL     = 41.4M
+ I_0     = {2*N*mu_0*C_0*U_T^2}
+ mu_0    = 9.3m
+ C_0     = {8.85p * 3.9 / TOX}
+ C_O     = 761p
+ TOX     = 13.3n
+ FT      = {g_m/(c_gs+c_dg)/2/pi}
.ends

.subckt MOS5ND drain1 drain2 gate1 gate2 W={W} L={L} ID={ID}
M1 drain1 drain2 gate1 gate2 MOS5ND
.model MOS5ND MD
+ cgg     = {c_gs/2}
+ gm      = {g_m/2}
+ go      = {g_o/2}
+ cdg     = {c_dg}

.param
+ IC_CRIT = {1/(8*(N*U_T)^2*(Theta+1/L/E_CRIT))}
```

```
+ g_m     = {ID/(N*U_T*sqrt(IC*(1+IC/IC_CRIT)+0.5*sqrt(IC*(1+IC/IC_CRIT))+1))}
+ g_o     = {ID/VAL/L}
+ c_gs    = {W*L*C_0 + C_O*W}
+ c_dg    = {C_O*W}
+ U_T     = 25.6m
+ Theta   = 0.28
+ E_CRIT  = 5.6M
+ N       = 1.1
+ IC      = {ID*L/W/I_0}
+ VAL     = 66.6M
+ I_0     = {2*N*mu_0*C_0*U_T^2}
+ mu_0    = 53m
+ C_0     = {8.85p * 3.9 / TOX}
+ C_O     = 463.7p
+ TOX     = 13.1n
+ FT      = {g_m/(c_gs+c_dg)/2/pi}
.ends

.subckt CMOS18PD drain gate source bulk W={W} L={L} ID={ID}
M1 drain gate source bulk CMOS18PD
.model CMOS18PD MD
+ cgg     = {c_gs/2}
+ gm      = {g_m/2}
+ go      = {ID/VAL/L/2}
+ cdg     = {c_dg}

.param
+ IC_CRIT = {1/(8*(N*U_T)^2*(Theta+1/L/E_CRIT))}
+ g_m     = {ID/(N*U_T*sqrt(IC*(1+IC/IC_CRIT)+0.5*sqrt(IC*(1+IC/IC_CRIT))+1))}
+ g_o     = {ID/VAL/L}
+ c_gs    = {W*L*C_0 + C_O*W}
+ c_dg    = {C_O*W}
+ U_T     = 25.6m
+ Theta   = 0.35
+ E_CRIT  = 14M
+ N       = 1.35
+ IC      = {ID*L/W/I_0}
+ VAL     = 20M
+ I_0     = {2*N*mu_0*C_0*U_T^2}
+ mu_0    = 8.92m
+ C_0     = {8.85p * 3.9 / TOX}
+ C_O     = 700p
+ TOX     = 4.1n
+ FT      = {g_m/(c_gs+c_dg)/2/pi}
```

.ends

10.2 Appendix B: MATLAB codes for Root Locus analysis

10.2.1 Loop gain analysis with small signal equivalent circuit

```
%Use servobandwidth function in slicap to find the achieveable bandwidth
%and the number of dominant poles in the system.
slicap()
makeNetlist('cd_smallsignal', 'cd_smallsignal');
errors = checkCircuit('cd_smallsignal');
htmlPage('Poles and zeros of loopgain');
simType('numeric');
dataType('pz');
gainType('loopgain');
source('V1');
detector('V_out');
lgRef('G1');
%defPar('c_dg_X1',0);
%defPar('c_gs_X1','1a');
%Why put this to 0: To make the asymptotic gain equal to the ideal gain at
%high frequencies.
%defPar('C_1', 0);
loopgain=execute();
pz2html(loopgain);
params2html();
simType('symbolic');
dataType('Laplace');
result = execute();
loopgain.laplace = result.results(1);
```

```
syms 'L';
eqn2html(L, loopgain.laplace);
%servoBw = findServoBandwidth(loopgain.laplace);
%lowPassData = servoBw(2);
%f_h = lowPassData(1);
stophtml();
```

10.2.2 Root Locus analysis with load current as Root Locus variable

```
slicap()
makeNetlist('2realphantomzeros', '2realphantomzeros');
errors = checkCircuit('2realphantomzeros');
htmlPage('Poles and zeros of gain');
simType('numeric');
dataType('poles');
gainType('gain');
source('V1');
detector('V_out');
lgRef('Gm_M1_X1');
defPar('c_dg_X1',0);
defPar('c_dg_X2',0);
defPar('c_dg_X3',0);
%defPar('c_gs_X1','1a');
%Why put this to 0: To make the asymptotic gain equal to the ideal gain at
%high frequencies.
%defPar('C_1', 0);
gain=execute();
pz2html(gain);
%root locus
```

```
stepVar('I_L');
stepStart('3u');
stepStop('250m');
stepNum(200);
stepMethod('log');
Step('true');
simType('numeric');
dataType('poles');
rootlocus = execute();
plotPZ('root locus step I_L', rootlocus, 'auto', 'auto')
```

10.2.3 Root Locus analysis with source current as Root Locus variable

```
%Use servobandwidth function in slicap to find the achieveable bandwidth
%and the number of dominant poles in the system.
slicap()
makeNetlist('translevel_trial_cd', 'translevel_trial_cd');
errors = checkCircuit('translevel_trial_cd');
htmlPage('RLLL');
simType('numeric');
dataType('pz');
gainType('gain');
source('V1');
detector('V_out');
lgRef('Gm_M1_X1');
defPar('c_dg_X1',0);
defPar('c_dg_X2',0);
defPar('c_dg_X3',0);
%defPar('c_gs_X1','1a');
%Why put this to 0: To make the asymptotic gain equal to the ideal gain at
```

```
%high frequencies.
%defPar('C_1', 0);
loopgain=execute();
pz2html(loopgain);
%root locus
%stepVar('I_L');
%stepStart('1u');
%stepStop('1m');
%stepNum(2000);
%stepMethod('lin');
%Step('true');
%simType('numeric');
%gainType('gain');
%dataType('poles');
%rootlocus = execute();
%plotPZ('root locus step I_L', rootlocus, 'auto', 'auto')
%
%I_L=10u I_sink=0 step I_source
defPar('I_L','3u');
stepVar('I_N');
stepStart('3u');
stepStop('3.5m');
stepNum(200);
stepMethod('lin');
Step('true');
simType('numeric');
gainType('gain');
dataType('poles');
RLStepIsourceIL3u = execute();
```

```
RLStepIsourceIL3u.gainType = 'IL=3u'
%plotPZ('root locus I_L=10u Step I_source', rootlocus, [-2e7,0], [-1e7,1e7]);
%I_L=100u I_sink=0 step I_source
defPar('I_L','10u');
stepVar('I_N');
stepStart('3u');
stepStop('3.5m');
stepNum(200);
stepMethod('lin');
Step('true');
simType('numeric');
gainType('gain');
dataType('poles');
RLStepIsourceIL10u = execute();
RLStepIsourceIL10u.gainType = 'IL=10u'
%
defPar('I_L','100u');
stepVar('I_N');
stepStart('3u');
stepStop('3.5m');
stepNum(200);
stepMethod('lin');
Step('true');
simType('numeric');
gainType('gain');
dataType('poles');
RLStepIsourceIL100u = execute();
RLStepIsourceIL100u.gainType = 'IL=100u'
%plotPZ('root locus I_L=100u Step I_source', rootlocus, [-2e7,0], [-1e7,1e7]);
```

```
%%I_L=1m I_sink=0 step I_source
defPar('I_L','1m');
stepVar('I_N');
stepStart('3u');
stepStop('3.5m');
stepNum(200);
stepMethod('lin');
Step('true');
simType('numeric');
gainType('gain');
dataType('poles');
RLStepIsourceIL1m = execute();
RLStepIsourceIL1m.gainType = 'IL=1m'
%plotPZ('root locus I_L=1m Step I_source', rootlocus, [-2e7,0], [-1e7,1e7]);
%
defPar('I_L','10m');
stepVar('I_N');
stepStart('3u');
stepStop('3.5m');
stepNum(200);
stepMethod('lin');
Step('true');
simType('numeric');
gainType('gain');
dataType('poles');
RLStepIsourceIL10m = execute();
RLStepIsourceIL10m.gainType = 'IL=10m'
%plotPZ('root locus I_L=10m Step I_source', rootlocus, [-2e7,0], [-1e7,1e7]);
%
```

```
defPar('I_L','100m');
stepVar('I_N');
stepStart('3u');
stepStop('3.5m');
stepNum(200);
stepMethod('lin');
Step('true');
simType('numeric');
gainType('gain');
dataType('poles');
RLStepIsourceIL100m = execute();
RLStepIsourceIL100m.gainType = 'IL=100m'
%plotPZ('root locus I_L=100m Step I_source', rootlocus, [-2e7,0], [-1e7,1e7]);
%
defPar('I_L','250m');
stepVar('I_N');
stepStart('3u');
stepStop('3.5m');
stepNum(200);
stepMethod('lin');
Step('true');
simType('numeric');
gainType('gain');
dataType('poles');
RLStepIsourceIL250m = execute();
RLStepIsourceIL250m.gainType = 'IL=250m'
%plotPZ('root locus I_L=250m Step I_source', rootlocus, [-2e7,0], [-1e7,1e7]);
%
```

```
plotPZ('Root
loci',[RLStepIsourceIL3u,RLStepIsourceIL10u,RLStepIsourceIL100u,RLStepIsourceIL1m,RLStepIsourceIL10
m,RLStepIsourceIL100m,RLStepIsourceIL250m],'auto', 'auto');

%

params2html();

dataType('Laplace');

result = execute();

loopgain.laplace = result.results(1);

syms 'G';

eqn2html(G, loopgain.laplace);

servoBw = findServoBandwidth(loopgain.laplace);

lowPassData = servoBw(2);

f_h = lowPassData(1);

stophtml();
```

10.2.4 Root Locus analysis for determining the value of R_s

```
slicap()

makeNetlist('translevel_trial_cd', 'translevel_trial_cd');

errors = checkCircuit('translevel_trial_cd');

htmlPage('Poles and zeros of gain');

simType('numeric');

dataType('poles');

gainType('gain');

source('V1');

detector('V_out');

lgRef('Gm_M1_X1');

defPar('c_dg_X1',0);

defPar('c_dg_X2',0);

defPar('c_dg_X3',0);

defPar('R_s',1);
```

```
%defPar('c_gs_X1','1a');
%Why put this to 0: To make the asymptotic gain equal to the ideal gain at
%high frequencies.
%defPar('C_1', 0);
gain=execute();
pz2html(gain);
%root locus
stepVar('R_s');
stepStart('1');
stepStop('500');
stepNum(200);
stepMethod('lin');
Step('true');
simType('numeric');
dataType('poles');
rootlocus = execute();
plotPZ('root locus step I_L', rootlocus, 'auto', 'auto')
```

10.2.5 Generating Bode Plots

```
slicap()
makeNetlist('loopgainoftranslevel', 'loopgainoftranslevel');
errors = checkCircuit('loopgainoftranslevel');
htmlPage('loopgain');
simType('numeric');
dataType('Laplace');
gainType('loopgain');
source('V1');
detector('V_out');
```

```
lgRef('E1');
defPar('I_L','10u');
%defPar('c_dg_X1',0);
%defPar('c_gs_X1','1a');
%Why put this to 0: To make the asymptotic gain equal to the ideal gain at
%high frequencies.
%defPar('C_1', 0);
loopgain10u=execute();
loopgain10u.gainType = 'I_L=10u'
%loopgain.laplace = result.results(1);
%servoBw = findServoBandwidth(loopgain.laplace);
%lowPassData = servoBw(2);
%f_h = lowPassData(1);
defPar('I_L','1.257e-4');
loopgain1257=execute();
loopgain1257.gainType = 'I_L=1.257e-4'
defPar('I_L','1.58e-3');
loopgain158=execute();
loopgain158.gainType = 'I_L=1.58e-3'
defPar('I_L','1.99e-2');
loopgain199=execute();
loopgain199.gainType = 'I_L=1.99e-2'
defPar('I_L','0.25');
loopgain250m=execute();
loopgain250m.gainType = 'I_L=250mA'
stophtml();
%There is no perfect model for certain circuit, but there is a perfect model for
%certain purpose.
```

```
plotdBmag('loopgain magnitude', [loopgain10u,loopgain1257,loopgain158,loopgain199,loopgain250m], 1, 1e9, 200)

plotPhase('Phase', [loopgain10u,loopgain1257,loopgain158,loopgain199,loopgain250m], 1, 1e9, 200)
```

10.2.6 Verification of conceptual active compensation

```
clear all;

slicap()

makeNetlist('cd_smallsignal_nocom', 'cd_smallsignal_nocom');

errors = checkCircuit('cd_smallsignal_nocom');

htmlPage('Poles and zeros of gain');

simType('numeric');

dataType('pz');

gainType('gain');

source('V1');

detector('V_out');

lgRef('G1');

%defPar('c_dg_X1',0);

%defPar('c_gs_X1','1a');

%Why put this to 0: To make the asymptotic gain equal to the ideal gain at

%high frequencies.

%defPar('C_1', 0);

gain=execute();

pz2html(gain);

params2html();

dataType('Laplace');

result = execute();

gain.laplace = result.results(1);

%transferCoeffs = coeffsTransfer(loopgain.laplace);

%coeffsTransfer2html(transferCoeffs);

syms 'L';
```

```
eqn2html(L, gain.laplace)

servoBw = findServoBandwidth(gain.laplace);

lowPassData = servoBw(2);

f_h = lowPassData(1);

stophtml();
```

10.3 PCB and Packaging calculation result

Height(μm)	Width(μm)	Thickness(μm)	Inductance(10^{-7}H/m)	Capacitance(10^{-11}F/m)
250	25	18	7.3	3.9
700	70	18	8.05	3.5
1500	150	18	8.3	3.4
1600	300	18	7.2	3.9
1600	660	18	5.7	5
250	25	35	6.6	4.3
700	70	35	7.6	3.7
1500	150	35	8.1	3.5
1600	300	35	7.1	4
1600	660	35	5.7	5
250	25	70	5.6	5.1
700	70	70	7	4.1
1500	150	70	7.7	3.7
1600	300	70	6.8	4.2
1600	660	70	5.5	5.1
100	25	18	5.5	5.2
100	70	18	4.2	6.8
100	150	18	2.9	9.7
100	300	18	1.7	17
220	660	18	1.8	16.1
100	25	35	4.8	6
100	70	35	3.8	7.6
100	150	35	2.7	10
100	300	35	1.6	18.4
220	660	35	1.7	16.7
100	25	70	3.8	7.5
100	70	70	3.1	9.2
100	150	70	2.3	12.4
100	300	70	1.3	21.7
220	660	70	1.6	18

Table 10-1 Unit capacitance and unit inductance in the PCB model

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