Energy-Efficient High-Voltage Driver

for High-Frequency Ultrasound Medical Applications

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by

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Acknowledgment

Two years ago when I first came to Delft, I was alone and terrified. I have no idea whether I can adapt to my new life abroad, whether I can keep up with the courses, or whether I can make any new friends. But there is one thing for sure, I wish to get involved in the biomedical field and learn how to provide medical solutions through the circuit level. I always dream about alleviating the pain of patients and improving people's quality of life. Although life is hard sometimes, this dream has become a powerful arm to overcome any obstacles. Therefore, I joined the Bioelectronics group and basically completed all recommended courses. I started getting in touch with noninvasive brain stimulation, organs-on-chips, and electroceuticals. Also, I learned medical diagnosis methods like MRI, CT, and PET. And I was so excited to know the idea about implants and vagus nerve stimulation from the class on Active Implantable Biomedical Microsystems. I always hope to design a medical device that can help people out and I can tell from my lectures that this dream has already come true.

Since my two-year's journey as a master student is coming to an end, I really need to express thanks to those who helped me. First of all, I would like to thank my supervisor Tiago. It is my privilege to join his friendly and supportive group. Whenever I encounter difficulties, he is always willing to give me kind and useful help and answer my questions patiently. I am so lucky to have a supervisor who can offer me a cozy and friendly working environment and give me the courage to overcome difficulties. Secondly, I really need to thank my daily supervisor Hassan who taught me everything about circuits patiently. With the lead of Hassan, I gained more insight into IC design. He is my role model who stuck with me through the hard times. Thirdly, many thanks to MIND group members Gandhi, Francesc, Niels Burghoorn, Niels Van Lith, Reka and Patricija. The working environment of the MIND team is the best I have ever met and everyone is so friendly and supportive to me. I am so lucky to know all of you. A special thanks to Wenyu who accompanies me through the rough times and spares no effort to help me solve all kinds of problems.

In the end, a big thanks to my friends and family who always give me support and love. You always provide an emotional anchor for me to follow my dream. In the past two years I met so many good friends and professors who would like to help and support me. I am so happy to have all of you. I was not alone and I gained a lot from the past two years. Hope I can still have so many good friends in the next journey and keep going toward my dream.

Yidi Xiao
Delft, September 2022

Abstract

Noninvasive brain stimulation plays an essential role in diagnosing and treating diseases of the brain. This stimulation can affect disease-related changes in brain activation, inhibition, or connectivity. Ultrasound neuromodulation is a rapidly growing field of noninvasive brain stimulation. In a form of acoustic pressure waves, ultrasound can transmit mechanical forces to modulate neurons. The acoustic waves can be focused on a particular location with a spatial resolution that depends on the set frequency. Compared to other noninvasive brain stimulation methods, ultrasound neuromodulation is a safe and reversible method that can be used to accurately simulate neuronal circuits for the treatment of neurological diseases.

New medical ultrasound solutions, from ultrasound imaging to ultrasound neuromodulation and ultrasonic powering of medical implants, require a wearable form factor and low power consumption. In these applications, pulsers are the most power-hungry block since they deliver high voltages to the ultrasound transducers and transducers contain massive parasitic capacitance. The ultrasound transducer needs to be driven by a high voltage (HV) square wave so that it can generate desired pressure for ultrasound brain stimulation. Therefore, improving the power efficiency of the driver part is very important for the whole system.

The purpose of this thesis is to design an energy-efficient driver within a limited area. There are two energy-consuming parts in the driver circuit. One is the parasitic capacitance of HV transistors, and the other is the capacitance of the transducer. In order to achieve HV operations, the driver part is typically implemented with HV transistors which have massive parasitic capacitance and also consume large areas. To solve this problem, stacked 5 V CMOS transistors are implemented to replace HV transistors. As for the energy loss due to charging and discharging the ultrasound transducer, many energy-saving methods are introduced in the literature such as energy-replenishing technique, charge redistribution method, and multi-level pulse-shaping technique. The proposed design compared the advantages and disadvantages of these methods and made some improvements on the basis of these techniques.

This work presents a power-efficient high-voltage pulser to drive integrated lead zirconate titanate (PZT) ultrasound transducers for ultrasound medical applications. The proposed pulser employs charge redistribution technique by utilizing a storage capacitor to save part of the charges before discharging the transducer. Furthermore, HV transistors are replaced by stacked 5V CMOS transistors that allow delivering 10 V to the piezo transducer. The pulser is designed and simulated in 180nm CMOS technology with 10 V power supply and 15 MHz operating frequency. The simulation results demonstrate that the proposed circuit improves the power efficiency by 30.55% compared to the traditional class-D pulser.

Contents

1 Introduction

1.1. Ultrasound Neuromodulation

So far, the demands for accurate and painless diagnosis and therapy of neurological and psychiatric disorders have increased dramatically. Neuromodulation has been realized through different aspects like chemical, optical, electrical, electromagnetic, and acoustic methods [1]. As for the electrical way, Deep Brain Stimulation (DBS) is an invasive therapy invented decades ago to treat Parkinson's disease and made a large difference in neurology. However, there are risks associated with every surgery. Transcranial Brain Stimulation (TBS) technology appeared as an alternative to DBS, capable of modulating neuron excitement without surgery. The major noninvasive ways like transcranial magnetic stimulation (TMS), and transcranial direct-current stimulation (tDCS), suffer from poor spatial resolution of centimeter (cm) scale and limited depth of penetration [2]. The comparison between different neuromodulation approaches in terms of their spatial coverage, resolution, and invasiveness has shown in Fig. 1.2.

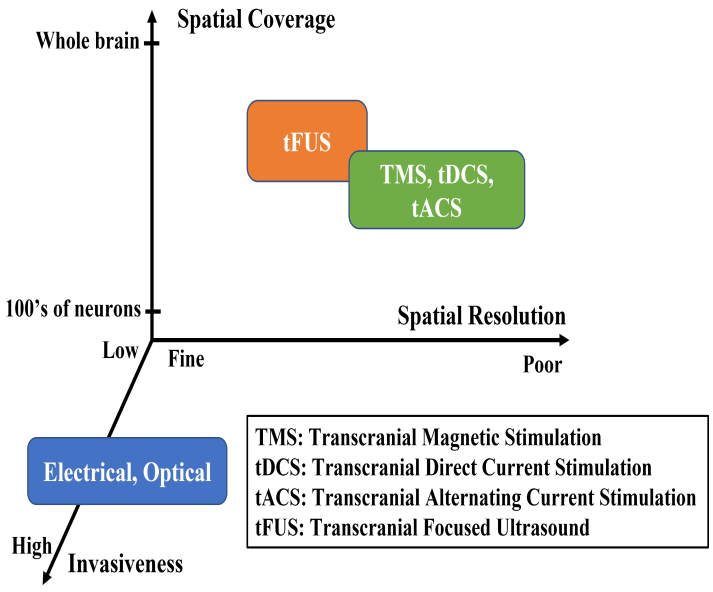


Figure 1.1: Comparison of different neuromodulation approaches in terms of their spatial coverage, spatial resolution, and invasiveness [1].

Ultrasound neuromodulation is a brain stimulation modality that is safe, reversible, and can stimulate neural circuits for the treatment of neurological diseases. Compared to the other neuromodulation methods like TMS and tDCS, ultrasound neuromodulation can penetrate deep regions and achieves higher spatial resolution [3]. Low-intensity focused ultrasound (LIFUS) is an attractive non-surgical

experimental method to modulate brain activity [4]. The major principle is to inhibit cortical evoked potentials, interfere with cortical oscillatory dynamics, and control the state of sensory or motor by an ultrasound transducer. Modern ultrasound medical solutions like ultrasound diagnostic imaging, ultrasound power transfer for medical implants, and ultrasound neuromodulation have emerged and developed rapidly. Ultrasound has been used in the clinical field since the 1920s and has shown the ability to affect excitable tissues [5]. As a kind of sound wave with a frequency of over 20 kHz, ultrasonic waves provide impressive properties like low scattering, low attenuation, and safe energy levels when propagating and interacting with tissue [6]. In the future, ultrasound neuromodulation has the potential to become a low-cost and high-resolution noninvasive method to solve both conscious and unconscious mental illness and disturbance [7].

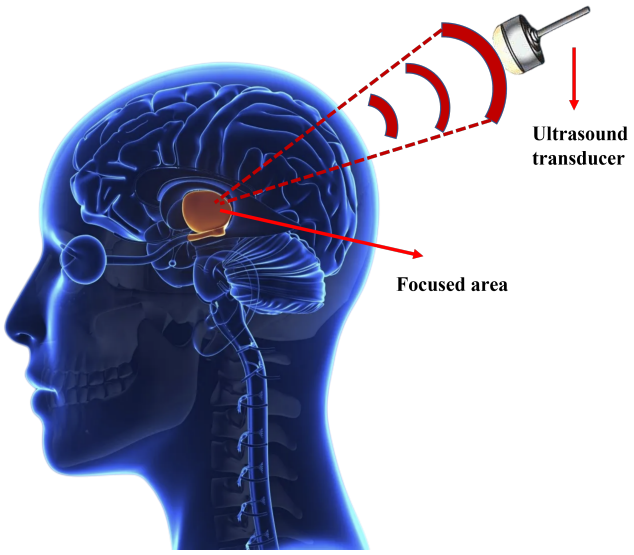


Figure 1.2: Ultrasound neuromodulation working principle.

1.2. 2D phased array of ultrasound transducers

Traditional ultrasound transducers use piezoelectric crystals to convert electrical energy into vibrations in the form of ultrasonic waves [8]. Ultrasound is usually generated by sending a time-varying voltage to a piezoelectric transducer. Due to the piezoelectric effect, when there is an input of a varying voltage, the piezoelectric material begins to vibrate. This vibration generates ultrasonic waves and propagates into the medium. Conventional ultrasound transducers have limitations because of bulky size, high production costs, and the difficulty of electronically steering and focusing ultrasound waves. These single-element-focused transducers have large sizes and require physical movement of the transducer to change the focus position. In order to overcome these limitations, in recent years, many works have reported employing a 2D phased array of ultrasound transducers as a steerable source of generating ultrasound waves. Advancements in the applications such as implantable devices, ultrasonic wireless power delivery, and ultrasound neuromodulation demand power-efficient, and wearable form factor 2D ultrasound transducers [6]. These devices consist of an integrated circuit and a 2D array of piezoelectric transducers, which are implemented on top of the IC. The integrated circuit part includes an array of driving circuits, each including a beamforming circuit and a pulser, which drive the transducers with a signal which contains a pre-determined phase towards two-dimensional beam steering and focusing. Since most of the power in a 2D array of US transducers consume by pulsers, a power efficient pulser is required to decrease the overall power consumption.

Ultrasound neuromodulation requires continuous-wave signals for allowing higher available power in ultrasound-powered implantable devices and for meeting the pulse duration (PD) specifications of ultrasound neuromodulation. An arbitrary PD is easier to be realized with a single enabled input signal compared to pulsed-mode ultrasound that requires complex counter-based approaches. Also, a higher

spatial resolution for the ultrasound focal spot can be achieved by increasing the ultrasound frequency.

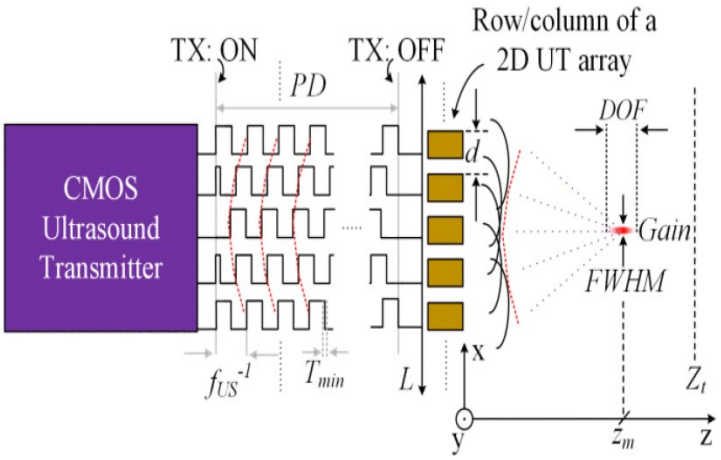


Figure 1.3: The working principle of 2D ultrasound phased array transmitter [6].

As shown in Fig. 1.3, a CMOS ultrasound transmitter is programmed to generate driving signals with a given frequency (f_{US}), PD, and a delay with a given timing resolution (T_{min}). These signals will be applied to 2D array piezoelectric transducers with an aperture L and an inter-element pitch d. With well-defined delays for 2D beamforming, the piezoelectric transducers generate focused ultrasound waves at a pre-determined depth (Z_m, up to a maximum Z_t) and steering angle, in both the XZ (θ_{XZ}) and YZ planes (θ_{YZ}). The focal spot properties are characterized by the full width at half maximum (FHWM), the depth of field (DOF), and the focusing gain (Gain) [6]. Although nowadays, CMUT (capacitive micromachined ultrasound transducer) and PMUT (piezoelectric micromachined ultrasound transducers) have been developed to replace piezoelectric transducers in ultrasound imaging applications, piezoelectric technology shows better performance in ultrasound neuromodulation for its higher transmit electroacoustic sensitivity (S_{tx}) [9]. Hence, this work focuses on piezoelectric transducers to generate ultrasonic waves.

1.3. Pulsers for ultrasound transducers

A pulser driving an ultrasound transducer is the most power-hungry block in ultrasound neuromodulation systems since the transducer has a large equivalent capacitance and a low parallel resistance [10]. Therefore, the main task is to find ways that can effectively reduce the power consumption of pulsers. The basic working principle is illustrated in Fig. 1.4. However, conventional high voltage (HV) pulser employs two HV transistors which not only occupy a large area but also add large parasitic capacitance to the output node that increases the dynamic power consumption [11]. There are two challenges in designing a power-efficient pulser for ultrasound transducers. One is to increase power efficiency on the basis of high driving voltages because the driving voltage must be as high as possible to generate maximum pressure at the surface of the piezoelectric element. Typically, the pulser should deliver a square wave with an amplitude of 10 V or more so that it can enable the transducer to generate enough pressure for ultrasound brain stimulation. Secondly, the circuit must be implemented in a limited area. Since the size of one channel is limited in by half of the ultrasound wavelength, high frequency leads to a smaller focal spot size [12]. Therefore, 2D array of ultrasound transducers require a high operating frequency to improve intensity at the focal spot and the volumetric resolution. Consequently, the ultrasound transducer needs to be driven by a relatively high voltage while implemented in a small area.

In order to reduce the occupied area, [13] has replaced the HV transistors with a stack of low voltage transistors. In spite of the fact that removing the HV transistors leads to fewer parasitic capacitance, the parasitic capacitance of the US transducer, C_p, plays the most significant role in the power consumption of a pulser [10]. To overcome the energy loss by the parasitic capacitance of the US transducer, [10] has used the energy replenishing technique that can achieve zero C_pV^2f loss by storing and reusing the energy in an inductor. Nevertheless, implementing an on-chip inductor occupies a large area. A multi-level pulse-shaping technique has been introduced by [14]. As hown in Fig. 1.5, it reduces the

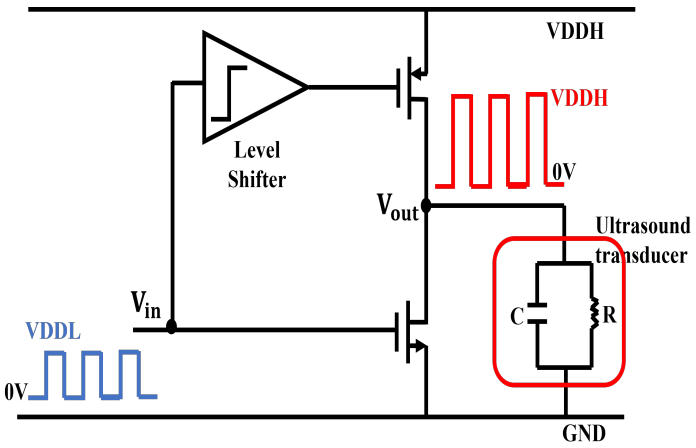


Figure 1.4: The working principle of ultrasound pulsers.

energy loss by charging and discharging ultrasound transducers in multiple voltage steps (N) so that the dynamic power loss by C_p can be reduced from C_pV^2f to $C_pV^2f/(N-1)$. Although increasing N improves the power efficiency, it complicates the circuit as well. [15] has used a charge redistribution method. In the discharging phase, this technique connects both plates of the US transducer together, which results in 50% energy-saving ideally. However, this technique is only suitable for CMUTs and PMUTs where both plates of the ultrasound transducer are accessible.

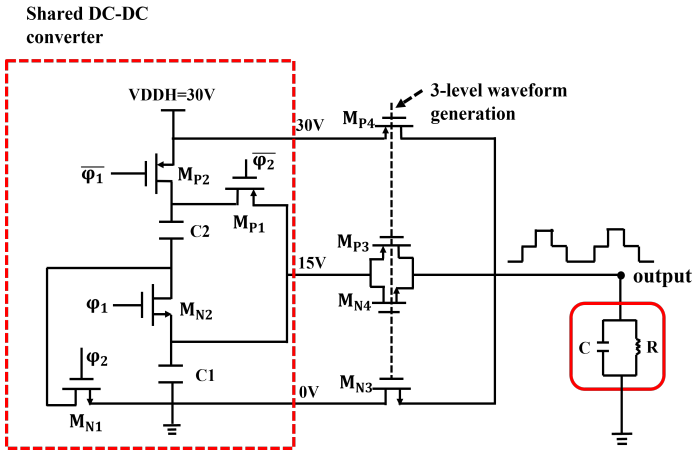


Figure 1.5: The schematic of the multi-level pulse-shaping technique adapted from [14].

The aim of this thesis is to design a power-efficient driver for ultrasound transducers and find a superior one based on the trade-off between power and area consumption. The proposed method analyzes the advantages and disadvantages of the current energy-saving techniques and improves the charge redistribution method that is suitable for all ultrasound transducer types. Furthermore, by utilizing a stack of low voltage transistors, both the driver area and the capacitance at the output node are decreased. In this work, the power efficiency of the ultrasound transmitter circuit, one of the major bottlenecks of this solution, is investigated and an optimized transmitter architecture is proposed.

2

Energy efficient ultrasound transducer drivers

2.1. The structure of high voltage drivers

2.1.1. Equivalent circuit model of ultrasound transducers

The equivalent model of ultrasound transducers can be represented as the Butterworth-Van-Dyke (BVD) model illustrated in Fig. 2.1 (a). R_m represents acoustic emission and motional loss. C_m and L_m are motional mass and compliance, respectively, and C_p is parasitic capacitance [16]. Electrical energy can be converted into acoustic energy when ultrasound transducers are driven by pulses. The ultrasound transducer acts like a band-pass filter (BPF) with two resonance frequencies ω_s and ω_p in the frequency domain, where ω_s and ω_p are the series and parallel angular resonance frequencies, respectively. Since the reactance of one ultrasound transducer typically appears at a frequency between ω_s and ω_p, the transducer model can be simplified as a parallel connection between one resistor and one capacitor [17], [18]. Therefore, this work uses the simplified model shown in Fig. 2.1 (b) to represent the ultrasound transducer.

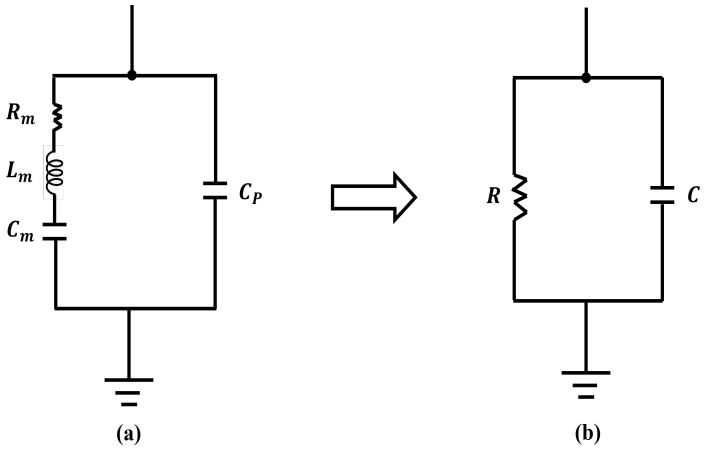


Figure 2.1: (a) Butterworth-Van-Dyke (BVD) model of ultrasound transducers (b) Equivalent simplified circuit model of ultrasound transducers [18].

2.1.2. Conventional class-D high voltage driver

Typically, the high voltage driver comprises a level shifting stage and a high voltage switch as the output stage as shown in Fig. 2.2. A class-D design is the simplest and most widely used pulser structure [10] while suffering from excessive $C_P V_{DDH}^2 f$ loss caused by a large parasitic capacitance C_P driven by a high supply voltage. Double-diffused MOS (DMOS) transistors have been widely used in the level

shifter and the output driver block to avoid device breakdown due to the high voltage driving signals [19]. And large-sized transistors are implemented to achieve low on-resistances [18]. However, even for the high voltage transistors like HV CMOS, DMOS, and LDMOS that can tolerate high drain-source voltages (V_{DS}), the allowable gate-source voltage (V_{GS}) of them is limited to 6V [11]. Consequently, a gate driver with a floating ground (LV1) at the level of $V_{DDH} - |V_{GS}|$ is required to make sure the safety of the PMOS transistor. LV2 represents a low supply voltage, which in this work is 5 V.

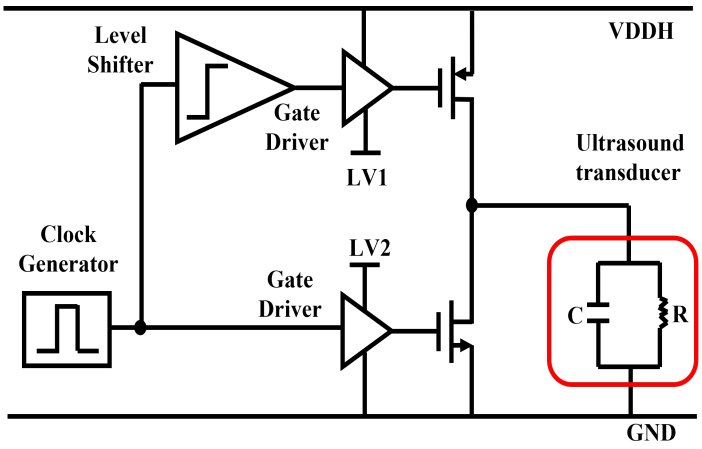


Figure 2.2: High voltage (HV) pulser based on class-D design adapted from [18].

As shown in Fig. 2.2, when the input signal switches to a lower voltage level, the PMOS transistor turns on and charges the ultrasound transducer to V_{DDH}. When a capacitor is charged from ground to V_{DDH}, the energy stored in the capacitor is

$$E_1 = \int_0^\infty I(t)V(t)dt = \int_0^\infty C_P \frac{dV}{dt} V(t)dt = C_P \int_0^{V_{DDH}} V(t)dV = \frac{1}{2} C_P V_{DDH}^2 \tag{2.1}$$

During the charging phase, the energy that the power supply dissipates is

$$E_2 = \int_0^\infty I(t)V_{DDH}dt = \int_0^\infty C_P \frac{dV}{dt} V_{DDH}dt = C_P V_{DDH} \int_0^{V_{DDH}} dV = C_P V_{DDH}^2 \tag{2.2}$$

Therefore, half of the energy ($E_2 - E_1 = \frac{1}{2} C_P V_{DDH}^2$) from the power supply is dissipated for charging the capacitor to V_{DDH}. The other half is converted into heat when dissipated in the pMOS transistor because the transistor has a voltage across it and a current flows through it at the same time [20].

As for the discharging phase, there is no energy delivered from the power supply, and the energy stored in the capacitor ($E_1 = \frac{1}{2} C_P V_{DDH}^2$) is dissipated in the NMOS transistor. When the input signal switches to a higher level, the NMOS transistor turns on while the PMOS transistor turns off so that the capacitor inside the transducer will be discharged.

So overall, since the pulser should charge and discharge the transducer every cycle, a dynamic power loss of $C_p V_{DDH}^2$ occurs. Also, from the above equations, the energy dissipation only depends on the load capacitance instead of the size of the transistor or the frequency of the gate switches. However, the dissipated power depends on the frequency of the gate switches. Suppose the ultrasound transducer is charged and discharged at an average frequency f_{sw}. Over some interval T, the transducer will be charged and discharged $T f_{sw}$ times. Then, the average power dissipation is

$$P = \frac{E}{T} = \frac{T f_{sw} C_P V_{DDH}^2}{T} = C_P V_{DDH}^2 f_{sw} \tag{2.3}$$

Since the driver part is the most power-hungry block due to the parasitic capacitance of the transducer, the main target of this thesis is to improve its power efficiency. Also, if a series of pulsers can be used to transmit large acoustic energy through a high-frequency transducer instead of a single pulse, the dynamic power consumption of the driving part will increase linearly with the number of pulses [18]. So, it is very important to reduce the power consumption caused by C_p for the pulser to deliver more energy to the transducer.

2.1.3. Level shifter

Level shifter is used to convert the voltage level of an input signal to another voltage level at the output node. The schematic of two conventional basic level shifters is shown in Fig. 2.3 [21]. The principle of the circuits is as follows: when there is a low-to-high signal applied at the input stage, M_{N1} turns on. This makes the node on the drain of MN1 discharged to ground so that M_{P2} turns on. Then, the output node can charge to the specific high voltage V_{DDH}. The advantage of the conventional differential cascade voltage switch (DCVS) topology is it exhibits very low static power. Nevertheless, it suffers from the current contention between the pull-up network (PUN) and pull-down network (PDN) during the switching signal of the output, which can affect both the switching time and the dynamic power consumption. As for the current mirror (CM)-based circuit, the power dissipation type is the opposite: the problem caused by current contention is neglectable while the static current flowing through M_{P1} and M_{N1} the huge when the output signal is high [21].

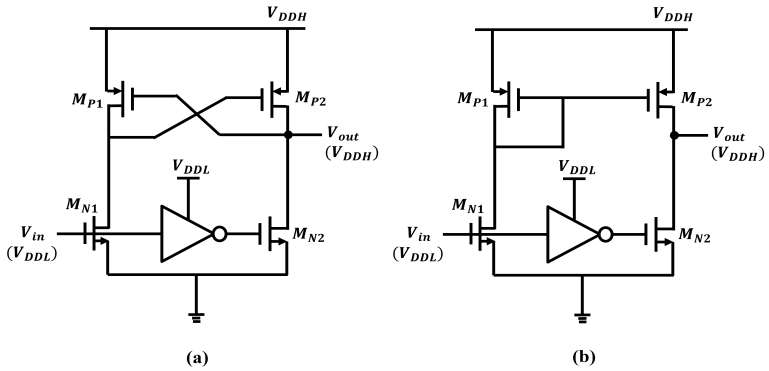


Figure 2.3: Two conventional level shifter topologies adapted from [21].

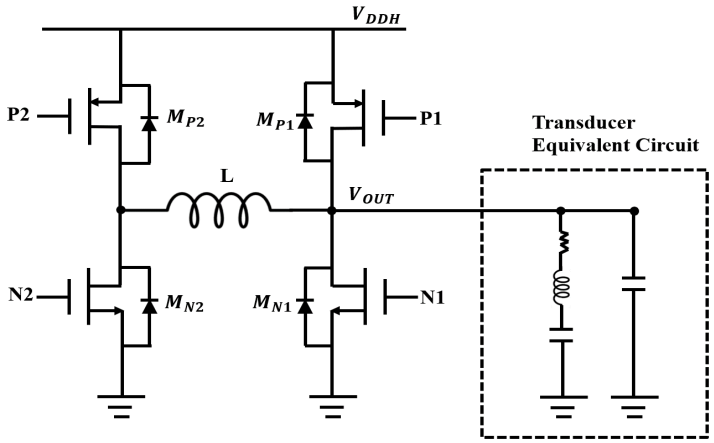


Figure 2.4: The structure of the energy-replenishing circuit adapted from [10].

2.2. A review of power efficiency optimization strategies

2.2.1. Energy-replenishing technique

An energy-replenishing (ER) pulser is proposed by Choi et al., which can ideally achieve zero C_pV^2f loss by replenishing the supplied energy from the energy stored in an inductor [10]. The structure is shown in Fig. 2.4. The ER pulser consists of 4 high-voltage power switches (M_{P1-2} and M_{N1-2}), an inductor (L), and a $\Delta\Sigma$-based switching time controller ($\Delta\Sigma$-STC) that provides gate voltages for 4 power switches. The basic principle is separated into four phases, Φ_1 to Φ_4. During the phase Φ_1, M_{P2} turns on while current I_{IND} flows from V_{DDH} to the transducer and charges the inductor L and capacitor C_p. When the output node is charged to V_{DDH}, every switch is open and Φ_2 starts. During the

phase Φ_2, the inductor energy forces I_{IND} to flow through parasitic junction diodes of M_{N2} and M_{P1} to return its own energy stored during Φ_1 to the power supply and V_{OUT} is restored to V_{DDH}. Instead of discharging the capacitor in Φ_3, turning on M_{N2} can transfer the energy inside C_p into magnetic energy in L. When V_{OUT} is discharged to 0 V, Φ_4 is triggered to return the energy stored in L during Φ_3 to the power supply. Therefore, all the energy coming from the power supply to charge C_P during Φ_1 is returned to the supply during Φ_2 and Φ_4. Although this energy replenishing method can achieve 100% energy efficiency with the help of an inductor, this technique is abandoned because inductors consume large areas in IC technology. However, the idea can be implemented by replacing inductors with other components such as capacitors or transistors.

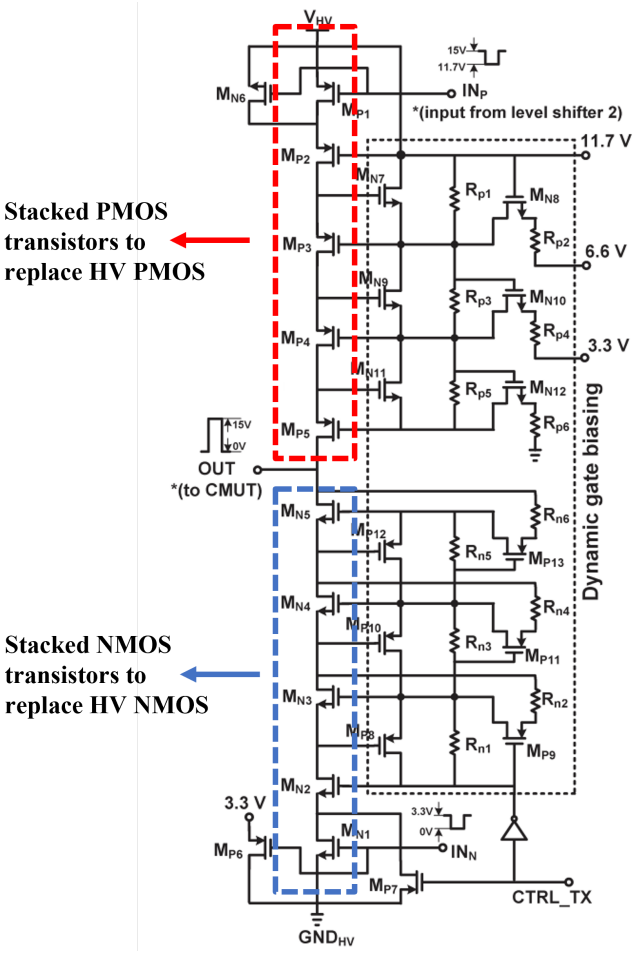


Figure 2.5: The schematic circuit of self-biased topology adapted from [19].

2.2.2. Stacked architecture

HV transistors have many disadvantages like limited V_{GS}, high process cost, large size, and huge parasitic capacitance [13]. Also, since the on-resistance of these transistors is larger than that of standard CMOS transistors, the sizing has to be sufficiently large so that the ultrasound transducer can be driven to a high voltage at megahertz frequencies. To overcome these problems, Serneels et al. proposed to use stacked standard CMOS transistors to replace those HV transistors. The stacked architecture is shown in Fig. 2.5 [22]. The stacked CMOS topology works simply. Several regular CMOS transistors are stacked together to share a high voltage. The number of transistors depends on how each shared voltage keeps the drain-source voltage (V_{DS}) of each transistor at a safe level.

The goal of stacked architecture is to find the correct operating point so that the voltage can be limited across the terminals of the transistors. In the case shown in Fig. 2.5, transistors M_{N1-5} and M_{P1-5} are used to divide the HV voltage of 15 V into equal shares so that each transistor can work at a safe level (within 3 V). In this way, 5-stacks of standard 3.3 V transistors are used to support a

15-V_{pp} pulse signal with dynamic gate biasing circuits that can guarantee the voltages between the four terminals of each transistor are within 3.3 V.

HV output driver with dynamic gate biasing

Since we are using stacked architecture of standard CMOS transistors to replace HV transistors, dynamic gate biasing is very important to make sure that the voltage between every terminal of NMOS and PMOS transistors in the stacks is within the margin without oxide or junction breakdown during ON-OFF and OFF-ON transitions.

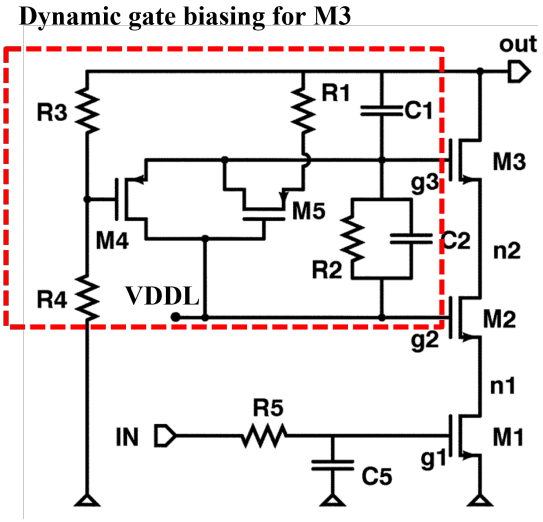


Figure 2.6: The schematic circuit of self-biased cascode topology adapted from [22].

Serneels et al. have proposed a self-biased cascode topology where the bias voltage of the transistors closest to the output depends on the output voltage [22]. Fig. 2.6 has shown the circuit of the n-switch block. The topology for the p-switch block would be the same since it is the complement of the n-switch block. The gate voltage is quite easy to set for M1 and M2. R_5 and C_5 are used as low-pass filters to soften the transitions at g1 since node 2 must be discharged with the same speed as node 1 to prevent hot carrier effects caused by a large drain-source voltage. The gate of M2 is connected to an LV power supply that can make sure M2 can be turned on when the source is discharged. The tricky part is the gate driver of M3. This topology sets the bias voltage of transistor M3 in two ways: one is through a resistor division comprised of R_1 and R_2, triggered by M_5, or by the gate voltage of M_2 which passes through M_4. The increased gate-drain capacitance of M_3 operates with the resistances R_1 and R_2 as a high-pass filter and capacitance C_2 is added which acts as a low-pass filter for the transient overshoot on g3. And in this way, the MOS device can be protected from high supply voltage without using the HV process.

Cha et al. proposed another design which is an improvement of the previous design [22] with a reduced number of passive components and overall complexity [13]. They removed the area-consuming capacitors and resistors since the parasitic gate-drain capacitance that causes the overshoot during ON–OFF transitions was not critical because of the lower operating frequency and smaller sizing of transistors. From Fig. 2.7, all the HV DMOS transistors are replaced with 5 V standard CMOS transistors. The working principle of the NMOS part is shown as followed: firstly, when IN_N experiences a low-to-high transition, it will make M_{N1} turn on, which will discharge the source node of M_{N2} and turn on M_{N2} since its gate is biased at $VDDL_1$. M_{P5} and M_{N3} will also turn on followed by the discharging of M_{N2}. The output node is also discharged and the voltage changes to $GND_{HV} + VDS_{MN1,2,3}$. From the circuit, we can see that the $VDS_{MN1,2,3}$ is equal to the voltage drop due to the dynamic current flowing through the output drain terminals multiplied by the combined R_{ON} resistance of M_{N1}, M_{N2}, and M_{N3}. Then, when there is a high-to-low transition in IN_N, M_{N1} will be turned off while M_{P4} is turned on. This will turn off M_{N2} since the gate and source nodes of M_{N2} will be biased at $VDDL_1$ when M_{P4} is turned on. Now, since the output voltage changes from low to high, M_{P6} can be triggered to turn on. Then, the gate voltage of M_{N3} is decided by the resistive division of R_4, $R_{ON,MP6}$, and R_3

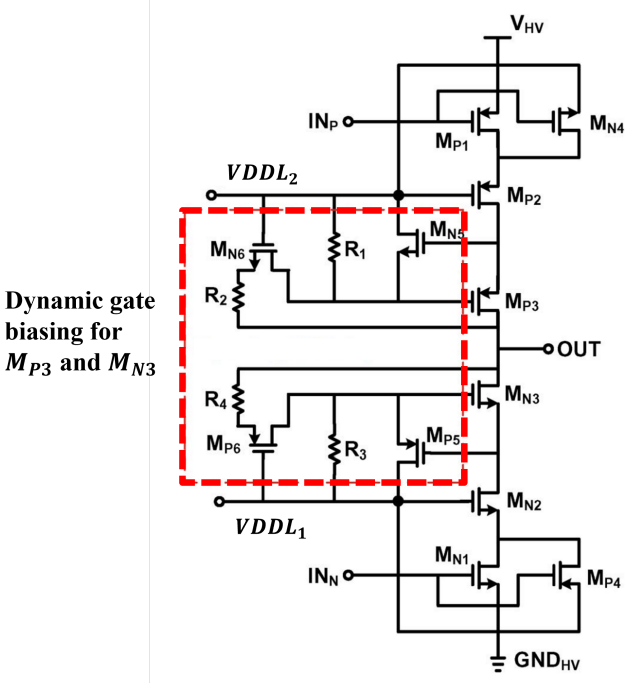


Figure 2.7: Dynamic gate biasing schematic circuit adapted from [13].

resistors between the output node and the bias voltage of M_{N2}. In this way, dynamic gate biasing can be realized.

Based on the previous design, another way to simplify the stacked architecture is shown in Fig. 2.8. Only standard 3.3 V transistors are used as the stacked switches as well as the dynamic gate biasing circuit that can keep the voltage across each terminal within 3.2 V to prevent breakdown due to high voltage. This topology is only implemented by transistors. By means of the property of the transistor itself, the principle of the driver circuit is as follows, firstly, when there is a low-to-high signal applied to the gate of M_{N1}, M_{N1} is turned on. And the source terminal of M_{N2} is discharged to the low voltage node. Since the voltage of the gate terminal of M_{N2} is 3.2 V, M_{N2} is also turned on so that the gate terminal of M_{BP1} is shorted to the low voltage node and M_{BP1} is also turned on. Therefore, the gate of M_{N3} is shorted to the 3.2V voltage, and M_{N3} is also turned on. Similarly, the M_{BP2} and M_{N4} are turned on so that the entire switch SW_1 is turned on. The operation of SW3 is applied in the same way. When the gate terminal of M_{P1} is applied by 9.6V from the level shifter, the M_{P1} switch is turned on. Also, since the source terminal of M_{P2} is shorted to a high voltage node and M_{BN1} is turned on. Similarly, M_{P3}, M_{BN2}, and M_{P4} switches are also turned on by the same operation so that the entire switch SW_3 is turned on. SW_2 and SW_4 will operate in the same way to achieve a high voltage output.

Power consumption of stacked architecture

Like HV pulsers, the overall architecture of pulser with stacked structure also consists of level shifters and an output driver. The stacked standard CMOS architecture will also be used in the part of level shifters to replace HV transistors. Typically, it requires two level shifters to transmit a small input signal like 1.8 V_{pp} to a medium pulse signal like 3.3 V_{pp} or 5 V_{pp}. Then this medium pulse signal will be set to two paths. One is sent to a lower path through an inverter to drive the gate of the NMOS transistor of the output driver. The upper path contains the second level shifter with stacked architecture and a tapered buffer to convert the medium pulse signal to the high voltage level like 20V to drive the gate of the PMOS transistor of the output driver. In the end, the output driver will be connected to the ultrasound transducer which can be driven by HV pulses to generate an ultrasound signal with sufficient acoustic pressure for propagation through the acoustic medium [24].

A simplified formula can represent the efficiency of the driver without considering dynamic power consumption [22]:

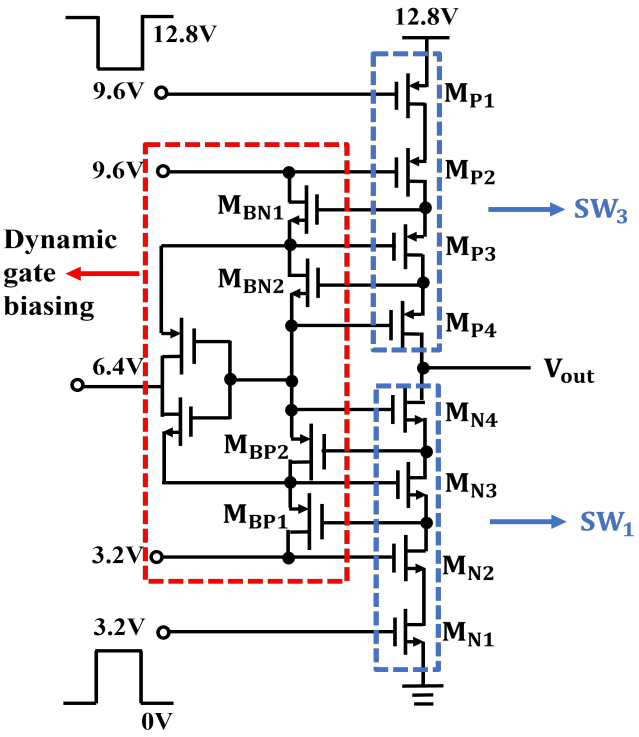


Figure 2.8: The schematic circuit of self-biased topology adapted from [23].

$$\eta = \frac{P_{out}}{P_{supply}} = \frac{R_{load}}{R_{load} + R_{on}}. \tag{2.4}$$

where R_{load} is the load resistance driven by the output driver and R_{on} represents the total on-resistance of the stacked transistors.

In the triode region, the simplified formula for the desired resistance of a transistor can determine the ratio of its width and length shown in Eq. (2.5).

$$\frac{W}{L} = \frac{m}{\mu_n C_{ox} R_{on} (V_{GS} - V_{th})}. \tag{2.5}$$

where m is the number of stacked transistors for every block.

In order to guarantee standard CMOS transistors can tolerate high voltages, we need more stacked transistors to make sure every transistor can work properly. Also, we can see from the equation that there is a trade-off between power and area consumption. Furthermore, for higher efficiency, dynamic power consumption becomes critical and plays an important role in the design circuit. In order to reduce the R_{on} resistance to minimize the voltage drop during the ON operation, the size ratio (W/L) of the output transistors needs to be large. However, a large area leads to large parasitic capacitance, which increases the occupied area as well as power consumption.

2.2.3. Charge-redistribution technique

Since the pulser should charge and discharge the transducer during each cycle, a dynamic power loss of $C_p V^2 f$ occurs. Instead of finding a way to reduce parasitic capacitance, charge-redistribution technique was presented in [15]. As shown in Fig. 2.9, when the discharging phase comes, both the top plate and the bottom plate are shorted with each other while the driving and ground electrodes are floated. With an equal electrode size and negligible leakage, the charge redistributes quickly to result in both electrodes being close to $V_{DDH}/2$ with the respect to the system ground. In the next charge cycle, the transducer can be charged from $V_{DDH}/2$ instead of charging from GND. Since each electrode charge or discharge by $V_{DDH}/2$, half of the initial charge from the transducer can be recycled for the next charge

cycle. The voltage difference between each plate of the transducer is equal to $V_{DDH}/2$, which is similar to the conventional drive circuit.

So, the energy stored in C_p is not discharged to the ground directly during the discharging phase but is transferred and stored inside the transducer so that part of the energy for charging C_p in the next operation cycle can be saved. Ideally, during each charging period, 50% of energy is saved since both ends of the transducer are shorted to make the two terminal voltages equal to $V_{DDH}/2$ instead of discharging C_p to the ground. In this way, the charge stored in each plate of the capacitor is $Q = \frac{1}{2}CV$. The conventional power consumption is $P = CV_{DDH}^2 f$ while the total power dissipated after using charge-redistribution method is $P = \frac{1}{2}CV_{DDH}^2 f$.

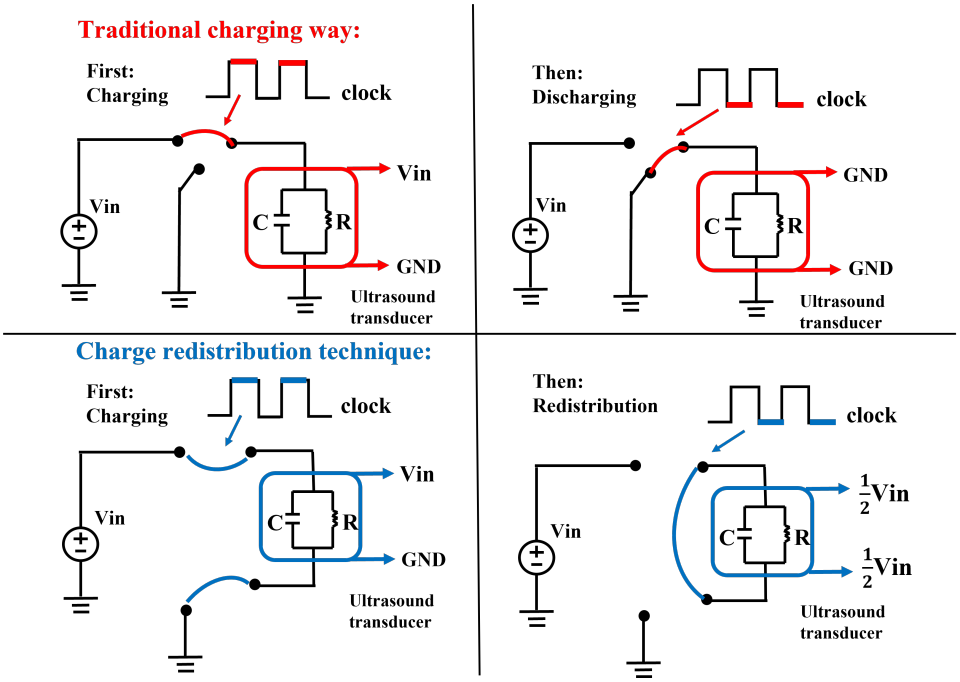


Figure 2.9: Comparison between a conventional pulser and a pulser employing charge redistribution technique with their operation waveforms observed at the pulser output and electrodes of the pMUT adapted from [15], [18].

However, this method is only suitable for CMUTs and PMUTs where both plates of the ultrasound transducer are accessible. Since in a phased array of piezoelectric transducers, one plate of piezoelectric transducers is always connected to the ground; therefore, the tricky problem is one terminal of PZT must be connected to the ground so that it is impossible to short the two ends of PZT like the charge redistribution method used in CMUT and PMUT.

2.2.4. Multi-level pulse-shaping technique

Multi-level pulse-shaping technique is to charge and discharge a transducer in multiple voltage steps (N) so that the dynamic power loss by C_p can be reduced from C_pV^2f to $C_pV^2f/(N-1)$ [14]. This method reduces the dynamic power consumption significantly by reducing the acquisition of meaningless energy in the power supply and recycling the charged energy partially to the power supply. The larger the number of voltage levels, the closer the signal waveform is to a sinusoidal wave so that more power can be saved. As shown in Fig. 2.10, the left part is a 2:1 parallel-series switched-capacitor DC-DC converter. With the help of HV transistors M_{N1}, M_{N2}, M_{P1}, and M_{P2}, capacitors are first connected in series in phase 1 (Φ_1) and then in parallel during phase 2 (Φ_2). In this way, a middle voltage of 15 V is generated from $V_{DDH} = 30V$. $M_{N3}, M_{N4}, M_{P3}, and M_{P4}$ are also HV transistors that are implemented in three-level pulse shaping topology. NMOS transistors M_{N3} and M_{N4} can realize transitions from 0 V to 15 V and from 15 V to 0 V, respectively, while PMOS transistors M_{P3} and M_{P4} are used for the transitions from 15 V to 30 V and from 30 V to 15 V, respectively. Since the on-resistance of each transistor can form an RC time constant with the capacitor in the ultrasound transducer, decreasing the value of on-resistance can reduce pulse voltage level settling time. The size of these transistors needs to

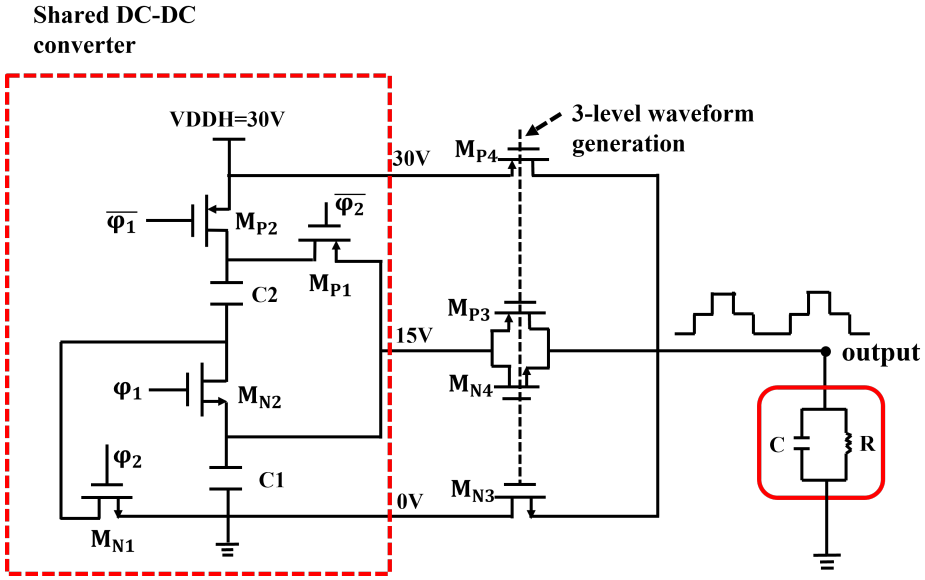


Figure 2.10: Multi-level pulse-shaping pulser and its output voltage waveforms adapted from [14].

be sufficiently large so that the on-resistance of each transistor can be relatively small.

Although this technique can reduce power consumption significantly from C_pV^2f to $C_pV^2f/(N-1)$, the topology requires generating additional voltage levels which consume extra areas and increase the overall system complexity, thus increasing power consumption. In addition, all the transistors need to be implemented as HV devices, which can cost huge area and power. So, even though it can save dynamic power consumption sufficiently, it is not an ideal method for a power-efficient driver for ultrasound transducers.

2.2.5. Discussion

This work aims to design an energy-efficient HV driver for ultrasound transducers. Since the parasitic capacitance inside the ultrasound transducer dominates the power consumption of the HV driver, finding a way to save part of the wasted charges can help to improve the power efficiency. To recycle these wasted charges through charging and discharging phases, [10] has used the energy replenishing technique that can achieve zero C_pV^2f loss by storing and reusing the energy in an inductor; [15] proposed the charge redistribution method that shorts both plates of the capacitor before discharging it to get $\frac{1}{2}C_pV^2f$ energy saving; a multi-level pulse-shaping technique has been introduced by [14] that reduces the energy loss by charging and discharging ultrasound transducers in multiple voltage steps (N) so that the dynamic power loss by C_p can be reduced from C_pV^2f to $C_pV^2f/(N-1)$. In addition, since HV transistors occupy a large area and contain high parasitic capacitance, [13] presented an idea to replace the HV transistors with a stack of LV transistors. This work studied the advantages and disadvantages of these published methods. The proposed HV energy-efficient driver combined the stacked architecture along with charge redistribution technique and can be applied to all ultrasound transducer types. In the next chapters, the proposed solution and its implementation and simulation results are discussed.

3

The proposed power-efficient HV driver

3.1. System level design

In order to improve power efficiency as well as reduce the area occupied by the circuit, this work presents a method that combines both stacked architecture and charge redistribution method. Since HV transistors have large parasitic capacitance and also occupy large areas, the proposed design uses standard 5V CMOS to replace HV devices. Also, this work applies the principle of charge redistribution technique to piezoelectric transducers because PZT material has better acoustic performance compared to CMUT and PMUT in ultrasound neuromodulation. Although charge redistribution method has been commonly used in CMUT and PMUT devices, it cannot be directly implemented on piezoelectric transducer since one terminal of the PZT transducer element in a phased array of ultrasound transducers is always connected to the ground due to the difficulty of the integration of PZT transducers and CMOS technology. In other words, a charge redistribution technique based on one terminal is required to save the delivered power to the piezo elements. In this regard, this work utilizes a parallel capacitor to the PZT transducer to save power, as shown in Fig. 3.1, and originally proposed by [25] for energy harvesting applications. Unlike the original charge redistribution method that stores part of the energy directly inside the ultrasound transducer, this method introduces another capacitor to store the energy that is going to be wasted by discharging the transducer to the ground. This storage capacitor is working as a bucket that can store part of the charges by connecting with the transducer. Before the next charging cycle comes, this storage capacitor will charge the transducer with charges stored inside the bucket so that the transducer can be charged efficiently.

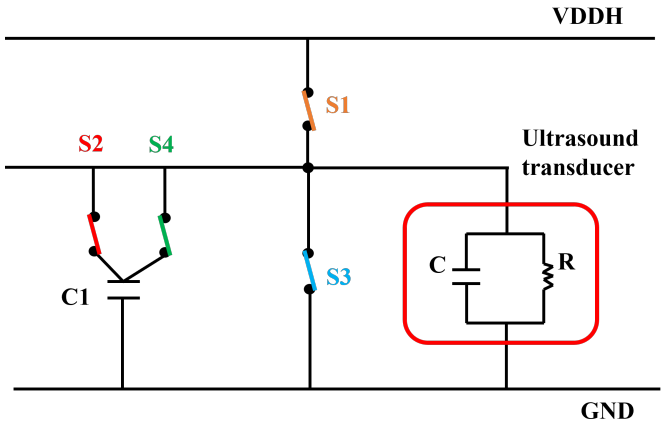


Figure 3.1: System level circuit of the proposed charge redistribution design with one storage capacitor.

As shown in 3.1, first of all, switch S_1 is closed to charge the ultrasound transducer to V_{DDH}. Then, the storage capacitor is connected with the transducer by closing switch S_2 so that C and C_1 can share the charges, After charging C_1, the transducer is discharged when S_3 is closed. In the end, switch S_4 is used to connect C_1 and the transducer again so that the charges stored in C_1 can be partially charged back to the transducer.

In order to save more power, more storage capacitors can be added. As shown in Fig. 3.2, two storage capacitors are used for saving more charges. After the transducer is charged to V_{DDH}, switches $S_{2,1}$ and $S_{2,2}$ will be closed step by step for storing charges and when the transducer is discharged to the ground, switches $S_{4,2}$ and $S_{4,1}$ will be closed for charging back to the transducer. Considering the robustness of the whole circuit, fast leakage of the load resistor, as well as power and area consumption of switches, the topology of two storage capacitors is chosen for the highest power efficiency.

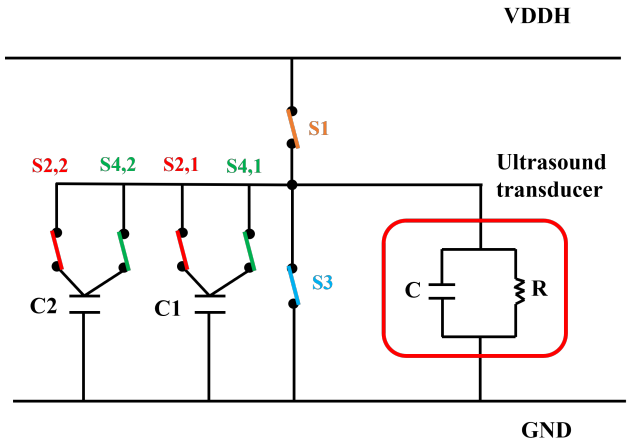


Figure 3.2: System level circuit of the proposed charge redistribution design with two storage capacitors in parallel when charging back to the transducer.

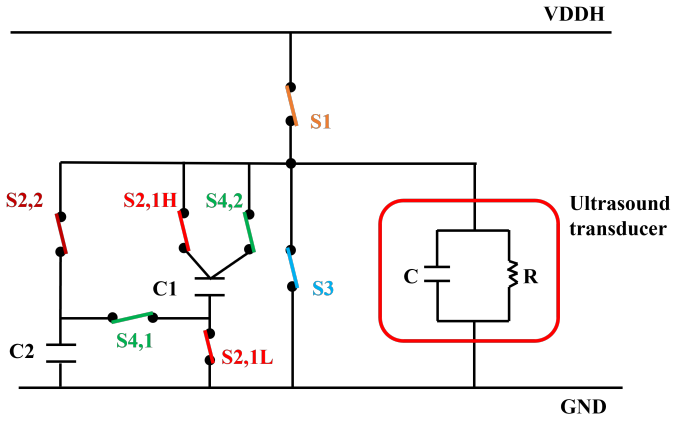


Figure 3.3: System level circuit of the proposed charge redistribution design with two storage capacitors in series when charging back to the transducer.

In high-frequency ultrasound medical applications, both power and area need to be minimized to allow narrow spacing in phase arrays and large transducer apertures [6]. Therefore, we face a trade-off between power and area consumption. In the proposed circuit of Fig. 3.3., we save area by reducing one switch in the charge redistribution scheme, while adding more power consumption. This way, instead of charging back to the transducer separately, storage capacitors are connected in series to charge back into the transducer in the final step. The basic principle of Fig. 3.3 is as follows: same as previous methods, the ultrasound transducer will be charged to V_{DDH} by closing switch S_1. Then, switches $S_{2,1H}$ and $S_{2,1L}$ are closed for the transducer charging capacitor C_1. when switches $S_{2,1H}$ and $S_{2,1L}$ are turned

off, switch $S_{2,2}$ is turned on to connect capacitor C_2 with the transducer. in this way, the transducer is discharged to the ground in three steps. As for charging back to the transducer, switches $S_{2,1H}$ and $S_{2,1L}$ are closed successively so that capacitors C_2 and C_1 are in series to charge the transducer.

3.2. Theoretical calculations

3.2.1. A common mistake

Theoretically, considering only one storage capacitor, it is easy to make a common mistake that when $C_1 = C_0$, the charging efficiency is the best. As shown in Fig. 3.4, assume the capacitances of the transducer and the storage capacitor are C_0 and C_1, respectively, and the transducer has already been charged to V_0. During the first phase, assume C_0 will charge C_1 to a voltage of V_1. Since charges before and after connecting C_0 and C_1 will be the same, we have

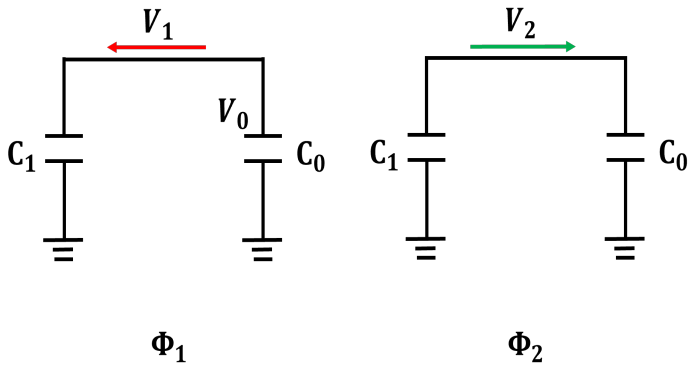


Figure 3.4: Theoretical calculations with only one storage capacitor.

$$Q_{initial} = Q_{final} \tag{3.1}$$

and

$$Q_{initial} = C_0 V_0 \tag{3.2}$$

$$Q_{final} = (C_1 + C_0)V_1 \tag{3.3}$$

After discharging the transducer, the second phase is to reconnect C_0 and C_1 for C_1 to charge C_0. Assume C_1 can charge C_2 to V_2 and $Q_{initial} = Q_{final}$,

$$C_1 V_1 = (C_1 + C_0)V_2 \tag{3.4}$$

As for high transfer efficiency, V_2 should be as large as possible.

$$V_2 = C_0 V_0 \frac{1}{C_1 + \frac{C_0^2}{C_1} + 2C_0} \tag{3.5}$$

When $C_1 = C_0$, V_2 has the maximum value of $V_2 = \frac{1}{4}V_0$ This result only applies for the first time of charging. As for the next period, the storage capacitor has initial charges that cannot be neglected.

3.2.2. Energy efficiency

Assume the initial charge inside C_1 is Q_s, the calculation steps are similar to the previous one shown in Fig. 3.4: Since $Q_{initial} = Q_{final}$, during phase 1,

$$Q_{initial1} = Q_s + C_0 V_0 \tag{3.6}$$

equals to

$$Q_{final1} = (C_1 + C_0)V_1 \tag{3.7}$$

As for phase 2:

$$Q_{initial2} = C_1 V_1 \tag{3.8}$$

equals to

$$Q_{final2} = (C_1 + C_0)V_2 \tag{3.9}$$

So, $Q_s = C_1 V_2$ and

$$V_2 = \frac{V_0}{2 + \frac{C_0}{C_1}} \tag{3.10}$$

If C_1 is as large as possible, V_2 can reach a maximum value.

According to Eq. (2.1), the energy stored inside the capacitor during the charging phase is $CV^2/2$. As for the conventional HV driver, the energy stored in the ultrasound transducer is

$$E_{S1} = \frac{1}{2} C_0 V_0^2 \tag{3.11}$$

After applying the charge redistribution method, the energy stored in the ultrasound transducer is

$$E_{S2} = \frac{1}{2} C_0 (V_0 - V_2)^2 + \frac{1}{2} C_0 V_2^2 \tag{3.12}$$

Consequently, the improved energy saving from the conventional charging method is

$$\Delta E_s = E_{S2} - E_{S1} = C_0 V_2^2 - C_0 V_0 V_2 \tag{3.13}$$

Eq. (3.13) is a parabolic function shown in Fig. 3.5 that has a minimum value when $V_2 = C_0 V_0/2$. Based on Eq. (3.10), as long as C_1 is larger than $C_0^2/2$, E_s will increase with the increase of V_2. According to the previous calculation, C_1 is positively correlated with V_2. Hence, for the purpose of storing more energy inside the ultrasound transducer, the capacitance of C_1 should be as large as possible.

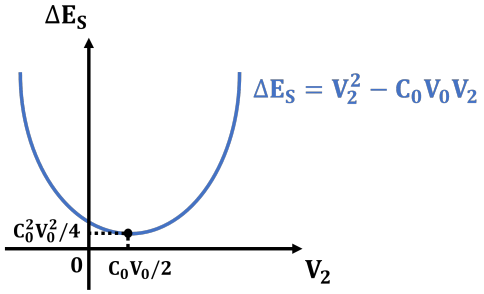


Figure 3.5: Saved energy ΔE_s versus V_2.

However, since this work aims to reach a 15 MHz frequency, which means the chip area should be within 50 μm × 50 μm, the capacitors should not be too big. Since the total capacitor area is expected to be less than half of the whole chip area, the overall value of capacitance should be less than 2.5 pF because one 2 fF capacitor occupies $1 \mu m^2$ of area. To optimize the circuit for better power efficiency and area savings, the storage capacitance can be chosen as 600 fF.

3.3. Transistor level circuit design

3.3.1. Stacked architecture

HV transistors reduce power efficiency because they not only occupy a large area, but also add a large parasitic capacitance to the output node. Therefore, this work utilizes a stack of 5 V CMOS transistors to implement a 10 V-driver. In this design, the dynamic gate biasing part is implemented by a voltage supply of 5 V that can make sure the voltage between each terminal of transistors in the stacks is within a safe margin without oxide or junction breaking down during low-to-high and high-to-low voltage transitions. Since the overshoot caused by the parasitic gate-drain capacitance during ON–OFF transitions was not critical because of the lower operating frequency and smaller sizing of transistors,

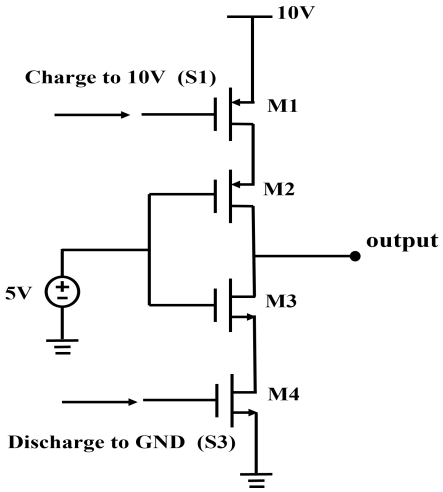


Figure 3.6: Schematic level circuit of the stacked architecture with V_{DDH}=10V.

some area-consuming capacitors and resistors have been removed by [23]. This work simplifies the idea of the self-biased method, using only stacked transistors instead of capacitors and resistors.

The stacked driving circuit is shown in Fig. 3.6. The principle of the driver circuit is as follows: Firstly, when there is a high-to-low signal applied to the gate of M_1, M_1 is turned on and the source terminal of M_2 is charged to 10 V. Since the gate terminal of M_2 is always 5 V, M_2 is also turned on so that the output (transducer part) will be charged to 10 V. Similarly, when the gate terminal of M_4 is applied by a low-to-high signal, M_4 is turned on so that the source of M_3 will be discharged to the ground. Due to the gate voltage of M_3 being always 5 V, M_3 is turned on while the output is discharging to the ground. In this way, the voltage between every two terminals of a transistor is within 5 V, which can make sure every 5 V standard CMOS transistor work in a safe region.

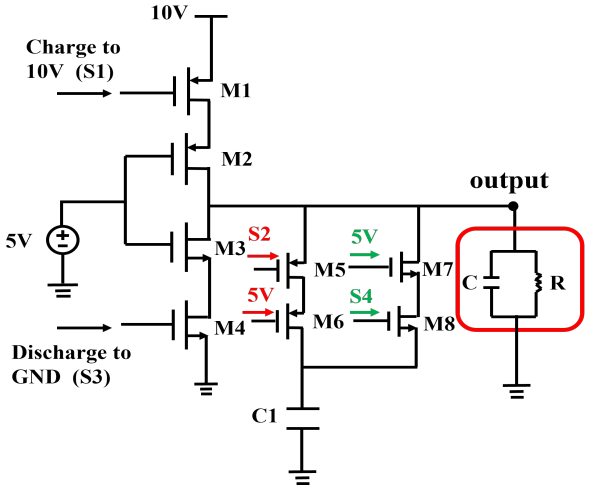


Figure 3.7: Schematic circuit of the proposed method with one parallel capacitor.

3.3.2. Charge redistribution design

The charge redistribution part also uses the stacked structure and is shown in Fig. 3.7. To make sure every 5 V-transistor works within 5 V, transistors M_6 and M_7 are driven by a DC voltage of 5 V. Switch S_2 first remains at 10 V before the transducer is charged to 10 V after the ultrasound transducer is charged to 10 V by the switch S_1, S_2 is turned to 5 V for the transducer charging the storage capacitor C_1. In this way, S_2 is set to be the inverter of S_1. Since the gate-driving voltage of M_6 is always 5 V, the transistor M_6 can be turned on as soon as its source is charged to a voltage higher than 5 V plus the threshold

voltage of M_6 so that C_1 can be charged by the transducer. After discharging the transducer through the switch S_3, S_4 changes from 0 V to 5 V for C_1 to charge the transducer. When S_4 is changed from low to high, M_8 is turned on. Since the driven voltage of the gate of M_7 is always 5 V and the source of M_7 is 0 V, M_7 will be turned on and C_1 can be connected with the ultrasound transducer.

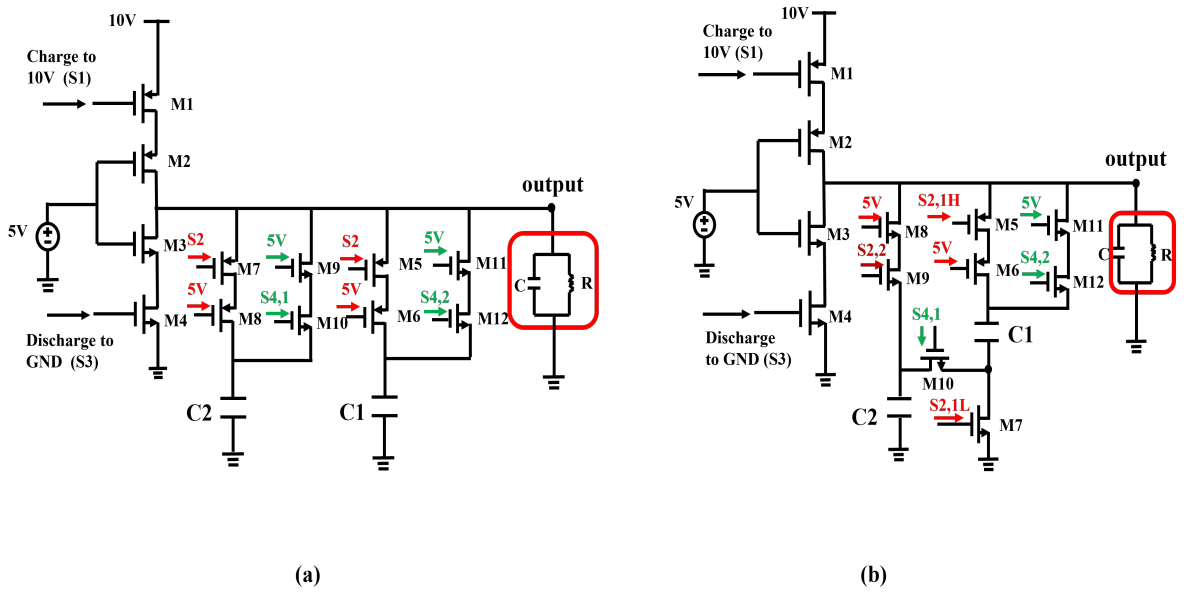


Figure 3.8: Schematic of the proposed circuits. (a) Charge redistribution method with two storage capacitors in parallel when charging back to the transducer. (b) Charge redistribution method with two storage capacitors in series when charging back to the transducer.

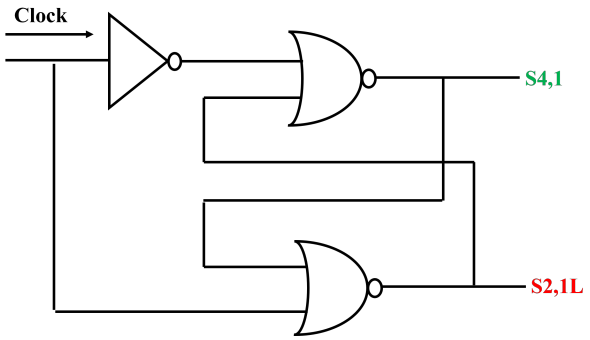


Figure 3.9: Non-overlapping circuit

In order to improve the power efficiency based on the stacked charge redistribution technique, more storage capacitors are introduced to the circuit. However, considering the complexity of the circuit and the occupied area, the work only adds two storage capacitors into the circuit. There are two ways of saving charges shown in Fig. 3.8. Fig. 3.8(a) shows two storage capacitors are first charged by the ultrasound transducer and then charge back to the transducer successively. Take Fig. 3.8 (b) as an example, the working principle is as followed: transistors M_5 and M_6 work as switch $S_{2,1H}$ for the ultrasound transducer to charge capacitor C_1. Similarly, M_8 and M_9 are a combination of switch $S_{2,2}$ that can connect PZT and capacitor C_2; transistors M_{11} and M_{12} represent switch $S_{4,2}$ to connect the top plate of C_1 for charging back into the ultrasound transducer. The three pairs of transistors all include self-body biasing technology to prevent current flow inside the transistors. The stacked principle is also applied here: take switch $S_{2,2}$ as an example, the gate of transistor M_8 is constantly biased at 5 V and only the gate terminal of M_9 has the signal controlled by clock $S_{2,2}$. When the output node is 10 V, the source node of M_8 will be charged to 5 V until M_8 is turned off automatically. Only when there is a high logic signal at the gate of M_9, can C_2 be charged by the ultrasound transducer. Since only when

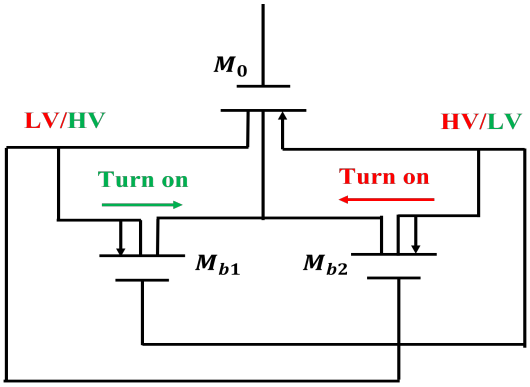


Figure 3.10: Principle of body biasing part [26].

switch $S_{2,1L}$ turns off, can switch $S_{4,1}$ can be turned on. A non-overlapping circuit is used to create a non-overlapping time of 660 ps, which is shown in Fig. 3.9.

Since the gate of M_6 is always biasing at 5V, it limits C_1 from being charged to a voltage higher than 5V. Nevertheless, C_1 can be charged to 6.67V theoretically. Although this design can achieve a higher power efficiency if the gate-biasing voltage of M_6 can be set to a higher value, it will increase the complexity of the circuit for adding another DC-DC converter. So overall, a 5V-gate-biasing-voltage for M_6 is still the optimum option.

3.3.3. Body biasing

During the process of implementing the principle shown in Fig. 3.7, there is a problem with charging the storage capacitor C_1 correctly. The voltage of C_1 should stay at 0 V before S_2 is switched from 10 V to 5 V. However, C_1 is always charged with the transducer from the beginning of each clock cycle, which is caused by reverse-bias source/drain junction leakages. Although the p-n junctions between the source/drain and the substrate are reverse-biased, a small amount of current flows causes these junctions to leak. Therefore, a leakage current in the substrate leads to invalid control of switch S_2.

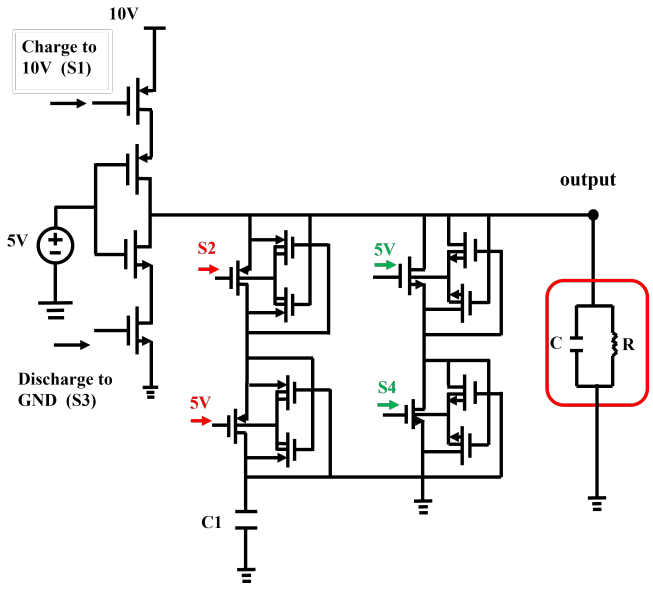


Figure 3.11: Schematic level circuit of the charge redistribution method with one parallel capacitor.

Fig. 3.10 shows a method of self-body biasing technology to prevent current flow inside the transistors when not needed [26]. Assume the left side of M_0 has low voltage (LV) while its right side contains high voltage (HV). Since the gate of M_{b1} has high voltage while the gate of M_{b2} is driven by LV, M_{b1} turns off and M_{b2} turns on. Therefore, the HV will flow from the source of M_{b2} to its drain, and

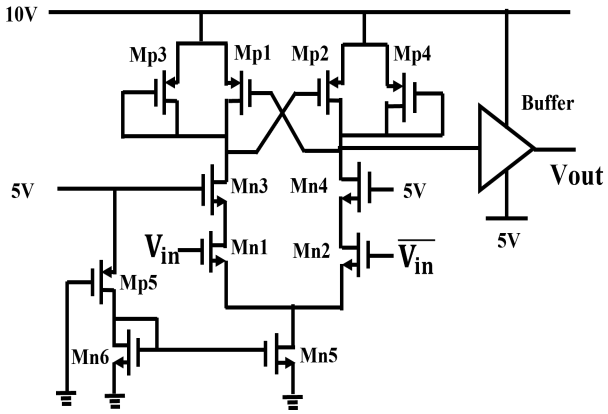


Figure 3.12: Conventional level shifter with stacked architecture adapted from [13].

only the source and body of M_0 will be connected. In this way, the drain of M_0 is disconnected from the substrate through the block of M_{b1} so that C_1 can be charged correctly.

After adding the body biasing part, the final schematic of the stacked charge redistribution method with one parallel capacitor is shown in Fig. 3.11.

3.3.4. Level shifter

Fig. 3.12 shows the conventional level shifter with stacked architecture [13]. Based on the principle of stacked structure, stacked transistors M_{n1}, M_{n2}, M_{n3}, and M_{n4} are used to bear a 10 V voltage drop without oxide or junction breakdown for each transistor. By sizing M_{p3} and M_{p4} transistors, a voltage drop of 5 V ($V_{DSMp3,4} = 5V$) can be created to protect transistors M_{p1} and M_{p2}. The gate of M_{n1} is driven by a 0-5 V pulse signal and the gate of M_{n2} is driven by the inverse of the pulse signal. When the signal is at a high voltage level, M_{n1} is turned on so that the source node of M_{n3} is discharged and Mn3 is also turned on because the gate of M_{n3} is always biased at 5 V. As the drain of M_{n3} becomes discharged, this turns on M_{p2} so that the output node can be charged to 10 V. By the sizing of the $M_{P1,4}$ transistors, the voltage at the input node of a tapered buffer can provide transitions between V_{HV} and $V_{HV} - VDS_{MP1,4}$. This tapered buffer is added to adjust the output signal to swing between 5 V and 10 V properly.

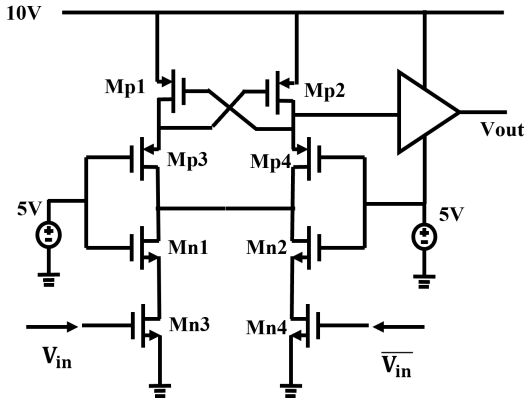


Figure 3.13: Schematic level circuit of power efficient level shifter.

However, this type of level shifter consumes large power because of the tail current. This design changed the topology of the level shifter and only uses the stacked architecture shown in Fig. 3.13. In this level shifter, transistors M_{p3}, M_{p4}, M_{n1}, and M_{n2} are biased at 5 V to keep every transistor working at a safe voltage level within 5 V. At the same time, the power consumption can be limited to a small level of around 60 μW.

4

Simulation Results

4.1. One parallel capacitor

The proposed driver has been designed in TSMC 0.18 μm technology. The transient simulation results of pulser with one parallel capacitor, Fig. 4.3 (a), is shown in Fig. 4.1. The frequency of each clock signal is 15MHz. When the charging signal shows a high-to-low transition, the ultrasound transducer is charged to 10 V. After the charging signal turns from low to high and finishes charging, signal S_2, which is controlled by the charging signal (S_1) passing through an inverter, changes from 10 V to 5 V to connect the transducer with the storage capacitor. There is no need to set this second charging time since transistors M_5 and M_6 are turned off when the output voltage is lower than $5V + |V_thp|$. Then, there is a short period of low-to-high transition in S_4 after discharging the ultrasound transducer. Since the time constant of charging back to the ultrasound transducer is around 1.2 n, the charging and discharging time is very short. Therefore, the last charging period should be as small as possible to prevent charge loss. However, in practice, the rising time and falling time of each control signal are around 1 ns, which will lead to inevitable power loss. With this short transition, the output can be charged to around 1.78 V before the next charging cycle comes.

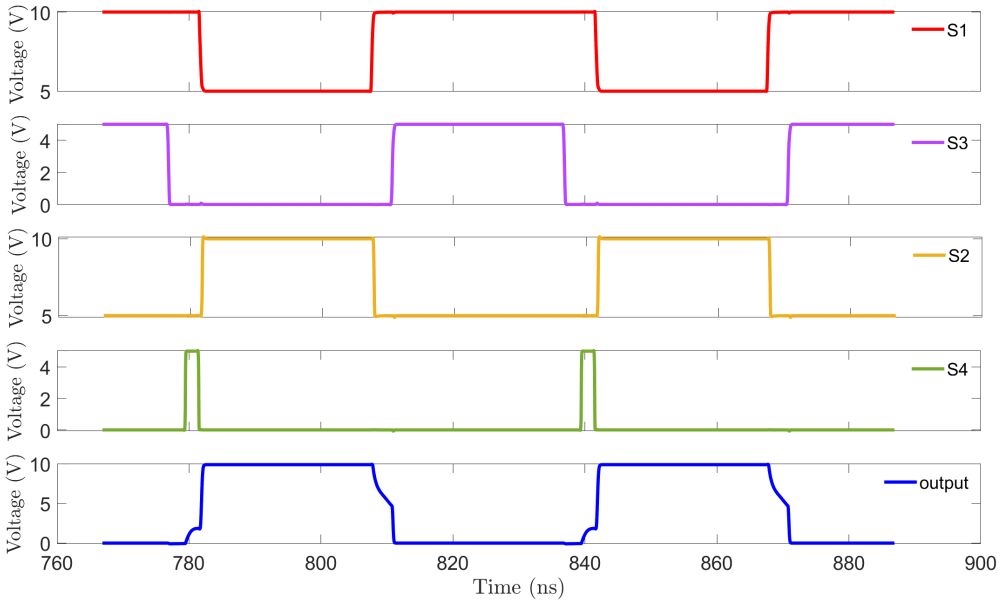
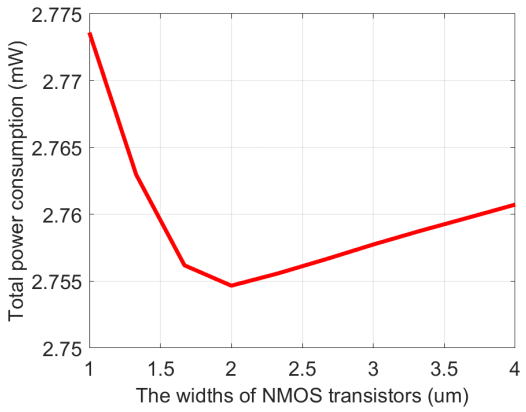
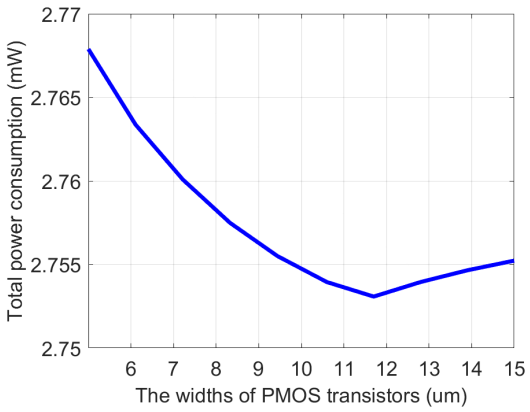


Figure 4.1: Timing diagram of input clocks and transient waveform of output.

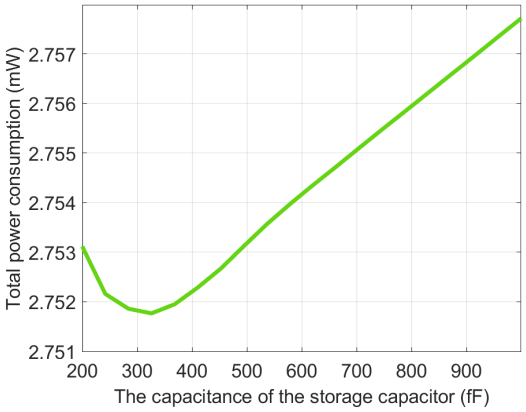
In reality, the parasitic capacitance associated with the interconnect lines and the gate capacitance of transistors at the output driver stage are around one order of magnitude greater than the transducer



(a) Total power consumption versus the widths of M_7 and M_8.



(b) Total power consumption versus the widths of M_5 and M_6.



(c) Total power consumption versus the capacitance of the storage capacitor.

Figure 4.2: Total power consumption versus the widths of Wn, Wp, and the storage capacitor.

capacitance. These large capacitors can significantly reduce the amplitude of the output signal and the sensitivity of the transducer. Therefore, in order to better excite the transducer, optimizing the size of transistors at the driver part can generate pulses that have sharp rise and fall times [11]. The widths of transistors in the driver part are 40 μm for PMOS and 20 μm for NMOS so that the rising time is 564 ps and the falling time is 479 ps. The widths of transistors that are used for body biasing is 1 μm.

In order to find the most power-efficient circuit, the widths of transistors of the charge redistribution part have been swept in Cadence. Fig. 4.2 (a) shows the total power consumption as a function of the widths of M_7 and M_8. When the widths are around 2 μm, the circuit has the lowest power consumption. Similarly, the widths of M_5 and M_6 in Fig. 4.3 (a) are swept as shown in Fig. 4.2 (b). When the width is 11.5 μm, the circuit has the best power efficiency. The most important part is to decide the capacitance of C_1. As shown in chapter 3, the storage capacitor should be as large as possible. However, during the simulation part, the lowest power consumption of 2.752 mW shows when $C_1 = 326pF$ as shown in Fig.

Table 4.1: Design choices for the size of transistors and capacitance of the charge redistribution part.

	NMOS transistors	PMOS transistors	The storage capacitor
Fig. 4.3 (a)	M_7 and M_8	M_5 and M_6	C_1
	2 μm	11.5 μm	326 pF
Fig. 4.3(b)	M_9, M_{10}, M_{11} and M_{12}	M_5, M_6,M_7 and M_8	C_1 and C_2
	2 μm	9 μm	both 325 pF
Fig. 4.3(c)	M_8, M_9, M_{10}, M_{11} and M_{12}	M_5, M_6	C_1 and C_2
	2 μm	16 μm	400 pF and 200 pF

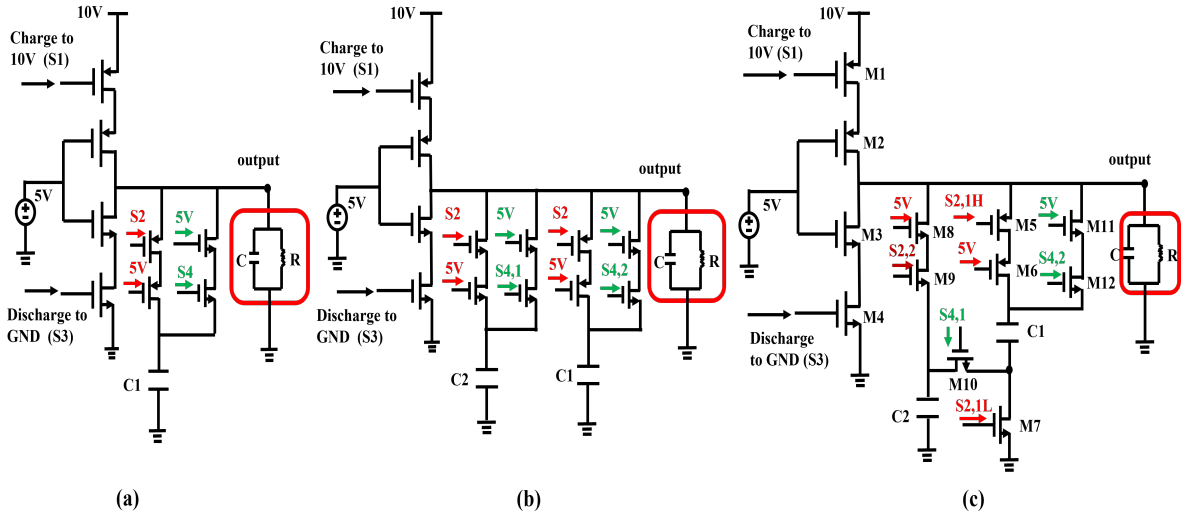


Figure 4.3: Schematic of the proposed circuits. (a) Charge redistribution method with one storage capacitor. (b) Charge redistribution method with two storage capacitors in parallel when charging back to the transducer. (c) Charge redistribution method with two storage capacitors in series when charging back to the transducer.

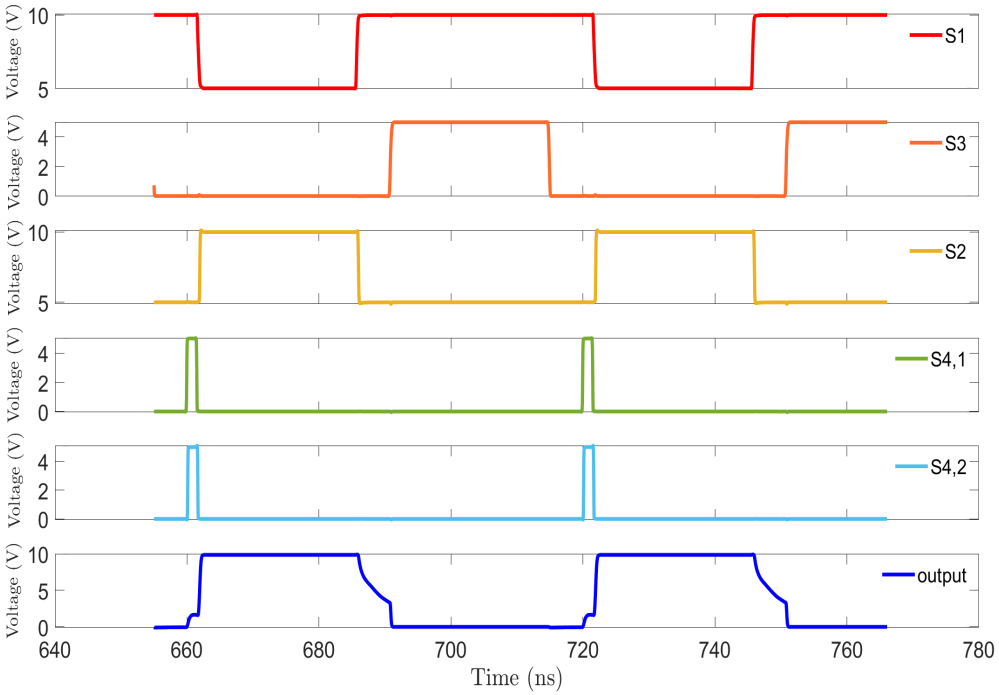
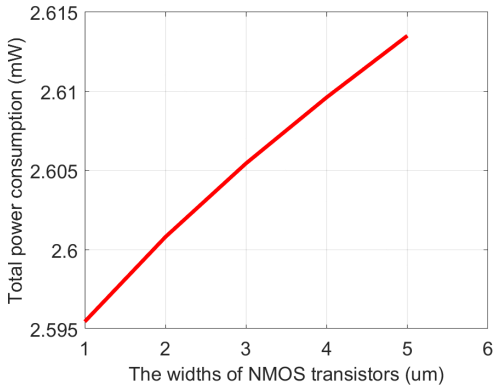


Figure 4.4: Timing diagram of input clocks and transient waveform of output when $S_{4,1}$ and $S_{4,2}$ are closed together.

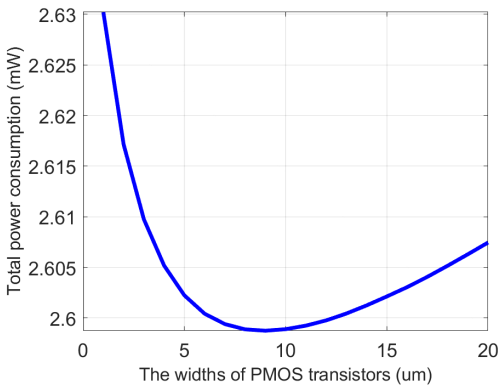
4.2 (c). The overall design choices for the charge redistribution part are shown in Table 4.1.

4.2. Two parallel capacitors

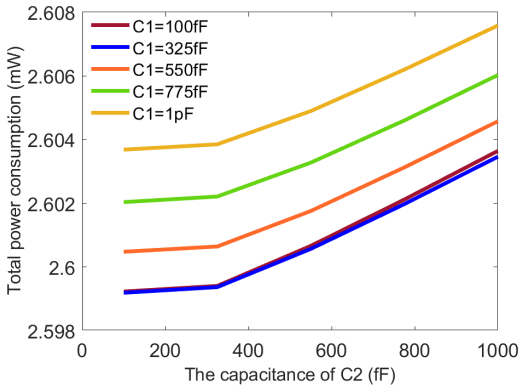
Fig. 4.4 illustrates the input timing diagram and transient output waveform of the pulser. The working principle is similar to the circuit of one storage capacitor. Firstly, use S_1 to generate a high-to-low signal to charge the ultrasound transducer to 10 V. Then, S_2 turns from 10 V to 5 V to charge C_1 and C_2 together. Since $|V_{thp}| = 0.76V$ in the simulation, when C_1 and C_2 are charged to 5.76 V, switch S_2 will be turned off automatically. Next, the rest charges inside the ultrasound transducer are discharged by turning on



(a) Total power consumption versus the widths of M_9, M_{10}, M_{11} and M_{12}.



(b) Total power consumption versus the widths of M_5, M_6, M_7 and M_8.



(c) Total power consumption versus the capacitance of the two storage capacitors.

Figure 4.5: Total power consumption versus the widths of Wn, Wp, and C.

switch S_3. There are two ways to charge back the ultrasound transducer during the final step: Fig. 4.3 shows the output is charged by C_1 and C_2 together while another way is to charge the output step by step. The difference is the closing time of $S_{4,1}$ and $S_{4,2}$. The comparison result shows charging together has the best power efficiency since the output can be charged to a higher value of 2.021 V compared to 1.771 V. When $S_{4,1}$ and $S_{4,2}$ are closed together, the power consumption is 2.596 mW while it takes 2.606 mW when $S_{4,1}$ and $S_{4,2}$ are turned on step by step. Therefore, the charging time from storage capacitors to the ultrasound transducer should be as short as possible to reduce leakage. As shown in Fig. 4.5 (a) and (b), the widths of NMOS and PMOS are chosen as 2 μm and 9 μm, respectively, so that the circuit has a lower power consumption. When sweeping both C_1 and C_2, Fig. 4.5 (c) shows that when the two capacitors have the same capacitance of around 325 fF, the power consumption is the lowest. The final settings for the charge redistribution part are shown in Table 4.1.

4.3. Two series capacitors

The transient simulation results of pulser with one parallel capacitor, Fig. 4.3 (c), is shown in Fig. 4.6. When charging signal S_1 by a high-to-low signal from 10 V to 5 V, the ultrasound transducer is charged to 10 V so that the output voltage will be charged from 0 V to 10 V. Signal S_{2H} is set to be the inverse of charge signal S_1 for driving the gate of transistors M_5 and M_8. Theoretically, M_8 and M_9 can be implemented as both NMOS and PMOS. If using NMOS transistors for M_8 and M_9, another control signal needs to be introduced to turn on the gate of M_9 while the gate of M_8 is controlled by a DC signal of 5 V. This structure has a better power consumption of 2.73 mW compared to using PMOS transistors to implement M_8 and M_9, which consumes 2.78 mW. If M_8 and M_9 are implemented by PMOS transistors, the top plate of C_2 can only be charged to 2.6 V since M_8 and M_9 can be turned off automatically when $V_{SG} < |V_{thp}|$. Therefore, a part of the charges in the ultrasound transducer will

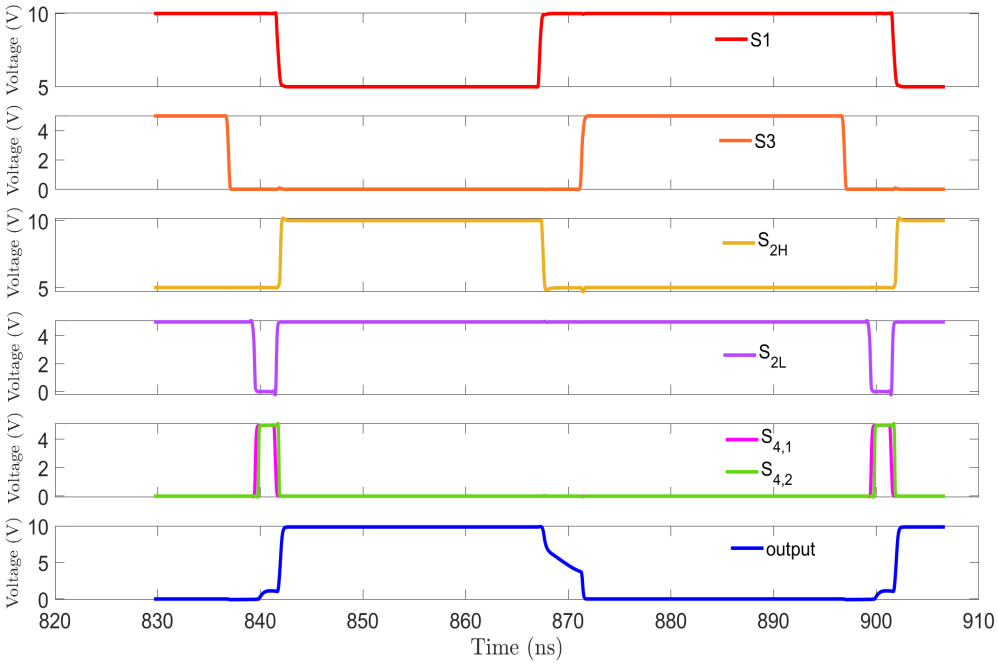
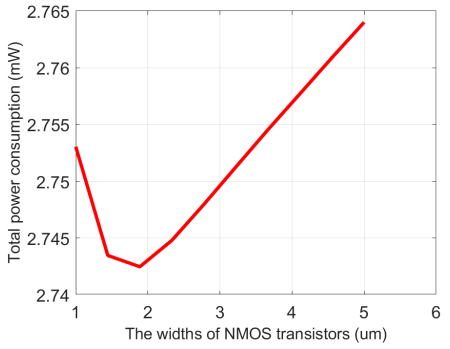
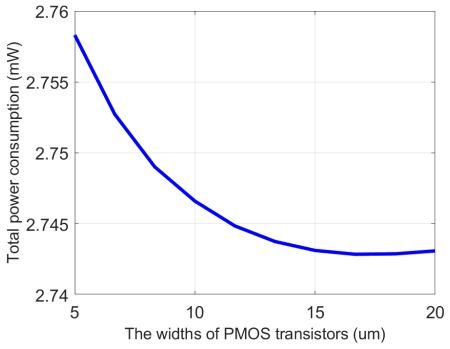


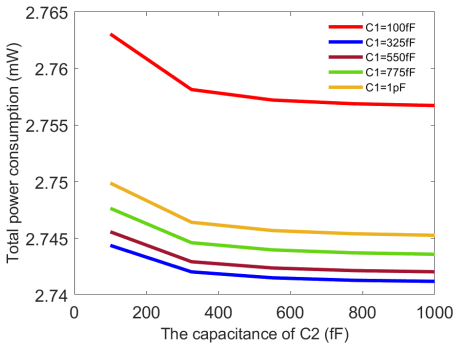
Figure 4.6: Timing diagram of input clocks and transient waveform of output.



(a) Total power consumption versus the widths of M_8, M_9, M_{10}, M_{11} and M_{12}.



(b) Total power consumption versus the widths of M_5 and M_6.



(c) Total power consumption versus the capacitance of the two storage capacitors.

Figure 4.7: Total power consumption versus the widths of Wn, Wp, and C.

be wasted which leads to higher power consumption for the whole circuit. When C_1 and C_2 finish charging, switch S_3 is closed to discharge the output node to the ground. There is a non-overlapping block used to guarantee S_3 will experience a low-to-high signal after switch S_{2L} is disconnected. Before the next clock cycle comes, $S_{4,1}$ and $S_{4,2}$ are closed to make C_1 and C_2 be connected in series and then charge back into the output node. The output voltage will be discharged in two steps before discharging to the ground and be charged back to 1.09 V before the next clock cycle arrives.

If M_8 and M_9 are PMOS transistors, the advantage compared to the topology shown in Fig. 4.3(c) is that the area is saved. This structure can save 6 deep-n-well transistors while consuming more power compared to the circuit that has two parallel storage capacitors. However, this topology should be discarded because it only improves 0.02 mW while using two storage capacitors and one more deep-n-well transistor compared to the circuit that only has one storage capacitor.

Similarly, Fig. 4.7 is the best case for the parameters set in the circuit. When the width of each PMOS and NMOS are 16 μm and 2μm, respectively, the circuit has a better power efficiency. Although the power consumption is smallest when $C_1 = C_2 = 600fF$, this circuit chooses $C_1 = 400fF$ and $C_2 = 200fF$ for the trade-off between area and power consumption. Overall, the total power consumption is 2.73 mW.

5

Layout

In the design of the standard CMOS, the substrate of each NMOS needs to be connected with the ground, however, in this circuit design, stacked architecture is implemented so that the body of NMOS transistors which are in the middle level of the stacked structure needs to be attached to a higher voltage level. Therefore, deep-n-well transistors are needed in this design. Since this proposed high-efficient driver has been designed in TSMC 0.18 μm technology, deep-n-well transistors are realized by NBL isolation shown in Fig. 5.1.

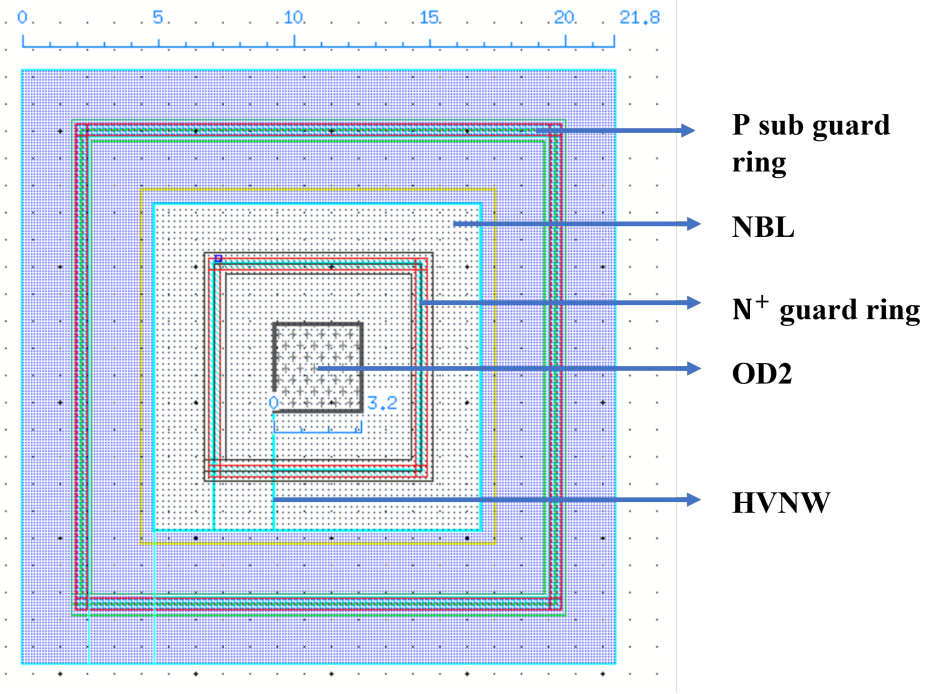


Figure 5.1: The components of NBL isolation structure.

In Cadence, this model is called iso-ring with type $hvnwnbl29_od2_f$. At the center of this model, an OD2 layer defines this model as an NMOS device since OD means diffusion layer in layout and this OD layer is inside P substrate. OD layer constrains the area that can put NMOS devices and its minimum area is $3.2\mu m \times 3.2\mu m$. Outside OD2 layer, there is an N^+ guard ring that connects to the high voltage as well as the HVNW (high-voltage drift n-well layer). Inside this iso-ring, every HVNW inside the NBL (n^+ buried layer) must have the same voltage as the NBL polarization [27]. In this case, the NBL is connected to 10 V. Besides iso-ring for deep-n-well transistors, the other standard PMOS and NMOS transistors are also surrounded by guard rings to protect devices from external disturbance. The overall layout of the circuit with one storage capacitor is shown in Fig. 5.2. In this layout, every NMOS

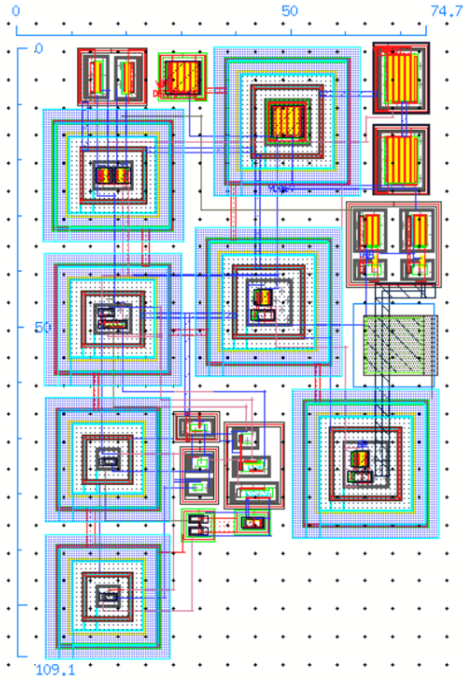


Figure 5.2: The final layout view of the circuit with one storage capacitor.

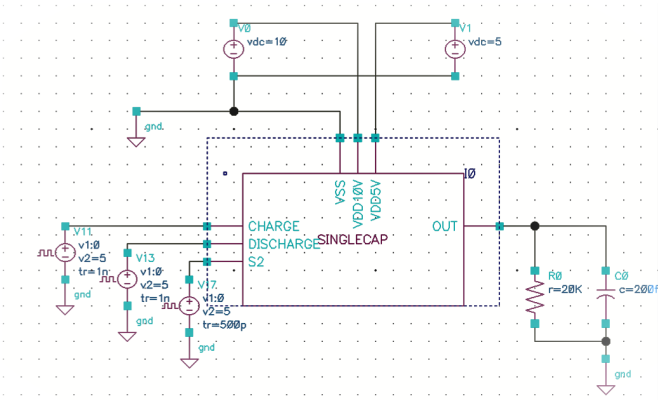


Figure 5.3: The Test bench for post-layout simulation results.

transistor whose source shares the same voltage level shares one NBL and the capacitance of the storage capacitor is 200 fF. The total area of this design is $74.7\mu m \times 109.1\mu m$. For future reference, one way to save more area is to have multiple p^+ guard rings inside the same NBL by separating them with HVNW. This layout has passed DRC check and LVS check. Fig. 5.3 shows the schematic after running PEX. Fig. 5.4 and Fig. 5.5 present the transient simulation results of pre-layout and post-layout simulation, respectively. Since the rising and falling propagation delay of the control signals in the post-layout simulation are larger than those in the pre-layout simulation, the power consumption in the post-layout simulation is higher (2.91 mW) compared to the pre-layout simulation (2.78 mW) due to the fast power loss caused by the resistor inside the ultrasound transducer.

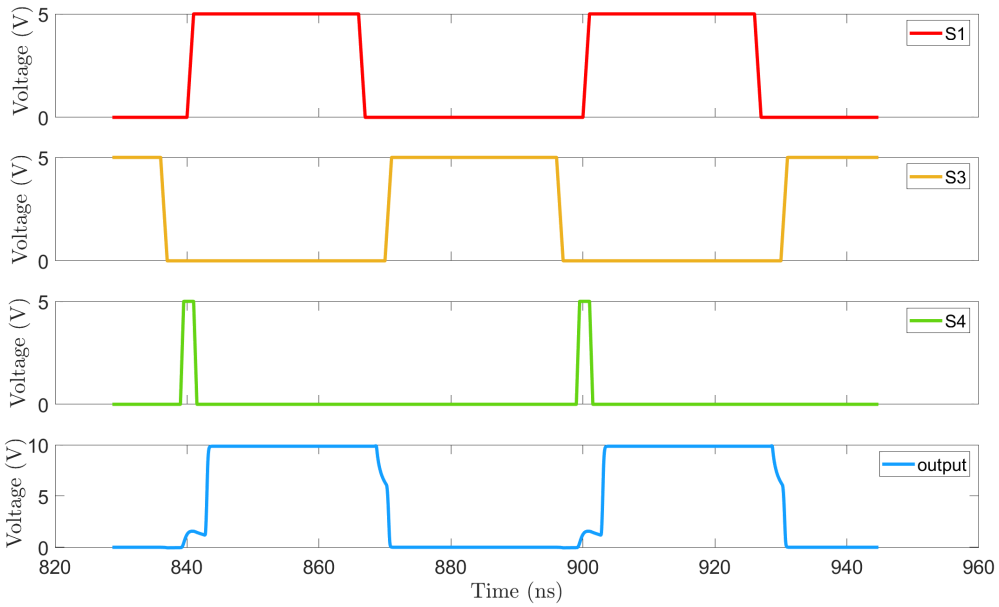


Figure 5.4: Timing diagram of input clocks and transient waveform of output during pre-layout simulation.

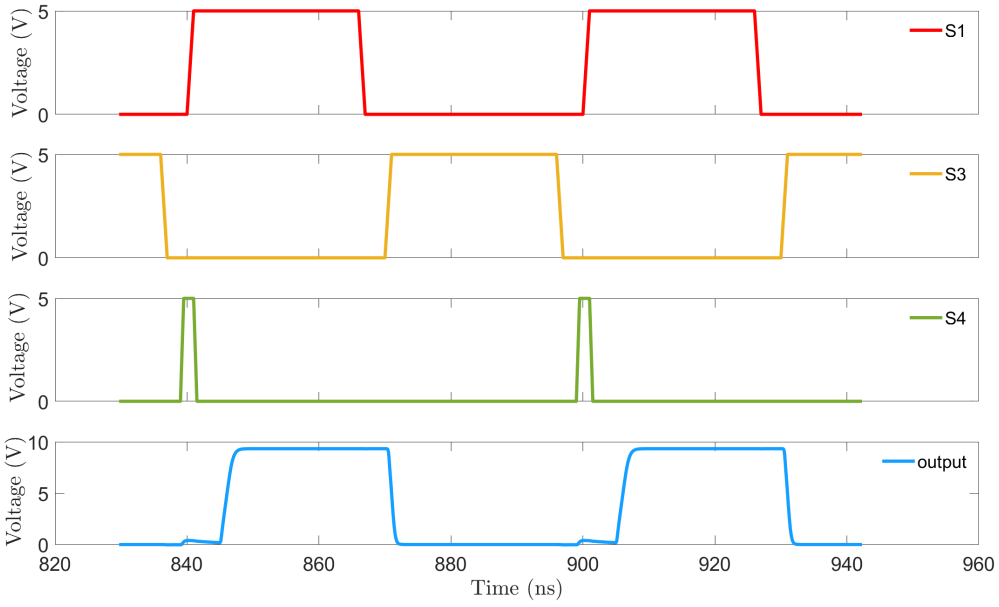


Figure 5.5: Timing diagram of input clocks and transient waveform of output during post-layout simulation.

6 Discussion

6.1. Difference between theoretical result and simulation result

According to the theoretical calculations, when there is only one storage capacitor in the circuit, this storage capacitor should be as large as possible to save more energy. However, the simulation result shows this storage capacitor (326 fF) should be only a little bit higher than the capacitance of the ultrasound transducer (200 fF). The reason behind this is we only considered the charges we saved through transition while ignoring the charging loss of the capacitors. Take the circuit of one storage capacitor as an example, the storage capacitor will be charged to V_1 in the first charging phase. The energy loss in this charging phase is:

$$E_1 = \frac{1}{2}C_1V_1^2 \tag{6.1}$$

Based on the calculation of chapter 3,

$$V_1 = V_0\frac{C_1 + C_0}{2C_1 + C_0} \tag{6.2}$$

and

$$V_2 = V_0\frac{C_1V_0}{2C_1 + C_0} \tag{6.3}$$

When this storage capacitor is connected with the output to charge the ultrasound transducer, the voltage of C_1 is V_2. The energy loss for discharging C_1 is:

$$E_2 = \frac{1}{2}C_1(V_1 - V_2)^2 = \frac{1}{2} \times \frac{C_0^2V_0^2}{4C_1 + \frac{C_0^2}{C_1} + 4C_0} \tag{6.4}$$

Both E_1 and E_2 have a minimum value only when C_1 is as small as possible. As for C_0, the charging loss from V_2 to $V_{DDH} = 10V$ is:

$$E_3 = \frac{1}{2}C_0(V_{DDH} - V_2)^2 \tag{6.5}$$

When V_2 is as large as possible, the energy consumption will be small, which is consistent with the calculation result in chapter 3. So overall, the choice of storage capacitance should not be as large as possible. Instead, considering the severe charging loss caused by large capacitors, the storage capacitor should be slightly larger than the capacitor inside the ultrasound transducer.

6.2. Optimum topology and performance comparison

Since this work aims to reach a 15 MHz frequency, which means the chip area should be within $50\mu m \times 50\mu m$, the capacitors should not be too big. Since the total capacitor area is expected to be less than half of the whole chip area, the overall value of capacitance should be less than 2.5 pF because one 2 fF capacitor occupies $1\mu m^2$ of area. To optimize the circuit for better power efficiency and area savings, each size of the transistor and the value of C_1 and C_2 are swept in Cadence. The overall simulation

Table 6.1: The comparison of power consumption between each design

	Power consumption	Increased efficiency compared with HV driver	Increased efficiency compared with Stacked driver
HV driver	4.19mW		
Stacked driver	3.91mW	6.68%	
Method 1: one parallel capacitor	2.75mW	34.37%	29.67%
Method 2: two parallel capacitors	2.60mW	37.95%	33.50%
Method 3: two capacitors first parallel then series	2.73mW	34.84%	30.18%
Post-layout simulation for Method 1	2.91mW	30.55%	25.58%

Table 6.2: The performance comparison of this work and the state of art design

	[6]	**[28]**	**[29]**	**This work**
Application	**Neuro-modulation**	**Neuro-modulation**	**Machine vision**	**Neuro-modulation**
CMOS process	**0.18μm LV**	**0.18μm HV**	**0.18μm HV**	**0.18μm LV**
Transducer	**PZT**	**CMUT**	**PMUT**	**PZT**
Operation frequency	**8.4MHz**	**2MHz**	**0.19MHz**	**15MHz**
Driving voltage	**5V**	**60V**	**10V**	**10V**
Power consumption	**1.5mW**	**18.75mW** [a]	**4.3mW**	**2.60mW**

[a] The power was calculated based on the duty cycle shown in [28].

results of the three proposed methods and the improvements in power consumption are shown in TABLE 6.1. The second method shown in Fig. 3.8(a) has the best power efficiency of 2.60 mW and can save 37.95% compared with the HV driver. However, there is a trade-off between area and power consumption. Since deep n-well transistors are used in the stacked architecture, minimizing the number of deep n-well transistors can save the total occupied area. From Table 6.1, although the third method shown in Fig. 3.8(b) scarifies 3.11% energy efficiency compared with the second method, it decreases 5 deep n-well transistors to save more area. Compared to the occupied area and the improvement of power efficiency, method one shown in Fig. 3.7 is the best solution because it only contains one storage capacitor which can save a large number of switches and can achieve 34.37% of energy saving compared to HV drivers. However, the power consumption from the post-layout simulation is higher due to the rising and falling propagation delay of the control signals in the post-layout simulation are larger than pre-layout simulation.

The comparison of this work and the other published design is shown in Table 6.2. Although work [28] achieves a high driving voltage, it uses HV transistors which consume large power. Also, this work has the highest aiming frequency and a higher driving voltage compared with work [6] with relatively low power consumption.

7

Conclusion

This work presents a design of a fully integrated energy-efficient HV pulser with TSMC 0.18-μm technology for ultrasound medical applications. For the purpose of reducing the occupied area and energy loss during the transition between charging and discharging the ultrasound transducer, this thesis analyzed the advantages and disadvantages of current techniques and proposed a method that contains stacked architecture and charge-redistribution technique.

7.1. Thesis contribution

This work aims to improve the power efficiency of an ultrasound driver by implementing a charge redistribution method that is suitable for all US transducer types. Furthermore, by utilizing a stack of low voltage transistors, both the driver area and the capacitance at the output node are decreased. Three different circuits are presented and discussed. One is introducing a capacitor for storing part of the wasted charges during the discharging phase. The other two circuits attempt to improve on the previous design by adding two storage capacitors in the circuit. However, simulation results showed that the performance the worse than only using one storage capacitor. Since increasing the number of storage capacitors also increases the complexity of the whole circuit, the power efficiency is not remarkable, instead, the occupied area has been increased.

During this thesis project, blocks like lever shifters, non-overlapping circuits, the body biasing method, and gate drivers are used to solve specific problems like designing DC-DC converters, timing issues, and reverse-bias junction leakages. Also, different techniques for energy saving are analyzed thoroughly. Also, this work absorbs the idea of charge redistribution method, multi-level pulse shaping technique, and energy replenishment. Learning from these methods inspires the whole design.

This proposed method aims to enable a 15 MHz ultrasound phased-array system that can drive PZT ultrasound transducers at $10V_{pp}$ with 5 V standard CMOS transistors. Overall, the proposed circuit can save 30.55% of energy compared to the conventional HV driver while avoiding the use of HV transistors in high-frequency phased array designs.

7.2. Further improvements of power efficiency for future work

- Since PZT comprises a small capacitance of 200 fF and a resistor of 20 kΩ, this parallel resistance plays a significant role in power dissipation. The charging time needs to be very short to prevent charge loss from the resistor because the time constant in the circuit of charging back to the ultrasound transducer is around 1.2 n. From the post-layout simulation results, the rising and falling propagation delay of the control signals can affect the circuit performance significantly. Therefore, finding a way to improve the charging time or reduce the propagation delay can help to save more charges.
- Also, the stacked structure constrains the voltage level of the storage capacitor. Since the gate of the second PMOS transistor (M_6 in Fig. 3.7) is always biasing at 5 V, it limits C_1 from being charged to a voltage higher than 5.76 V (the threshold voltage of the PMOS transistor is -0.76V). Nevertheless, C_1 can be charged to 6.67V theoretically. This design can achieve a higher power

efficiency if the gate-biasing voltage of M_6 can be set to a higher value if adding another DC-DC converter will not increase too much complexity of the circuit.

- As for the layout aspect, the total area can be reduced by sharing NBL with transistors containing different source voltages. This work only combines every NMOS transistor whose source shares the same voltage level in one NBL. If NBL can be separated properly by HV layers, the circuit can achieve a smaller area.
- In the aspect of circuit design, this work presents three ways to save wasted charges. Although the method with only one storage capacitor shows better performance, for the circuit with two storage capacitors, different connections between storage capacitors and the ultrasound transducer require further consideration. For example, the charging efficiency may be higher when the two storage capacitors are first charged in series and then discharge in parallel with the ultrasound transducer. Nonetheless, this topology might require more deep n-well transistors.
- Multi-level pulse shaping technique illustrated previously shows appealing results. By charging and discharging the ultrasound transducer step by step, part of the charges can be saved. This idea is similar to charge redistribution method, however, it might be difficult to implement with LV transistors. In the future, if multi-level pulse shaping technique can be realized without HV transistors, this method may achieve further improvement in power efficiency.

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