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Demodulation Techniques for Self-Oscillating Eddy-Current Displacement Sensor Interfaces: A Review

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***Abstract*— This paper presents a comprehensive study of demodulation techniques for high-frequency self-oscillating eddy-current displacement sensor (ECDS) interfaces. Increasing the excitation frequency is essential for lowering the skin depth in many demanding industrial applications, that require better resolution. However, a high excitation frequency poses design challenges in the readout electronics, and particularly in the demodulation functional block. We analyze noise, linearity, and stability design considerations in amplitude demodulators for nanometer and sub-nanometer ECDSs. A number of state-of-the-art amplitude demodulation techniques employed in high-frequency ECDSs are reviewed, and their pros and cons are evaluated.**

***Index Terms*— Displacement, eddy-current, ECS, mixer, oscillator, position, sensor, demodulation, inductance.**

I. Introduction

PRECISE displacement sensing is an essential requirement in various industries as hi-tech industry, metrology, nano-mechatronics and space-equipment manufacturing. Displacement sensors can also be used for measuring other physical quantities, which can first be converted into movement, such as pressure, acceleration, vibration etc.[1]–[5] Eddy-current displacement sensors (ECDSs) are compact, robust, stable, accurate and relatively low-cost. An advantage of ECDSs is that the sensing coil is a reactive component which ideally does not dissipate energy and is hence noiseless, which is similar to capacitive sensors. However, unlike capacitive sensors, ECDSs do not require electrical contact with the target. Another important advantage of ECDSs is their immunity to environmental conditions. They are not sensitive to the presence of non-conductive contaminants such as oil, dirt, dust etc. However ECDSs are sensitive to stray magnetic fields and the mechanical instability of the sensor coil. It is important to mention that displacement measurement with ECDSs is limited to metallic/conductive targets, or non-metallic targets covered with a metallic film [6], [7].

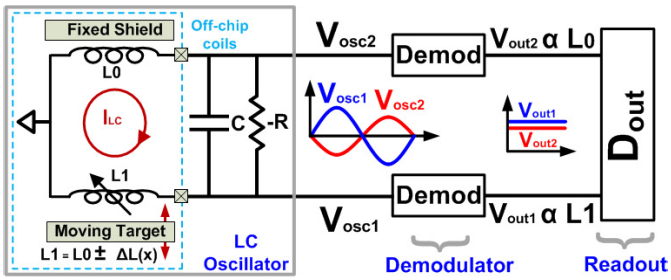

Fig. 1. Block diagram of a single-ended self-oscillating eddy-current displacement sensor interface. The active part of the oscillator is not shown.

The working principle of eddy current sensors is based on magnetic induction. The presence of a time-varying primary magnetic field near a conductive target induces eddy currents in the target due to the Lorentz force. These currents in turn generate a secondary magnetic field, as per Lenz's law, to oppose the initial magnetic field. As a result, the equivalent inductance of the coil is influenced by the target. Since the intensity of eddy currents depends on the coil-target distance, this phenomenon is exploited when measuring the absolute distance or the proximity to a metallic target [8]–[11].

Skin depth is a very important limitation of an ECDS. The skin depth is given by $\delta = 1/\sqrt{\pi \mu \sigma f_{exc}}$, where f_{exc} is the excitation frequency, μ is the magnetic permeability of the conductor, and σ is the electrical conductivity. At a high excitation frequency ($>$ 10 MHz), the distance $X_{cx,hf}$ sensed by an ECDS can be approximated by [8] and [11],

$$X_{cx,hf} \cong X + \frac{\delta}{\sqrt{2}} \tag{1}$$

where X is the actual distance between the sensor and the target. Equation 1 characterizes the behaviour of an ECDS. The skin depth acts as an offset to the ECDS system and must be minimized to relax the dynamic range of the interface. Moreover, cross-sensitivity to the skin depth δ, e.g. due to a change in the target conductivity with temperature, limits the applicability of ECDSs in high precision position/displacement measurements. For example, an 1 °C change of the temperature of a copper target will change its conductivity σ and correspondingly the skin depth δ, leading to an apparent displacement error of $\approx$ 32 nm, at 10 MHz excitation frequency. Similar errors in the displacement can be induced by any

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drift in the excitation frequency. The detrimental effect of the skin depth on the displacement measurement can be lowered below the error budget by employing a high enough excitation frequency (small δ). This can make ECDSs more desirable in advanced industrial applications [12], [13].

Figure 1 illustrates the conceptual block diagram of a self-oscillating ECDS interface. The front-end consists of an LC-oscillator with two coils, the sensing coil L_1 and a reference coil L_0. The reference coil nominally has inductance equal to that of the sensing coil at the stand-off distance x_{so} to the target. This is achieved by positioning a metallic shield at distance x_{so} from the reference coil L_0. The inductance of the sensing coil is a function of the relative displacement w.r.t the target ($L_1 = L_0 \pm \Delta L(x)$). Two coils L_0 and L_1, along with the capacitor C, form a resonator at the frequency $\omega_{osc} = 1/\sqrt{(L_1 + L_0)\,C}$, which is used as the excitation frequency f_{exc} for coils. The LC tank loop current I_{LC} produces the output voltages V_{osc1}andV_{osc2}which are directly proportional to the inductancesL_1 and L_0 respectively. Depending on the design requirements, the excitation frequency may range from a few megahertz up to few hundreds of megahertz. However, the signal bandwidth is a few kHz as the measurand x is a mechanical signal.

The position of the target affects three parameters of the resonator: oscillating amplitude A_{osc}, oscillating frequency f_{osc} and quality-factor Q (losses in the resonator). Each of them can be used as an information carrier for the position of the target. Measuring the frequency is relatively easy and can also be realized in a power efficient way, utilizing simple demodulation techniques [14]–[17]. However, the sensitivity of the oscillator frequency to the target displacement is inferior ($f_{osc} \propto 1/\sqrt{L}$) when compared to the sensitivity of the amplitude or Q which makes it challenging to achieve high resolution (< 10 nm). Another issue with a frequency-output interface is that it is difficult to achieve high stability at high oscillation frequencies and low phase noise (due to small $Q < 20$ at low standoff distance). The Q of the LC tank can be measured indirectly by measuring the loss in the LC tank. This can be done by compensating the additional loss, due to the target displacement, by regulating the oscillator amplitude in a closed-loop configuration [17]. However, the resolution and especially the stability are limited with this approach due to the high thermal drift of the losses. This approach also depends on the stability and precision of the front-end blocks, and hence is useful for moderate displacement resolution applications ($\approx 0.1\ \mu$m). The amplitude output has the advantage of being more sensitive ($A_{osc} \propto L$). The challenge here is the dependence of the resolution and stability of the oscillator amplitude on errors in multiplicative terms as oscillator bias current, oscillator amplitude noise etc. However, this can be mitigated by using another coil as the reference and employing a ratiometric readout to suppress correlated multiplicative errors [8], [9]. Hence we focus on the amplitude demodulation approaches for ECDS in this paper.

To understand the front-end operation for amplitude-demodulation (Fig. 1), one can consider that the baseband displacement signal $\Delta L(x)$ modulates the oscillator output voltage amplitude. In order to detect $\Delta L(x)$, the oscillator outputs V_{osc1} and V_{osc2} are amplitude-demodulated to baseband voltages V_{out1} and V_{out2}, respectively. These voltages are then digitized and a ratio-metric readout $D_{out} = V_{out1}/V_{out2} \approx L_1/L_0$ is performed. This operation suppresses the correlated noise and drift associated with the front-end oscillator [8], [9]. Ratiometric measurement is indispensable for such a high precision and highly stable ECDS interface.

The main functionality of the demodulator blocks is to down-convert the displacement information modulated by the excitation frequency, without adding significant noise, instability or distortion to the measurement. The input-referred noise of the demodulator should be low enough so as not to limit the resolution of the system. The non-linearity of the demodulators has an impact on the cancellation of the correlated errors at the output of both channels when performing the ratiometric measurement. Therefore, the required linearity is decided based on the desired suppression of the correlated noise and drift originating from the front-end oscillator [18]. This performance must be achieved at low power consumption to avoid local self-heating which leads to mechanical and electronic drift.

In order to mitigate limitations introduced by the skin-effect in an ECDS, high-frequency excitation is indispensable. However, a high excitation frequency introduces design challenges in a precise and stable demodulator. In this paper, we discuss design requirements for demodulation in a high precision self-oscillating ECDS interface. Firstly we present linearity and noise considerations for the demodulator block. This is followed by the review of the present state-of-the-art demodulation approaches proven in high frequency ECDS interfaces. Finally we compare these approaches and provide recommendations for implementing a sub-nanometer resolution self-oscillating ECDS interface.

II. Linearity and Noise Requirements for The Demodulator

In this section we discuss important design considerations for demodulation in a high-resolution ECDS interface.

A. Linearity and Stability

As mentioned in Section I, the non-linearity of the demodulator degrades the suppression effect of the ratiometric measurement on correlated multiplicative errors. The noise and drift of the front-end oscillator is found to be correlated and multiplicative in nature. With a ratiometric readout this noise and drift can be successfully suppressed [18]. This analysis does not take into account odd harmonics in the output of the LC oscillator as ideally they are also suppressed by the ratiometric readout.

We studied the impact of the non-linearity of the demodulation block (Fig. 1) on the ratiometric readout in suppressing the correlated noise and drifts associated with a self-oscillating front-end, using COMSOL and MATLAB [18]. Fig. 2 shows that the displacement-to-voltage transfer characteristics of an ECDS interface is associated with two sources of non-linearity: the displacement-inductance relationship of the sensor and the characteristics of the demodulator. The transfer characteristic of the sensor coil, excited at ≈ 200 MHz, is

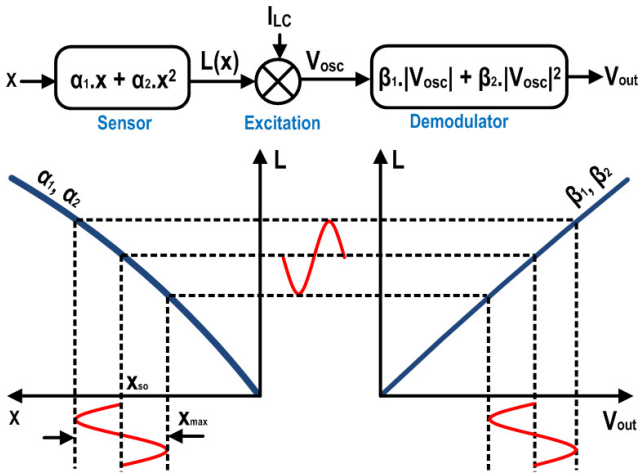

Fig. 2. Non-linearity in an ECDS interface. Displacement (X) goes through two non-linear transfer characteristics of the sensor and the interface respectively.

obtained using a finite element (FE) model in COMSOL. Fig. 3 shows the flat coil used in this analysis. The coil has 6 turns with an outer diameter of 6 mm. The coil's stand-off from a copper target is 55 μm. To obtain accurate simulation results (an accuracy in the order of 10^{-14} H, corresponding to 20 pm), a fine mesh was chosen in the FE model. By minimizing the *RMS* errors a second-order fit was obtained,

$$L_1(x) = L_0 + \alpha_1 (x - x_{so}) + \alpha_2 (x - x_{so})^2 \quad (2)$$

where L_0, α_1 and α_2 are the stand-off inductance, the sensitivity and the 2nd order non-linearity coefficient, and the extracted values of which are 40 nH, 4.49e-4 H/m and -0.96 H/m^2, respectively.

The non-linear behavior of the demodulator, illustrated in Fig. 2, is modelled in MATLAB. The oscillator amplitude is evaluated as $|V_{osc}| = 2\pi f_{osc} L I_{LC}$, where f_{osc} is the oscillation frequency, L is the coil inductance, and I_{LC} is the current flowing in the LC tank. The non-linear interface output is expressed as $V_{out} = \beta_1 |V_{OSC}| + \beta_2 |V_{osc}|^2$. Higher order terms are ignored here as their contribution in the measurement error is practically negligible. For a given oscillation amplitude drift (e.g. 1 %), the largest value of $|\beta_2/\beta_1|$ is evaluated so that the incremental error in D_{out} stays under 1 LSB = 105 pm for $x_{so} = 55$ μm and 19-bit resolution.

Figure 4 shows the variation of the sensor inductance and the oscillation frequency over a 50 μm displacement range around $x_{so} = 55$ μm. The relative change in oscillation frequency is only ≈ 7 % (considering that the oscillation frequency is defined by a single sensor inductor) when compared to relative inductance change of ≈ 25 %. This confirms that the frequency output indeed demonstrates a limited sensitivity.

Figure 5 depicts errors in D_{out} due to the sensor non-linearity, interface non-linearity, and drift with $|\beta_2/\beta_1| = 2e-3$, when compared to an ideally linear sensor with $\alpha_2 = 0$ in (2). The additional error incurred due to the interface non-linearity (difference between the blue and black curves) is much smaller than the absolute error caused by the sensor non-linearity (blue curve), hence the performance is limited by the

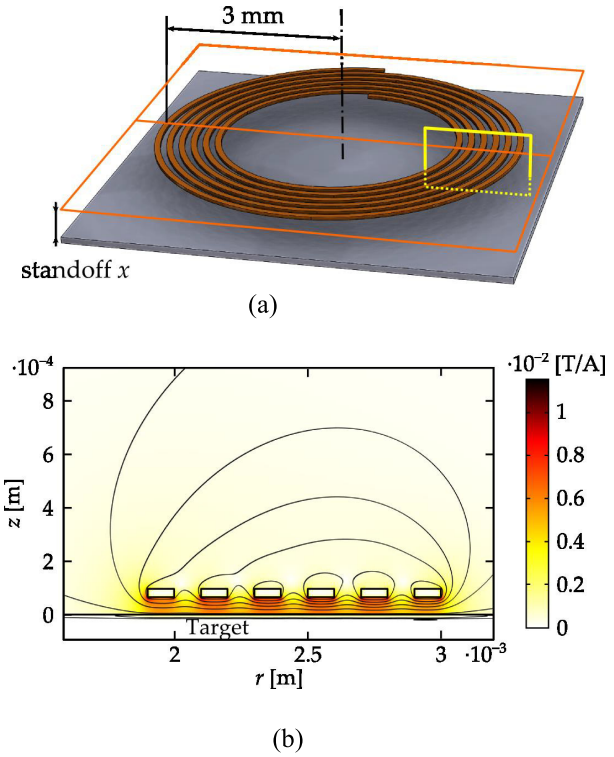

Fig. 3. (a) Illustration of the coil that is used for modeling the sensor transfer characteristics. (b) Magnetic field magnitude in the cross-section close to the coil windings (indicated in yellow in Fig. 3a).

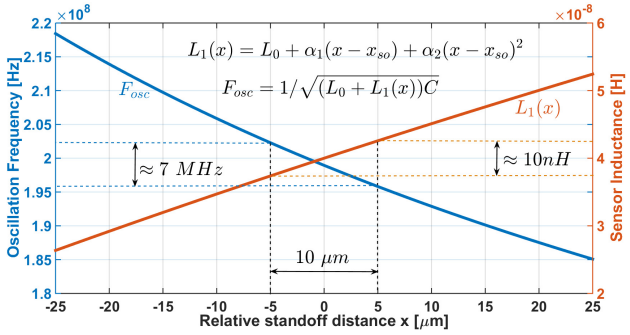

Fig. 4. Oscillation frequency and sensor inductance as a function of displacement relative to standoff $x_{so} = 55$ μm.

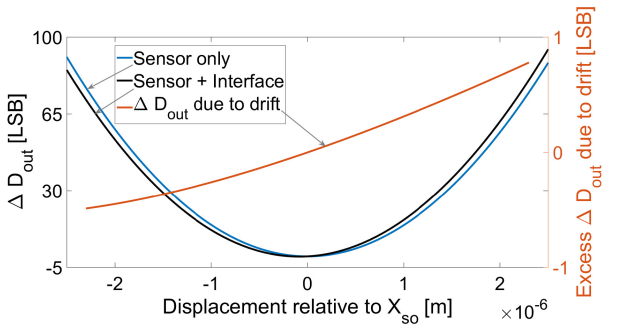

Fig. 5. Errors in the D_{out} vs displacement due to the sensor non-linearity, interface nonlinearity and drift ($x_{so} = 55$ μm).

sensor. Fig. 4 also shows that the excess error in D_{out}, caused by 1 % drift in the oscillator amplitude, remains under 1 LSB. For a 250 mV oscillator output amplitude and $|\beta_2/\beta_1| =$

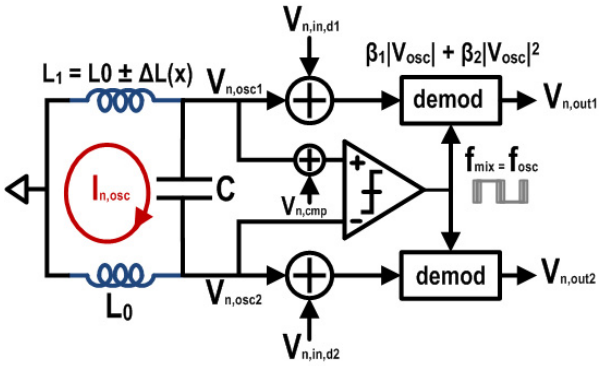

Fig. 6. Noise sources in a self-oscillating ECDS interface.

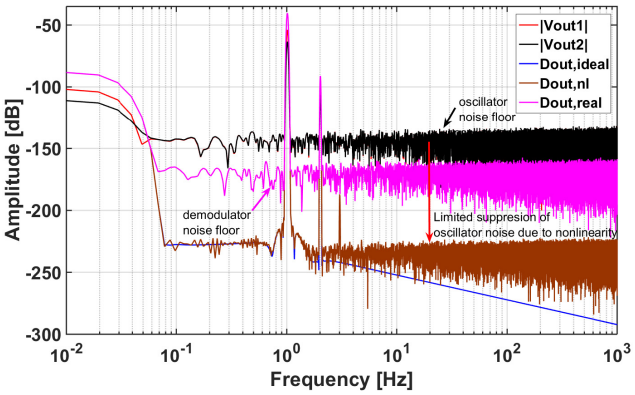

Fig. 7. Output noise spectrum in a self-oscillating ECDS interface.

$2e-3$, the demodulator linearity requirement for tolerating 1 % drift evaluates to -72 dB HD_2 ($=A_{max}|\beta_2/\beta_1|/2$). A tighter drift budget or higher resolution will demand even higher linearity from the demodulator.

B. Noise

In this section, we discuss the effect of important noise sources in a self-oscillating ECDS (Fig. 1). As shown in Fig. 6, the most important noise sources in a self-oscillating ECDS are: (1) the amplitude noise of the excitation oscillator ($i_{n,osc}$); (2) the noise of the demodulator ($v_{n,in,d}$) in the signal path; (3) the demodulator jitter in the clock path (f_{mix}) originating from the comparator noise ($v_{n,cmp}$) and the oscillator phase noise. The jitter of the demodulator clock f_{mix} is not critical in the amplitude demodulation assisted by the ratiometric signal processing because they manifest as multiplicative terms in the both demodulator outputs.

To understand the effect of the other two noise sources, the sensor plus the demodulator are again modelled as discussed in Section II.A. For the demodulator, $|\beta_2/\beta_1| = 2e-3$ is used in the analysis. The displacement is expressed as $x = x_{so} + \frac{x_{so}}{20}\sin(2\pi f_{in}t)$, with $x_{so} = 55$ μm and $f_{in} = 1$ Hz, for 5% maximum displacement (x_{max}) about x_{so}. The noisy oscillator amplitude and *demod* outputs are expressed as:

$$|V_{osc1}| = 2\pi f_{osc} L_1 (I_{LC} + i_{n,osc}) \quad (3)$$

$$|V_{osc2}| = 2\pi f_{osc} L_0 (I_{LC} + i_{n,osc}) \quad (4)$$

$$V_{out1} = \beta_1(|V_{osc1}| + v_{n,in,d1}) + \beta_2|V_{osc1}|^2 \quad (5)$$

$$V_{out2} = \beta_1(|V_{osc2}| + v_{n,in,d2}) + \beta_2|V_{osc2}|^2 \quad (6)$$

with $\sigma_{i_{n,osc}}/I_{LC} =$ 1e-3 and $\sigma_{v_{n,in,d}}/|V_{osc}| =$ 1e-5.

Figure 7 depicts the output spectrum for various cases, in which. the effect of the sensor non-linearity can be noticed. The noise in two outputs V_{out1} and V_{out2} is dominated by the oscillator amplitude noise. Ratiometric readout is helpful in suppressing this noise due to its correlated multiplicative nature [9]. However, this suppression is subjected to the demodulator linearity which is depicted by $D_{out,nl}$ (with no demodulator noise) in Fig. 7. The curve $D_{out,real}$ shows the ratiometric readout spectrum in presence of both the oscillator noise and the demodulator noise. If the ratiometric signal processing ideally cancels out the oscillator noise, the noise floor of the readout function is eventually dominated by the demodulator noise which is uncorrelated between the two channels.

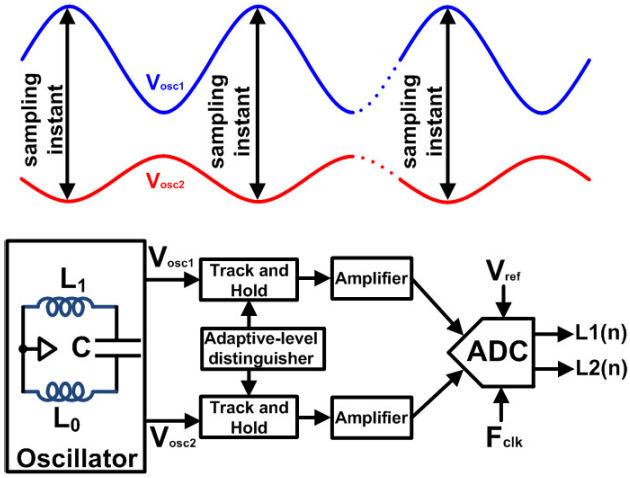

Fig. 8. Simultaneous Sampling based ECDS interface.

Therefore, ratiometric measurement and demodulator linearity are two important considerations to improve both noise and stability performances of the interface. The suppression of the oscillator noise is helpful in reducing the current consumption in it. The demodulator noise is another important design consideration and must be determined as per the resolution requirement by the ECDS interface.

III. State-of-the-Art Demodulation Techniques

In this section we review a number of state-of-the-art demodulation approaches employed for high excitation frequency ECDS interfaces. Advantages and disadvantages of each approach are also addressed.

A. Simultaneous Peak Sampling

Simultaneous sampling is one of the popular and power-efficient approaches to demodulate two AM signals. In this approach two synchronous signals are simultaneously sampled and ratios of the individual samples provide the ratiometric readout output [12]. Fig. 8 depicts the conceptual

block diagram of the ECDS interface, implemented in [12], which employed simultaneous sampling as the demodulation approach. There are two identical channels for two AM inputs $V_{osc1}(t)$ and $V_{osc2}(t)$ respectively. An adaptive level distinguisher (ALD) block is employed which identifies peaks of AM input signals and samples signals only during the peaks. This enables higher signal-to-noise ratio (SNR). Sampling at signal-peaks also makes the system less prone to clock timing related errors, since the signal's change is minimum at the peaks. The samples are also pre-amplified by using a switched-capacitor (SC) amplifier.

Bootstrapped metal-oxide-semiconductor (MOS) switch is employed to mitigate the effect of switch non-idealities as non-linearity, signal-dependent charge injection etc. Sampled signals are digitized using a 2-channel ADC and the output of the ADC is fed to a microprocessor to evaluate the ratiometric readout. A system level auto-zero technique is employed to mitigate low-frequency errors in the system, e.g. opamp offset, flicker noise etc. ALD consists of regenerative SC comparator together with a peak detector and a level shifter. More details about the ALD design can be found in [12].

The front-end resonator was implemented using an off-chip resonator and the rest was designed in a standard 0.35 μm 3.3V CMOS technology. A prototype coil of 4 mm diameter was designed and then its model was extracted using impedance analyzer. This model was used during the simulation of the complete system. The system is simulated at a clock frequency of 25 MHz and comparator working period is about 22 nsec. When the peak detector threshold voltage (in ALD) is considered to be 10 mV below the input signal level, at least one peak can be distinguished in every 0.5 μsec. The complete system achieves 11-bit resolution in 50 kHz signal bandwidth, with 1 mm displacement range (500 nm displacement resolution) and 12 mW power dissipation.

B. Peak Detector

Peak detector (PD) based demodulation is often employed for demodulating AM signals [13], [19]. In this approach, the input signal is tracked only when the input is higher than the output value. By doing this, the whole envelope of the input signal can be tracked using a storage element. The output signal is then low pass filtered to be smoothened. PD based demodulation circuitry typically consists of a diode (or MOS switch) and a capacitor. In an ECDS interface, PD can be embedded in the front-end oscillator [19] or can be a stand-alone block [13].

Figure 9 illustrate an ECDS interface proposed in [19]. The front-end oscillator comprises of an LC oscillator whose losses are compensated by the negative resistance provided by the cross-coupled bipolar junction transistors (BJT). The attractive part of the proposed interface is that the base-emitter (BE) junction along with the RC circuit in the emitter path is utilized to realize the peak-detector, which demodulates AM part of the oscillator output. If voltages $V_{osc1} = V_1\cos(\omega_{osc}t)$ and $V_{osc2} = V_2\cos(\omega_{osc}t)$, then output voltages can be estimated

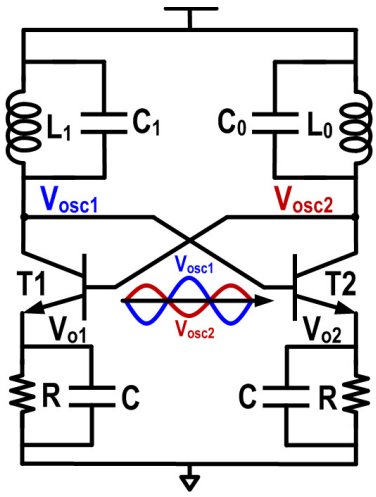

Fig. 9. A self-oscillating ECDS interface with embedded peak detector.

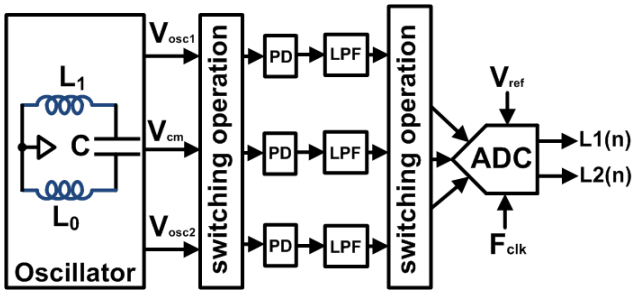

Fig. 10. An ECDS interface with stand-alone precision peak detectors.

as [16],

$$V_{o1} \approx V_1 - V_T \ln\left(\sqrt{2\pi V_1 / V_T}\right) \tag{7}$$

$$V_{o2} \approx V_2 - V_T \ln\left(\sqrt{2\pi V_2 / V_T}\right) \tag{8}$$

where V_T is the thermal voltage of the BE junction. The embedded PD's outputs are found to be non-linear and temperature sensitive.

The above disadvantages of an embedded PD can be mitigated by using stand-alone precision PD blocks. Figure 10 depicts the demodulation approach employed in [13]. A negative-g_mLC oscillator is utilized as the front-end block to excite the sensor and reference coils by a high-frequency sinusoidal current. The demodulator consists of three precision PDs, followed by low-pass filters. Three channels are employed, of which two are used for two oscillator outputs whereas the other is used to detect the common-mode voltage of the oscillator output. The operation of this interface is based on that the inputs of the channels are alternately switched to the outputs of the front-end oscillator, which can be compared with the dynamic element matching function. This operation helps suppress the effect of 1/f noise and offsets originating from mismatches between the channels. An external ADC digitizes demodulator outputs to perform further processing on them like ratiometric readout. The switched-channel technique associates with 12-times averaging to cancel out the offsets. This also improves the resolution by 1.5 bits. The sensor interface was designed in AMS 0.35 μm Si/Ge BiCMOS process and achieves 12.1 bits of effective resolution,

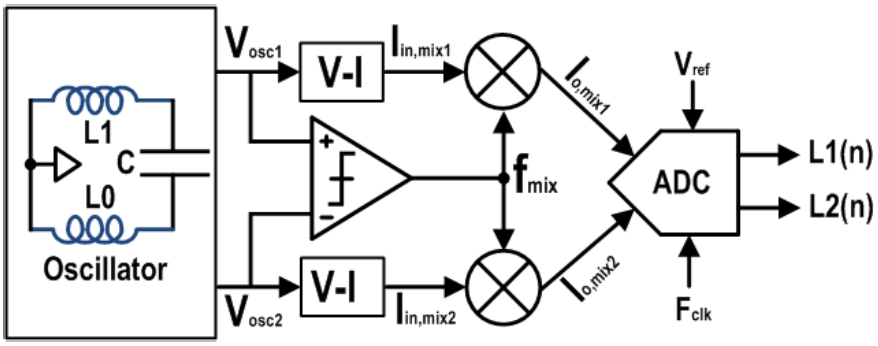

Fig. 11. Synchronous demodulation approach for a self-oscillating ECDS interface.

equivalent to 250 nm displacement resolution. The system consumes 9.5 mW and has a measurement bandwidth of 1 kHz.

C. Synchronous Demodulation

Synchronous demodulation is the most popular approach to demodulate a narrow-band signal situated at a high carrier frequency [22]–[26]. This approach utilizes a down-conversion mixer which can directly demodulate the signal to either DC (homodyne) or at an intermediate frequency (heterodyne). Direct conversion to DC is more advantageous because the baseband circuitry needs to operate at lower frequencies where analog circuitry is more accurate and less power-hungry. On the other hand, low-frequency errors as offset and flicker noise become more important and must be taken care of.

Down-conversion mixer could be a voltage mixer or current mixer, an active mixer or passive mixer. Voltage mixer is typically not favored as they present a switching load to the oscillator and can also form parasitic RLC circuit to cause ringing [8]. Active mixers are always more noisy than passive mixers, especially when it comes to flicker noise. Passive current mixers are more favored than voltage mixers or active mixers, even in RF applications, as they are low-noise and quite linear [27]. However the output of an LC oscillator is typically voltage, hence we need transconductor (V-I) blocks in order to output currents directly proportional to the coils' voltages.

Figure 11 demonstrates the synchronous demodulation approach for an ECDS interface which utilizes a current-driven passive mixer scheme [9]. Two AM oscillator outputs V_{osc1} and V_{osc2} are first converted to currents $I_{in,mix1}$ and $I_{in,mix2}$ respectively using two V-I blocks. Current-driven passive mixers demodulate these currents directly to DC using a clock at frequency f_{mix} which is equal to that of the oscillator. DC signals $I_{o,mix1}$ and $I_{o,mix2}$ are then processed by a baseband ADC to generate outputs L_1(n) and L_2(n). These codes can then be processed by digital backend to calculate a ratiometric readout. The ADC can also directly output the ratiometric readout [28].

A high-precision ECDS interface based on synchronous demodulation approach was presented in [9]. The system employs active transconductor blocks to convert oscillator output voltages to currents, which are then down-converted to DC using current-driven passive mixers. A clock synchronous to that of the oscillator is generated using a continuous-time comparator. Mixer output currents are first converted to voltages using two transimpedance amplifier (TIA) stages, which are then digitized using a dual-input off-chip ADC. Auto-zeroing, chopping, and nested-chopping techniques [29]–[31] are employed to mitigate low frequency errors of mixers and TIA stages.

The ECDS interface was implemented in 0.35 μm 3.3 V SiGe BiCMOS technology. The system consumed 18 mW from 3.3 V supply with the oscillation frequency of about 20 MHz. The displacement range in this work is 3 mm and the maximum inductance of each coil is 70 nH. The interface achieves 15.5 bits of resolution which corresponds to 65 nm of displacement resolution with a few kHz measurement bandwidth.

D. Comparison of Demodulation approaches

The simultaneous sampling demodulation approach has the advantage of having a simple architecture. The sampling process can be made quite accurate. This is helped by that fact that sampling at peaks has robustness against timing errors. But the detection of peaks of high frequency signals is quite challenging, especially for >50 MHz signals. Another problem with this approach is that the sampling process presents switching load at the front-end oscillator output which can produce parasitic RLC oscillations. The sampling process also increases noise due to aliasing. Hence this approach is useful only for moderate excitation frequencies (< 20-30 MHz) and moderate resolution applications. This approach utilizes many passive blocks as switches, capacitors etc which leads to a moderately low power dissipation.

Embedded PD based interface is attractive as it limits the excitation frequency signal to a single block. Hence, it supports much higher excitation frequency and has low power consumption. However, there are many disadvantages of this interface. The most important one is its high temperature sensitivity [20]. This signal dependent drift due to temperature is very difficult to track and can produce thermal drift of thousands of ppm/°C. This limits the usefulness of this demodulation approach for precision applications. Second issue with this interface is that the oscillator works in a voltage limited regime and the output is sensitive to the variations in the

supply voltage. Also, ratiometric suppression of the oscillator noise is ineffective because embedded PD are quite non-linear. Embedded PD based interface is only useful for low precision applications as proximity sensors etc.

In standalone PD based interface, above disadvantages of embedded PD are not present. Also, the only high-frequency block in such a demodulator is an amplifier (LPF) which drives a very small load (gate of a metal-oxide-semiconductor (MOS) switch). Consequently, the power consumption in this approach is not high. However, the demodulator requires a relatively wide bandwidth (e.g., $\times$ 100 kHz) to perform the offset cancellation operation, which causes the associated noise bandwidth to increase. As a consequence, the obtained resolution is in the medium range ($\approx$ 12 bits). This interface approach is an appropriate candidate for applications with medium resolution, moderate excitation frequency ($f_{exc} \approx$ 20 MHz), and a relatively moderate power consumption budget.

Synchronous demodulation based ECDS interfaces have many advantages when compared to other demodulation approaches. Firstly, the ratiometric suppression of noise and drift is quite effective, subjected to the linearity of the demodulator. Power consumption and noise performance are defined by baseband amplifiers, and can be made with significantly low noise. It is also straightforward to use low frequency error cancellation techniques such as chopping and auto-zeroing. The excitation frequency can be made quite high as current-driven mixers can easily work up to few GHz. The main challenge in such an ECDS interface is the linearity of V2I blocks (as Gm cells). It is challenging to attain high linearity at high excitation frequencies. Nevertheless, it is possible to design such blocks with sufficient linearity, subjected to requirement by the ratiometric readout [9]. Synchronous demodulation based ECDS interfaces are useful for applications requiring high precision, high excitation frequency and with moderate power consumption budget.

Table I summarizes the comparison of these demodulation approaches, based on excitation frequency, resolution, stability and power dissipation.

TABLE I

COMPARISON BETWEEN DEMODULATION APPROACHES FOR ECDS INTERFACE

Specifications	Simultaneous Sampling	Embedded Peak-detector	Precision Peak-detector	Synchronous Demodulation
Excitation frequency	Low	High	Medium	High
Resolution	Medium	Low	Medium	High
Stability	Medium	Low	Medium	High
Power dissipation	Low-Medium	Low	Medium	Medium-high

IV. FUTURE DIRECTIONS, CONCLUSION AND SUMMARY

The next generation of ECDS interfaces must solve a number of critical issues to cope with the requirements for a sub-nanometer resolution. To relax dynamic-range of the demodulators (hence power consumption), the sensor offset which is introduced by the large standoff distance and skin depth has to be compensated before its amplification. For example, an ECDS interface with 0.1 nm resolution, with $x_{so} = 100\ \mu$m and $x_{max} = 10\ \mu$m, will require $\approx$ 20 bits dynamic range without sensor offset compensation. For a fixed power budget, this can only be attained by sacrificing bandwidth. However, sensor offset compensation will relax the dynamic range by 10 times. This offset compensation will also improve the linearity performance of the demodulator because the amplifiers need to process the dynamic part of the sensor signal excluding the large sensor offset.

Power efficient, low noise and linear voltage-to-current conversion is indispensable for efficient synchronous demodulation based ECDS interfaces. Passive components can be utilized as voltage-to-current converters to obviate the use of active blocks as G_m cells. Another attractive solution could be the use of bandpass delta-sigma ADC to shift the down-conversion operation to the digital domain. This can be helpful in obviating DC errors since this type of data converter have a bandpass characteristic, and the mixing operation can be very accurate since it is performed in the digital domain. However, power-efficient resonator architectures are required to meet power consumption budget.

In this paper, we studied design requirements for demodulation in high-frequency self-oscillating ECDS interface. We also presented a comprehensive study of popular demodulation techniques for such interfaces and their pros and cons were addressed. Various challenges posed on the design of the demodulator by the high frequency operation were identified and discussed. We analysed noise, linearity, and stability requirements for a demodulator in a sub-nanometer sensor interface. Finally we made recommendations about the next generation demodulators to push ECDS interfaces in sub-nanometer resolution applications.

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