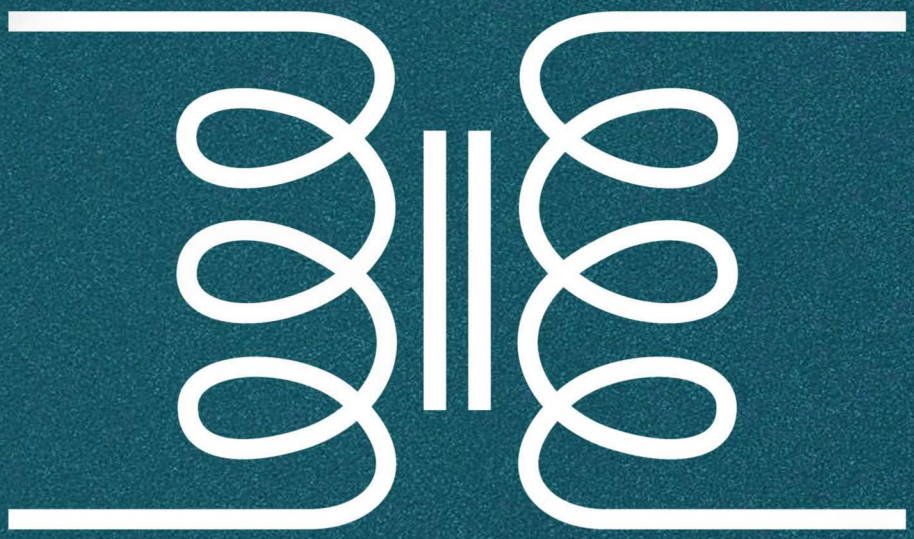
Galvanic Isolation Communication Link

Thomas John

Technische Universiteit Delft



TU Delft

Galvanic Isolation Communication Link

by

Thomas John

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Thesis committee:

dr. Kofi Makinwa,	Electronic Instrumentation, TU Delft, promoter
dr. Qinwen Fan,	Electronic Instrumentation, TU Delft, supervisor
dr. S. M. Alavi,	Electronic Circuits and Architectures, TU Delft
dr. M. A. P. Pertijs,	Electronic Instrumentation, TU Delft

TU Delft

Abstract

Digital isolators are devices that connect one electrical system block to another over a galvanically isolating barrier. They allow electrical systems to communicate with each other even though they may operate at vastly different potentials. They also do the job of eliminating potentially damaging ground loops between the two systems.

This thesis presents a digital isolator based on inductive coupling. It presents a better alternative to the traditional approach of using optocouplers. The design employs a transmitter and a receiver which communicates digital signals over an isolation barrier with emphasis on low power and high common-mode rejection. The design achieves a common-mode transient immunity of 100kV/us, a data rate of 50Mbps, power consumption of 2mA per channel and signal delay less than 15ns.

Acknowledgements

The last year has been nothing short of eventful. I have learned, I have grown, and I have made friendships that I hope will last a lifetime. The inception, growth, and conclusion of my thesis would not have been possible without the help of several people.

Firstly I would like to thank Dr. Kofi Makinwa for his support of the project and his invaluable feedback over its duration which helped me better my project. I would also like to thank Dr. Qinwen Fan for her technical guidance and mentoring over the past year.

I am indebted to my manager at NXP, Mr. Marco Maccarrone for giving me an opportunity as well as having faith in me to work on and complete this project. His patience and calm demeanor will forever serve as lessons for me to aspire to, I could not have asked for a better manager. I would like to thank Dr. Johan Huijsing, who spent countless hours carefully guiding me through the intricacies of circuit design, without him my project would have been dead in its tracks.

I am beyond grateful to Priyanka Bhat for her constant words of encouragement and motivation even at moments when I wanted to give up. I am also grateful to Shubham Khandelwal who has without hesitation lend a helping hand at moments that I needed it the most. My days at NXP Nijmegen would not have been as fun or eventful without my friends Melwin Thomas and Sagar Patel, I am a far better foosball player now because of you. I would also like to thank my friends at TuDelft who undertook this journey with me, Chaitra Pai, Raghu Mohandas, Rishabh Nagarkar, Abhairaj Singh, Pinakin Padiala, Yashwanth Vayza, Shardul Rautmare, I have become a better person from having known you all.

Thomas John
Delft, September 2019

Contents

1 Introduction

An electrical isolator is by definition a non-conducting material that electrically separates two parts of a system. And, it is often necessary to still transmit data and power over such an isolation barrier as shown in Figure 1.1. Establishing such a link is difficult because they must in no way affect the integrity of the isolation while at the same time maintain a link between the two parts. This means that it must operate reliably in extremely harsh conditions which may involve strong electromagnetic fields, electrical surges, fast transients, and high noise floors. Traditionally there are several components that can be used to couple two isolated systems such as transformers and optocouplers.

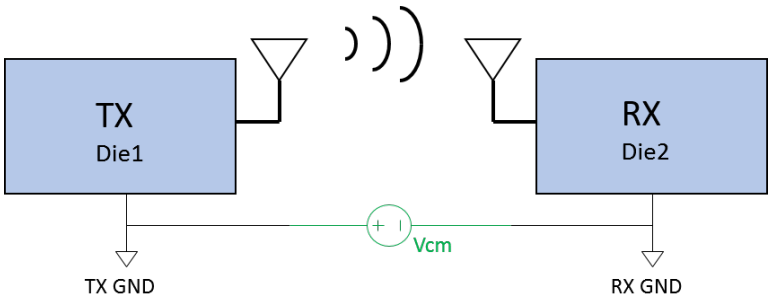


Figure 1.1: Basic Representation of a Digital Isolator

Because of their smaller size, ease of usage and manufacturing, optocouplers have been the primary choice for communication across isolations. However, in the last decade there has been a growing interest in other options due to certain inherent limitations of the optocoupler (Section 2.2). This thesis aims to focus on an isolation communication link that is inductively coupled across an isolation barrier.

1.1. Motivation

A lot of applications need isolation, especially those that involve control systems interacting with high voltage systems, e.g: gate-drivers. Without isolation, establishing such links is quite difficult. As devices get smaller and faster, manufacturers need

solutions that not only offer a high isolation rating but can also be realized in IC technology. Digital isolators are coupling solutions that involve capacitive or inductive links instead of optical coupling [1]. A digital isolator consists of a transmitter and receiver separated by an isolation barrier, with its output logic state determined by the presence or absence of an inductively or capacitively coupled high-frequency (HF) carrier instead of light. Compared to conventional optocouplers this isolation barrier can better withstand high-voltage stress and has improved immunity to large, common-mode transients, resulting in higher reliability and data integrity [2]. Optocouplers realized with Gallium Arsenide (GaAs) and Gallium Arsenide Phosphide (GaAsP) technology are easily outclassed by digital isolators [3]. Digital isolators offer higher performance at lower power, higher common-mode rejection and narrower receiver bands which allows for tighter frequency discrimination. Besides, the cost of optocouplers is proportional to the number of channels which is not the case for digital isolators [3] .However, digital isolators are still finding it hard to make their way into mainstream usage since a lot of manufacturers prefer to stay within their comfort zone and stick to optocouplers. The goal of this thesis will be to explore an inductively coupled solution with particular emphasis on low power and high common-mode rejection.

1.2. Thesis Organization

The thesis is organized into 7 chapters. A brief description of each following chapter is written below:

- **Chapter 2: Digital Isolator Technology**: Different ways of achieving isolation are discussed, followed by an in-depth analysis of the most commonly used methods. Also, the most commonly used communication protocols are described.
- **Chapter 3: System Overview**: A top-level overview of the proposed system along with its specifications is presented.
- **Chapter 4: Transmitter Design**: Provides an in-depth analysis of the transmitter.
- **Chapter 5: Receiver Design**: Provides an in-depth analysis of the receiver.
- **Chapter 6: Results**: Presents the simulations results and measurement results.
- **Chapter 7: Conclusion and Future Works**: The conclusion of the thesis is presented along with suggestions for future designs.

2

Digital Isolator Technology

Digital isolator technology came into the limelight almost ten years ago in order to tackle the shortcomings of the optocoupler. This chapter explores the benefits of digital isolator technology in comparison to optocouplers.

2.1. Methods of Isolation

When creating an isolation link, the first and foremost problem to be tackled is the means of establishing a link. Three approaches can be used to transfer a signal across a galvanic isolation: Magnetic (inductive) coupling, Capacitive coupling, and Optical coupling as shown in Figure 2.1.

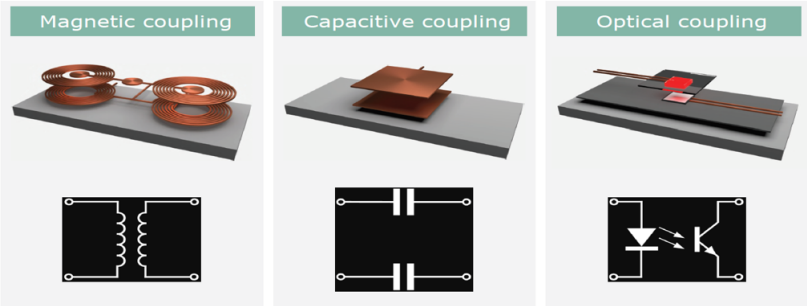


Figure 2.1: Different Types of Isolation Methods

2.2. Drawbacks Of Opto-couplers

Amongst the three, the optocoupler is without question the most well known and most widely used. As shown in Figure 2.2 it works by emitting light whenever there is a high input at the IN port, the photodetector picks up this light and turns the output transistor on. Similarly, the photodetector turns the output transistor off when the signal at port IN goes low.

Optocouplers are easy to use, reliable and have decades of validation to back them up. However, they have two main drawbacks [3]:

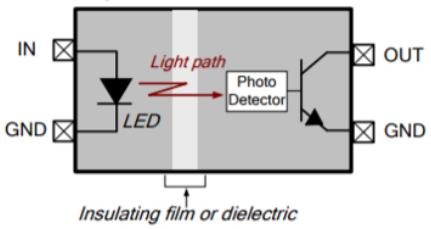


Figure 2.2: Optocoupler Technology

- Longevity
- Power Consumption

2.2.1. Longevity

Silicon Labs made a detailed comparison comparing the performance of their digital isolator products against that of optocouplers. Figure 2.3 shown below is a test run by the research team where they measure the light output of GaAs (Gallium Arsenide) LEDs over 10,000 hours [3].

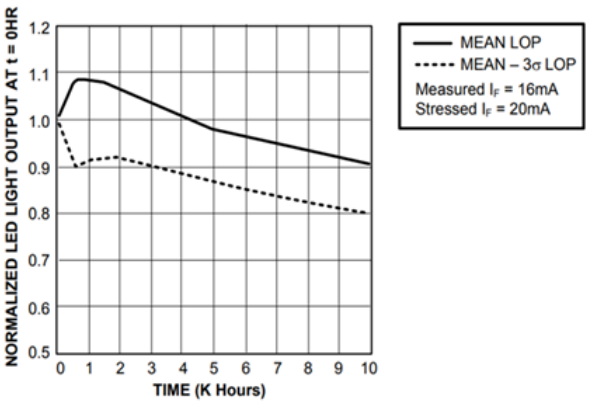


Figure 2.3: Optocoupler Light Output over Time [3]

The light output was normalized at the start of the test and then onwards measured continuously for the duration of the experiment. Over this relatively short duration, there was a 20% decay in light intensity in the worst-case scenario. This is a process that goes on for the entire life-cycle of the LED, and so optocouplers have a reduced life-time. An optocoupler's light output is directly proportional to the current it consumes and a certain minimum light intensity is required to activate the photo-detector. This means that an optocoupler has to supply an increasing amount of current to maintain a consistent data rate over its lifetime. This experiment shows a clear degradation of LED's over a relatively short period of usage. Passive components like capacitors and inductors, however, do not suffer this rate of degradation.

2.2.2. Power Consumption

Another result which may have been the major contributor to the paradigm shift in isolator technology is the difference in power consumption between optocouplers and

digital isolators. In the same test by Silicon Labs, the researchers also generated a graph comparing the optocouplers supply current vs its data rate of communication [3]. This is shown in Figure 2.4.

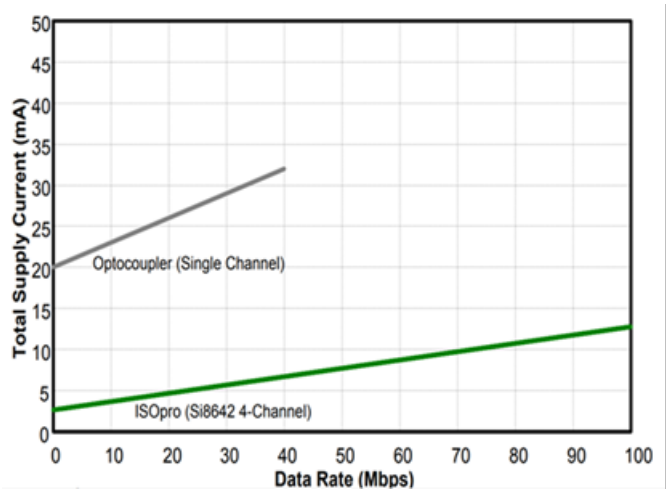


Figure 2.4: Current vs Data Rate Graph [3]

From the graph, we can infer that there is a measurable increase in current consumption with an increase in data rate. However, the difference in the power requirement of the two is quite evident, also, a limitation in the transmission rate of optocouplers can be seen at around 40Mbps. If we are to make our devices smaller and faster then this experiment shows us that optocouplers may not be the best way forward. The limitation in communication speed and the large power requirements can be a major constraint in power limited and space limited applications [2].

2.3. Digital Isolator Communication Protocols

The majority of Digital Isolators are based on either capacitive or inductive coupling. However, the communication protocol used to transfer information in the two cases is quite different. In this section, a high-level analysis of these protocols will be presented to provide some insight into the design choices made during the work described in this thesis.

2.3.1. Capacitive Coupling

Capacitive isolators usually use an edge-based communication protocol [1]. This involves coupling fast transients across isolation capacitors. The top-level view of such a system is shown in Figure 2.5.

A single-ended input signal entering the channel is split into a differential signal via an inverter. The following RC networks convert the signal into small and narrow transients, which are then converted into rail to rail differential pulses by two comparators. The comparator output drives an SR latch which does the job of providing the final output signal. The capacitively isolated systems have the benefit of being fast. However, transients in the relative common-mode voltages of the transmitter and the receiver

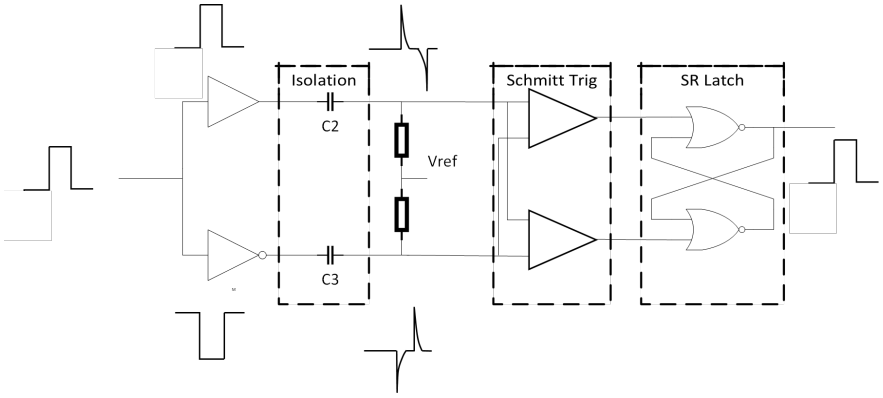


Figure 2.5: Capacitive Isolation Communication Protocol

are also coupled via the isolation capacitors and this can cause bit errors. As a result, capacitive isolators have a high data-rate, but low common-mode transient immunity [2].

2.3.2. Inductive Coupling

Inductive isolators typically use an ON/OFF Keying method. Figure 2.6 shows a top-level view of how such systems operate [1]. The system consists of a transmitter and a receiver inductively coupled across an isolation barrier. The receiver converts digital signals (at point A) into modulated high-frequency signals. These signals consist of high-frequency oscillations every time a logic 1 is presented at A. The receiver picks up this modulated signal and demodulates it to recreate the original signal at output B. Figure 2.7 shows an example of what an ON/OFF keying signal and its modulated signal looks like. The final output signal is simply a delayed version of the input.

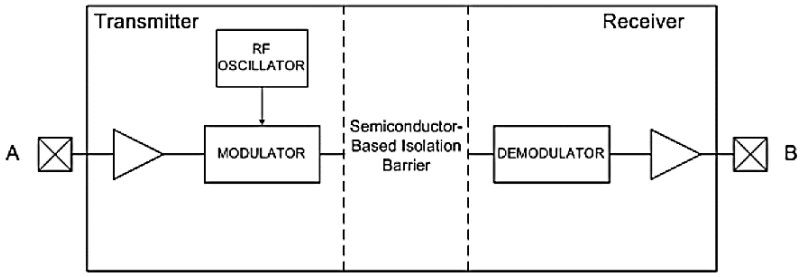


Figure 2.6: Conceptual Diagram of Inductive Communication protocol based system [1]

2.3.3. Conclusion

One of the major points of focus of this thesis is a high CMTI. The relative common-mode transients couple across the transmitter and receiver via the capacitances the isolation offers. This inherently makes capacitive isolators a less preferable choice. The only capacitance offered by inductive coupling is the parasitic capacitances of the isolation material. This results in far smaller common-mode signals being transmitted between the two side.

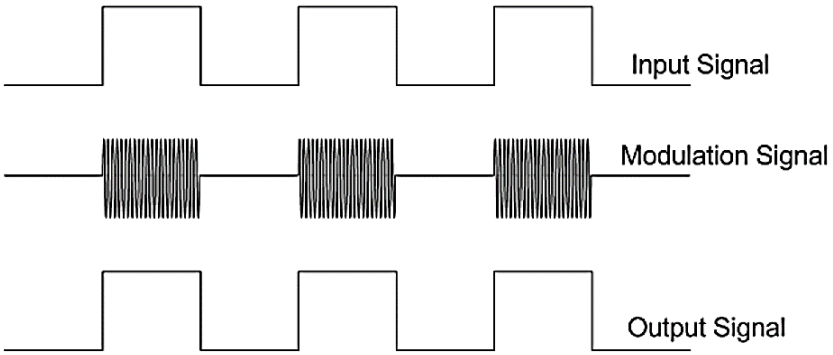


Figure 2.7: Representative signal in Inductive Communication

3

System Overview

A top-level of the system proposed in this thesis is presented in Figure 3.1 . It consists of a transmitter and a receiver inductively coupled over an isolation barrier. It uses an ON/OFF keying input as described in Section 2.3.2.

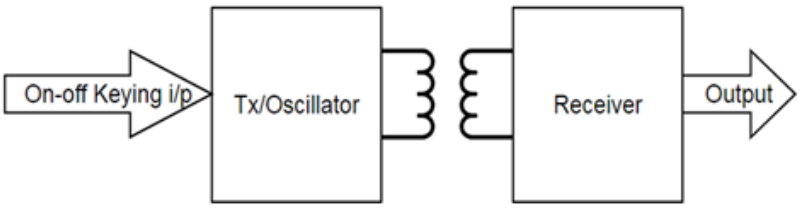


Figure 3.1: Overview of Proposed System

The system can be further broken down into three integral parts; mainly an oscillator, an amplifier and an envelope detector as shown in Figure 3.2.

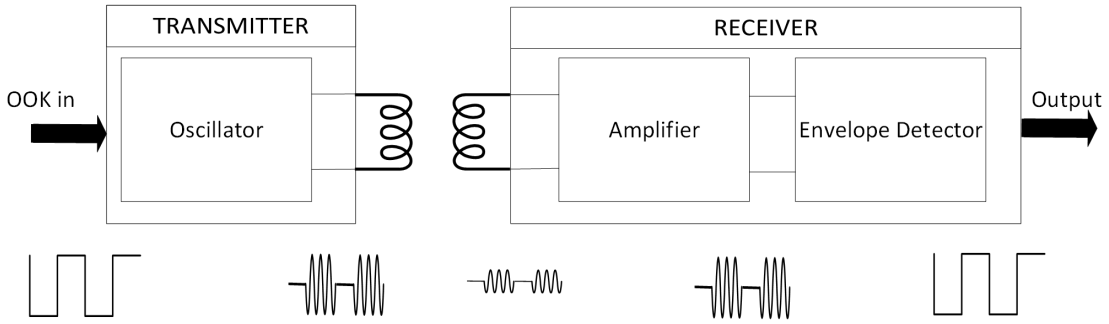


Figure 3.2: Signal Propagation across the system

The ON/OFF keyed digital input is modulated by the oscillator into high-frequency oscillations. These oscillations are coupled across the isolation. The isolation causes an attenuation of a factor of 10. The input amplifier receives this signal and amplifies it by a factor of 10, following which it is passed onto an envelope detector. The job of the envelope detector is to convert these signals back to their original format.

3.1. System Parameters

The system was built keeping in mind a few parameters as required by the application. The exact specifications are shown in Table 3.1.

Specifications	Target
Supply Voltage	1.8V
Power Consumption (Transmitter)	<1mA
Power Consumption (Receiver)	<1mA
Propagation Delay	<15ns
Common Mode Transient Immunity (CMTI)	100kV/us

Table 3.1: System Specifications

The power budget per link of 2mA was equally split between the transmitter and receiver. A speed of 30Mbps was required and a Common Mode Transient Immunity (CMTI) of 100kV/us. The common-mode transient event and its effects are explained in detail in Section 3.2. An earlier design by NXP used a similar architecture. Some aspects of the oscillator design such as the ON/OFF control (Section 4.4) and the inductor coil was used from that design. Designing the system to operate during large CMTI events as well as maintaining a low power consumption were some of the main challenges of this design. To get a better understanding of where the specifications lie in comparison to other digital isolator solutions, a study of the relevant literature has been made and a comparison is shown in Table 3.2. The table intends to show the relevance of this work when compared to other works of similar nature.

Specifications	ISSCC-16 [4]	SiLabs-Si861x [5]	RFICS-17 [6]	This Work
Supply Voltage	1.8V	2.5V-5V	3.5V	1.8V
Coupling Method	Inductive	Inductive	Inductive	Inductive
Temperature	-40C to 150C	-40C to 150C	-	-40C to 150C
Isolation Rating	5kV	5.5kV	3.3kV	6kV
CMTI	80kV/us	50kV/us	-	100kV/us
Data Rate	40Mbps	150Mbps	32Mbps	50Mbps
Power	-	5.5mA	-	2mA
Modulation Type	OOK	OOK	OOK	OOK
Signal Delay	-	10ns	17.6ns	14.2ns

Table 3.2: Comparison with other state of the art work

The CMTI rating and power consumption are comparable or better than other works. The Silicon Labs product offers a far better data rate but at the cost of more than twice the power.

3.2. CMTI explained

One of the key parameters with which an isolation link is judged is its capacity to reject common-mode transients. This is referred to as Common Mode Transient Immunity

(CMTI) [7]. Such transients consist of any spikes that may occur between the grounds of the transmitter and receiver as shown in Figure 3.3. Good CMTI is especially important when an isolator is used in high power applications.

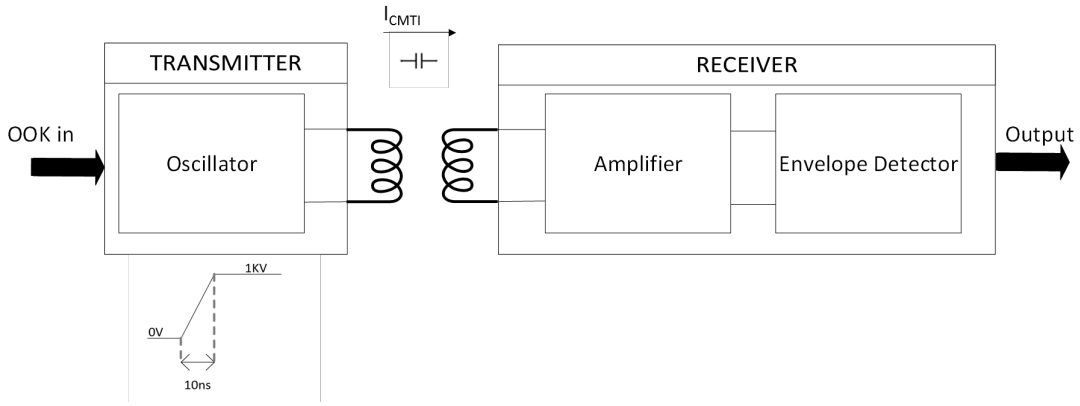


Figure 3.3: CMTI event

As shown in Figure 3.3, consider the case when a large 1kV pulse with a rise-time of 10ns occurs at the transmitter ground relative to the receiver ground. This will force the transmitter ground voltage to shoot up and create a large dV/dT between the transmitter and the receiver. The parasitic capacitance offered by the isolation will then act like pulsed current sources and dump current into the receiver. If this occurs during data transmission, then the data at the receiver output could very well be corrupted by these common-mode transients at the receiver input. Sections 4.2.1 and 5.3 explains in detail the measures taken to improve the CMTI of this design.

4

Transmitter Design

4.1. Transmitter Components

This chapter discusses each of the sub-blocks that constitute the transmitter. The transmitter consists of 5 main components.

- Oscillator
- Dummy oscillator
- Capacitor Bank
- Constant Gm biasing circuit
- Oscillator On/Off switching circuitry

The purpose of each block and the design methodology used are explained in the following sections. The design of the inductor coil and its parameters are not within the scope of this thesis. We use a pre-existing model from a previous design and the extracted values from that design.

4.2. Oscillator Design

In deciding the oscillator, the two main points of focus were that the oscillator needs to be low-power and exhibit fast-startup behavior. As compared to the more common NMOS only Voltage Controlled Oscillator (VCO), the complimentary VCO structure has the benefit of providing twice the transconductance for the same current [8]. This results in a faster switching rate and a larger output amplitude. Shown in Figure 4.1 is a complementary cross-coupled VCO.

An additional capacitor bank was also deemed necessary to allow for frequency trimming. The functioning of this block will be explained in Section 4.3. The condition required for oscillations to begin is quite simple, the oscillator must provide sufficient negative resistance to overcome the parasitic resistance introduced by the inductor core R_p. To calculate this, we start with the known quantities:

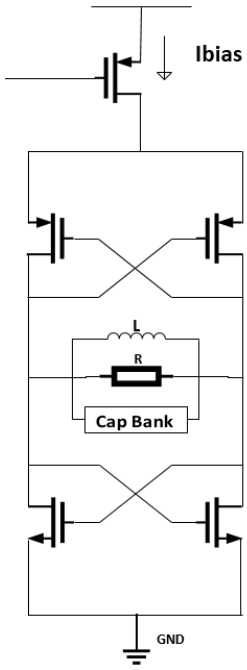


Figure 4.1: Cross-coupled VCO

$$F_{min} = 0.33GHz$$

$$F_{max} = 0.45GHz$$

$$L = 180nH$$

$$F_o = 0.36GHz$$

$$Q = 3.4$$

From these values we can calculate the R_p (parasitic resistance) and C_p (parasitic capacitance). We know that

$$F_o = \frac{1}{2 * \pi * \sqrt{L * C}} \tag{4.1}$$

This gives the solution for

$$C = \frac{1}{(2 * \pi * *F)^2 * L}$$

From this we obtain a C of 1085fF. Since the value of R_p is frequency dependent we calculate it using Equation 4.2.

$$R_p = 2 * \pi * F * L * Q \tag{4.2}$$

We can use this to solve for R_p

$$R_p = 1700\Omega \tag{4.3}$$

Once R_p has been calculated we know how much negative resistance is required to overcome R_p. And based on this we can calculate the required g_m of the oscillator core. During each cycle, the oscillator can be modeled as two negative resistance and an inductor as shown in Figure 4.2. Assuming

$$g_{mnmos} = g_{mpmos} = g_{mcore} \tag{4.4}$$

Therefore, the total negative resistance offered by both the NMOS and PMOS can be written as $\frac{2}{g_{mcore}}$. And so, we need a minimum g_m such that

$$\frac{2}{g_{mcore}} > R_p \tag{4.5}$$

Therefore, From Equation 4.5 we calculate that we need a minimum g_m of 4mS. We take twice the value to ensure smooth operation across PVT (Process, Voltage and Temperature).

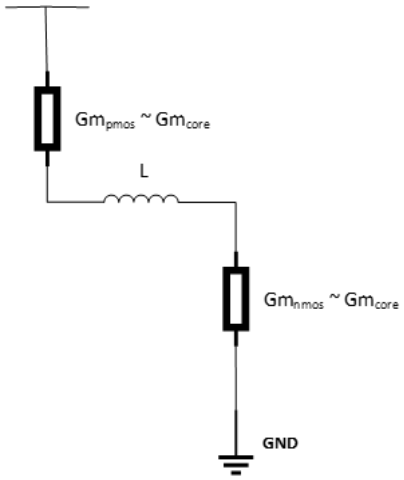


Figure 4.2: Equivalent Diagram of Oscillator during one half-cycle

Once we know the necessary g_m we can calculate the tank amplitude. At resonance the admittance of L and C will cancel, leaving an impedance of R_p. The differential pair can be modeled as a square-wave current source with amplitude I_{tail}, and since the LC tank filters out the higher harmonics, the tank amplitude can be found to be as shown in Equation 4.6 [9]. Since we know that the isolation attenuates the signal by a factor of 10, we need to maximize the oscillation amplitude. We take a value of 1.2V for the value of V_{tank}.

$$V_{tank} = I_{tail} * R_{eq} \tag{4.6}$$

Using Equation 4.6 we arrive at a value of 675uA for the I_{tail}. We know the relation between g_m and I_{bias} as shown in Equation 4.7. Using $I_{bias} = I_{tail}$, we can calculate the sizing of the MOSFETs by using the same Equation.

$$gm = \sqrt{2 * \mu * Cox * \frac{W}{L} * Ibias} \tag{4.7}$$

If we take a gm of exactly 2x as calculated, and fix L at a minimum of 0.4um. We arrive at the following widths for the MOSFETS as shown in Equations 4.8 and 4.9.

$$W_{pmos} = 60um \tag{4.8}$$

$$W_{nmos} = 30um \tag{4.9}$$

4.2.1. Correction for CMTI

As mentioned earlier one of the biggest problems plaguing isolator systems is the effect that CMTI events have on the data. The CMTI event, the oscillator output, and the final demodulated output are shown in Figure 4.3.

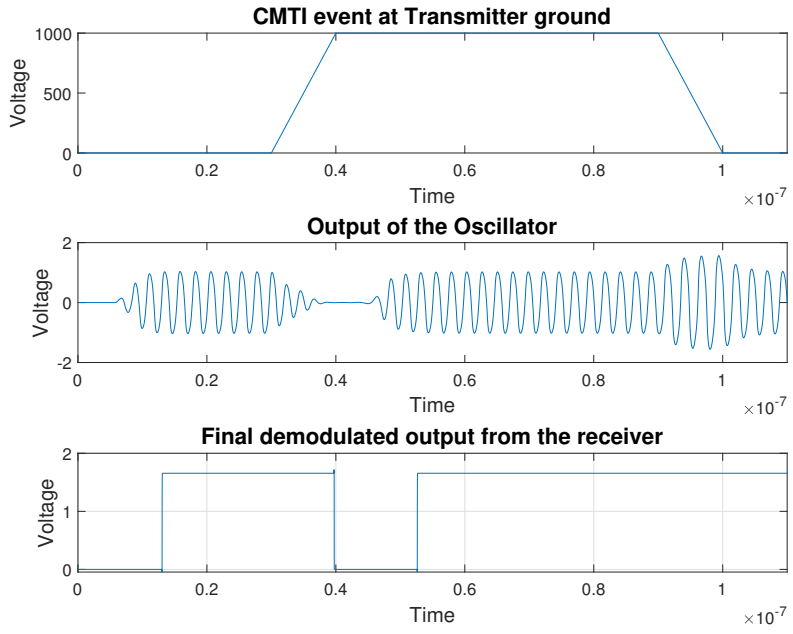


Figure 4.3: Effect of CMTI

During a CMTI event on the transmitter ground, the transmitter goes up by a dv/dt of 100kV/us. This would cause the parasitic capacitances in the isolation to act like pulsed current sources and dump a lot of current into the receiver. This current will be sourced from the oscillator core. Essentially, the oscillator current source will be unable to provide this amount of current during its oscillation (OOK input=1). When all the current from the oscillator core is routed into the isolation then the cross-coupled oscillator will no longer have the necessary negative resistance to sustain the oscillation. The resultant oscillations would die down. This would force it to propagate a false zero. It is the rate of change of voltage that matters and not necessarily the

peak value that it reaches. Therefore for simulation purposes, it can be translated to 1kV/10ns. However, during the -dv/dt slope the receiver would dump a lot of current into the transmitter. From Equation 4.6 we know that the current is directly proportional to the signal amplitude. Therefore this would cause an increase in the amplitude of the oscillation. This does not pose a problem since an increased amplitude would still propagate as a 1 to the output. To counter this problem, we need to find a solution that can supply the additional amount of current needed to sustain the oscillation during the CMTI event. The method used for that is shown in Figure 4.4.

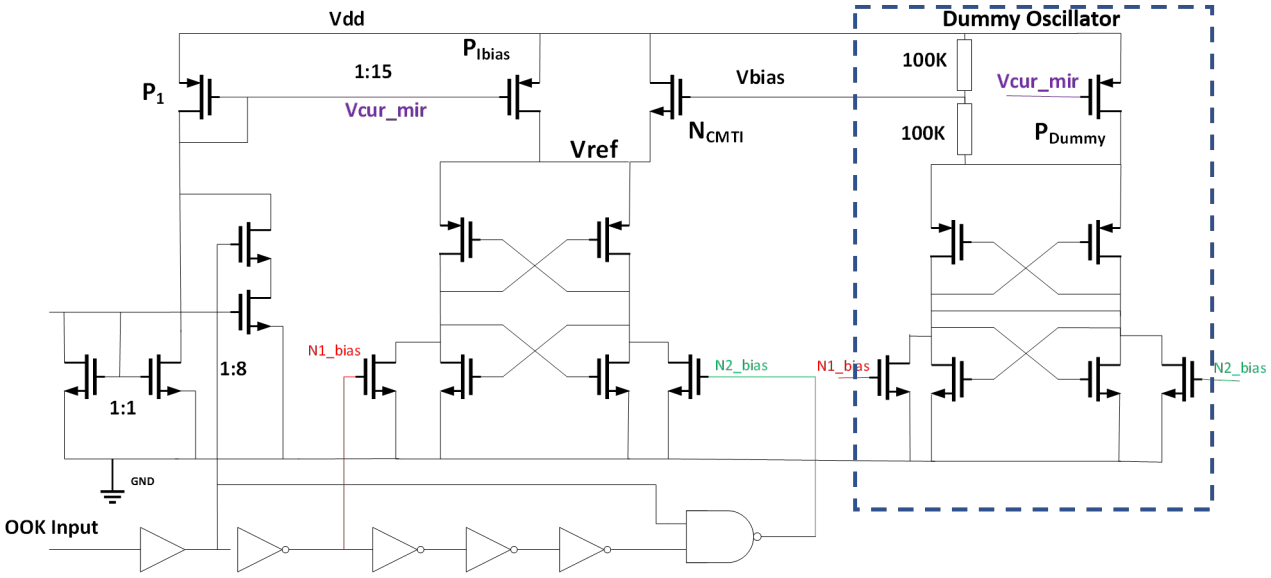


Figure 4.4: Complete Oscillator Circuit

An NMOS (N_{CMTI}) is added in parallel to P_{Ibias} where $V_{bias} = V_{ref} + V_{th}$ and V_{th} is the threshold voltage of N_{CMTI}. During the CMTI event when P_{Ibias} is forced to source extra current and cant, V_{ref} gets pulled down as the oscillations die down. N_{CMTI} provides the necessary current required to sustain the oscillations because the lowering V_{ref} increases the overdrive voltage of N_{CMTI} and forces it to supply even more current. During normal operation, N_{CMTI} is turned off and does not leak any significant current. To ensure the appropriate biasing of N_{CMTI}, a dummy oscillator is added in parallel to the main oscillator. This dummy oscillator was sized at a fraction (1/15) of the original oscillator and consumes only a very small current. Its purpose is to track the value of V_{ref} accurately over PVT. A resistance divider of 200K is added in parallel to the current source P_{Dummy} to up-convert the tracked voltage by an approximate value of the V_{th} of N_{CMTI}. The resulting oscillation during a CMTI event looks as shown in Figure 4.5. It can be seen that during the occurence of the +dv/dt slope of the event the additional current supplied by N_{CMTI} is able to sustain the oscillation which leaves the output uncorrupted.

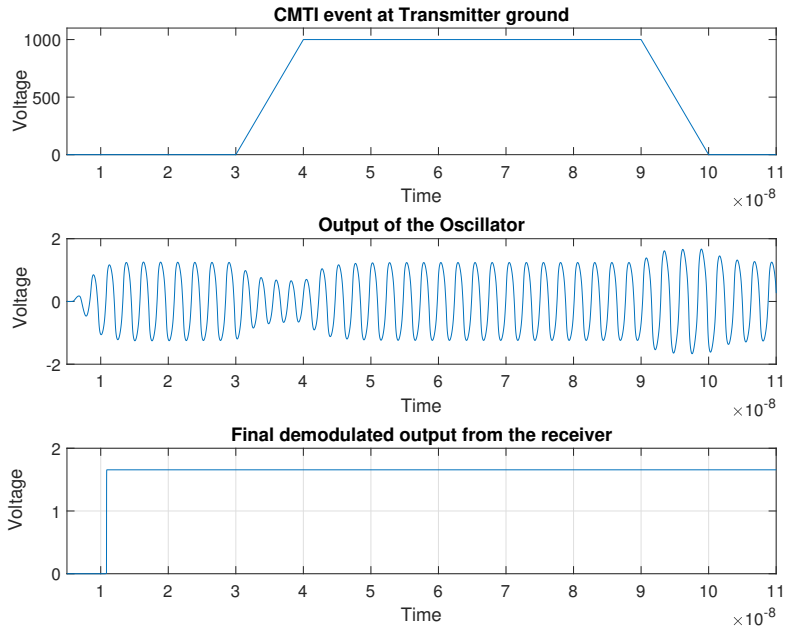


Figure 4.5: Effect of CMTI event after corrective measures

4.3. Capacitor Bank

The capacitor bank is placed in parallel to the inductor to allow frequency trimming. The design of the bank is quite simple, and it is digitally controlled as shown in Figure 4.6.

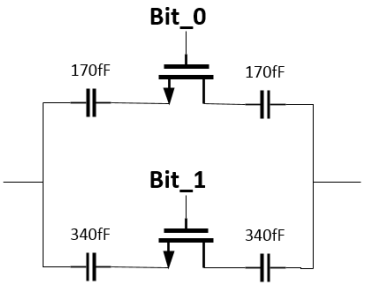


Figure 4.6: Capacitive Bank

From Equation 4.1, we know the capacitor value has an inverse relation to the oscillation frequency. This system tunes the oscillation frequency by changing its capacitive load. In this case, two capacitors, when enabled, load the oscillator with a capacitance of C/2 (Figure 4.7) [10]. However, the DC level across the switching transistor is undefined and therefore a pull-up and pull-down structure is required [11]. The structure implemented is shown in Figure 4.7. In Figure 4.7, the nodes 'Osc_out1' and 'Osc_out2' are connected across the inductor coil.

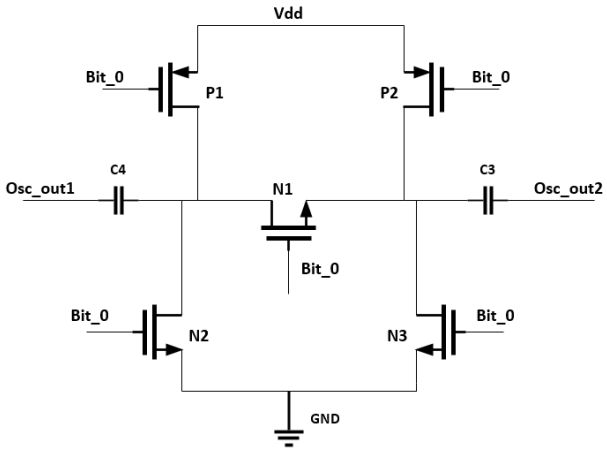


Figure 4.7: Complete Capacitor Bank Circuit for one bit

When Bit0 = 0, the source and drain of N1 is pulled up by P1 and P2. This would also put the Vgs of N1 to be 0 thereby turning the switch OFF.

When Bit0 = 1, the source and drain of N1 are pulled down by N2 and N3. The Vgs of N1 are then maximum at 1.8V thereby turning it on and connecting C3 and C4.

4.4. On/Off Control Design

An important requirement for the transmitter is to minimize power consumption as much as possible during the Off state. That is, when the input is zero, the power consumption should be minimal. A series of inbuilt switches in the biasing circuitry ensure that the oscillator is completely off when the input is low. Figure 4.8 shows the VCO along with its biasing structure.

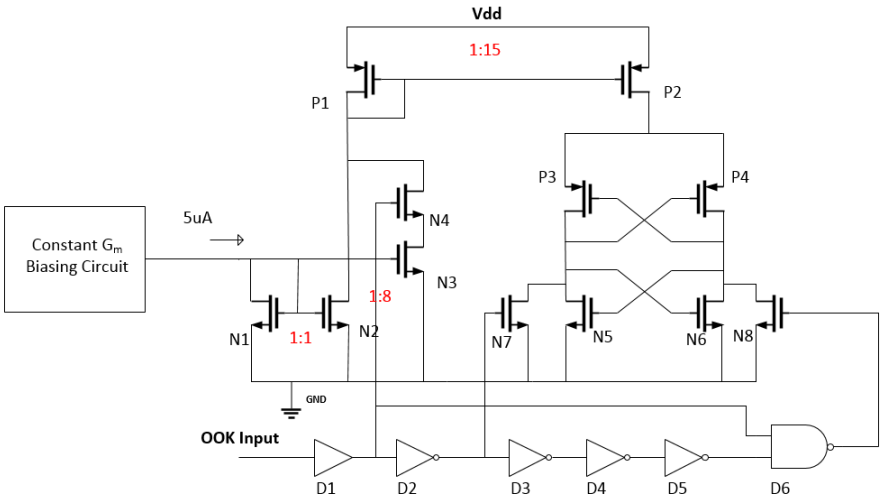


Figure 4.8: Transmitter Switch Circuit

At nominal conditions and room temperature, the constant Gm biasing circuit provides a 5uA current to N1. The current under these conditions is as shown in Table 4.1.

Parameter	OFF State	ON State	Explanation
OOK Input	0	1.8V	The Digital Input
IN1	5uA	5uA	-
IN2	5uA	5uA	Due to the 1:1 mirror ratio between N1 and N2
IN3	0	40uA	Depends on if N4 is ON or OFF
IP1	5uA	45uA	-
IP2	75uA	675uA	-

Table 4.1: Current through the transistors in On & Off state

During the 1→0 transition it is important that the inductor core is discharged as quickly as possible. The NAND gate D6 ensures that the logic 1 is propagated to the gate of N8 with just one logic gate delay. This would allow both N7 and N8 to be turned ON at almost the same time and with minimal delay thus discharging the inductor core quickly. However, during the 0 →1 transition. The gates D3, D4, D5 and D6 introduce a delay between the turning off of N7 and N8 which is less than ¼ of the time period of one oscillation. This creates an imbalance in the VCO during startup which essentially kickstarts the oscillations.

4.5. Constant Gm Biasing Circuit

Constant Gm biasing is used to supply the biasing current for the oscillator. At room temperature, this is to be a 5uA current source. The complete diagram is shown in Figure 4.9.

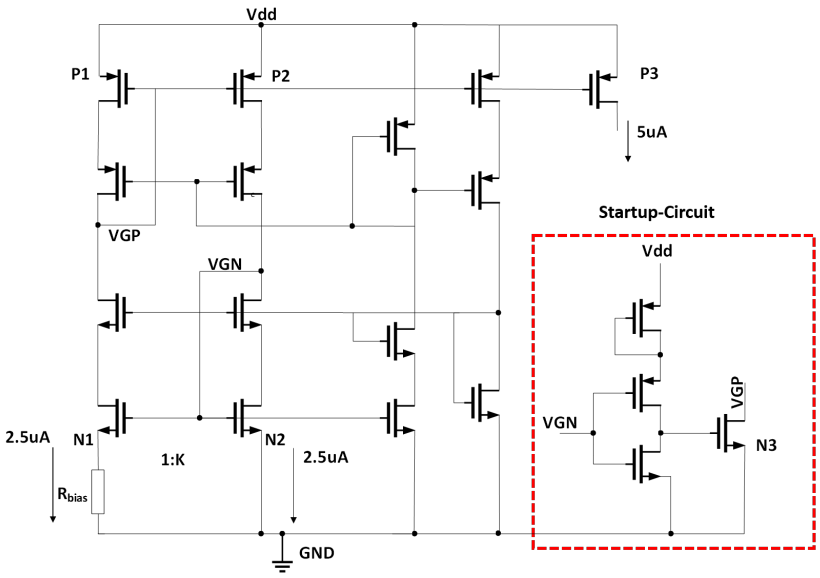


Figure 4.9: Constant Gm Biasing Circuit

The circuit is a beta multiplier that is designed to generate a constant Gm biasing source. If the currents through N1 and N2 are well matched, then the Gm of the

transistors depends only on R_{bias} and the relative sizing of N1 and N2 thereby making the biasing immune to PVT as long as the transistors are in saturation. The relation is shown in the Equation 4.10.

$$g_m = \frac{2}{R_{bias}} * (1 - \frac{1}{\sqrt{K}}) \tag{4.10}$$

Where K is the ratio of the sizing between N1 and N2, which in this case is a 1:4 ratio and R_{bias} is 2.4K. P1 drives a current of 2.5uA at nominal conditions. P1 and P3 have an aspect ratio of 1:2 which implies that P3 provides a current of 5uA by current mirroring.

It was also necessary to include a startup circuit [12]. The startup circuit consists of an inverter and a pull down transistor N3. The inverter tracks the voltage at node VGN and controls the V_{gs} of N3 .The transistor N3, working in triode region acts as a resistor and pulls the node VGP to GND which increases the V_{gs} of P1, essentially kick starting the positive feedback loop. This helps circumvent the undesirable state in which all the transistors are off as a result of the positive feedback around the circuit.

5

Receiver Design

5.1. Receiver Structure

The structure of the receiver can be seen in Figure 5.1 .

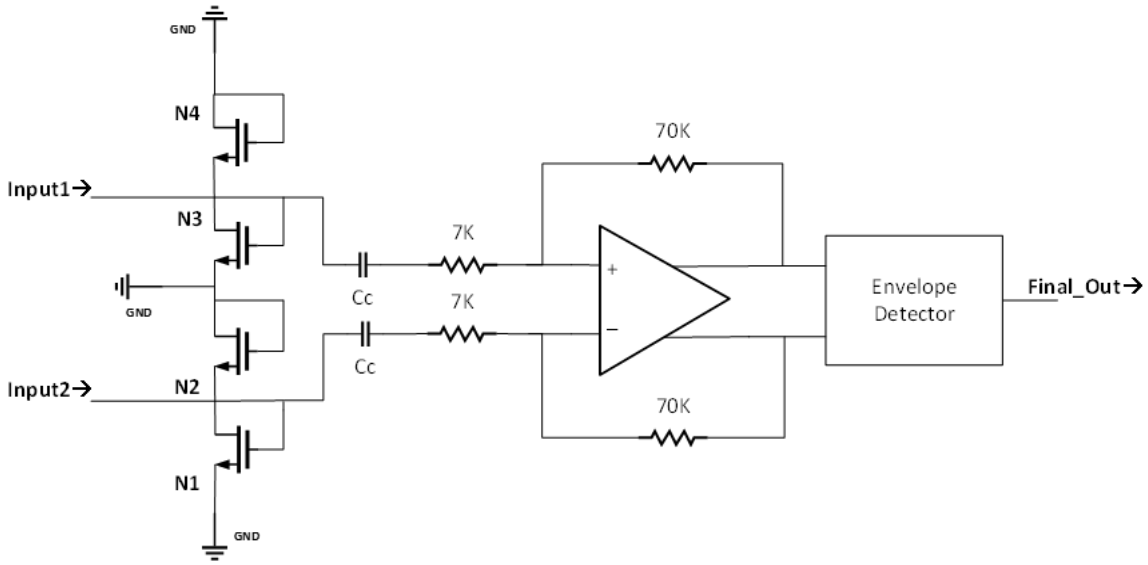


Figure 5.1: Receiver Structure

The inductor is connected across Inputs 1 and 2. Four diode connected transistors N_{1-4} connected in series sink large common mode transient currents during a CMTI event as shown in Section 3.2 . The clamping due to the diodes will also prevent common mode signals from becoming too large. This signal is then capacitively coupled to an amplifier with a gain of 10 and its output is passed on to the envelope detector which converts the signal back to the initial digital form.

5.2. Amplifier

For high CM immunity a fully differential structure is chosen for the amplifier. The carrier signal has a frequency centered at 360MHz. PVT and physical imperfections in the inductor coil post packaging can cause some frequency variation. A bandwidth

of 300MHz to 450MHz was taken to account for this. To ensure energy-efficiency and meet the power budget ,the current consumption is limited to 700uA. The specifications followed for the construction of the amplifier are shown in Table 5.1.

Specifications	**Target**
Current	<700uA
Closed Loop Gain	~20dB
Frequency of Operation	300MHz-450MHz
Output Load Equivalent	50fF
Expected Swing	1.8Vpp differential

Table 5.1: Amplifier Specifications

To maintain energy-efficiency, a pseudo class AB topology was chosen to attain the required 10x gain in the given bandwidth, Both the NMOS and PMOS are driven to achieve twice the g_m for the same current as shown in Figure 5.2. This has the added benefit of constraining the entire design into a single stage which saves a lot of area as well. The amplifier was also cascoded to increase the gain. In addition, a common-mode feedback circuit (CMFB) was established to maintain the output common-mode level. The closed-loop gain is achieved using a resistor feedback network as shown in Figure 5.1. The input was level shifted using a common source follower to drive the bottom NMOS, this signal was again level shifted by a capacitors C1 and C2 to drive the top PMOS pair [13]. The top PMOS was biased at a voltage of 1.2 volts (V_{bias}). The RC network formed by R1-C1 and R2-C2 would add a high pass cutoff and therefore their values had to be calculated such that the cutoff would be lower than the band of interest. The -3dB cutoff of the RC network was calculated at 15MHz using Equation 5.1.

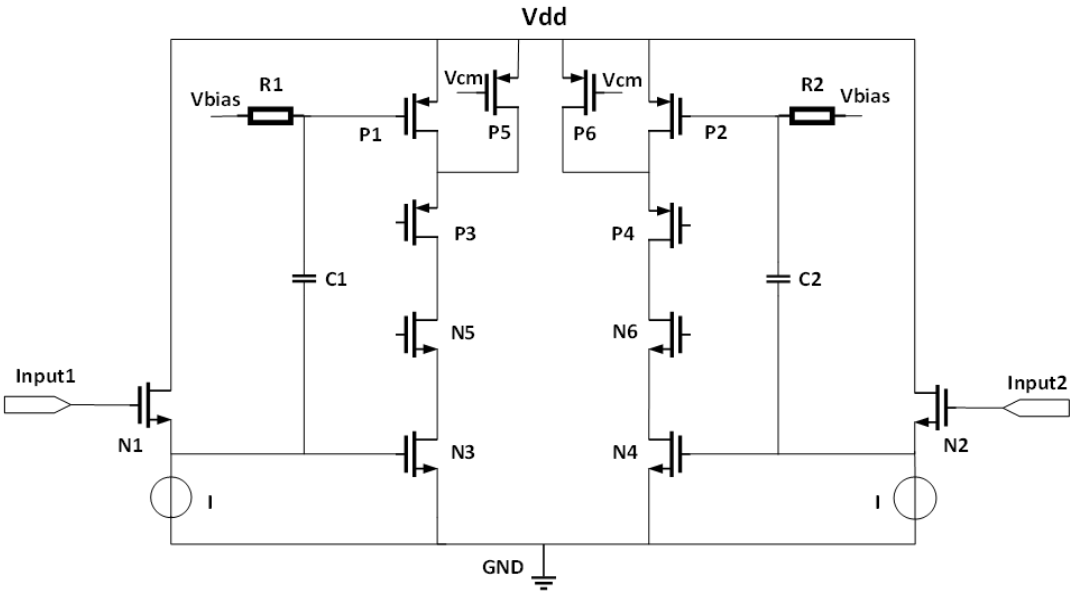
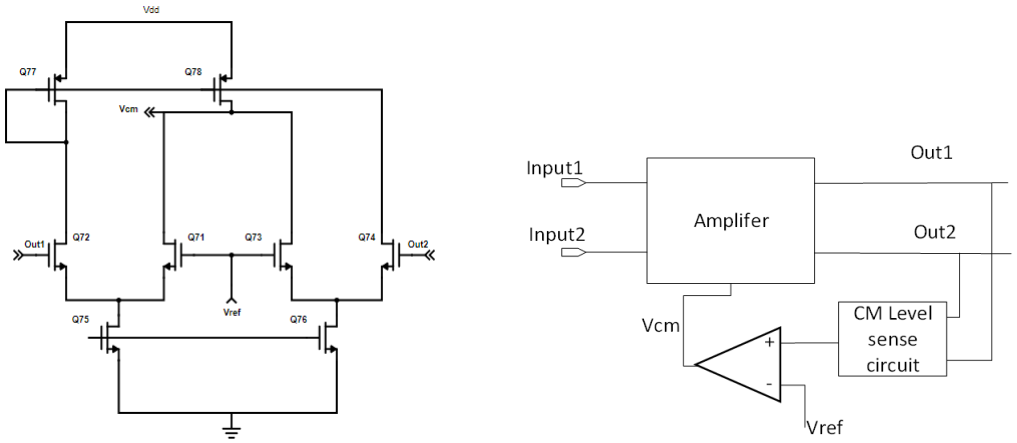


Figure 5.2: Amplifier Circuit



(a) Common-mode Feedback Circuit (b) Common-mode Feedback functionality

Figure 5.3: Common-mode Feedback

$$f_{cutoff} = \frac{1}{2 * \pi * R * C} \tag{5.1}$$

As shown in Table 5.1, a bandwidth of 450MHz was required. This means that a Unity Gain of 4.5GHz is required, assuming a 20dB per decade roll-off as shown in Equation 5.2.

$$UGBW = 4.5GHz \tag{5.2}$$

We can calculate the required transconductance for a particular UGBW using Equation 5.3.

$$g_m = 2 * \pi * C_L * UGBW \tag{5.3}$$

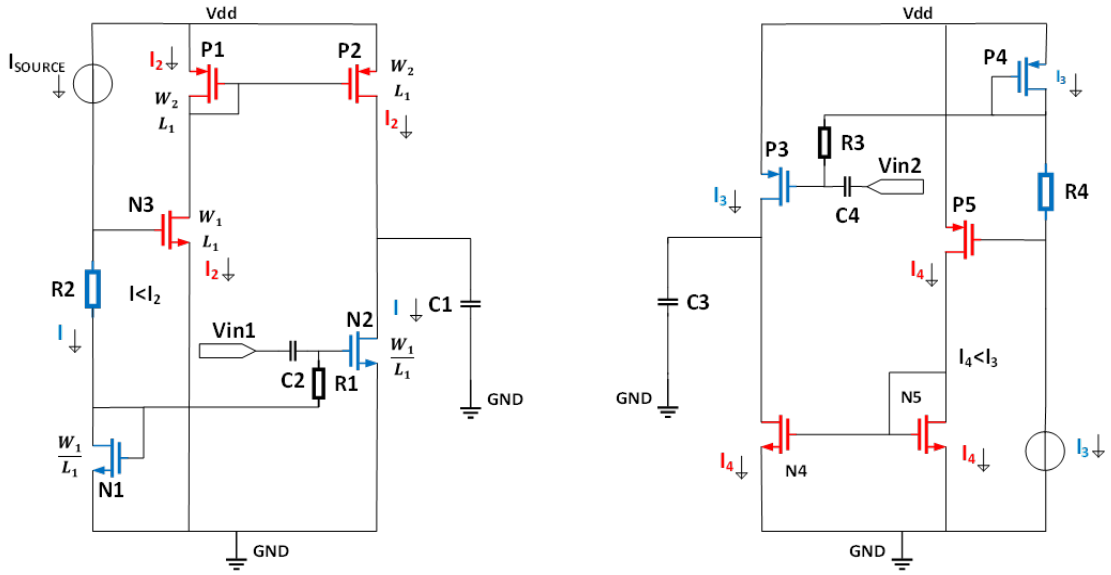
Once we know the required gm we can use that to calculate the current requirement by using equation 5.4.

$$I_d = \frac{g_m * V_{gt}}{2} \tag{5.4}$$

Once the value of the current is known then we can easily size the transistors.The common-mode feedback circuit shown in Figure 5.2 senses the output voltage , compares it with a reference voltage V_{ref} which has a nominal value of 900mV and then returns the error to the amplifier using transistors P5 and P6 (Figure 5.2), thus regulating the common-mode level of the amplifier.

5.3. Envelope Detector

The amplified signal has to be converted into its original digital format. In this design an envelope detector is employed for this purpose. The input modulation was such that every digital 1 at the input resulted in the oscillator being turned on and every 0 resulted in the oscillator turned off. Demodulation is done by detecting the envelope of the signals and then passing it through subsequent digital blocks. The analog part of the envelope detector is presented in Figure 5.4.



(a) NMOS referred Half-circuit of envelope detector

(b) PMOS referred Half-circuit of envelope detector

Figure 5.4: Envelope Detector Half Circuits

The working of the envelope detector can be better explained by using only the half circuit shown in Figure 5.4a. The aspect ratio of N1 and N2 are kept the same so that N2 mirrors the current I through N1. N3 (which also has the same aspect ratio) has a gate voltage that is $I * R2$ higher than that of N1 such that it drives a current I2>I. This current is mirrored to P2 via P1. The purpose of doing this is to ensure that P2 always has a higher drive strength than N2. This ensures that the voltage across C1 is always pulled high in normal operation when there is no input at Vin1 . The same principle can be applied to the PMOS referred half of the circuit as shown in Figure 5.4b. During normal operation the voltage across C3 is held low. When an oscillation presents itself at Vin1 and Vin2 this would discharge C1 and charge C2 respectively as shown in Figure 5.5. The waveforms from top to bottom are voltage across C3, amplifier output and voltage across C1. This would pass through a series of digital blocks as shown in the final circuit in Figure 5.6. The logic state of the digital gates during an oscillation at Vin1 and Vin2 are shown in green.

The addition of the half circuit in Figure 5.4b has the benefit of making the system immune to errors that may be caused due to common-mode noise. For instance as shown in Figure 5.7, a positive common mode spike at the gate of N2 would also cause overdrive voltage of N2 to increase and therefore the top plate of C1 would be discharged and pulled to ground. This is similar to the reaction that the system would have in the event of an oscillation. This false signal would then propagate to the output. However, such a positive common mode would not propagate through the PMOS referred side. A positive common mode would only reduce the overdrive voltage of P3. This means that the output of AND1 will remain at 0 and the erroneous value will not reach the output. Similarly negative common modes are also blocked by the NMOS referred side.

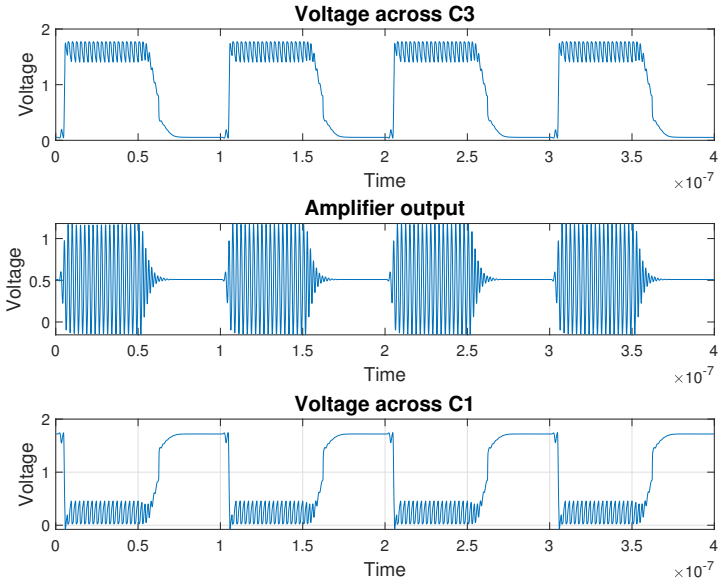


Figure 5.5: Envelope Detector Waveforms

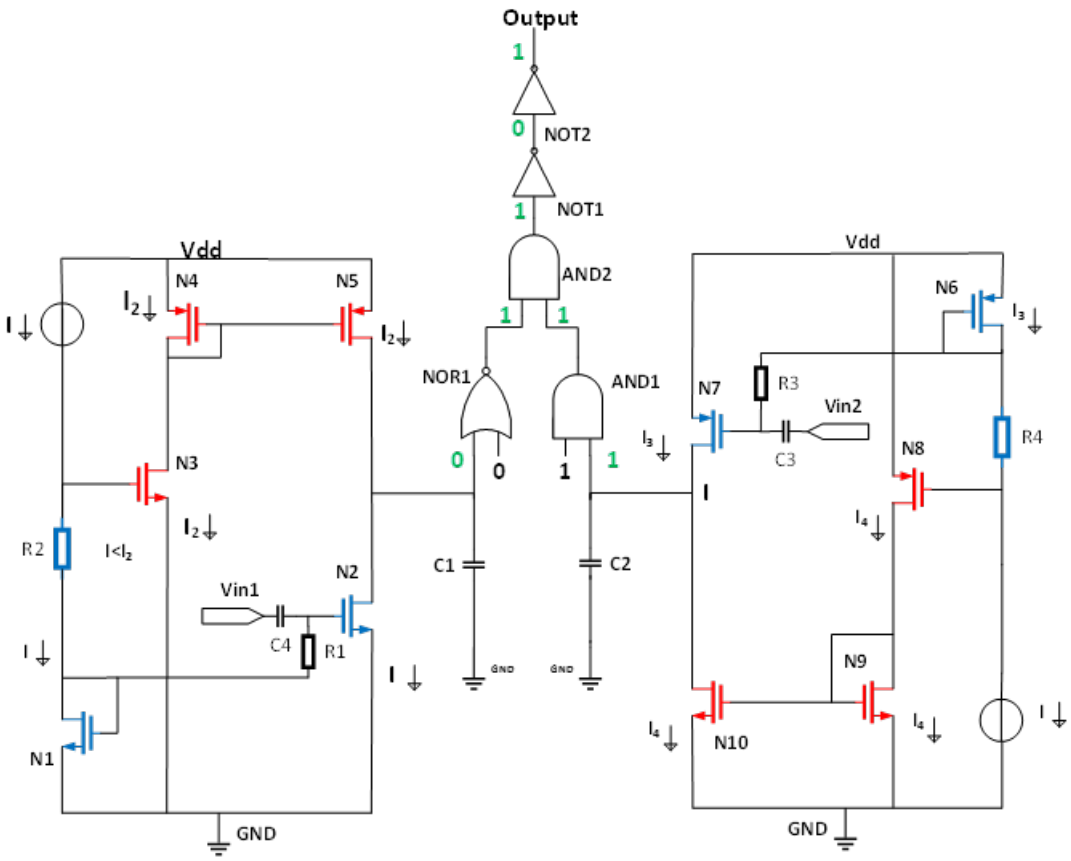


Figure 5.6: Envelope Detector Circuit during Oscillations

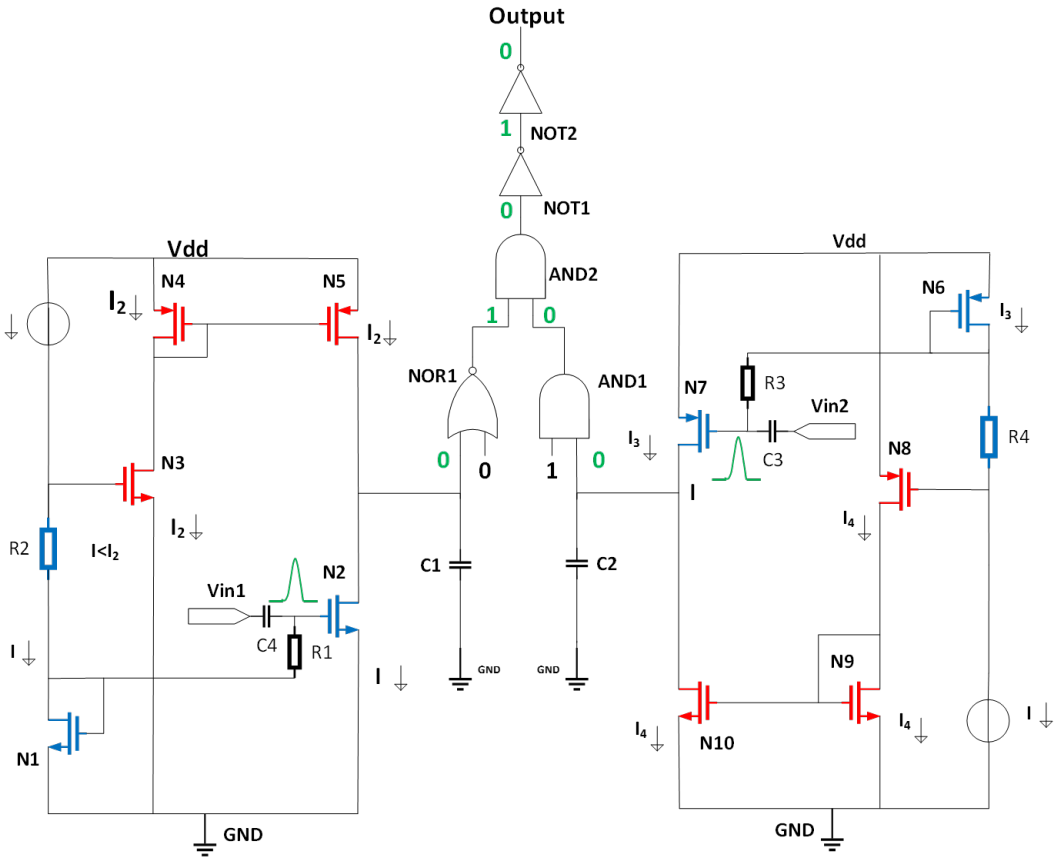


Figure 5.7: Envelope Detector Circuit during common-mode

6 Results

The results of the system are analyzed in this chapter. The transmitter and receiver side are individually analyzed and then the complete system results are presented.

This chapter also includes some actual measurements of the transmitter side. An early test vehicle to test the feasibility of the isolation layer was manufactured and tested. The thesis was at its nascent phase during this time and only the transmitter was designed. The receiver side used is from an earlier design model. The results of the measurements are included wherever applicable.

6.1. IC Block Diagram

The functional Block diagram of the IC is as shown in Figure 6.1.

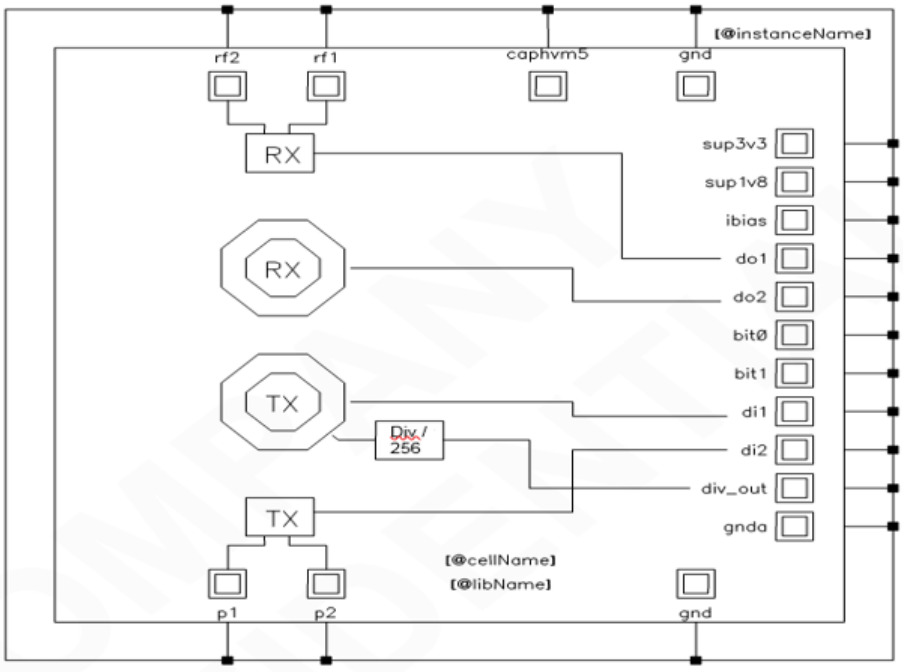


Figure 6.1: Block Diagram of IC

It includes one Transmitter (TX) and Receiver (RX) with their output and input connected to external pins to improve testability and one pair of transmitter and receiver placed in the center of an internal inductive coil. The functionality of each pin is as shown in Table 6.1.

Symbol	Description
rf1	RF receiver input 1
rf2	RF receiver input 2
p1	Transmitter output pin 1
p2	Transmitter output pin 2
GND	Ground (digital)
GNDA	Ground (Analog)
DIV_OUT	Divider Output (Transmitter Frequency/256)
di1, di2	OOK Input
bit1, bit0	Control bits of the capacitor bank
do1, do2	Digital output 1 and 2
i_bias	Bias current reference input
sup1v8	1.8V supply (both digital and analog)
sup3v3	3.3V supply

Table 6.1: Pin Description

6.2. Transmitter Results

6.2.1. Oscillator

One of the key aspects of the oscillator is about how fast it can start up its oscillations. This is the major delay contributor to the rising edge transition. This timing delay across corners and temperatures is shown in Figure 6.2.

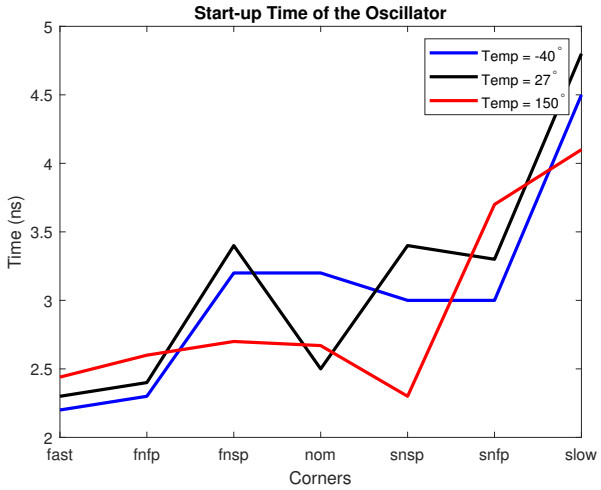


Figure 6.2: Time taken for the Oscillator to start Oscillating

Figure 6.2 shows a sub 5ns startup time for the oscillator. The overall system delay for the propagation of a 0→1 transition is less than 10ns. The spread of the R_{bias}

resistor in the constant Gm biasing circuit means that the slow corners will provide lesser current to the oscillator core which makes it the slowest corner. Consequently, this also makes the fast corner the fastest. The resonant frequency of the oscillator was also measured across 3 sample IC's and are shown in Table 6.2. The simulated frequency post-layout was 0.39MHz.

Sample	Frequency
A	403MHz
B	396MHz
C	408MHz

Table 6.2: Measured Resonant Frequency

6.2.2. Capacitive Bank

The capacitive bank is programmed with 2 bits and therefore has four tunable frequencies. The simulated frequencies are shown in Table 6.3.

Bit_1	Bit_0	Frequency Simulated	Frequency Measured
0	0	390MHz	408MHz
0	1	379MHz	393MHz
1	0	368MHz	381MHz
1	1	353MHz	372MHz

Table 6.3: Tunable Frequencies of the Capacitor Bank

6.2.3. Current Consumption

The transmitter has two states of operation. When OOK=0, and when OOK=1. The nominal currents during each state of operation are shown below in Table 6.4.

Transmitter Parts	Idle (uA)	Active (uA)
Oscillator (main)	75	675
Oscillator (dummy)	10	90
All Biasing circuits	25	75
Total	110	840

Table 6.4: Current Consumption of Transmitter

6.3. Receiver Results

6.3.1. Amplifier

The loop-gain of the amplifier along with the phase graph is as shown in Figure 6.3. The amplifier has a phase margin of 57 degrees and a UGBW of 580MHz.

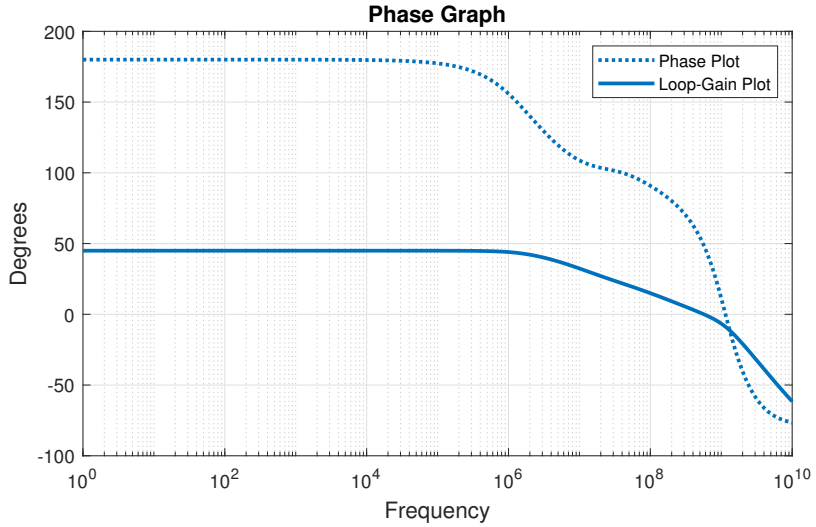


Figure 6.3: Amplifier Closed-Loop Gain over Corners and Temperatures

The closed-loop gain of the amplifier must maintain a high enough value such that the subsequent envelope detector stage can ensure a fast detection. The spread of the closed-loop gain of the amplifier across corners and temperatures are shown in Figure 6.4.

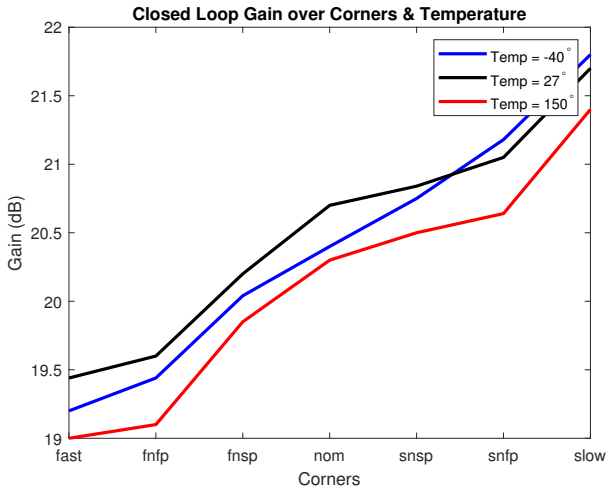


Figure 6.4: Amplifier Closed-Loop Gain over Corners and Temperatures

6.4. Receiver Sensitivity

It is possible for noise to couple into the receiver coil from external sources. This could also corrupt the data. Figure 6.5 shows the minimum signal amplitude that is required at the receiver input for it to propagate to the output.

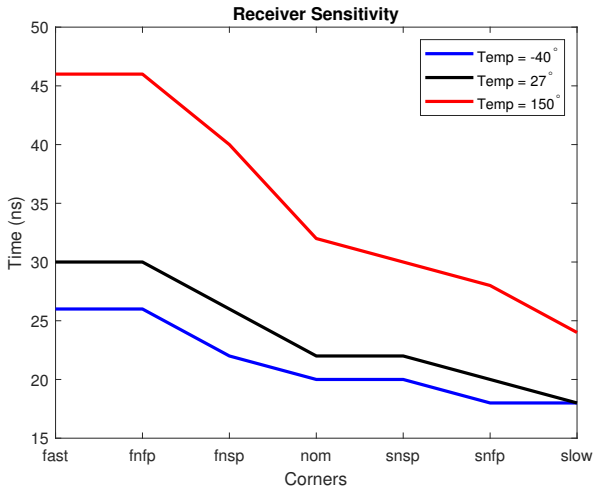


Figure 6.5: Sensitivity Of the Receiver Input to Differential Signal

The minimum required amplitude to trigger the receiver is a consequence of the way the envelope detector is designed as described in Section 5.3. The difference in the driving strength of the two output MOSFETs ensures that a minimum amplitude is required before a signal can be seen at the output. This minimum level can be further increased by increasing the value of R2 and R4 in Figure 5.4.

6.4.1. Current Consumption

The current consumption for each block of the receiver during nominal operation is shown in Table 6.5.

Receiver Parts	Current (uA)
Amplifier	680
Envelope Detector	100
Total	780

Table 6.5: Receiver Current Consumption

6.5. System Results

Three parameters are considered the most crucial for the system. They are the CMTI, power consumption and the data rate. Each of those three main points will be the focus of this section.

6.5.1. Common Mode Transient Immunity

The common-mode transient immunity is a very important parameter when it comes to digital isolators. A high CMTI prevents the corruption of the data during the occurrence of dangerous ground loops. However, only the transients that occur on the transmitter ground can corrupt data. Therefore there are two possible scenarios, and the CMTI rating for each of them are :

- when OOK=1 and the transient occurs at the transmitter ground: CMTI →100kV/us

- when OOK=0 and the transient occurs at the transmitter ground: CMTI →200kV/us

6.5.2. Data Rate

The delay in the propagation of digital data to the output determines the final data rate. The first simulation was run with a nominal value of attenuation across the channel which is a factor of 10. In this case, the delay experienced by the rising edge (0 →1) and the falling edge (1 →0) are simulated across corners and temperatures (Figure 6.6).

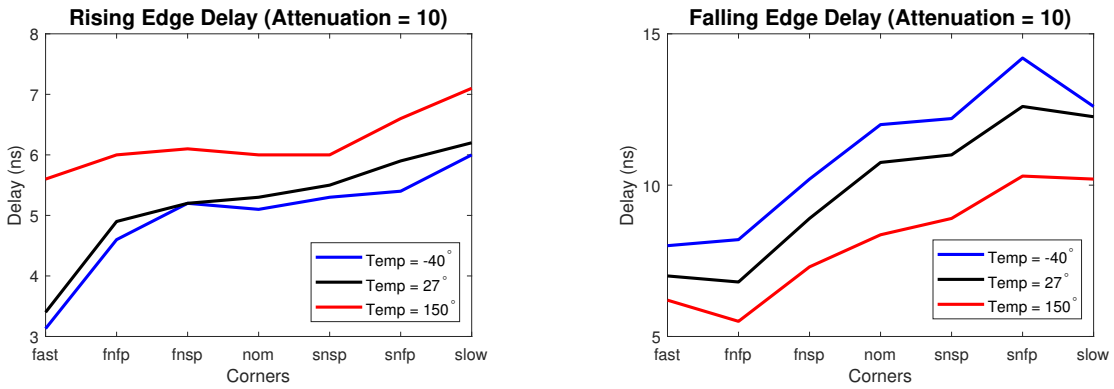


Figure 6.6: Delay of signals when isolation offers an attenuation factor of 10

However, it is completely possible that the attenuation across the channel could be far more in case of issues with the alignment of the coils, imperfections in the coil geometry, variation in distance between coils, etc. So a worst-case attenuation factor of 15 was taken and the measurements were taken across corners and temperatures as shown in Figure 6.7

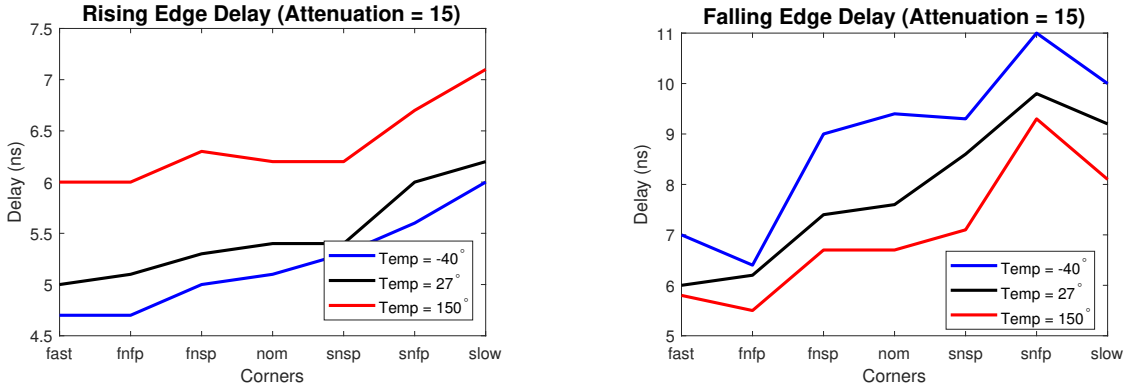


Figure 6.7: Delay Of signals when isolation offers an attenuation factor of 15

6.6. Final Results

Table 6.6 shows the final specifications achieved after simulations. They are compared against the initial values anticipated for the design.

Specifications	Target	Simulated
Supply Voltage	1.8V	1.8V
Power Consumption (Transmitter)	<1mA	980uA
Power Consumption (Receiver)	<1mA	930uA
Propagation Delay	<15ns	14.2ns
Common Mode Transient Immunity (CMTI)	100kV/us	100kV/us

Table 6.6: Final Specifications achieved

7

Conclusion and Future Works

7.1. Conclusion

This thesis presents an on-chip inductor based digital isolator system. It is designed in 160nm technology. The system is designed from a top-down design approach where the variables of the system are designed to meet the specifications for the application. It also offers several convincing solutions in overcoming the limitations of conventional digital isolators. Exhaustive simulations meet the specifications as well as confirm the solutions explored.

One of the salient features of the project is its CMTI specification. The design proves its ability to function even during the occurrence of really fast and large transient ground loops as high as 100kV/us. The power consumption is also considerably less at 2mA per channel in comparison to other state of the art work.

7.2. Future Work

The future work would involve validating the design and the simulated specifications on-chip. Ideally a structure consisting of two transmitter-receiver pairs should be tested such that bidirectional communication can be established and tested.

In addition, there are three possible approaches of achieving isolation that are currently being considered for testing. They are as listed below:

- **Stacked Die Approach**: This thesis is based on the stacked die approach where the die with the receiver and its coil is stacked above the die containing the transmitter and its coil. This is separated by an isolation material as shown in Figure 7.1. However, this method may prove to be challenging with regard to coil alignment. Also, the substrate of Die 2 will have to be a high ohmic substrate.

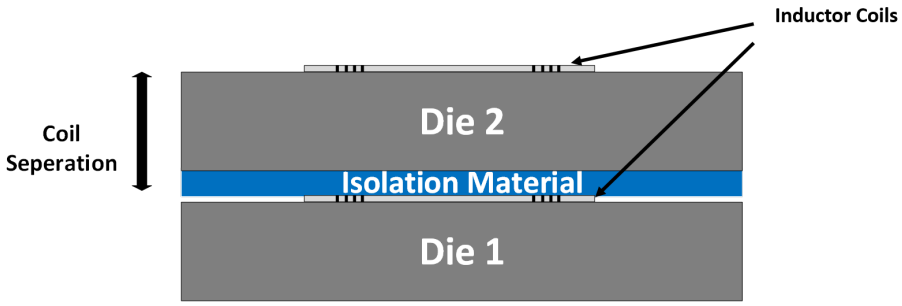


Figure 7.1: Stacked Die

- **Re-distribution Layer Approach (RDL)**: The second method being considered is the RDL approach as shown in Figure 7.2. It consists of Die 1 containing the transmitter and its coil upon which there is a thin isolation layer of polymide on which a subsequent coil is placed. The receiver has a similar structure and the two are connected via bond wires. The combined thickness of both the polymide layers offers the total isolation thickness. This method is a low-cost approach.

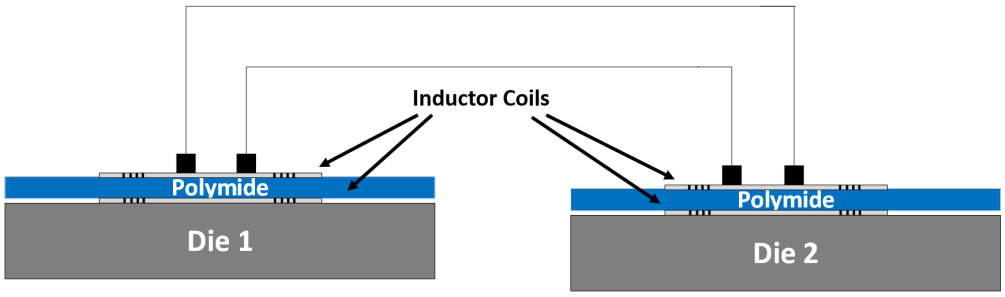


Figure 7.2: RDL Approach

- **Mini-PCB Approach**: The third approach involves testing the system with an intermediate mini PCB on which both the transmitter and receiver coil would be fabricated as shown in Figure 7.3. This method has the advantage of having reliable isolation but it will increase assembly complexity.

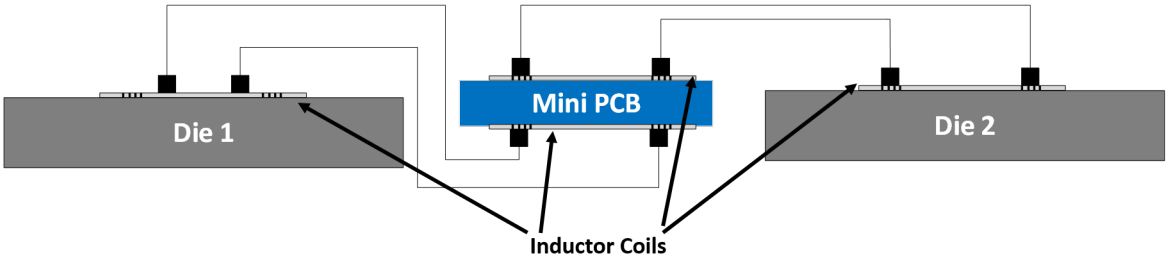


Figure 7.3: Mini-PCB Approach

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