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Dumitru, Florin-Silviu ; Cucu-Laurenciu, Nicoleta; Matei, Alexandru ; Enachescu, Marius

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Florin-Silviu Dumitru, Nicoleta Cucu-Laurenciu, *Member, IEEE*, Alexandru Matei, and Marius Enachescu, *Member, IEEE*

***Abstract*—McCulloch-Pitts neuron structures are comprised of a number of synaptic inputs and a decision element, called soma. In this paper, we propose a 5-bit Graphene Nanoribbon (GNR)-based DAC to fulfill the role of the summation element featuring programmable input weights. The proposed GNR-based 5-bit DAC relies on: (i) GNR unit current cells and (ii) a GNR logic thermometric decoding block. Our implementation is based on mapping the GNR structure's conductance using Matlab and performing the required SPICE analysis using the Matlab based GNR Verilog-A model. The unit current cell geometry and bias conditions were chosen based on the unit cell's conductance map from which we derived its I_{ON}/I_{OFF} ratio, as well as transfer and output characteristics, resembling the classical MOSFET counterpart. By utilizing GNR devices instead of FinFET counterparts, a reduction of the active area of the 5-bit current DAC by up to a factor of three can be achieved. Furthermore, the GNR implementation achieved this while maintaining comparable INL and DNL performance to that of the FinFET variant, i.e., DNL of [−0.196, 0.088] LSB and INL of [−0.809, 0.364] LSB for the proposed GNR 5-bit DAC while operating at a supply voltage of only 0.2 V.**

***Index Terms*—Carbon-nanoelectronics, DAC, graphene, McC ulloch-pitts, nanoribbons, neurons.**

I. Introduction

CMOS technology is nowadays tailored to building nano electronics systems. Within the Internet of Things (IoT) context, the main characteristics of such battery powered systems is low power consumption coupled with high frequency operation. At this time, MOSFETs reach atomic dimensions, their static power consumption dominates the total power consumption, their reliability gets degraded, while production costs increase exponentially. There are two different avenues one could take to achieve progress: (i) building emerging devices using CMOS technology platform, like NEMFET [1], and (ii) leveraging new materials, e.g., graphene (Graphene Nanoribbons - GNR) [2].

Past work in [2] compared GNRs-based logic gates (GNR-L) with 7 nm FinFET CMOS counterparts and proved via simulation results that GNR-L have the potential to achieve 2 orders of magnitude lower power consumption, 6x smaller propagation delay, and 2 orders of magnitude smaller active area footprint. Hence, these results open the premises for building an extreme low power, high speed, low cost McCulloch-Pitts neuron [3] to be used in neural network applications. However, multiple aspects still need to be taken into consideration when building GNR-based McCulloch-Pitts neurons, mainly, the matter of modulating nanoribbon conductivity for the decision element (soma) the matter of programming the input synaptic weights.

In this paper, the focus will be to generate analog functions from GNR structures that have digital inputs, hence building the programmable input weights by means of a current 5-bit GNR-based digital to analog converter (DAC). In order to do that, we will design, simulate, and develop basic current sources by modulating nanoribbon conductivity through topology, dimensions, and external top/back gates.

The proposed GNR-based 5-bit DAC relies on: (i) GNR unit current cells and (ii) a GNR logic thermometric decoding block. The unit current cell geometry and bias conditions were chosen based on the unit cell's conductance map from which we derive its I_{ON}/I_{OFF} ratio of $24.3\times$, as well as transfer and output characteristics, resembling the classical MOSFET counterpart. Our implementation is based on mapping the GNR structure's conductance using Matlab and performing the required SPICE analysis using the Matlab based GNR Verilog-A model [4]–[6]. To gain insight into the potential of our proposal, we evaluate the DAC linearity through differential nonlinearity error (DNL) and integral nonlinearity error (INL) parameters. Our results indicate a DNL of $[-0.196, 0.088]$ and an INL of $[-0.809, 0.364]$ errors, clearly meeting the requirements of true 5-bit resolution, while operating at supply voltage of only 0.2 V. To provide context for our analysis, we implemented and evaluted in matching bias conditions a FinFET-based DAC. When compared with the GNR-based DAC implementation, the 7nm FinFET-based DAC resulted in comparable INL and DNL results while a reduction of the active area by up to a factor of three can be achieved.

The rest of this paper has the following structure: Section II presents an overview of related work on graphene, GNR conductance computation, GNR simulation methodology, logic circuits using GNRs, and a way of implementing GNR-based

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Florin-Silviu Dumitru, Alexandru Matei, and Marius Enachescu are with the Department Electronic Devices, Circuits, and Architectures, Faculty of Electronics, Telecommunications, and Information Technology, "POLITEHNICA" University of Bucharest, 343058 Bucuresti, Bucharest, Romania (e-mail: florin.dumitru2610@stud.etti.upb.ro; alexandru.matei0601@stud.etti.upb.ro; m.enachescu@upb.ro).

Nicoleta Cucu-Laurenciu is with the Department of Quantum and Computer Engineering, Faculty of Electrical Engineering, Mathematics, and Computer Science, Delft University of Technology, CD 2628 Delft, The Netherlands (e-mail: N.CucuLaurenciu@tudelft.nl).

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programmable synaptic weights. Section III describes the GNR-based unit current cell geometry, electrical characteristics, its performance and the proposed DAC. Section IV presents the results of our simulations for the GNR and FinFET 5-bit DACs and compares their performance. Finally, the paper ends with some concluding remarks in Section V.

II. Background

In this section, we present the main idea behind how to use DACs for implementing programmable synaptic weights, then we describe the fundamental generic graphene-based device, and finally we provide an overview of the utilized graphene circuit simulation framework.

A. DAC-Based Programmable Synaptic Weights

Artificial neurons and synapses are main ubiquitous components of neural networks, which serve as fundamental processing units and as communication junctions between neurons, respectively. A fundamental operation performed by neurons regardless of their type (e.g., linear or nonlinear neurons) is the weighted sum operation, i.e., a neuron's output y can be expressed as linear combination of the neuron's inputs x_i, with weights given by the input-to-output synaptic connections strength w_i, $y = f(\sum x_i \cdot w_i)$. Subsequently, we focus on the synaptic weights circuit realization.

Synaptic weights are typically varying quantities, and thus the ability to set and change their values is essential for a synaptic circuit. To implement programmable synaptic weights, we employ Digital to Analog Converter (DAC) circuits which are mapping digitally encoded weights values into an analog current. In particular, a thermometric DAC implementation was chosen as it guarantees a monotonic output and provides superior differential non-linearity (DNL) characteristics, when compared to their binary weighted counterparts for instance [7]. This enables the implementation of synaptic weight values with high precision, which is beneficial for the neural network functionality. Figure 1 schematically illustrates the programmable synaptic weight circuit which uses a thermometric DAC to convert a desired binary synaptic weight value $w_i = B_0 \ldots B_{N-1}$ to an analog current I_{out}. A binary to thermometric decoder is used to convert the weight value $B_0 \ldots B_{N-1}$ to a thermometric code $D_0 \ldots D_{2^N-2}$ which is further used to control the individual "ON"-"OFF" switching of $2^N - 1$ current sources. The sum of the currents through the "ON" state sources yields the output current I_{out} which corresponds to the given weight value.

To implement the DAC-based programmable synaptic weights using graphene, we rely on the basic structure illustrated in Figure 2. The device consists of a monolayer Graphene Nanoribbon (GNR) that behaves as conductive channel when subjected to a V_{ds} voltage between the drain and source contacts. The GNR conductance can be modulated through external voltages applied on the top and back gate contacts (V_g and V_{bg}) as well as by modifying the GNR's geometry via altering the parameters illustrated in Figure 3. Specifically, the geometrical parameters include the total GNR width W, the GNR length L, the constriction width W_c and length L_c, the bump width W_b and length L_b, the width of the top gate contacts $WV_{g1,2}$, and the distance between the top gate contacts and the source/drain terminals $PV_{g1,2}$.

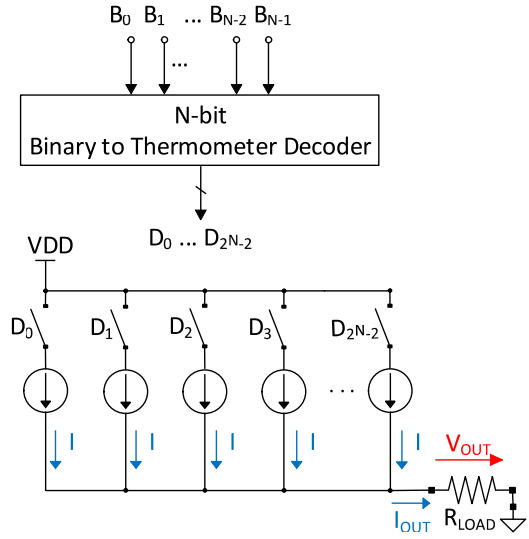

Fig. 1. DAC-based Programmable Synaptic Weight.

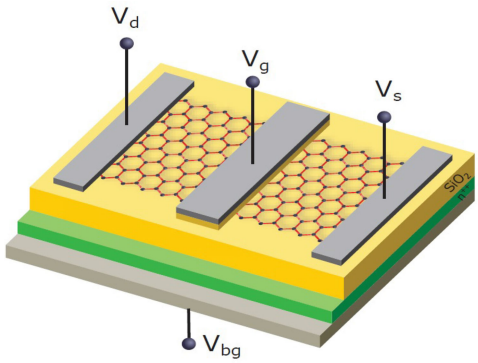

Fig. 2. GNR-based Fundamental Device.

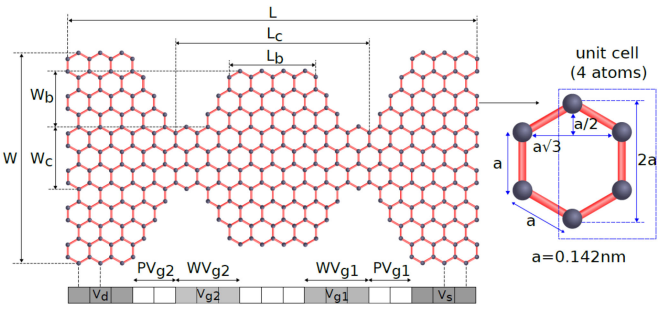

Fig. 3. GNR Geometry Description Parameters [2].

This GNR fundamental device has been demonstrated to provide a varying set of functionalities, among which Boolean operations. To perform a specific functionality, a GNR device instance that is specifically customized (in terms of GNR geometry) for that functionality, is employed [8].

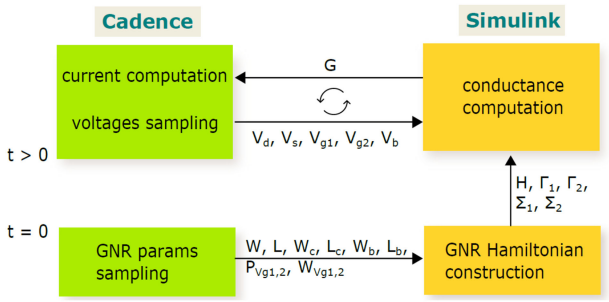

Fig. 4. Cadence Spectre - Matlab Simulink GNR Simulation Flow [9].

B. Simulation Framework

The evaluation of the GNR-based programmable synaptic weight circuit is done by means of utilizing a mixed-signal Cadence Spectre - Matlab Simulink simulation. The co-simulation approach enables us to perform SPICE circuit-level simulations while retaining the accuracy of atomistic-level simulations in Matlab. In Cadence, each GNR is modeled using a Verilog-A model which takes into account the geometrical parameters described in Figure 3, with an interface comprised of 5 input pins (source, drain, 2 top gates and 1 back gate) and one output pin (the GNR conductance).

The inter-communication between Cadence Spectre and Matlab Simulink is illustrated schematically in Figure 4. For every transient simulation time step Cadence gives as input to the Verilog-A model a set of voltages (the GNR source, drain, top/back gate voltages). The Verilog-A model then internally triggers a Simulink model which computes the GNR conductance for the current transient simulation time step. Once the conductance value is returned to the Verilog-A model, the current through the GNR is derived using the relation [9]:

$$I(d,s) = V(d,s) \cdot G. \tag{1}$$

In order to compute the GNR electronic transport properties, we employ the tight-binding Hamiltonian to describe the GNR system, the Non-Equilibrium Green Function (NEGF) quantum transport model for solving the Schrödinger equation and the Landauer formalism to obtain the GNR current and conductance [10]. Specifically, the GNR conductance can be accurately computed as:

$$G = \frac{q \cdot \int_{-\infty}^{+\infty} T(E) \cdot (f_0(E-\mu_1) - f_0(E-\mu_2))dE}{h \cdot (V_d - V_s)}, \tag{2}$$

where q is the electron charge, h is the Planck constant, T(E) is the transmission function which models the probability of transmission of one electron from source to drain, f_0(E) is the Fermi-Dirac distribution function at temperature T, and $\mu_{1,2}$ denotes the Fermi energy of the source and drain contacts.

III. GNR-Based DAC for Programmable Synaptic Weights

In this section we present the proposed graphene-based DAC circuit, and describe its principle of operation.

A thermometric current DAC consists of $2^N - 1$ unit current cells where N is the number of bits encoding the DAC input. Besides the current cells, in order to implement a thermometric DAC, a binary to thermometer decoder is also required. Although not implemented in this paper, GNR-based Boolean logic gates have already been proven [2], hence allowing for the decoder implementation. Subsequently, we focus on GNR-based current cell circuit, as key DAC component. A current cell is a current source which is typically constructed in CMOS technology using either an nMOS or a pMOS transistor, depending on whether the current source is connected to the power supply (source) or to the ground (sink).

The current cell performance is limited by several factors which need to be taken into consideration during the design process, including: (i) the variation of the output current, which ideally is independent of the voltage supply, temperature and load resistance, (ii) the output resistance of the current source which is ideally infinite, and (iii) the output voltage swing which should be maximized by design. Another aspect is that, while traditional CMOS analog design leverages the MOSFET square-law device equation for the initial hand calculations, working with graphene structures requires a different design approach.

To design the graphene-based DAC current source circuit, we consider the fundamental GNR device described in Section II-A, and perform a Design Space Exploration (DSE) with respect to the GNR geometry, contacts topology and biasing conditions. The DSE process culminates with the identification of a GNR device instance featuring high output resistance and I_{ON}/I_{OFF} ratio. From the functionality point of view, the GNR-based current cell is designed such that its electrical behavior resembles that of its CMOS transistor-based current cell counterpart.

Figure 5(b) depicts the proposed GNR current source with its equivalent electrical circuit shown in Figure 5(a). The GNR device drain terminal is connected to the supply voltage $V_{DD} = 0.2$ V, while the source terminal carries the source current I. The GNR device has two top gates which are connected together and through which the GNR current source receives the "ON"/"OFF" activation signal, and a back gate which is connected to a fixed bias voltage $V_{bg} = 0.3$ V. Figure 5(c) illustrates the GNR topology we identified for the proposed current cell by means of the atomistic-level DSE, with dimensions represented in terms of the distance between adjacent carbon atoms $a = 0.142$ nm. The geometry of the GNR is defined using width, W = 41a, length, L = $27\sqrt{3}$a, constriction width, W_C = 7a, constriction length, $L_C = 4\sqrt{3}$a, widths of the two top gates, $W_{Vg1,2} = 6\sqrt{3}$a, widths of the source and drain contacts, $V_D = V_S = 3\sqrt{3}$a, and distance from the drain or source contacts to the neighboring gate, $PV_{g1,2} = 2\sqrt{3}$a.

To provide a better view on the relationship between the determined GNR topology and the current source circuit behavior, we illustrate in Figure 6(a) the conductance map of the GNR structure. To this end, we set $V_{DD} = 0.2$ V, the source terminal to ground, the back gate voltage $V_{bg} = 0.3$ V, and vary the V_{g1} and V_{g2} gate voltages from 0 V to 0.2 V. We then compute the GNR conductance G. One can observe in Figure 6(a) that

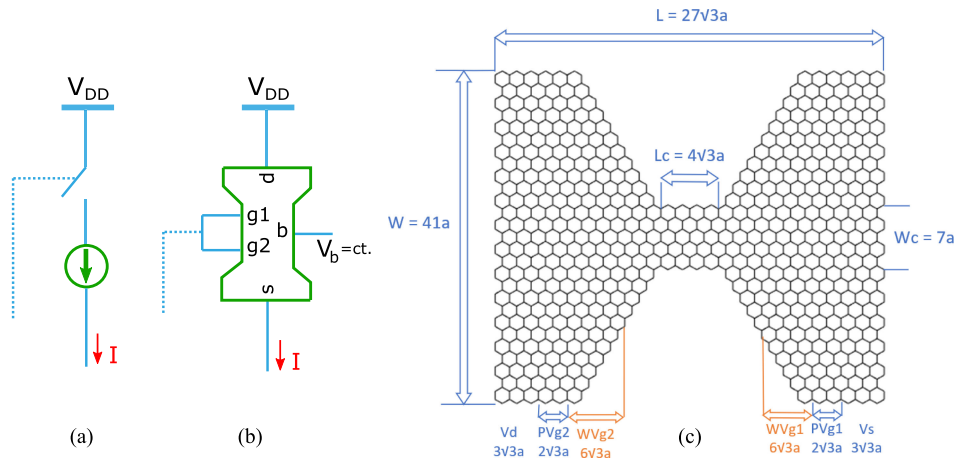

Fig. 5. Graphene-based Current Source Cell: a) Equivalent Electrical Circuit, b) GNR Current Source Circuit, c) GNR Geometry.

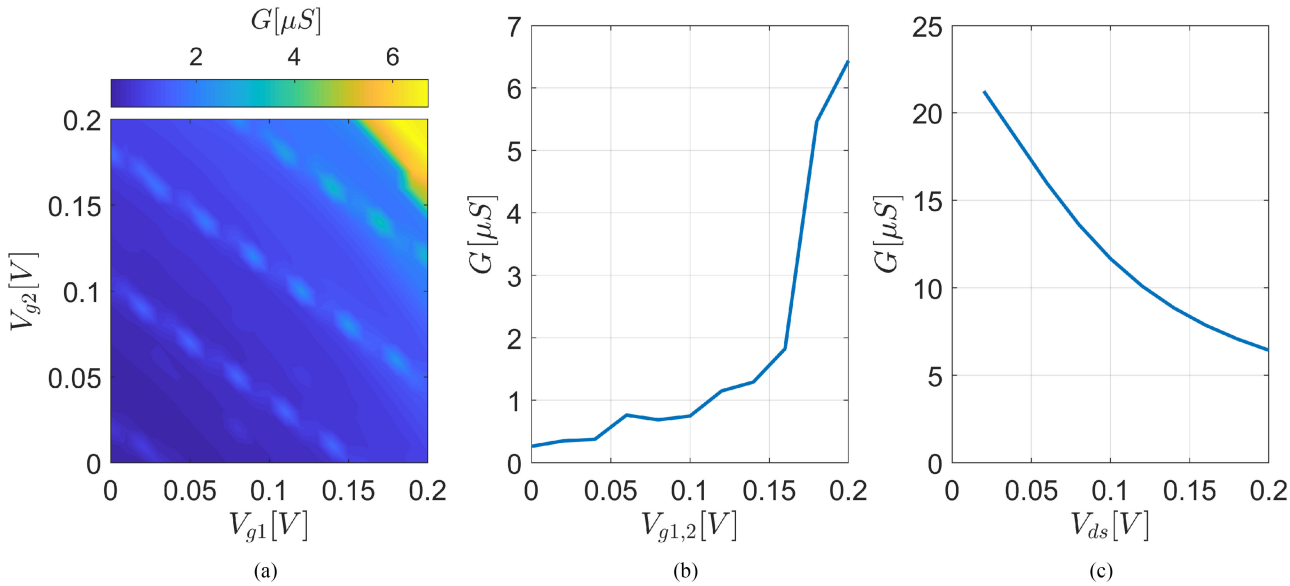

Fig. 6. Graphene Current Source Electrical Characteristics: a) Conductance Map, b) Conductance Transfer Characteristic, and c) Conductance Output Characteristic.

(i) when $V_{g1} = V_{g2} = 0.2$ V, the GNR has a high conductance value which corresponds to an activated "ON" current source, and (ii) when $V_{g1} = V_{g2} = 0$ V, the GNR has a low conductance value which corresponds to an inactive "OFF" current source.

From Figure 6(a) we remark that an effective means of controlling the transconductance of the proposed GNR may be attained by driving both V_{g1} and V_{g2} using the same gate voltage. As shown in Figure 6(b), this would enable the GNR to exhibit the variation of the G seen on the diagonal which passes through the origin. Using this approach we are able to achieve a transconductance variation of $24.3\times$ between $V_{g1,2} = 0$ V and $V_{g1,2} = 2$ V.

The output transconductance characteristic used to evaluate the GNR in the role of analog current source is presented in Figure 6(c). Here, the $V_{g1,g2}$ voltage is set to 0.2 V and V_{ds} is swept from 0 V to 0.2 V. As illustrated, increasing the V_{ds} leads to a decrease of the GNR's G which translates into an increasing output resistance. This behavior begins to diminish at a V_{ds} of approximately 0.1 V as the GNR's transconductance converges towards $G = 6$ μS and reveals similarities to the linear and saturation regions of its CMOS counterpart.

To get a better insight into the GNR device's electrical behavior, specifically when fulfilling the role of a current source, a Matlab simulation was run to map the variation of the I_{ds} current as a function of both the V_{ds} and $V_{g1,2}$ voltages. The resulting characteristic, depicted in Figure 7, shows that above a V_{ds} of 100 mV, the I_{ds} current enters a plateau-like region featuring a 9% variation of the I_{ds} current across the 100 mV to 200 mV V_{ds} range which resembles the CMOS device saturation region. Additionally, we remark that the $24.3\times$ variation of the I_{ds} current vs. $V_{g1,2}$ not only allows us to achieve the clear ON and OFF states necessary for toggling the DAC unit current source GNR device, but also opens up the possibility of implementing simple analog structures owing to the monotonic characteristic of I_{ds} at larger $V_{g1,2}$ values. Having identified the key characteristics of a CMOS current source, we have confirmed that the proposed

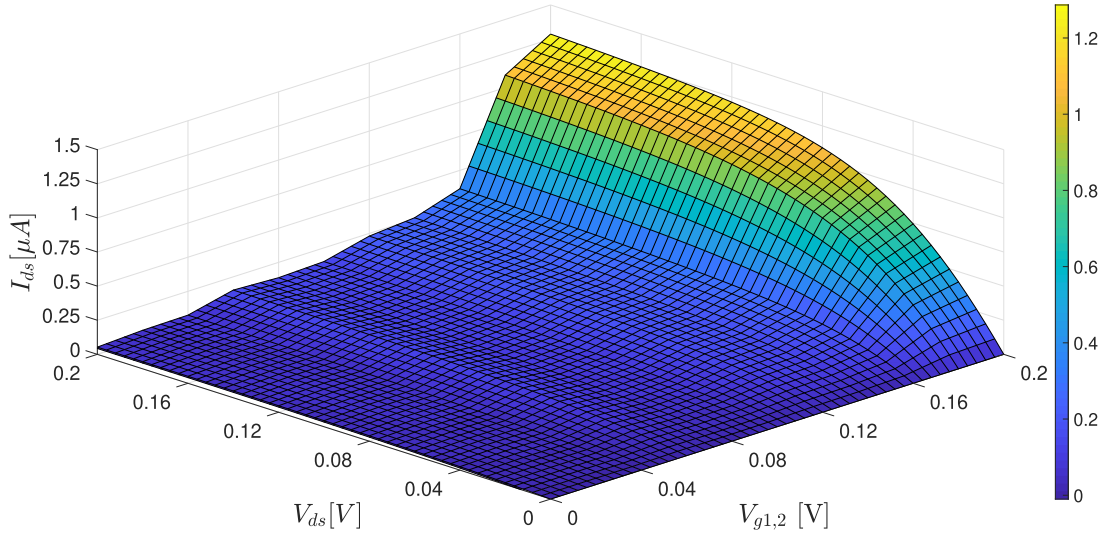

Fig. 7. GNR device I_{ds} Current Mapping as a Function of V_{ds} and $V_g 1, 2$.

GNR device may be used to fulfill the role of current source for the proposed DAC implementation.

To implement the GNR-based DAC, we adapted the topology shown in Figure 1 for 5-bit resolution. We used 31 current cells as the DAC's analog array. The current cell gates are individually driven by the GNR-based thermometric decoder's output. The entire circuit operates at a supply voltage of $V_{DD} = 0.2$ V and the DAC's output current drives a load resistor $R_{LOAD} = 2.764\,\mathrm{k}\Omega$, thus generating the DAC output voltage.

IV. Simulation Results

In this section we compare the proposed GNR-based 5-bit thermometric current DAC against the same topology implemented using a 7 nm FinFET technology [11], with respect to relevant metrics for DACs, i.e., DNL, INL, and footprint. The 7 nm FinFET technology was chosen as it provides the smallest feature size available and thus the most competitive active area to compare against.

A. Simulation Methodology

Given that in the GNR DAC's case (i) we are deprived of a compact SPICE model because of the high computational complexity involved in the GNR conductance derivation, and (ii) our final objective is that of running neural network scale simulations, we were required to identify a time effective, yet accurate, simulation strategy for our GNR based circuits. Initially we ran Cadence Spectre - Matlab Simulink cosimulations allowing Spectre to make calls to the Matlab engine to compute the GNR conductance for each transient operating point. Subsequently, we mapped the GNR device's conductance fine-grained mesh, as illustrated in Figure 7 (where G is derived using 1), into an extensive look up table for our GNR's Verilog-A model. This concentrated the GNR specific portion of the computational effort into the Matlab conductance look up table mapping phase and reduced all subsequent GNR DAC level Cadence simulation times, when compared with the Spectre - Matlab cosimulations.

The FinFET DAC was simulated using the 7 nm predictive technology model from [12] which allows the sizing of the PMOS device's channel length between 10 nm and 30 nm. The FinFET channel length of 15 nm was required to meet the DAC INL requirement of 5-bit resolution.

Both DAC variants had their control signals driven by a thermometric decoder implemented in Verilog-A. This approach ensured identical driving signals within the 0.2 V supply voltage domain, matching the voltage used by the GNR logic gates [2].

B. GNR-Based 5-Bit DAC

When analizing a DAC, the following aspects should be considered: (i) the resolution, which is evaluated using the INL and DNL, and (ii) the offset error. Figure 8 presents the relationship between the DAC's input code and analog output signal, i.e. the transfer characteristic.

In Figure 9 the resolution of the proposed GNR DAC was evaluated using the DNL and INL plots derived from the GNR DAC's transfer characteristic. Furthermore, Figure 8 was used to determine the LSB value of 3.10 mV necessary for calculating the aforementioned characteristics. The DNL's variation between $[-0.196, 0.088]$ LSB and the INL's variation between $[-0.809, 0.364]$ LSB indicate that the DAC: (i) is monotonic, (ii) meets the 5-bit resolution requirements, and (iii) GNR structure's behavior matches that of a current source across the entire output voltage range, resulting in a true 5-bit DAC. As expected from a thermometric DAC, a much smaller DNL error is achieved, while the INL error remains unaffected, as the thermometric approach cannot suppress the latter nonlinearity [7].

In addition to the LSB value, Figure 8 provides us with the DAC's offset voltage value of 4.52 mV. This offset is caused by the off-state leakage current of the GNR DAC's current sources corresponding to input code zero. The offset can be eliminated completely, by designing GNR topologies that have a much higher I_{ON}/I_{OFF} ratio. However, this might also increase the difficulty of maintaining (i) a purely monotonic transfer

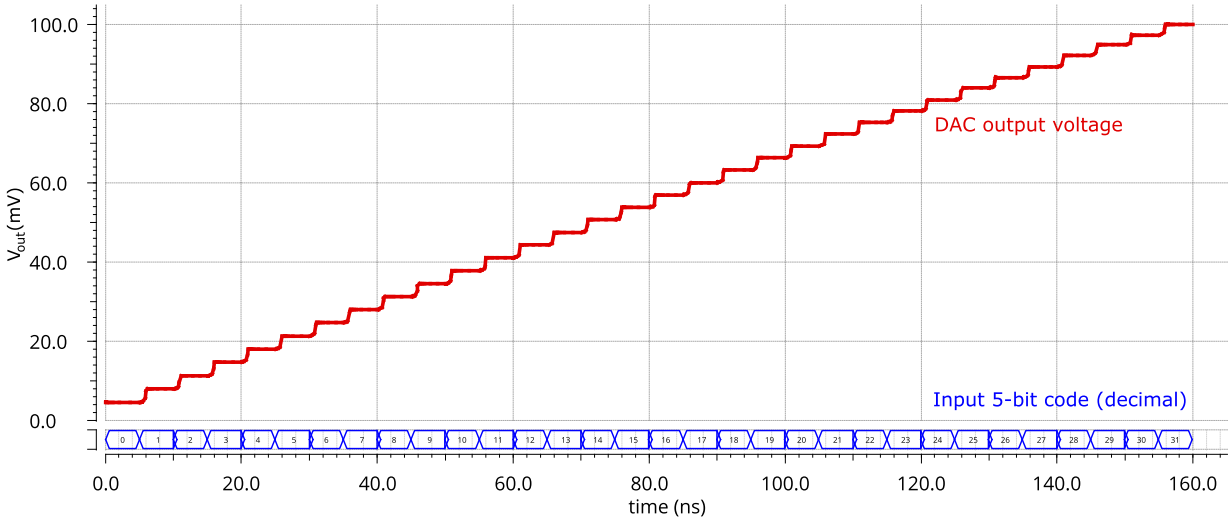

Fig. 8. 5-bit GNR-based DAC Transfer Characteristic.

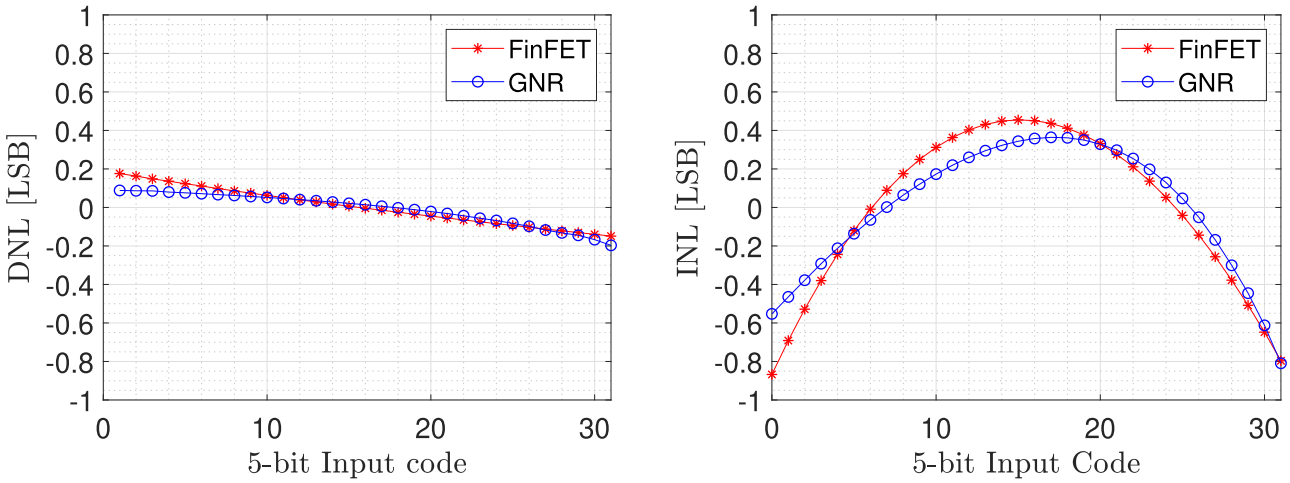

Fig. 9. DNL and INL Plots for GNR vs. FinFET Comparison.

function and (ii) an output characteristic that continues to enable operation across a large V_{DS} voltage range while sustaining minor variations of the GNR's I_{ds} current. Alternatively, since when implementing a complete neuron, the output of the DAC is intended to drive a comparator's input, while the other comparator input is tied to a fixed threshold value, the offset can simply be accounted for in the fixed threshold value at no cost.

TABLE I
GNR DAC VS. 7 NM FINFET DAC

	INL_{min} [LSB]	INL_{max} [LSB]	DNL_{min} [LSB]	DNL_{max} [LSB]	Area $[nm^2]$
FinFET	-0.796	0.454	-0.148	0.176	3255
GNR	-0.809	0.364	-0.196	0.088	1199

C. GNR Based DAC vs. 7 nm FinFET Based DAC

A comparison between the GNR based DAC and its FinFET counterpart is made across the INL, DNL, and offset voltage results, as well as the active area occupied by each variant.

As shown in Figure 9, the DNL and INL results for the FinFET and GNR are similar, with the FinFET variant achieving a DNL ranging between $[-0.148, 0.176]$ LSB, an INL ranging between $[-0.796, 0.454]$ LSB, and an offset voltage of 0.11 mV. Overall, nonlinearity wise, the GNR based DAC is marginally superior, as shown in Table I. The GNR DAC achieved a smaller INL variation compared to that of the FinFET, even though a longer 15 nm channel length was used for the FinFET, as 10 nm minimum length devices exhibited an INL higher than 1 LSB and were outruled. Evaluating the transfer characteristic for the FinFET device at $V_{gs} = V_{DD} = 0.2$ V, we measured an $I_{ds} = 81.76$ nA at $V_{ds} = 100$ mV and an $I_{ds} = 96.39$ nA at $V_{ds} = 200$ mV. This translates into a 15% variation of the I_{ds} current across the 100 mV to 200 mV V_{ds} range corresponding to the 0 mV to 100 mV output swing of the DAC. Comparatively, the GNR which achieves a variation of only 9% in matching conditions. In turn, this indicates that the output resistance of the FinFET device is smaller than that of the GNR for the

ultra-low supply voltage operating conditions listed above once the FinFET device multiplicity is scaled to provide matching current values. Alternatively, we could have only increased the multiplicity of the FinFET devices in the design, leading to an artificially increased FinFET area and an unfair comparison. In order to compensate for the fact that the FinFET is operating in the subthreshold region [13] and has a smaller current compared to the unit GNR element, we scaled the load of the FinFET to $R_{LOAD} = 40\ \text{k}\Omega$ to achieve matching ouput voltage swings for both DAC implementations.

When looking at the device's active area, we see that the GNR DAC occupies approximately one third of the active area used by the FinFET DAC, as shown in Table I.

D. Manufacturing Challenges

The DAC performance evaluation is centered on the DAC transfer characteristics by accounting for the finite output resistance of our current sources, when they are enabled, and their leakage currents, when they are disabled, with their impact on the DAC's performance being revealed in the DNL and INL characteristics. Another aspect to consider relates to the manufacturing challenges and their potential impact on the DAC performance. Because of manufacturing related defects, inadvertent mismatches among the current source units may occur and limit the DAC performance. When fabricating GNR devices, accurate GNR widths and clean edges which preserve the crystallographic orientation are key requirements as they can have a big influence on the GNR conduction properties. Up to date, the current manufacturing lithography cannot fabricate the GNR structures with geometry dimensions we proposed. Recently rapid progress has been made though for other fabrication techniques, e.g., chemical vapor deposition synthesis of graphene [14], or longitudinally unzipping of high quality grown carbon nanotubes [15]. Nevertheless, while exceeding the precision limit of the current lithography, they are still facing difficulties in producing GNRs with atomic precision. Since we don't have fabrication data for proposed GNR topologies dimensions, we cannot perform a meaningful statistical mismatch analysis. However, we know from other studies [16] which employ GNRs with small scale dimensions that variability (e.g., caused by manufacturing related edge defects) is not changing the expected functionality of the GNR. Moreover, neural networks exhibit naturally variability and stochasticity, and thus synaptic variability might create diversity in the device that is beneficial for the overall neural network dynamics.

V. Conclusion

In this paper we proposed a 5-bit DAC implemented in the appealing GNR technology, i.e., featuring low active area and ultra-low voltage operation, thus opening the path to implementing programmable synaptic weights necessary for building McCulloch-Pitts neuron structures. The proposed DAC relies on: (i) GNR unit current cells and (ii) a GNR logic thermometric decoding block. The DAC's analog array was implemented using 31 GNR-based current sources, whose current cell gates are individually driven by the GNR-based thermometric decoder's output. The thermometric approach was chosen to guarantee a monotonic transfer function. Our implementation was based on mapping the GNR structure's conductance using Matlab, while a Matlab based GNR Verilog-A model was used for running extensive SPICE simulations. By utilizing GNR devices instead of FinFET counterparts, a reduction of the active area of the 5-bit current DAC by up to a factor of three can be achieved. Furthermore, the GNR 5-bit DAC implementation achieved this while maintaining comparable INL and DNL performance to that of the FinFET variant, i.e., DNL of $[-0.196, 0.088]$ LSB and INL of $[-0.809, 0.364]$ LSB, while operating at an ultra-low supply voltage of only 0.2 V.

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