An FM-UWB Transceiver for Autonomous Wireless Systems

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An FM-UWB Transceiver for Autonomous Wireless Systems

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CHAPTER 1. INTRODUCTION

Human are social beings who like to connect to one another, either in the form of active or passive communication. In active communication, two or more parties exchange information in a two-way fashion, while in passive observation one party receives information sent by another. Technology that provides a medium for information flows that enables such connectivity has always flourished. An active example is the telephone industry (both wired and wireless), a passive example is the television, and for both passive and active is the internet. The common element in these technologies is an interconnection network that allows information or data to be exchanged or spread.

The network can be established using a cable or a wireless channel. Wireless technology simplifies the connection process as it requires no cable installation and less infrastructure, which is attractive for aesthetic and also practical purposes. A wireless connection is advantageous in term of its flexibility and mobility, for example, when the sender and receiver change position, there is no cable that limits their movements or position. On other hand, there are also disadvantages to wireless, such as: slower transmission rate, security risk, and sensitivity to interference. Nowadays, the demand for wireless interconnectivity continues to increase and thus research on wireless communication methods has also flourished [1.1].

Recently, “the internet of things”, whereby sensor-enabled physical objects can communicate with each other is under development [1.2]. These devices are able to sense their surrounding environment, and then automatically communicate and coordinate a response for various conditions. Furthermore, a better understanding of the environment locally and globally can be obtained by collecting a lot of data from these devices. Interconnection between devices on a grand scale could open a new potential for applications that could change people's lives. One potential application is precision farming, where data collected by wireless sensors in the ground enable crop conditions to be adjusted individually, e.g., by spreading extra fertilizer on areas that need more nutrients [1.3].

An autonomous wireless system could realize such a network. Autonomous implies that the device is independent from physical infrastructure, and draws so

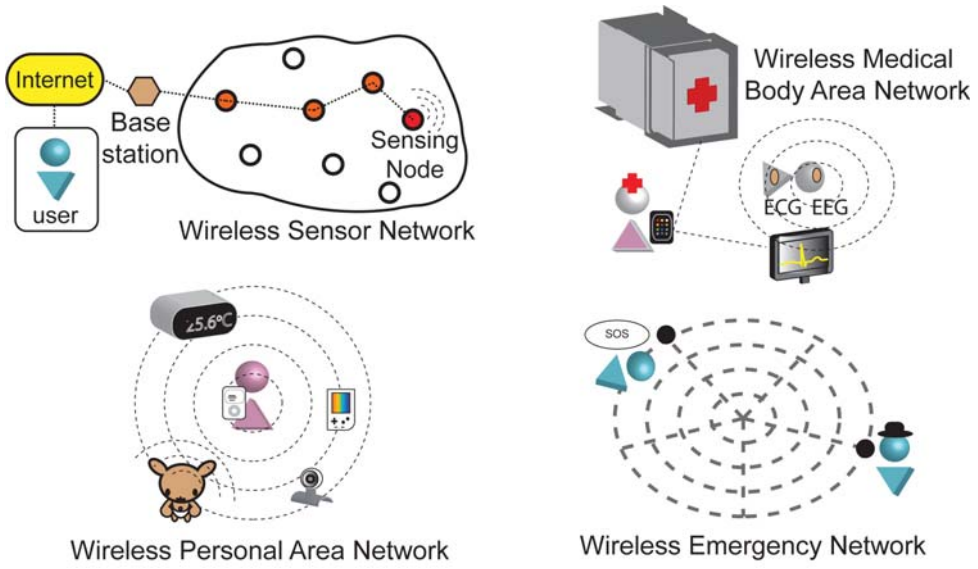

Figure 1.1. Applications for autonomous wireless network.

little net energy that it can be powered by a small battery and/or energy harvested from the local environment (e.g., using solar cell, etc.). Independence is important because the devices are deployed in a dynamic environment, where they could be self-configured, adapting, and communicating wirelessly. Autonomous wireless devices therefore can be installed in hard to reach places (e.g., underground to monitors soil or embedded in a bridge to monitor stress or strain), and must operate maintenance-free for years.

With a limited power source, the output power of the transmitter is kept low to conserve energy, while the receiver will a have lower sensitivity as the signal amplification is similarly limited. Thus, the link span between transmitter and receiver is shorter than for a conventional radio and is only suitable for applications that need local connectivity. At a longer distance, data can be relayed across transceivers forming a multi-hop network.

Autonomous wireless devices are constrained at present by their weight, volume and cost of the energy source (e.g., Li-ion battery). Therefore, energy efficiency is of paramount concern for the wireless link. Harvesting renewable energy from the surroundings will reduce the capacity of the battery required and prolong the operating time of the device when the transceiver is sending/receiving data, and the system is consuming maximum power. Embedded power management is therefore an essential part of the autonomous wireless system in order to conserve energy. The power management controller also monitors if energy can be harvested, estimates amount of energy left in the energy storage, and activates the device on based on priority. Overall, the power management sub-system ensures that the wireless device can be function as long as possible.

There are many other possible applications for such autonomous devices that could be linked to form a network (illustrated in Figure 1.1). One of the important

applications is wireless sensor networks (WSN). Sensors could be deployed to monitor defects due to aging or provide maintenance alerts in a plant, structure, or building. Sensors monitored via a wireless network avoid tedious and expensive inspection in order to collect data and allows the early detection of faults that improves safety [1.4].

Another application is wireless body-area networks (WBANs) or wireless personal-area networks (WPAN). These networks involve sensing our personal surrounding and provide connectivity between handheld devices and our environment. By automatically adapting the environment based on certain condition (e.g., turning on a heater when the temperature drops, or turning on music based on our mood as detected by a camera), a WPAN could ultimately improve our quality of life [1.5]. On a bigger scale, a smart home system could be created enabling automatic management of things such as energy consumption according to demand, monitoring of ambient conditions (e.g., temperature, lighting, music, etc.) and tracking of family members or their pets [1.6]. On an industrial scale, a smart building integrates building automation, telecommunication, facility management, and energy systems [1.7].

Wireless medical body-area networks (WMBAN) or wireless medical telemetry services (WMTS) facilitate continuous data streaming between patients being monitored and healthcare practitioners [1.8]. Monitoring wireless devices are usually compact enough so that they can be worn easily without discomfort. The network could monitor one's blood pressure or heart rate at home, and then transmit the data to a medical practitioner via a smartphone and/or personal computer. At a hospital, the network could monitor intensive care patients' conditions (e.g., their respiratory frequency, blood pressure, etc. [1.9]). A medical doctor could then be alerted in an emergency, which could potentially save a patient's life and improve the chances of surviving for critically ill patients. The wireless network also enables long-term surveillance for chronic patients, the handicapped or the elderly in real time. This promises to reduce the number of hospital visits and the work load of medical workers and healthcare professionals. Another application in the medical area is a bio-metric sensor such as non-invasive heart rate monitoring using radar [1.10].

Natural disasters, such as earthquakes or forest fires, require an emergency communication network [1.11]. A robust and highly redundant ad-hoc network formed by the interconnection of autonomous wireless nodes could provide a backup connectivity during a catastrophic event when infrastructure maybe damaged. The potential applications are not limited to the ones describes above. Other applications and opportunities are likely to emerge when autonomous short distance wireless transceiver devices are widely available [1.12].

1.1. Motivation

An autonomous wireless system is an attractive technology that has a huge potential to improve the quality of human life as described in the previous section. The aforementioned applications motivate the development of wireless transceiver hardware for the system. Development of the physical layer, network protocols, and

standardization are also needed. As more applications emerge and the technology develops, the performance of the system will improve while the cost reduces due to the increase in production volume and higher manufacturing efficiency. This trend will make the devices required to implement the system ubiquitous at an affordable price.

Autonomous wireless systems will likely be deployed on a large scale in the future. Figure 1.2 shows growth in WSN deployment (doubling every year) for the smart building sector, i.e., smart metering, smart home, industrial, healthcare, etc. Market research forecasts that tens of billion modules could be shipped over the next decade [1.14]. These devices would collectively require a lot of energy; assuming that each device consumes just an average of 1 mW, the total power consumption (assuming 10 billion devices) would be on the order of tens of megawatts. Therefore, energy should come from renewable sources collected through scavenging in order to be sustainable. Energy can be scavenged from many sources in the surrounding environment, such as mechanical vibration, light, heat, and microwaves radiation [1.15].

Figure 1.3 shows an example of integrated autonomous wireless system that might be implemented in the near future. The integrated wireless system consists of a wireless transceiver, baseband, embedded memory, micro-controller, power management, and CMOS sensors. A solar cell harvests energy and is also integrated together with the antenna for wireless transmission, while a button cell battery is a back-up power source. Harvested energy is stored temporarily on a supercapacitor or rechargeable battery. The ultimate goal is to build a device that operates for an indefinite period of time by managing energy harvesting and consumption itself, while sharing information collected by the CMOS sensors with other wireless devices.

Complementary metal-oxide semiconductor (CMOS) is a silicon integrated circuit (IC) technology that can integrate more than 1 billion transistors on-chip (at the current time of writing) to realize high performance analog, digital and RF circuits on the same die [1.16], [1.17]. System integration reduces the number of

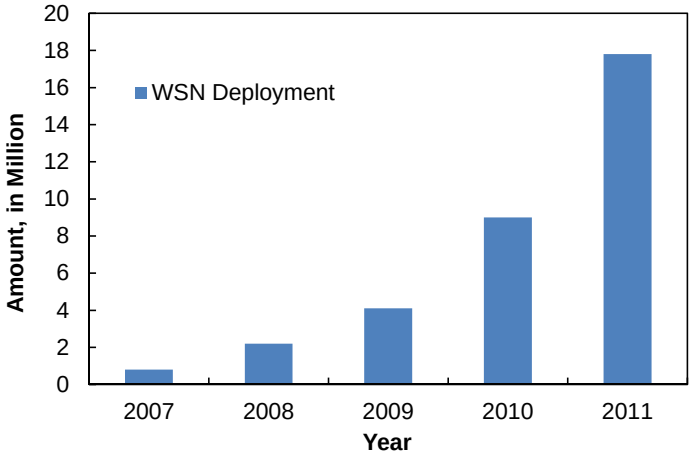

Figure 1.2. WSN deployment in smart building sector [1.13].

external components and IC chips (e.g., a one chip system). The advantages of integration using CMOS are: lower cost in high volume production, small size, less input/output interfacing, and lower leakage or standby power consumption. Furthermore, the trend in scaling of CMOS transistors to even smaller dimensions in the future will push integration levels higher, improve RF performance and lower power consumption [1.18].

Wireless interfaces often utilize the unlicensed (e.g., ISM) bands currently occupied by WiFi, Bluetooth and Zigbee appliances. However, the potential number of short-range wireless devices operating in a body-area or wireless sensor network would crowd the same space, and the resulting congestion would degrade the quality of service and link availability. However, other frequency bands could be used. The US Federal Communications Commission (FCC) [1.19] authorized the unlicensed use of ultra-wideband (UWB) transceivers in the 3.1–10.6 GHz range. The bandwidth available for UWB provides us opportunity to work on a UWB wireless transceiver for an autonomous wireless system. Due to the overlap with other communication channels in this band, the FCC specified a power emission limit for UWB signals of -41.3 dBm/MHz between 3.1 and 10.6 GHz. The spectral density limit is not constant over the entire band as seen from the specific indoor mask proposed by the FCC is shown in Figure 1.4. In Europe, ETSI/CEPT proposed a similar mask [1.20]. However, the 3.1-5 GHz band used for the transceiver designed in this thesis is more restricted in Europe, i.e., the transceiver needs to employ a detect and avoid scheme, otherwise the transmitted power spectral density is limited to -70 dBm/MHz [1.21]. It should be noted that the transceiver operating frequency can be scaled easily. The effective isotropic radiated power (EIRP)

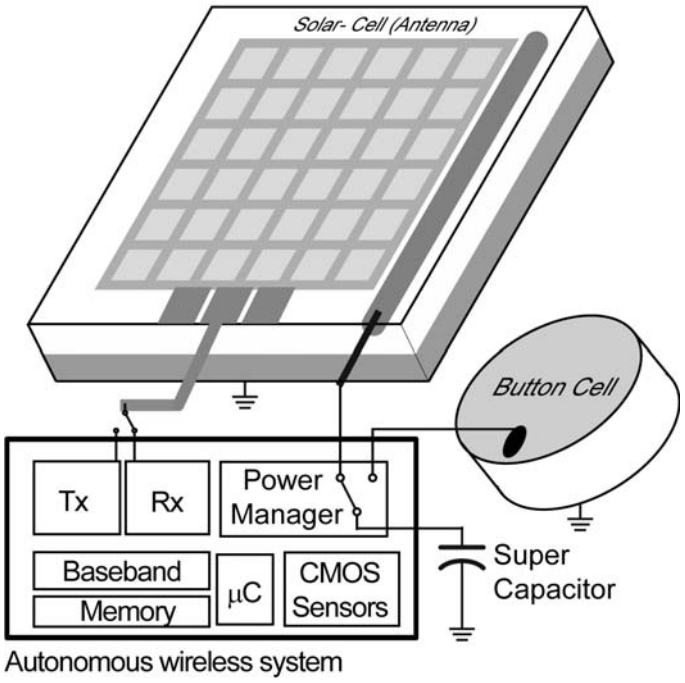

Figure 1.3. Building block for the envisioned autonomous wireless system.

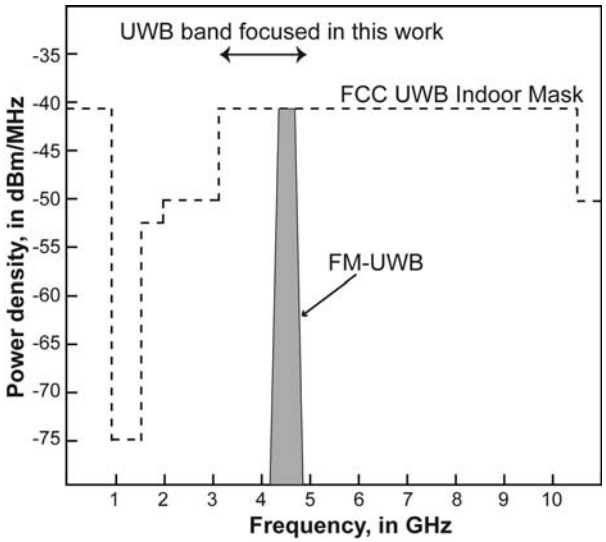

Figure 1.4. Ultra-wideband spectrum density.

spectral density limit and coexistence between UWB and other wireless standards is the subject of ongoing study [1.22].

The work in this thesis focuses on the design of low power FM-UWB transceiver for short-distance, low data rate indoor applications. Simplicity in the transceiver architecture, robustness to interference, and low-cost access to unlicensed spectrum available worldwide motivates us to work on a low power FM-UWB transceiver for autonomous wireless systems. Frequency-modulated ultra-wideband (FM-UWB) is a low-complexity scheme for wireless data communication at rates up to 250 kbit/s across spans less than 10 m [1.23]. The FM-UWB radio does not require a local oscillator or carrier synchronization at the receiver, which results in a simple transceiver architecture that consumes little power in continuous operation [1.24]. FM-UWB is intrinsically robust against multipath fading and narrowband interference, while mitigation techniques (e.g., using a notch filter or applying detect and avoid schemes) can be added to enhance its robustness [1.25]. An FM-UWB physical layer for body area networking has also been developed [1.26]. FM-UWB was recently adopted into the IEEE standard by the IEEE802.15 task group 6 [1.27]. Short distance transmission allows for a working link at a transmit power less than -10 dBm, and also minimizes interference to other wireless systems nearby. Relatively low transmit power reduces the risk of radiation harmful to the human body, which is important in WBAN and WMBAN applications [1.5]. Uniform spectral density and steep spectral roll-off at a typical bandwidth of 500 MHz (see Figure 1.4) for the transmit signal power spectrum is easily realized. Co-existence with other communication systems may be accommodated by transmitting the signal within a selected portion of the bandwidth allocated for UWB systems, according to the cognitive radio paradigm [1.28]. The FM-UWB scheme will be analyzed and described in more detail in the following Chapter 2 of this thesis.

1.2. Design challenges and overview

Despite the advantages of implementing an autonomous wireless system in CMOS, the technology also introduces compromises in performance. For example, the transit frequency (f_T) of a transistor is lower in CMOS than in bipolar junction transistor (BJT) technology. Although there are disadvantages to CMOS compared with the BJT, there are incentives to use CMOS, e.g., seamless integration with digital circuits and manufacturing capacity.

In general, integrating the wireless system on a single chip adds an extra complexity and challenge. A circuit has to satisfy the desired specifications regardless of manufacturing process, supply voltage, or temperature (i.e., PVT) variations in order to increase its manufacturability and yield [1.33]. Robustness against interference and coexistence with other wireless systems is also necessary in a wireless application. In a wireless transmitter, unwanted interference with other

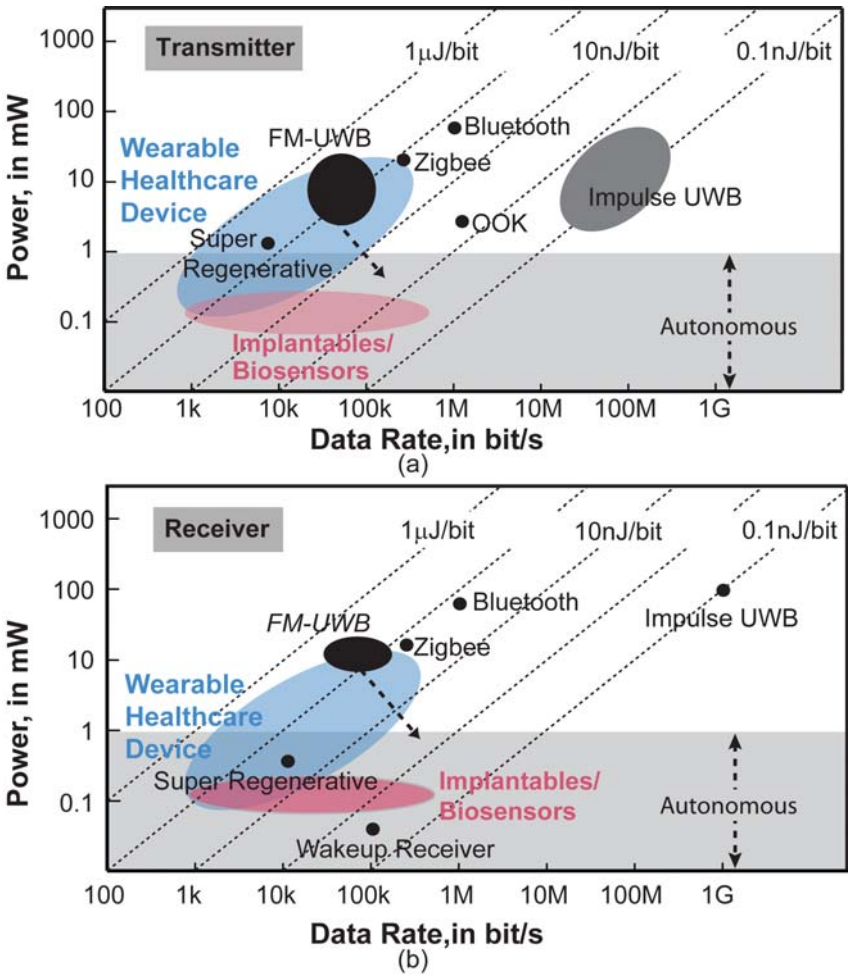

Figure 1.5. Energy efficiency of various wireless (a) transmitter and (b) receiver.

TABLE 1.1 TRANSMITTER PERFORMANCE SUMMARY

Ref.	Year	CMOS Technology (nm)	Modulation	Max. Tx power (dBm)	DC power (mW)	Tx efficiency (%)	Data rate (Mbit/s)	Energy per bit (nJ/bit)
[1.42]	2007	180	OOK	-11.4	3.8	1.9	1	3.8
[1.43]	2005	180	OOK	-4.4	1.6	22	0.005	320
[1.44]	2008	90	UWB	-16.4	4.36	0.52	15.6	0.28
[1.45]	2006	130	BFSK	-5	1.12	28.2	0.3	2.3
[1.46]	2010	180	BFSK	-5.2	1.15	26.2	0.125	9.2

TABLE 1.2 RECEIVER PERFORMANCE SUMMARY

Ref.	Year	CMOS Technology (nm)	Modulation	Sensitivity (dBm)	SIR at 10 MHz offset	DC power (mW)	Data rate (Mbit/s)	Energy per bit (nJ/bit)
[1.43]	2005	180	OOK	-100.5	N/A	0.4	0.005	80
[1.47]	2009	90	OOK	-72	-10	0.052	0.1	0.52
[1.48]	2010	180	BFSK	-86	-10	0.215	0.25	0.84
[1.49]	2007	90	UWB	-99	-15	35.8	0.1	2.5
[1.51]	2010	130	UWB	-55	-15	3.3	1.3	3.3

devices is mitigated by limiting the output power, filtering, and accurate control of center frequency or bandwidth of the transmitted signal. A wide tuning range, along with a detect-and-avoid scheme can be employed to combat interference in the receiver [1.34]. This implies that the system must be reconfigurable, and on-chip calibration circuitry must be included to handle any PVT variations and interference. Electrostatic discharge (ESD) protection must also be included. The ESD event could damage the input output (I/O) part of the chip, or in worst case, damage the entire chip. ESD protection in the RF signal path adds parasitic capacitance which limits the bandwidth and could cause signal degradation and distortion [1.35].

Improving energy efficiency, defined as ratio of power consumption (in Watts) to data rate (in bit/s), of the autonomous wireless system is the main challenge in this work. If a continuous operating lifetime of 50 days using a 10 gr Li-ion battery (energy density of 120 W-h/kg [1.36]) is desired, the transceiver should have an energy efficiency of less than 10 nJ/bit when operating at a data rate of 100 kbit/s. Conventional radio transceivers (e.g., WiFi, Bluetooth and Zigbee) consume approximately an order of magnitude more energy per bit transmitted as shown in Figure 1.5 [1.37]-[1.39]. This constrains their operating lifetime, battery size, and potential applications in autonomous systems.

Duty-cycling of a conventional wireless transceiver to scale the power consumption may not be possible if real-time data connectivity and high reliability are required. For example, many wireless health-monitoring devices require continuous data streaming between the patient being monitored and healthcare practitioners [1.40]. Health-monitoring devices use sensors that typically produce data rates in the range of 1-100 kbit/s, as opposed to multimedia applications that might stream video at 100 Mbit/s [1.41]. The FM-UWB scheme is suitable for lower data rate applications (see Figure 1.5), although improvement in energy

efficiency is required in order for it to compete with other radio schemes (e.g., wake-up receiver or super regenerative transceiver) in autonomous applications such as implantable biosensors.

Some narrowband and ultra-wideband radio technologies have demonstrated energy efficiency suitable for a wireless autonomous system. On the transmitter side (see Table 1.1), efficiency (measured as transmitted output power divided by the DC consumption, along with energy per bit) indicates the level of autonomy that may be achieved. On-off keying (OOK) modulation has been a popular choice for implementation of ultra low-power radio demonstrators. An OOK transmitter operating with an efficiency of 3.8 nJ/bit at 1 Mbit/s was reported in [1.42]. The super-regenerative transmitter designed by [1.43] also employs OOK modulation running at 5 kbit/s, and achieves 320 nJ/bit efficiency and 22% transmitter efficiency. Although similar in total power consumption, the energy efficiencies of these examples are radically different due to the factor 10^3 in their respective data rates. An external high-Q SAW or BAW RF bandpass filter shapes the transmit output spectrum, but adds to the cost of components, their assembly, packaging, and testing. Time-domain impulse radio is a UWB technology suitable that offers the potential for improved energy efficiency at low data rates. However, the spectral side lobes emitted by an impulse UWB transmitter could interfere with other users. Also, the poor peak-to-average transmit power ratio at low data rates also affects the efficiency of the antenna driver adversely [1.44]. Binary frequency shift keying (BFSK) transmitters in [1.45] and [1.46] achieve transmitter efficiency of 28% and 26%, respectively. BFSK transmitter benefits from the high efficiency PA that can be designed for the constant envelope signal in BFSK. The transmitter in [1.45] uses a 0.4 V supply that is not commonly used. The transmitter in [1.46] directly couples the oscillator to the load through a matching network, which cause vulnerability to frequency pulling from strong interference.

On the receiver side (see Table 1.2), energy per bit indicates the receiver efficiency. Signal-to-interference ratio (SIR), measured when the bit-error rate (BER) deteriorates to 10^{-3} due to narrowband interference in-band or at a small frequency offset (e.g., 10 MHz), indicates the robustness of the receiver. The narrowband 'wake-up' receiver monitors the wireless channel continuously and activates the main transceiver when addressed by the wireless network. An energy efficiency of 520 pJ/bit at a data rate of 100 kbit/s and -72 dBm RF sensitivity was reported for a prototype wake-up receiver [1.47]. However, the modest sensitivity and OOK modulation scheme used by the wake-up radio restricts its span and reliability in a wireless link. Also, an off-chip bulk acoustic wave (BAW) RF preselect filter is required to reject potential interferers in the wake-up radio design, which increases the size and cost of the receiver. The super-regenerative receiver in [1.48] achieves high energy efficiency and sensitivity by using BFSK modulation. However, the narrowband receiver is susceptible to multipath fading or interference effects because the front-end operates at a fixed input frequency and is not tunable. The receiver relies on the narrowband filter, and achieves an SIR of -10 dB at 10 MHz offset, but it degrades to 0 dB in-band. The UWB receiver in [1.49] also realizes good energy efficiency by duty cycling, but it requires synchronization to the received data, and possibly a wake-up receiver to detect incoming data.

TABLE 1.3 FM-UWB TRANSMITTER PERFORMANCE COMPARISON

Parameters	**[1.52]**	**[1.53]**	**[1.54]**	**[1.55]**	**[1.56]**
Year of publication	2006	2008	2009	2009	2011
Technology	180 nm CMOS	180 nm CMOS	180 nm CMOS	130 nm CMOS	180 nm CMOS
RF Tuning Range (GHz)	2.7-4.1	0.5-5	3-5.6	6.2-8.2	3.2-4.45
V_{DD} (V)	1.8	1.8	1.8	1.1	1.6
Phase Noise (dBc/Hz at 1 MHz)	-70	-75	-80.6	-107	-92
Max. Output Power (dBm)	-34	-9	-11	-5	-12.8
Bandwidth (MHz)	-	550	-	550	700
Sub-carrier Frequency (MHz)	-	1	-	1	51
Data rate (kbit/s)	100	100	-	100	1000
Power Consumption (mW)	7.2-14	2.5-10	19.8	4.6	18.2
Active Area (mm^2)	0.7	0.25	0.77	0.062	1.4
Energy Efficiency (nJ/bit)	72-140	70-100	198	46	18.2

TABLE 1.4 FM-UWB RECEIVER PERFORMANCE COMPARISON

Parameters	**[1.57]**	**[1.58]**	**[1.59]**	**[1.60]**
Year of publication	2006	2006	2009	2011
Technology	180 nm CMOS	SiGe BiCMOS 180 nm	SiGe BiCMOS 250 nm	180 nm CMOS
RF band, in GHz	3-5	3.1-4.9	7.2-7.7	3.4-4.3
Power Consumption, in mW	19.8	10	9.1	9.6
Receiver sensitivity, in dBm	-65	-46	-86.8	-70
Data rate, in kbit/s	100	100	50	50
Energy efficiency, in nJ/bit	198	100	182	192
Active area, in mm^2	-	0.72	0.88	1

Synchronization in IR-UWB requires complex hardware and additional power consumption [1.50]. The other UWB receiver in [1.51] operates at 1.3 Mbit/s, but has poor sensitivity (-55 dBm) and is confined to RF inputs below approximately 1 GHz. The UWB receiver obtains an in-band SIR of -15 dB, due to its spectral diversity.

A summary of existing FM-UWB transceivers reported in recent publications are listed in Table 1.3 and 1.4 for transmitters and receivers, respectively. Unfortunately, it is clear that the energy efficiency is nowhere near the 10 nJ/bit that would make it practical for an autonomous wireless system. The work in this thesis attempts to shows the suitability of FM-UWB for low power, low data rate

applications such as WSN, WMBAN, and WPAN, which will increase interest in FM-UWB transceiver development and implementation.

The main challenge in power management is to maintain energy efficiency across different operating conditions and voltage levels. It has to provide the wireless system with a clean supply voltage with minimal ripple. Both the input and output voltages have to be monitored. A digital controller sets the power manager configuration based on conditions such as the availability of energy to be harvested, amount of required current load, requirement on step up/down voltage conversion, etc. The DC to DC converter in the power management sub-system is constrained by the chip area required for passive components compared to the area occupied by transistors in an IC that can be produced economically. Realizing on-chip passive devices, e.g., a capacitor with a size of few nF or inductor with a size of few μH [1.61], will requires few mm^2 of die size.

Several challenges to realize an on-chip autonomous wireless system have been described. The work in this thesis attempts to address many of the key barriers to implementation and to propose and demonstrate solutions. The objective of the work described in this thesis is to realize a fully-integrated FM-UWB transceiver consuming less than 1 mW at an energy efficiency of better than 10 nJ/bit (see arrow trajectory in Figure 1.5). The power management sub-system will also be prototyped so that a battery and power scavenging devices can be used as energy sources.

1.3. Outline of the thesis

This thesis is divided into seven chapters. Chapter 2 describes the technical background of a wireless transceiver. Several wireless modulation schemes relevant to low power wireless systems will be described and compared, and the FM-UWB scheme will be highlighted and analyzed in detail. A wireless link margin analysis and parameter-performance trade-offs for the transceiver are described in Chapter 2 along with the specification for the proposed autonomous transceiver. Conventional FM-UWB transceiver designs from the recent literature will be described and analyzed. The efficiency limitations of a wireless system are analyzed, and several CMOS circuit techniques from the literatures that attempt to improve power efficiency are described.

A proposed low-power FM-UWB wireless transmitter is the subject of Chapter 3. A fully-integrated transmitter prototype was implemented using 90 nm CMOS and tested as a proof of the concept. A current-controlled ring oscillator generates the RF carrier frequency, followed by a class-AB power amplifier (PA) to drive the antenna. A frequency calibration scheme utilizing the successive approximation technique and a frequency-locked loop (FLL) is also proposed and implemented. The transmitter has been characterized completely and the results validate the proposed architecture.

A wireless receiver design for FM-UWB using a regenerative RF preamplifier and an envelope detector is presented in Chapter 4. The receiver front-end was implemented in 65 nm CMOS, while baseband circuitry is implemented externally using off-chip components. The regenerative receiver is analyzed and compared

briefly with the conventional FM-UWB receiver. Measured data for the new design are compared with other low-power receivers.

A fully-integrated FM-UWB transceiver prototype based on receiver and transmitter concepts described in Chapters 3 and 4 is the subject of Chapter 5. The RF-ICO generates a signal at one-third the operating frequency, which is then frequency multiplied by a tripler and amplified. The regenerative receiver front-end amplifier is implemented using an inductive positive feedback followed by envelope detector and IF amplifier. The transceiver was implemented in 90 nm CMOS and includes on-chip biasing, baseband processing, a serial input control port, and digital calibration circuitry.

Chapter 6 describes a power management circuit suitable for an autonomous FM-UWB system. Building blocks including the DC-DC converter, battery, supercapacitor, and solar cell described in the first sections of this chapter. The power management sub-system uses a button cell battery and solar cell as energy sources, and a supercapacitor to store energy during transient conditions. A hybrid of a switched-capacitor and an LDO regulator is designed to provide a constant supply voltage for the transceiver with average conversion efficiency of 64%, and ripple of less than 0.1 mV in the output voltage.

Finally, the main findings and major contributions of this research work are summarized in Chapter 7. Suggestions for future work aimed at developing the concepts and presented prototypes conclude this thesis.

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CHAPTER 2. TECHNICAL BACKGROUND

2.1. Introduction

As stated in chapter 1, developing a low FM-UWB wireless transceiver is one of the main objectives of this thesis. This chapter begins with an overview of available wireless communication modulation methods. Subsequently, the FM-UWB modulation scheme will be described in more detail. Technical background for the conventional FM-UWB transceiver will be discussed. Specifications for an FM-UWB transceiver using CMOS technology and a link margin analysis will then be presented. Finally, a brief technical review of CMOS technology that relates to power consumption and various CMOS circuit techniques that enable low power design will be described.

2.2. Digital Modulation

This section will not attempt to list all existing wireless modulation techniques, instead it will focus on digital modulation techniques that are suitable for low power wireless systems. Digital modulation offers greater accuracy than analog in the presence of noise and distortion. The main tradeoff between each modulation scheme is receiver sensitivity for a certain signal to noise ratio (SNR), bandwidth efficiency, and complexity of the implementation.

Shannon's theorem states that the channel capacity, *C* in bit/s, is an upper bound on the data rate that can be transmitted, as given by

$$C = B \cdot \log_2(1 + \frac{S}{N}) = B \cdot \log_2(1 + \frac{Eb}{N_O}\frac{R}{B}), \tag{2.1}$$

where a given average signal power, *S*, is transmitted through a communication channel that subject to additive white Gaussian noise (AWGN) of power *N* [2.2]. *Eb* is the energy per bit, N_O is the thermal noise spectral density. R/B, in bit/s/Hz is the ratio between data rate and signal bandwidth, also referred to as the spectral efficiency. As shown in Figure 2.1, a complex modulation scheme (e.g., QAM) packs many bits of data into each signal transition but requires higher SNR per bit

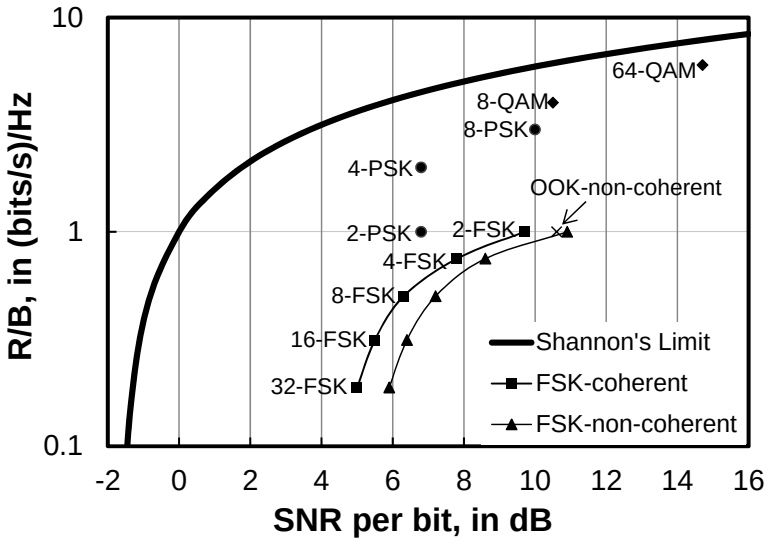

Figure 2.1.Spectral efficiency versus SNR per bit at BER = 10^{-3} for various modulation schemes [2.3], [2.4].

for equivalent BER compared to a simpler modulation scheme. A complex modulation scheme also requires extra hardware, such as a fast, high-resolution ADC, complex baseband circuitry, and high-linearity PA that consumes more power. On the other hand, FSK modulation sacrifices bandwidth to achieve a lower SNR requirement. Although bandwidth can be traded to get better sensitivity (as in FSK modulation), both are bounded by the Shannon limit (see Figure 2.1). The asymptotic limit for SNR per bit as defined by equation (2.1) is -1.6 dB, assuming that the bandwidth is infinite. An error correcting code (ECC) can reduce the required SNR by a few dB at the cost of reduced data throughput due to computational overhead which consumes more power [2.3].

For a low power transceiver design, the priority goes to low complexity and high sensitivity for the modulation scheme, at the cost of bandwidth efficiency. Binary frequency shift keying (BFSK) and on-off keying (OOK) are typically the main choice of modulation scheme in low power narrowband applications (see Table 1.1 and Table 1.2).

OOK is the simplest modulation scheme, whereby the carrier is turned on or off to represent digital bits. For example, the transmitter can be turned off, when the transmitted bit is '0', making the transmitter power efficient. A digital coding scheme can be employed to maximize the "off" time of the transmitter [2.1]. The power amplifier for OOK can be implemented with a high efficiency non-linear amplifier. OOK modulated data can be received using an envelope detector, removing the need for a local oscillator and mixer. OOK typically uses a single frequency carrier, which simplifies the frequency synthesizer requirements. Two limitations of OOK modulation are that it is spectrally inefficient and that it is susceptible to interferers. An OOK modulated carrier includes harmonic tones which increases its effective bandwidth. Since the receiver detects the received bits

by sensing the energy within a specified band, any noise or interference will cause an error.

BFSK is a constant envelope signal, and hence a high efficiency non-linear power amplifier can be used in the transmitter. A BFSK receiver typically uses a limiter which reduces the susceptibility to fast fading. Non-coherent detection for BFSK is generally used at the cost of 1-2 dB less sensitivity compared to a (more complex) coherent demodulator.

2.3. Ultra-wideband (UWB)

Ultra-wideband (UWB) communication is defined as wireless data transmission in which the emitted signal bandwidth exceeds 500 MHz or 20% of its center frequency [2.5]. Unlike a traditional wireless standard, where data is confined within a specific band, the data energy in UWB is spread over a large portion of spectrum, giving it some immunity to multipath fading and interference.

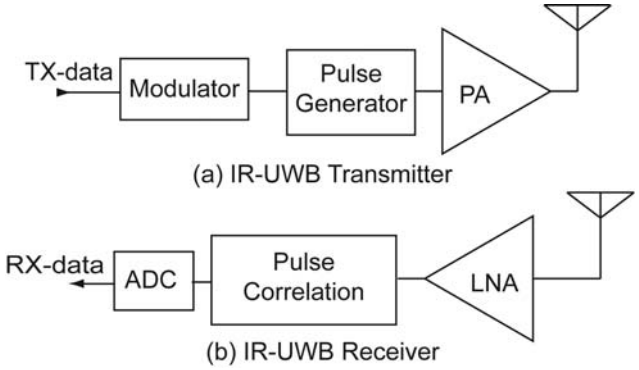

Figure 2.2. A typical transceiver block diagram for IR-UWB

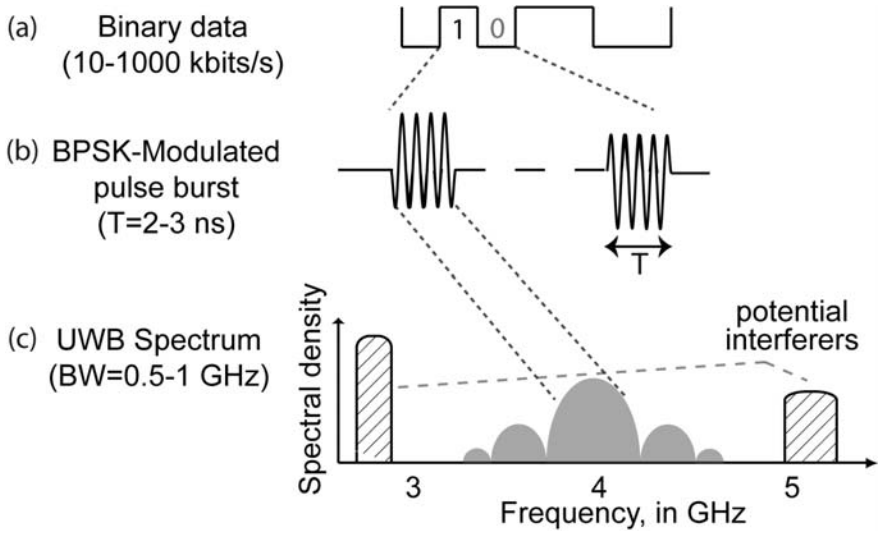

Figure 2.3. BPSK modulation scheme for low data rate IR-UWB [2.13]

Transceivers operating in the unlicensed UWB range are constrained in their link span by the regulations (see Chapter 1), with an average transmit power density of -41.3 dBm/MHz and peak transmit power of 0 dBm [2.6]. However, the RF transmit power from a UWB device is consistent with the capabilities of an energy-efficient, short-range wireless transceiver. Co-existence with other UWB communication systems may be accommodated by transmitting the signal within a selected portion of the bandwidth allocated for UWB systems, and employing detect-and-avoid or a frequency hopping scheme in a cognitive-type radio system [2.7]. A cognitive radio may change its parameters by monitoring channel conditions, (i.e., avoiding interference) and thus allows efficient spectral reuse [2.8].

As shown in equation (2.1), UWB offers greater capacity due to the large bandwidth available and enables data throughput up to 1 Gbit/s across a short distance [2.9]. Choosing UWB modulation for a low data rate application might seem counterintuitive. Fortunately, information spread over a large bandwidth can be recovered with an additional gain in the SNR called a processing gain [2.3], [2.10] (i.e., ratio between bandwidth and data rate). Furthermore, as in other spread-spectrum modulation techniques (e.g., CDMA), low data rate UWB attains immunity to jamming in proportion to the processing gain. Hence, the specification for the transceiver can be relaxed, e.g., lower output power or higher noise figure. This presents an opportunity to implement a simpler and lower power transceiver for low data rate applications.

UWB does not specifically constraint to a certain waveform, though a popular choice is a time domain pulse [2.11]. The energy of the pulses emitted through the antenna occupies a large bandwidth at a certain time instant. This type of transmitter originated early in the 20th century in the form of a spark gap transmitter [2.12]. A typical impulse radio UWB (IR-UWB) transceiver (shown in Figure 2.2) promises a simple and power efficient architecture. The transmitted data is modulated using pulse position modulation (PPM) or BPSK. Figure 2.3 shows an example of an IR-UWB modulation scheme using BPSK. A burst of pulses is used in this example in order to boost the average output power without violating the maximum peak transmit power as per FCC ruling [2.6]. Pulses produced by the generator are then transmitted by the antenna through a power amplifier. The receiver amplifies the received pulses using an LNA and then the pulses are demodulated using correlation. An ADC quantizes the demodulated signal and regenerates the received data bit stream.

There are several practical challenges that so far have prevented a fast market adoption of IR-UWB transceivers. On the transmitter side, the pulses need to be accurately shaped such that the spectrum has a certain center frequency, bandwidth and spectrum density. This is not an easy task, because such pulse shaping requires an RF filter that is sensitive to manufacturing variation. Typically, the spectral side lobes emitted by an impulse UWB transmitter could interfere with other users. The power amplifier (PA), low noise amplifier (LNA), and the antenna must have a wide bandwidth and it is a challenge to make the wideband amplifiers power efficient. The LNA is typically power hungry, although recent development has shown promising results for reducing the power consumption [2.14]. The wideband amplifier is susceptible to in-band interference that could severely reduce the

dynamic range. Another practical challenge for the receiver is to synchronize blindly when it receives the transmitted pulses, thus requires accurate timing and also requires initialization time to acquire the correct synchronization.

Other types of modulation that utilize the UWB spectrum are emerging, for example: orthogonal frequency division multiplexing (OFDM), where data is transmitted using a multiple narrowband carriers [2.15], [2.16]. OFDM transceivers need a complex carrier generator system that involves a fast PLL, and are neither simple nor low power. Thus, OFDM-type UWB transceivers are limited to high data rate applications. For low data rate applications, a novel UWB modulation scheme that utilizes frequency modulation (FM) such that the transmitted signal occupies a wideband spectrum at a uniform spectral density will be presented in the following section.

2.4. FM-UWB Modulation Scheme

Frequency modulated ultra-wideband (FM-UWB) is well-suited to low-complexity, low power wireless transceiver implementations, and suitable for transmission links up to 10 m [2.10]. FM-UWB uses low modulation-index (m_i) FSK (e.g., $m_i = 1$) to encode binary data at a rate of 10-250 kbit/s (typicaly100 kbit/s) onto a sub-carrier at an intermediate frequency (IF) of 0.5-2 MHz. This is followed by a high modulation index (e.g., $m_i = 500$) analog frequency modulation of an RF carrier, resulting in RF signal bandwidth of 0.5-1 GHz as shown in Figure 2.4, where the RF carrier is swept back and forth at constant speed. Uniform spectral density and steep spectral roll-off for the transmit signal are realized through the use of a

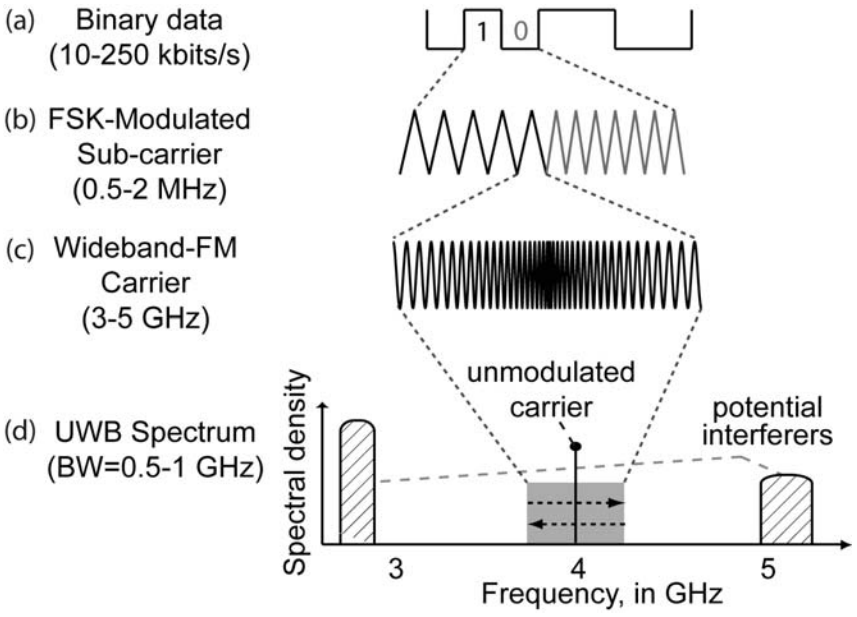

Figure 2.4. FM-UWB modulation scheme, where data (a) is FSK modulated onto a triangular sub-carrier (b). Subsequently wideband frequency modulation of RF carrier (c) results in UWB spectrum shown in (d).

triangular sub-carrier waveshape. The transmit bandwidth is determined by the sub-carrier amplitude that can be controlled and calibrated easily. Not only the bandwidth, but also the center frequency are controllable, allowing flexibility in the transmitted UWB spectrum.

The agility of FM-UWB also allows a robust wireless system that could avoid potential interferers by employing a frequency hopping scheme similar to frequency-hopped CDMA (FH-CDMA) [2.1], but using a regular frequency hop

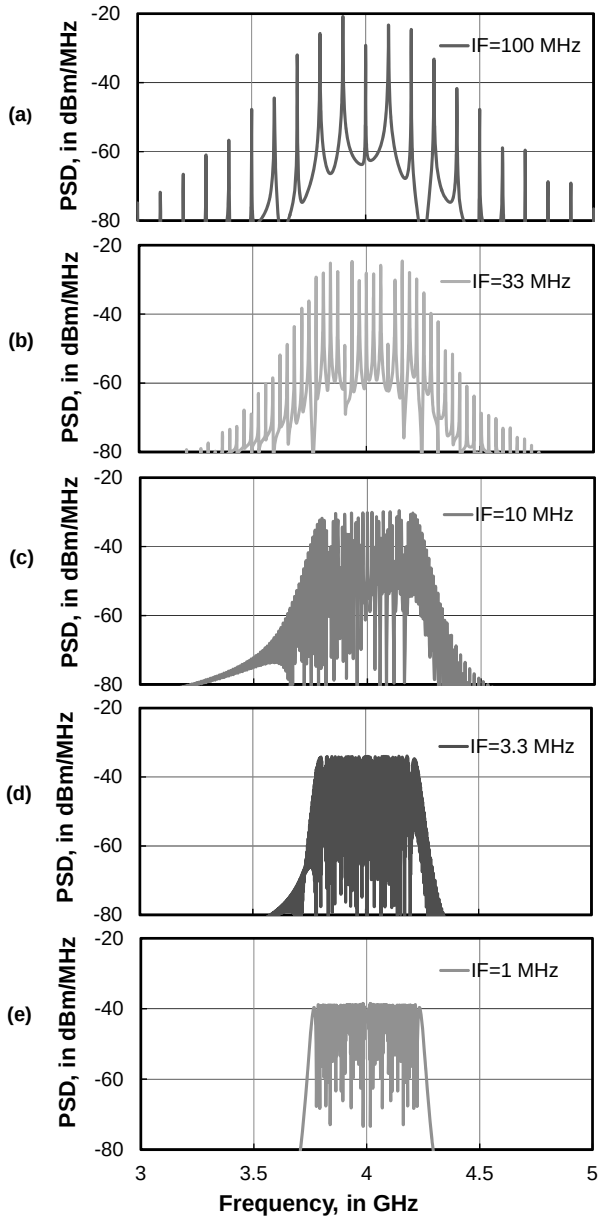

Figure 2.5. Simulated FM-UWB spectral density at 500 MHz bandwidth for different sub-carrier frequencies (IF).

instead of a random one. In this regard, FM-UWB has benefits associated with the spread-spectrum technique, such as immunity to jamming, a transmitting signal that is hidden in the background noise, and the ability to accommodate simultaneous transmission in the same frequency band (i.e., up to 15 users) [2.17]. FM-UWB accommodates multi-user capability in a network using time-division multiple access (TDMA), frequency division multiple access (FDMA), or sub-carrier FDMA sharing the same carrier frequency. In conclusion, FM-UWB offers robust, low-power and low-cost access to unlicensed spectrum available worldwide.

The FM-UWB transceiver operating frequency is defined by the regulators (see Figure 1.4), and preferably where maximum power could be transmitted in order to maximize link margin. The work in this thesis will focus on the 3-5 GHz band. A modulated signal bandwidth of at least 500 MHz is therefore required to conform to the definition of an UWB signal. Higher bandwidth means more spreading, and thus allows higher transmitted output power and link margin, but the transmitter consumes more power as a consequence. Flexibility to control the bandwidth is therefore advantageous for FM-UWB to be power efficient as channel conditions vary.

Figure 2.5 shows various FM-UWB spectra for different sub-carrier IFs. The higher the IF, the higher the spectral density and the more gradual the spectral roll-off. The sub-carrier IF needs to be at least one hundred times less than the RF bandwidth to obtain a large modulation index and create a uniform spectral density across the band. The IF should be limited to a frequency below 5 MHz, because above 5 MHz the spectrum is no longer uniform and power is concentrated at harmonics of the IF. Baseband data modulates the sub-carrier using BFSK modulation. Frequency deviation between symbols '0' and'1' needs to be at least equal to the data rate (i.e., modulation index $m_i > 1$) to avoid intersymbol interference and relaxes the FSK demodulator sensitivity requirement. A higher IF can be chosen to accommodate a higher data rate and multi-user FDMA scheme [2.17]. The double modulation in the FM-UWB scheme limits the maximum data rate. A practical FSK demodulator, such as a PLL, requires that the carrier is at a higher frequency (e.g., > 10 times) than the data rate [2.18]. FM-UWB could (theoretically) employ a maximum data rate up to one-half of the minimum IF [2.19], however, it will need an accurate FSK demodulator. This thesis will focus only on data rates less than 250 kbit/s, which applicable to WSN, WPAN, and WMBAN applications.

FM-UWB uses direct modulation, instead of up converting the modulated signal as in a conventional radio. Therefore, the sub-carrier wave shape determines the spectral density flatness and spectral roll-off. Figure 2.6 shows the simulated FM-UWB spectra for various sub-carrier wave shapes. Triangular and sawtooth sub-carriers have a uniform and flat spectrum density, thus they are suitable for FM-UWB. The triangular sub-carrier, which has a steeper roll-off and easier implementation, is therefore the preferable choice. Sine and hyperbolic sine functions create peaking at the edge of the signal band and steeper roll-off. As a consequence, the overall transmitted power must be reduced to conform to the spectral mask, and it could adversely affect the overall link margin. A low pass-

filtered triangular or sawtooth wave also exhibits similar peaking because the carrier power is not distributed evenly across the bandwidth.

Non-linearity in the carrier generator (e.g., frequency versus voltage in a voltage-controlled oscillator) will cause a non-uniform spectral density. This non-linearity only distorts the output spectral shape, and it is not critical for the FM-UWB communication. The output spectrum is usually distorted by the wireless condition (e.g., due to multipath), and is tolerable in an FM-UWB system [2.20]. Therefore, a linear carrier generator for FM-UWB is desired, but not necessary.

Multipath occurs when the same transmitted signals arrives at the receiver through different paths and hence with different time delays. The phase difference between these signals adds up constructively or destructively. This phenomenon

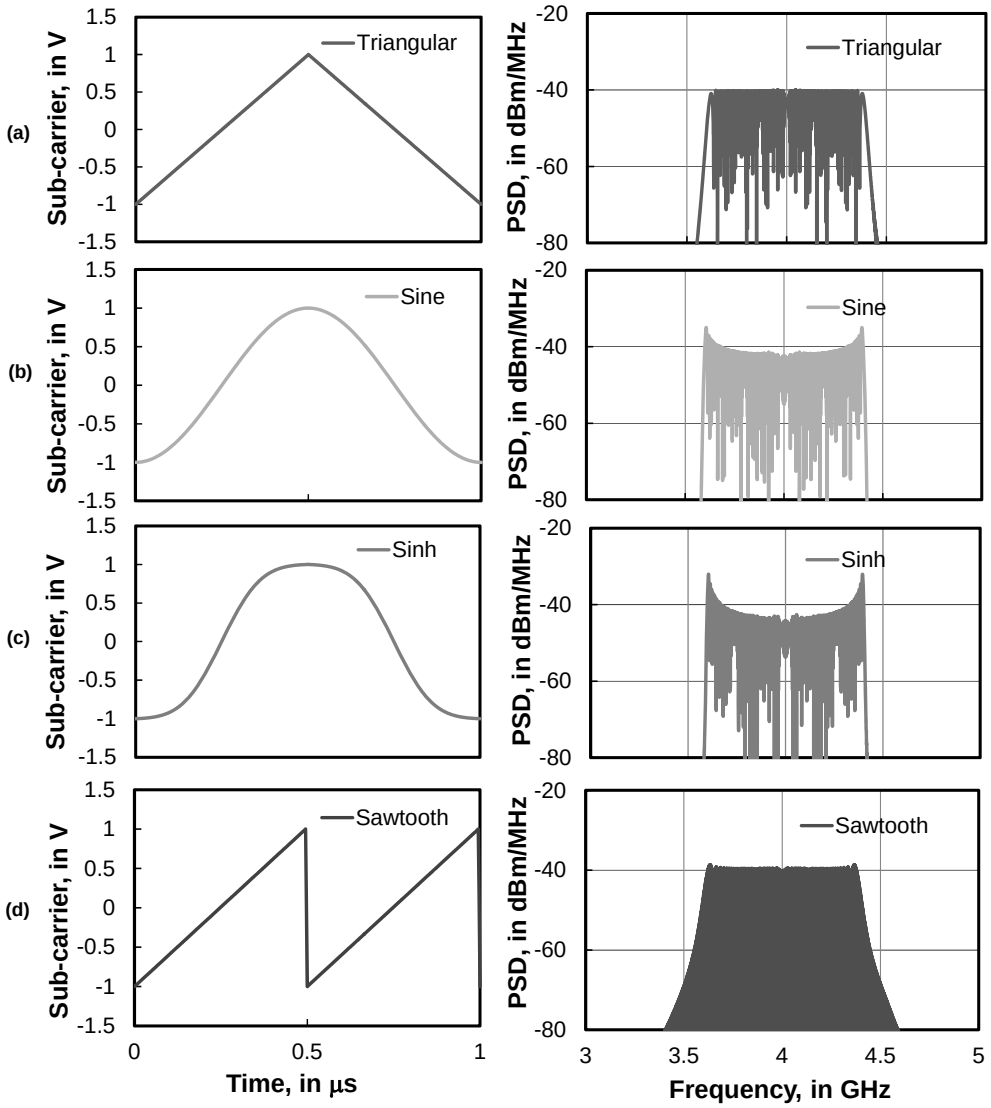

Figure 2.6. Simulated FM-UWB spectrum for various sub-carrier wave shapes.

typically happens in an indoor environment, where walls could reflect wireless signals and cause them to arrive at the same point with different phases. Figure 2.7 shows a simulation setup for the multipath effect (2 paths) on an FM-UWB signal. Each path has a different time delay and magnitude, where the attenuation is simulated based on the free space path loss (see Equation 2.4). Note that, the signal is attenuated more for longer delays emulating a longer path. Figure 2.8 shows that the simulated FM-UWB spectrum suffers from the two path effect for various time delay differences. Multipath causes fading at specific frequencies that depends on

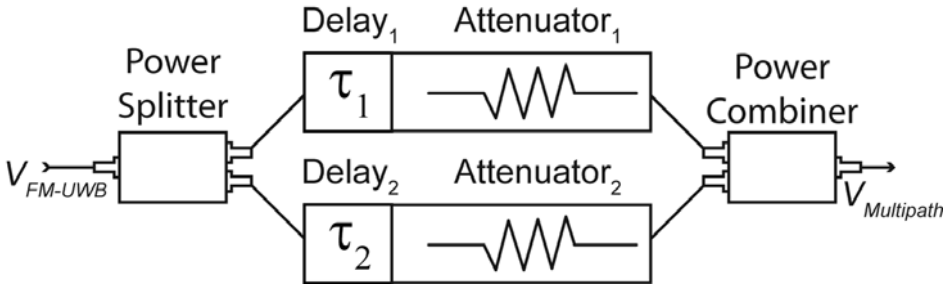

Figure 2.7. Setup used to simulate the multipath effect.

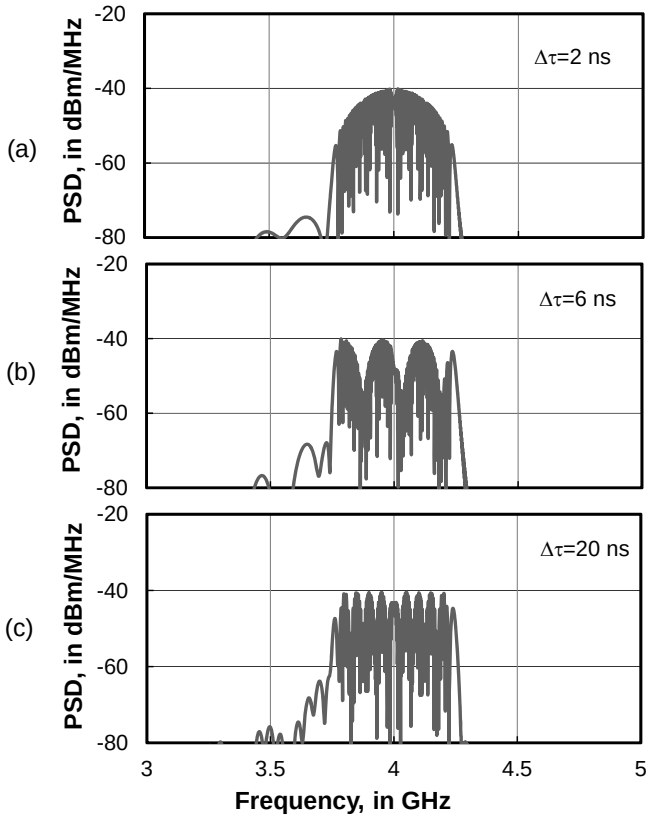

Figure 2.8. Simulated FM-UWB spectrum for two paths with a time delay difference of (a) 2 ns, (b) 6 ns, and (c) 20 ns.

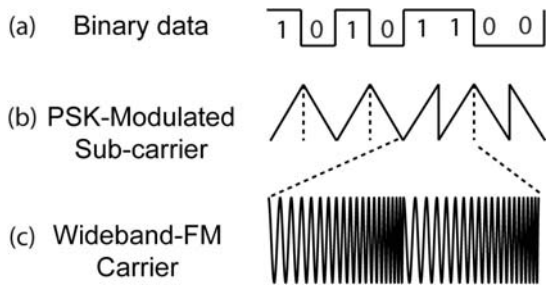

Figure 2.9. PSK sub-carrier signal using a sawtooth waveform.

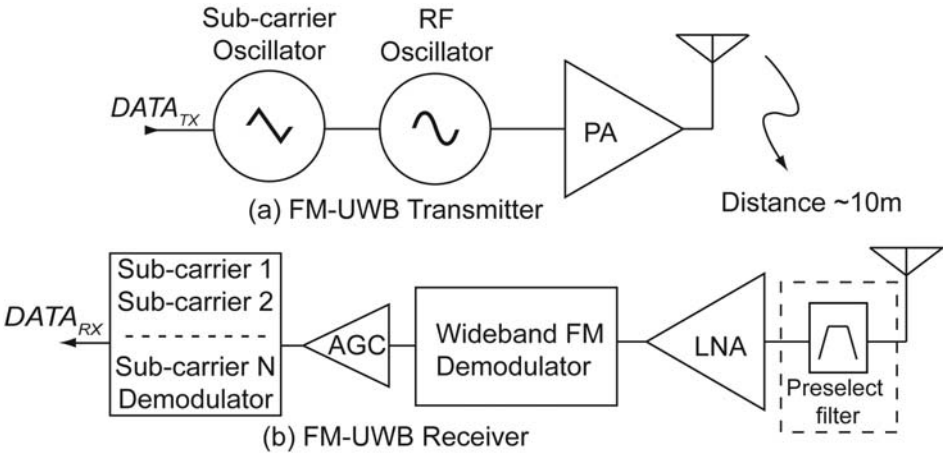

Figure 2.10. Block diagram of typical FM-UWB transceiver.

the delay time difference. A shorter delay difference causes fewer in-band nulls, but they are wider and deeper in bandwidth. The fading could also be time varying, which makes it difficult to compensate. Fortunately, the transmitted power of an FM-UWB signal is spread across a wide bandwidth, hence fading does not significantly degrade the signal, unlike the narrowband FM radio where receptions suffers when multipath fading occurs.

It is possible to use phase-shift keying (PSK) to modulate the sub-carrier signal while maintaining a uniform output spectral density by using a sawtooth wave shape. The sawtooth wave shown in Figure 2.9 represents a BPSK modulated signal, where the two phases are represented by an increasing or decreasing ramp. The phase that represents a data bit can be detected by a receiver employing a demodulator that distinguishes the direction of the sawtooth ramp. BPSK modulation opens a possibility for higher data rates or duty-cycled FM-UWB. However, these are beyond the scope of this thesis.

2.5. Specifications for FM-UWB transceiver

A generic transceiver block diagram suitable for FM-UWB is shown in Figure 2.10. The FM-UWB receiver does not require a local oscillator or carrier synchronization

TABLE 2.1 TARGET SPECIFICATIONS FOR THE FM-UWB TRANSCEIVER

Parameters	**Values**
Supply voltage, V_{DD}	1 V
Process technology	CMOS 65 or 90 nm
RF range	3-5 GHz
RF bandwidth	> 500MHz
Sub-carrier frequency	0.5-4 MHz
Data rate	< 250 kbit/s
Power dissipation, at 4 GHz	< 1 mW
Energy efficiency	< 10 nJ/bit
Chip area	< 1 mm^2
Transmitter	
Phase noise, at 4 GHz and offset frequency of 1 MHz	< -62 dBc/Hz
Output power	> -14.3 dBm
Spectral flatness within 500 MHz	< 3 dB
Receiver	
Receiver sensitivity	< -80 dBm
Bit error rate	10^{-3}
$\|S_{11}\|$	< -10 dB
Signal-to-interference ratio (NBI at 4 GHz)	< -20 dB

and the transmitter (in its simplest form) may be implemented using just a wideband voltage-controlled oscillator, which results in a simple transceiver architecture that consumes little power in continuous operation. Digital data transmitted from, for example a sensor, modulates the sub-carrier oscillator. Then, the sub-carrier wave directly modulates the RF carrier oscillator. A power amplifier (PA) acts as a buffer to drive the antenna. The receiver consists of an RF amplifier followed by a wideband FM demodulator. An AGC amplifier or limiter further amplifies the received sub-carrier. FSK demodulation of the received data intended for a different user is then required. Selectivity and robustness against out of band interference may be improved further by adding an optional preselect filter between the antenna and RF input. The UWB antenna could also be modified to provide a frequency notch to mitigate expected interference [2.21]. Compared to a conventional radio [2.22], the transceiver for FM-UWB is much simpler and hence better suited to low power applications.

The targeted specifications for the FM-UWB transceiver are summarized in table 2.1. CMOS is the technology choice for the FM-UWB transceiver prototypes developed in this thesis. IBM CMOS 65 nm and 90 nm technologies are employed [2.23], facilitated through MOSIS [2.24]. Standard devices in 90 nm CMOS typically use a 1 V supply to avoid breakdown of the active devices. In the various prototypes described in subsequent chapters, a single 1 V supply is chosen to power the RF front-end, analog and digital circuitry. A targeted power consumption of

1 mW is set for the receiver and transmitter to achieve an energy efficiency better than 10 nJ/bit at a data rate of 100 kbit/s. Chip area is minimized by using as few on-chip inductors as possible and the minimum number of bondpads. An (arbitrary) chip area of 1 mm^2 is the goal for the full transceiver.

The RF carrier frequency deviation in an FM-UWB system is typically > 250 MHz, which implies that phase or frequency jitter of the transmit source has less effect upon the received signal-to-noise ratio (SNR) than for a narrowband system. It has been shown that FM-UWB is able to tolerate transmitter phase noise as high as -73 dBc/Hz at 1 MHz offset with no significant degradation in bit-error performance [2.25]. The FM-UWB phase noise requirement is much relaxed compare to UWB-OFDM which requires of -87 dBc/Hz at 1 MHz offset [2.26]. RF carrier deviation for the FM signal compared to FM noise has to be higher than the required SNR. For a non-coherent BFSK demodulator at a BER of 10^{-3}, the required SNR is 11 dB [2.10]. FM-UWB has a minimum frequency deviation of 250 MHz, which corresponds to maximum frequency jitter due to white noise, σ_f of 49 MHz. Obviously, the higher the modulated FM bandwidth, the higher is the tolerable frequency jitter. Frequency jitter can be related to time jitter, σ_T by the equation

$$\sigma_T = \frac{\sigma_f}{{f_C}^2}, \tag{2.2}$$

where f_C is the carrier center frequency. Equivalent phase noise at frequency offset Δf can be described as [2.27]

$$L(\Delta f) = \frac{{f_C}^3}{\Delta f^2}{\sigma_T}^2. \tag{2.3}$$

From equation (2.3) and the calculated frequency jitter requirement, the FM-UWB transmitter must have a phase noise better than -62 dBc/Hz at 1 MHz offset to satisfy the minimum SNR for the BFSK at BER of 10^{-3}.

The spectral mask for UWB signals dictates that the maximum effective isotropic radiated power (EIRP) density is -41.3 dBm/MHz. For a 500 MHz modulation bandwidth, the power density limit translates into a total carrier power of -14 dBm, or 40 μW. A margin of 4 dB is added to the PA output in order to compensate for losses in chip packaging, the antenna matching network and variations in the antenna gain. Spectral flatness indicates how uniform the in-band signal spectral density is, and it is limited to a maximum variation of 3 dB.

Assuming line of sight (LOS), path loss (PL) between transmitter and receiver at a short distance can be approximated by the Friis' free space equation

$$PL = \left(\frac{4\pi d}{\lambda}\right)^2, \tag{2.4}$$

where d is the distance between transmitter and receiver, and λ is wavelength. Equation (2.4) is accurate when the distance higher than one wavelength (7.5 cm for f_C = 4 GHz). At shorter distances the antenna operates in the near field, and an advanced path loss model must be used [2.28]. Friis' equation is adequate in practice for calculating distances between the transmitter and receiver. A typical indoor FM-UWB link that covers a distance of 10 m translates into a free space

propagation loss of 66 dB at 5 GHz (assuming 0 dBi antenna gain). Thus, the sensitivity of the receiver required to accommodate a link span of 10 m is at least -80 dBm, as listed in Table 2.1.

Sensitivity of the receiver (P_{RX_MIN}) can be calculated using the link budget equation as follows

$$P_{RX\_MIN} = 10\log(kTB_{RF}) + NF + SNR_{FSK} - G_P . \quad (2.5)$$

The 50 Ω thermal noise in a 500 MHz bandwidth corresponds to -87 dBm noise power, which gives 7 dB SNR at the input of a receiver 10 m away from the transmitter. The required SNR at the receiver baseband for demodulation of 2-FSK at a bit error rate (BER) of 10^{-3} is 11 dB. FM-UWB may be considered a spread spectrum system with a processing gain (G_P) determined by the ratio of the RF to data bandwidths. Assuming 100 kbit/s data rate, the bandwidth of the 2-FSK data signal is 200 kHz, giving a processing gain of 34 dB (ideally). However, the receiver output SNR is a quadratic function of the RF-input SNR due to the non-linearity inherent in this type of non-coherent receiver. This results in an additional 6 dB degradation in SNR [2.10], so the overall margin for the receiver noise figure is the receiver input SNR (6 dB), minus the sum of the receiver penalty of 6 dB and required SNR_{FSK} of 11 dB, plus the processing gain (34 dB), or 23 dB margin. The margin will be reduced by the non-ideality of the filter and losses from envelope detector (if it is used). At higher data rate, the sensitivity reduces because the 2-FSK data bandwidth increases and thus G_P decreases.

RF input matching (i.e., $|S_{11}| < -10$ dB) is required to minimize energy reflection between the antenna and the receiver. The sensitivity to single-tone interference is defined by detecting the degradation in BER up to 10^{-3}. Signal-to-interference ratio (SIR) measures the strength of the input signal compared to interference, and is negative when the interference power is stronger than input signal. An UWB radio should be able to withstand SIR of less than -20 dB from narrow band interference (NBI) [2.29]. The following section will review previous work on FM-UWB transceivers.

2.6. Conventional FM-UWB Transceiver

The existing FM-UWB transmitters and receivers that have been proposed recently are usually based on the RF front-end shown in Figure 2.11. The conventional FM-UWB transmitter shown in Figure 2.11a [2.30], [2.31] generates the RF carrier using an LC-oscillator. An LC oscillator is widely used in RF wireless transceivers because of its simplicity, low power consumption at high frequencies of oscillation, and low phase noise. The frequency of the oscillator depends on the resonant frequency of its LC (inductor and capacitor) tank,

$$f_C = \frac{1}{2\pi\sqrt{LC}} . \quad (2.6)$$

The losses of the tank must be compensated by the negative impedance generated by an active device. Therefore, the tank Q-factor, especially for an on-chip inductor

with Q < 20, limits the minimum power consumption of the LC oscillator [2.32]. An LC-oscillator that has a tuning range less than 20% of the center frequency might not have enough frequency range for the FM-UWB transmitter. The oscillator output drives a 50 Ω antenna load using a CMOS buffer. To calibrate its center frequency, a periodic duty-cycled PLL plus external ADC/DAC and a microcontroller are included. The loop is closed until the oscillator reaches the desired frequency, and then it is opened for the remaining time period of the calibration cycle.

The sub-carrier could be generated by a direct digital synthesizer (DDS) and DAC [2.33]. The clock frequency of the DDS must be at least 24 times the sub-carrier IF. The minimum resolution of the DAC is defined by the RF bandwidth of 500 MHz divided by a resolution bandwidth of 1 MHz, which is 500, or 9-bits. Simulated power consumption of the DDS and DAC is 0.75 mW [2.33].

The conventional FM-UWB receiver shown in Figure 2.11b [2.30] first amplifies the FM signal using a wideband LNA and then transforms FM to a phase-modulated (PM) signal via a delay line with constant time delay (τ). The PM signal is then multiplied with the original FM signal to yield an amplitude-modulated (AM) output (illustrated in Figure 2.12a). By removing the high frequency carrier using a lowpass filter, the transmitted sub-carrier signal ($V_{IF\text{-}CONV}$) is recovered.

Assuming an ideal multiplier with gain of K and an ideal lowpass filter, the demodulated voltage as a function of frequency can be expressed by

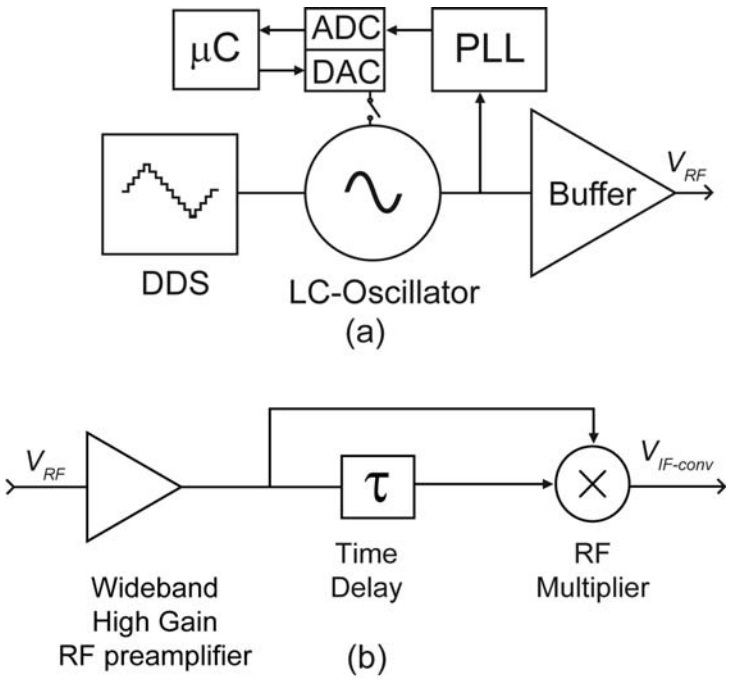

Figure 2.11. Conventional FM-UWB (a) transmitter and (b) receiver front-ends architectures.

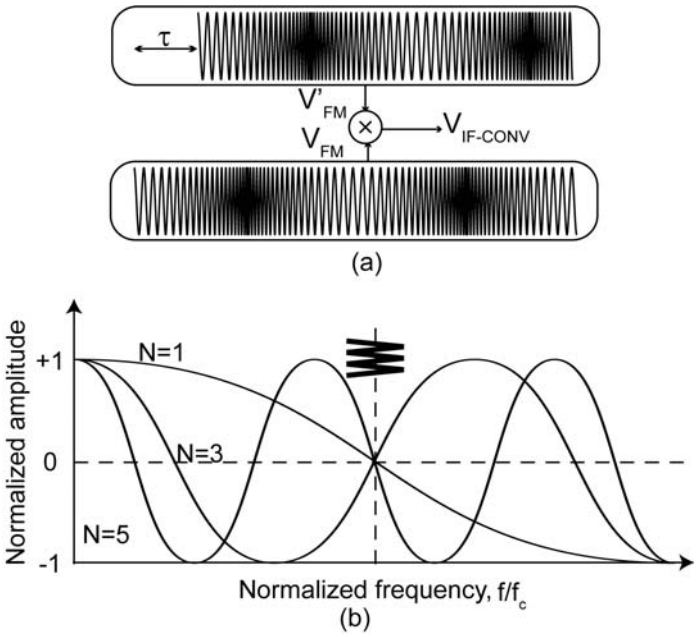

Figure 2.12. Illustration of (a) multiplication of an FM-UWB signal with its delayed version, and (b) its transfer function between amplitude and frequency.

$$V_{IF-CONV}(f) = K\frac{V_{FM}.V'_{FM}}{2}\cos(2\pi f\tau). \tag{2.7}$$

The delay (τ) must be an odd multiple of quarter periods at the center frequency of carrier signal, as expressed by

$$\tau = N\frac{T}{4} = \frac{N}{4f_c}, \qquad \text{for } N = 1,3,5,\ldots \tag{2.8}$$

By substituting (2.7) and (2.8), $V_{IF\text{-}CONV}$ can be expressed as

$$V_{IF\text{-}CONV}(t) = K\frac{V_{FM}.V'_{FM}}{2}\cos\left(N\frac{\pi}{2}\frac{f_c \pm \Delta f_c(t)}{f_c}\right). \tag{2.9}$$

Equation (2.9) predicts that the bandwidth of the FM signal ($2\Delta f_c$) determines the amplitude of the demodulated signal. As illustrated in Figure 2.12b, different values of N produce different transfer functions. *N* can be chosen to obtain maximum sensitivity and voltage swing based on the bandwidth of the signal. The required delay can then be derived from N and f_C. A wideband delay would consume a large inductor area [2.34] or large power consumption [2.35] if implemented on chip. Additionally, some tuning elements are required to tune the delay to its optimum value when the center frequency or operating frequency band is changed.

The conventional transceiver architecture has been proven not to be power efficient enough for autonomous wireless system (see Table 1.3 and Table 1.4). Therefore, a new architecture is developed in this thesis to realize a low power FM-

UWB transceiver suitable for autonomous applications. The following section will briefly describe various methodologies and circuit techniques that could improve power efficiency in CMOS technology.

2.7. Survey of Low Power CMOS Circuits

Circuit design techniques or methodologies could overcome CMOS technology limitations. As CMOS technology advances into smaller feature sizes, it allows compact circuits and higher integration. However, there are several factors that degrade analog circuit performance as technology advances, such as, lower supply voltage, lower transistor breakdown voltage and transistor intrinsic gain (*gm.ro*), and also higher mismatch between transistors and gate leakage current [2.36]. A survey of various state of the art CMOS circuits suggests several design methodologies and techniques that can be adopted in the FM-UWB transceiver design to improve performance and reduce power consumption. Keys principles of low power circuits are:

- Bias CMOS in the sub-threshold region [2.37].
- Increase amplifier gain by improving its output impedance (e.g., gain boosting and Q-enhancement techniques [2.38], [2.39]).
- Maximize headroom, i.e., use lowest possible V_{DD}, or apply the current reuse technique [2.14], [2.40].
- Power management by adjusting power consumption or shutting down circuits according to environmental condition or periodically (i.e., duty cycling) [2.41], [2.42].
- Design systems that requires relaxed subsystem performance or fewer building blocks for a given functionality (e.g., low complexity and non-coherent radio) [2.10], [2.43].
- Use digital circuits and calibration to compensate for non-idealities (e.g., offset, mismatch, non-linearity, frequency error, or temperature drift) [2.44], [2.45].

Note that not all of these principles are applicable to the FM-UWB transceiver design. This list only offers guidelines that may be utilized when there is an opportunity.

2.7.1. Sub-threshold CMOS

Transconductance (*gm*) is directly proportional to voltage gain and bandwidth in amplifier circuits. The transconductance per unit of current (i.e., transconductance efficiency, a *gm/Id*) of a transistor is lower when operates at a higher current density (see Figure 2.13) [2.37]. Small signal unity current-gain frequency or transit frequency (f_T) intrinsic to the MOS device, so f_T cannot be arbitrary small for the device to operate at RF. Sub-threshold bias is a powerful tool when reducing power consumption, but as can be seen from Figure 2.13, the device is slower (i.e., operates at lower f_T). On the other hand, the CMOS transistor can be biased at maximum f_T but at the cost of power efficiency (i.e., requiring more current for a certain *gm*). As CMOS is scaled further and f_T increases in smaller feature CMOS,

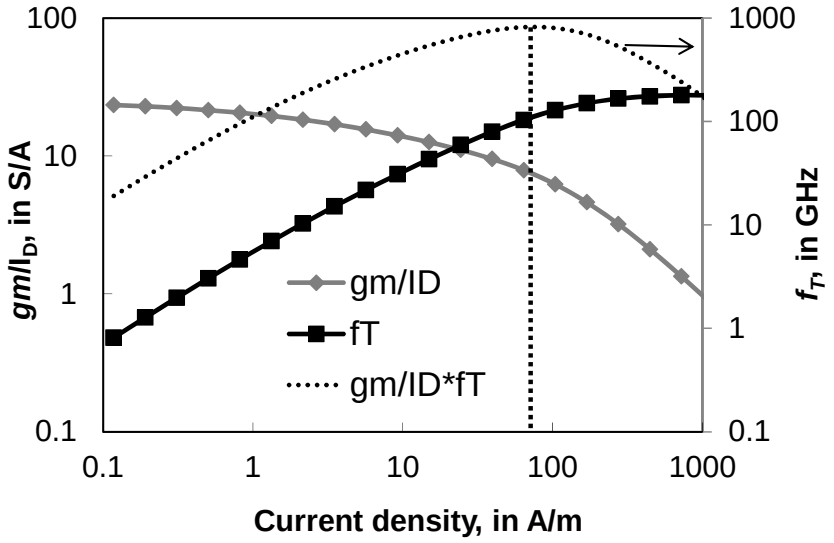

Figure 2.13. gm/I_D and f_T versus current density of NMOS device in 90 nm CMOS (W = 1µm, L = 90nm).

sub-threshold biased circuits should become a viable technique for RF circuits implementation.

Figure 2.13 shows gm/I_D and f_T versus current density of an NMOS device (Width is 1 µm and Length is 90 nm) in CMOS 90 nm technology. The current density at the peak f_T of 160 GHz for a 90 nm NMOS device is 0.8 mA/µm. The optimum trade-off (i.e., maximum product of gm/I_D and f_T) can be achieved at current density of around 80 µA/µm [2.46].

2.7.2. Gain boosting or Q-Enhancement technique

Gain boosting is a technique that increases the voltage gain of a single-stage amplifier by increasing its output impedance. This technique is suitable for low power circuits, because the cost of boosting is smaller than the power consumed by adding extra stages. At low frequency, output impedance can be boosted by adding an auxiliary amplifier in the negative feedback configuration [2.38]. Typically, a passive inductor is used at the output in a resonant tank to provide an output impedance of on the order of few kΩ at RF. Positive feedback could also be used to boost the output impedance in the resonant tank (i.e., Q-enhancement), at the risk of instability [2.39].

A simplified RF common-source amplifier (shown in Figure 2.14) has a voltage gain that can be described as

$$A_V = gm_n \times Z_L, \tag{2.11}$$

where gm_n is the transconductance of the NMOS (M_N), and Z_L is the impedance of the LC tank. The amplifier is a bandpass amplifier where maximum gain is attained at the resonant frequency of the tank. At RF, the on-chip inductor usually

determines the tank Q-factor. Many efforts have been made to improve quality factor of inductor on chip [2.47]. On-chip inductors of several nH and Q of more than 10 in the GHz range are now practical. Losses can be approximated as a lumped resistor. A negative resistor synthesized using active device will cancel this loss. Effectively, the Q of the lossy component is enhanced by the active circuit at the cost of power consumption. The negative resistance is realized using a feedback that reverses the signal phase (i.e., positive feedback) [2.49].

A radio frequency receiver typically receives a weak incoming signal, hence the need for amplification at RF. The Q-enhancement technique boosts the gain at low bias currents by operating the amplifier transistor on the verge of instability. For example, the closed-loop transfer function of the positive feedback amplifier shown in Figure 2.15(a), with forward path gain A and feedback factor β, is given by

$$H_{cl} = \frac{A}{1 - A\beta}. \tag{2.12}$$

The gain increases as loop gain (Aβ) approaches unity, but the bandwidth decreases as the gain-bandwidth product is approximately constant as illustrated in Figure 2.15(b) [2.50].

Such a regenerative amplifier (i.e., an amplifier with positive feedback) is employed in Armstrong's regenerative FM radio receiver shown in Figure 2.16. Here, the FM signal is received by the antenna, and transformer coupled into the grid leak (analogous to the CMOS transistor gate) of the tube. The output signal is fed back through the 'tickler', which is coupled to the input transformer in a positive feedback fashion. By adjusting the tickler input transformer distance, the

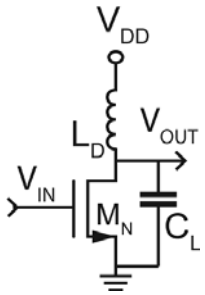

Figure 2.14. Schematic of a single stage RF amplifier.

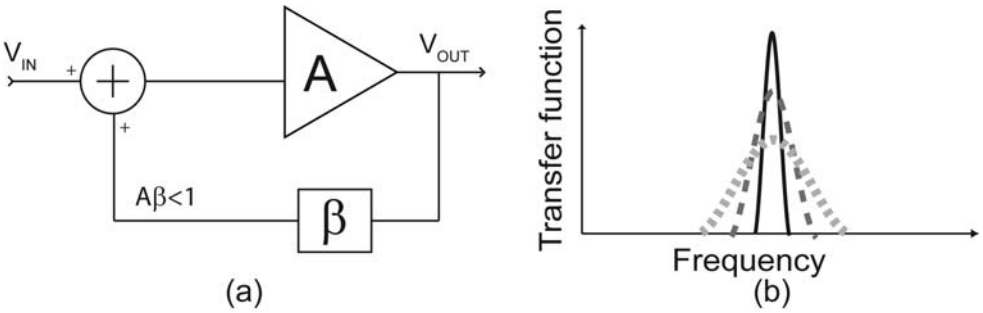

Figure 2.15. Positive feedback (a) block diagram and (b) transfer function.

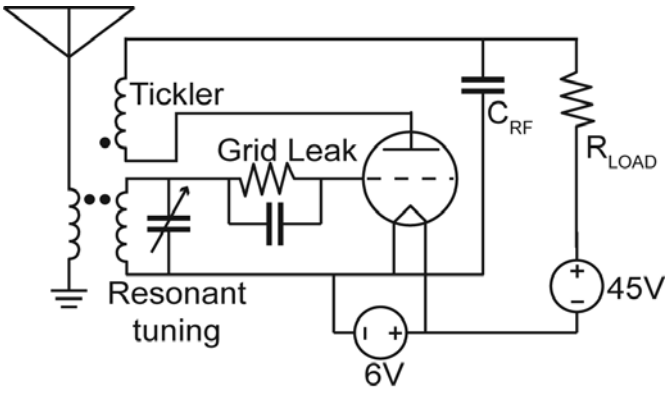

Figure 2.16. Armstrong's wireless FM receiving system [2.48].

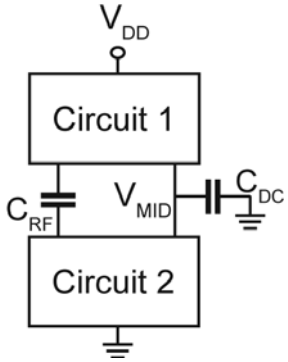

Figure 2.17. Illustration of current reuse for 2 circuit blocks.

positive feedback and hence the gain of the amplifier can be adjusted.

2.7.3. Maximum Voltage Utilization

In low power circuits, the available voltage or "headroom" is a precious resource. A single supply voltage is usually used, and all the circuits on the IC must utilize it. Individual circuits block may have different optimum supply voltages, but the highest voltage requirement usually sets the overall supply. This creates compromises efficiency as not all the circuits utilize the headroom. A multi-voltage supply increases complexity, size, and cost of the power management sub-system required for implementation.

Cascoding circuit blocks is an obvious way to reduce current consumption as illustrated in Figure 2.17. However, the designer must ensure that unwanted coupling between blocks is avoided and also to regulate the voltage supplying each sub-circuit connected between the supply and ground. For example, a 2-stage RF amplifier can re-use the bias current that consumed in both amplifier stages by cascoding the bias path [2.14]. The signal and DC paths are separated by inductor/capacitor networks. In [2.40] the VCO uses the bias current of other RF blocks to save overall power consumption. Stacking more than one circuits is possible (a VCO and a 2-stage PA [2.40]), but requires circuit topologies that

operate properly at a reduced supply voltage. Ultra-low voltage (< 0.5 V) circuit techniques are useful if they can be stacked easily to ultimately reduce power consumption. A CMOS RF receiver, analog filter and opamp topology for ultra-low supply voltages have been proposed in [2.51], [2.52].

2.7.4. Adaptive power control

Adaptive power control is an obvious technique that leads to reduced power consumption for the transceiver circuit. There are various ways of controlling the power that can be classified as duty cycling and adaptive biasing. Duty-cycling is turning on and off the transceiver periodically to scale power consumption with respect to data rate, available data or power source. Adaptive biasing changes the bias level in the transceiver according to channel conditions, e.g., reducing the receiver sensitivity and/or transmitted power when the received signal is strong.

A higher data rate transceiver usually has the advantage in term of energy efficiency per bit [2.53]. Duty cycling assumes that the data rate could be scaled easily without any penalty (i.e., to maintain energy efficiency). However, there are limitations when applying duty cycling in the transceiver, as extra time is required between on and off states to prepare the supply, bias, reset, etc. Hence, duty cycling at rates less than the order of once per microsecond is usually not effective. Reliability of transmission for a concentrated data burst is a problem if fading occurs. This is aggravated at very low duty cycles (< 0.1%), where all the data transmitted in a very short time. There is also a delay (latency) when duty cycling is applied that could pose a problem in medical applications, for example.

There is also a need for time synchronization or rendezvous between a duty-cycled transmitter and receiver (i.e. transmitting and receiving in agreed time). Several rendezvous schemes have been proposed in [2.54] that complicate the system as they requires a clock accuracy better than 1% [2.55] and might require an extra wake-up receiver. The rendezvous scheme also prone to channel fading [2.54].

Adaptive biasing schemes that change the dynamic range adaptively based on the channel conditions could be applied in the transceiver to reduce power consumption [2.56]. Also, circuits like the class-AB amplifier stage that change the current bias automatically with the signal amplitude could be used [2.57]. There is a trade-off between DC power consumption and sensitivity in the receiver and output power in the transmitter. Hence, optimum power consumption is realized at a certain link distance [2.58].

2.7.5. Low complexity transceiver

Low power can be achieved by simpler hardware at the cost of a performance, such as lower data rate or sensitivity. For example, a receiver that does not need a low NF does not require the LNA [2.59]. A super-regenerative scheme simplifies the receiver design by only using one oscillator [2.60]. Alternatively, a modulation scheme might be devised that accommodates simpler hardware such as the aforementioned FM-UWB modulation scheme [2.10].

Hardware requirements could also be simplified using non-coherent detection. Coherent detection implies that the receiver must know the carrier phase, and this information is obtained through synchronization. Tracking the received RF signal

requires additional hardware (i.e., using a PLL), and usually involves circuits that consume power [2.61]. Non-coherent detection does not require a local oscillator.

In some modulation schemes, the carrier phase is irrelevant and therefore locking carrier is not necessary. In this case, non-coherent detection is possible although there is some penalty in sensitivity. It is generally thought that performance of a coherent receiver is superior to non-coherent in a typical additive white Gaussian noise environment. In reality, wireless communication signals are affected by fluctuations of amplitude and phase due to frequency-selective fading. Additionally, in close proximity links such as a WPAN, sensitivity is not critical.
Some advantages of the non-coherent detection are [2.62]:

1. Better performance in fast frequency selective fading, large Doppler spread, strong phase noise, or co-channel interference.
2. No time delay for resynchronization
3. Simpler hardware (no PLL)

There are 3 categories of non-coherent detection [2.62]:

1. Energy detector (e.g., OOK system using envelope detector)
2. Orthogonal signaling (e.g., FSK receiver, where signals are orthogonal irrespective of carrier phase)
3. Differential (use the current carrier phase to decode the phase difference relative to the next symbol).

2.8. Summary

In this chapter, wireless modulation schemes that suitable for low power consumption are described. As discussed before, it is attractive for the autonomous wireless device to utilize the available unlicensed UWB spectrum. Hence, the FM-UWB scheme with its advantages and limitations will be the main focus of this thesis. The emphasis is made on realizing an energy efficient FM-UWB transceiver that satisfies the specifications listed on Table 2.1, therefore improving upon existing FM-UWB transceivers.

Various low power techniques have been summarized and will be utilized where possible. For example, the possibility of using regenerative amplifier along with an envelope detector in the receiver will be investigated. This results in a narrowband receiver that has simple architecture, but requires wideband tuning to process an UWB signal. A non-coherent detector will be implemented for the FSK demodulator for the receiver. An analog relaxation oscillator should be able to generate triangular wave at a lower power consumption than the aforementioned DDS circuit. Class-AB and current reuse technique should be employed in PA stage, which is usually the most power hungry block in the wireless transmitter. On the system level, a power management circuitry is needed, especially if the transceiver relies on an intermittent power source such as a power harvesting device.

The following chapter will describe the proposed FM-UWB transmitter prototype realized in 90 nm CMOS.

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CHAPTER 3. FM-UWB TRANSMITTER

3.1. Introduction

The RF transmitter contributes a significant part of the power budget in an FM-UWB wireless transceiver system. The RF blocks, namely RF oscillator and PA, usually consume the most power in the transmitter chain (up to 80%), and therefore should be designed to be as power-efficient as possible. Fortunately, using FM-UWB relaxes the phase noise requirement on the transmit oscillator [3.1], [3.2] (see Section 2.5). With no synchronization or PLL block required, it gives the designer the opportunity to build a simple and low power RF transmitter prototype, where most of the building blocks are integrated on-chip.

Based on the specifications listed in Table 2.1, a ring oscillator topology is chosen as a carrier generator. It is followed by a power-optimized power amplifier, instead of simple buffer. Additionally, calibration circuitry is added to compensate for PVT variation. Baseband and bias circuits are included on the chip which eases characterization.

The FM-UWB transmitter building blocks and their design are described in Section 3.2. Measurement results of the prototype realized in 90 nm bulk CMOS are presented and discussed in Section 3.3. A comparison with other low-power FM-UWB transmitters from the recent literature is presented in Section 3.4 of this chapter.

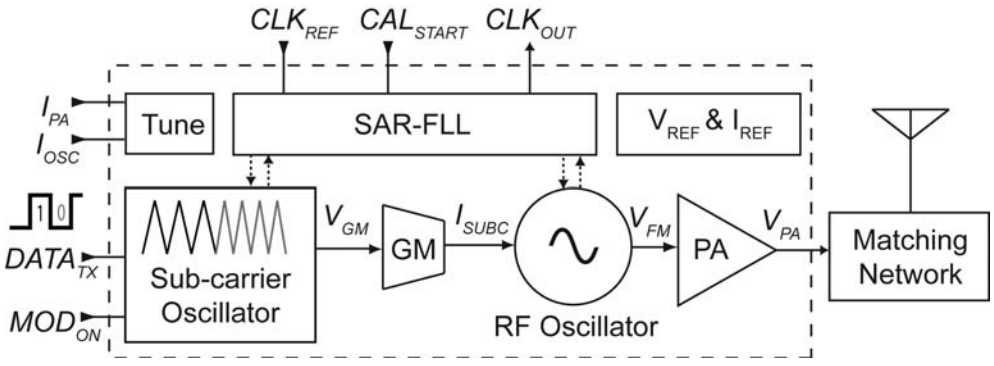

Figure 3.1. Proposed FM-UWB Transmitter [3.2].

3.2. FM-UWB Transmitter circuit designs

The proposed fully-integrated FM-UWB transmitter is shown in Figure 3.1. A current-controlled ring oscillator (ICO) is the source for the RF carrier. The transmit signal is buffered and amplified by a multi-stage power amplifier that drives the antenna through an external matching network. The triangular sub-carrier is generated using a relaxation oscillator, where the triangular oscillator output voltage is converted to a current by transconductor, GM. An on-chip successive approximation register frequency-locked loop (SAR-FLL) calibrates the sub-carrier and RF oscillator frequencies. Voltage and current references are also implemented on-chip to generate supply voltage and temperature insensitive references, and for general biasing. External (analog) currents can also be injected for testing and characterization purposes through CMOS current mirrors (i.e., I_{OSC} for tuning the ICO output frequency, and I_{PA} for changing the PA output power).

The prototype FM-UWB transmitter is implemented in 90 nm bulk RF-CMOS with thick metal and metal-insulator-metal (MIM) capacitor options [3.3]. The all-copper interconnect scheme (from bottom to top of the stack) consists of 5 thin, two medium-thick, and one thick top metal.

3.2.1. RF Carrier Oscillator

Well-known for its simplicity, compact physical layout and wide tuning range, a ring topology is chosen for the RF transmit oscillator. The ring oscillator benefits from technology scaling because its power consumption decreases as the supply voltage and transistor sizes are reduced. Three stages are used in the ring to meet the

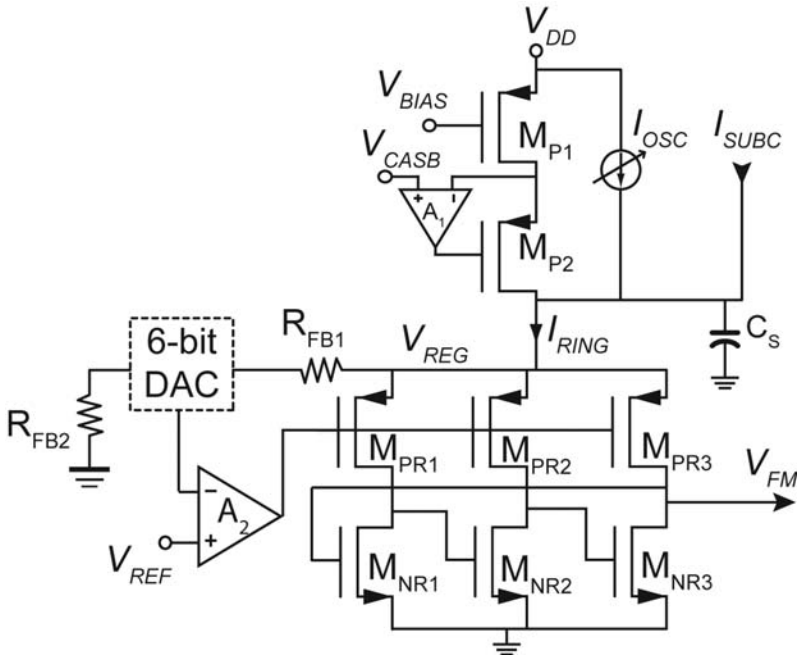

Figure 3.2. Current-controlled RF Oscillator (RF-ICO) schematic.

desired oscillation frequency with minimal power consumption, but at the cost of higher phase noise [3.4]. As mentioned before in the specification (section 2.5), the phase noise requirement of the RF oscillator is relaxed, and thus ring oscillator is a suitable topology. Tuning of the control current is independent of the supply voltage, making the current-controlled oscillator (ICO) less susceptible to noise present on the supply or ground lines, and improving its portability between advanced technology nodes, where further scaling of the supply voltage is anticipated.

Each stage of the ICO consists of a NMOS driver with active PMOS load, as shown in Figure 3.2. Regulation of the ring oscillator supply desensitizes it to external variations in supply voltage, V_{DD}. The PMOS (M_{PR1-3}) source voltage (V_{REG}) is regulated at 0.7 V by opamp A_2 via a feedback loop that derives the

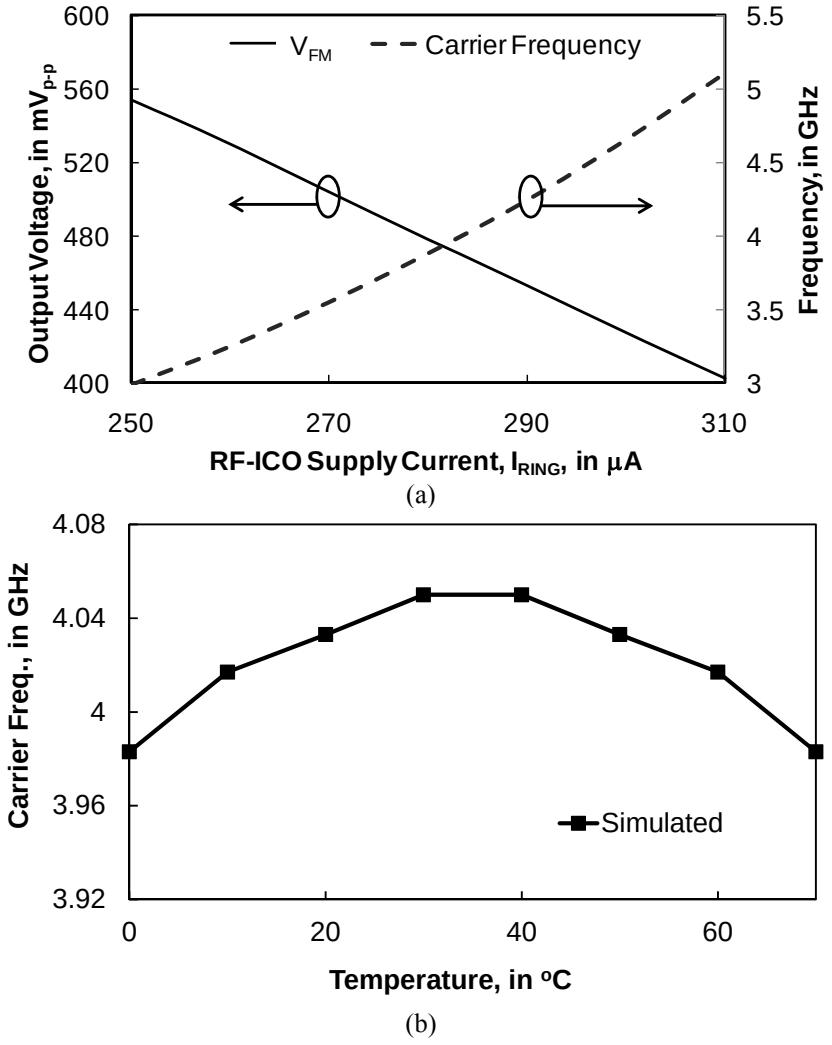

Figure 3.3. Simulated (a) frequency and amplitude of the RF-ICO versus current bias, and (b) frequency versus temperature.

desired supply-voltage using temperature-compensated voltage reference, V_{REF}. The opamp bandwidth must be at least ten times larger than the sub-carrier frequency for proper regulation of the ICO supply. The ICO output frequency (f_{osc}) is tuned by current I_{RING}, which is the sum of the bias current from M_{P1}, the external tuning current I_{OSC}, and the sub-carrier modulation current I_{SUBC}, all of which are supplied by PMOS current sources. The current sources are implemented in parallel from a high ratio (> 100) current mirror, hence their output impedance is low. Feedback amplifier A_1 enhances the current sources' output impedance, improves current mirror accuracy, and yields 65 dB power supply rejection from DC up to 10 kHz.

The ICO is a current starved design [3.5]. The rise/fall time of each stage is slew rate limited. The output frequency (f_{osc}) for the 3-stage ring oscillator may be estimated from

$$f_{OSC} = \frac{I_{RING}}{6C_G |V_{FM}|}, \tag{3.1}$$

where C_G is the total capacitance seen at all the NMOS gates (including Miller effect) and $|V_{FM}|$ is the output voltage swing. The voltage swing decreases slightly as the frequency increases (see Figure 3.3a). As the loop gain decreases with increasing frequency, the output swing settles at a lower peak-to-peak voltage. Equation (3.1) predicts that I_{RING} is linearly proportional to f_{osc} for constant $|V_{FM}|$, however, there is non-linearity caused by slight changes in $|V_{FM}|$. Another advantage of tying f_{osc} to the current reference is that it can be made temperature insensitive. Simulation results shown in Figure 3.3b indicates that the ICO temperature sensitivity is 1.25 MHz/ºC.

The aspect ratios (W/L) of the transistors in each stage of the ICO are scaled progressively by a factor of two in order to increase the current driving capability at output, V_{FM}. Scaling also balances the overall capacitive loading on each stage, thus optimizing oscillation frequency. RF carrier power increases from the first to third stages, while the voltage swing in each stage remains constant. The 1 pF decoupling capacitor (C_S) showed in Figure 3.2 acts as a charge reservoir which reduces fluctuations in the node voltage V_{REG}, and also filters out high frequency supply noise. A 6-bit resistor-DAC is used to tune the ICO frequency during calibration by adjusting V_{REG}.

The ICO (incl. opamps and bias circuits) consumes 280 µA of DC current when it is oscillating at 4 GHz. A change in the tuning current of 15 µA causes 500 MHz deviation in the RF output, resulting in a tuning sensitivity of 33 MHz/µA.

3.2.2. Power Amplifier

The largest proportion of the total transmitter power is dedicated to the power amplifier (PA) in order to maximize the link span between transmitter and receiver. FM-UWB produces a constant envelope RF signal that enables the PA to operate at its maximum power output where its efficiency is highest. The output power of the transmitter is adjusted via the bias current I_{PA} (see Figure 3.4), which controls the bias of the last stage. Separate bias voltages reduce coupling between stages and avoid self-oscillation in the multi-stage amplifier (biasing circuit not shown).

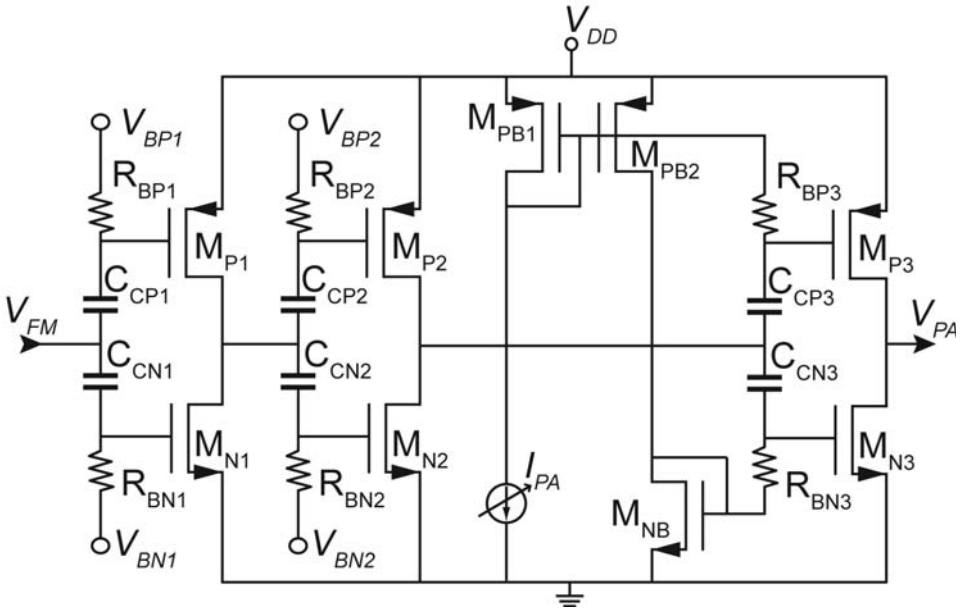

Figure 3.4. The 3-stage class-AB power amplifier schematic.

The PA consists of 3 push-pull stages in cascade as shown in Figure 3.4, where each stage is biased Class-AB. Class-AB biasing increases the power efficiency by drawing peak current only during the charging phase. This comes at the cost of reduced linearity, which is less important as the carrier amplitude is approximately constant for FM-UWB. Additionally, the PA provides isolation between the antenna and the ICO, as a strong interferer at the transmitter output could cause unwanted pulling of the ICO frequency. The simulated reverse isolation is -61 dB below 10 GHz, although this result must be considered optimistic because parasitics from interconnect lines are not included in the simulation.

The RF signal is coupled from stage-to-stage through R-C bias-T networks (R_{Bx} and C_{Cx} in Figure 3.4). The multi-stage amplifier is scaled by 2.5 times from stage to stage, and the PMOS to NMOS scaling factor is 1.5. The gain per stage is 5 dB, and the (simulated) input power to the PA from the oscillator is -25 dBm, which is sufficient to drive the output stage into saturation (0.85 $V_{p\text{-}p}$ drain voltage) for maximum efficiency at targeted peak power of 100 µW. A matching network transforms the 50 Ω load impedance to the optimum load of 900 Ω for the amplifier output.

The PA consumes 750 µW when running at 4 GHz, and produces -10 dBm (maximum) output power into a 50 Ω load via the external LC matching network, which consist of a 6 nH shunt inductor and 0.3 pF series capacitor. The simulated peak power-added efficiency (PAE) of the PA is 12.9%.

3.2.3. Sub-carrier Oscillator

The 0.6-1.2 MHz triangular sub-carrier signal is generated by the relaxation oscillator shown in Figure 3.5. Current reference I_{REF} charges and discharges capacitor C_{SUB}, thereby generating a ramp voltage (V_{TRI}) across the capacitor. The

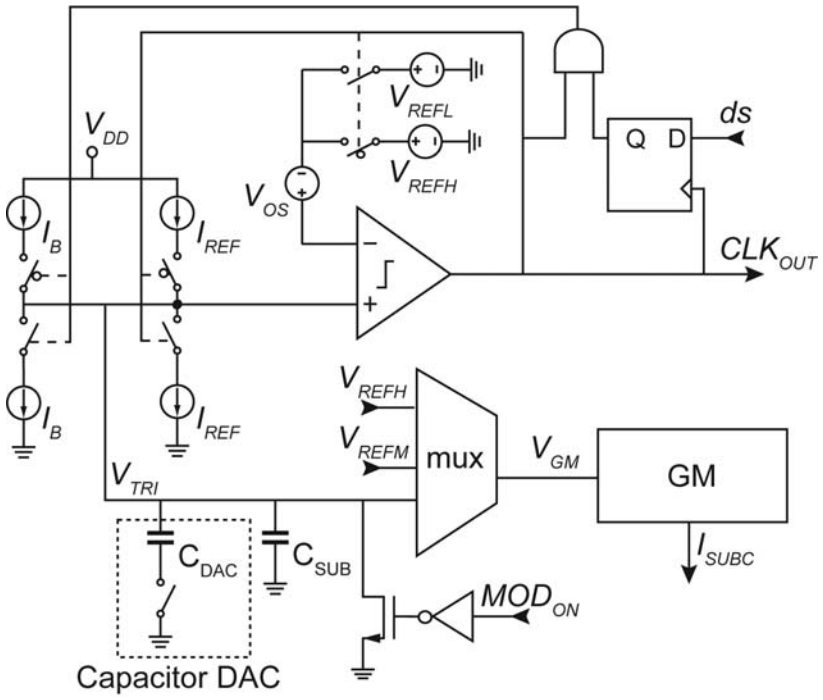

Figure 3.5. Sub-carrier oscillator schematic.

peak-to-peak amplitude of the ramp is determined by the upper (V_{REFH}) and lower (V_{REFL}) trigger points of the comparator, which determine the switching of the capacitor current between charge and discharge modes. The voltage across C_{SUB} (V_{TRI}) and the comparator output are set to 0 V initially in order to ensure proper startup of the triangle generator when the modulation is off. The input data stream (*ds*) modulates the frequency of the sub-carrier oscillator by injecting an additional current I_B (25% of I_{REF}) in parallel with I_{REF} into capacitor C_{SUB} when the input data is 'high'. A D-flip-flop synchronizes frequency shifts of the sub-carrier to occur only when the ramp generator toggles between charge and discharge modes.

The sub-carrier frequency (f_{SUB}) generated by the relaxation oscillator is given by

$$f_{SUB} = \frac{I_{REF} + (ds.I_B)}{2C_{SUB}(V_{REFH} - V_{REFL})}. \tag{3.2}$$

A linear (MIM) rather than a MOS capacitor is used to realize C_{SUB} in order to improve the linearity of the ramp generator output. There are other circuit imperfections that affect f_{SUB}, including: channel length modulation of MOS current sources, variation in the propagation delays of the comparator and control logic circuits, and variation in the capacitance value of C_{SUB}. Thus, a 6-bit capacitor-DAC in parallel with C_{SUB} is added to adjust the ramp capacitor value and tune the sub-carrier frequency with a resolution of 3.5 kHz, or within 0.2% of the desired sub-carrier frequency. As mentioned before, FM-UWB is non-coherent and only requires frequency accuracy on the order of 10^3 ppm (e.g., 5000 ppm [3.5]), or

about one order of magnitude poorer than the stability required to track the carrier phase in a coherent system.

Current I_{REF} and reference voltages V_{REFL} and V_{REFH} are derived from the same source in order to desensitize the circuit from process, supply voltage, and temperature (PVT) variations. This topology is also insensitive to the comparator offset (V_{OS}) because offset affects both upper and lower threshold voltages equally, and therefore offsets in the comparator reference voltages are cancelled as seen from equation (3.2). The amplifier input is initialized to V_{REFM} (mid-level between V_{REFH} and V_{REFL}) through a multiplexer (mux) when the modulation is turned off (i.e., MOD_{ON} = 0), allowing the RF-ICO to be calibrated at its desired center frequency. $V_{REFH,}$ which corresponds to maximum RF frequency deviation, can be selected through the mux to accommodate RF bandwidth calibration.

In the second version of the transceiver (see Chapter 5), a 9-bit capacitor DAC is implemented to extend the frequency range to 0.5-4 MHz. Also, an option to boost I_B to 50% of I_{REF} is included to increase the FSK frequency deviation, which will allow a higher data rate.

3.2.4. Transconductance amplifier

Transconductance amplifier A_0 translates the sub-carrier voltage to a current that modulates the transmit RF-ICO via feedback resistor R_{GM} (see Figure 3.6). R_{GM} is implemented externally, and is tunable to control the bandwidth of the wideband frequency modulation. Unfortunately, I_{SUBC} consist of a DC offset plus modulating current. If R_{GM} is tuned to increase bandwidth, the DC offset also increases, and shifts the center frequency of the ICO. A better solution requires a sink-source type of current output without DC offset, which is implemented in the second version and described in Chapter 5.

Amplifier A_0 is a 2-stage folded-cascode topology with 70 dB DC gain and 20 MHz unity-gain bandwidth. Wide bandwidth is required to reproduce the triangle wave with the desired fidelity (i.e., harmonics preserved). The output current source formed by transistors M_{P1} and M_{P2} is gain boosted by amplifier A_1 to improve the accuracy of the mirrored current and to enhance its low frequency output impedance.

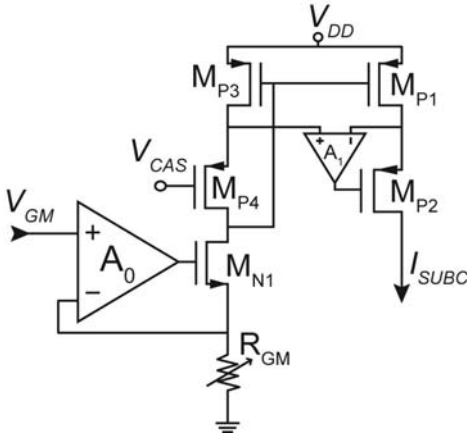

Figure 3.6. Transconductance amplifier (GM) schematic.

3.2.5. SAR-FLL Calibration

Simulations predict that the sub-carrier and RF-ICO center frequencies vary by up to 10% due to PVT spreads, and hence require calibration. The transmitter operating and sub-carrier frequencies are calibrated to 0.5% and 0.2% accuracy, respectively. A block diagram of the digital frequency-locked loop (FLL) used to set the initial carrier frequency is shown in Figure 3.7. It consists of a digital controller, a 12-stage frequency divider, a digital counter, a 6-bit successive approximation register (SAR), and a 6-bit DAC. A successive binary search algorithm is implemented that ensures convergence of the frequency tuning loop.

The calibration sequence is initiated when a pulse is applied to the positive edge-triggered CAL_{START} input (at t_1) and the controller (Dig. Control) resets the digital counter (at t_2), as shown in Figure 3.8. The digital counter integrates both the divide-by-2^{12} RF-ICO output (CLK_{OUT}) and the external reference clock (at t_3). A digital comparator senses the frequency difference (at t_4), and adjusts the RF-ICO frequency via the SAR and the DAC. N cycles of successive approximation (where N is the SAR resolution; N = 6 in this case) tunes the divided output of the RF-ICO to the external reference clock frequency. Note that the SAR cycles are not synchronous; a new SAR cycle starts when any of digital the counters reach a certain threshold. The counter threshold could also be made digitally programmable, if desired. To provide a programmable frequency ratio, a variable frequency

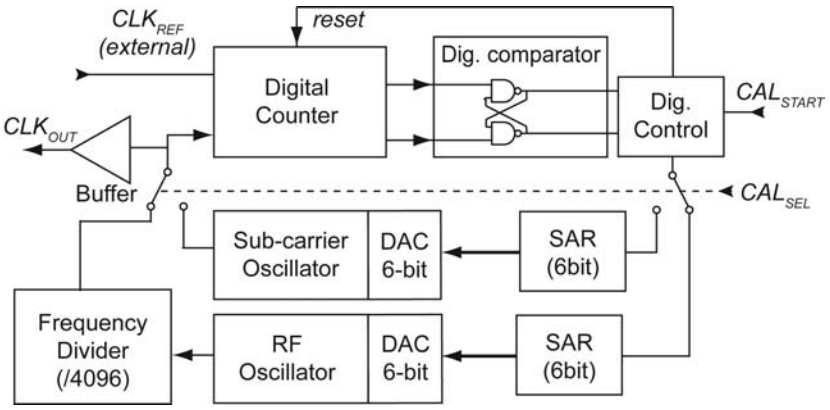

Figure 3.7. The SAR frequency-locked loop calibration scheme.

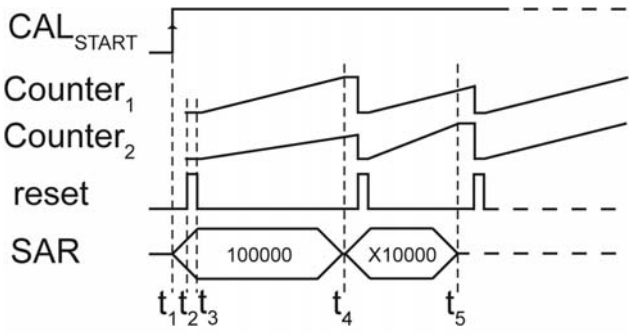

Figure 3.8. SAR-frequency-locked loop timing diagram.

external reference clock is assumed. The external reference clock would be sourced from the baseband digital processor in a wireless sensor application. Calibration requires 6 ms (i.e., 1 ms/SAR cycle) for a nominal 1 MHz external clock. The same calibration loop is also used to tune the sub-carrier oscillator by selecting the appropriate oscillator output and SAR input using the CAL_{SEL} switch.

The calibration setting is stored until another calibration sequence is initiated, which may be necessary if there are changes in the supply voltage or ambient temperature. Simulation predicts that calibrated frequency accuracy is within 1.5% when operating at supply voltage of 0.9-1.1 V, and within 2.5% when operating at a temperature of 0-80 ºC.

The RF divider is implemented using a cascade of 12 D-flip-flops, as shown in Figure 3.9a. The first 6-stages are implemented using the true, single-phase clock (TSPC) flip-flop [3.7] shown in Figure 3.9b, while the remainder are conventional CMOS pass-gate flip-flops [3.8]. Using only a few transistors and precharged nodes, the TSPC flip-flop is suitable for dividing a high frequency (above 50 MHz) periodic (i.e., clock) signal. At lower frequencies, charge leakage from the precharged nodes affects reliability of the divider output. The frequency divider is

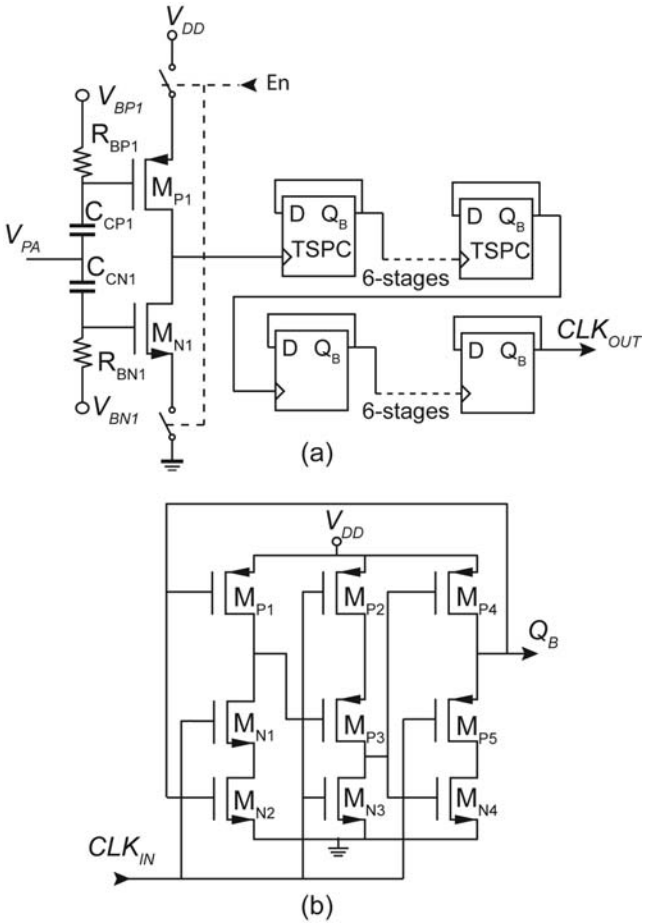

Figure 3.9. (a) Frequency divider, and (b) TSPC divide-by-2 circuit schematic.

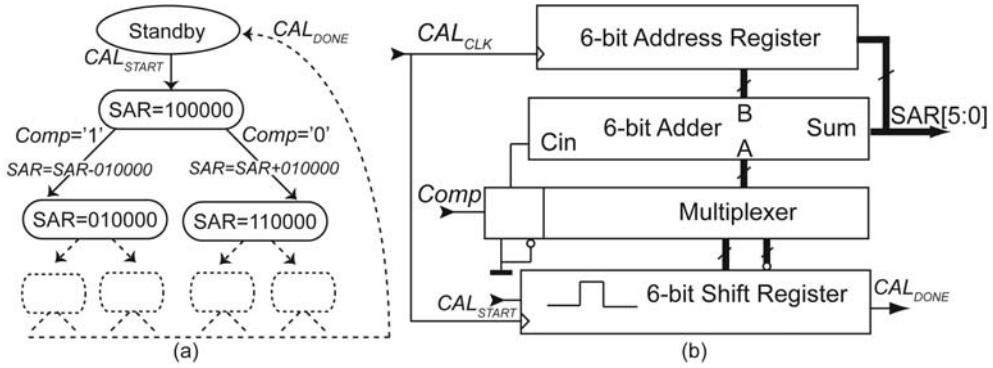

Figure 3.10. SAR state (a) and block (b) diagram.

active only during the calibration process, and it consumes 35 μW when running continuously.

The SAR is controlled by a state machine as shown in Figure 3.10. The bits that are stored in the SAR are the state address. When calibration begins, the SAR address is initialized with an MSB trial. The MSB is kept at logic '1' or changed back to logic '0' depending on the digital comparator result (*Comp*). The state address is changed progressively from MSB to LSB. A 6-bit shift register generates a traveling pulse which marks which bit need to be changed. It is initialized with the CAL_{START} signal and produces a CAL_{DONE} output signal when the calibration cycle is finished. The state address is changed by arithmetically adding (or subtracting) the current address to the marker address from the shift register. Subtraction is implemented using adder circuitry and two's complement arithmetic. A multiplexer is employed to select between the non-inverted or inverted bits, which effectively decides the sign of the result based on the *Comp* state. Asynchronous calibration clock (CAL_{CLK}), generated when each SAR bit is decided, drives the state machine. Using an asynchronous clock speeds up the calibration process [3.9].

The SAR-FLL scheme employed here does not require precision components or high-speed circuitry. The measured sub-carrier FLL locking range is 580-750 kHz and 710-910 kHz for logic '0' and logic '1' input data, respectively. The carrier frequency generated by the RF-ICO can be locked between 3.4-4.8 GHz by the FLL with a resolution of 20 MHz, which is sufficient for communication between transmitter and receiver using the non-coherent FM-UWB scheme. In the second version of the transceiver (see chapter 5), the SAR-FLL also calibrates the RF bandwidth, ICO tuning range, and center frequency of the receiver.

3.2.6. Voltage and Current References

Circuits which supply current and voltage references are essential for highly-integrated systems on a chip, like the FM-UWB transmitter. The current and voltage references have to be well-controlled despite variations in the supply voltage, IC temperature and processing. They consist of a proportional to absolute temperature (PTAT) current generator and an inverse-PTAT current generator as shown in Figure 3.11. The PTAT current is generated by applying the difference in the

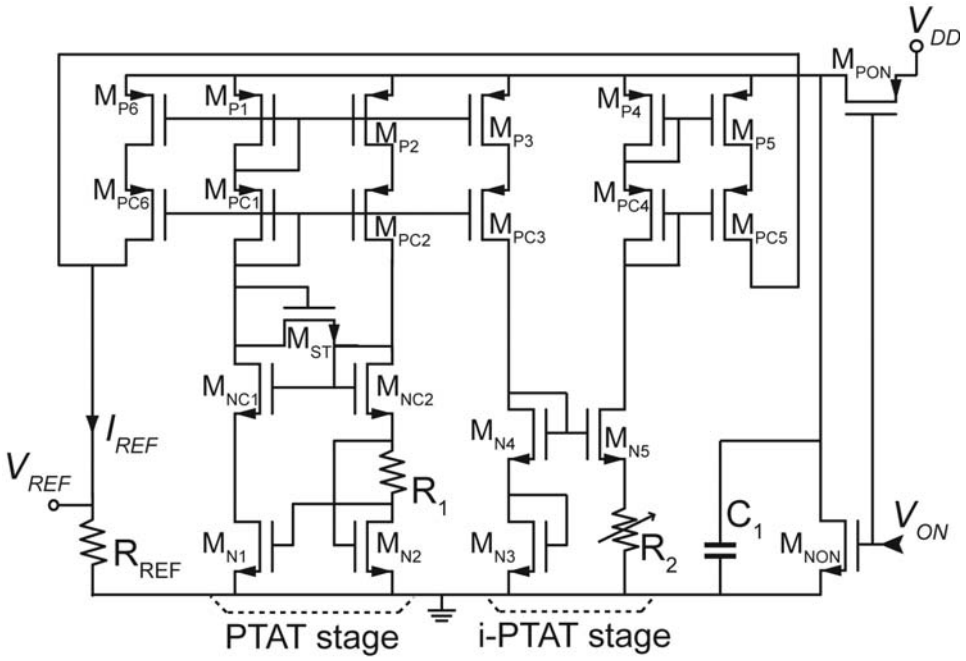

Figure 3.11. Schematic of built-in voltage and current references.

threshold voltage between different size NMOS transistors across polyresistor R_1, in a manner analogous to a conventional bandgap reference [3.10]. The inverse-PTAT is generated using an NMOS transistor's threshold voltage (with negative temperature coefficient of approximately -1.5 mV/ºC) dropped across polyresistor R_2. The reference current is given by

$$I_{REF} = \frac{V_{GS}}{R_2} + \frac{\Delta V_{GS}}{R_1}. \tag{3.3}$$

Voltage reference (V_{REF}) is derived from I_{REF} flowing through polyresistor R_{REF}. Note that any variation in the polyresistor value on the reference current value is cancelled as long as the resistors are matched (n.b., simulation models estimate 0.3% mismatch).

Resistor R_1 provides feedback to reduce the sensitivity of the current reference (I_{REF}) to supply voltage when operating at a 1 V supply. Capacitor C_1 filters any noise that comes from the supply voltage V_{DD}. Diode connected M_{ST} ensures that the biasing loop operates during startup, and automatically shut-off when the correct operating point is reached.

The simulated current variation due to ±10% changes in supply voltage is 1.5%. The simulated current variation due to changes in temperature is approximately 200 ppm/ºC at the nominal supply voltage of 1 V. These variations can be corrected (if required) by trimming or further calibration. In the second version of transceiver (see chapter 5), R_2 can be trimmed by 2-bit switches to minimize current variation

due to process variation. The reference circuit can be turn on/off by V_{ON} to reduce current consumption during times when the transmitter is inactive.

3.3. Experimental Measurement

The die photo of the transmitter prototype is shown in Figure 3.12. Note that the testchip is pad-limited, as some I/Os are used only for diagnostic/verification purposes. Area not required by the active circuitry is occupied by supply decoupling capacitors. Each pad is ESD protected using a standard library double diode cell that offers human body model (HBM) protection of 2 kV. On-chip inductors are not used in the design, giving a relatively small active area of just 0.1mm^2 (excluding bondpads). All measurement results presented in this section are for a packaged sample, where the test die is wirebonded to a custom printed-circuit board (PCB) and test fixture for characterization, as shown in Figure 3.13. The laminate used for the circuit board has a loss tangent of 0.004 at 5 GHz. A 50 Ω transmission line

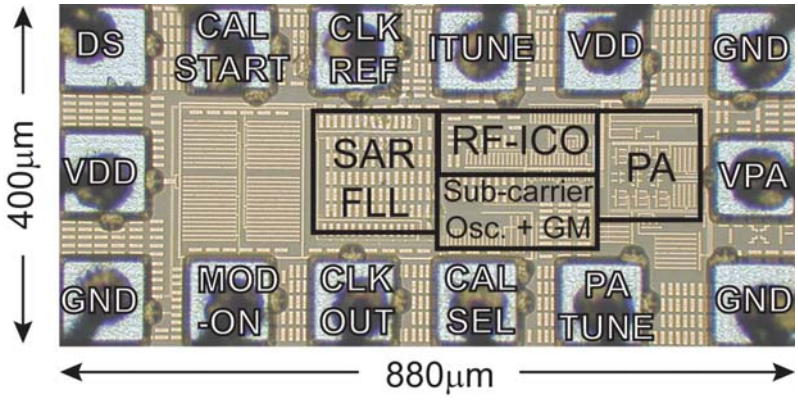

Figure 3.12. Chip micrograph of the FM-UWB transmitter.

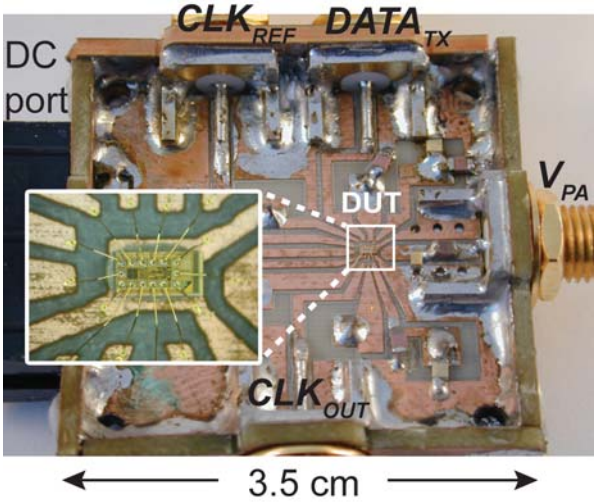

Figure 3.13. Assembled test PCB.

fabricated on this material has a (measured) insertion loss of 0.07 dB/cm at 4 GHz. Transmission lines are used to connect the IC to SMA connectors at the board's periphery. The bondwire length between the RF input on the chip and the PCB is approximately 1 mm, resulting in a series inductance of approximately 1 nH. The supply lines are filtered using 10 nF and 330 pF decoupling capacitors in parallel on the PCB side, as well as a 50 pF MIM decoupling capacitor implemented on-chip.

The measured RF spectrum with a resolution bandwidth of 1 MHz is shown in Figure 3.14. The unmodulated carrier power in this measurement is -14 dBm, and the spectral bandwidth of the FM-UWB output when modulated by the on-chip sub-carrier generator is 500 MHz with a peak power output of -41.4 dBm. The variation in RF output power across the FM-UWB spectrum is less than 2 dB. The maximum unmodulated output power is plotted versus frequency in Figure 3.15. There is some variation in the output power due to the matching network, however, across 500 MHz bandwidth the flatness in the response is within 1 dB, which is acceptable. The spectral flatness can be controlled by dynamically adjusting I_{PA} (see Figure 3.4) using a fraction of the sub-carrier current.

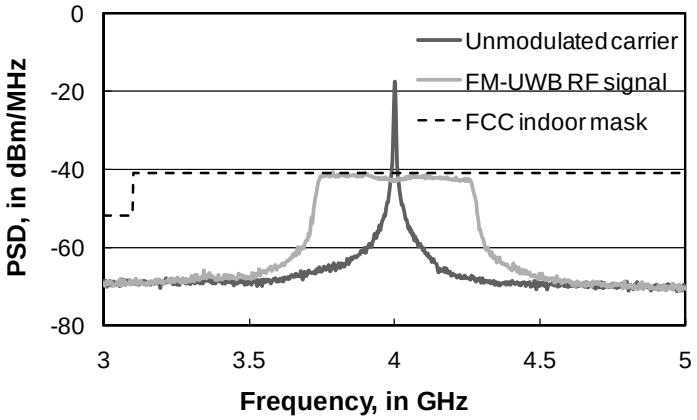

Figure 3.14. Measured transmitter output spectrum (unmodulated and modulated).

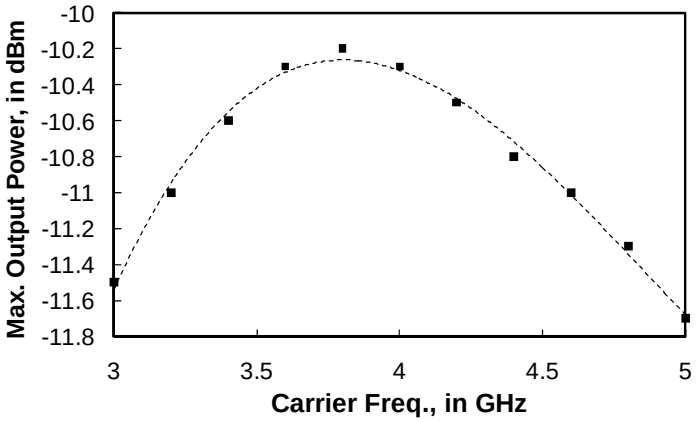

Figure 3.15. Measured maximum output power versus frequency.

Measured and simulated sensitivity of the carrier frequency to changes in supply voltage are plotted in Figure 3.16. The data shows that measurement and simulation agree well, and that the current-controlled tuning input is relatively insensitive to changes between 1 V and 1.1 V in supply voltage. The relationship between the RF carrier frequency and tuning current is plotted in Figure 3.17. The measured behavior is close to linear, as predicted by (1), but with a small non-linearity due to slight changes in the oscillation amplitude, which can cause non-uniformity in the power spectral density (PSD) at the output. Given that FM-UWB systems are more tolerant to multipath transmission effects (e.g., fading), which also affect the uniformity of the transmit PSD, the non-linearity is not expected to cause significant impairments. However, the output power might have to be reduced slightly in order to satisfy the -41 dBm/MHz transmit power regulation. The maximum measured oscillation frequency of 5.2 GHz is limited by the output swing of amplifier A_2 (see Figure 3.5). Figure 3.18 shows results from phase noise measurement of the transmitter at 4 GHz center frequency and -12 dBm output power. The resulting phase noise is -75 dBc/Hz at 1 MHz offset, which exceeds the specification of

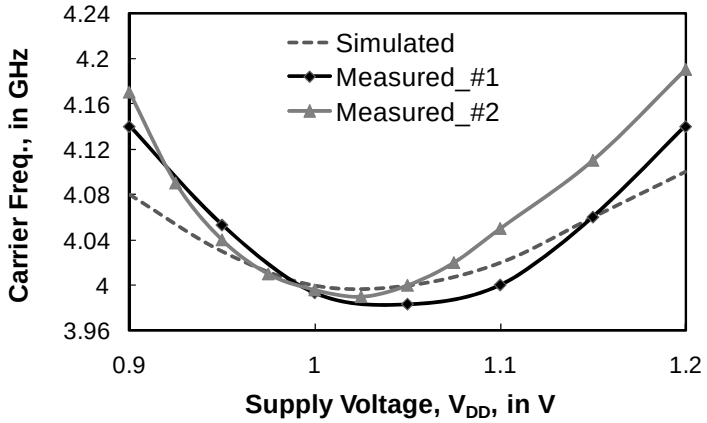

Figure 3.16. Carrier frequency vs. supply voltage, V_{DD}.

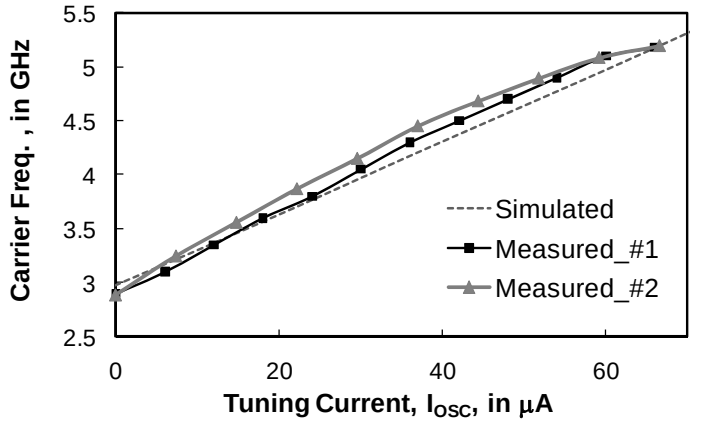

Figure 3.17.Carrier frequency vs. RF-ICO tuning current, I_{OSC}.

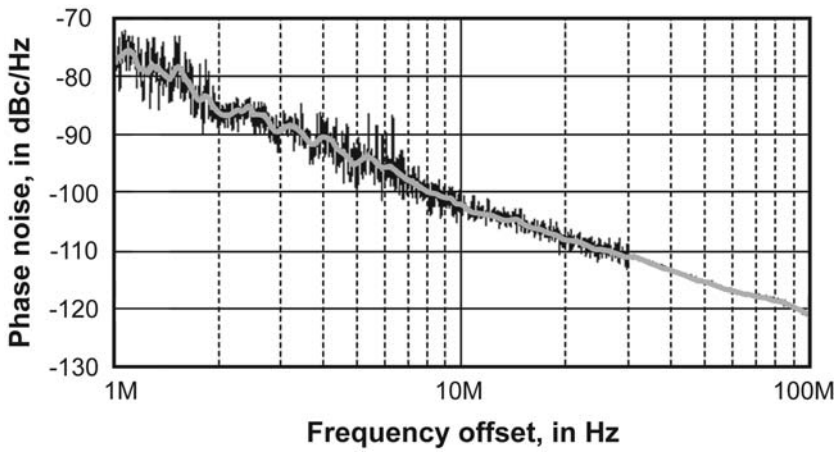

Figure 3.18. Measured phase noise of the transmitter.

-62 dBc/Hz. An advantage of the FM-UWB modulation scheme is that the oscillator phase noise performance can be relaxed, which lowers the overall power consumption of the oscillator and transmitter as a whole.

The measured performance of the FM-UWB transmitter is summarized and compared to other FM-UWB front-ends from the literature in Table 3.1. The transmitter consumes one-quarter of the power, but has a much higher integration level when compared to the other designs listed in the table. The energy consumption of the transmitter running continuously (i.e., not duty-cycled) at 4 GHz (center frequency) is 9 nJ/bit at a data rate of 100 kbit/s. The maximum overall power efficiency (RF output power divide by total DC power) of the full transmitter is 9.1%. Compared to the other FM-UWB transmitters, the IC developed in this work integrates all self-calibration, voltage and current reference circuits on-chip

TABLE 3.1 FM-UWB TRANSMITTER PERFORMANCE SUMMARY

Parameters	**This work**	**[3.11]**	**[3.12]**	**[3.13]**
Technology	90 nm CMOS	180 nm CMOS	180 nm CMOS	130 nm CMOS
RF tuning range, in GHz	2.9-5.2	2.7-4.1	0.5-5	6.25-8.25
V_{DD}, in V	1	1.8	1.8	1.1
Phase noise, in dBc/Hz at 1 MHz	-75	-70	-75	-107
Max. output power, in dBm	-10.2	-34	-9	-5
Bandwidth, in MHz	500	-	550	550
Sub-carrier frequency, in MHz	0.8	-	1	1
Data rate, in kbit/s	100	100	100	100
Power consumption, in mW	0.8-1.1	7.2-14	2.5-10	4.6
Active area, in mm^2	0.1	0.7*	0.25*	0.062
Energy efficiency, in nJ/bit	8-11	72-140	70-100	46

*Including bondpads

TABLE 3.2 LOW-POWER TRANSMITTER PERFORMANCE COMPARISON

Parameters	This work	[3.14]	[3.15]	[3.16]
Technology	90 nm CMOS	180 nm CMOS	130 nm CMOS	180 nm CMOS
Modulation	FM-UWB	OOK	BFSK	BFSK
Frequency, in GHz	4	0.9	2.4	2.4
Max. output power, in dBm	-10.2	-11.4	-5	-5.2
Data rate, in kbit/s	100	1000	300	125
Power consumption, in mW	0.9	3.8	1.12	1.15
Active area, in mm^2	0.1	0.27*	-	0.273
Energy efficiency, in nJ/bit	9	3.8	2.3	9.2
Power efficiency, in %	9.1	2.1	30	26.8

*Including Rx circuit

and consumes less power. Energy efficiency is also improved by approximately a factor of approximately 5 compared to the 0.13 μm CMOS design from [3.13].

3.4. Summary and Conclusions

FM-UWB offers efficient utilization of spectrum available for unlicensed use when the center frequency is well-controlled due to the shape of its transmit power spectral density. A fully-integrated FM-UWB transmitter for the 3-5 GHz band has been realized in a low-cost 90 nm bulk CMOS technology which benchmarks the scheme for potential low-power, short-range applications. The 0.35 mm^2 transmitter IC demonstrator consumes just 900 μW from a 1 V supply when operating at 4 GHz RF center frequency. A simple, low-cost and effective SAR-FLL calibration method was implemented to tune the center frequency of the FM-UWB transmitter. The nominal energy consumption of the transmitter is 9 nJ/bit at 100 kbit/s data rate in continuous operation, which is suitable for low data rate, portable wireless applications powered from a battery.

Table 3.2 compares the FM-UWB transmitters with other low-power transmitters. Energy efficiency in J/bit is an indicator of efficient design. However, applications such as data logging and monitoring require low kbit/s data rates that typically yield poor energy efficiency as it is inversely proportional to the data rate. Duty cycling could be applied to our FM-UWB transmitter (and other designs) to improve efficiency. Another performance indicator is output power efficiency, but it is also dependent on maximum transmitted power. Generally, BFSK transmitters [3.15], [3.16] offer higher transmitter efficiency using a tuned, narrowband output stage rather than a wideband (e.g., UWB) scheme which consumes more power. However, the narrowband FSK transceivers will require additional power to improve their robustness to multipath fading and to supply self-calibration and biasing circuits required on-chip to accommodate IC manufacturing, supply voltage

and temperature variations (included in our prototype FM-UWB transmitter). The FM-UWB transmitter designed in this work offers competitive energy efficiency at low data rates despite the overhead in power consumption associated with continuous operation. With on-chip calibration and a small chip area, the measured results establish FM-UWB as a viable alternative for short-range, low data rate wireless applications.

To further improve the transmitter's scalability, an all-digital architecture more amenable to scaling in future CMOS process generations could be applied [3.17]. Accurate temperature and voltage sensing circuits [3.18] with a digital look-up-table could be added to compensate for frequency drift due to changes in the supply voltage or temperature. A fully-integrated transceiver for FM-UWB including on-chip output power calibration is the next step in the development of a practical, low-power wireless transceiver for use in autonomous WSN, WBAN, and WMTS scenarios.

The next chapter will discuss the FM-UWB receiver prototype. The receiver uses the RF signal that generated by the FM-UWB transmitter described in this chapter for characterization purposes. Functionality of both the transmitter and receiver are validated from experimented measurements.

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CHAPTER 4. FM-UWB RECEIVER

4.1. Introduction

The FM-UWB receiver prototype described in this chapter will be experimenting with a positive feedback (i.e., regenerative) amplifier that will enhance RF gain (see Section 2.7.2 for detail). The amplifier is followed by an envelope detector to recover the IF sub-carrier. The RF signal must be amplified such that it can be detected by the envelope detector without limiting the sensitivity. The RF preamplifier typically consumes the largest portion (> 80%) of power in the receiver that employs an envelope detector [4.1]. The objective of the work in this chapter is to realize a power efficient receiver utilizing the advantages of the regenerative amplifier.

Power consumption of the receiver cannot be reduced arbitrarily due to the constraints imposed by operating frequency, gain-bandwidth product, and noise. Noise generated by the preamplifier limits the receiver sensitivity. The receiver sensitivity is (in general) proportional to transconductance (*gm*) of the preamplifier. As *gm* is also proportional to current and is directly related to power consumption, so the sensitivity is inversely (not linearly) related to power consumption. The receiver must be designed to meet the specification listed in Table 2.1, while consuming as little power as possible.

The operating principles of the proposed FM-UWB receiver are described in Section 4.2. Circuit design details of the receiver prototype and its operation are discussed in Section 4.3. Experimental measurements of the receiver prototype realized in 65 nm CMOS are then presented followed by a brief comparison with other FM-UWB receiver realizations in Section 4.4. A comparison with other low power receivers, and areas identified for future work are summarized in Section 4.5.

4.2. Proposed FM-UWB Receiver

An FM signal can only be detected indirectly (i.e., by converting it into phase modulation (PM) or amplitude modulation (AM) before detection) because physical

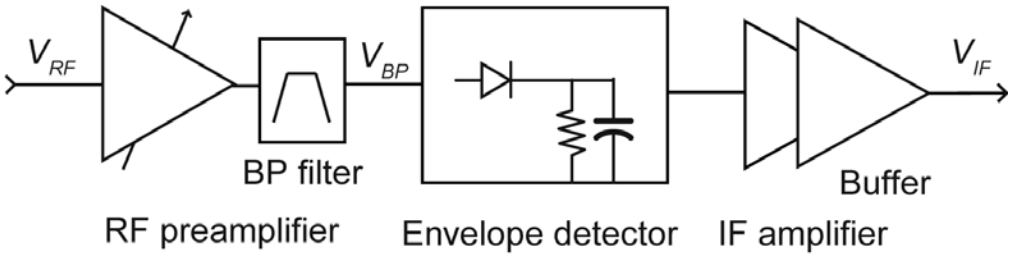

Figure 4.1. Proposed FM-UWB receiver front-ends.

systems are unable to read the instantaneous frequency of a carrier [4.2]. The conventional FM-UWB demodulator described in Section 2.6 first transforms FM to PM via a delay line with constant time delay, and then multiplies it with the original FM signal to yield an AM output.

In the proposed receiver, the FM-AM transformation is realized directly via an RF bandpass filter. Selecting a sub-band does not (ideally) affect the SNR of the received signal compared to processing the entire FM-UWB transmit signal. In fact, measurement of the prototype reveals that the received SNR and sensitivity for the sub-band FM-UWB receiver is on par with a conventional wideband receiver. However, the receiver RF amplifier is made more power efficient by processing a sub-band rather than the entire band. In contrast to conventional UWB receivers which receive the entire transmitted signal (including noise and unwanted interference), the receiver proposed in this work [4.3] (see Figure 4.1) is designed according to the cognitive radio paradigm [4.4], in that it selects and operates on a sub-band of the FM-UWB RF signal. Potential interferers may be avoided in this way, and the received signal-to-noise ratio (SNR) optimized to improve robustness by sub-band selection. The proposed receiver front-end consists of a transconductance RF amplifier and pulse-shaping RF filter followed by an envelope detector. An IF amplifier and output buffer are also included on-chip in order to facilitate characterization of the receiver front-end.

The FM demodulation process used in the proposed receiver is illustrated in Figure 4.2. The carrier is initially moving down in frequency between time t_1 to t_2 (Figure 4.2(a) and Figure 4.2(b)). The bandpass response of the RF preamplifier, which is tuned to f_C-Δf, detects and amplifies the carrier energy within its passband. Otherwise the carrier signal is attenuated. The narrowband response of the RF front-end therefore shapes the envelope of the received FM into an AM signal according to the bandpass response of the preamplifier. Amplification is highest when the carrier is centered in the passband (i.e., V_{IF} at t_3 in Fig. 4(c)), resulting in a peak in the amplitude of the demodulated signal. When the carrier is moving up in frequency (at t_4), the voltage at the IF output (V_{IF}) returns back to its original level. The carrier sweeps back and forth across the band at a rate determined by the (modulating) sub-carrier signal, resulting in a pulse train output at the IF. Setting the peak of the passband as shown in Figure 4.2 (i.e., close to the maximum deviation) maximizes the IF output amplitude. Note that if the passband is set to center

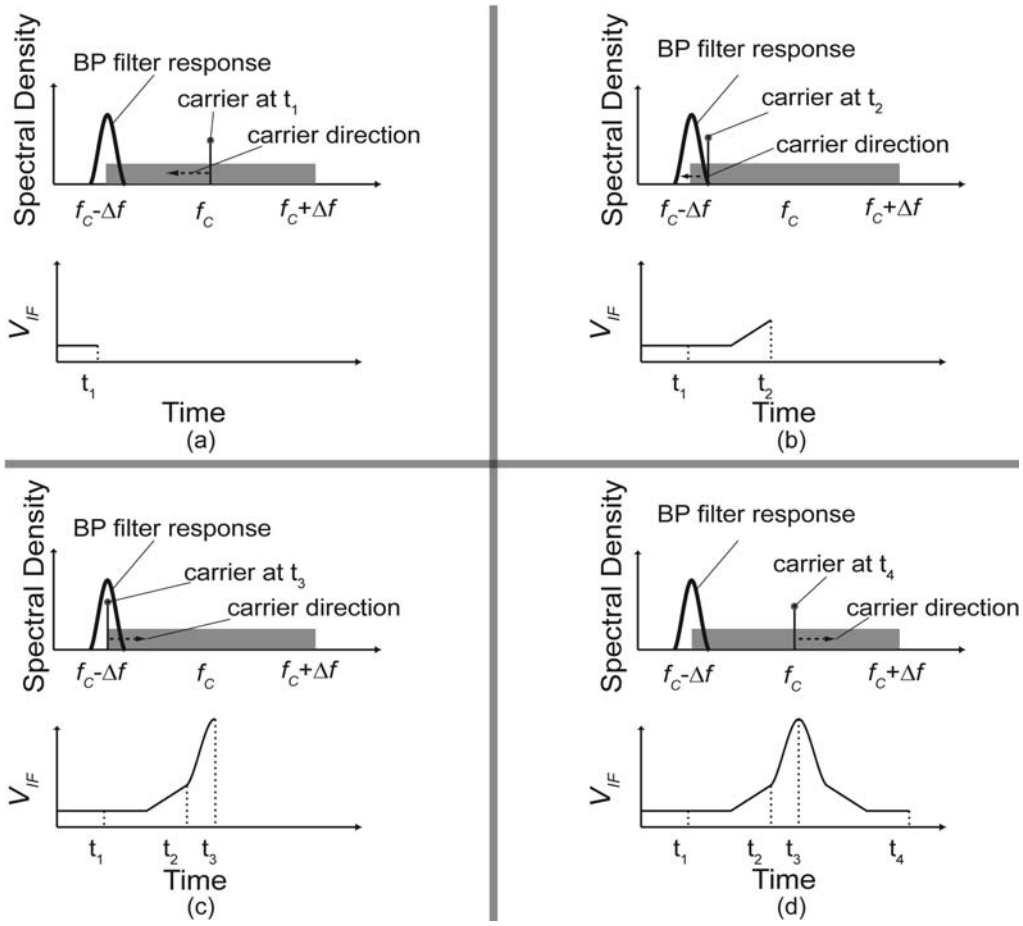

Figure 4.2. FM-UWB demodulation in sequence from: (a) t_1, (b) t_2, (c) t_3 and (d) t_4, with the bandpass (BP) filter response tuned to low side of the FM-UWB signal.

frequency f_C, the output pulse rate is at double the data rate. A divide-by-2 circuit is therefore required in the baseband processing circuits.

Tuning the bandpass filter center frequency adds complexity to the receiver, however, it also permits optimization of the SNR when interference and noise are present. An automated tuning scheme has not been implemented for this prototype, although calibration circuits that optimize the SNR and bit-error performance of the receiver could be devised and implemented on-chip. For example, in [4.5] an RF filter is tuned using a replica phase-locked loop, which has the disadvantage of possible mismatch between the filter and its replica. In [4.6]-[4.8], the filter is initially configured as an oscillator so that the center frequency can be detected and tuned using a digital control loop. After initial calibration of the center frequency, the gain is reduced to suppress the oscillation. In the second version of the receiver described in Chapter 5, this calibration circuit is included.

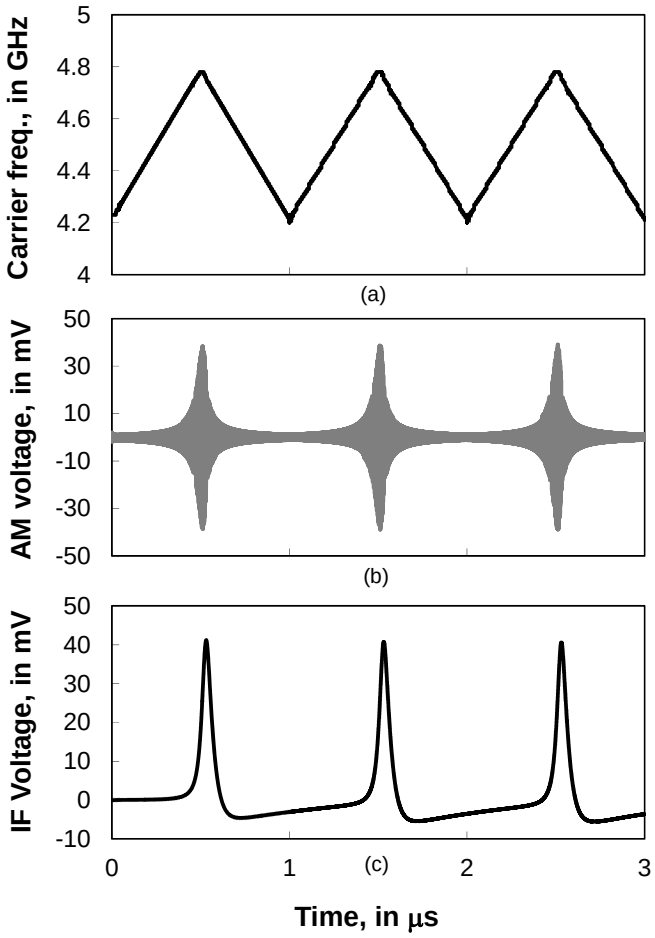

Figure 4.3. Signal transformation in the receiver chain: (a) input V_{RF} frequency, (b) AM signal at the preamplifier output, V_{BP}, and (c) detected output at IF, V_{IF}.

The demodulated signal (V_{IF}) is a periodic train of amplitude-modulated pulses. The shape of each pulse can be approximated as a Gaussian pulse g(t),

$$g(t) = e^{-\left(t^2/2b^2\right)}, \tag{4.1}$$

where the pulse width ($2b$) is proportional to the bandwidth of the bandpass filter. The periodic train of pulses can be obtained by convolving (4.1) with the following periodic train of impulses [4.9]

$$p(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT), \tag{4.2}$$

where T is the pulse repetition rate. This resulting periodic signal in time is given by

$$h(t) = \sum_{n=-\infty}^{\infty} e^{-(t-nT)^2/2b^2} . \tag{4.3}$$

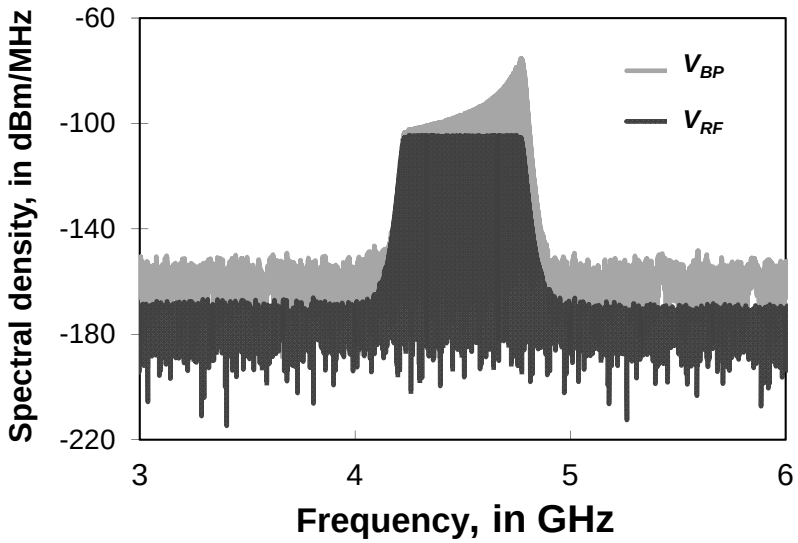

Figure 4.4. Simulated FM-UWB spectrum before (V_{RF}) and after the preamplifier (V_{BP}).

The Fourier transform of (4.3) yields the frequency spectrum of the filtered signal, which is:

$$H(f) = be^{-b^2 f^2/2} \sum_{m=-\infty}^{\infty} \delta(f - \frac{m}{T}). \tag{4.4}$$

Equation (4.4) predicts that the demodulated signal spectrum is also Gaussian, with a bandwidth inversely proportional to the width of the pulse (i.e., 2*b*). It also consists of many equally spaced spectral lines (1/T apart). Filtering can remove the higher harmonics while preserving the fundamental frequency of the demodulated signal. Choosing the sub-carrier frequency so that the harmonics do not interfere with each other is needed when the FM-UWB system employs more than one sub-carrier frequency at the same time (e.g., in a multi-user system).

Results from simulation of the proposed receiver chain are shown in Figure 4.3. The FM-UWB signal has 500 MHz bandwidth and the sub-carrier frequency is 1 MHz (f_C = 4.5 GHz and -80 dBm RF power). The top part of the figure shows the carrier frequency versus time. The preamplifier and narrowband filter convert FM into AM as shown in Figure 4.3(b), and the envelope detector produces the pulse IF wave as shown in Figure 4.3(c). The simulated power spectra of the input carrier signal before and after the pulse shaping RF preamplifier are shown in Figure 4.4. The filter center frequency is tuned at the edge of the FM-UWB band; hence, that edge sees greater amplification than the rest of in-band signal. The output signal is amplitude modulated (AM) in the time domain, as shown in Figure 4.3(b).

4.3. Circuit Designs

The prototype 4-5 GHz band FM-UWB receiver is designed and implemented in a bulk 65 nm bulk CMOS [4.10]. The back-end interconnect scheme in this technology includes: 4 thin copper (Cu) metal layers, 2 medium-thick Cu layers, and 2 thick-Cu top metal layers.

4.3.1. Regenerative Preamplifier and Filter

The input preamplifier should realize more than 30 dB RF gain at the lowest possible DC power consumption. It also requires good selectivity (i.e., 30 dB attenuation at 500 MHz offset) in order to select a 50 MHz sub-band. Positive feedback is therefore applied to the preamplifier to increase the voltage gain (but at the expense of lower bandwidth), thereby increasing its selectivity and sensitivity, as previously described in Section 2.7.2.

The regenerative preamplifier is shown in Figure 4.5. M_1 and M_2 form a differential transconductance amplifier, which drives the LC tank formed by L_D, C_{VAR} and the parasitic capacitances at the drains of M_3, M_4, M_5 and M_6. Inductor L_D is 2 nH, with a self-resonant frequency (f_{RES}) of 15 GHz and peak-Q of 14.2 at 5.9 GHz. C_{VAR} is an NMOS accumulation mode varactor, which ranges from 1.1 pF to 0.3 pF as V_{CAP} is changed from 0.4 V to 1.5 V. V_{CAP} tunes the center frequency of the load resonator with a range of 3.8 5.1 GHz. Cascode transistors M_3, M_4, M_7 and M_8 increase isolation between the RF input and output, while cross-coupled

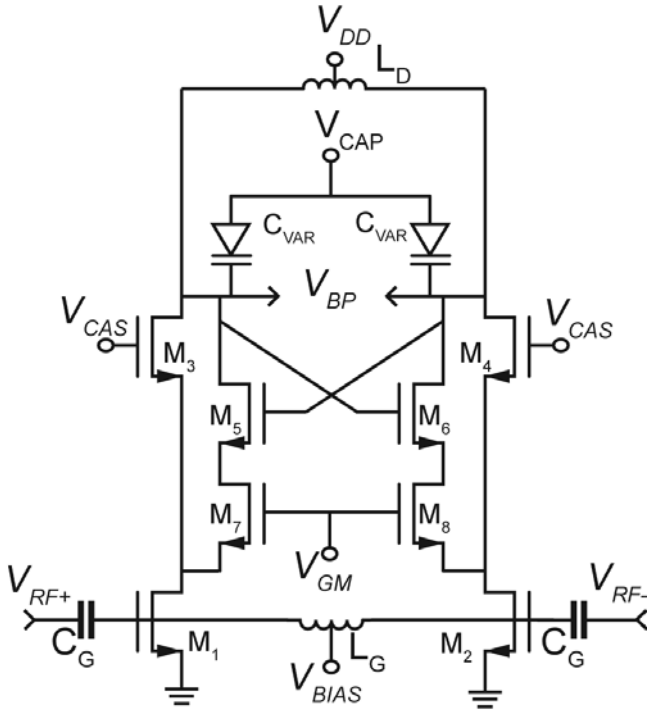

Figure 4.5. Simplified schematic of the RF preamplifier.

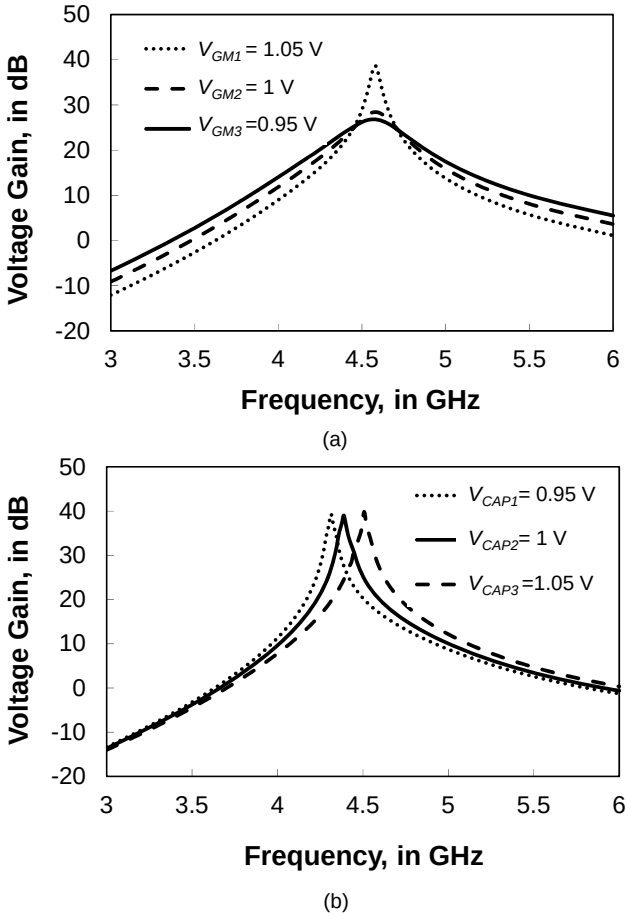

Figure 4.6. Simulated voltage gain of the preamplifier versus: (a) *gm* control voltage V_{GM}, and (b) frequency control voltage V_{CAP}.

transistors M_5 and M_6 form a positive feedback loop at the preamplifier output. V_{CAS} and V_{GM} control the proportion of signal current flowing through M_5 and M_6, thereby controlling the amount of positive feedback. The simulation results shown in Figure 4.6(a) illustrates the gain and bandwidth change as V_{GM} is varied ($V_{GM1} > V_{GM2} > V_{GM3}$). Figure 4.6(b) shows the simulated change in the center frequency of the preamplifier's response when V_{CAP} is varied ($V_{CAP1} < V_{CAP2} < V_{CAP3}$). The measured tuning range is 3.8 GHz to 5.2 GHz. The preamplifier input is matched to 50 Ohm in the 4-5 GHz band by a conventional L-type network which consists of the 6.6 nH shunt input inductor (L_G), with a self-resonant frequency of 9.3 GHz and peak-Q of 11.2 at 5 GHz, and a 0.3 pF capacitor in series (vertical plate backend capacitor, C_G). L_G also provides a DC bias path (V_{BIAS}) and shunts any electrostatic discharge (ESD) event away from the transistor inputs. L_D and L_G are fully-symmetric on-chip inductors that provide the highest Q-factor in the smallest possible chip area [4.14].

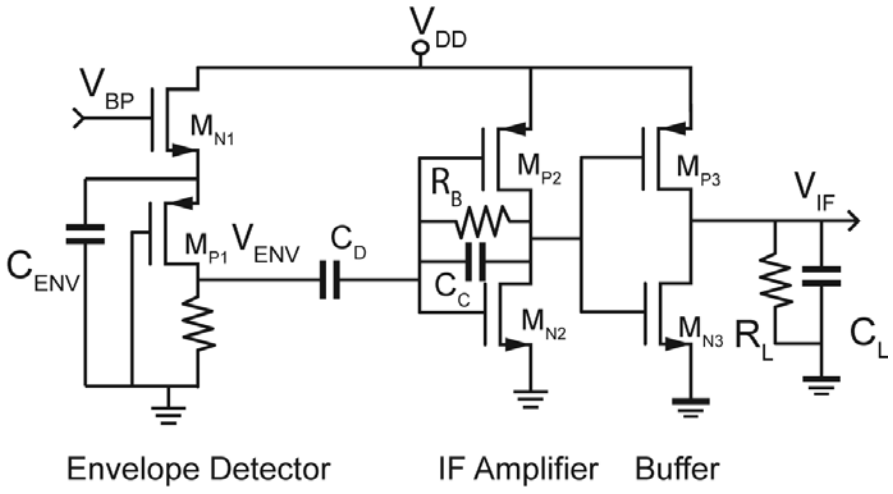

Figure 4.7. Schematic of the envelope detector (M_{N1}, M_{P1}), IF amplifier (M_{N2}, M_{P2}) and test buffer (M_{N3}, M_{P3}).

Positive feedback around M_5 and M_6 enhances the selectivity of the amplifier, as seen from Figure 4.6(a). Although the MOSFET transconductance (*gm*) is small at low bias current, positive feedback also increases the output impedance (Z_O) of the preamplifier. Hence, the voltage gain, which is proportional to the product of transconductance and output impedance (Z_O) increases from 16 dB to 35 dB at the expense of bandwidth (520 MHz to 45 MHz) as the feedback increases. The preamplifier linearity in terms of input -1 dB compression also drops from -20 dBm to -41 dBm. The 50 Ω noise figure increases from 4.6 dB (the main noise contribution comes from LG and pairs of M_1, M_2) to 7.3 dB (the main noise contribution comes from positive feedback branch M_3, M_4, M_5 and M_6) at an RF input frequency of 4.5 GHz. The preamplifier consumes 1.6 mW from the 1 V supply, which is 55% less power than the conventional FM-UWB preamplifier design described in [4.15] at comparable voltage gain.

4.3.2. Envelope detector and IF amplifier

Envelope detector (M_{N1} in Figure 4.7) removes the carrier from the filtered RF signal. Source follower $_{MN1}$ acts as diode detector because the RF voltage swing on its source terminal is constrained by 2 pF MOS capacitor, C_{ENV}. It is well-known that the envelope detector gain is less than unity for signal amplitudes below a certain threshold [4.16]. The simulated overall detector voltage gain as a function of input amplitude is shown in Figure 4.8. Signals smaller than the detector's input threshold of 250 mV are squared by the nonlinearity of the MOSFET. The gain peaks at around 80 mV_{rms}, and then drops at higher input amplitudes as M_{P1} drops out of saturation and into the triode operating region.

Common-gate transistor M_{P1} amplifies and buffers the detected signal to the IF amplifier input. The PMOS amplifier reuses bias current flowing through the envelope detector, thereby saving power. M_{P1} provides a voltage gain of 6 dB from the source to the drain and extra filtering. The envelope detector is biased at 200 μA

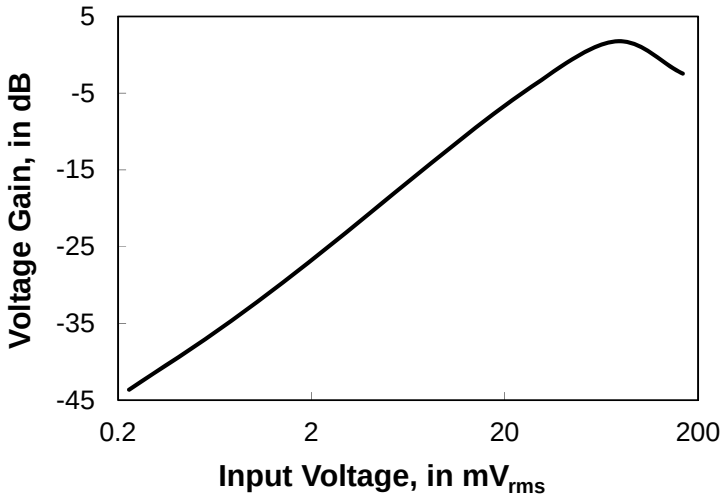

Figure 4.8. Voltage gain of the envelope detector (V_{ENV}) as a function of rms input voltage (V_{BP}).

and is sensitive to variations in process, voltage and temperature (PVT), because its bias current depends on the threshold voltages of M_{N1} and M_{P1}. A circuit can be added to compensate for this effect [4.17].

The envelope detector is followed by intermediate frequency (IF) amplifier and output buffer stages, as shown in Figure 4.7. The detected envelope is amplified 20 dB by CMOS IF amplifier M_{N2} and M_{P2}, which has a 100 kHz to 10 MHz bandwidth. R_B provides a DC feedback path to bias the amplifier, while capacitor C_D provides bias isolation from the envelope detector. The output buffer (M_{N3} and M_{P3}) is capable of driving the 50 Ω input impedance of the test instrumentation used for chip characterization. M_{N3} and M_{P3} are scaled six times wider than M_{N2} and M_{P2}, and symmetry in their physical layout is used to promote matching of the device parameters. The output buffer consumes 2.5 mW from a 1 V supply.

4.4. Measurement Results

The 0.3 mm^2 receiver prototype (see Figure 4.9) was realized in a production 65 nm bulk CMOS technology. The 0.09 mm^2 input matching inductor (L_G) dominates the chip area. While the matching inductor is an essential part of the receiver input matching network (together with C_G), it could also be implemented off-chip, reducing the die area by 30%. The test die was characterized from on-wafer measurements and also mounted and wirebonded onto a printed circuit board (PCB) for characterization as shown in Figure 4.10. A high frequency laminate PCB (tanδ=0.004 at 5 GHz) is used to implement 0.16 dB/inch insertion loss 50 Ω transmission lines between the IC and coaxial test connectors located at the PCB periphery. The RF input bondwire length is 0.5 mm, resulting in a series inductance of approximately 0.5 nH and parasitic capacitance of 10 fF. The supply and bias lines are filtered using 10.33 nF off-chip (i.e., on the PCB) in parallel with 15 pF on-chip decoupling capacitance.

The RF input reflection coefficient (S_{11}) was characterized using a 4-port network analyzer with a true-mode stimulus [4.18] and on-wafer probing of the test circuit. The measured receiver input S_{11} from 4 5 GHz is plotted in Figure 4.11 for the positive feedback turned off. In this condition, the circuit behaves like a conventional cascode amplifier. The S_{11} measured with on-wafer RF probes (SOLT calibrated to the probe tips) and for the die mounted on the PCB shows good agreement with the post-layout simulation result. The slight shift in minimum S_{11} of 150 MHz observed for the packaged device (SOLT calibrated to the connector interface) is due to parasitics added by the bondwire and RF-connector to the RF input.

It is difficult to measure the center frequency of the receiver filter directly at the preamplifier output without an extra buffer, because of its high output impedance (> 1 kΩ). With positive feedback active, the output signal leaks back to the source of the cascode transistor and then to the RF input terminal through C_{GD} of the input transistor. The null normally seen in S_{11} without feedback is therefore disturbed, and

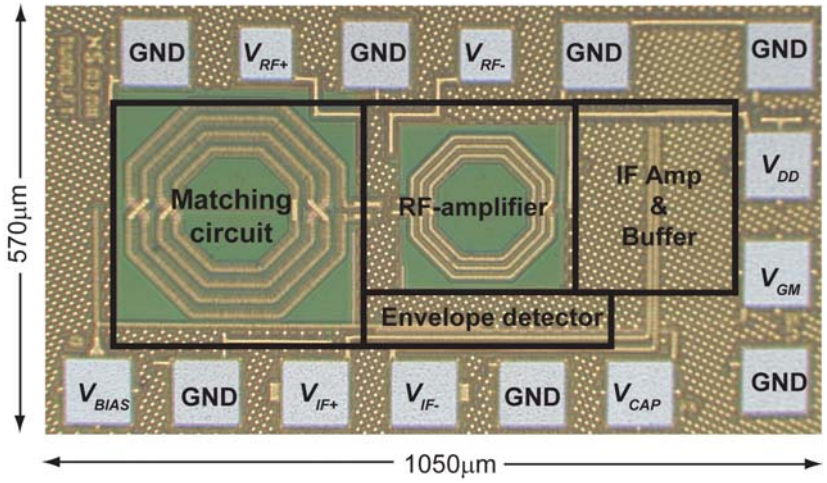

Figure 4.9. Micrograph of the 65 nm CMOS receiver prototype.

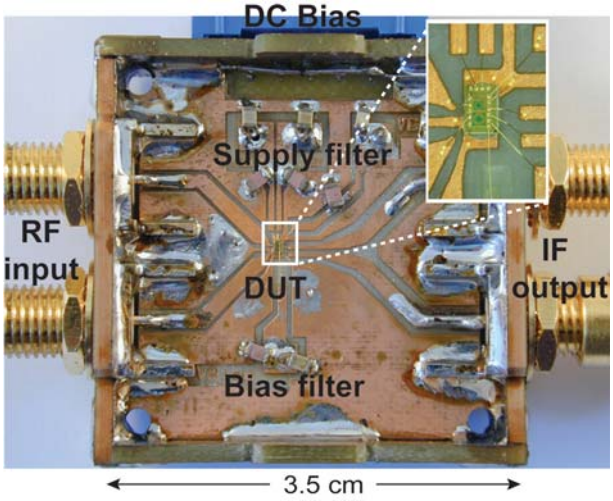

Figure 4.10.Assembled test PCB.

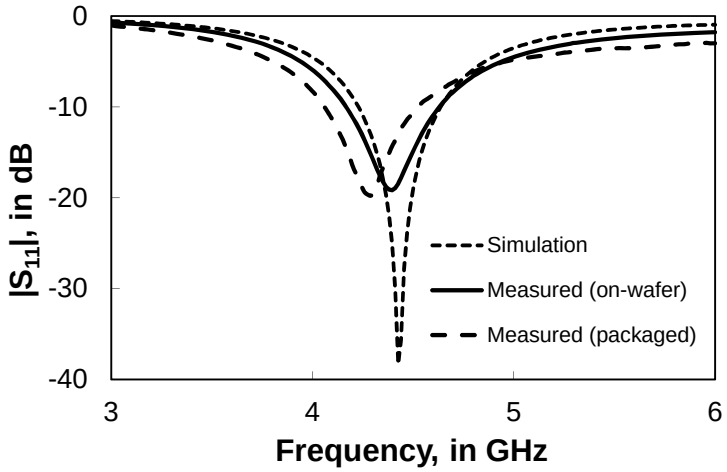

Figure 4.11. Measured and simulated receiver S_{11} (no positive feedback).

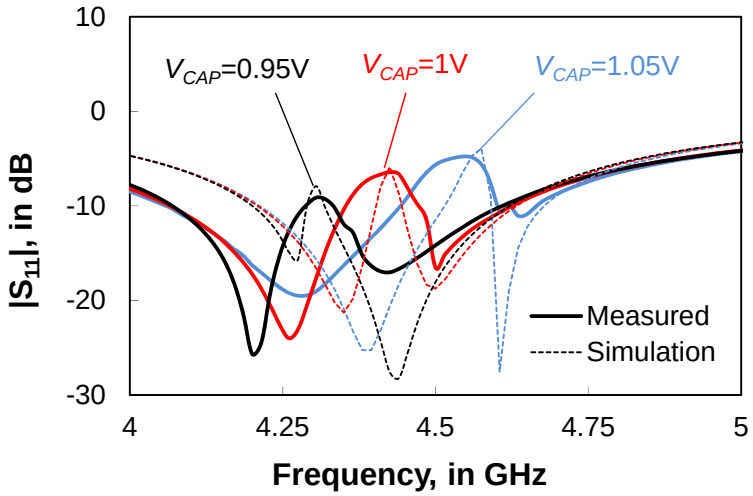

Figure 4.12. Measured and simulated receiver S_{11} for different settings of VCAP when positive feedback is applied.

can be controlled by changing V_{CAP} as shown Figure 4.12. Compared to Figure 4.11 (no feedback), the positive feedback degrades the input match in the vicinity of the bandpass center frequency, and the effect of tuning V_{CAP} on the measured S_{11} can be seen (tuning sensitivity). Figure 4.13 shows the measured center frequency of the receiver as a function of V_{CAP}. The measured frequency range is 3.8-5.2 GHz with a curve that corresponds to the shape of the varactor C-V function.

In testing, the receiver was tuned to its optimum sensitivity by adjusting V_{GM} and V_{CAP} to change the preamplifier's tank Q and its sub-band frequency, respectively. Firstly, the amplifier gain was increased via V_{GM} until oscillation commences, which causes an abrupt change in the output DC bias. Then, V_{GM} was slowly decreased until oscillation stops, which can be observed easily as the DC bias drops back to its

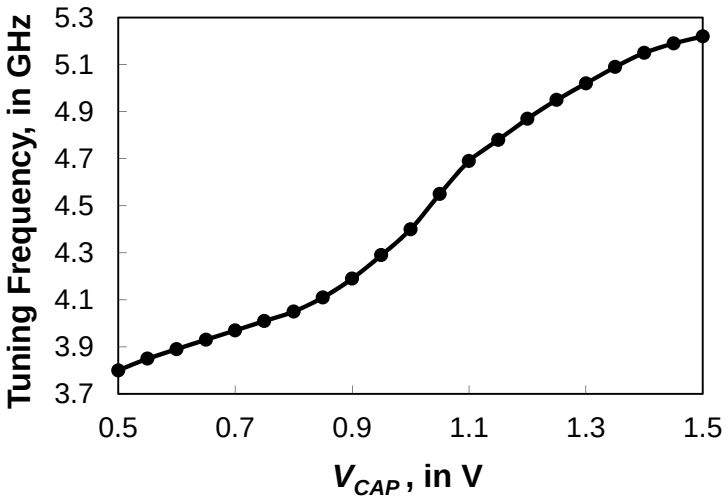

Figure 4.13. Measured tuning range versus control voltage, V_{CAP}.

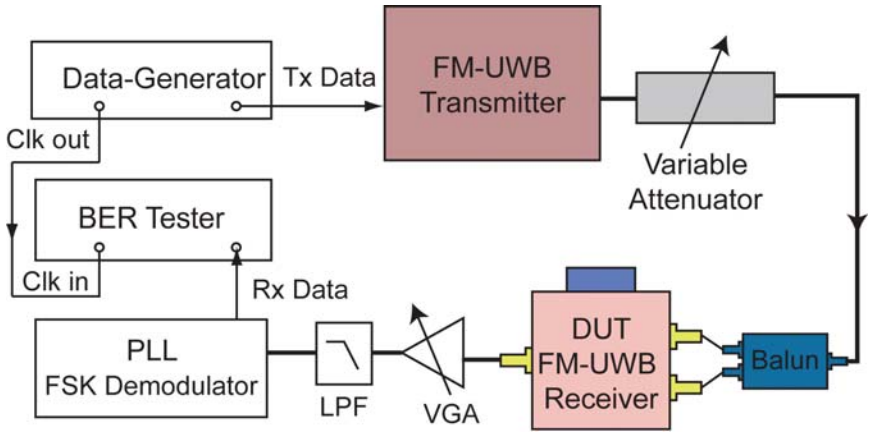

Figure 4.14. Block diagram of measurement setup.

original value. The receiver is now operating near its highest voltage gain and selectivity.

Figure 4.14 is an illustration of the test setup used to measure the receiver sensitivity. The FM-UWB transmitter is driven by a random digital data source and produces a wideband FM signal at a -14 dBm. The received signal level is adjusted using a variable attenuator to emulate the propagation losses of an RF link. A balun converts the single-ended signal to differential at the FM-UWB receiver chip RF input. A variable gain amplifier (VGA) amplifies the IF output signal to 0.5 $V_{p\text{-}p}$. The FSK IF signal is then low-pass filtered, and demodulated using a 74HCT9046 phase-locked loop and then fed to the error detector to measure the bit-error rate (BER).

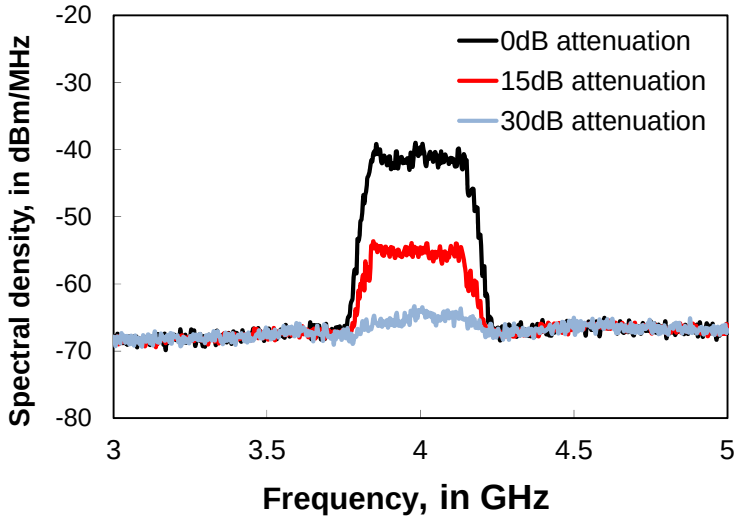

Figure 4.15. Transmitter output spectrum for various attenuations.

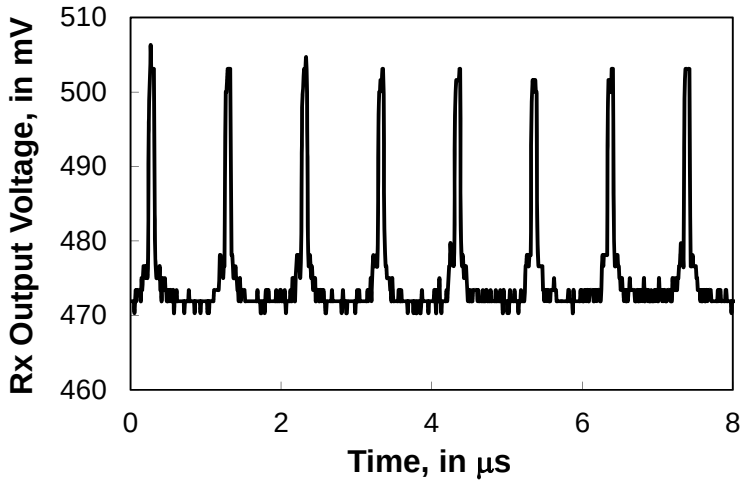

Figure 4.16. Receiver output pulses measured for 1 MHz sub-carrier.

The measured spectra at the FM-UWB transmitter output are plotted in Figure 4.15 for peak power spectral densities of -40, -55 and -70 dBm/MHz. The transmitted signal occupies 500 MHz bandwidth. Figure 4.16 shows the received sub-carrier output waveform at 1 MHz for a measured RF input power of -50 dBm. The pulse train seen at the IF output agrees well with the analysis presented from Section 4.2 and the simulation results shown in Figure 4.3(c).

The measured bit-error rate of the receiver a function of received input power is plotted in Figure 4.17. The receiver is tuned to a center frequency of 4.3 GHz and the transmitted signal band ranges from 4.25-4.75 GHz. The receiver sensitivities (10^{-3} BER) at data rates of 50, 100 and 200 kbit/s are -87, -84 and -78 dBm, respectively. Deviation from the theoretical BER 'waterfall' shape for the measured

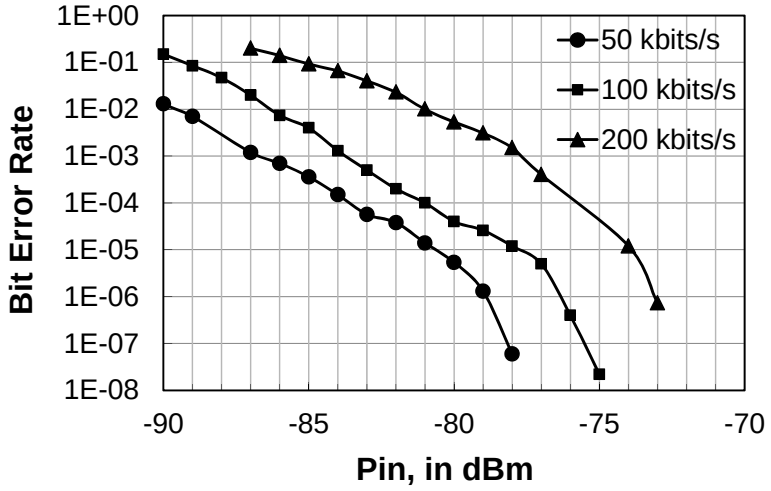

Figure 4.17. Measured bit-error rate at various data rates for center frequency of 4.3 GHz.

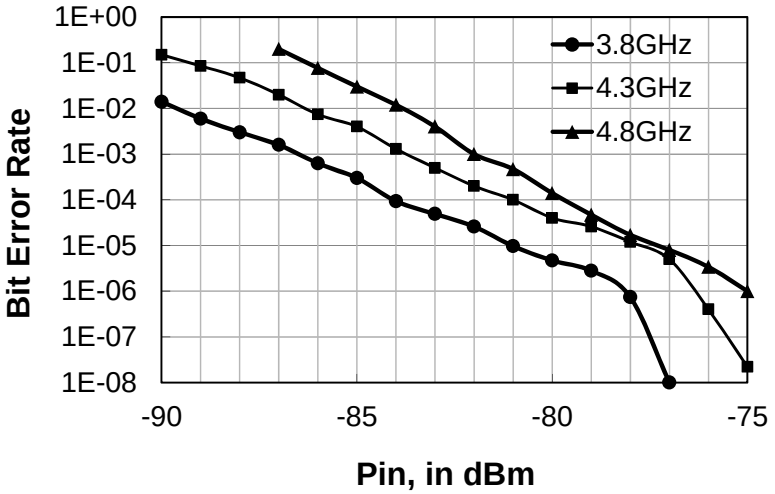

Figure 4.18. Measured bit-error rate at various center frequencies for data rate of 100 kbit/s.

BER curves is likely caused by the FSK (PLL) demodulator (not on-chip), which displays a threshold effect before reliably demodulating the received signal. The measured results imply 4 dB link margin for the receiver running at 100 kbit/s (some of which will be taken up by the baseband processor) given that -80 dBm sensitivity is desired for 10 m range.

Figure 4.18 shows the measured BER when the receiver center frequency is tuned to 3.8, 4.3 and 4.8 GHz. The sensitivity of the receiver (10^{-3} BER) within the tuning range varies from -82 to -86 dBm at a data rate of 100 kbit/s. The variation of the sensitivity is contributed by output noise variation of the receiver at different center frequencies, and also variation of the input matching condition. Figure 4.19

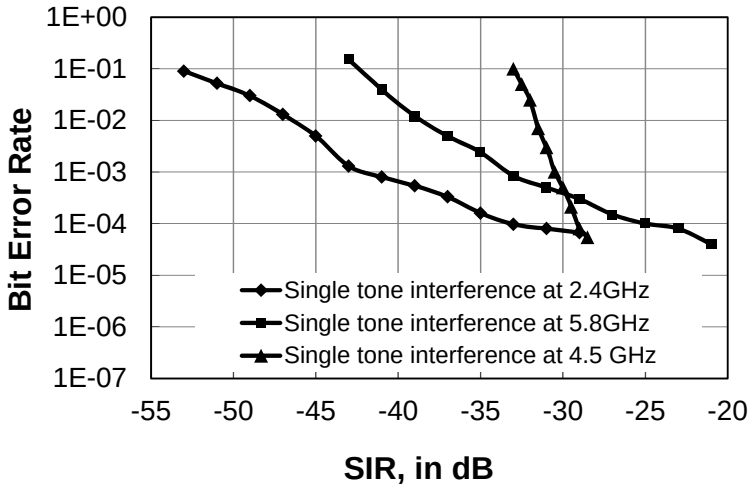

Figure 4.19. Measured bit-error rate versus single-tone interference strength for interference at 2.4, 4.5 and 5.8 GHz at data rate of 100 kbit/s and center frequency of 4.3 GHz.

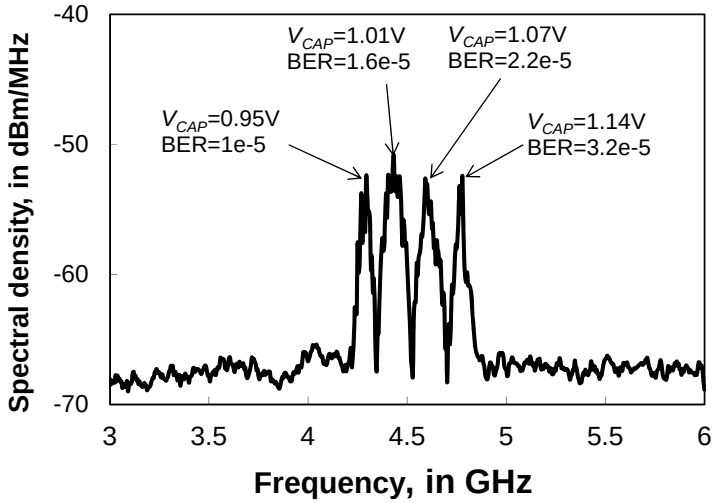

Figure 4.20. Transmitted output spectrum when frequency selective fading occurs due to multipath.

illustrates the measured BER for single tone interference applied out of band at 2.4GHz and 5.8 GHz, and in-band at 4.5 GHz. The received input power is -80 dBm at a data rate of 100 kbit/s. The FM-UWB receiver is able to tolerate in-band interference that is 30 dB stronger than the input signal power. The out-of-band interference rejection can be improved by adding a preselect filter ahead of the receiver RF input.

Frequency selective fading due to multipath is simulated by splitting the transmit signal into two paths which have different lengths (Δl = 1.2 m). The two paths are combined again at the receiver, yielding the spectrum shown in Figure 4.20. The

TABLE 4.1 FM-UWB RECEIVER PERFORMANCE COMPARISON

Parameters	This work	[4.19]	[4.20]
Technology	CMOS 65 nm	SiGe BiCMOS 180 nm	SiGe BiCMOS 250 nm
RF band, in GHz	4-5	3.1-4.9	7.2-7.7
Power consumption, in mW	2.2	10	9.1
Receiver sensitivity, in dBm	-84	-46	-86.8
Data rate, in kbit/s	100	100	50
Energy efficiency, in nJ/bit	22	100	180
Active area, in mm^2	0.3	0.72	0.88

peaks and nulls emulate the nulls and peaks in the received signal that might be encountered due to propagation path delay differences (i.e., multipath effect). The receiver center frequency is tuned across 4 GHz to 5 GHz and the receiver sensitivity measured in the transmission 'windows' in the emulated channel. The experiment demonstrates the receiver agility when frequency selective fading is present in the channel. However, a mechanism for active tuning is required in practice, which is a topic for future study and development. Adaptive control circuitry could be added to the receiver to initiate a frequency hopping scheme to scan the receiver across the UWB for a suitable transmission window when the BER is high due to multipath or strong interference. Overall, the receiver has an advantage of more power efficient by processing a sub-band, rather than the entire UWB band.

Consuming just 2.2 mW at 100 kbit/s, the energy efficiency of the receiver front-end is 22 nJ/bit, which is an improvement of almost an order of magnitude compared to earlier FM-UWB designs. The receiver performance is summarized and also compared with other FM-UWB receiver in Table 4.1.

4.5. Conclusion and Summary

A low data rate FM-UWB receiver typically consumes less energy-per-bit in continuous operation than receivers utilizing burst mode transmission at much higher data rates (i.e., a duty-cycled). A new architecture for detecting FM-UWB signals was described and validated in this chapter. Positive feedback was employed in a controlled way to realize selectivity, high gain and FM-to-AM transformation in a single circuit block, which improves sensitivity and lower power consumption. The ability to process a sub-band of the received FM-UWB signal could also be used to optimize reception at the receiver. The 0.3 mm^2 (active area) receiver front-end prototype realized in a production 65 nm CMOS technology demonstrated -84 dBm input sensitivity at 100 kbit/s, while consuming 2.2 mW from a 1 V supply for an energy efficiency of 22 nJ/bit. The energy efficiency is slightly higher than

TABLE 4.2 LOW POWER RECEIVER PERFORMANCE COMPARISON

Parameters	**This work**	**[4.21]**	**[4.22]**	**[4.23]**	**[4.24]**	**[4.25]**
Standard	FM-UWB	Zigbee	Wake-up	Super-Regen.	UWB	UWB
Technology	CMOS 65 nm	CMOS 180 nm	CMOS 90 nm	CMOS 180 nm	CMOS 90 nm	CMOS 130 nm
Modulation	2-FSK	QPSK	OOK	BFSK	PPM	BPSK
RF band, in GHz	4-5	2.4	2	2.4	4.4	0-0.96
Power Consumption, in mW	2.2	26.5	0.052	0.215	35.8	3.3
Receiver sensitivity, in dBm	-84	-101	-72	-86	-99	-55
Data rate, in kbit/s	100	250	100	250	100	1300
Energy efficiency, in nJ/bit	22	106	0.52	0.84	2.5	3.3
Active area, in mm^2	0.3	3.8	0.1	0.55	1	4.52

the specification. The second prototype described in next chapter will address this shortcoming.

The receiver is compared with other low power, low data rate receivers in Table 4.2. The receiver designed in this work consumes the least power and chip area among the FM-UWB receivers, while realizing comparable sensitivity. The wake-up receiver [4.22] consumes less power than an FM-UWB design, however, the sensitivity is 12 dB poorer at -72 dBm. The wake-up receiver also required a high selectivity passive RF preselect filter (e.g., SAW or BAW high-Q bandpass) to attenuate potential interferers to a tolerable level. The super-regenerative receiver in [4.23] achieves high energy efficiency and sensitivity by using BFSK modulation. However, the narrowband receiver is susceptible to multipath fading or interference effects because the front-end operates at a fixed input frequency and is not tunable. The UWB receiver in [4.24] also realizes good energy efficiency by receiver duty cycling, and efficiency will suffer when continuous data streaming is required. The other UWB receiver in [4.25] operates at 1.3 Mbit/s, but has poor sensitivity (-55 dBm) and is confined to RF inputs below approximately 1 GHz. In summary, the FM-UWB receiver designed in this work offers the potential for a low cost, compact implementation with better coexistence and robustness than other low-power receiver technologies in continuous data streaming applications at rates on the order of 100 kbit/s.

The results of this study validate the regenerative FM-UWB receiver front-end concept. Automatic digital tuning is required to control the positive feedback loop in a practical receiver. Simultaneous frequency and Q tuning for the RF preamplifier [4.5]-[4.8] can also be applied to this receiver in the same ways it has been applied to monolithic filters. A fully-digital front-end calibration scheme and digital baseband processing are preferred because they are more amenable to scaling in future CMOS process generations [4.26], [4.27]. A fully-integrated receiver incorporating baseband processing to demodulate the sub-carrier will be

implemented to further validate the receiver concept and benchmark its overall performance.

The following chapter will describe a full FM-UWB transceiver (i.e., transmitter, receiver, baseband modulator, and demodulator) prototype. The design is an improvement in terms of power consumption compared to the designs described in Chapter 3 and this chapter. Both the receiver and transmitter will be integrated on-chip, along with other peripheral circuitry such as biasing, control logic and calibration.

4.6. References

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CHAPTER 5. FM-UWB TRANSCEIVER

5.1. Introduction

In Chapters 3 and 4, FM-UWB transmitter and receiver prototypes have been described. The next objective is to integrate them together into a full FM-UWB transceiver. The main building blocks in the transmitter are the sub-carrier oscillator, RF oscillator, and power amplifier, while the receiver consists of a low-noise amplifier, FM demodulator, and FSK detector, as shown in Figure 5.1.

The desired specifications for the transceiver are listed in Section 2.5. The main objective of this work is to reach an energy efficiency of less than 10 nJ/bit for each of the transmitter and receiver. Integrating the transmitter and receiver together onto the same IC saves power, reduces the number of I/O pads, and the overall chip area, as they share building blocks such as biasing, clock generator and calibration circuitry.

Depending upon the application, the transmitter and receiver may be active at the same time, which requires duplexing so that transmitter and receiver do not share the same frequency band. A communication protocol is therefore required to manage wireless transmission between devices. Also, sufficient isolation between

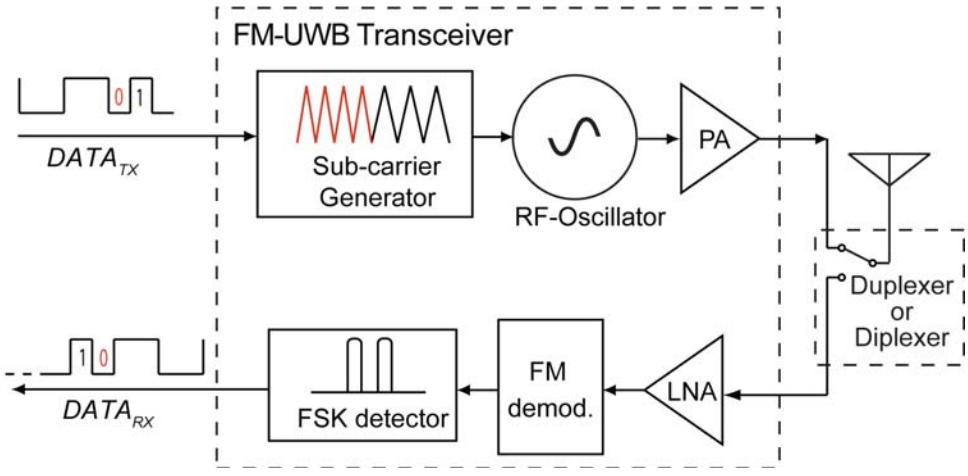

Figure 5.1. Block diagram of a typical FM-UWB transceiver.

the transmitter and receiver is required so that they do not interfere with each other. Alternately, time duplexing may be used so that transmitting and receiving sections are not active at the same time. In a time-duplexed FM-UWB transceiver, the transmitter (or receiver) is turned 'off' during reception (or transmission) of data in order to save power. An external duplexer (for time switching) or diplexer (for transmitter and receiver frequency separation) is therefore required between the antenna and the transceiver IC, and an RF filter (which may be incorporated in the antenna design) that attenuates out of band harmonics and potential RF blockers.

The FM-UWB transceiver test chip architecture and building blocks are described in Section 5.2 of this chapter. Design details of each of the transceiver circuit blocks are discussed in Section 5.3. Experimental results of the transceiver prototype realized in 90 nm CMOS are discussed and a compared with other FM-UWB transceivers in Section 5.4. Conclusions, a chapter summary, and areas identified for future work are summarized in Section 5.5.

5.2. Transceiver Architecture

The proposed fully-integrated FM-UWB transceiver is shown in Figure 5.2. The triangular sub-carrier is generated using a relaxation oscillator and FSK modulated by the binary transmit data. The triangular output voltage from the relaxation oscillator is converted to a current by transconductor G_M. A current-controlled ring oscillator (ICO) generated RF carrier operating at one-third of the output frequency (RF oscillator in Figure 5.2). The transmit signal is tripled in frequency and amplified for transmission by the tripler/power amplifier that drives the antenna via an on-chip output matching network.

On the receive side, the received carrier signal from the antenna (V_{RX}) is amplified and filtered by a regenerative RF amplifier. An envelope detector recovers the FSK-modulated sub-carrier signal. The detected signal is bandpass filtered, amplified at IF, quantized by a 1-bit limiter, and then FSK demodulated to produce the received data bit stream. A current reuse technique is employed extensively in the transceiver in order to conserve power. For example, supply current is shared between the frequency tripler and PA circuits in the transmitter, and also between the regenerative LNA, envelope detector and IF limiter in the receiver front-end.

An on-chip successive approximation register frequency-locked loop (SAR-FLL) calibrates the sub-carrier, RF oscillator, and regenerative amplifier center frequencies. Positive feedback is adjusted during calibration to tune the regenerative amplifier in order to reach its highest sensitivity. Voltage and current references are also implemented on-chip to generate PVT insensitive references, and for general biasing. As the transceiver operating mode and bias are controlled digitally, DACs are implemented in various building blocks. Serial registers are also included to store the digital control signals for all of the various blocks. Buffers are added to monitor the IF, various clocks, and digital data signals for test purposes. A mirror of the current reference (typical value of 600 nA) can also be measured to characterize its sensitivity to supply voltage and temperature variations.

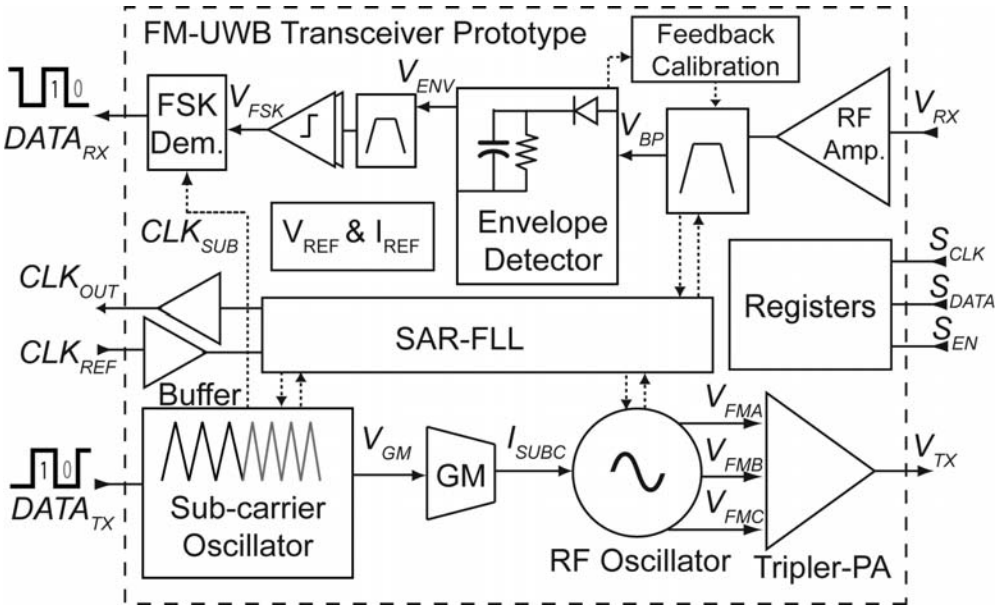

Figure 5.2. Proposed FM-UWB transceiver prototype chip.

5.3. Transceiver Circuit Design

The prototype FM-UWB transceiver is implemented in a 90 nm bulk CMOS technology with thick metal and metal-insulator-metal (MIM) capacitor options for RF circuit applications [3.3]. The all-copper interconnect scheme (bottom to top of the stack) consists of 5 thin, two medium-thick, and one thick top metal. In this prototype, a single 1 V supply is chosen. Small modifications and improved circuit layouts are implemented across the blocks described in the previous chapter, such as the voltage/current reference, SAR-FLL, and the sub-carrier oscillator. The ICO is modified and optimized to operate at one-third the RF carrier frequency and has 3-phase outputs. The receiver blocks and the PA are completely new. The following section describes the new or upgraded building blocks in the transceiver that were not described in previous Chapters 3 or 4.

5.3.1. RF current-controlled ring oscillator

As discussed in Section 3.2.1, a current-controlled ring oscillator (ICO) was chosen for the RF transmit oscillator because it has advantages such as a linear and wide tuning range, scalability with technology, scalable control current, and low susceptibility to noise present on the supply or ground lines. A three-stage ring oscillator is used, and it operates at one-third of the desired RF oscillation frequency to minimize power consumption. By operating at one-third of the operating frequency, unwanted pulling of the ICO frequency from a strong interferer at the transmitter output is mitigated. Furthermore, the required tuning range of the ICO is reduced to one-third and the amplitude variation is much less than the first version

of the ICO described in section 3.2.1, which improves the frequency versus current linearity.

Each stage of the ICO consists of an NMOS driver with PMOS active load, as shown in Figure 5.3. The PMOS (M_{PR1}-M_{PR3}) source voltage (V_{REG}) is regulated to 0.75 V by opamp A_2, via a feedback loop that derives the desired supply voltage from temperature-compensated voltage reference (typical V_{REF} = 0.5 V). Regulation of the ring oscillator supply desensitizes it to external variations in the supply voltage, V_{DD}. As the current that supplies the ICO (I_{RING}) increases (while maintaining V_{REG} constant), the ICO output frequency (f_{osc}) increases proportionally. I_{RING} is the sum of the bias current from M_{P1}, a 6-bit current DAC (I_{DAC}), and the sub-carrier modulation current I_{SUBC}, all of which are supplied by PMOS current sources. The output impedance of the current source is enhanced by feedback amplifier A_1, which improves the accuracy of the current mirror, and yields 65 dB power supply rejection from DC up to 10 kHz.

The three output phases generated by the ICO (V_{FMA}, V_{FMB}, and V_{FMC}) are 120º apart. One of the phases (V_{FMA}) is buffered, frequency-divided by 1024, and calibrated using an FLL. The transistor sizes in each stage of the ICO are equal and symmetrically drawn in the layout to minimize mismatch between the output phases. The capacitive loading on each stage is also balanced, i.e., dummy buffers (D_1 and D_2) are implemented. A 1 pF decoupling capacitor (C_S) acts as a charge

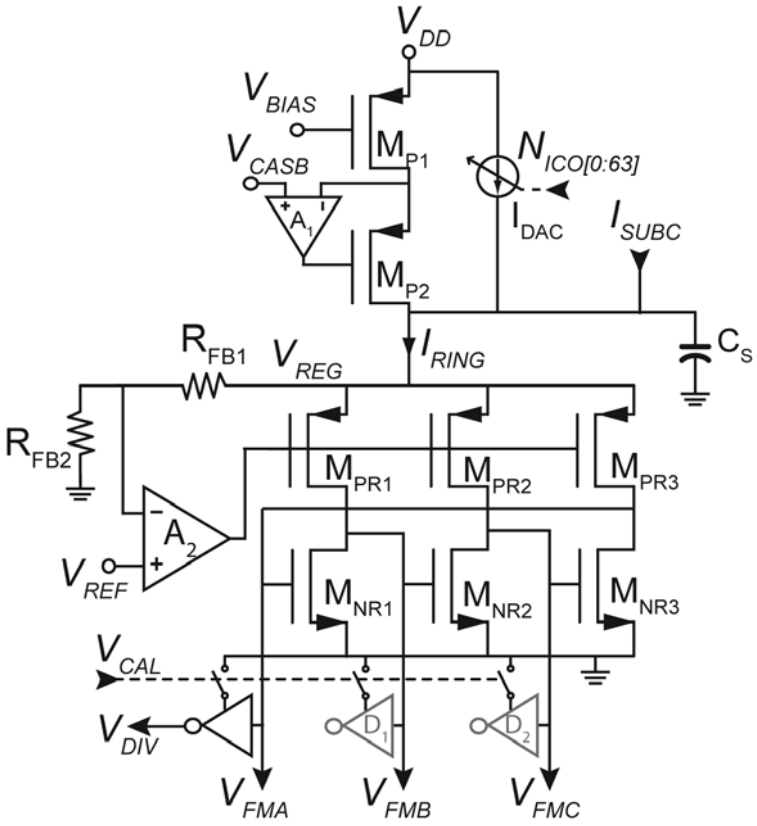

Figure 5.3. Current-controlled RF oscillator (RF-ICO) schematic.

reservoir which reduces fluctuations in node voltage V_{REG}, and also filters out high frequency supply noise. The current DAC is controlled by 6-bit word N_{ICO}, and it is calibrated to provide a frequency tuning range of 1-1.7 GHz. The ICO (incl. opamps and bias circuits) consumes 90 µA of DC current when it is oscillating at 1.33 GHz (one-third of the RF carrier at 4 GHz). The tuning sensitivity of the ICO is 38 MHz/µA.

5.3.2. Frequency tripler and power amplifier

The output signal of the ICO is buffered into a full swing, rail-to-rail clock signal. Each of the phases is multiplied with each other by a series of NMOS switches, creating a times-three frequency multiplier as shown in Figure 5.4. Finally, a CMOS power amplifier (PA) amplifies the frequency-tripled signal, and drives a 50 Ω load via an LC matching network consisting of a 4 nH bondwire inductor and 0.1-0.3 pF shunt capacitance controlled by a DAC (C_{BD2}). Absorbing the wirebond in the output matching network reduces the number of components, and minimizes the chip area and cost. A large proportion (> 40%) of the total transceiver power is dedicated to the PA stage in order to maximize the link span between transmitter and receiver. Power consumption is minimized by having the frequency multiplier and the PA share the same bias current (i.e., current reuse). The DC current consumed by the PA flow via L_1 to the tripler, with C_D providing the AC ground for M_{N1} of the PA.

The tripler AND function is realized by a series of two NMOS devices (e.g., $M_{NA'}$ and M_{NC}), where drain current flows when 2 phases from the ICO overlap. The sum of these AND pairs gives a times-three frequency output. The tripler sizes are controlled by 2-bit digital word N_{PA} to adjust the overall gain and output power of the PA stage over a 5 dB range. The tripler current generates a voltage across resonant tank L_1 and C_{BD1}, which drives the CMOS PA (M_{N1} and M_{P1}) through

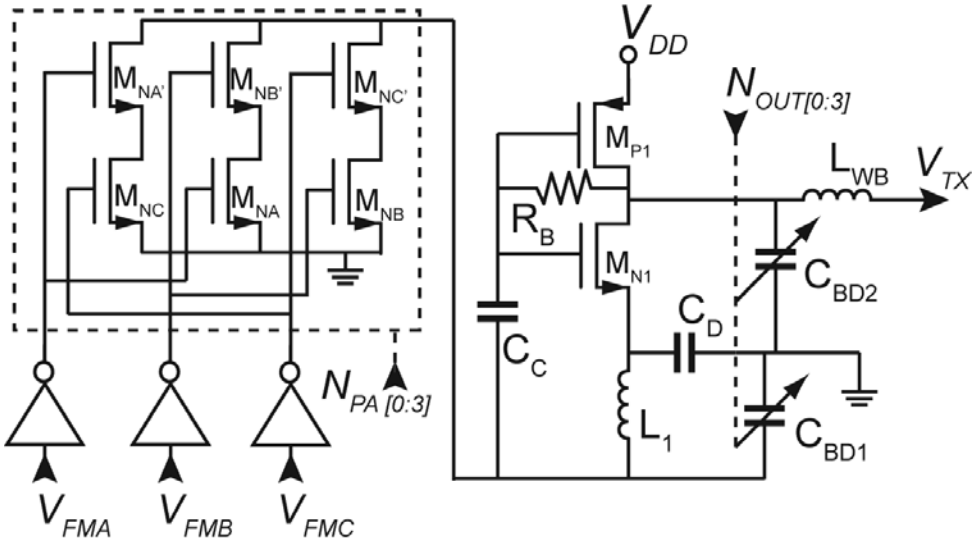

Figure 5.4. Frequency tripler and current reuse power amplifier schematic.

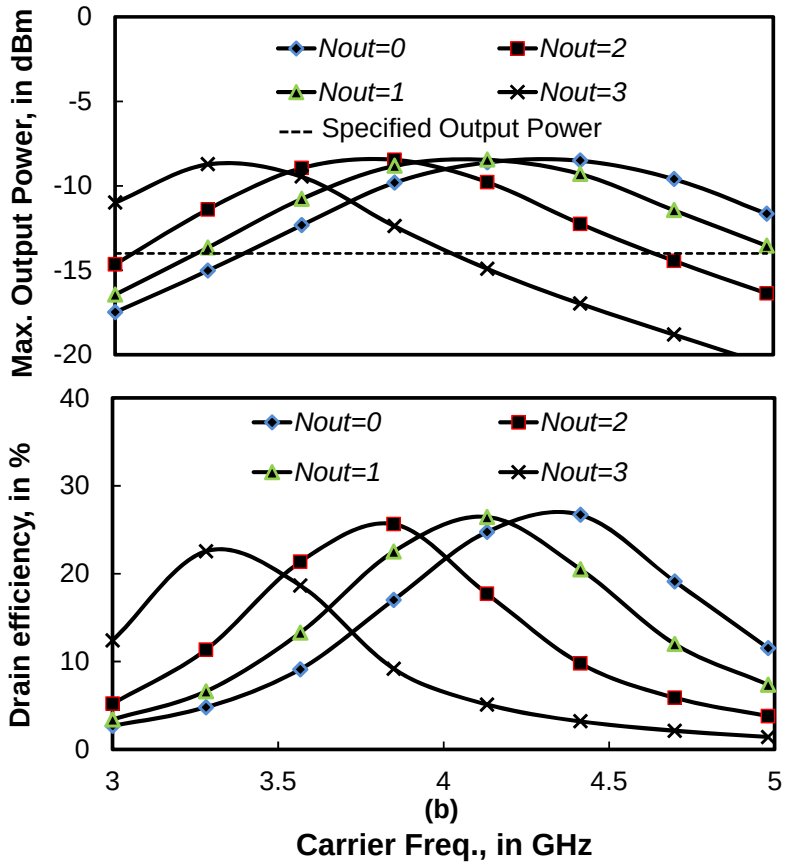

Figure 5.5. Simulated maximum output power (a) and drain efficiency (b) of the PA versus frequency for various setting of N_{OUT}.

coupling capacitor C_C.

The typical FM-UWB bandwidth is only 500 MHz, but the transmitter must cover the frequency range from 3-5 GHz. The LC matching network at the PA output has a -3 dB bandwidth of less than 1 GHz. Sub-band selection with some overlapping is employed to cover the entire frequency range specified and ensures efficient coupling of the transmitted power to the output as shown by simulation results in Figure 5.5. The 2-bit control world N_{OUT} is employed to vary the capacitor DAC in the resonant circuit (L_1, C_{BD1}) and the output matching network (L_{WB}, C_{BD2}) to select the operating sub-band. The 10 pF decoupling capacitor (C_D) AC grounds the CMOS PA. It is implemented using a parallel stack of MOS, MIM, and back-end metal-oxide-metal (MOM) capacitors to maximize the capacitance density and minimize the area of C_D on-chip. The tripler-PA consumes 490 µW and produces up to -8.8 dBm (simulated) maximum output power. The simulated peak drain efficiency of the tripler-PA is 27%.

5.3.3. Transconductance amplifier

The differential push-pull transconductance amplifier (GM block) shown in Figure 5.6 translates the sub-carrier voltage to a current that modulates the transmit RF-ICO. Amplifiers A_1 and A_2 form a push-pull buffer that drives on-chip polyresistor R_{GM}. The resulting current

$$I_{inj} = \frac{V_{GM} - V_{REFM}}{R_{GM}} \tag{5.1}$$

is injected into the sources of transistors M_{S2} and M_{S4}. When the frequency modulation is turned on, V_{GM} is a triangular wave voltage generated by the sub-carrier oscillator (see Section 3.2.3), otherwise V_{GM} is equal to V_{REFM} so that no

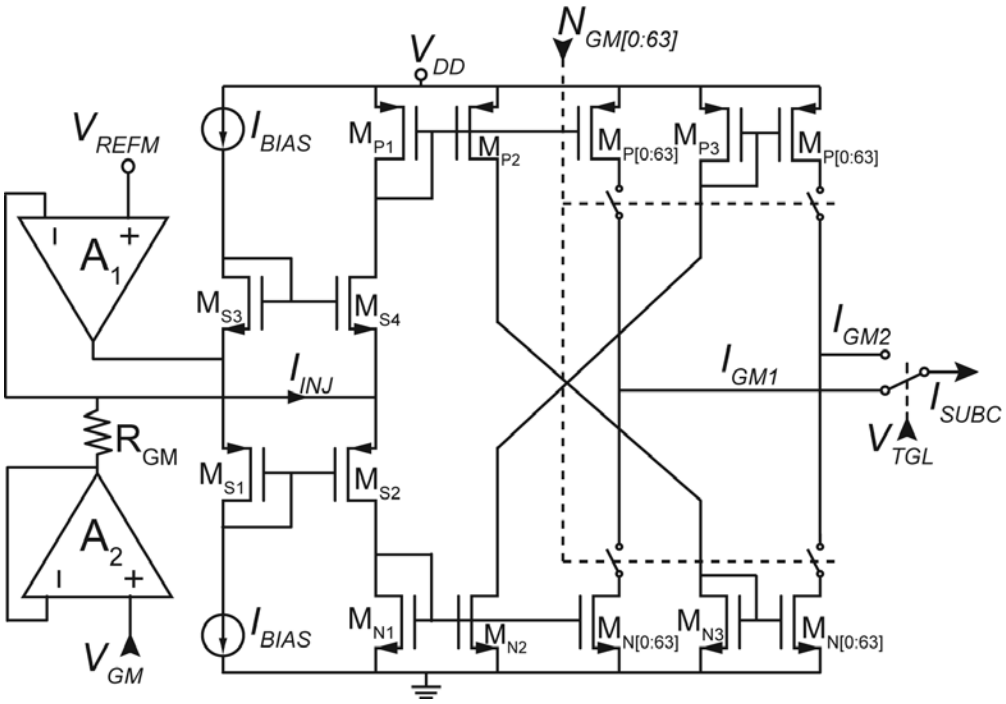

Figure 5.6. Push-pull transconductance amplifier (G_M) schematic diagram.

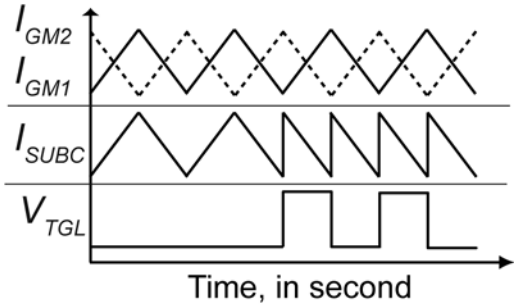

Figure 5.7. Timing diagram of triangle and sawtooth current modulations.

current is injected. Internal reference voltage V_{REFM} has a typical value of 0.4 V. The injected input current splits between PMOS M_{P1} and NMOS M_{N1}, and it is then mirrored to form a push-pull output current with no DC offset. The output current magnitude is set by a 6-bit word (N_{GM}) that controls the current DAC (instead of varying R_{GM}) because it does not change the bias voltage in the GM circuit. Output current I_{SUBC} has a range of 4-15 μA in magnitude. It modulates the transmitter ICO, which translates into a range of 0.25-1 GHz for the FM-UWB signal bandwidth. The bandwidth is calibrated by setting V_{GM} equal to V_{REFH} (internal reference voltage of 0.5V) and employing the SAR-FLL calibration scheme described in Section 3.2.5 to adjust N_{GM}.

There are two current DACs (one is a mirror of the other) generating anti-phase currents I_{GM1} and I_{GM2}. Selecting one of the DACs generates a triangle output current waveshape. Alternating both DACs synchronously using V_{TGL} generates a sawtooth output current, as illustrated in Figure 5.7. The sawtooth current waveform adds the possibility of modulating the sub-carrier wave using phase-shift keying (see Figure 2.8 for PSK modulation scheme).

Amplifiers A_1 and A_2 use a 2-stage folded-cascode topology and have 70 dB DC gain and 20 MHz unity-gain bandwidth. The wide bandwidth is required to reproduce a triangle wave with the desired fidelity (i.e., preserving up to the 21st harmonic for a 1 MHz sub-carrier). All current mirror and current sources shown in Figure 5.6 are cascoded and gain boosted to minimize current variation due to supply voltage changes. The G_M block has an effective transconductance of 8.4 μA/V and consumes 30 μA from a 1 V supply.

5.3.4. Regenerative amplifier and bandpass filter

The noise figure of the first amplifier in the receive path must be less than 7 dB in order to obtain an overall sensitivity better than -80 dBm. However, decreasing the noise figure requires higher power consumption, in general [5.3]. Moreover, the amplifier gain should be greater than 30 dB so that the received signal amplitude is sufficient to drive the envelope detector properly. An LC bandpass filter at the amplifier output (i.e., tuned load) converts the received FM-UWB signal into an AM signal. Positive feedback enhances the Q of the LC filter thereby increasing its voltage gain and shrinks the bandwidth to the desired value of 50 MHz, increasing the selectivity and sensitivity of the receiver [5.4], [5.5]. However, the feedback needs to be controlled to avoid oscillation. A calibration circuit that addresses this challenge will be described in the next section (5.3.7). Regenerative amplifiers have a non-linear voltage gain; the highest gain is achieved when the input signal is weakest [5.6].

The regenerative amplifier schematic is shown in Figure 5.8, where M_1 and M_2 form a cascode transconductor that drives an LC tank formed by L_D, C_{BP}, the gate capacitance of M_3 and parasitic capacitances at the drain of M_2. Cascode transistor M_2 increases the isolation between the RF input (V_{RX}) and output (V_{BP}) of the amplifier, while transistor M_3 forms a positive feedback loop at the preamplifier output via coupling between the 2 halves of transformer L_D. The amplifier gain increases quickly as the loop gain approaches unity, but its bandwidth also

decreases as the gain-bandwidth product is approximately constant. The loop gain is given by

$$A\beta = kQ\omega L_D gm_3 \le 1, \tag{5.2}$$

where k and Q are the coupling coefficient and quality factor, respectively, of inductor L_D. The transconductance of M_3 is gm_3, and ω is radian frequency. The loop gain is frequency dependent and depends mainly on fixed parameters of the passive inductor (L_D), so the loop gain can only be varied electronically by changing gm_3. The voltage gain of the overall regenerative amplifier is given by

$$A_V = \frac{V_{BP}}{V_{RX}} = \frac{gm_1 Z_O}{1 - A\beta} = \frac{gm_1 Z_O}{\left(1 - kQ\omega L_D gm_3\right)}, \tag{5.3}$$

where gm_1 is transconductance of M_1, and Z_O is impedance seen at the drain of M_2. It is clear from equation (5.3) that the voltage gain of the amplifier is enhanced by increasing loop gain $A\beta$ (i.e., $A\beta \rightarrow 1$). The 5 pF capacitor C_S forces the source of transistor M_3 to ground at RF. DC current at the source of M_3 (I_{FB}) controls transconductance gm_3, thereby varying the amount of positive feedback. The source voltage of M_3, V_{LV}, at approximately 0.6 V is used as the supply voltage for other blocks (i.e., the envelope detector, IF amplifier and limiter). Bias current I_{FB} shown in Figure 5.8 consists of the DC current drawn by those 3 blocks plus the current drawn or injected by the DAC_{CAL}, which is controlled by control word N_{CAL}.

Inductor L_D is 3.9 nH, with a self-resonant frequency of 9.1 GHz and peak-Q of 19.3 at 4.1 GHz. C_{BP} is determined by a 6-bit capacitor DAC, and can range from 80 fF to 400 fF. The 6-bit word code N_{CDAC} tunes the center frequency of the load resonator in a range from 3.2-4.9 GHz. The DAC is thermometer coded, where a

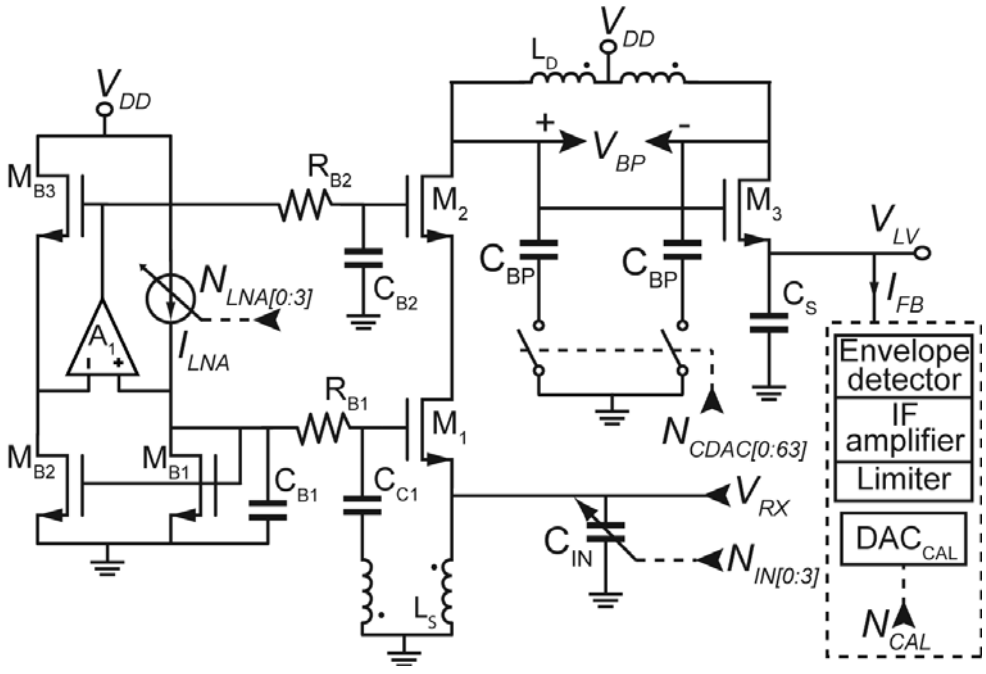

Figure 5.8. Simplified schematic of the regenerative RF amplifier.

row and a column decoder connect V_{BP} to a set of capacitors, from the first capacitor (number 1) to the selected one (e.g., number 28) as illustrated in Figure 5.9(a). The capacitor DAC is not scaled uniformly, instead it scales progressively larger so that there is a linear relationship between the center frequency and word code, and a consistent frequency step as the word code is incremented. A comparison between progressive and uniform scaling from simulation is shown in Figure 5.9(b).

The preamplifier input is matched to 50 Ω across the 3-5 GHz band using matching network C_{IN} and L_S. The matched condition ($|S_{11}| < -10$ dB) is achieved in several sub-bands (with overlap) by varying C_{IN} via 2-bit digital word $N_{IN,}$ which controls the setting of a 2-bit capacitor DAC (see Figure 5.10). Sub-banded input matching automatically realizes minimum noise figure for the preamplifier in each sub-band frequency range, because the signal gain (passive gain due to input

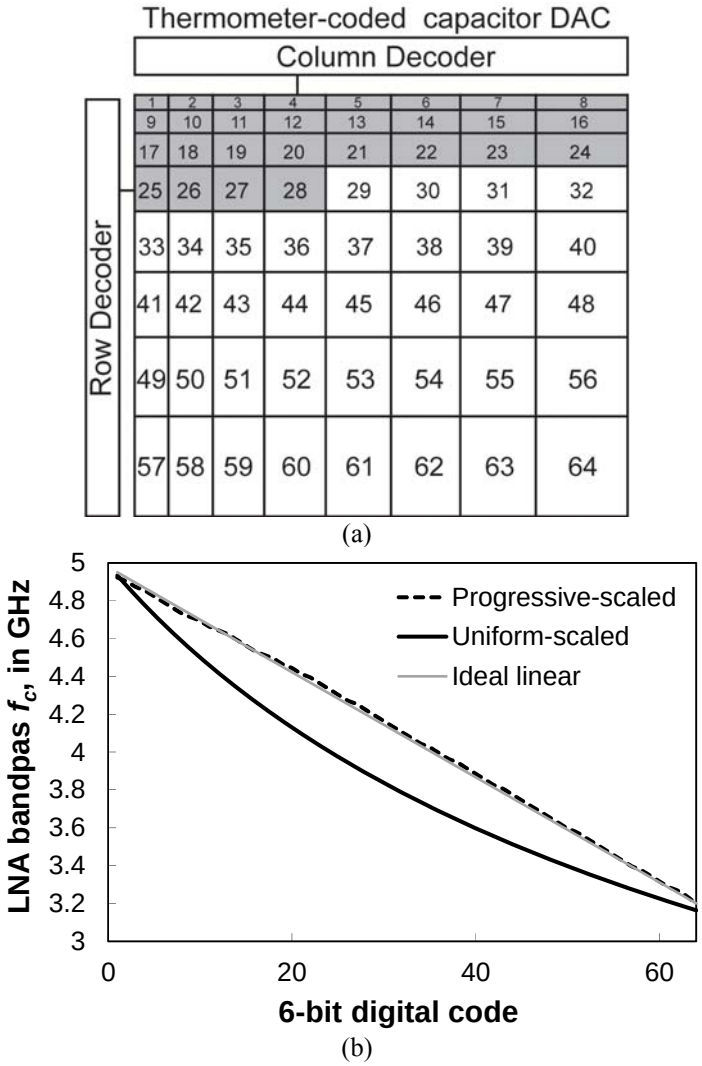

Figure 5.9. (a)Progressively-scaled capacitor DAC illustration and (b) simulation result compared to uniformly-scaled capacitor DAC.

resonant tank) is highest at the frequency where the impedance matching occurs. Inductor (L_S) is 3.6 nH, with a self-resonant frequency of 9.6 GHz and peak-Q of 20.2 at 4.2 GHz. Both L_D and L_S are fully-symmetric on-chip inductors that provide the highest Q-factor in the smallest possible chip area [5.7]. Shunt-series negative feedback at the input of the main amplifier is also provided by L_S, which increases input matching bandwidth from 0.45 GHz to 1 GHz. The opposite phase of the received signal appears at the gate of M_1 via 3 pF coupling capacitor C_{C1}, effectively doubling the input signal amplitude. The larger input signal lowers the 50 Ω noise figure from 9.1 dB (C_{C1} = 0) to 6.6 dB. It should be noted that the main noise contribution comes from (positive feedback) transistor M_3 (28%) and main amplifier transistor M_1 (24%) when the RF input frequency is 4 GHz.

The amplifier is biased using a feedback-controlled replica circuit (A_1 and M_{B1}-M_{B3} shown in Figure 5.8) so that the bias is made insensitive to supply voltage variation without loading the drain of M_1. The measured bias current of the preamplifier varies by just ±1.5% for a supply range of 0.9-1.1 V. A PTAT current biases the amplifier such that the transconductance of the main amplifier is desensitized to temperature changes. Bias current I_{LNA} can be halved or doubled via a 2-bit current DAC controlled by N_{LNA} in order to raise the receiver sensitivity, or to work in a low-power mode. In the high-sensitivity mode, the amplifier noise figure improves when a higher SNR is required at the expense of higher power consumption. On other hand, the noise figure is poorer in the low-power mode, which may be suitable when there is plenty of link margin (e.g., communication across a shorter range).

The regenerative amplifier has voltage gain of 40 dB when it is tuned for optimal positive feedback at a loop gain (Aβ) of 0.9. The regenerative amplifier consumes 0.56 mA from the 1 V supply (0.45 mA for the 1st stage, M_1 and M_2) at 4 GHz operating frequency, which is 75% less power than the FM-UWB amplifier design described in [5.8] for the same voltage gain.

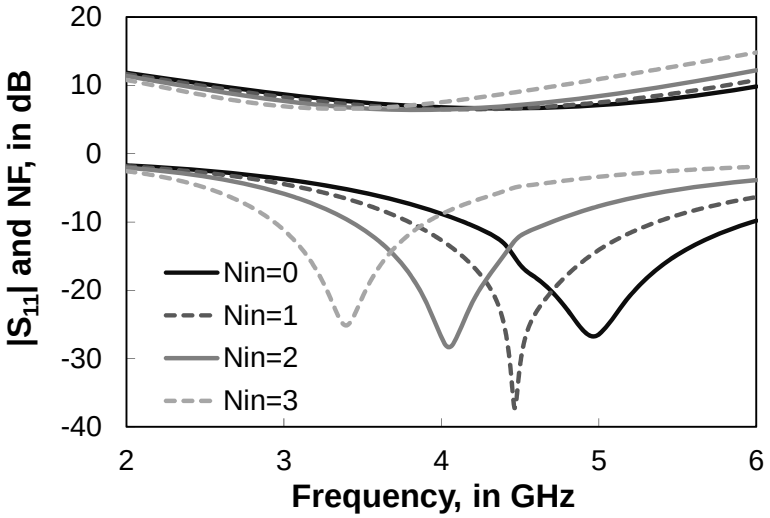

Figure 5.10. Simulation results of the $|S_{11}|$ and noise figure for various N_{IN}.

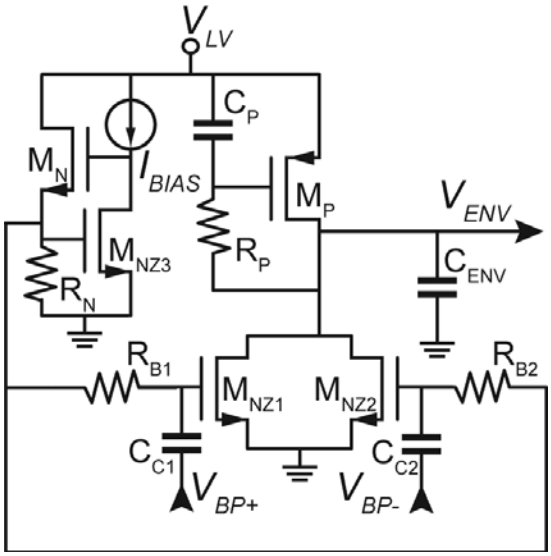

Figure 5.11. Schematic of the envelope detector.

5.3.5. Envelope detector, IF-amplifier and limiter

The envelope detector (see Figure 5.11) removes the carrier from the filtered RF signal. Transistors M_{NZ1} and M_{NZ2} are a differential half-wave rectifier which discharges the 2.7 pF capacitor C_{ENV} when the RF voltage swing peaks at input V_{BP}. Transistor M_P and passives R_P and C_P form an active load that give a high impedance at the IF ($Z_L = ro_p$) and small impedance ($Z_L = 1/gm_p$) at DC. The DC component in the AM input signal after detection comes mainly from thermal noise and any narrowband interference. The envelope detector bias current (I_{BIAS}) is derived from a PVT-compensated current reference. Transistors M_{NZ1}, M_{NZ2}, and M_{NZ3} are matched using native devices that have a very low threshold voltage (typical is 40 mV), which enhances the sensitivity of the envelope detector (simulated input sensitivity is 1 mV_{p-p}). The envelope detector reuses bias current flowing through the regenerative amplifier, thereby saving power. It is biased at 40 μA from the voltage at the regenerative amplifier output (V_{LV} in Figure 5.8 and Figure 5.11), which ranges from 0.5-0.6 V.

The envelope detector is followed by an intermediate frequency (IF) amplifier and limiter, as shown in Figure 5.12. The 3-stage CMOS bandpass IF amplifier formed by transistors M_{N1}-M_{N3}, amplifies the detected envelope by 50 dB. It has a 100 kHz to 10 MHz bandwidth. Resistors R_{B1} and R_{B2} provides a DC feedback path to bias the amplifier, while Miller capacitor C_M sharpens the upper roll-off of the bandpass filter [5.8]. Coupling capacitor C_{IF} provides bias isolation between envelope detector and IF amplifier in the AC signal path. The output voltage of the IF amplifier (V_{IF}) is compared with the reference voltage generated by I_{REF} flowing through resistor R_{REF}, which is set by a 6-bit resistor DAC. Calibration via this DAC compensates for changes in the DC level of the V_{IF} signal and also for the offset voltage of the limiter with hysteresis.

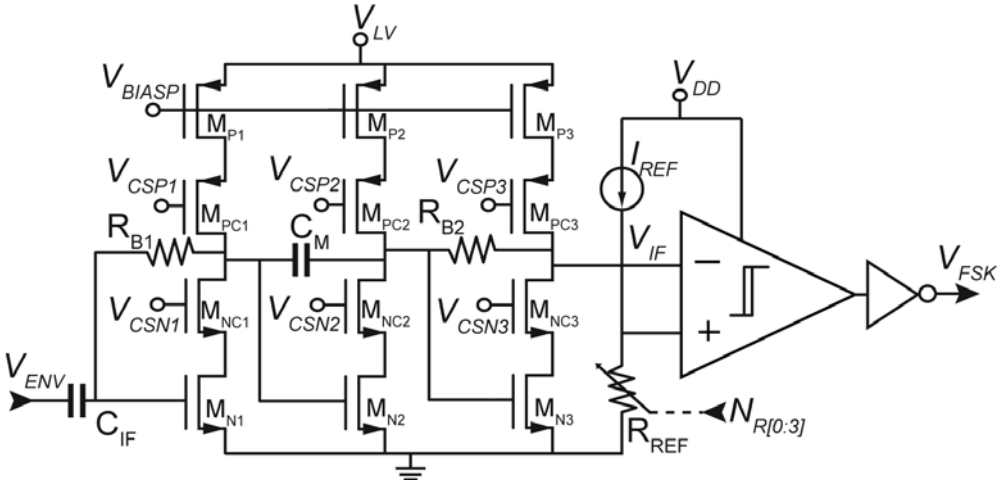

Figure 5.12. Schematic of the IF bandpass amplifier.

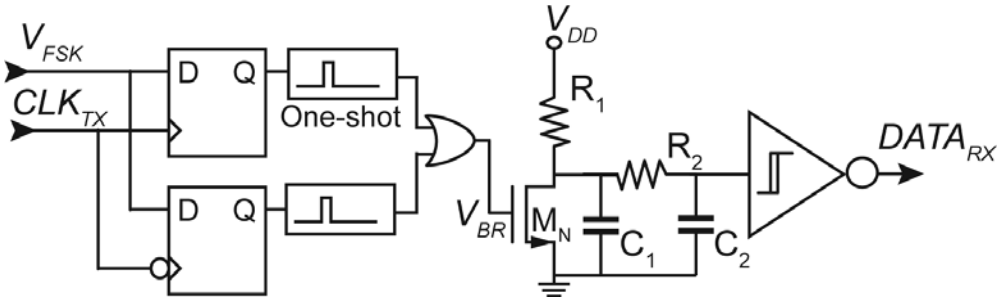

Figure 5.13. Schematic of the FSK demodulator.

Separate bias voltages for cascode devices (V_{CSN1}-V_{CSN3} and V_{CSP1}-V_{CSP3}) are implemented to avoid creating a feedback path from the output to the input of the amplifier, where it may cause instability. A source follower buffer (not shown in Figure 5.12) is included so that V_{IF} may be measured for characterization and debugging purposes. A 2-bit DAC sets the bias current of the amplifier. For example, a higher bias current increases the upper cutoff frequency of the bandpass filter and raises the IF. The IF amplifier consumes 10-20 μA from source voltage V_{LV}, while the limiter consumes 5 μA from a 1 V supply at a 1 MHz IF.

5.3.6. FSK Demodulator

An FSK demodulator that detects the received data by demodulating the recovered sub-carrier IF signal is implemented on-chip. As shown in Figure 5.13, the FSK modulated IF signal (V_{FSK}) is sampled by a clock (CLK_{TX}) sourced from the transmitter's sub-carrier oscillator using two edge-triggered D flip-flops. The sampled FSK signal (V_{BR}) produces a DC signal when V_{FSK} has the same frequency as CLK_{TX}, indicating a bit '0'. Otherwise, it produces a clock at a rate of 2Δf when the received bit is a '1'. One-shot circuits create a short duty cycle pulse (typical is 5 ns) for each of the flip-flops output clock edges. Transistor M_N, which is driven by

the pulses drives low pass filter $R_{1\text{-}2}$ and $C_{1\text{-}2}$ which averages the pulse burst (in the case of a received '1'). The signal is then quantized by an inverter with hysteresis, producing the received data stream. The threshold of the inverter could be adjusted digitally by changing the number of finger of NMOS or PMOS that are active (i.e., connected to the inverter circuit).

The demodulator is non-coherent in that it only requires the received IF bits '0' or '1' to have the same frequency as the on-chip, calibrated sub-carrier oscillator. The demodulator consumes an average of 4.6 μW from a 1 V supply at 1 MHz IF.

5.3.7. Positive feedback calibration

Automatic digital tuning is required to control the positive feedback loop of the regenerative amplifier. Simultaneous frequency and Q-tuning for the RF preamplifier can be supplied by a replica circuit [5.11], however, this method suffers from mismatch, requires additional chip area, and consumes more power. The calibration method implemented here uses direct tuning [5.12], where the feedback is increased until oscillation occurs. In this way, the center frequency is detected and can be tuned using a digital FLL. After calibration of the center frequency the loop gain is reduced (until it is less than unity) to suppress the oscillation. One drawback of this method is that data cannot be received during the calibration. However, the transceiver could be calibrated only when required (this would require some supervision at the system level) in order to minimize this disadvantage of the direct tuning method.

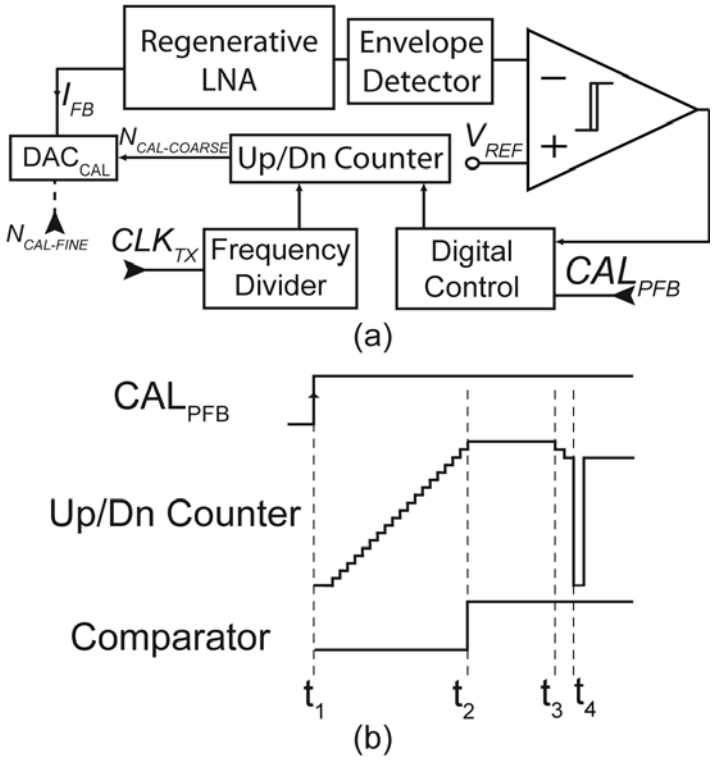

Figure 5.14. Block (a) and timing (b) diagrams for the positive feedback calibration loop.

The block diagram of the feedback calibration sub-system is shown in Figure 5.14(a). The total current of the regenerative amplifier (i.e., I_{FB}) is adjusted by a current DAC, a coarse control word ($N_{CAL\text{-}COARSE}$) with 2.4 μA per LSB and a fine control word ($N_{CAL\text{-}FINE}$) with 0.08 μA per LSB. The $N_{CAL\text{-}COARSE}$ is set by an up/down counter. The $N_{CAL\text{-}FINE}$ with a range of +/- 1LSB of the coarse level is added to fine tune the positive feedback during data reception. Optimization at system level is therefore possible using a preamble in the receive data. The up/down counter is driven by a clock signal from the sub-carrier oscillator through a frequency divider circuit that produces 1 ms/cycle, thus allowing enough time for oscillation to build up in each counter state.

The timing diagram of the calibration cycle is shown in Figure 5.14(b). The DAC is zeroed by resetting the counter, and calibration is initiated by signal CAL_{PFB} at time t_1. The coarse current DAC is increased incrementally by the up/down counter until the envelope detector circuit (shown previously in Figure 5.11) and a comparator detect oscillation (i.e., at t_2 in Figure 5.14). Once oscillation has built up, the SAR-FLL circuitry performs a center frequency calibration (described in the following Section 5.3.8). After the frequency calibration is finished (at t_3), the counter is decremented for a few cycles in order to quench the oscillation. Simulations predict that two cycles (i.e., reducing I_{FB} by 4.8 μA and waiting for 2 ms) sets the amplifier at the optimal value where the RF gain to noise trade-off is optimized, and closed-loop gain Aβ is approximately 0.9. A DAC reset is performed at t_4 for one clock cycle to quell any oscillation that might still occur due to hysteresis in the circuit.

5.3.8. Frequency calibration

As the passive elements (R, L, and C) that define time constants on-chip are varying by (an estimated) ±10%, a frequency calibration scheme is needed to control the operating frequency or frequency range of various blocks. The successive approximation frequency locked-loop (SAR-FLL) is employed to calibrate or directly control the operating frequency. A detailed schematic and description of the operating principle of the SAR-FLL was presented in the Section 3.2.5. Figure 5.15 shows that the RF-ICO, sub-carrier oscillator, and the LC tank in the regenerative amplifier share the same SAR-FLL calibration block through multiplexing (MUX) and de-multiplexing (DEMUX) selection blocks. The CAL_{SEL} control word selects a block that will be calibrated (i.e., selecting one path in the MUX and DEMUX), and the calibration result is stored in a 6-bit register. The RF-ICO and RF regenerative amplifier outputs are frequency divided such that it operates at IF range of 0.5-4 MHz for the calibration loop. A programmable reference clock (CLK_{REF}) with the same frequency range as the IF is assumed available externally (e.g., crystal oscillator with a programmable synthesizer).

The regenerative amplifier (described in Section 5.3.4) center frequency is controlled by the 6-bit capacitive DAC (C_{BP}) through the SAR-FLL calibration loop when it is in oscillation mode. The oscillation frequency is divided by 4096 and compared to the CLK_{REF}. The calibration loop will set the C_{BP} so that the tank resonant frequency is equal to CLK_{REF} times 4096.

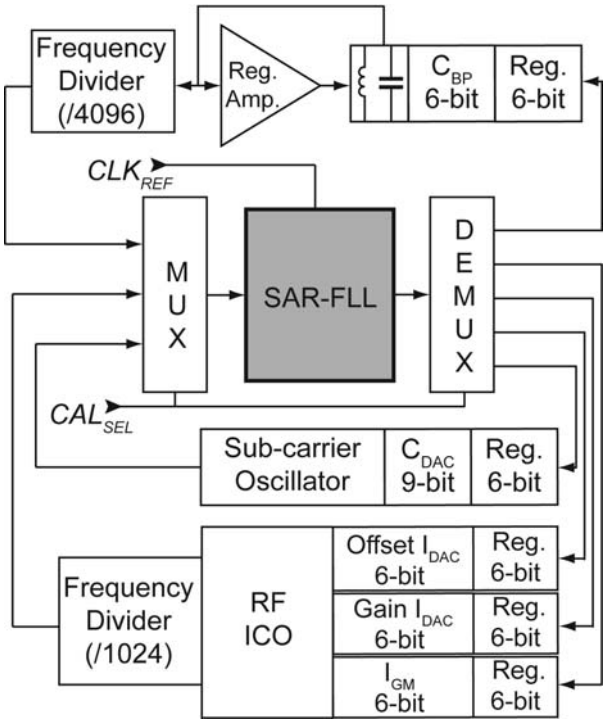

Figure 5.15. Block diagram of frequency calibration scheme for various blocks.

The sub-carrier oscillator frequency (described in Section 3.2.3) is controlled by a 9-bit C_{DAC}. The 3 MSBs are manually controlled to select various bands of sub-carrier frequency. The 6 LSB bits are set by the SAR-FLL such that the sub-carrier frequency (IF) is equal to CLK_{REF}.

The RF-ICO I_{DAC} (see Section 5.3.1) that controls the RF is calibrated such that its frequency range fits the desired operating range. The SAR-FLL calibrates the offset and the slope/gain of the transfer function between center frequency and the DAC control word (N_{ICO}). The SAR-FLL calibrates 3 GHz and 5 GHz center frequencies at N_{ICO} = 0 and 63, respectively. The FM bandwidth is calibrated by controlling the N_{GM} in the GM block (see Section 5.3.3) when its input V_{GM} is set to V_{REFH} at 0.5 V. The carrier frequency is shifted from the center to a lower value, where the difference will be one-half of the desired FM bandwidth.

A tracking loop scheme can be used to compensate for any change in the operating frequency due to temperature or supply changes without interrupting the transmission [5.13]. For example, the RF-ICO frequency can be monitored during modulation, as its average is approximately the same as its center frequency without modulation. All the DAC control bits can be changed manually for characterization purposes and therefore it is possible to use other calibration schemes beside the SAR-FLL. In contrast with successive approximation, where the operating frequency hops around to find the best approximation, the frequency in the tracking loop is only changed step by step. The SAR scheme could be used in conjunction with the tracking loop running periodically in the background.

5.4. Measurement Results

A photomicrograph of the 0.9 mm^2 (including bondpads) transceiver prototype is shown in Figure 5.16. Each pad is ESD protected using a double diode cell from a standard-cell library that offers human body model (HBM) protection of at least 2 kV [3.3]. Receiver and transmitter are separated as far as possible to minimize coupling between them, while the bias and digital circuitry are located between them. All measured results presented in this section are from a test die wirebonded to a custom printed-circuit board (PCB) shown in Figure 5.17. A pair of 200 pF RF coupling capacitors is inserted in the V_{RX} and V_{TX} path to the connector. A set of decoupling capacitors (total value of 0.34 µF) is added for the supply voltage (V_{DD}). The bondwire on the V_{TX} pad is manually placed such that it has a length of

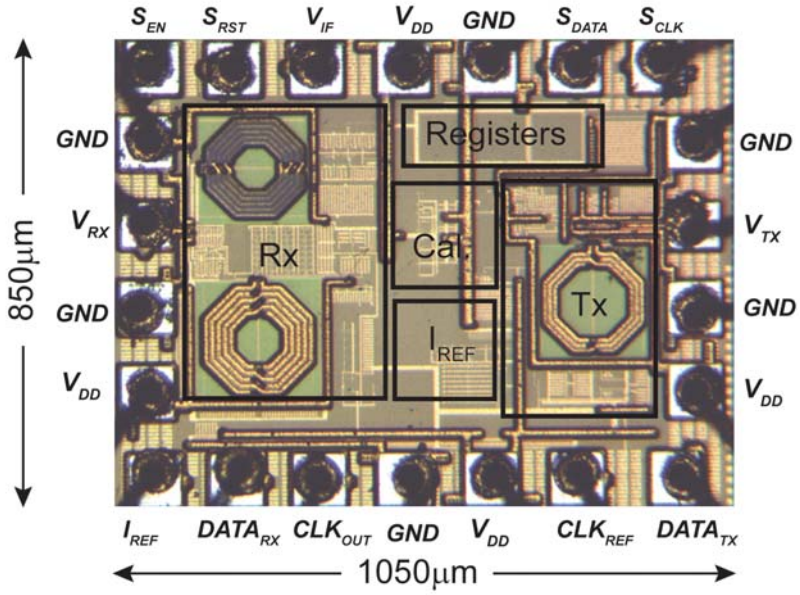

Figure 5.16. Photomicrograph of the transceiver IC.

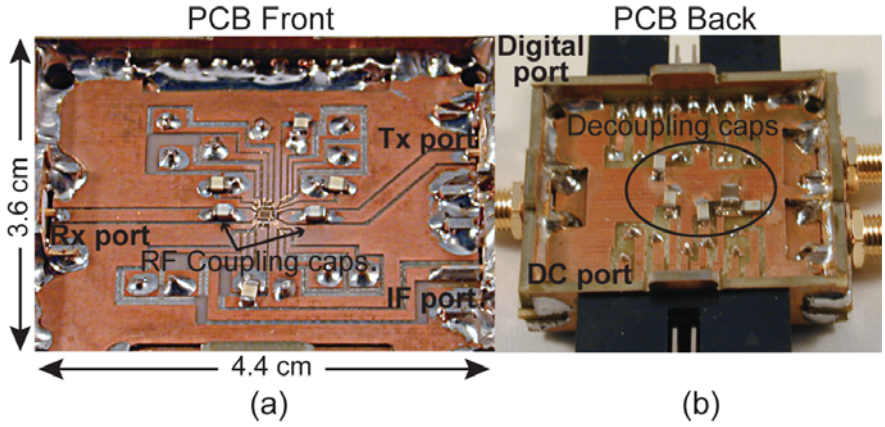

Figure 5.17. (a) Front and (b) back view of the custom made PCB for the transceiver.

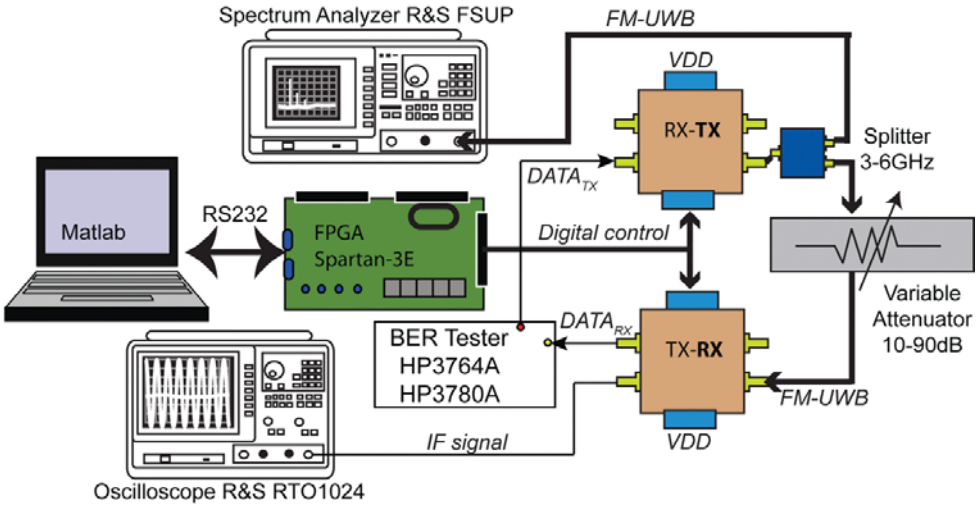

Figure 5.18. Measurement setup for the FM-UWB transceiver.

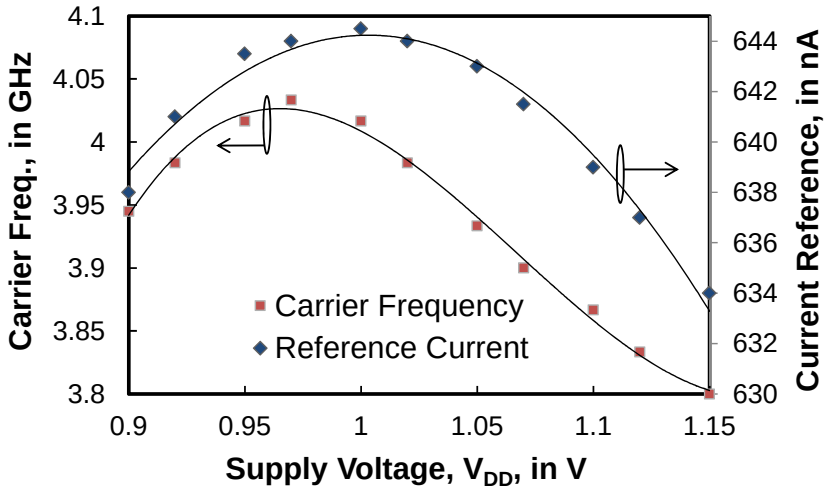

Figure 5.19. Measured reference current and carrier frequency versus supply voltage

approximately 4 mm, because it is part of the output matching network that should give a value close to 4 nH. Figure 5.18 shows the measurement setup, where the transceiver is controlled by a Matlab™ script through a field programmable gate array (FPGA). The FPGA provides serial digital interface to communicate with test chip. The transceiver performance is characterized using a network analyzer, spectrum analyzer, oscilloscope, multimeter, and BER counter.

The transmitted center frequency and internal reference current are measured against supply voltage and temperature changes. There should be correlation between the change in the reference current and the output frequency generated by the RF-ICO. Figure 5.19 shows the variation of the reference current and transmitted carrier frequency versus supply voltage. The measured current has a

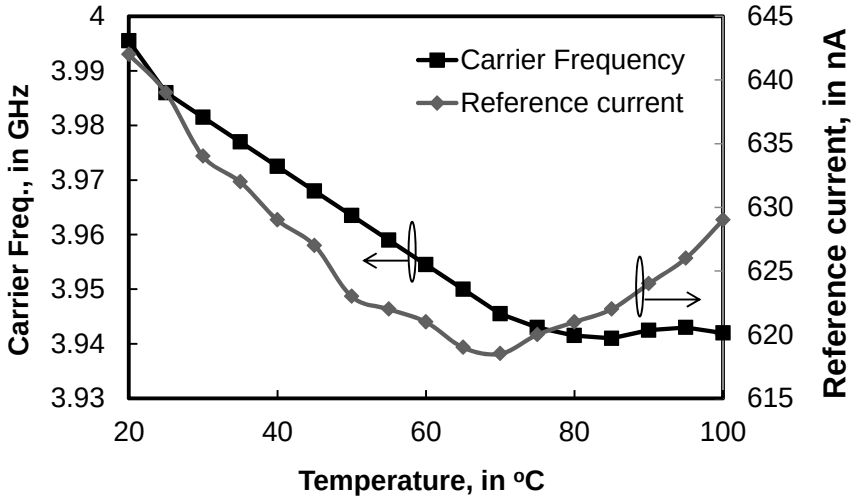

Figure 5.20. Measured reference current and carrier frequency versus temperature.

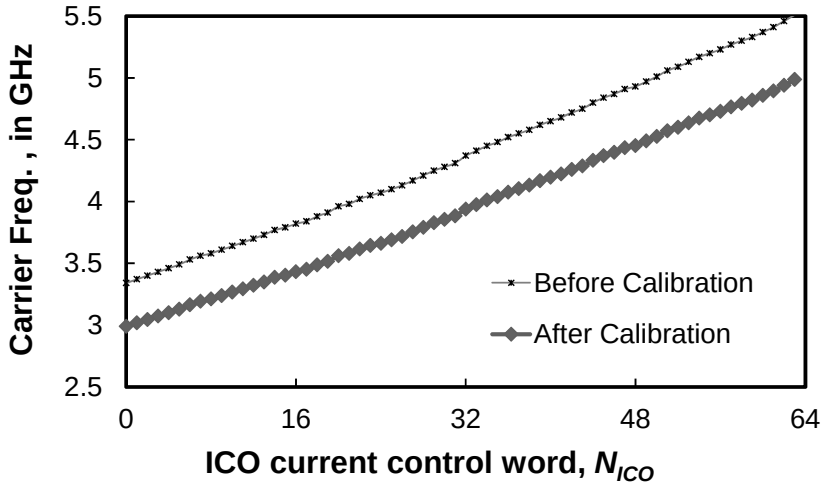

Figure 5.21. Measured carrier frequency versus DAC current controlled by N_{ICO}.

parabolic shape with a peak located at a supply voltage of 1V. The carrier frequency dependency on supply voltage should track the reference current, however, it is shifted slightly. The carrier frequency varies by ±2.5% across supply voltage range of 0.9-1.1 V.

Figure 5.20 shows the variation of the reference current and carrier frequency versus temperature. The PCB was put on a hot plate and the temperature was measured using a thermocouple and multimeter. The carrier frequency falls as the temperature increases, with an average sensitivity of 0.75 MHz/ºC. The carrier frequency is insensitive to temperature between 80-100 ºC, where the current is PTAT. It signifies that a PTAT current could be used to bias the RF-ICO to desensitize the RF-ICO to temperature.

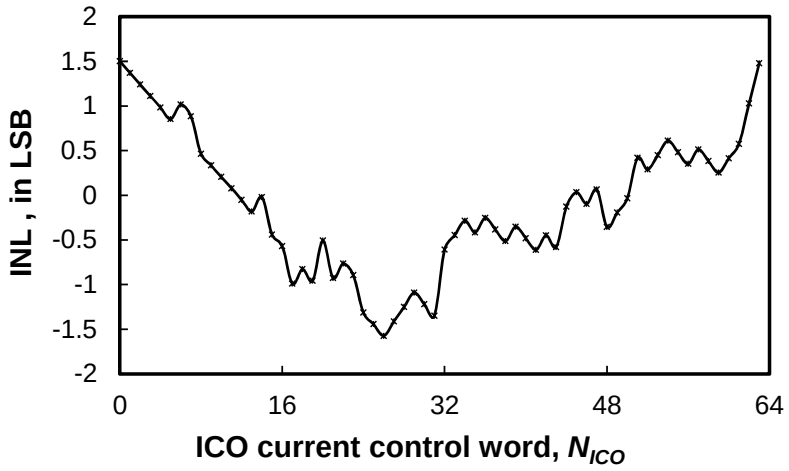

Figure 5.22. Integral non-linearity (INL) of the RF-ICO.

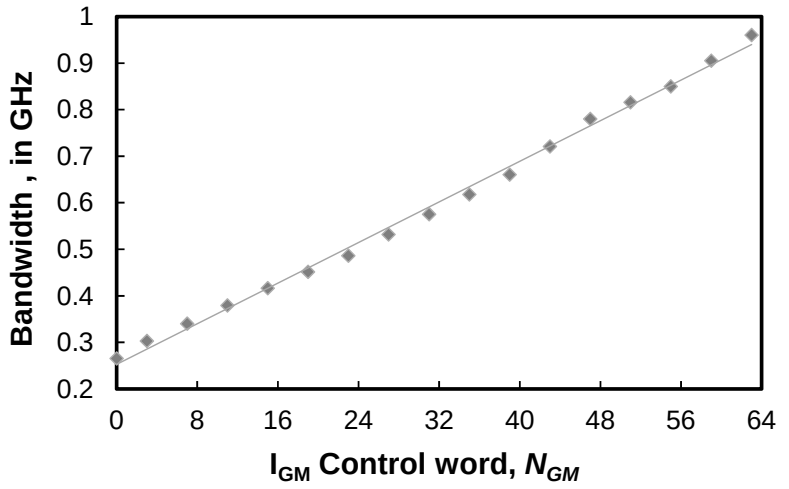

Figure 5.23. Measured FM bandwidth versus DAC current that controlled by N_{GM}.

The transmitter carrier frequency was also measured against the ICO current DAC as shown in Figure 5.21. The default setting for the offset and gain does not give the desired frequency range. However, once the offset and gain are calibrated (see Section 5.3.8), the range easily fits into the desired 3-5 GHz band. The DAC word and carrier frequency have a monotonic relationship, although there is a slight non-linearity. The non-linearity could be caused by mismatch in the DAC and a change in the oscillation amplitude. The integral non-linearity (INL) of the RF-ICO is ±1.5 LSB (see Figure 5.22). The linearity is sufficient to give precise frequency control and a flat FM-UWB spectral density.

The measured FM-UWB modulated signal bandwidth is plotted as function of the GM DAC control word (N_{GM}) in Figure 5.23. The bandwidth can be controlled in the range of 265-960 MHz, and it is linearly related to the GM DAC current.

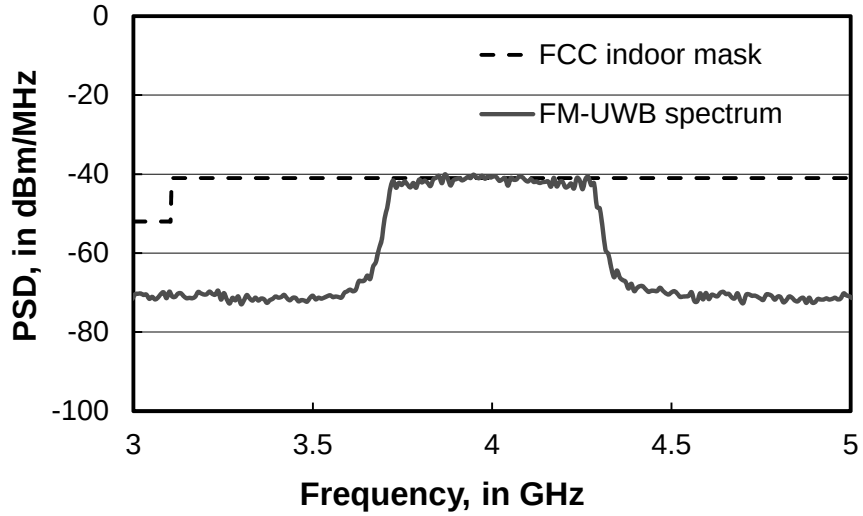

Figure 5.24. Measured FM-UWB modulated signal spectral density.

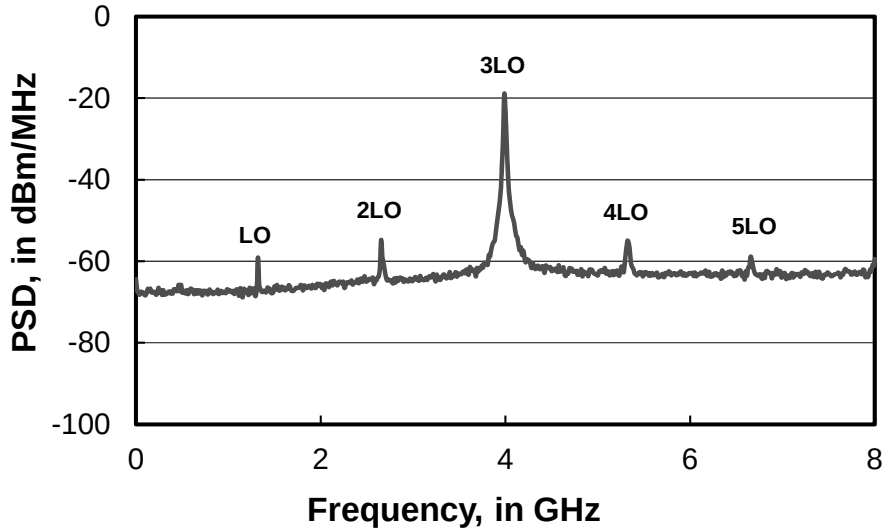

Figure 5.25. Measured unmodulated carrier signal.

The spectral density of the modulated FM-UWB for center frequency of 4 GHz and bandwidth of 500 MHz is shown in Figure 5.24. The output power is adjusted so that it is just below the FCC indoor UWB mask and it is measured under a resolution bandwidth of 1 MHz. The unmodulated carrier spectrum is shown in Figure 5.25, where the sub-harmonic component of the carrier can be seen. All harmonic components exist due to random mismatch in the 3-phase signals that are combined by the frequency tripler. The harmonic components are at least 30 dB lower than the main carrier, and they can be further suppressed by the bandpass response of the antenna.

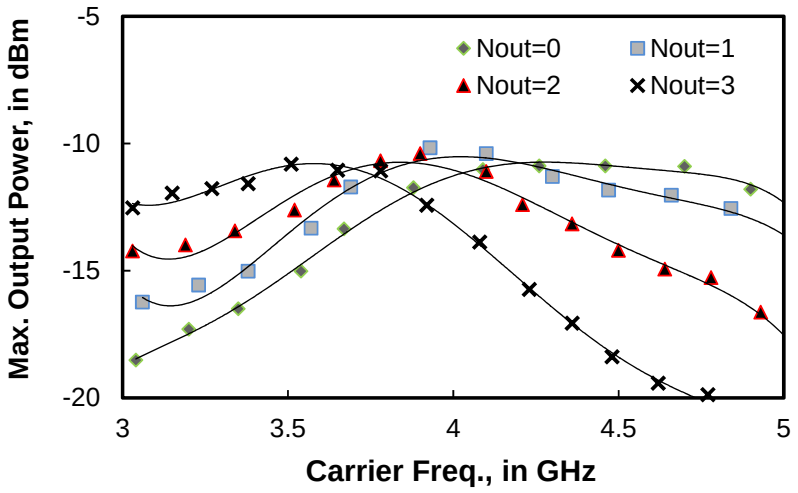

Figure 5.26. Measured A simulated maximum output power of the transmitter versus frequency at various N_{OUT}.

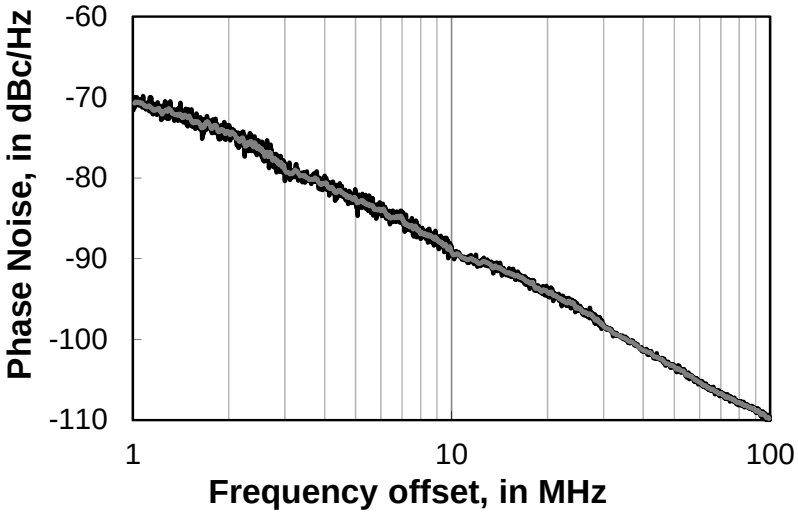

Figure 5.27. Measured phase noise of the carrier signal at 4 GHz.

The transmitter output power versus frequency measured in the 3-5 GHz range is plotted in Figure 5.26 for various output matching conditions (by changing N_{OUT}). Each N_{OUT} setting maximizes the transmitted output power in a sub-band. The maximum output power at 4 GHz is -10.1 dBm, which is 1.5 dB lower than the expected value from simulation. The discrepancy could be caused by extra losses in the bondwire, PCB trace, and connector. The N_{PA} control word varies the output power in steps from -10.1, -11.2, -12.8, to -14.8 dBm, and the transmitter consumes 0.72, 0.67, 0.63, and 0.57 mW of DC power, respectively, at each output power level. An output power of -14 dBm is sufficient to transmit a 500 MHz bandwidth FM-UWB signal at the maximum allowable spectral density. Figure 5.27 shows the

measured phase noise of the output carrier signal at 4 GHz and an output power of -10.1 dBm. The phase noise is -70.7 dBc/Hz at 1 MHz offset. The phase noise result is comparable to the previous transmitter design described in Chapter 3, and still meets the specification with 8.7 dB margin.

The receiver input impedance is reflected in the S_{11} measurement result shown in Figure 5.28. The result is close to the simulation result shown in Figure 5.10, where the receiver can be matched ($|S_{11}| < -10$dB) within a 1 GHz range, but to cover the 3-5 GHz range, a sub-band matching condition with overlap is desired. The results show that a tunable matching network is realized in CMOS technology.

The measured resonant frequency of the regenerative amplifier is shown in Figure 5.29. It is measured when the regenerative amplifier operates on oscillation

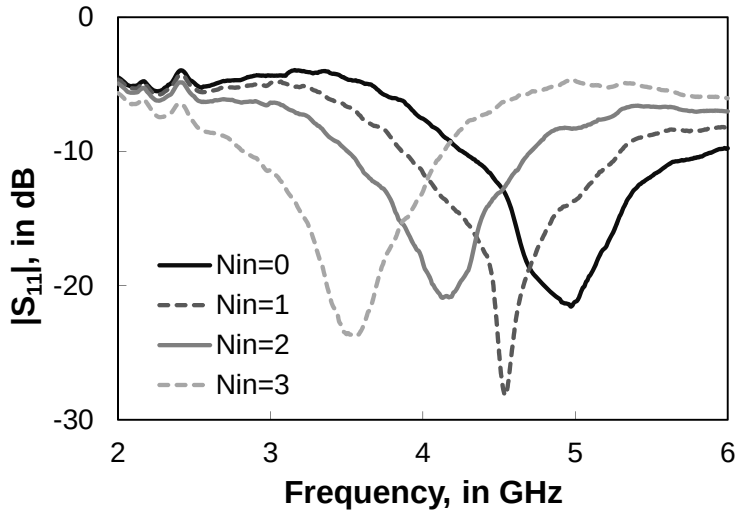

Figure 5.28. Measured $|S_{11}|$ of the receiver at various input matching conditions.

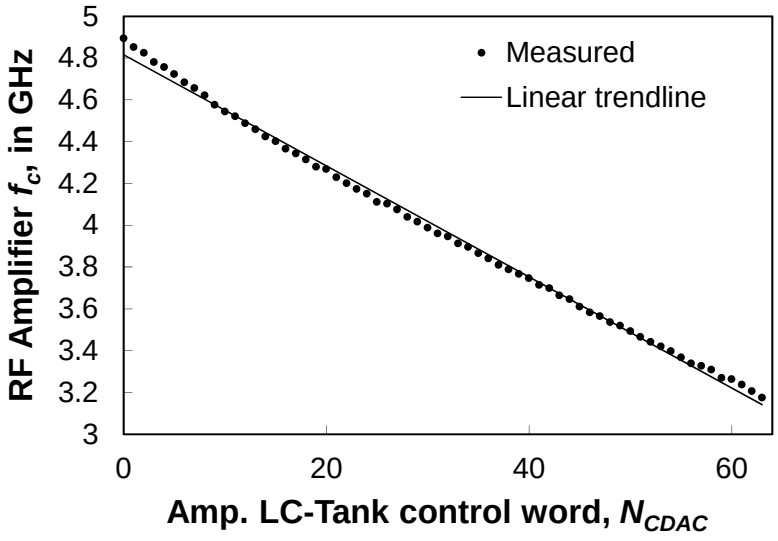

Figure 5.29. Measured resonant frequency of the regenerative amplifier.

mode and its output frequency is divided by 4096, which could be measured through the output clock buffer at CLK_{OUT}. Although progressive scaling is used, there is still non-linearity due to parasitics and processing variation in the capacitance values of the DAC.

The IF pulse generated by the envelope detector is measured via an on-chip buffer. The measured pulses at an IF of 3.2 MHz are shown in Figure 5.30 for an RF carrier of 4 GHz at a power of -70 dBm. It can be observed from the pulses that there is AM noise, which is removed by a limiter. A Fourier transform of the 1 MHz IF pulses is also shown in Figure 5.31 (2-FSK modulated at 100 kbit/s data rate).

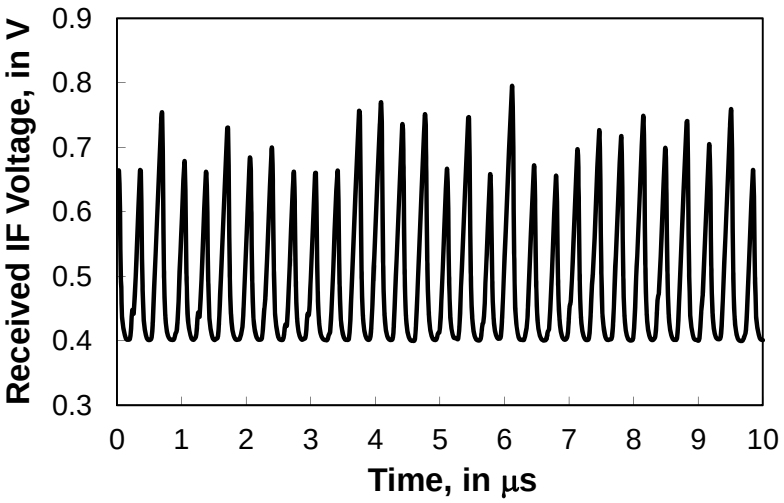

Figure 5.30. Measured IF pulses when the transceiver received -70 dBm FM-UWB signal.

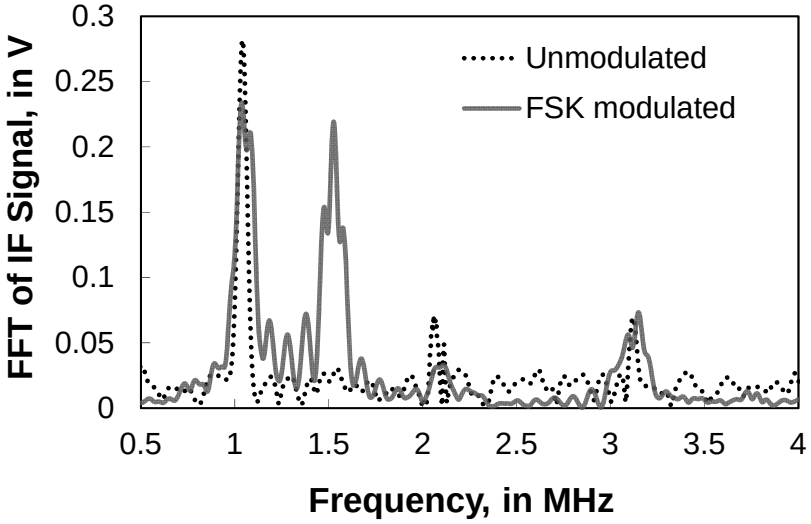

Figure 5.31. An FFT of the received IF signal with and without FSK modulation.

The frequency spacing between the tones is around 500 kHz in this case. It can be controlled by the relaxation oscillator in the transmitter. The frequency spectrum of an unmodulated signal is also shown for comparison.

The FSK demodulator will detect the quantized IF pulse by sampling it using the same clock frequency (e.g., 1 MHz or 1.5 MHz clock for the IF in Figure 5.31). If the sampling rate and the IF are the same, then no pulse is generated, and vice-

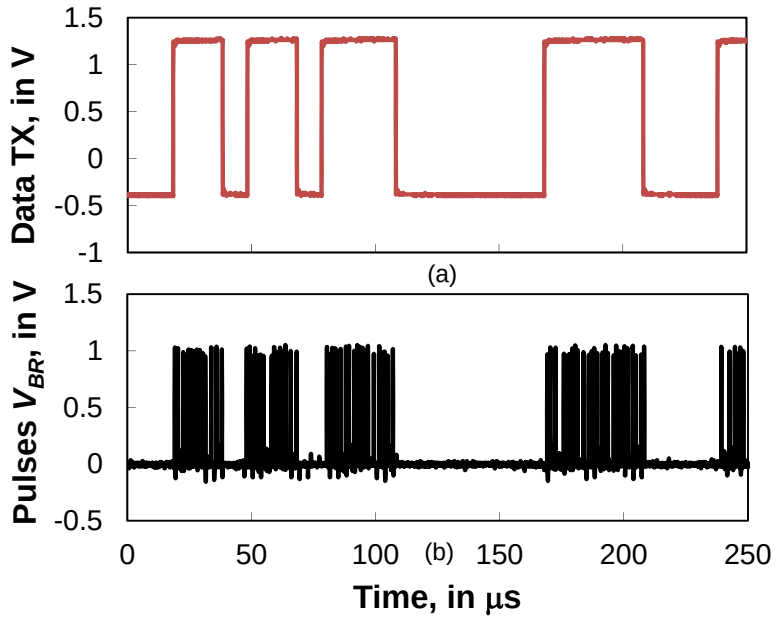

Figure 5.32. Measured pulse burst from the FSK demodulator.

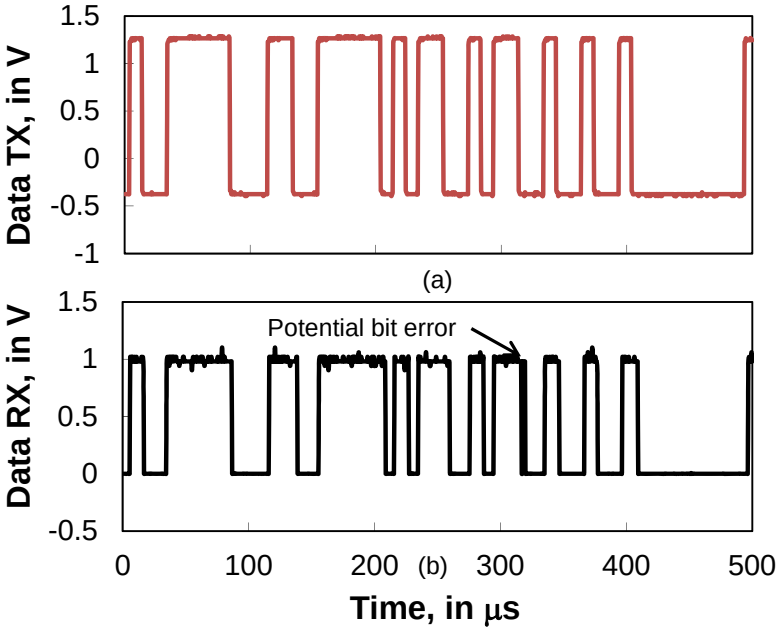

Figure 5.33. Measured received bit compared with transmitted bit.

versa. The measured pulse burst shown in Figure 5.32 is correlated (i.e., burst of pulses when data is '1', no pulses when data is '0') to the transmitted pseudo-random binary sequence (PRBS) data. The received bits for a data rate of 100 kbit/s and input power of -70 dBm are shown Figure 5.33. The received bits are identical to the transmitted bits, but occasionally there is a glitch that could be interpreted as an error by the receiver. If the RF input signal power is reduced, the occurrence of the glitches increases.

The bit error rate of the received data bit is also plotted against the received power in Figure 5.34 for a 4 GHz RF carrier under various conditions (i.e., different receiver DC powers and a higher data rate of 200 kbit/s). The regenerative

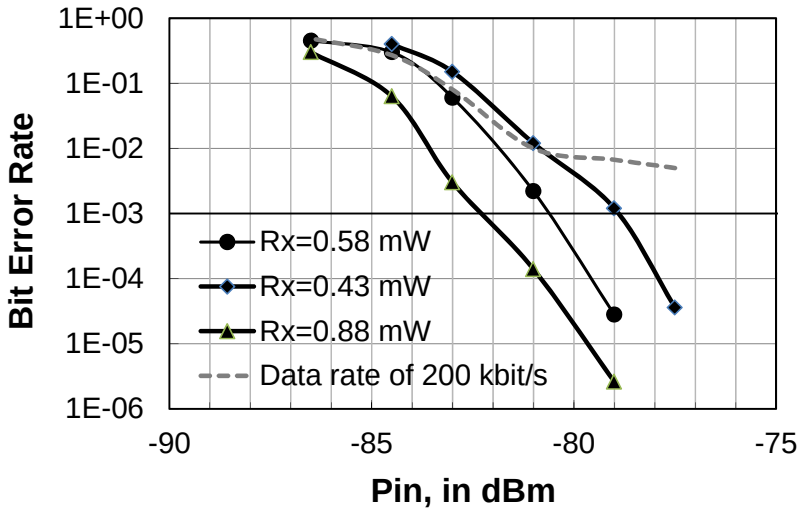

Figure 5.34. Measured BER versus received power for various Rx DC power consumption settings and data rates.

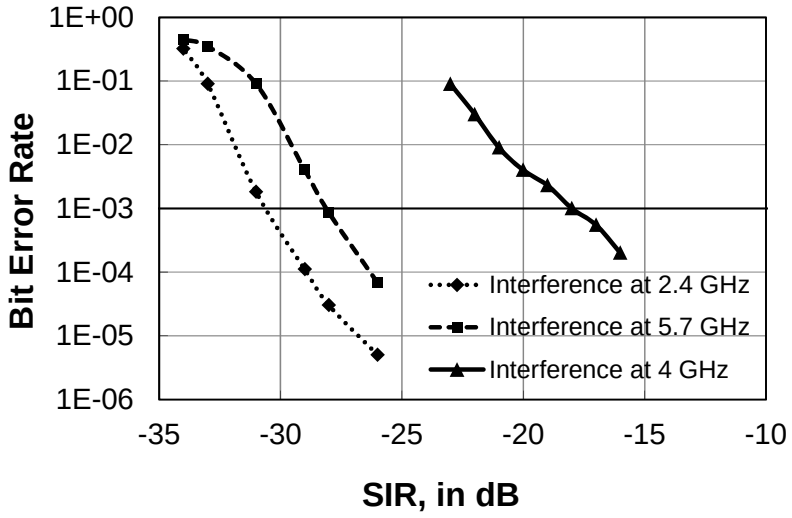

Figure 5.35. Measured BER versus SIR for various single-tone interference frequencies.

amplifier bias can be controlled by the control word N_{LNA} to improve its noise figure at the expense of greater power consumption (see Figure 5.8). The noise figure directly affects the bit error rate (BER) and sensitivity (sensitivity is defined by input power when BER is 10^{-3}). The default setting (i.e., when the receiver consumes 0.58 mW) gives a sensitivity of -80.5 dBm, while the lower (0.43 mW) and higher (0.88 mW) power receiver setting give sensitivities of -79 dBm and -82.5 dBm, respectively. The data rate in this receiver does not change the BER curve, however, at a data rate of 200 kbit/s the BER is limited to 5×10^{-2}. This is because of the limited bandwidth of the FSK demodulator. When an external demodulator is used, this constraint on the data rate is relaxed.

The sensitivity to a single-tone interference is also measured by detecting the degradation in BER as shown in Figure 5.35. The signal-to-interference ratio (SIR) measures the strength of the input signal compared to interference, and is negative when the interference power is stronger than input signal. The interference at frequencies of 2.4 and 5.7 GHz (ISM bands) gives an SIR limit (for BER of 10^{-3}) of -32 and -28 dB, respectively. In-band interference at 4 GHz can only be tolerated at

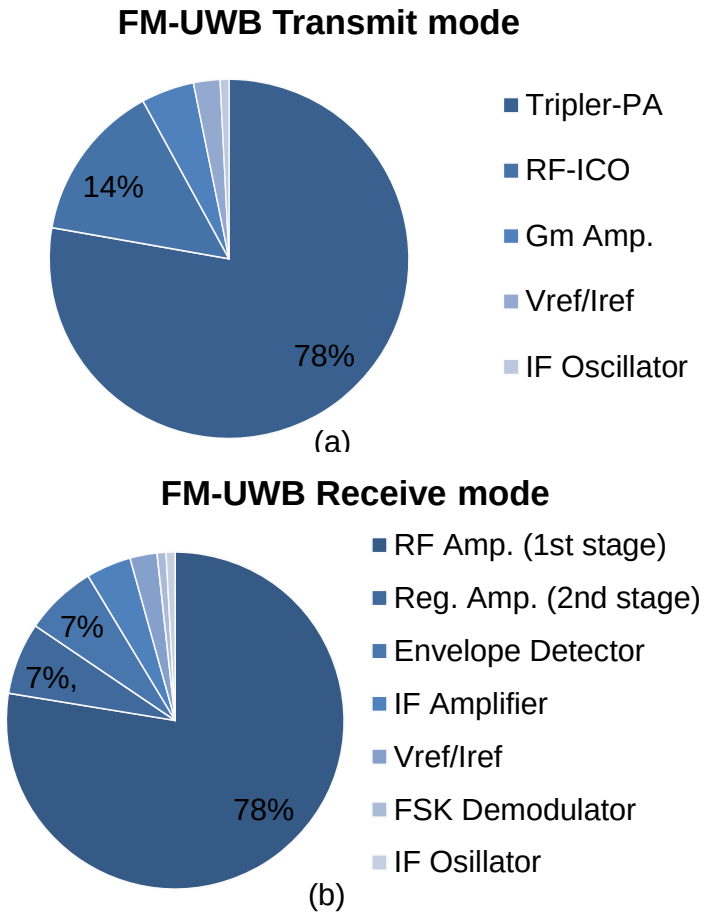

Figure 5.36. Power consumption distribution of the FM-UW transceiver for (a) transmit mode and (b) receive mode.

an SIR level of -18 dB.

Figure 5.36 shows the power distribution among various building blocks for the FM-UWB transceiver in transmit and receive mode, respectively. The PA that delivers the signal to the load consumes the most DC power (78%) in the transmitter. Improving the PA can directly benefit the overall power efficiency. On the receiver side, the LNA consumes the biggest portion of DC power (78%).

Table 5.1 shows a summary of the transceiver performance compared to recent FM-UWB transceivers published in the literature. This work is the first full transceiver that includes back-end processing in CMOS technology. The transceiver is compact and consumes only 0.55 mm^2 of active area, and achieves an average (Tx and Rx) energy efficiency of 6 nJ/bit at a data rate of 100 kbit/s. The transceiver is digitally controllable and consumes only 7 µW when put into standby mode (i.e., part of the bias circuit is turned on to get less than 1µs wake-up time). The transmitter efficiency is 13.3%, which is an improvement from previous FM-UWB transmitter in [5.2]. The measured receiver sensitivity and in-band SIR are -80.5 dBm and -18 dB, respectively. The performance meets the specification but is poorer compared to the previous receiver in [5.8]. The degradation in sensitivity is caused by the non-optimal on-chip FSK demodulator; the sensitivity is improved by 3.4 dB if the IF signal is demodulated using external demodulator (described in Section 4.4). Overall, the fully integrated transceiver is suitable for low power, low data rate wireless applications that rely on energy scavenging to power the device.

TABLE 5.1 FM-UWB TRANSCEIVER PERFORMANCE SUMMARY

Parameters	**This work**	**[5.14]**	**[5.15]**	**[5.2], [5.8]**
Technology	CMOS 90nm	CMOS 180nm	CMOS 130nm, SiGe BiCMOS	CMOS 90 & 65nm
RF range, in GHz	3-5	3.43-4.27	7.2-7.7	4-5
V_{DD}, in V	1	1.6	1.1, 2.5	1
Phase noise, in dBc/Hz at 1 MHz	-71	-90	-107	-75
Max. Output Power, in dBm	-10.1	-13.7	-10	-10.2
Bandwidth, in MHz	265-960	560	500	500
Sub-carrier Frequency, in MHz	0.5-4.3	13.2	1-2	0.8
Receiver sensitivity at BER = 10^{-3}, in dBm	-80.5	-70	-87	-84
Signal to interference ratio, in dB	-18	-	-20	-30
Data rate, in kbit/s	100	50	100	100
Tx power consumption, in µW	630	8700	5000	900
Tx max. power efficiency, in %	13.3	0.5	2	9.1
Rx power consumption, in µW	580	7200	14000	2200
Standby power consumption, in µW	7	-	-	-
Active area, in mm^2	0.56	2.2	0.94	0.4
Tx energy efficiency, nJ/bit	6.3	174	50	9
Rx energy efficiency, nJ/bit	5.8	144	140	22

TABLE 5.2 LOW POWER TRANSCEIVER PERFORMANCE COMPARISON

Parameters	This work	[5.16]	[5.17]	[5.18]	[5.19]
Standard	FM-UWB	900 MHz ISM	Super-Regen.	2.4 GHz ISM	Super-Regen.
Technology	CMOS 90 nm	CMOS 180 nm	CMOS 180 nm	CMOS 130 nm	CMOS 180 nm
Modulation	2-FSK	OOK	OOK	BFSK	BFSK
RF band, in GHz	3-5	0.9	1.9	2.4	2.4
Power Consumption, in mW (Tx/Rx)	0.63/0.58	3.1/ 2.4	1.6/0.4	1.12/ 0.75	1.15/0.215
Receiver sensitivity, in dBm	-80.5	-71	-100.5	-	-86
Max. Output Power, in dBm	-10.1	-10	-4.4	-5	-5.2
Data rate, in kbit/s	100	1000	5	300	125
Signal to interference ratio, in dB	-18	-	-	-	-
Energy efficiency, in nJ/bit (Tx/Rx)	6.3/5.8	3.1/2.4	320/80	2.3/ 2.5	9.2/1.7
Active area, in mm^2	0.56	0.9	0.7	0.8	0.55

5.5. Conclusions

A fully-integrated FM-UWB transceiver for the 3-5 GHz band which benchmarks the scheme for potential low-power, short-range applications has been realized in a 90 nm bulk CMOS technology. The 0.9 mm^2 full transceiver IC demonstrator consumes just 630 μW in transmit mode and 580 μW for the receive mode from a 1 V supply. The transmitter generates a maximum RF output power of -10.1 dBm and achieves a power efficiency (RF output power divided by DC power) of 13.3%. The receiver achieves a sensitivity of -80.5 dBm at a BER of 10^{-3} and in-band SIR of -18 dB from an NBI. On-chip calibration was implemented to tune the center frequency of various blocks in the FM-UWB transceiver. The average energy consumption of the transceiver is 6 nJ/bit at a data rate of 100 kbit/s in continuous operation, with a standby power consumption of 7 μW. The transceiver is therefore suitable for low data rate, portable wireless applications powered from a battery or an energy harvester.

Table 5.2 lists performance comparison between the FM-UWB transceiver and other low power transceivers from the literature. In term of energy efficiency, this work achieve few nJ/bit and comparable to the other transceivers. FM-UWB has an advantage compare to other narrowband transceiver in term of in-band SIR. Additionally, FM receiver is generally more robust to amplitude noise compare to AM/OOK. This work also has the smallest chip area implementation among the other transceivers, which is suitable for low-cost application.

Further improvements can be made, especially in the FSK demodulator block, where it is seen to limit the sensitivity and data rate of the receiver. By employing

more digital techniques and migrating to a smaller feature size (e.g., 65 nm CMOS), the chip area and power consumption can be reduced further while maintaining performance.

5.6. References

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CHAPTER 6. POWER MANAGEMENT FOR FM-UWB

6.1. Introduction

Wireless devices in an autonomous wireless network require electrical energy in order to operate and communicate with each other. Conventional approaches using energy stored in a battery limit the active time when wireless communication takes place and/or the operational lifetime of the device itself. To get unlimited operation time, it is desirable to have energy sources that can be harvested regularly in an autonomous system. Research into energy harvesting has increased rapidly in recent years as indicated by the number of publications that contain the keywords "energy harvesting" (610 publications in year 2011), listed by the IEEE-Xplore™ website (see Figure 6.1).

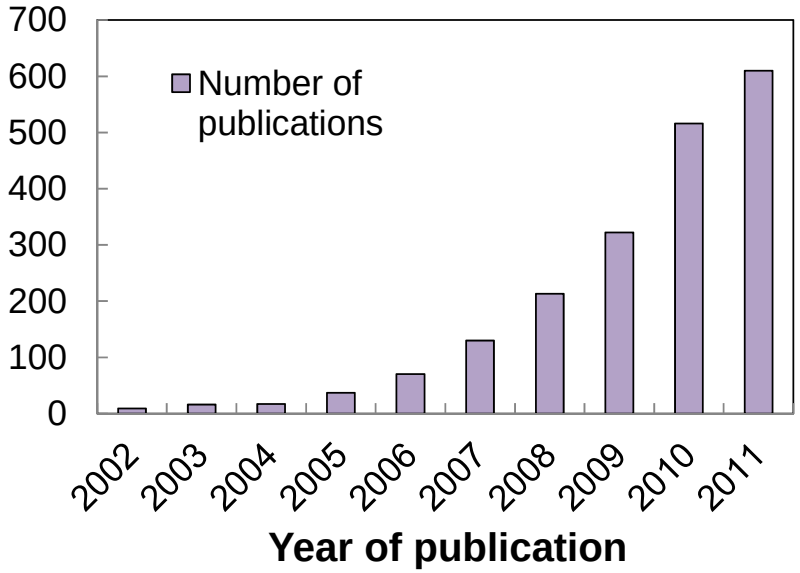

Figure 6.1.Numbers of publications that contain the keywords "energy harvesting" listed on the IEEEXplore™ website in recent years.

TABLE 6.1 POWER ESTIMATES FOR MICROWATT ENERGY HARVESTING [6.5]

Energy source	Condition	Harvested power density
Vibration	Human	4 μW/cm^2
	Machine	100-800 μW/cm^2
Thermal (temperature difference)	Human	5-25 μW/cm^2
	Industrial	1-10 mW/cm^2
Light	Indoor	10-100 μW/cm^2
	Outdoor	10-25 mW/cm^2
Microwave	GSM	0.1 μW/cm^2
	WiFi	0.001 μW/cm^2

Different energy source can be chosen, for example: light, thermal, vibration, and microwave, as listed in Table 6.1. In this work, a photovoltaic or solar cell is chosen because it generates the most energy for a surface area of just a few cm^2 indoors. Furthermore, recent research has demonstrated that it is also feasible to use a solar cell as the substrate for an antenna in wireless applications, thereby realizing a compact system [6.1]-[6.4]. A silicon solar cell achieves a typical efficiency of 10% and power density of 10 mW/cm^2 on a bright sunny day (e.g., irradiated at 1000 Watt/m^2) [6.5]. However, less than 1% of its maximum output power can be generated using indoor illumination. A 2 x 2 cm^2 solar antenna (solant) is employed as an energy source for this work [6.6].

Unfortunately, solar energy as well as other renewable energy sources are intermittent. Therefore, energy is not available from the solant at all times (e.g., in darkness) unless harvested energy can be stored in quantities sufficient to meet the demands of a wireless sensor node at any time (e.g., load leveling). Furthermore, if the system itself is not running continuously, the energy demand by the sensor node on the power supply is intermittent as well. Electrical energy storage is therefore required. Energy harvested from the solant can be stored on a capacitor, a supercapacitor or a rechargeable battery. A "normal" capacitor is too small, and a battery cannot be charged/discharged fast enough unless it occupies very large volume compare to a supercapacitor. A supercapacitor greater than 1 F can store enough energy from a solar antenna to level the energy demand from a sub-mW wireless sensor node in applications such as wireless sensor network (WSN), wireless medical body area network (WMBAN), etc. (see Chapter 1).

The wireless front-end in the autonomous wireless system typically consumes most of the overall system power [6.7]. A robust wireless transceiver for autonomous system applications utilizing FM-UWB modulation that consumes less than 1 mW has been described in Chapters 3-5 of this thesis [6.8], [6.9]. Other circuit functions, such as an on-chip sensor, memory and microcontroller may be included, depending on the application. The supply voltage for the low power

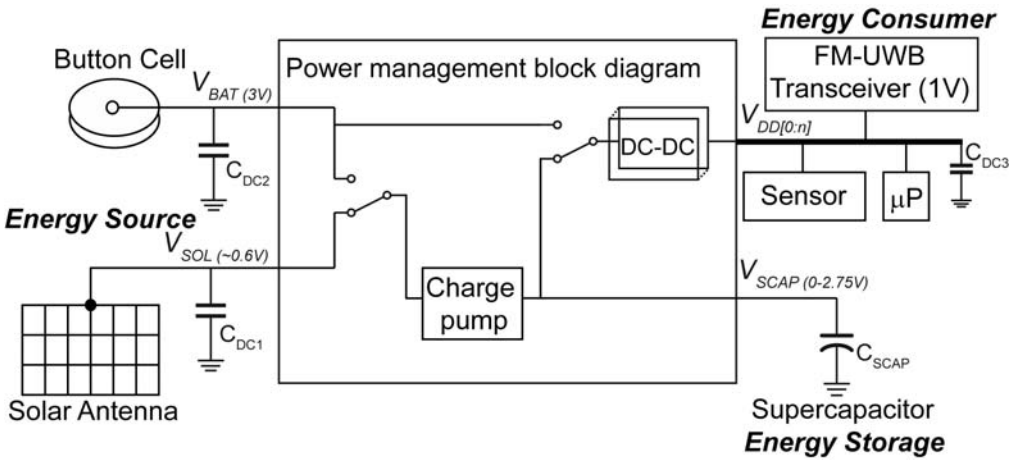

Figure 6.2. Block diagram of the power management scheme for an autonomous wireless system.

CMOS transceiver is 1 V (typical), while other circuits implemented in different technologies may have different supply voltage requirements.

Connecting the energy harvester directly to supply the wireless sensor system (assuming that all circuits run from the same nominal supply voltage) will yield poor efficiency and is unreliable because the harvested supply voltage and current depends on the operating conditions of the solar cell (e.g., intensity of illumination). A power management sub-system is therefore required to provide a regulated DC supply to the autonomous wireless system, store harvested energy and generate optimum interfaces for transducers.

The objectives of this work are to design and characterize a power management sub-system that demonstrates the feasibility of an autonomous wireless system. The power management scheme shown in Figure 6.2 consists mainly of switches and a DC-to-DC converter. Energy is drawn from the battery initially in order to bootstrap the system (i.e., when there is no energy stored on the supercapacitor). Energy produced by the solar antenna can then be accumulated onto supercapacitor C_{SCAP} via the charge pump. This energy could be stored for a few days, but it will diminish as there is a small leakage in the supercapacitor. The DC-DC converter draws energy from the supercapacitor to operate the FM-UWB transceiver, sensor and digital processing circuitry, when enough energy has been stored. It converts a voltage ranging from 0.6-2.75 V (i.e., V_{SCAP}) to a regulated supply voltage of 1 V used in the transceiver. Several DC-DC converters might be needed to supply other power consumers that require different supply voltage.

The technical background of the power management building blocks, namely, the solar cell, battery, supercapacitor, and DC-DC converter are described briefly in Section 6.2. The architecture and building blocks of the power management test chip and the design of each of the circuit block are detailed in Section 6.3. Experimental measurements of a prototype realized in 90 nm CMOS are then presented, followed by a brief comparison with other power managements reported from the literature in Section 6.4. Conclusions and suggestions for future work are summarized in Section 6.5.

6.2. Power management background

Batteries as an energy source as well as energy storage element are considered in this section. The solar cell as an energy source will also be described, along with its electrical model and characteristics. Supercapacitor technology used to store charge is then described briefly. Finally, various DC-DC converter circuits along with their advantages and disadvantages are discussed.

6.2.1. Solar cell

The solar cell converts light energy from the sun to electricity. It is based on the photovoltaic effect, where a potential difference is generated at the junction of two different semiconductors in response to illumination by visible light (or other wavelengths). Free charge carriers are generated when photons are absorbed by materials forming a diode junction. Subsequently, the photo-generated charge carriers are separated and collected at the positive (anode) and negative (cathode) terminals of the cell. Photons within a specific range of frequencies depending on the bandgap of the material are absorbed and generate electron-hole pairs. Thus, different types of solar cell are sensitive to different wavelengths (λ) of light, for example, an amorphous-silicon (a-Si) solar cell is sensitive to wavelengths of 0.4-0.7 μm, while single-crystal silicon solar cells respond to 0.7-1.05 μm [6.10].

The solar cell is modeled as a diode and a current source as shown in Figure 6.3(a). The electrical losses intrinsic to the solar cell are modeled by shunt and series resistors R_{SH} and R_{SE}, respectively. A typical I-V curve for a solar cell is illustrated in Figure 6.3(b). Maximum power output, $P_{MAX,}$ from the solar cell is obtained at the knee of the curve, which corresponds to the optimum power voltage, V_{PMAX}. Short circuit current (I_{SC}) flows though the external circuit when the electrodes of the solar cell are short circuited. The open circuit voltage (V_{OC}) is the

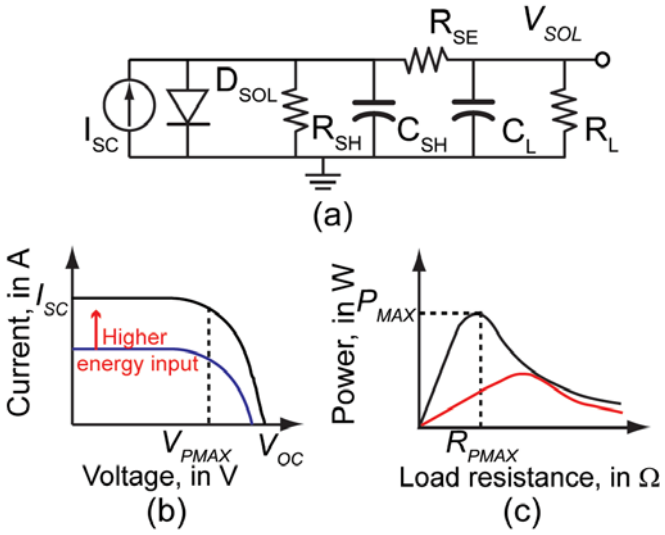

Figure 6.3. (a) Simplified electrical model of a solar cell, and (b) I-V relationship, and (c) power versus R_L for a solar cell.

terminal voltage when no current flows through the external circuit, which is the maximum voltage that a solar cell can deliver. V_{OC} corresponds to the voltage across a forward biased p-n junction, and typically ranges from 400-900 mV depending upon the material used to fabricate the solar cell and the light intensity [6.10]. As the energy of the arriving photons increases, the I-V curve shifts upward, increasing I_{SC} dramatically while V_{OC} is only changed slightly. The fill factor is defined as the ratio between P_{MAX} and $I_{SC} \times V_{OC}$. It is a figure of merit indicating the quality of the solar cell. A typical value of the fill factor for amorphous silicon is 0.8 [6.10]. Figure 6.3(c) shows the output power versus load impedance, which indicates that there is an optimum load resistance which generates P_{MAX}. At a lower light input power, the optimum resistance shifts to a higher value. Therefore, an electronic interface that is attempting to collect energy from the solar cell as efficiently as possible under various lighting conditions should match the load impedance to the cell impedance in order to obtain the maximum power transfer [6.11].

Conversion efficiency is defined as a ratio of P_{MAX} to the input power from a (standard) 1000 W/m^2 AM1.5 light source [6.10]. The highest efficiency is obtained from GaAs solar cells, which can offer efficiencies as high as 42% [6.12]. The amorphous silicon (a-Si) thin film solar cell used in the solant design is 10% efficient (max.) [6.13]. Amorphous-silicon tends to have a lower efficiency compared to other solar cell materials, but it is cheaper to produce in large areas and quantities. However, due to the relatively high intrinsic source resistance R_{SH}, the efficiency of an a-Si solar cell degrades less in low light conditions (i.e., cell efficiency indoors relative to outdoors is around 90%) [6.14]. The efficiency-limiting factors for a solar cell are [6.15], [6.16]:

- Phonon generation (54%).
- Photons which carry energy not equal to the bandgap are not absorbed (18%).
- Part of the usable energy that can be converted is lost by reflection (2%).
- Not all light is absorbed due to the limited thickness (2%).
- Shading due to area used by electrodes (2%).
- Voltage drop due to series resistance R_{SE} of solar cell or due to leakage current characterized by R_{SH} (6%).

6.2.2. Battery

The electrochemical battery is the conventional energy source for portable electronic devices. While IC technology has advanced by miniaturization and doubling of the transistor density every one and one-half years, battery technology does not benefit for such miniaturization, and energy density is advancing at a much slower rate, doubling every 10 years [6.5]. Batteries can be classified as non-rechargeable and rechargeable, and also by their electrochemical material composition. Table 6.2 is a short list of some of the batteries available for portable applications at the time of writing. A lithium-ion (Li-ion) battery has an energy density of 200 Wh/kg. Assuming a 10 g Li-ion battery, a wireless transceiver that consumes 1 mW can operate for 3 months continuously. If 10% duty cycling is used for the transceiver power supply, the operational lifetime is (ideally) increased to 2.5 years. However, the battery itself has a limited lifetime of around 5 to 10 years

due to self-discharge caused by internal and external current leakages. Also, replacing a battery in the field may be impossible or may increase the maintenance cost for an autonomous wireless system, so long-term maintenance-free operation is preferred. Using harvested energy as an additional energy source to supplement or recharge the battery periodically can increase the lifetime and utility of an autonomous wireless system.

A fully-charged battery can be modeled as a voltage source in series with a non-linear internal resistance [6.17]. A typical discharge curve of a battery for a constant load current is shown in Figure 6.4. The battery provides almost a constant DC output voltage in the range 0.9-3.2 V, depending on the type [6.18]. When the stored energy is depleted, the output voltage collapses suddenly. The charge capacity of the battery is sensitive to temperature and the magnitude of the load

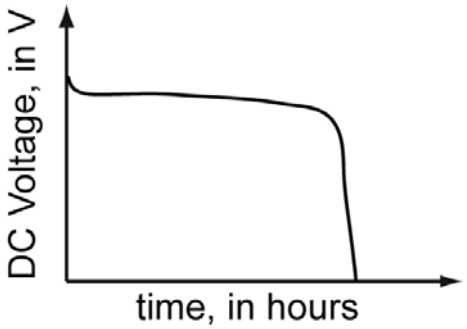

Figure 6.4. A typical discharge characteristic of a battery.

TABLE 6.2 COMPARISON OF BATTERIES SUITABLE FOR PORTABLE DEVICES [6.26]

Chemistry	Model	Voltage (V)	Capacity (mA-h)	Weight (g)	Volume (cm^3)	Energy Density ($mW\text{-}h/cm^3$)	Energy Density (mWh/g)
Alkaline	AAAA	1.5	625	20	1.20	781	47
NiMH	AAA	1.5	1000	13	3.85	389	115
	AA	1.5	2900	30	7.91	550	145
	C	1.5	6000	80	26.53	339	113
Li-ion	CR1225	3	50	2	0.28	531	75
	CR1632	3	120	5	0.64	560	72
	CR2032	3	225	2.9	1.00	672	233
	CR2450	3	610	6.9	2.08	880	265
	CR2477	3	1000	10	3.48	862	300
Silver Oxide	SR43	1.55	120	2	0.44	419	93
	SR44	1.55	175	2.5	0.57	476	109
	SR66	1.55	26	1	0.09	427	40
Li-ion Rechargeable	MS920S	3.1	11	0.47	0.15	229	73
	ML2032	3	65	3	1.00	194	65
NiMH Rechargeable	V600HR	1.2	600	14.5	4.29	168	50
	V20HR	1.2	20	1	0.21	116	24

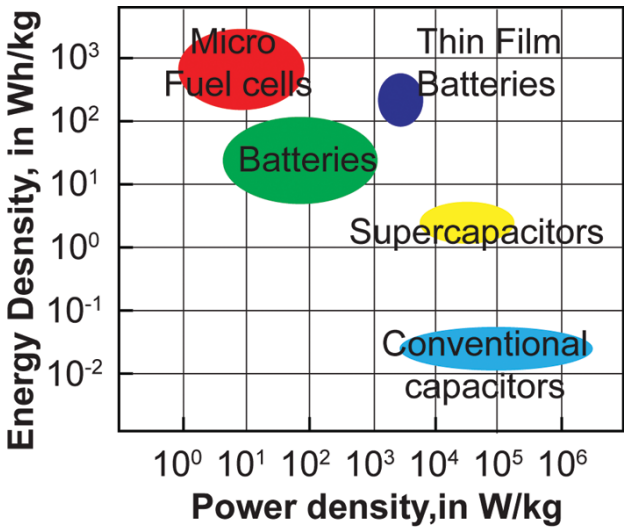

Figure 6.5. Energy density versus power density for various energy storage type [6.27].

current. At loads above its rating, over-discharge occurs, and the battery is depleted faster. The internal resistance increases and therefore parasitic energy losses increase [6.19]. There is a limit to how much current can be pulled from a battery which depends on the battery chemistry, volume, and construction.

The autonomous wireless transceiver is usually duty cycled, so the battery output current has a pulse like profile over time [6.20]. However, duty-cycling a radio can draw a transient over-discharge current from the battery, which has a detrimental effect on the battery lifetime. A capacitor connected in parallel with the battery supplies enough transient current to extend the lifetime by up to 170% under pulsed load conditions for load currents of just tens of mA [6.21]. It has also been shown that fast duty cycling (i.e., a few kHz) has 50% less battery capacity compared to duty-cycling at a frequency ten times slower [6.22].

A rechargeable battery can also be used to store harvested energy. Unfortunately, rechargeable batteries have a lower energy density and higher leakage current compared to non-rechargeable batteries [6.23]. The charging current must be controlled to avoid excessive heating or damage due to overcharging [6.24]. Limits on the number of recharge cycles (~200 [6.25]) and the need for an extra circuitry to manage the charging process add to the complexity of the overall energy supply system when rechargeable batteries are used. As opposed to a capacitor, it is more difficult to monitor the amount of energy that is stored in the battery, as the terminal voltage is almost the same whether the battery is full or empty (see Figure 6.4), and the maximum voltage decreases as the number of charge cycles increases [6.25].

6.2.3. Supercapacitor

A capacitor used for electrical energy storage is tolerant to the rate at which energy is transferred to and from it (power density is in the range of 10^3-10^6 W/kg). Power is defined as the rate of energy is transfer. High energy density elements can store more energy, while components with a high power density can fill or empty the

storage in a short time. Typically, high energy density storage cells have low power density and vice-versa (see Figure 6.5). The energy density of a ceramic or tantalum dielectric capacitor is much lower than a typical battery. Supercapacitors (a.k.a. ultracapacitors) have an energy density much higher (100 times) than a normal capacitor, as shown in Figure 6.5. The number of recharge cycles for a supercapacitor is on the order of 1 million, which is very favorable compared to a battery which may be recharged less than 10 thousand times.

Supercapacitors range from 0.01 – 10 F and have a packaging area of 1-4 cm^2. The leakage current of a supercapacitor ranges between 0.5-20 μA, and its effective series resistance (ESR) is typically less than 1 Ω [6.28]. It also has a maximum charge/discharge current rating on the order of few amperes [6.28]. Absolute maximum voltage ratings are approximately 2.5 V for a single supercapacitor, or 5 V for two capacitors connected in series [6.29].

The voltage across the supercapacitor, V_{SCAP}, depends on how much energy is stored, which can be expressed by

$$V_{CAP} = \sqrt{\frac{2E}{C_{SCAP}}}, \tag{6.1}$$

where E is the energy stored, and C_{SCAP} is the supercapacitor size. Knowing the amount of energy that is stored by sensing the terminal voltage can be advantageous for power management purposes. However, a wide input range DC-DC converter is required to supply the load with the stored energy as the terminal voltage of the capacitor will drop exponentially towards zero as it is discharged.

6.2.4. DC-DC converter

The output voltage from an energy harvester must be regulated and voltage conversions are required between the source and load (i.e., the solar cell terminals and the wireless transceiver). There are two classes of DC-DC conversion techniques used commonly in power management sub-systems. The first is the linear voltage regulator, and the other is the switching regulator.

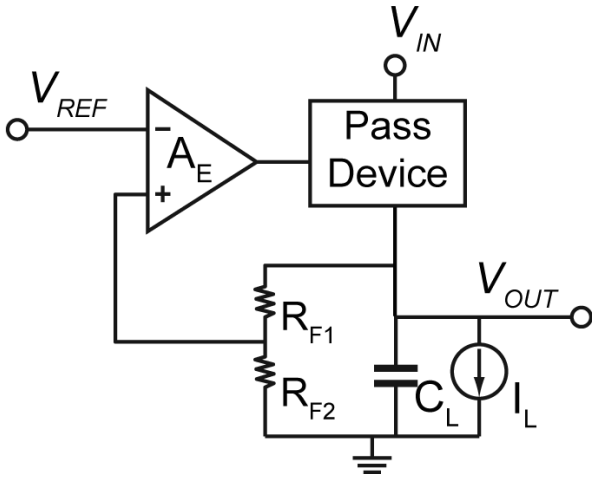

Figure 6.6. Schematic of a typical LDO.

A linear regulator, as shown in Figure 6.6, provides regulation using a pass device (e.g., a transistor). Output voltage, V_{OUT}, is sensed by a resistive divider, and fed back and compared with reference voltage, V_{REF}. The voltage difference is amplified by the error amplifier A_E that controls the pass device in a negative feedback loop. Feedback forces V_{OUT} to equal $(1+R_{F1}/R_{F2})V_{REF}$ in the steady-state. The pass device controls the amount of current flowing from V_{IN} to V_{OUT}, and can be implemented using either NMOS or PMOS devices in a CMOS technology. An efficient regulator consumes little quiescent current, so most of the current feeds the load through the pass device. The efficiency of the regulator can be estimated by the ratio of the output voltage divided by the input voltage, and there is a power dissipated by the pass device. A low voltage drop across the pass device is desirable, and low dropout (LDO) voltage regulators are designed to minimize this voltage drop. The voltage drop cannot be zero, because a certain working voltage is required to ensure that the CMOS pass device works in the saturation region. As V_{OUT} decreases, the voltage dropped across the pass device becomes a more significant part of the loss, and efficiency suffers.

The LDO has a low impedance at the regulated output; at low-frequency due to

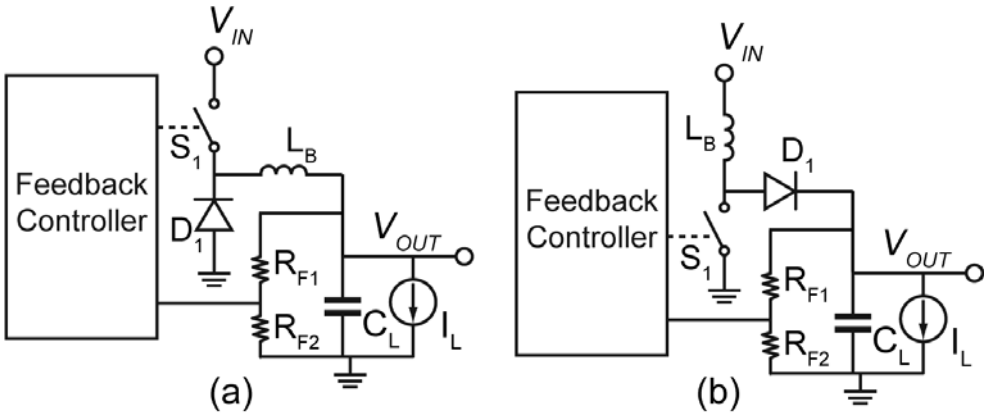

Figure 6.7. Schematic of (a) buck and (b) boost switched-inductor DC-DC converters [6.30].

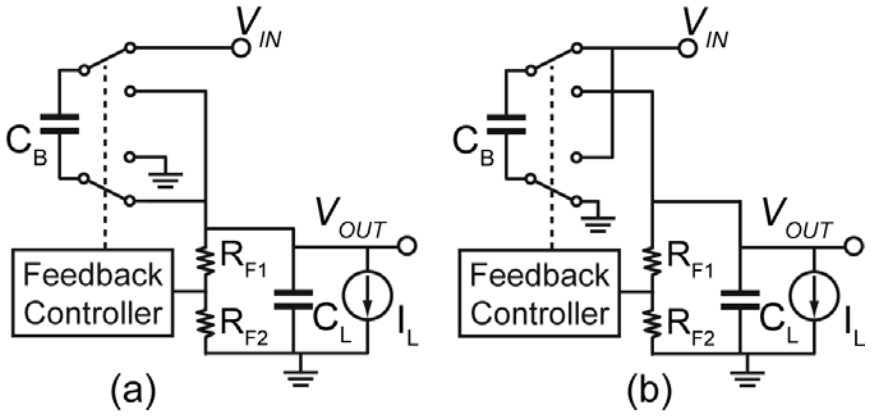

Figure 6.8. Schematic of (a) buck and (b) boost switched-capacitor DC-DC converters [6.31].

negative feedback, and at high-frequency due to shunt decoupling capacitor, C_L. Its simple implementation and compact size make the LDO a popular choice for a DC-DC converter. However, DC voltage step-up between input and output is not possible, because the output voltage must be always lower than the input voltage in proper operation.

Another type of a DC-DC converter is the switching regulator, which transfers a small amount of energy at a regular rate from the input source to the output. This is accomplished with the help of electrical switches and a controller to regulate the rate of the energy transfer. Switching regulators offers higher efficiency than linear regulators because energy is transferred to the load via either a capacitor or an inductor, which has low losses. Inefficiency results from parasitic losses in the switches and switch drivers. The switching regulator allows either a step-up (boost) or step-down (buck) of the DC voltage between its input and output. However, it has the disadvantage of generating unwanted periodic voltage variations called ripple at the output. The ripple voltage (if large enough in amplitude) can generate in-band interference in a radio transceiver, or reduces the resolution of an ADC.

The passive component values used in the switching regulator are inversely proportional to frequency, and proportional to the load current required. This may result in a large chip area in contrast with a linear LDO, which can be made more compactly. Fortunately, the 1 mA load current required from the on-chip DC-DC converter in this work can be implemented within a reasonable chip area (< 1 mm^2).

Switching regulators can be divided into two types depending on the passive device that transfers energy. The buck and boost (step-down and step-up) switched-inductor topology shown in Figure 6.7 charges the output voltage by inductive current. The switch controls the amount of inductive current by changing the duty cycle of the clock signal driving the switch. Diode D1 ensures that current cannot flow back from load towards source V_{IN}. In CMOS technology, the switches and diodes are usually implemented using MOSFETs [6.30]. A switched inductor topology is able to achieve a peak efficiency higher than 90% [6.30]. Step-up or step-down DC conversion requires different L-C network configurations, therefore this type of switching regulator is not easily reconfigured from step-up to step-down on the fly (see Figure 6.7). A low (<0.5 Ω) equivalent series resistance (ESR) inductor is required, which must be implemented off-chip [6.32]. Inductive (voltage) switching transients are a strong source of electromagnetic interference (EMI) that can disturb sensitive circuitry such as a wireless transceiver or a sensor.

Figure 6.8 shows a switched-capacitor DC-DC converter topology where electrical charge is transferred through capacitor C_B. A clock input controls the switch timing (i.e., open or closed). A feedback controller can be employed to control the clock duty cycle or frequency that drive the switches, and thus changes the energy transfer rate and regulates the output voltage. A switched-capacitor DC-DC converter does not require a bulky, external, low-ESR inductor, produces lower electromagnetic emissions, can operate in either step-up/down configuration on the fly, and generates less ripple as there is no inductive switching noise [6.33]. However, ripple is still generated because charge is injected into the output node to maintain the desired voltage at each clock cycle. The conversion factor or DC gain of the switched-capacitor DC converter is always a discrete number, because

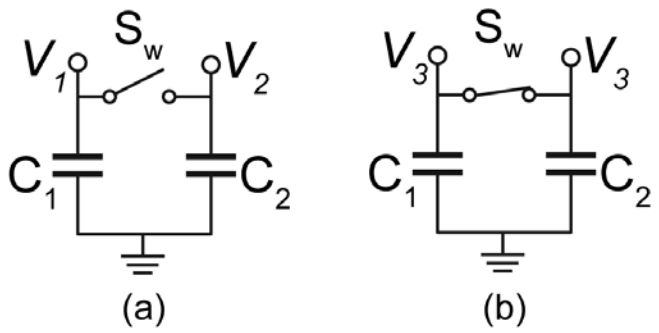

Figure 6.9. Illustration of charge transfer between two capacitors through a switch.

voltages across the capacitor are either added or subtracted in some quantized amount. The disadvantages of the switched-capacitor scheme are: it is less efficient (< 80%), requires more switches (i.e., higher circuit complexity), and efficiency depends upon the output voltage magnitude.

There is energy loss inherent in the charge transfer mechanism in a switched-capacitor circuit, which can be illustrated by examining the charge transfer process between two capacitors ($C_1$and C_2). Initially, C_1 is charged to voltage V_1 and C_2 is charged to V_2 (see Figure 6.9 (a)). The total energy stored in both capacitors is given by

$$E_a = \frac{1}{2}\left(C_1 V_1^2 + C_2 V_2^2\right). \tag{6.2}$$

When the switch is closed, charge is transferred from a higher to lower potential, creating a new equilibrium voltage, V_3 across both capacitors (see Figure 6.9 (b)). V_3 can be calculated as

$$V_3 = \frac{C_1 V_1 + C_2 V_2}{C_1 + C_2}, \tag{6.3}$$

and the total energy stored in both capacitors is now given by

$$E_b = E_a - \frac{1}{2}\frac{C_1 C_2}{C_1 + C_2}\left(V_1 - V_2\right)^2. \tag{6.4}$$

As long as there is charge transfer in a switched-capacitor circuit, there is energy loss. Energy is lost due to dissipation in the finite resistance of the switch that depends on the initial voltage difference V_1-V_2, where a bigger voltage difference results in higher loss. This loss limits the maximum efficiency that can be achieved by a switched-capacitor DC converter.

There are other sources of energy loss in a switched-capacitor DC converter [6.34]. There is overhead in the peripheral circuitry, such as biasing, clock generation, and buffering. The overhead should be small compared to the power delivered to the load. Another source of energy loss is parasitic capacitances associated with the switches, e.g., C_{GS} and C_{GD} in a MOSFET switch. The gates of the switches must be charged and discharged at the clock rate, and the energy required to do that contributes to the loss. Parasitic capacitance at the bottom plate

of the flying capacitor (e.g., C_B in Figure 6.8) is charged and discharged without contributing to charge transfer, therefore, it also contributes to the total losses. A high density capacitor with low parasitic capacitance between its top and bottom plates and the substrates is desirable for a switched-capacitor DC-DC converter.

The work in this thesis will focus on a switched-capacitor regulator design because a wide input range DC-DC converter is needed to convert the voltage across the supercapacitor to a supply voltage of 1 V. A stand-alone LDO is not suitable for a wide input voltage range as its output voltage is limited, and efficiency is (on average) less than that of a switching regulator. However, an LDO is needed to supply sensitive analog and RF circuits that cannot tolerate ripple on the DC supply voltage. On the other hand, the switched capacitor DC converter works across wide input voltage ranges and offers better average efficiency than the LDO, but generates ripple. A hybrid between the switched capacitor DC converter and LDO regulators is proposed to improve the overall efficiency with negligible ripple (below 0.1 mV) in the output voltage.

6.3. Power management circuit design

The proposed power management testchip shown in Figure 6.11 was designed to harvest solar energy, store it on supercapacitor C_{SCAP}, and provide the supply voltages required by the wireless transceiver. A 225 mAh Li ion (CR2032) battery at 3 V nominal voltage and feature size of 1 cm^3 is used as an auxiliary energy source that provides energy during the start-up of the power management unit, and when energy is needed urgently but not available from the solant. A 2 x 2 cm^2 amorphous silicon solant is employed to harvest the solar energy and act as an RF transducer [6.35]. The solant has a V_{OC} of 0.9 V and I_{SC} of 43 mA while radiated at the AM1.5 standard of 1000W/m^2 and temperature of 25 ºC [6.35]. The solant achieves P_{MAX} of 20 mW and efficiency of 6.3%. Indoors, and near a window, the

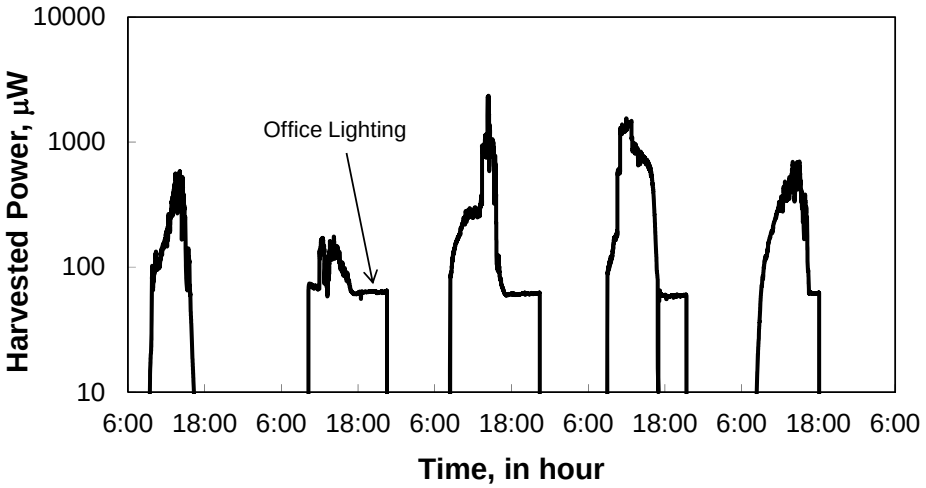

Figure 6.10. Power generated daily by the solar antenna (facing upward near a window that faces south-west direction) in an office at Delft, the Netherlands, during the first week of November, 2011.

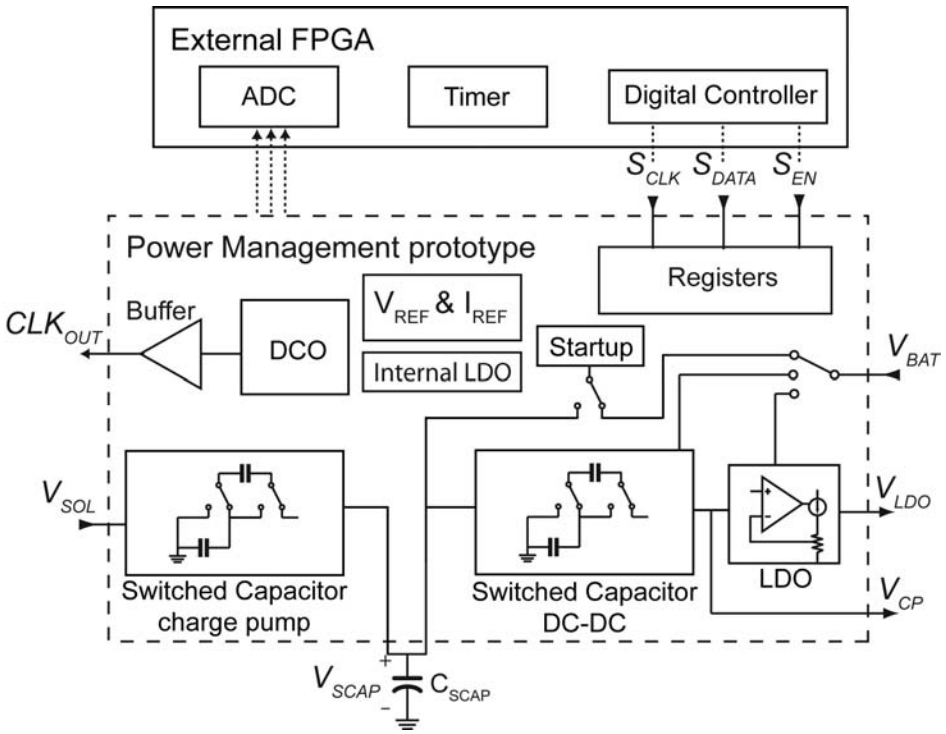

Figure 6.11. Block diagram of the power management test chip.

average generated power is 120 µW with an average V_{PMAX} of 0.42 V. Figure 6.10 shows power generated daily by the solant in a typical office during first week of November in Delft, the Netherlands. The solant is facing upward, near a window that faces the south-west direction. The energy generated daily varies by a factor of eight between cloudy and sunny days. The summer season on average generates twice the amount of energy compared to the winter season [6.36]. Note that the power generated due to office lighting (at 435 lux) is approximately 60 µW.

The switched-capacitor charge pump (SC-CP) (see Figure 6.11) transfers the charge generated by the solar cell to a supercapacitor. The supercapacitor size is chosen from an estimate of the energy that can be harvested from the solar antenna. Assuming indoor operation at an average generated power of 0.12 mW, the total energy generated daily by the solant is 10.4 Joule. From equation (6.1), it is estimated that a 2.7 F supercapacitor with a voltage rating of 2.75 V could store the maximum energy collected per day. If we consider that part of the energy is consumed by the load, power harvester, and other monitoring circuitry, then a fraction of the maximum capacitor size is adequate. The HS130F 2.4 F supercapacitor (Cap-XX) used in this work has a leakage current of less than 2 µA, and is 3.9 x 1.7 cm^2 in size [6.28]. The supercapacitor can be stacked with the solant, battery and the chip packaging, realizing a sensor node with an approximate volume of 7 cm^3.

The stored charge provides energy to a DC-to-DC converter that generates the required supply voltages. Three modes of DC-to-DC conversion can be selected.

The first uses a low-dropout regulator (LDO), the second uses a switched-capacitor DC-to-DC converter (SC-DC), and the third uses a hybrid of the LDO and SC-DC converter, with performance intermediate to the other two supplies.

A digitally-controlled oscillator generates non-overlapping clocks required for the SC-CP and the SC-DC converter. Voltage and current references are also implemented on-chip to generate temperature insensitive references, and for general biasing. Serial registers store the digital data used to control all of the various blocks. Internal LDOs supply circuitry internal to the power management IC that operates below the battery voltage (i.e., 0.6 V and 1 V). The battery supplies these blocks initially through a startup network. The supply is then come from V_{SCAP} when the supercapacitor is full. Most of the digital blocks that are switching periodically in normal operation are operated at 0.6 V to minimize their power consumption.

The complete implementation of a power management sub-system would employ a microcontroller, timer and ADC functions in addition to the basic energy management functions implemented in this prototype. In this work, an FPGA with on-chip ADC monitors the various input and output voltages, and controls the operation of the power management test chip (i.e., microcontroller function).

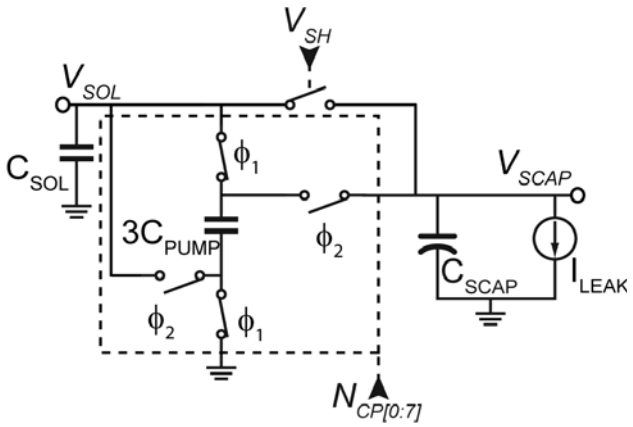

Figure 6.12. Switched capacitor charge pump (SC-CP) schematic.

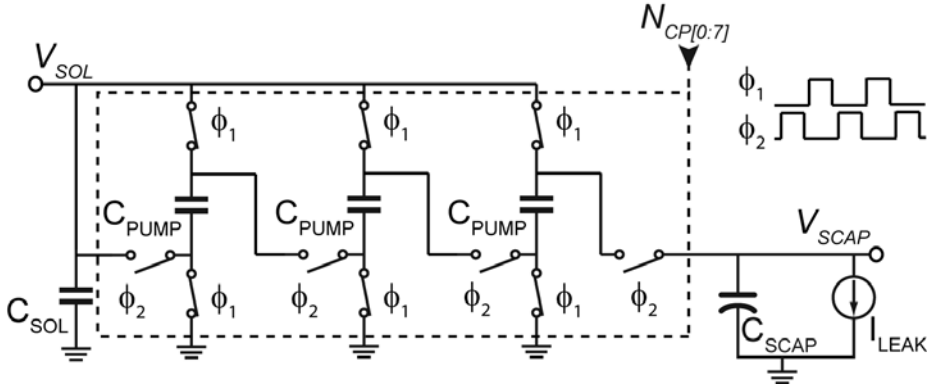

Figure 6.13. SC-CP with a DC gain configuration of four.

6.3.1. Switched-capacitor charge pump (SC-CP)

The charge generated by the solar cell at its output V_{SOL} (see Figure 6.3) is transferred to a supercapacitor via a switched-capacitor charge pump (SC-CP). Different charge pump topologies have been proposed, e.g., the Dickson charge pump [6.37] or the Cockcroft-Walton charge pump [6.38]. Here, the serial-parallel charge pump topology is adopted [6.39]. The charge pump operates in two phases and is driven by non-overlapping clocks. As shown in Figure 6.12, the solar cell charges capacitors $3C_{PUMP}$ during phase ϕ_1. During second phase ϕ_2, capacitors $3C_{PUMP}$ are rearranged in series with V_{SOL}, and transfer charge from $3C_{PUMP}$ to the supercapacitor C_{SCAP}. The charge pump shown in Figure 6.12 effectively multiplies DC voltage V_{SOL} by two to output V_{SCAP} in the steady-state condition. The charge pump can be configured with a multiplication/gain of one when the output voltage is less than V_{SOL} by directly connecting V_{SOL} to V_{SCAP} through the switch controlled by V_{SH}. A DC gain of four is realized by the configuration shown in Figure 6.13, where each of the three capacitors C_{PUMP} is connected in series with V_{SOL} during the second phase. If the expected maximum value of V_{SOL} is 0.75 V, a maximum output voltage V_{SCAP} of 2.75V can be realized theoretically (limited by the supercapacitor voltage rating [6.28]).

It is desirable for the charge pump to be able to vary the load on the solar cell so that the maximum available power can be obtained from the solar cell. The loading of the solar cell (R_{SOL}) by the switched capacitor circuit is given by

$$R_{SOL} = \frac{1}{3C_{PUMP} f_{clk}} \frac{1}{N_{CP}}, \tag{6.5}$$

where $3C_{PUMP}$ is the total pump capacitance used in the SC-CP (see Figure 6.12), and f_{CLK} is the clock rate of the charge pump. In the power management testchip, there are seven parallel charge pumps controlled by a 3-bit digital control word, N_{CP}. Together with varying clock rate, control word N_{CP} also varies loading for the

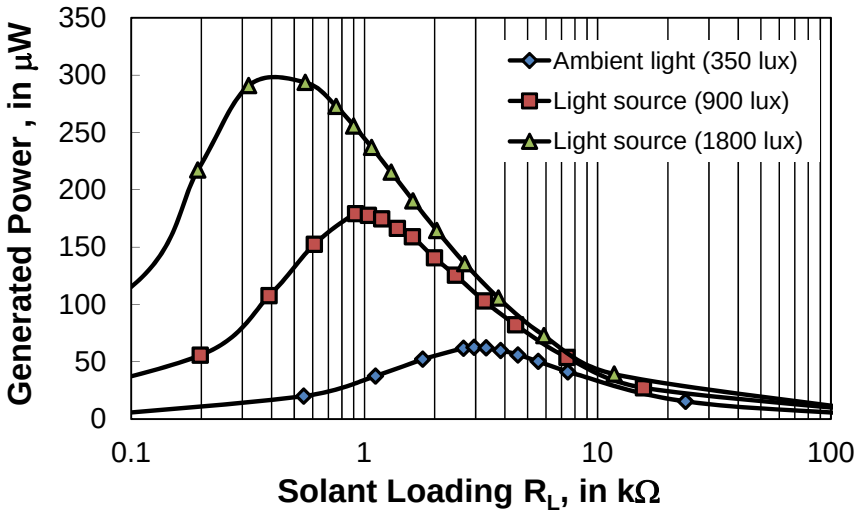

Figure 6.14. Measured generated power versus loading resistance on the solant.

solar cell (i.e., changing effective size of C_{PUMP}) to obtain optimum power transfer. The optimum load for the solar cell varies with the received illumination power and lies within the range between 0.1-10 kΩ (estimated from solant characterization). Figure 6.14 shows the measured power generated by the solant versus load impedance for varying light intensity. The optimum impedance that extracts maximum power is lower for a higher light intensity. The optimum (extrapolated) impedance for a light that comes from the sun at indoor (measured intensity of around 10,000 lux) is 0.1 kΩ. The power harvester circuit must be able to estimate the optimum impedance in order to extract the maximum power from the solar cell [6.40]. Based on the curve shown in Figure 6.14, the optimum voltage for maximum available power is around 0.4 V.

When the SC-CP is used in conjunction with a solar cell to harvest energy, the output voltage V_{SCAP} (i.e. voltage stored in the supercapacitor) will be in the range of 0-2.75 V. Due to its inherent loss, maximum efficiency is attained by a charge pump when the output voltages reaching the maximum value [6.41]. Therefore, the efficiency is low until V_{SCAP} achieve four times $V_{SOL,}$ if a DC gain of four is

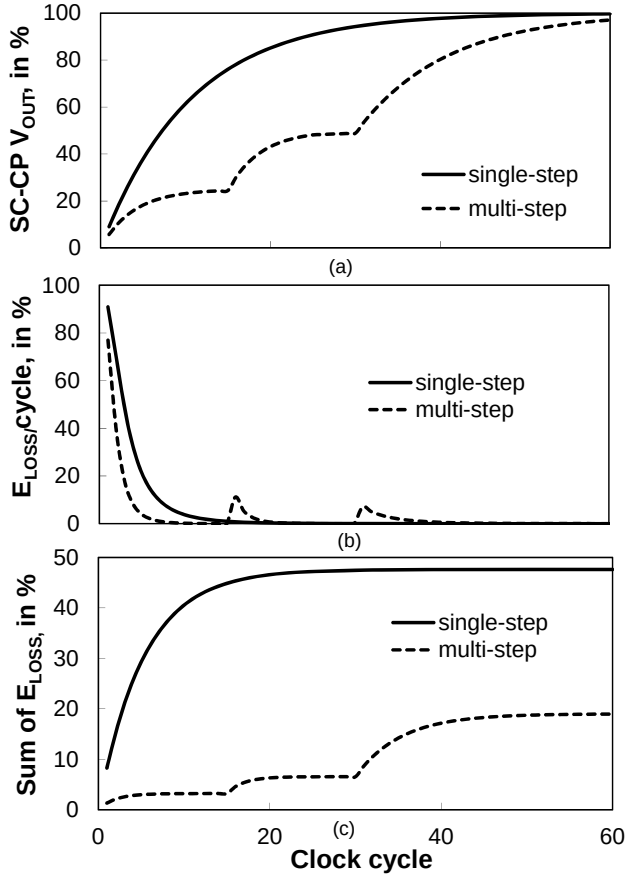

Figure 6.15. Illustration of energy transfer loss for a single-step and a multi-step charge pump circuit. (a) Output voltage, (b) Energy loss per cycle, and (c) Cumulative energy loss versus clock cycle.

employed. A multi-step mode using incremental gain ensures that the charge transfer process is as energy efficient as possible. In multi-step mode, the SC-CP uses the smallest gain initially, and then the gain is increased incrementally when the output reaches the maximum achievable voltage for each respective gain setting. Figure 6.15 compares the theoretical energy transfer efficiency of single-step and multi-step charge pumps, where the C_{SCAP} is 10 times C_{PUMP}. Only energy loss as defined by equation (6.4) is considered in this calculation. The output charges exponentially, eventually reaching a final voltage of $4V_{SOL}$ in this case. Gain steps of 1, 2 and 4 are used in the multi-step example. Charging in multiple steps is slightly slower than when a single step is used, as shown in Figure 6.15(a). The amount of time required to charge C_{SCAP} to its maximum voltage can be estimated by the 1/RC time constant

$$T_{CH} = \frac{1}{RC} = \frac{C_{SCAP}}{C_{PUMP} f_{clk}}. \tag{6.6}$$

The energy loss per clock cycle is highest initially and diminishes as the output charges (see Figure 6.15(b)). Figure 6.15(c) shows the cumulative energy loss as a percentage of the total energy stored in the output capacitor. While a single step charge pump loses 48% of the total transferred charge in the pumping process, energy loss is reduced to less than 20% by using three steps. A larger number of steps could reduce the inherent energy loss (asymptotically) to zero in theory. However, it is not practical to realize this in practice, because it will requires a large number of switches and capacitor configurations to generate the various gains. The circuit will become more complex and suffers from increased parasitics, which will then reduce overall power efficiency.

An ADC samples the charge pump output voltage and an algorithm determines the best configuration for the charge pump gain, f_{CLK} and N_{CP} (i.e., close to optimum within the limited number of configurations). The output voltage has to be monitored periodically, as the solar cell output varies due to changes in ambient lighting. If the charge pump is operated at the wrong gain, charge could travel backward, discharging the supercapacitor instead of charging it.

An external 1 nF capacitor (C_{SOL}) is connected in parallel with the solar cell to reduce voltage fluctuations caused by switching of the switched capacitor circuit. Each C_{PUMP} unit is implemented using a 18.6 pF MIM capacitor with 2% parasitic capacitance on its bottom plate. The nominal clock frequency (f_{CLK}) for the charge pump is 10 MHz. The power consumed by the charge pump is 15 µW and 105 µW for N_{CP} of 1 and 7, respectively.

6.3.2. Low Drop-Out (LDO) Regulator

The LDO design showed in Figure 6.16 supplies the load with 1 mA and 1 V under typical operating conditions. The output stage uses a zero-threshold NMOS source follower instead of a PMOS pass transistor as used in a conventional LDO [6.42]. A zero-threshold device allows low offset between the input and output, resulting in a dropout voltage of just 0.15 V. The source-follower configuration offers a good power supply rejection ratio (PSRR) at all frequencies as long the NMOS transistor is operating in the saturation regime [6.43]. The 3.6 pF MOS capacitor, M_{CAP},

stabilizes the loop, which has a phase margin of 75º for a capacitive load of 1 nF. The main regulating amplifier, A_1, uses a folded cascode topology and has a DC gain of 52 dB and gain bandwidth product of 10 kHz as shown in Figure 6.17. Feedback resistors R_{F1} and R_{F2} are implemented externally using 1 MΩ potentiometers.

The extra circuitry shown in the dashed box in Figure 6.16 compensates for any

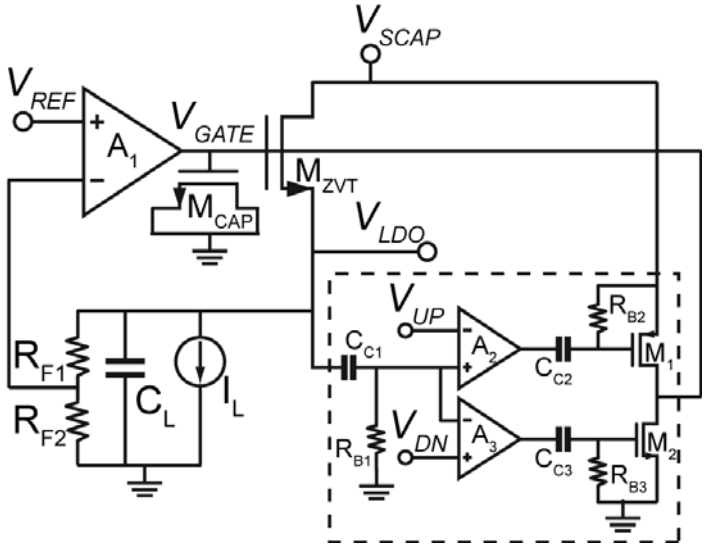

Figure 6.16. Schematic of the proposed LDO.

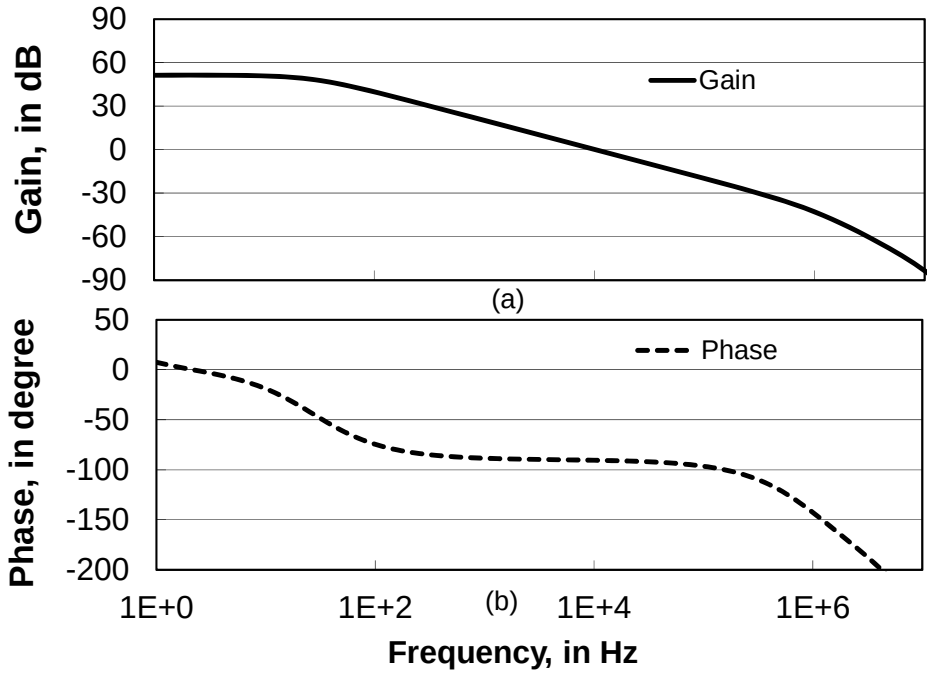

Figure 6.17. (a) Gain and (b) phase simulation plot of the LDO at C_L = 1 nF and I_L = 1 mA.

fast transients (e.g., spikes) in the output voltage caused by load switching. For example the load current in a duty-cycled radio has a pulse like profile which peaks during the active time. Because of the low frequency (dominant) pole seen at V_{GATE} in Figure 6.16, the loop takes a few tens of microseconds to respond when a large step in the load current occurs. Transient spikes are detected via an RC highpass network (C_{C1} and R_{B1}) and window comparators, A_2 and A_3. The pulse generated by this comparison pulls or pushes the voltage at node V_{GATE}, effectively speeding-up the loop response time. The amount of compensation is controlled by a 3-bit DAC (not shown) that tunes the speed of the comparators by varying its current bias. The LDO quiescent current (excluding current through R_{F1-2}) is 0.4 µA from a 3 V battery or V_{SCAP}. The usable voltage range of V_{SCAP} is 1.15- 2.75 V.

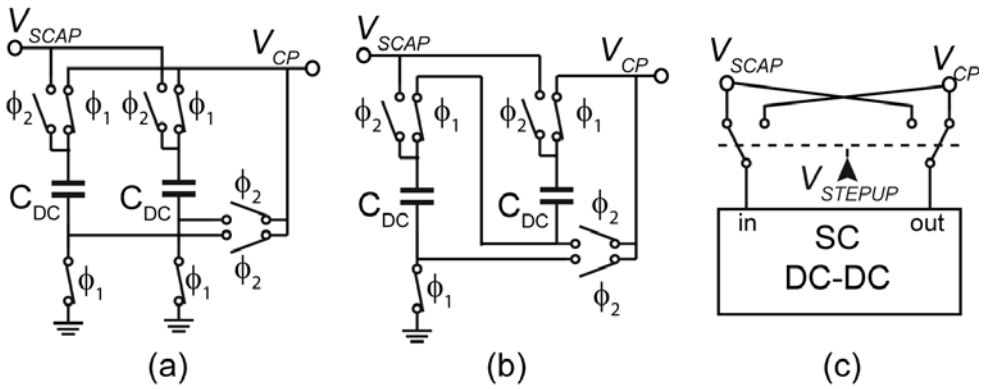

Figure 6.18. Switched-capacitor DC-DC converter schematic for a gain, (G) of: (a) 1/2, (b) 2/3, and (c) in the step-up configuration.

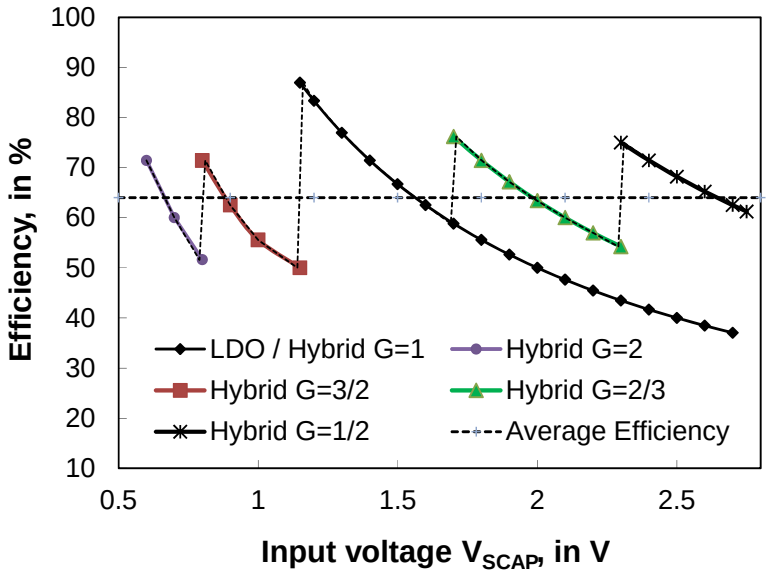

Figure 6.19. Efficiency of a hybrid DC-DC converter compared to an LDO as function of input voltage.

6.3.3. Switched-capacitor DC converter (SC-DC)

The switched-capacitor DC-DC converter prototype uses a series-parallel topology circuit [6.39]. The converter configuration shown in Figure 6.18(a) realizes a DC gain of one-half when operating as a step-down DC converter. In this case, the input is the voltage across supercapacitor, V_{SCAP}, and the output is its scaled voltage, V_{CP}. By switching capacitors C_{DC} between V_{CP} and ground in one phase, and between V_{SCAP} and V_{CP} during the other phase, V_{CP} is charged to one-half of V_{SCAP} in the steady state. This network can be reconfigured by changing the switch configuration to realize a gain of two-thirds, as shown in Figure 6.18(b). The step-up converter of Figure 6.18(c) can be obtained by exchanging the input and output ports of the networks shown in Figure 6.18(a) and Figure 6.18(b), which realizes a gain of two, and a gain of one and a half, respectively. The gain (G) of the DC converter can be changed easily by changing the switch configuration, showing the versatility of the switched-capacitor DC-DC converter circuit. Variable gain (G) is needed to accommodate a range of possible input voltages; in this case the voltage across the supercapacitor, V_{SCAP}, which can range from 0 to 2.5 V.

To maximize efficiency, there are several aspects of the design that can be optimized. Choosing a capacitor with low bottom or top plate parasitics (e.g., MIM-cap) is beneficial. Intrinsic losses can be minimized by ensuring that the voltage drop across C_{DC} is small during loading. This can be realized using a bigger capacitance value and/or a faster clock speed. However, a bigger capacitor requires larger switches in the converter, which actually increases losses in the switch drivers. Similarly, increasing the clock speed also increases losses in the driver circuit, due to charging and discharging of the parasitic capacitance in the switch and bottom plate capacitances. Extensive simulations were performed to balance intrinsic and switching losses. Depending on the magnitude of the parasitic capacitance, there is an optimum clock speed that results in maximum efficiency for a given capacitor size. The power consumption of the peripheral circuitry is minimized by using high-speed, low-voltage CMOS switches (to minimize transient currents) and a low voltage supply, and level shifting to a higher voltage only when necessary. From the simulation result, the intrinsic loss is estimated to be 10% and other losses are another 10%.

A wireless circuit requires a clean supply voltage free of ripple and harmonic energy that could corrupt the transmit/received data or jam the receiver. A hybrid DC-DC converter that combines an SC-DC converter and an LDO regulator is proposed for power management of the FM-UWB transceiver. Efficiency is maintained above 50% over a wide input voltage range for the hybrid DC-DC converter compared to an LDO alone (see Figure 6.19). The measured efficiency of the SC-DC is 79%, and the LDO efficiency is ratio of the 1 V output and V_{CP} (LDO quiescent current is negligible). The usable input voltage range is extended by using a step-up SC-DC converter configuration. The gain associated with each input voltage range is shown in Figure 6.19. The hybrid solution has an average efficiency of 64% for input voltages ranging from 0.55-2.75 V.

Figure 6.20 shows block diagram of the hybrid DC-DC converter designed in this work for the autonomous wireless system. There is no feedback mechanism that

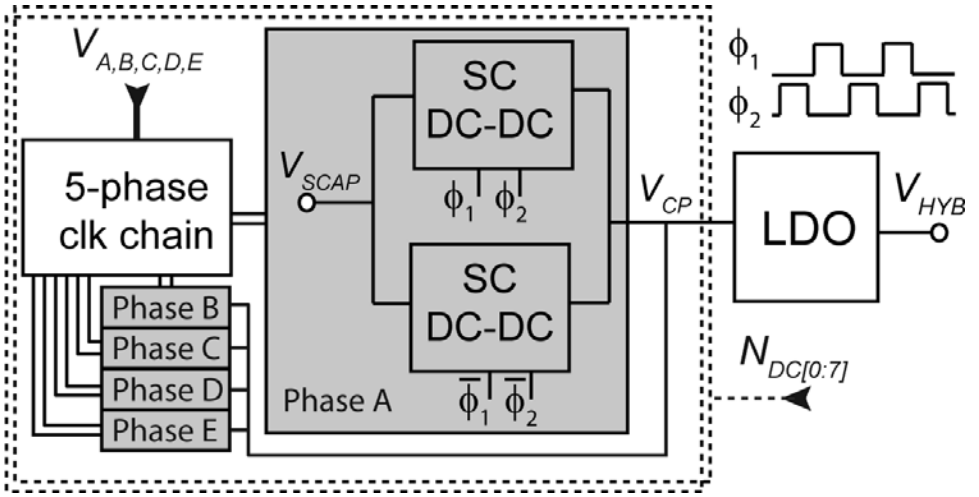

Figure 6.20. Hybrid switched-capacitor DC-DC converter block diagram.

regulates the SC-DC output, instead an LDO provides the voltage regulation. An ADC could be employed to monitor V_{SCAP} and V_{CP} when current loading is applied. A digital control algorithm could be deployed to set the gain of the SC-DC, the clock frequency, and the N_{DC} such that the converter operates with optimum performance.

Ripple is inherent in the SC-DC converter output, and can be as high as 30 mV_{p-p} [6.44]. While an LDO may offer up to 40 dB of ripple rejection, this is not sufficient for the wireless receiver. The ripple should be less than 10 μV (equivalent to -90 dBm in a 50 Ω system), which implies 70 dB ripple rejection for the receiver's supply. Ripple is generated when charge is injected into the supply line to maintain the desired supply voltage at each clock cycle. Splitting the charge pump into a differential circuit, where each half-circuit works in tandem during opposite phases, reduces the ripple voltage at the output by a factor of 2 while maintaining the same time to charge the load. To further reduce the ripple voltage generated by the SC-DC converter, a multiphase clock is employed as shown in Figure 6.20. The 5-phase clock implemented in this prototype drives the SC-DC in time interleaving fashion. The multiphase clock not only reduces the magnitude of the ripple, but it also pushes the ripple to a higher frequency where capacitance in the supply line can further filter the ripple. Reducing the ripple in the output voltage benefits efficiency as it also reduces ripple in the load current, and a multiphase factor of 10 is shown to be adequate [6.45].

The efficiency typically reaches its maximum value at the designed power rating, and it is poorer at lower output powers. In this prototype, a unit DC-DC converter is designed so that is optimized for a lower output power. The unit converter could also be configured to operate in parallel so that a wide range of load powers can also be delivered efficiently. Scaling can be controlled digitally by the 3-bit control signal N_{DC}, which is activated depending on the power demanded by the load similar to method used in digital power amplifiers [6.46]. Each C_{DC} unit is implemented using MIM capacitor with a total capacitance of 25 pF. The nominal

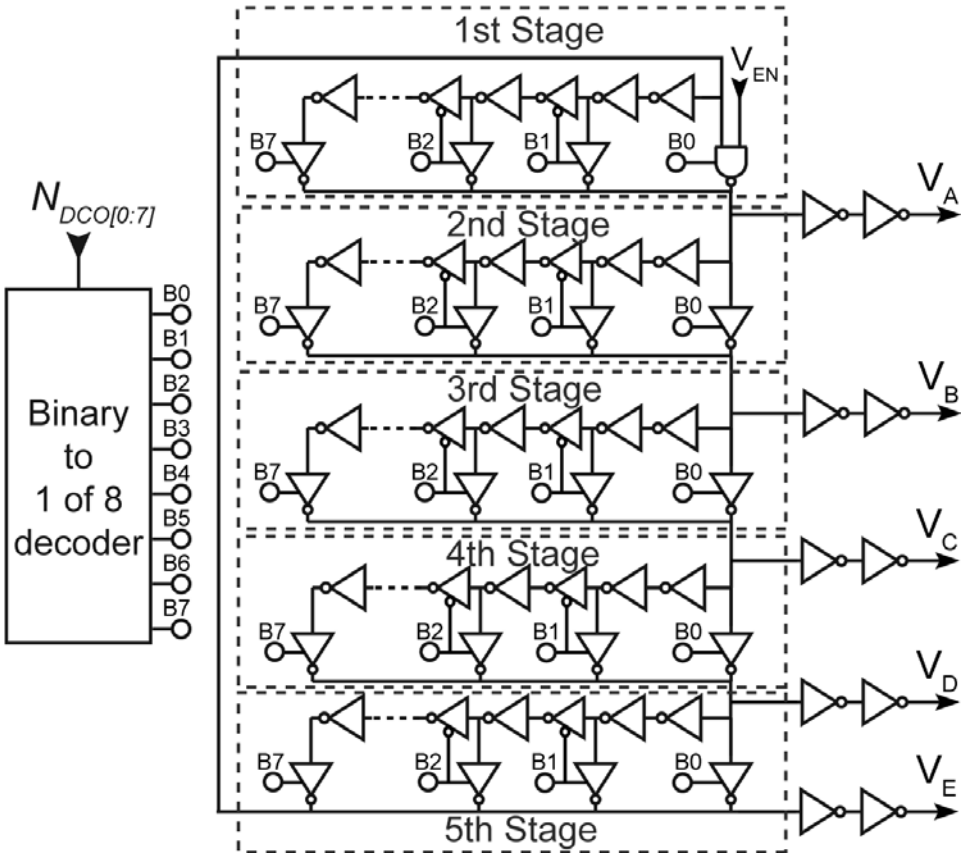

Figure 6.21. Schematic of the digitally-control oscillator (DCO).

clock frequency (f_{CLK}) for the charge pump is 10 MHz. The power consumed by the SC-DC per unit (N_{DC} = 1) is 21 μW.

6.3.4. Clock generator

The switched capacitor charge pump and DC-DC converter requires non-overlapping, two-phase clocks. The on-chip, 5-stage ring DCO that generates the 5-phase clock used by the SC-DC converter is shown in Figure 6.21. The ring oscillator starts-up when V_{EN} is high, and the buffered clock outputs are V_A, V_B, V_C, V_D and V_E. The DCO is supplied with a regulated voltage of 0.5-0.6 V, which controls the frequency of the clock. Additionally, a 3-bit control signal fed through a 3-to-8 decoder controls the delay by adding inverters to each stage of the ring oscillator under the control of tri-state inverters. The frequency range of the DCO is 1-40 MHz and it consumes 1.4 μW when running at the highest frequency.

The clock needs to be distributed to the switched-capacitor circuits. Figure 6.22 shows the clock tree from the DCO towards the switches. A multiplexer selects whether a 1-phase or 5-phase clock is used to drive the switch capacitor circuits. A non-overlapping two-phase clock is generated from each DCO output by a cross-coupled NAND (S-R) flip-flop, as shown in Figure 6.23(a). Buffers and the non-

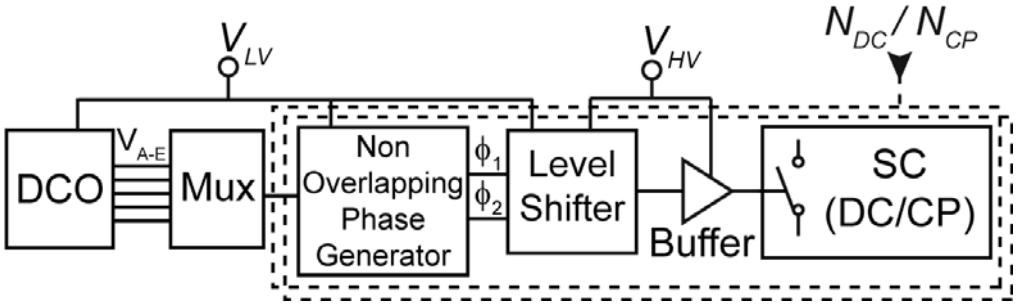

Figure 6.22. Clock distribution chain for the SC circuits.

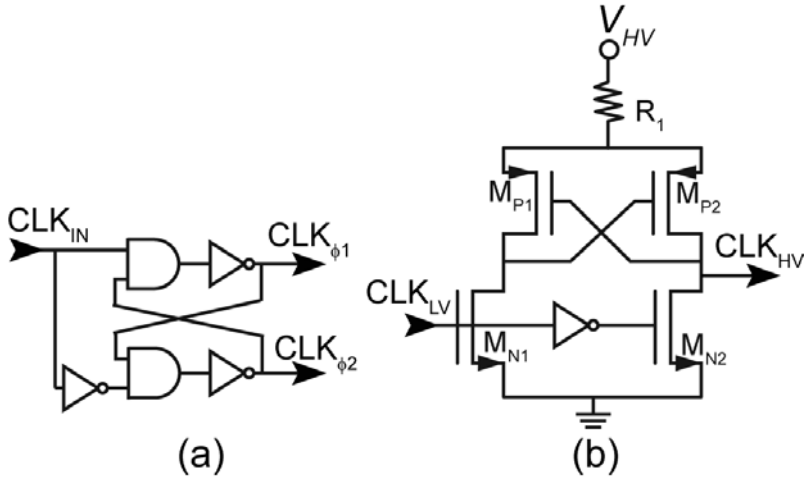

Figure 6.23. Schematic of (a) non-overlapping clock generator and (b) clock level shifter.

overlapping generators are supplied from 0.6 V (typically) to take advantage of the high-speed, low-threshold voltage transistors and minimize power consumption. The clock is shifted to a higher voltage (2.5-3 V) by the level shifter circuit shown in Figure 6.23(b). Resistor R_1 in Figure 6.23(b) speeds-up the switching process by bringing the common-mode voltage down dynamically during switching. Transistors M_{N1} and M_{N2} are low threshold devices to improve the circuit sensitivity to the 0.6 V input voltage. A clock buffer drives the switches of the switched-capacitor charge pump or DC-DC converter. The central clock generated by the DCO is distributed to each unit of the switched capacitor circuits, i.e., SC-DC and SC-CP. Each branch of the SC-CP and SC-DC circuits (there are 7 branches requiring a 3-bit control word) has its own clock chain and it is only turned on when needed to minimize the dynamic power consumption.

6.3.5. Bias Generator

Bias current and voltage references are also generated on-chip. A schematic of the bias generator is shown in Figure 6.24. Transistor M_{N1} and $4M_{N1}$ loop creates a PTAT current, while the loop containing transistor M_{N2} and $4M_{N2}$ creates a current that is proportional to the threshold voltage of transistor M_{LVTN}, and hence is an

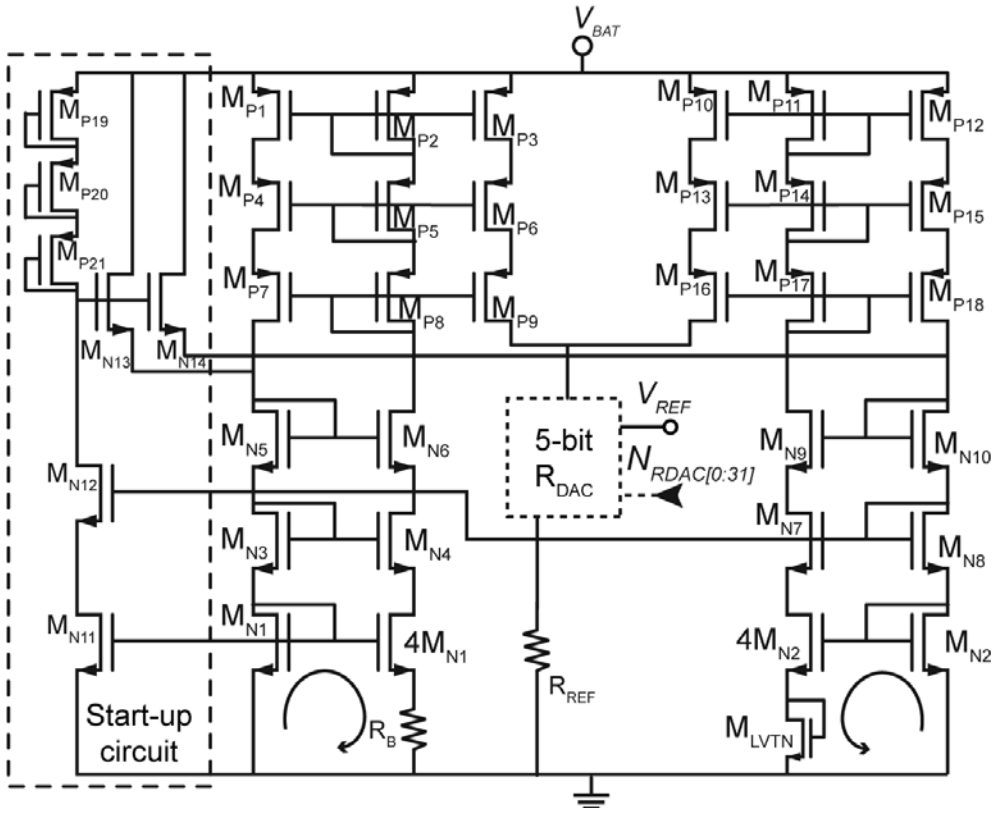

Figure 6.24. Schematic of the current bias and voltage reference generators.

inverse-PTAT current [6.47]. The sum of these currents produces a (first-order) temperature independent current source. Since there is plenty of supply headroom, a triple cascode configuration is used to obtain 60 dB PSRR across frequency range of DC to 100 kHz. A start-up circuit ensures that the loop operates at the desired operating point. A reference voltage for trimming purposes is created from the current source across R_{REF} using a 5-bit R_{DAC}. The reference voltage can be measured and calibrated to obtain a nominal value of 0.3 V. Each unit of the current bias is 50 nA, and it supplies the LDOs and current DACs. The bias generator consumes a total of 0.75 µA from a 3 V supply (battery, V_{BAT}).

6.4. Measurement Results

The power management testchip is implemented in a 90 nm bulk CMOS with the metal-insulator-metal (MIM) capacitor option [6.41]. MIM capacitors are used in the switched capacitor DC-DC converter as a means to transfer energy. MIM capacitor is preferred to the back-end metal-oxide-metal (MOM) capacitor in this technology because it has higher density (3.1 fF/µm^2 versus 1.9 fF/µm^2), a lower parasitic (2% versus 15%), and a higher breakdown voltage (5.5 V versus 3.6 V). The all-copper interconnect scheme consists of 5 thin, two medium-thick, and a

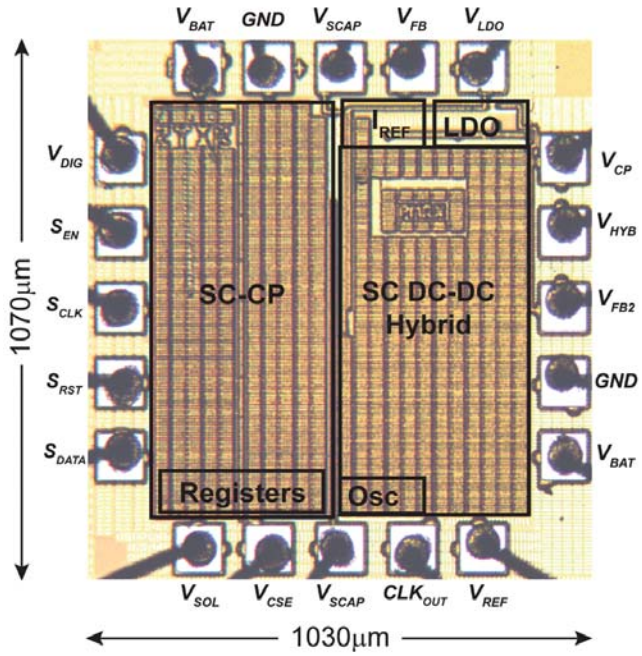

Figure 6.25. Chip photograph of the power management prototype.

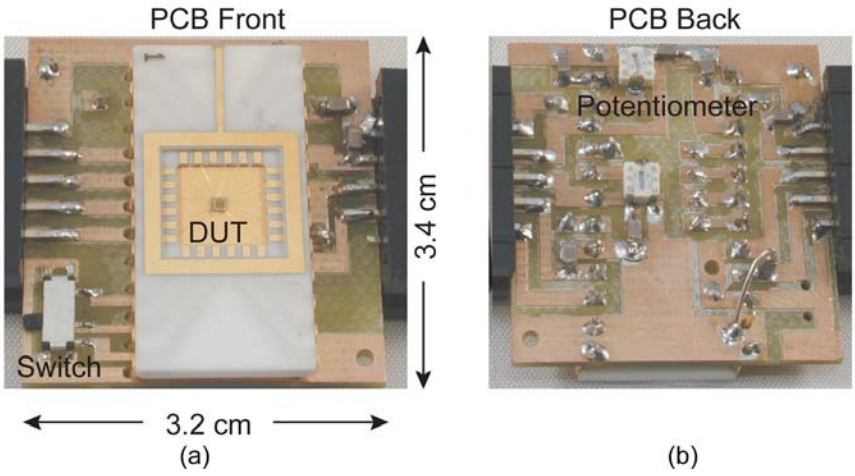

Figure 6.26. (a) Front and (b) back view of the PCB board for the power management characterization and testing.

thick top metal. Thick-oxide MOS devices with a breakdown voltage of 3.3V are used for circuits that operate at the nominal battery voltage.

The 1.1 mm^2 (including bondpads) die photo of the power management prototype is shown in Figure 6.25. Each pad is ESD protected using a standard library double-diode cell. The die is wirebonded in a 24-DIP and soldered onto a custom made PCB for testing, as shown in Figure 6.26. A potentiometer is employed as a feedback resistor to control the output voltage of the LDO. A switch

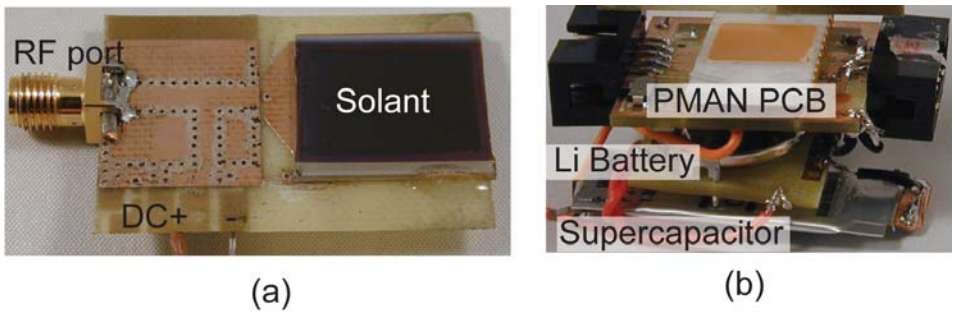

Figure 6.27. Photograph of the (a) solant PCB and (b) combination of power management (PMAN) board with the Li-ion battery and supercapacitor.

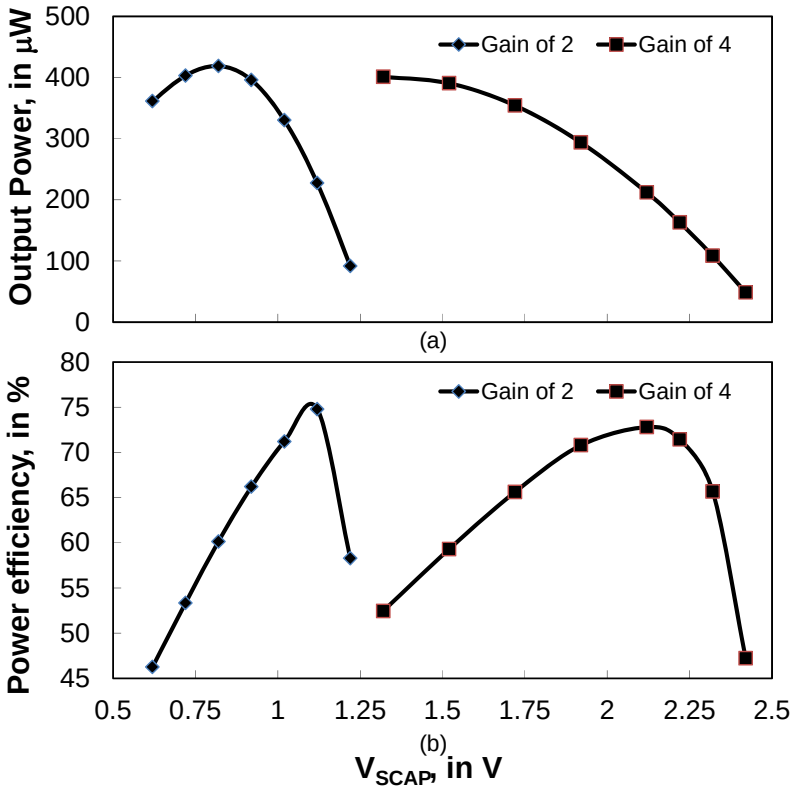

Figure 6.28. Measured power efficiency versus SC-CP output voltage, V_{CAP}.

is added to connect/disconnect the supercapacitor to the SC-DC. Figure 6.27(a) shows a PCB with an embedded solant that is used for various measurements and testing. More detailed characterization of the solant is reported in [6.35]. The power management PCB, Li-ion button cell battery, and the 2.8 F Cap-XX supercapacitor are stacked on top of each other as shown in Figure 6.27(b). A compact packaging that integrates these components will be made in the future.

6.4.1. SC-CP characterization

The measured output power and efficiency of the SC-CP are shown in Figure 6.28 at f_{CLK} of 10 MHz, and DC-gain setting of 2 and 4 for an input voltage of 0.625 V. Power efficiency gradually improves because the inherent loss in the switched-capacitor circuit diminishes when the output voltage is close to its maximum value. When it happens, there is less power delivered to the load. At the same time, the clock is still running and consuming power, hence, efficiency peaks just before it reaches its maximum voltage output. The power efficiency reaches a peak at output voltages (V_{SCAP}) of 1.1 V and 2.15 V at DC gains of two and four, respectively.

Figure 6.29 shows the measured input resistance of the SC-CP at the minimum and maximum number of parallel charge pumps (N_{CP} of 1 and 7) for clock frequency range of 6-18 MHz. The SC-CP has an input resistance range of 150-3,500 Ω, which fits the optimum resistance range for the solant at indoor condition (see Figure 6.14). Table 6.3 summarizes the performance of the SC-CP compared to

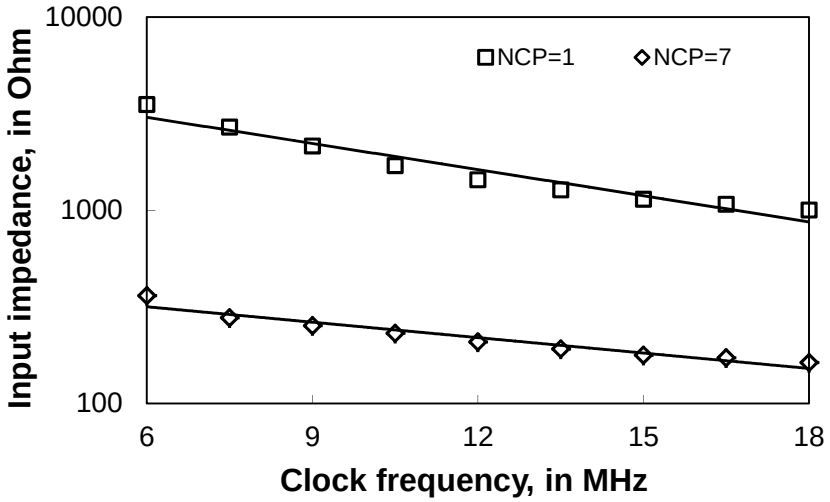

Figure 6.29. Measured input resistance of the SC-CP.

TABLE 6.3 PERFORMANCE SUMMARY OF SC-CP

Parameters	**This work**	**[6.48]**	**[6.49]**
Technology	90 nm CMOS	350 nm CMOS	350 nm CMOS
Input Voltage (V)	0.4-0.8	1-8	1-2.7
Output voltage (V)	0-2.75	1-8	2
Clock Frequency (MHz)	1-20	0.06	0.05
Max. Output Power (μW)	400	62.5	80
Peak efficiency (%)	75	58	86
Active area (mm^2)	0.32	3.06	2.28

other power harvester circuits. The SC-CP is customized for the solant, which provides a single diode voltage as an input. The output range fits the supercapacitor voltage rating. The SC-CP achieves a peak power efficiency of 75%, lower than the power harvester reported in [6.49], because the clock frequency is above 5 MHz. A higher clock frequency means more power dissipated in the clock generator, buffer and parasitics. On the other hand, the SC-CP has an advantage of a small chip area of 0.32 mm^2 and a higher output power of 0.4 mW. There is a trade-off between clock frequency and area for a given power capacity.

6.4.2. LDO characterization

Figure 6.30 shows the measured regulation of the LDO at an output voltage of 1 V

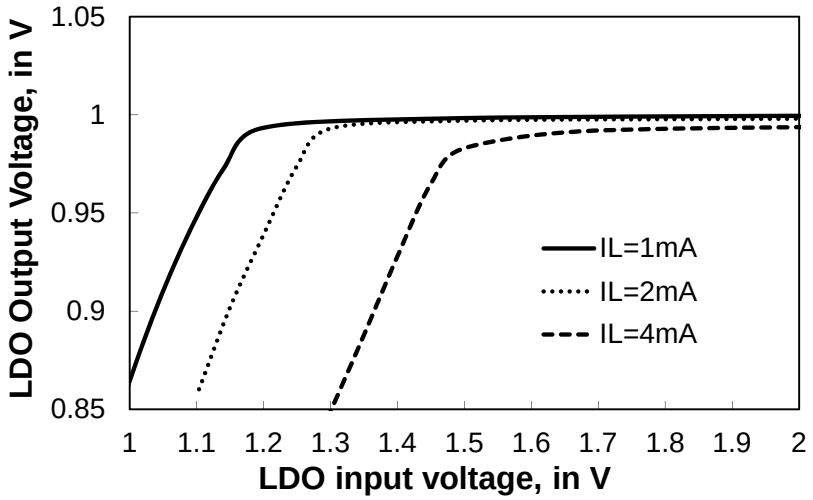

Figure 6.30. Measured line regulation characteristic of the LDO.

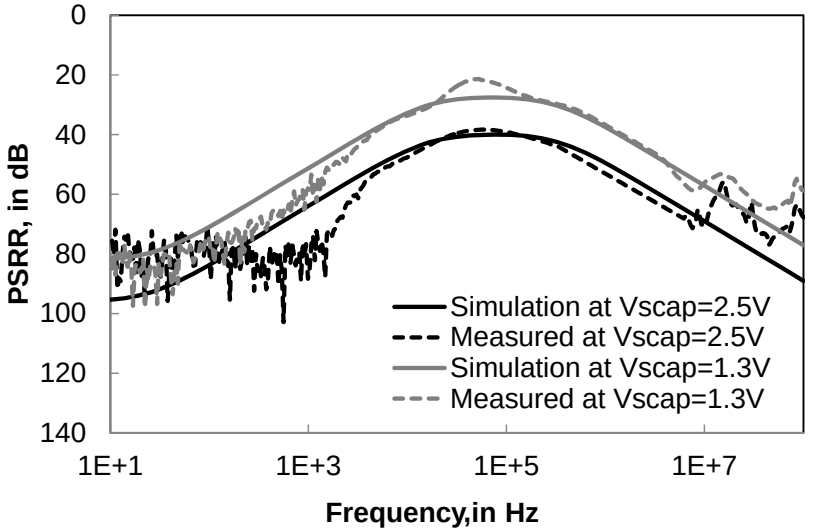

Figure 6.31. Measured power supply rejection ratio (PSRR) of the LDO.

for various load currents (I_L). The voltage regulation at 2.5 V is 1.25 mV/mA. At a higher load current, the regulation diminishes and the dropout voltage increases. The dropout voltage is 0.15, 0.25, and 0.45 V for I_L of 1, 2, and 4 mA, respectively. Figure 6.31 shows measurement and simulation of the power supply rejection of the LDO versus frequency. At lower supply voltages PSRR decreases because the NMOS pass device of the LDO operates closer to triode and hence the isolation from source-drain decreases. The poorest PSRR of 21 dB can be seen from the measured data at 50 kHz, and it is worse than simulation as it probably caused by the lower output impedance in the NMOS pass device.

Figure 6.32 shows the measured step response of the LDO output voltage for a

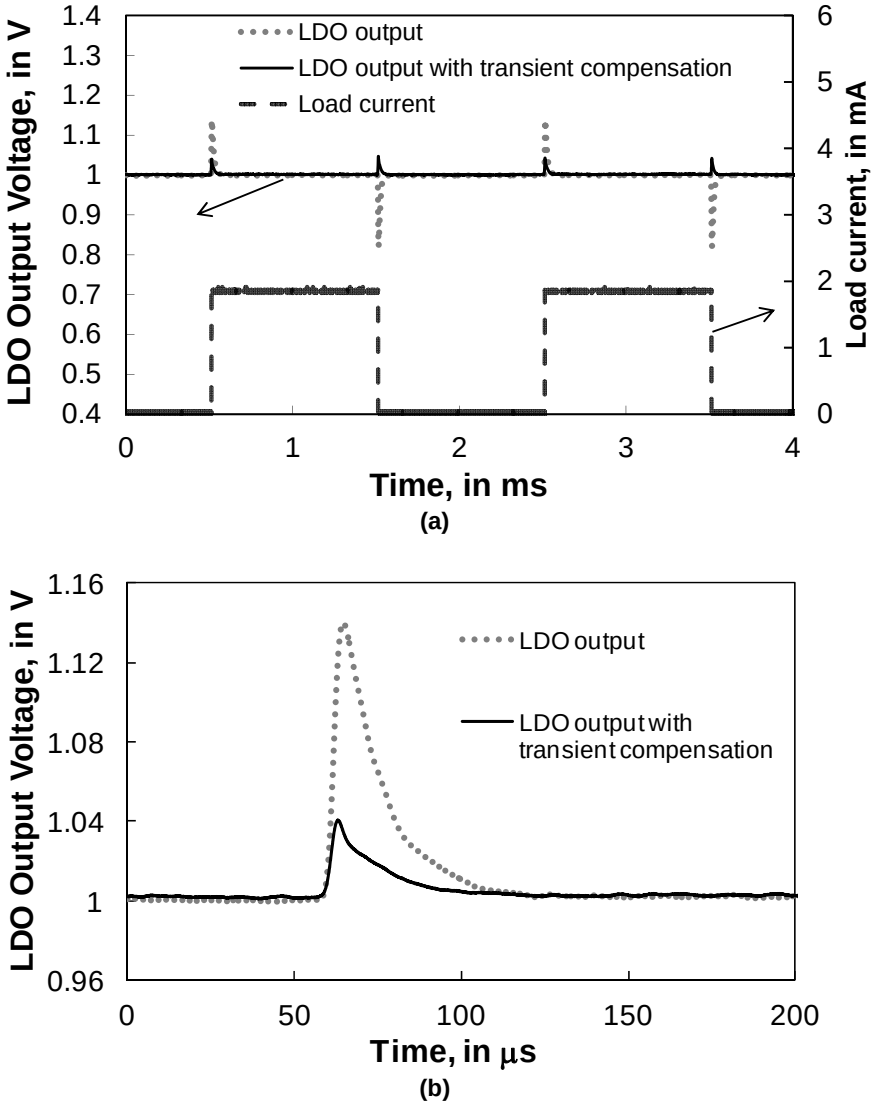

Figure 6.32. (a) Measured load transient response of the LDO, and (b) zoom-in on the voltage spike.

TABLE 6.4 PERFORMANCE SUMMARY OF THE LDO REGULATOR

Parameters	This work	[6.50]	[6.51]	[6.52]
Technology	90 nm CMOS	130 nm CMOS	350 nm CMOS	350 nm CMOS
Active Area (mm^2)	0.013	0.049	0.9	0.264
Dropout Voltage (V)	0.15	0.15	0.2	0.2
Maximum Load (mA)	1	25	120	200
Quiescent Current (µA)	0.4	50	0.12	20
PSRR, at 1MHz (dB)	55	67	-	-
Load Regulation (mV/mA)	1.25	0.048	0.006	0.17
ΔV_{OUT} in transient (mV)	40	26	150	54
Settling time (µs)	30	-	1900	-

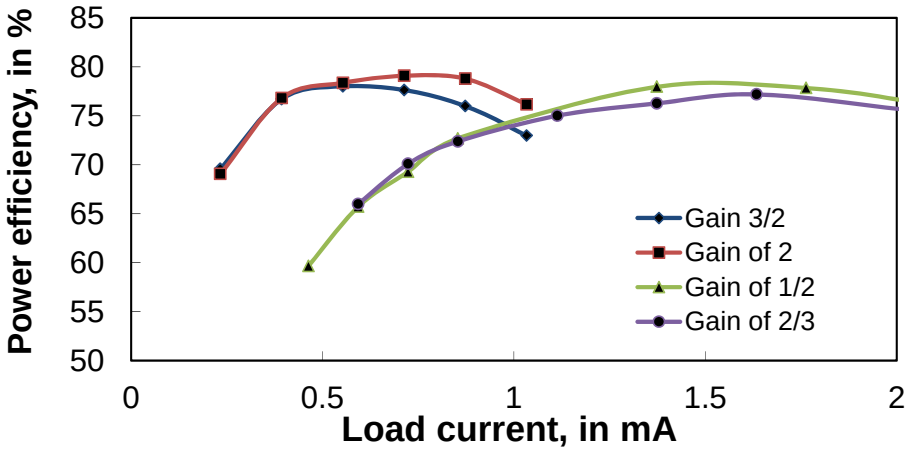

Figure 6.33. Measured power efficiency of the SC-DC for different gain settings at a clock frequency of 10 MHz.

pulse current load of 2 mA. There is a spike in the output voltage when the current load suddenly changes due to the slow response of the opamp. The output voltage variations due to the 2 mA current pulse are 0.14 V and -0.2 V at the rising and falling edges, respectively, while the settling time is 60 µs. The aforementioned fast transient compensation circuit helps to reduce the spike to only 0.04 V for both the rising and falling edges, and also improves the settling time to 30 µs.

Table 6.4 lists all the important parameters of the proposed LDO in comparison to other published results from the literature. The proposed LDO is tailored to a small current load of 1 mA from a 1 V supply, which is the estimated current consumption of the FM-UWB transceiver. The LDO has a PSRR of 55 dB at 1 MHz, and fast settling of 30 µs, while consumes the quiescent current of only 400 nA. The LDO described in [6.51] has a smaller quiescent current, but at the

cost of a much longer settling time**.** The LDO has a low dropout voltage of 0.15 V, and the smallest chip area. This LDO is suitable for a lightly loaded (< 1 mA) circuit block that uses duty cycling rather than continuous operation.

6.4.3. SC-DC characterization

Power efficiency of the SC-DC has been measured versus load current for different gain settings, number of units in parallel, and clock frequencies. Figure 6.33 shows the measured power efficiency at a maximum N_{DC} and various gain settings. For the same I_L, the step-up converter requires more input current than the step-down converter. Therefore, peak efficiency of the step-up setting in the SC-DC occurs at a smaller I_L for the same capacitor size compared to the step-down setting. The measured peak power efficiency is 78.3%, 79.1%, 78% and 77.2% at gain settings of 3/2, 2, 1/2, and 2/3, respectively.

Figure 6.34 shows power efficiency for different numbers of parallel SC-DC units as controlled by N_{DC}. The result shows that the peak efficiency can be controlled and maximized for the required current load. A power efficiency above

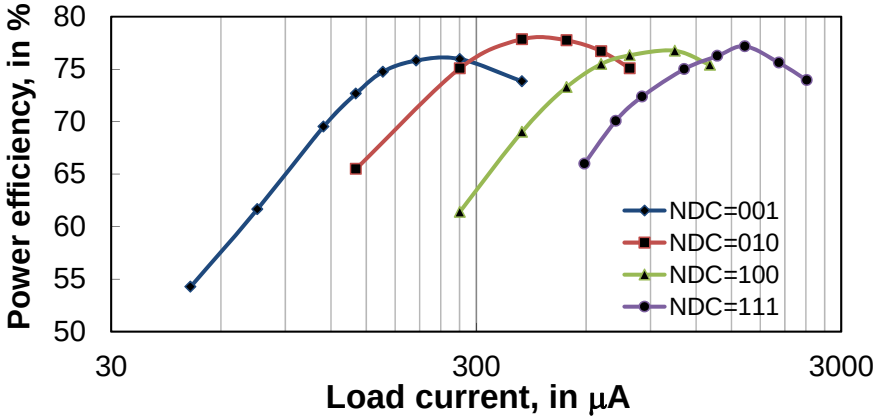

Figure 6.34. Measured power efficiency of the SC-DC at different number of parallel units that controlled by N_{DC} at gain setting of 2/3 at a clock frequency of 10 MHz.

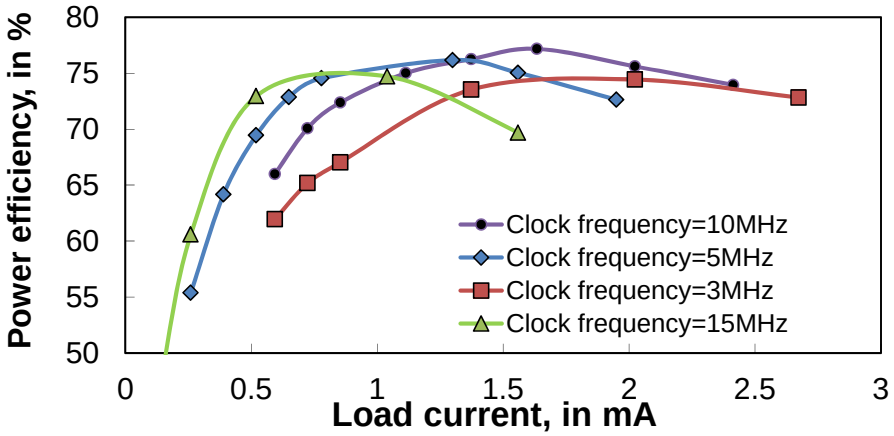

Figure 6.35. Measured power efficiency of the SC-DC for different clock frequencies.

75% can be maintained over a wide range of load current. The range across which efficiency peaks can be increased further by changing the clock frequency. Power efficiency at a gain setting of 2/3 and maximum N_{DC} for various clock frequencies is plotted in Figure 6.35. A clock slower than the nominal of 10 MHz shifts the peak efficiency to a smaller load current, and vice-versa. However, the highest peak efficiency was achieved at the nominal clock frequency.

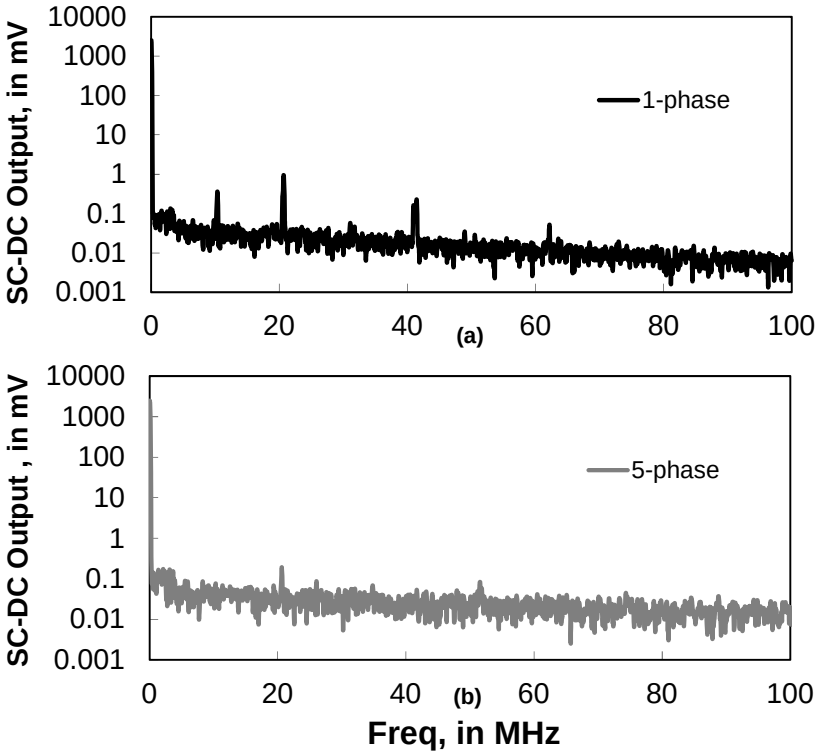

Figure 6.36. Measured spectrum on the SC-DC output voltage using (a) 1-phase and (b) 5-phase clocks at 10 MHz.

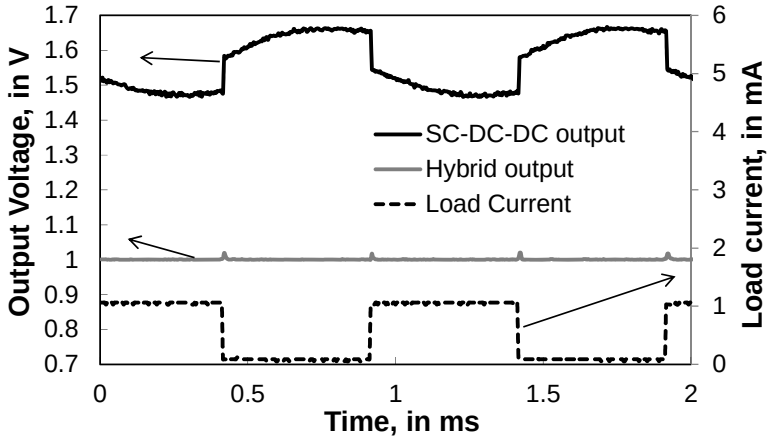

Figure 6.37. Measured step response of the hybrid DC-DC converter.

TABLE 6.5 PERFORMANCE SUMMARY OF THE SC-DC CONVERTER

Parameters	This work	[6.34]	[6.44]	[6.53]
Technology	90 nm CMOS	180 nm CMOS	130 nm CMOS	130 nm CMOS
Input Voltage	0.7-2.75	1.8	2.5-3.6	1.2
Output voltage (V)	1	0.3-1.1	0.44	0.7-2.1
Maximum Load (mW)	1	1	2.5×10^{-4}	4
Clock Frequency (MHz)	10	15	2×10^{-3}	30
Peak efficiency	79.1%	81%	56%	84.3%
Peak ripple (mV)	0.1	-	50	-
Active area (mm^2)	0.27	0.57	0.26	4
Power Density (mW/mm^2)	3.7	1.75	1×10^{-3}	1

As mentioned previously in Section 6.3.3, a multiple phase clock could reduce the ripple voltage generated by the SC-DC. Figure 6.36 shows the spectrum measured at the SC-DC output. The top figure shows the spectrum when using a 1-phase clock signal. A peak tone of around 1 mV appears at 20 MHz together with other harmonics and sub-harmonics. When the SC-DC uses the 5-phase clock, the main tone due to ripple at 20 MHz is reduced to around 0.1 mV. The LDO, with a PSRR better than 40 dB, will further suppress this ripple to below 1 μV.

Figure 6.37 shows the transient performance of the hybrid SC-DC/LDO for a load current pulse of 1 mA. There is no regulation in the SC-DC so the output voltage drops when the load current increases. However, the output voltage of the hybrid is regulated by the LDO, and generates 25 mV variations due to the 1 mA load current pulse.

Table 6.5 lists all the important parameters of the SC-DC converter in comparison with other published work. The SC-DC gets an input voltage from the charge stored on the supercapacitor in the range of 0.7-2.75 V. The output voltage for the FM-UWB transceiver load is 1 V. The SC-DC achieves 79.1% power efficiency, which is comparable to other SC DC-to-DC converters from the recent literature. Ripple voltage is suppressed using the on-chip 5–phase clock, generating only 0.1 mV, which is better than the other converters. The power density is 3.7 mW/mm^2, considerably better than other converters. The power density is usually limited by the technology (i.e., availability of high density, low parasitic capacitors).

6.4.4. Power management sub-system

The power management sub-system combines all the building blocks that were described previously. A real-time measurement with an actual load is currently not available, but will be done in the future. A calculated voltage level across the 2.8 F supercapacitor (V_{SCAP}) is shown in Figure 6.38, based on the measured solant energy

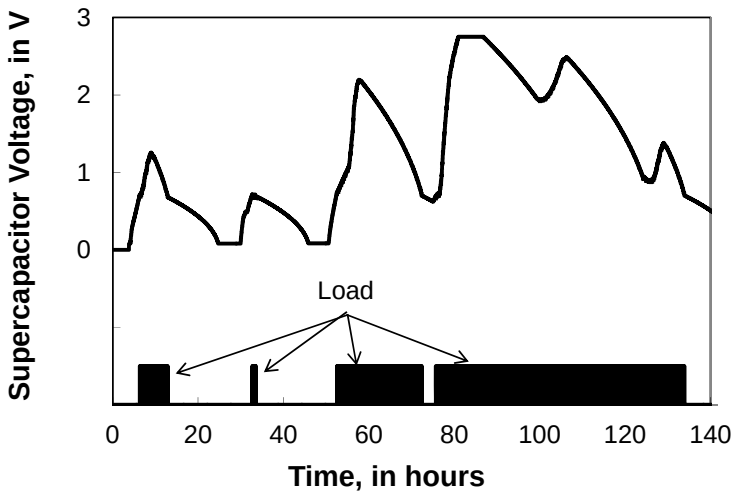

Figure 6.38. Calculated available voltage across the supercapacitor from indoor solar energy generated by the solant.

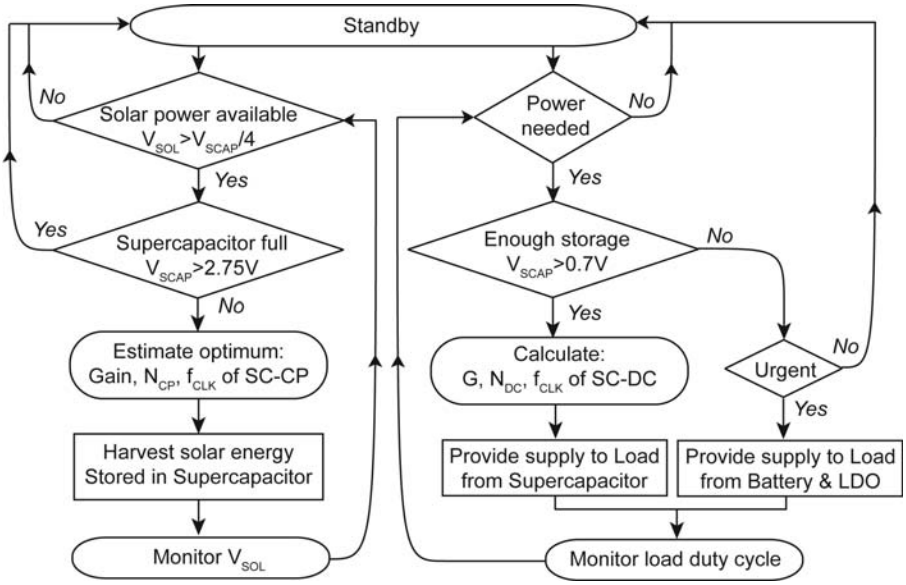

Figure 6.39.Flow chart of the power management controller.

that was collected indoor (see Figure 6.10). Leakage current at V_{SCAP} is estimated based on the standby current consumed in the power management and the measured leakage of the supercapacitor (~5 µA). The SC-CP is assumed to charge the supercapacitor at an efficiency of 75%. In this case the load current of 1 mA is applied when the V_{SCAP} above 0.7 V for a minute, every 10 minutes (duty cycle of 10%).

The simplified flow chart of the microcontroller for the power management is shown in Figure 6.39. The controller detects the available energy, stores it in the

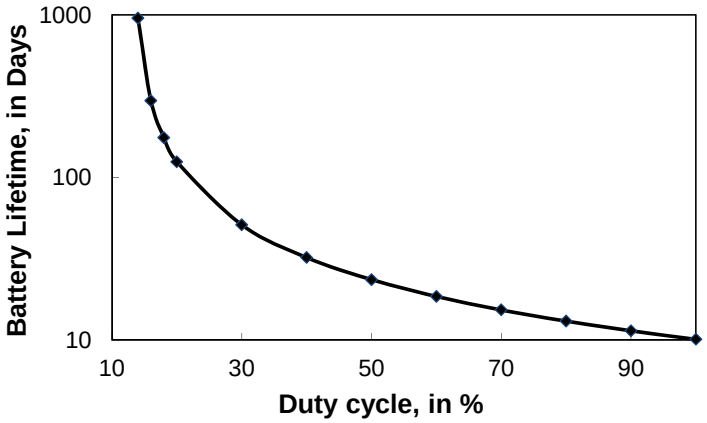

Figure 6.40. Estimated lifetime for a 225 mA-hour Li battery when using the collected solant energy and loaded with the FM-UWB transceiver (see Chapter 5).

supercapacitor and supplies the load when there is enough stored energy. As expected, there is not much energy stored during startup, and data throughput is intermittent. Later on, when the supercapacitor is almost full, transmission is more reliable.

Battery as a backup power source is therefore essential for any urgent or emergency transmission. The energy from the battery can be used during startup and in emergency situations. The lifetime of the battery depends on the leakage power (e.g., standby power in the power management, self-leakage of the battery) and how often the battery is used by the load. Figure 6.40 shows a 225 mA-hour battery lifetime versus duty cycle of the FM-UWB transceiver load described on Chapter 5. The average power collected from the solar cell is assumed to be 180 μW (averaging winter and summer condition), and the total leakage current is 10 μA. At 14% duty cycle, the battery lifetime is 3 years, while at 13% (i.e., when collected power equals consumed power) the lifetime is limited by the battery shelf life (~10 years). The solar energy that could be collected is on average 15.55 Joule per day, which is enough to supply a 10 nJ/bit wireless transceiver to transmit or receive raw data at 0.76 Gbit per day.

6.5. Conclusions

A power management prototype, suitable for autonomous wireless applications when powered from the button cell battery and a solar antenna, has been realized in a low-cost 90 nm bulk CMOS technology. The 1.1 mm^2 IC demonstrator consumes just 3.6 μA of stand-by current when supplied from a 3 V, 225 mA-hr button-cell battery allowing 7 years of standby time (theoretically). A 2.8 F Cap-XX supercapacitor is employed to store the energy generated by the solant. The switched-capacitor charge pump achieves 75% peak efficiency and provides loading resistance in the range of 0.15-4 kΩ. The hybrid DC-DC converter achieves an average efficiency of 64% from an input voltage range of 0.7-2.75 V, and an output ripple voltage less than 1 μV. The battery lifetime (estimated) when loaded by the

0.6 mW transceiver described in Chapter 5 is 10 days when operated continuously and 3 years when operates at 14% duty cycle.

A future version of the power management sub-system could include an integrated low power ADC and an embedded micro-controller. An algorithm that controls various building blocks in the sub-system will also be developed to optimize the power efficiency based on a real time environmental condition. The power efficiency could further be improved to 85% by using a slower clock speed at the cost of a larger die area [6.53]. The SC DC converter is programmable and scalable, The SC-CP and the SC-DC could be implemented as multiple cells of SC circuit and share the same capacitor arrays. A number of cells could be assigned for the CP and the DC-DC based on real time harvested power availability and load demand. By merging SC-CP and SC-DC, the total chip area could be minimized.

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CHAPTER 7. CONCLUSIONS

This thesis focused on developing an autonomous wireless system for various applications (e.g., WSN, WMBAN, and WPAN). These applications will benefit from autonomous wireless device that could operate independently without maintenance for years. For example, strain sensors that monitor a bridge conditions could be deployed and automatically alarms the engineer if any maintenance required. In hospital, patients that wear wireless heart monitoring device could move around more freely, while the doctor monitors their condition continuously. Many works on different expertise area needs to be done to realize these applications. The work on this thesis contributes to this endeavor by designing and implementing a low power FM-UWB transceiver along with a power management and harvesting sub-system.

A holistic approach is taken to a system design, where important sub-systems such as an FM-UWB transceiver and power management ICs are designed and implemented in CMOS technology. The FM-UWB modulation scheme uses unlicensed available UWB spectrum, and is chosen due to advantages of the schemes (e.g., a low-complexity transceiver architecture and robustness to multipath fading and narrowband interference [7.1]), which have been described in Chapter 2 and are verified by the work presented in this thesis.

A prototype FM-UWB transmitter that uses a ring oscillator as its carrier generator has been demonstrated in Chapter 3. Employing an optimized power amplifier, the full-transmitter (includes back-end circuitry) consumes only 0.9 mW (one-fourth compared to the previous state of the art [7.2]). Frequency calibration for IF an RF was implemented using on-chip SAR-FLL circuits. A prototype FM-UWB receiver that uses a positive feedback regenerative amplifier was demonstrated in Chapter 4. The narrowband and high-gain amplifier followed with the simple envelope detecting circuit consumes four times less power than FM-UWB front-end receiver in [7.3]. The receiver prototype is capable of achieving a sensitivity of -84 dBm, which is comparable to the previous design of [7.3]. The FM-UWB receiver shows 30 dB rejection against narrowband interference and agility against selective frequency fading multipath.

Improving upon the previous prototype, a 0.9 mm^2 fully integrated FM-UWB transceiver that achieves power efficiency of 5.8 nJ/bit (receiver) and 6.3 nJ/bit

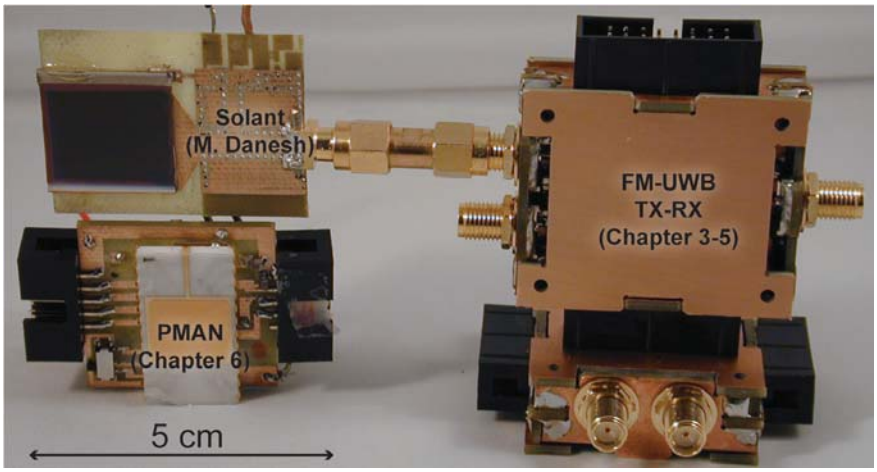

Figure 7.1. Photograph of prototypes developed in this project.

(transmitter) at data rate of 100 kbit/s (70% better than the thesis goal) was demonstrated in Chapter 5. The transmitter has a maximum output power of -10.1 dBm, and power efficiency of 13.3%, while the receiver has a sensitivity of -80.5 dBm and in-band SIR of -18 dB. The chip consumes 0.56 mm^2 active area using the 90 nm CMOS technology. The transceiver sets a new benchmark for the FM-UWB transceiver and competes well with other low power radios. The demonstrators shown in Chapters 3, 4, and 5 prove that FM-UWB transceivers are suitable for autonomous wireless systems.

A prototype of power management sub-system was demonstrated in Chapter 6. A solar antenna developed in our research group [7.4] and a button cell-battery is used as energy sources, and a 2.8 F ultra-capacitor is used as energy storage. The 1.1 mm^2 90 nm CMOS IC demonstrator consist of a switched-capacitor charge pump power harvester with 75% peak efficiency and a hybrid DC-DC converter with an average efficiency of 64% from an input voltage range of 0.7-2.75 V at an output ripple of less than 1 μV. It is estimated that the power management could supply the FM-UWB transceiver operating at 14% duty cycle for 3 years from energy harvested under typical indoor conditions.

The work described in this thesis is a part of a project to develop an autonomous wireless system. The milestones achieved are summarized in Figure 7.1, including the FM-UWB transceiver and power management prototypes that were described in this thesis along with the solant that was developed in [7.4]. The main contributions to knowledge from the work in this thesis are listed in Section 7.1. Clearly, the project is not finished but we have progressed in the right direction. Further works and collaborations must be continued to achieve the stated goal. Suggestions for future work are described in Section 7.2.

7.1. Thesis Contributions

The original contributions presented in this thesis are summarized as follow:

1. Analysis of the FM-UWB modulation scheme has been made, especially sub-carrier frequency, multipath effect, and PSK modulated sub-carrier. (Section 2.4).
2. Specifications for FM-UWB have been derived. (Section 2.5).
3. Development of a supply insensitive ring oscillator as wideband RF carrier generator (Section 3.2.1).
4. Development of an FLL-SAR calibration technique to calibrate the center frequency and bandwidth in the FM-UWB signal, that only costs minimal overhead in term of chip area and power consumption (Section 3.2.5).
5. Realization of a full-transmitter prototype for FM-UWB in 90 nm CMOS (Chapter 3) [7.5].
6. Development of a new receiver architecture that utilizes a regenerative amplifier with wideband tunability and envelope detector (Section 4.2).
7. Development of a CMOS regenerative RF amplifier using controlled positive feedback (Section 4.3.1).
8. Realization of a front-end receiver prototype for FM-UWB in 65 nm CMOS (Chapter 4) [7.6].
9. Development of a tripler-PA that improves energy efficiency of the FM-UWB transmitter (Section 5.3.2).
10. Development of a power efficient inductive-coupled RF regenerative amplifier (Section 5.3.4).
11. Development of a digital calibration scheme for controlling the positive-feedback in the regenerative receiver (Section 5.3.7).
12. Realization of a 0.9 mm^2 FM-UWB full transceiver in 90 nm CMOS with an all-digital interface. The transceiver achieves 6 nJ/bit energy efficiency at a data rate of 100 kbit/s (Chapter 5).
13. Development and analysis of a switched-capacitor charge pump and DC-DC converter for energy transfer between a solar cell, an ultra-capacitor, and the load, i.e., FM-UWB transceiver (Section 6.3.1 and 6.3.3).
14. Analysis of the energy that can be harvested from a 2x2 cm^2 solar cell under indoor conditions (Section 6.3).
15. Realizations of a power management chip in 90 nm CMOS that utilizes a solar antenna and small battery as energy sources, and an ultra-capacitor for energy storage (Chapter 6).

7.2. Suggestions for Future Research

An integrated autonomous wireless system where sensors, transceiver, power management, memory, and a processor are integrated onto low-cost CMOS will be a logical next development goal for this project. Not only the IC domain, but also packaging is an important factor. Low cost, small form factor and robustness are important factors for the packaging design. The system includes off-chip components, such as antenna, battery, ultra-capacitor, and a power harvester. Maximum on-chip and system in package (SiP) integration would offer a compact autonomous system that can be deployed in many applications.

In term of modulation schemes, more research should be conducted into the FM-UWB schemes. PSK modulation using a sawtooth wave as the sub-carrier offers an interesting possibility to increase the data rate or sensitivity with modest modifications (See Figure 2.8). A receiver that demodulates PSK-modulated FM-UWB could be developed in the future. The possibility of using fast duty cycling and data coding for the FM-UWB transceiver has been proposed in [7.7]. Further development that combines the concept from [7.7] with the circuit design described in this thesis should result in higher power efficiency.

FM-UWB transceiver operating at frequency band of 7-9 GHz needs to be developed as well. Power consumption are expected to scaled with operating frequency, but further innovation and smaller feature CMOS should keep the power consumption low. The data rate of the FM-UWB will be increased to 250 kbit/s, conforming to the IEEE 802.15.6 standard [7.7]. Multi-user baseband processing will also need to be developed for the next FM-UWB receiver prototype.

A power sensing circuit should also be developed for the FM-UWB hardware. This will be useful to adjust the output power automatically such that it conforms to government regulation. The circuit could also be used for a cognitive radio to detect whether the frequency band is occupied or not. Finally, power sensing can be used to adjust the transmitted power. For example in the case when the receiver has more than enough SNR, the receiver could request to the transmitter to reduce the output power while maintaining an acceptable BER. BER could be detected in the background using an embedded error detecting code in the data stream. The overall network would operate at higher power efficiency by adaptively changing the transmitted power depending on channel conditions. The power detection should be accurate (requiring some calibration) such that it does not degrade the performance of the transceiver.

In power management, further improvements could be made such as, higher efficiency for the DC-DC converter, lower leakage current during standby, and higher integration that includes an ADC and a microcontroller. A goal would be to develop a power management circuit that provides energy for the wireless system indefinitely.

Low cost and popular applications drive the IC market. Further research is required to identify potential applications for autonomous wireless systems. Using the available prototype and human creativity, applications unknown at present may

actually be the main industry in the future. This would encourage more funding for research and development to develop these devices.

7.3. References

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SUMMARY

This thesis discusses the design and implementation of a transmitter and a receiver for an FM-UWB scheme in CMOS. The main challenge is to reach a power efficiency of better than 10 nJ/bit at a data rate of 100 kbit/s for both the transmitter and the receiver design. This thesis also discusses the design and implementation of a power management unit for an autonomous wireless system. The challenge in this design is to obtain a high efficiency DC-DC conversion using the switched capacitor topology and low voltage ripple at the output voltage.

In chapter 2, several modulation schemes and ultra-wideband technology are briefly described as the background knowledge for this thesis. The advantages of FM-UWB schemes, that use double modulation to realize uniform output spectrum and steep spectral roll-off, are highlighted. Specifications for an FM-UWB transceiver were derived and listed in Table 2.1 of this chapter, along with the conventional implementation of the FM-UWB transceivers. Design methodologies that benefit for low power CMOS design in this thesis are described.

In chapter 3, a fully-integrated 3-5 GHz-band FM-UWB transmitter implemented in 90 nm bulk CMOS is presented. The front-end consists of an RF current-controlled oscillator (RF-ICO) and a class-AB power amplifier. Transmit data modulate a sub-carrier oscillator. The 2-FSK modulated output is amplified by a transconductor, and directly modulates the RF-ICO tune input. A successive approximation register (SAR) algorithm and on-chip all-digital frequency-locked loop (FLL) calibrate the carrier and sub-carrier frequencies. All voltage and current references required by the transmitter are included on-chip. The 0.2×0.5 mm^2 active area transmitter consumes 900 μW from a 1V supply. Energy efficiency of the transmitter is 9 nJ/bit running continuously at 100 kbit/s.

In chapter 4, a regenerative, FM ultra-wideband (FM-UWB) receiver for a low data rate (< 100 kbit/s) and short distance (< 10 m) reception in the 4-5 GHz band, consisting of a 35 dB gain preamplifier, envelope detector/demodulator, IF amplifier and 50 Ω test buffer is described. The tunable (3.8-5.1 GHz) receiver front-end operates on a 50 MHz sub-band that is selected, amplified and transformed from FM to AM by a regenerative preamplifier. Energy efficiency of the regenerative FM-UWB receiver compared to the previously published FM-UWB implementations is improved by a factor of 8, to 22 nJ/bit. Measured receiver sensitivity is -84 dBm at 100 kbit/s data rate (10^{-3} BER). Implemented in 65 nm bulk CMOS, the 0.3 mm2 test chip consumes 2.2 mW (excluding test buffer) from a 1 V supply.

In chapter 5, a fully-integrated FM-UWB transceiver for the 3-5 GHz band which benchmarks the scheme for low-power and short-range (< 10 m) applications was realized in a 90 nm bulk CMOS technology. The transmitter uses RF current-controlled oscillator (RF-ICO) that operates at one-third of the carrier frequency, and followed by a tripler-PA that multiplies the frequency by three and amplifies the power of the FM-UWB signal, delivering it to a 50 Ohm load. The maximum output power is -10.1 dBm, resulting in a transmitter power efficiency of 13.3%. The receiver uses a 40 dB regenerative RF-amplifier followed by an envelope

detector, IF limiter and FSK demodulator. The measured receiver sensitivity is -80.5 dBm at 100 kbit/s data rate (10^{-3} BER). On-chip digital calibration was implemented to tune the RF-ICO and the regenerative RF amplifier. The chip is controlled digitally through a serial interface, and all voltage/current references required by the transceiver are included on-chip. The 0.9 mm^2 transceiver IC demonstrator consumes just 630 μW and 580 μW from a 1 V supply when it operates at the transmitter and receiver mode, respectively. The nominal energy consumption of the transceiver is 6 nJ/bit at a data rate of 100 kbit/s in continuous operation.

In chapter 6, a power management prototype, suitable for autonomous wireless applications when powered from the button cell battery and a solar antenna, was realized in a low-cost 90 nm bulk CMOS technology. The 1.1 mm^2 IC demonstrator consumes just 3.6 μA of stand-by current when supplied from a 3 V, 225 mA-hr button-cell battery allowing 7 years of standby time, theoretically. A 2.8 F Cap-XX supercapacitor is employed to store the energy generated by the solant. The switched-capacitor charge pump achieves 75% peak efficiency and provides loading resistance in the range of 0.15-4 kΩ. The hybrid DC-DC converter achieves an average efficiency of 64% from an input voltage range of 0.7-2.75 V, and an output ripple voltage less than 1 μV. The power management settings are controlled digitally through a serial interface. The battery lifetime when loaded with the 0.6 mW transceiver described in Chapter 5 is 3 year when operates at 14% duty-cycle.

In chapter 7, the thesis conclusion and original contributions are presented, as well as a few recommendations for a future project.

SAMENVATTING

Dit proefschrift behandelt het ontwerp en de implementatie van een zender en een ontvanger voor een FM-UWB systeem in CMOS. De belangrijkste uitdaging is om een energie-efficiëntie van lager dan 10 nJ/bit te bereiken op een datasnelheid van 100 kbit/s voor zowel de zender als de ontvanger. Verder bespreekt dit proefschrift het ontwerp en de implementatie van een power management unit voor een autonoom draadloos systeem. De uitdaging hierbij is om een hoog rendement DC-DC conversie te bereiken met behulp van een geschakelde condensator topologie en lage spanning rimpel op de uitgangsspanning.

In hoofdstuk 2 worden een aantal modulatieschema's en ultra-wideband technologie kort beschreven als de achtergrondkennis van dit proefschrift. De voordelen van FM-UWB schema's, die een dubbele modulatie gebruiken om een uniform uitgangspectrum en steile spectrale roll-off te realiseren, worden naar voren gebracht. Specificaties voor een FM-UWB transceiver zijn afgeleid en vermeld in de tabel 2.1 van dit hoofdstuk, samen met de conventionele uitvoering van de FM-UWB transceivers. Ontwerpmethodieken die van toepassing kunnen zijn voor een laag vermogen CMOS ontwerp worden beschreven.

In hoofdstuk 3 wordt een volledig geïntegreerde 3-5 GHz-band FM-UWB-zender, geïmplementeerd in een 90 nm CMOS bulk gepresenteerd. De front-end bestaat uit een RF stroom geregelde oscillator (RF-ICO) en een klasse-AB versterker. Uitgezonden data moduleren een sub-carrier oscillator. De 2-FSK gemoduleerde uitvoer wordt versterkt door een transconductor en moduleert rechtstreeks de RF-ICO tune invoer. Een opeenvolgende benaderingsregister (SAR)-algoritme en een on-chip volledig digitale frequentie-locked loop (FLL) ijken de frequentie van de carrier en sub-carrier. Alle spannings- en stroomreferenties nodig voor de zender zijn opgenomen op de chip. De 0,2 x 0,5 mm^2 transmitter's actief gebied verbruikt 900 µW uit een 1V energiebron. Energie-efficiëntie van de zender is 9 nJ / bit continu draaiend op 100 kbit / s.

In hoofdstuk 4, een regeneratieve, FM ultra-wideband (FM-UWB) ontvanger voor een lage datasnelheid (< 100 kbit/s) en de korte afstand (< 10 m) ontvangst in de 4-5 GHz-band wordt beschreven. Deze bestaat uit een 35 dB gain voorversterker, een envelop detector / demodulator, een IF-versterker en een 50 Ω te test buffer. De instelbare (3.8 tot 5,1 GHz)-ontvanger front-end werkt op een 50 MHz sub-band, die is geselecteerd, versterkt en overgezet van FM naar AM door een regeneratieve voorversterker. Energie-efficiëntie van de regeneratieve FM-UWB-ontvanger ten opzichte van de eerder gepubliceerde FM-UWB-implementaties is verbeterd door een factor van 8, tot 22 nJ / bit. Gemeten ontvangersgevoeligheid is 84 dBm bij 100 kbit/s datasnelheid (10^{-3} BER). Geïmplementeerd in 65 nm CMOS-bulk, de 0,3 mm^2 testchip verbruikt 2,2 mW (excl. test buffer) van een 1-V-energiebron.

In hoofdstuk 5 werd een volledig geïntegreerde FM-UWB transceiver voor de 3-5 GHz-band, die benchmarkt het schema voor low-power en korte afstand (< 10 m) toepassingen gerealiseerd in een 90 nm bulk CMOS technologie.De zender maakt gebruik van een RF-stroom-gecontroleerde oscillator (RF-ICO), die werkt op

één derde van de dragersfrequentie en gevolgd door een Tripler-PA, dat de frequentie vermenigvuldigt met drie en versterkt het FM-UWB-signaal, opleverend naar een 50 Ohm belasting. Het maximale uitgangsvermogen is -10.1 dBm, wat resulteert in een zendersenergie-efficiëntie van 13,3%. De ontvanger maakt gebruik van een 40 dB regeneratieve RF-versterker, gevolgd door een envelop detector, IF begrenzer en een FSK demodulator. De gemeten ontvangersgevoeligheid is -80.5 dBm bij 100 kbit/s datasnelheid (10^{-3} BER). On-chip digitale calibratie is doorgevoerd om de RF-ICO en de regeneratieve RF-versterker af te stemmen. De chip wordt digitaal geregeld via een seriële interface en alle spannings-/ stroomreferenties nodig voor de transceiver zijn opgenomen op de chip. De 0,9 mm^2 transceiver IC demonstrator verbruikt slechts 630 µW en 580 µW van een 1-V-energiebron, wanneer het respectievelijk werkt op de zender en ontvanger mode. Het nominale energieverbruik van de transceiver is 6 nJ/bit met een datasnelheid van 100 kbit/s bij continu gebruik.

In hoofdstuk 6 werd een power management prototype, geschikt voor autonome draadloze toepassingen, gevoed door de knoopcel batterij en een zonne-antenne, gerealiseerd in een low-cost 90 nm bulk CMOS technologie. De 1,1 mm^2 IC demonstrator verbruikt slechts 3,6 µA stand-by stroom, wanneer gevoed door een 3 V, 225 mA-hr knoopcel batterij, in theorie gelijk aan 7 jaar standby-tijd. Een 2,8 F Cap-XX supercondensator werd gebruikt om de energie, opgewekt door de solant op te slaan. De geschakelde-condensator lading pomp behaalt 75% maximale efficiëntie en zorgt voor een ladingsweerstand in het bereik van 0,15-4 kΩ. De hybride DC-DC converter haalt een gemiddeld rendement van 64% ten opzichte van een ingangsspanning van 0,7-2,75 V en een output rimpelvoltage minder dan 1 µV. De instellingen voor energiebeheer worden digitaal bestuurd via een seriële interface. De geschatte levensduur van de 0,6 mW transceiver beschreven in hoofdstuk 5 is 3 jaar wanneer hij werkt op een 14% duty-cycle.

In hoofdstuk 7 worden de thesisconclusies en originele bijdragen weergegeven met tevens enkele aanbevelingen voor een toekomstig project.

LIST OF ABBREVIATIONS

AWGN	Additive White Gaussian Noise
AM1.5	Air Mass coefficient (1.5 atmosphere thickness)
AC	Alternating Current
a-Si	Amorphous Silicon
AM	Amplitude Modulation
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
BPF	Band-Pass Filter
BFSK	Binary Frequency Shift Keying
BPSK	Binary Phase Shift Keying
BJT	Bipolar Junction Transistor
BER	Bit-Error Rate
BAW	Bulk Acoustic Wave
C-V	Capacitance versus Voltage
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
CT	Continuous Time
ICO	Current-Controlled Oscillator
dB	deciBel
DEMUX	De-Multiplexer
DAA	Detect and Avoid
DUT	Device Under Test
DSP	Digital Signal Processing
DAC	Digital to Analog Converter
DCO	Digitally-Controlled Oscillator
DC	Direct Current
DDS	Direct Digital Synthesis
DS	Direct Sequence
DFT	Discrete Fourier Transform
DR	Dynamic Range
DUT	Device Under Test
EIRP	Effective Isotropic Radiated Power
ESR	Effective Series Resistance
EMI	Electro-Magnetic Interference
ESD	Electrostatic Discharge
CEPT	European Conference of Postal and Telecommunication Administrations
ETSI	European Telecommunications Standards Institute
FFT	Fast Fourier Transform
FCC	Federal Communications Commission
FOM	Figure of Merit
FSM	Finite-State Machine
FEC	Forward Error Correction

FM-UWB	Frequency Modulation Ultra-wideband
FDMA	Frequency Division Multiple Access
FH	Frequency Hopping
FM	Frequency Modulation
FSK	Frequency Shift Keying
FLL	Frequency-Locked Loop
GaAs	Gallium Arsenide
HBM	Human Body Model
ICO	Current(I)-Controlled Oscillator
IEEE	Institute of Electrical and Electronics Engineers
IR	Impulse Radio
ISM	Industrial, Scientific, and Medical
IO (I/O)	input output
INL	Integral Non Linearity
IC	Integrated Circuit
IF	Intermediate Frequency
ISI	Inter-Symbol Interference
kbps	kilobit per second
LSB	Least Significant Bit
LOS	Line-of-Sight
LUT	Look Up Table
LDR	Low Data Rate
LDO	Low Dropout (Regulator)
LNA	Low-Noise Amplifier
LPF	Low-Pass Filter
Mbps	Megabit per second
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MIM	Metal-Insulator-Metal
MOM	Metal-Oxide-Metal
MSB	Most Significant Bit
MUX	Multiplexer
NBI	Narrowband Interference or Narrowband Interferer
NiMH	Nickel Metal Hydride
NF	Noise Figure
NMOS	N-type Metal Oxide Semiconductor
OOK	On-Off Keying
Opamp	Operational Amplifier
OTA	Operational Transconductance Amplifier
OFDM	Orthogonal Frequency Division Multiplexing
PM	Phase Modulation
PLL	Phase-Locked Loop
PV	Photo Voltaic
PAE	Power Added Efficiency
PA	Power Amplifier

PMAN	Power Management
PSD	Power Spectral Density
PSRR	Power Supply Rejection Ratio
PCB	Printed Circuit Board
PVT	Process, Voltage, Temperature
PTAT	Proportional to Absolute Temperature
PRBS	Pseudo Random Binary Sequence
PMOS	P-type Metal Oxide Semiconductor
PPM	Pulse Position Modulation
QAM	Quadrature Amplitude Modulation
Q	Quality factor
RF	Radio Frequency
RMS	Root Mean Square
SR-FF	Set Reset Flip-flop
SOLT	Short Open Load Through
SNR	Signal-to-Noise Ratio
SG-TFT	Single Grain Thin Film Transistor
Solant	Solar cell Antenna
SMA	Sub-Miniature A
SAR	Successive Approximation Register
SAW	Surface Acoustic Wave
SC	Switched-Capacitor
SC-CP	Switched-Capacitor Charge Pump
SC-DC	Switched-Capacitor DC-to-DC converter
S-R	Set and Reset
TH	Time-Hopping
UWB	Ultra-wideband
UGBW	Unity Gain Bandwidth
VGA	Variable Gain Amplifier
VCO	Voltage-Controlled Oscillator
WBAN	Wireless Body Area Network
WMBAN	Wireless Medical Body Area Network
WMTS	Wireless Medical Telemetry Service
WPAN	Wireless Personal Area Network
WSN	Wireless Sensor Network

LIST OF PUBLICATIONS

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