A 720 nW Current Sensor with 0-to-15 V Input Common-Mode Range and ±0.5% Gain Error from -40 to 85 °C

Zamparette, Roger; Makinwa, Kofi

DOI
10.23919/VLSITechnologyandCir57934.2023.10185309

Publication date
2023

Document Version
Final published version

Published in
Proceedings of the 2023 IEEE Symposium on VLSI Technology and Circuits, VLSI Technology and Circuits 2023

A 720 nW Current Sensor with 0-to-15 V Input Common-Mode Range and ±0.5% Gain Error from −40 to 85 ˚C

Roger Zamparette[1], Kofi Makinwa[1]
[1]Delft University of Technology, Delft, The Netherlands

Abstract

This paper presents a nano-power high-side shunt-based current sensor (CS) that digitizes the voltage drop across an on-chip (±1A) or a lead-frame (±30A) shunt. A TC-tunable ADC reference compensates for the shunts' large temperature coefficient (TC), resulting in ±0.5% gain error from -40 to 85°C. The CS employs a capacitively coupled g_m-boosted front-end followed by a CCO-based ΔΣ ADC. Together with a floating input chopper, this results in an input common-mode range (ICMR) of 0-to-15V, the largest reported for a CS implemented in a standard CMOS process. It achieves high energy efficiency (164dB FoM) while consuming only 720nW, representing a 4× improvement on the state-of-the-art and making this the first ever reported sub-μW smart current sensor.

Introduction

Knowing the battery State of Charge is essential for the reliable operation of IoT devices, and it is typically determined by Coulomb counting. Since it must always be on, this requires a low-power CS [1-4], which, for IoT applications, should also be low-cost. The latter can be achieved using metal shunts, such as on-chip, lead-frame, and PCB traces, but their readout circuits often consume several μWs, significantly impacting battery life. High-side sensing is preferred, but it is an extra challenge in multi-cell battery applications and typically requires an expensive BCD process [3,4]. This work proposes a nano-power high-side CS compatible with low-cost metal shunts and fabricated in a standard 0.18μm CMOS process.

Proposed Current Sensor

As shown in Fig.1a, the CS employs an ADC with a TC-tunable $V_{REF}=V_{PTAT}\pm\lambda\cdot V_{CTAT}$ [2] to digitize the voltage across a metal shunt $V_S = R_S I_S$ while simultaneously compensating for its 1st-order TC (~3500 ppm/°C). The CS can be used with either a lead-frame shunt (300μΩ, ±30A, Fig.1b) or an on-chip metal shunt (40mΩ, ±1A, Fig.1c) [2,4].

Previous TC-tunable V_{REF} generators used separate circuits for V_{PTAT} and V_{CTAT} [1,2]. In this work, V_{REF} is generated by a single circuit to save power (Fig. 2). The PTAT voltage across a dynamic threshold MOST (DTMOST) pair is added to a CTAT voltage $I_{BIAS}\cdot\lambda\cdot R_{CTAT}$, where λ is a trim factor. The use of DTMOSTs instead of BJTs enables V_{DD}<1V since V_{SG} (250mV @ 25ºC) is ~3× smaller than V_{BE} (700mV @ 25ºC). However, a low-TC bias current I_{BIAS} is required to minimize the non-linear temperature dependence of the resulting V_{REF}.

As shown in Fig. 3, I_{BIAS} is generated by forcing the PTAT voltage produced by a DTMOST pair across a silicided poly resistor (R_{SIL}), whose near-PTAT TC results in a near-zero TC current. This is realized by a current-voltage mirror (CVM) [5] rather than the usual opamp, saving power and enabling V_{DD}<1V. The current is then mirrored to another DTMOST pair in series with two 4-bit resistor ladders, R_{MSB} (R_{UNIT}=8kΩ) and R_{LSB} (R_{UNIT}=0.5kΩ) that realize the TC-tuning. A polarity bit λ_{PN} selects the appropriate ladder, resulting in a 9-bit trim DAC using just 34 switches, thus significantly reducing switch leakage while providing accurate Kelvin connections. The CVM and mirrors are chopped at $f_{CH}=f_S/2$ to suppress offset/flicker noise.

As shown in Fig. 4, V_S is sensed by a capacitively-coupled g_m stage, which is chopped at $f_{CH}=f_S/2$, thus suppressing its offset/flicker noise and decoupling the DC levels of the input and the ΔΣM summing node. System-Level Chopping (SLC) further suppresses offset with $f_{SLC} = f_S/64$. The floating input choppers [4] are protected by a custom ESD structure, which enables a high ICMR (<15V). Using a 1st-order ΔΣM ensures a uniform impulse response [2], but its finite DC gain leads to dead zones and low SQNR. A phase quantizing loop filter based on two current-controlled oscillators (CCOs) is employed to address these issues. It provides multi-bit quantization and high DC gain, even for V_{DD}<1V [6]. A phase frequency detector (PFD) quantizes the CCOs' phase difference, resulting in a 4-bit, 3-level output that drives a capacitive DAC C_{DAC}. Compared to [6], the middle level is obtained by simply shorting the bottom plates of C_{DAC}. Finally, dead-banding (DB) suppresses chopping-induced non-linearity [7].

For energy efficiency, the bias current of the g_m stage also supplies the CCOs ($I_{CCOP(N)}$) (Fig.5). Large loop-gain ($\propto g_m\cdot k_{CCO}$) is required for high SQNR, while reducing k_{CCO} reduces f_{CCO} and dynamic power consumption. A current-reuse g_m-boosting scheme is proposed to decouple the g_m choice from the I_{CCO}. The cross-coupled M_{boost} transistors create a negative g_m that boosts the effective g_m (g_{meff}) to, ideally, infinity. The series resistors R_S stabilize the system and define $g_{meff}=1/R_S=4\mu S$ (~3x the g_m of M_{gm}) with $I_{CCOP(N)}$ =60nA and f_{CCO}=16kHz. They also provide pseudo-differential degeneration, leading to a wider input range. A large bias resistor R_B=5GΩ is required to minimize its noise contribution, which is realized as a Segmented Duty-Cycled Resistor (SDCR) [1] operating at $f_{SDCR} = f_S$.

Measurement Results and Performance Summary

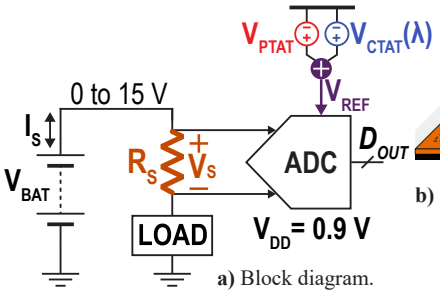
The CS is fabricated in a standard 0.18μm CMOS process (Fig.6a) and consumes 720nW from a single 0.9V supply. The ADC achieves a $4\mu V_{RMS}$ resolution in a 5ms conversion time for f_S=32kHz. Decimation is performed off-chip for flexibility. The chip is shown in Fig 6b mounted on the lead-frame from a standard package.

Fig.7 shows ΔI_{OUT} vs. ΔV_{IN} of the g_m stage with and without g_m-boosting. As shown in Fig. 8, the lower quantization noise and increased gain with g_m-boosting increase the modulator's thermal-noise limited BW from ~60Hz to ~200Hz. Fig. 9 and Fig. 11 show the D_{OUT} (I_S=0.5A, on-chip / I_S=20A, lead-frame) and I_{BIAS} variation from −40 to 85°C for a typical sample. The TC of I_{BIAS}=140ppm/°C, and the on-chip/lead-frame D_{OUT} variation is ±0.3%/<0.5%. Fig.10 shows the gain error for the on-chip/ and lead-frame shunts (0.5%, four samples each) after a room temperature gain trim and a λ batch calibration. The spectrum for different ICMs is shown in Fig. 12, demonstrating the 0-to-15V ICMR. The offset stays below 100μV/5μV with SLC on/off for eight samples, as shown in Fig.13.

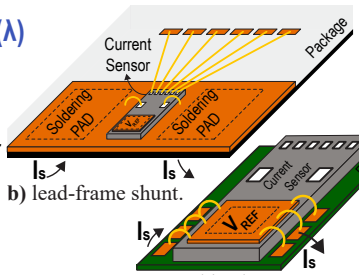
The sensor's performance is summarized in Tab.1. Compared to the state-of-the-art, it requires ~4× less power and is more energy efficient. Moreover, it supports high-side sensing up to 15V and is the first reported sub-μW CMOS current sensor.

References

[1] Z. Tang ,*et.al.*, *ISSCC,* 2023. [2] R. Zamparette,*et.al.,VLSI*, 2021.
[3] C. Vroonhoven, *ISSCC,* 2020.[4] L. Xu, *et al., ISSCC,* 2018.
[5] K. Souri, *ISSCC,* 2014. [6] W. Zhao, *JSSC,* 2019.
[7] H.Chandrakumar, *JSSC*, 2018



a) Block diagram.



b) lead-frame shunt.

c) on-chip shunt.

Fig. 1: Diagram of the shunt resistor-based current sensor system.

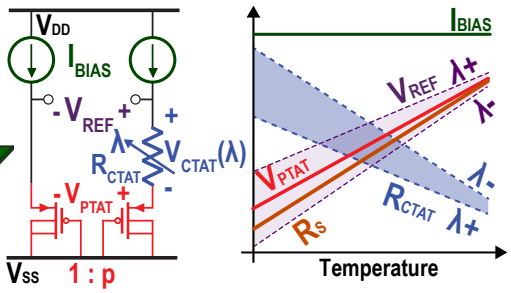


Fig. 2: Temperature compensation scheme.

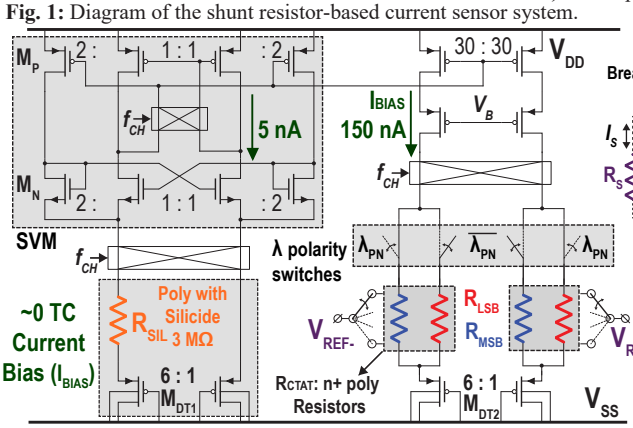
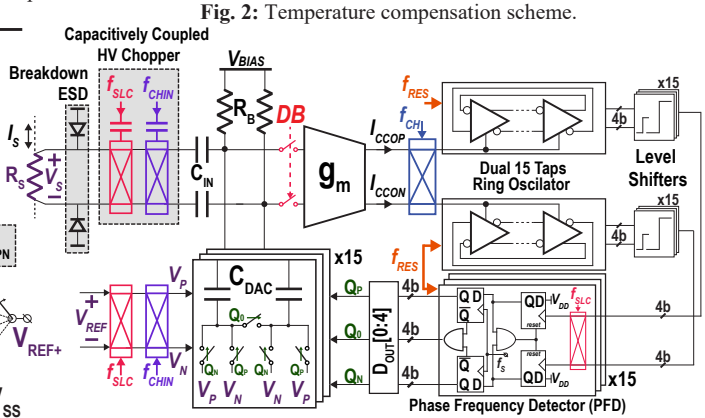


Fig. 3: V_{REF} and I_{BIAS} generation.



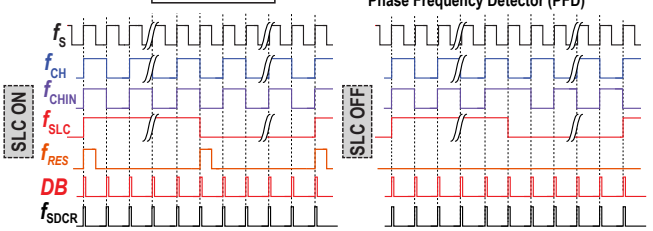


Fig. 4: Diagram of the readout circuit.

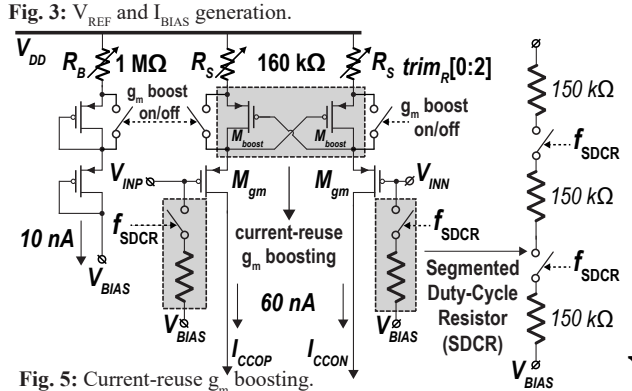


Fig. 5: Current-reuse g_m boosting.

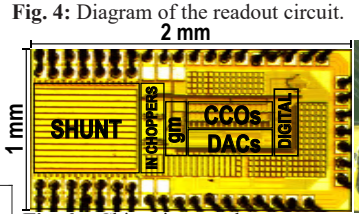


Fig. 6a: Chip micrograph.

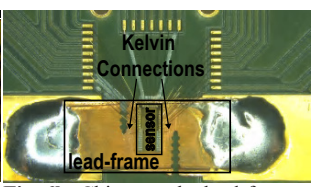


Fig. 6b: Chip over the lead-frame

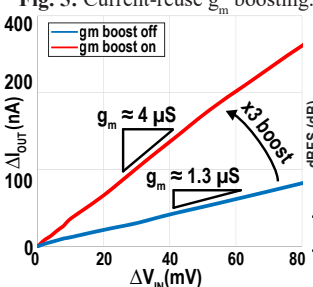


Fig. 7: g_m boost.

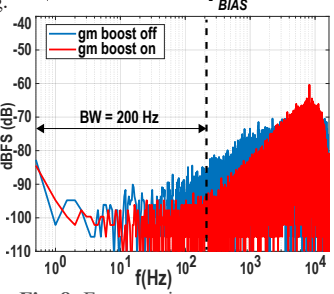


Fig. 8: Free running spectrum.

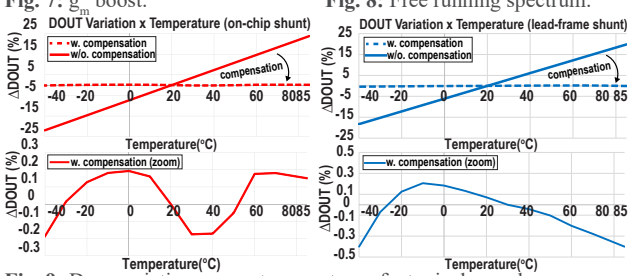


Fig. 9: Dout variation versus temperature of a typical sample.

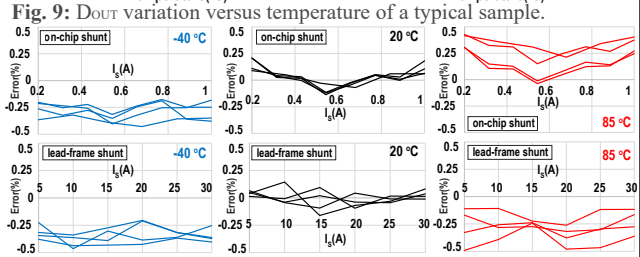


Fig. 10: Gain error.

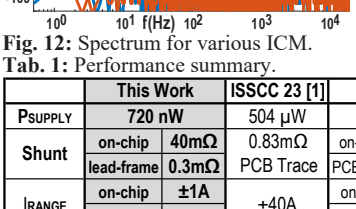
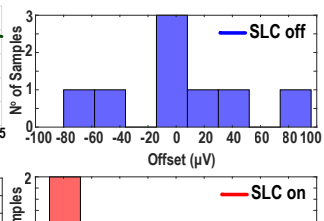


Fig. 11: I_{BIAS} vs. Temperature.



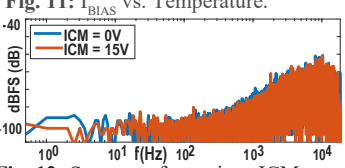


Fig. 12: Spectrum for various ICM.

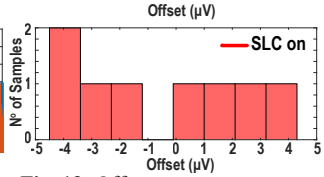


Fig. 13: Offset.

Tab. 1: Performance summary.

	This Work		ISSCC 23 [1]	VLSI 21 [2]		ISSCC 20 [3]	ISSCC 18 [4]
P_{SUPPLY}	720 nW		504 µW	2.5 µW		9 µW	19.6 µW
Shunt	on-chip	40mΩ	0.83mΩ	on-chip	20mΩ	50mΩ	10mΩ
	lead-frame	0.3mΩ	PCB Trace	PCB trace	3mΩ	low-TCR*	on-chip
I_{RANGE}	on-chip	±1A	±40A	on-chip	±2A	±1A	±4A
	lead-frame	±30A		PCB trace	±15A		
Gain Error	on-chip	±0.5%	±0.2%	on-chip	±0.35%	±0.5%*	±0.9%
	lead-frame	±0.5%		PCB trace	±0.6%		
Offset	5µV		4µV	500nV		1µV	400nV
ICMR	0 to 15V		low-side	-0.3 to 5 V		0 to 60 V	0 to 25 V
Tech.	0.18		0.18	0.18		0.18 BCD	0.18 BCD
V_{SUPPLY}	0.9V		1.8 V	1.8 V		1.7V	1.5V
T_{RANGE}	-40 to 85°C		-50 to 125°C	-40 to 85°C		-50 to 125°C	-40 to 85°C
Resolution	4µV$_{RMS}$		1.4µV$_{RMS}$	5.4 µV$_{RMS}$		-	1.5µV$_{RMS}$
T_{CONV}	5ms		0.1ms	16ms		-	2ms
FOM**	164dB		160dB	149dB		-	162dB

* Uses a custom/off-chip low-TCR shunt

** FoM=Dynamic Range + 10log(Bandwidth/Power)