

M.Sc. Thesis

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A Continuous Calibration Method  
For the Transfer Stabilization of  
Successive Detection Logarithmic Amplifiers

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# A Continuous Calibration Method for the Transfer Stabilization of Successive Detection Logarithmic Amplifiers

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THESIS

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# Abstract

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To ensure efficient and reliable operation of power amplifiers it is very important to precisely measure and control the power of the signal they transmit. A device most often used to do precise power measurements of RF systems is the so-called RF power detector. As this detector is used as measurement device the precise measurement ability of the RF power detector is very important. For the precise predictability of the output power of power amplifiers the transfer of the RF power detector has to be fixed and accurately known.

In this thesis we develop a new calibration method for the transfer stabilization of logarithmic power detectors. Via thorough investigation at system level and circuit level it is shown that the proposed method can be used to continuously calibrate the transfer of a logarithmic RF power detector to a predefined and fixed position over mismatch, part-to-part spread, temperature and input frequency.

The method depends on a novel switching algorithm around a log device that is capable to do continuous slope, intercept and dynamic range correction on the transfer of the logarithmic power detector. When accurate enough, the method would make calibration of each individual device unnecessary. Furthermore a new method is presented that can be used to extend the dynamic range of log detectors. System simulations show that the calibration method leads to the wanted transfer stabilization of the logarithmic power detector.

A critical part of the new logarithmic transfer calibration method is the need of an accurate multiplication procedure at the input of the logarithmic device. For this accurate multiplication a new accurate gain fixation procedure for a non-linear high bandwidth gain stage was developed. A big part of the thesis is dedicated to the investigation and circuit implementation of this new accurate and fast gain fixation procedure. The gain stabilization method leads to the implementation of a new innovative gain fixation system, including several new architectural innovations. One of these innovations is the implementation of a new accurate ripple blocking system with relative small form factor and fast response time. Simulation results of the circuit implementation of the gain stabilization system prove that the accuracy of the gain stabilization of the non-linear high bandwidth gain stage is well within the required specifications.



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*Dedicated to my parents....*





# 1 Introduction

## 1.1 RF Power Detection

People nowadays are used to communicate with anyone, at any time, from any place. This is only possible through the aid of wireless technology [1]. Various wireless technologies have literally changed the way we live. Cell phones, Wireless LAN, Bluetooth, and GPS are examples of technologies that reached must-have status with consumers worldwide.

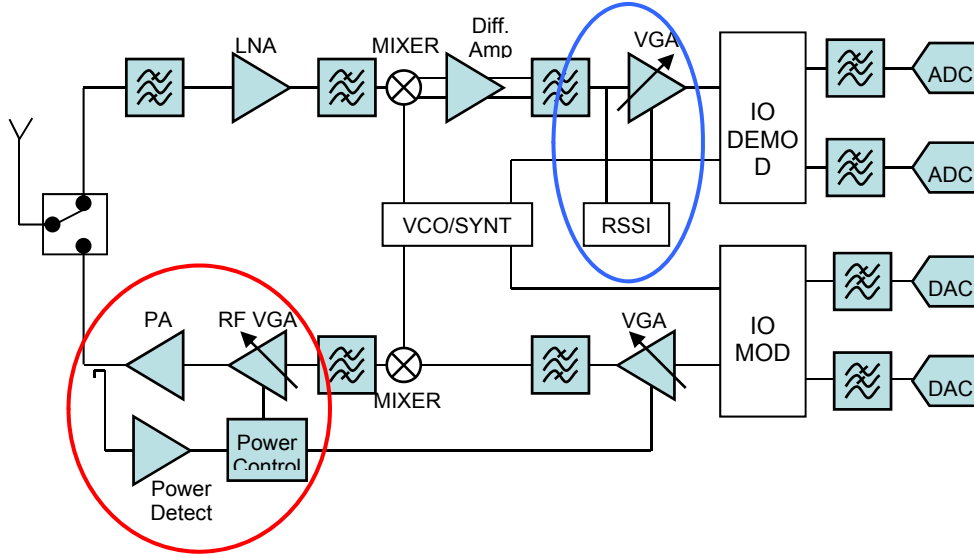
When information is transmitted over Radio Frequencies (RF), power amplifiers are utilized. To ensure efficient and reliable operation of these power amplifiers it is very important to precisely measure and control the power of the signal they transmit. RF-power measurements and control inside for example a mobile communication system is needed to continuously adjust power levels to ensure reliable and efficient communication between the mobile handsets and wireless base stations.

RF power management allows the transmitted power to be precisely adjusted to the minimum required power level, which is of great importance in mobile communications system because it reduces the possible occasion of so-called co-channel interference and minimizes the power consumption. Minimizing the power consumption is particularly important for handsets, as most handsets operate on batteries which have a finite amount of power storage. Minimizing the power consumption will extend battery life, prolonging the usage time for portable handsets. Especially nowadays minimizing the power consumption is increasingly getting more important, because consumers are doing more with their handsets than ever before. Where mobile phones in the past were only used for voice communications, today mobile phones are also increasingly used for to connect to the internet over long and short distance wireless data connections to transmit and receive multimedia content. Emerging telecommunications applications such as music download, multimedia streaming, content browsing and on-line gaming are popular examples of the digital revolution we have been facing as the world gets connected. As consumers increase their use of multimedia content, the demand for high throughput with robust wireless connectivity continues to grow rapidly. As a result mobile phones requires more power to operate than ever before, thereby setting the need for high power energy efficiency.

In base stations, which are responsible for handling traffic and signaling of mobile phones, accurate RF power management is also of great importance. Monitoring and controlling the performance of power amplifiers inside these base stations makes it possible to maximize the output power while achieving optimal linearity and efficiency [2]. Reduced overall energy consumption of base stations not only minimizes their impact on the environment, but also gives financial benefits to telecom industry because of lower energy cost.

## 1.2 The RF power detector

A device which is most often used to do precise power measurements of RF systems is the so-called RF power detector. An RF power detector is a device that produces a DC output voltage which is proportional to the RF power level of the signal applied to its input. Figure 1.1 shows a typical modern communications signal chain where the transmit and receive sections are measured and controlled by RF power detectors [3].



**Figure 1.1** Typical modern communications signal chain

Both detectors are part of a so-called Automatic Gain Control (AGC) system. The AGC system in the receiver section (upper ellipse) is used to control the received signal strength. The signal strength is a key factor in maintaining optimal sensitivity and selectivity which is necessary for reliable communication. The AGC loop in the transmitter section (lower ellipse) is used to control the amount of power transmitted. The amount of power transmitted is critical for maintaining the range and reliability of the radio link but also to assure compliance with government regulations.

### 1.3 The definition of signal power in RF systems

Before we go into more detail about power detectors we first have to know more about the definition of signal power in RF systems.

The signal power in watts is most commonly inferred from a measurement of the Root Mean Square (RMS) voltage squared, divided by the load impedance, as shown by following equation [4]

$$P_{IN} = \frac{V_{IN\_RMS}^2}{R} \quad (1.1)$$

In RF systems the signal power is usually specified in dBm. The dBm unit is defined as the power in dB relative to 1 mW and can be calculated as follows

$$P_{dBm} = 10 \log_{10} \left( \left( \frac{V_{IN\_RMS}^2}{R} \right) / 1mW \right) \quad (1.2)$$

From Equation (1.2) it follows that 0 dBm occurs at 1mW, +10 dBm corresponds to 10 mW, +30 dBm corresponds to 1 W, etc. Because impedance is a parameter of this equation, it is always necessary to specify load impedance when talking about dBm levels. For RF power

measurements it is common to use an RF load impedance level of 50 ohm. Because most RF systems have a constant load and source impedance of 50Ω, we only need to know the RMS voltage to calculate the power [3]. As a result, many practical power measurement circuits rely on measuring RMS voltage.

The RMS voltage is a fundamental measurement of the magnitude of an AC signal and can be defined both practically and mathematically.

**Defined practically:**

The RMS voltage value assigned to an AC signal is the amount of DC voltage required to produce an equivalent amount of heat in the same load. For example: an AC signal of 1 volt RMS will produce the same amount of heat in a resistor as a 1 volt DC signal [3].

**Defined mathematically:**

The RMS value of a voltage is defined as:

$$V_{RMS} = \sqrt{\frac{1}{T} \int V(t)^2 dt} \quad (1.3)$$

According to this definition, the average power is a metric for the average energy content of a signal and is independent of the waveform of the signal in time.

According to Equations (1.1-1.2) a RF power detector should measure the RMS value of the input signal. However, depending on the internal detection mechanism of the RF power detectors, as will be discussed in later sections, there are detectors which do not respond to the RMS value of the signal but rather to some other average. As a consequence these non-RMS responding detectors will be waveform dependent, resulting in different measurement readings at the detector output, for input signals of equal RMS power but different shape. e.g. for a 0 dBm WCDMA signal the output is different from an 0 dBm signal with an unmodulated carrier.

## 1.4 Signal Crest-Factor

Especially for input signals that exhibit a high crest-factor, the non-RMS responding detectors will cause errors in their output reading. When we talk about the crest factor of a signal, we are referring to the ratio of peak voltage to the RMS value of the signal. For an RF system this corresponds to the envelope's peak to average power ratio (PAR) [4] [5]. DC voltages have a crest factor of 1 since the RMS and the peak amplitude are equal, which also holds for a amplitude symmetrical square wave. Other waveforms, more complex in nature, have higher crest factors, as shown in Table 1.1. [6]

**Table 1.1** Known proportionalities between RMS and average values

Waveform 1 Volt Peak	V <sub>RMS</sub>	Crest Factor
Undistorted Sine-wave	$V_{peak} / \sqrt{2} = 0.707 \cdot V_{peak}$	$V_{peak} / V_{RMS} = 1.414$
Symmetrical Square-wave	$V_{peak} / 1 = V_{peak}$	$V_{peak} / V_{RMS} = 1$
Undistorted triangle-Wave	$V_{peak} / \sqrt{3} = 0.580 \cdot V_{peak}$	$V_{peak} / V_{RMS} = 1.73$

In general we can say that an error in the interpretation of the log detector output will occur if the waveform of the signal is unknown. However from Table 1.1 we can see that when the signal shape is known, the crest factor of the signal can be used to calculate the real power of the signal. The known proportionality between the RMS and peak values is a very interesting property for power detectors in which the internal detection mechanism is based on peak voltage detection.

When these type of power detectors are dealing with a known input signal shape with relative low crest-factor the peak-to-average ratio can be used to cancel out the error during production, by means of calibration. However, for signals with varying crest factor it will be difficult to use calibration. A calibration method to correct the measurement error caused by the varying crest factor is to make use of look-up tables. Calibration using look-up tables is often attempted to correct for simple modulated waveforms. However for signals that are modulated and multiplexed with techniques like higher-order Quadrature Amplitude Modulation (QAM) [5], the use of look-up tables becomes very difficult to cancel out the error [7] [8] [9]. This is because of their complex waveforms with high crest-factors which are changing over time [10]. Especially the changing crest factors over time, which is common in wireless cellular networks due to the ever changing number of calls being carried by a cellular base station [11], makes it difficult to use look-up tables [3]. Removing the error at the output of such systems requires keeping track of how many users are on the system, tight control of which Walsh codes are being used, and a very large look up table in order to know the peak-to-average ratio of the signal at a particular time.

For complex signals used in for example WCDMA cellular systems or next generation wireless communications systems using Orthogonal Frequency Division Multiplexing (OFDM) signals [12], such as WiMAX and LTE [13], which employ multiple carriers, each modulated with high-order QAM modulation, the use of look-up tables is becoming inadequate. These types of signals, can have crest factors as high as 10 to 13 dB and changing over time [14].

In systems where such high-crest-factor signals have to be precisely measured and controlled, a true RMS detector is generally more desirable, since these detectors are largely immune to variations in crest factors. As the name of this detector already indicates they perform a true RMS measurement. A true RMS detector provides a 'DC' output voltage equal to the RMS value of its input voltage, independently of the input signal wave shape.

From the previous discussion, it can be concluded that, depending on the complexity of the signal to be measured, RMS or non-RMS RF power detectors can be chosen to provide the optimum solution for precise power measurement.

## **1.5 Importance of precise power measurements**

Precise measurement ability of the RF power detector is very important because it determines the accuracy of the output power of the system that it controls. The precision and stability of the measurement is therefore dependent upon the accuracy and predictability of the input to output transfer of the detector. The accuracy and predictability of the transfer of the detector is a considerable challenge to designers of power detectors. To reach high quality performance, designers have to minimize the drift of the detector transfer over various conditions, most importantly temperature. Errors due to temperature dependence of elements from which power

detectors are constructed often are substantial. With proper design, the temperature dependency can be greatly reduced, but even after temperature dependencies are removed, structural architectural details of the design will introduce deviations in the detector transfer.

## 1.6 The quality measure of RF power detectors

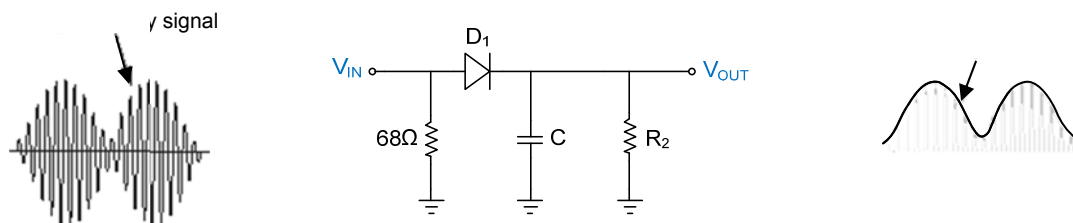
To examine the deviation of the detector's transfer over various conditions, manufactures use a quality measure, which is called the "log conformity error". When we talk about the log conformity of a power detector, we actually say that we are interested in the conformance of the amplitude, in decibels, of the actual output response of the detector to the ideal output response over the full dynamic range of detector. With this measure the linear-in-dB linearity and deviations of the detector's transfer are examined. Later in this report a more thorough discussion about the log conformity error is given.

## 1.7 Types of RF Power Detectors

The structure of the power detector largely determines the precise measurement or accuracy of the system. Besides change in response vs. signal crest-factor and temperature stability, characteristics such as dynamic range, power consumption, ease of integration, size, overall component count and operating frequency are also important to take into account. To get a better understanding of the different power detector characteristics as was mentioned in previous section we will now start to discuss the different RF detector types.

### 1.7.1 Diode Detector

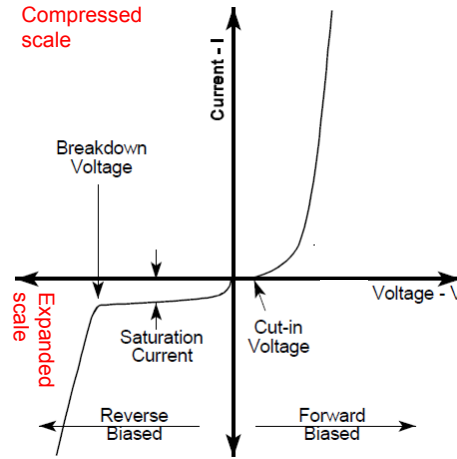
The first type of detector to be discussed is the diode detector. [4] Compared with other types of RF detectors diode detectors are the cheapest and the simplest to implement. This detector, which is shown in Figure 1.2, functions as a simple half-wave rectifier.



**Figure 1.2** Diode detector

The heart of the circuit is the detector diode  $D_1$ , which converts the RF input voltage  $V_{IN}$  into a rectified unidirectional current. Resistor  $R_2$  and capacitor  $C$  form a filter that produces the DC detector output voltage,  $V_{OUT}$ . The averaging time of this filter must be sufficiently long to allow filtering at the lowest frequencies of operation desired. The diode impedance for small RF signals is typically much larger than the required 50  $\Omega$  [15]. To provides the approximately right 50  $\Omega$  input impedance match used in RF systems a separate matching resistor of 68  $\Omega$  is placed at the input of the detector circuit. [3]

The I-V characteristic of semiconductor device like the diode, as well as the BJT and FET, are non-linear. As will be shown, the operation of the diode detector depends on this nonlinearity.

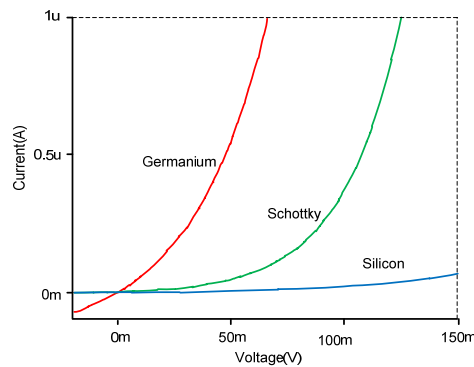


**Figure 1.3** I-V characteristic of a diode with some scales expanded and others compressed in order to reveal details

Figure 1.3 shows the I-V characteristic of a diode. We have to note that the scales of the axes in this figure are modified in order to reveal details. When a diode is reverse biased, very less current passes through unless the reverse breakdown voltage is exceeded. When forward biased and after exceeding the cut-in voltage of the diode, the current starts increasing rapidly. The diode-detector transfer function can be divided into two distinct regions, which are known as "square law" and "linear" region. For larger input signals, the detector works in the "linear" region. In this region the output signal varies linearly with the input-signal envelope, as is shown in Figure 1.2. The square-law region is operative for very small input-signal levels. In this region, the output  $V_{OUT}$  is proportional to the square of the RF input voltage  $V_{IN}$ , which means that  $V_{OUT}$  is proportional to the input power [16]:

$$\begin{aligned} V_{OUT} &= nV_{IN}^2 = nP_{IN} \\ P_{IN} &\propto V_{OUT} \end{aligned} \quad (1.4)$$

Where  $n$  is the proportionality constant. The proportionality constant  $n$  depends on how "curved" the diode's I-V curve is [17]. Diodes with a sharp I-V curve will give more output sensitivity, as can be seen in Figure 1.4.



**Figure 1.4** I-V characteristic of a different type of diodes

Before we will discuss some non-idealities of the diode we first will clarify the quadratic and linear behaviour of the diode mentioned before.

The basic functionality of a diode can be described using the well-known diode equation:

$$I_D = I_S \left( e^{\frac{qV_D}{nkT}} - 1 \right) \quad (1.5)$$

where,

$I_D$  ... diode current

$I_S$  ... saturation current

$q$  .... charge of electron ( $1.6 \cdot 10^{-19}$  C)

$V_D$  ...voltage across the diode

$n$  .... "non-ideality" coefficient (typ. between 1 and 2)

$k$  .... Boltzmann's constant ( $1.38 \cdot 10^{-23}$ )

$T$  .... junction temperature in kelvin

When looking at Equation (1.5), it seems to be somewhat confusing to talk about a quadratic and a linear region, while the diode equation is actually described by an exponential function. To explain the quadratic behaviour for low amplitude input signals, we have to approximate the exponential function  $e^x$  by its polynomial [15]:

$$e^x = \sum_{p=0}^{\infty} \frac{x^p}{p!} = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \dots + \frac{x^p}{p!} \quad (1.6)$$

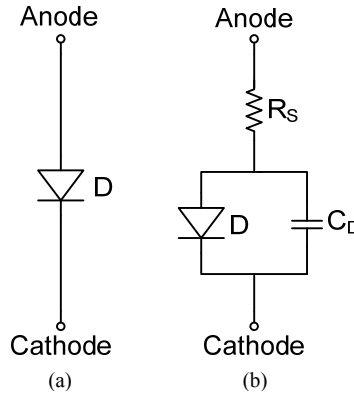
With the use of Equation (1.6) the I-V behaviour of the diode represented by Equation (1.5) can be rewritten in terms of the following polynomial:

$$I_D = I_S \left( \frac{qV_D}{nkT} + \frac{\left( \frac{qV_D}{nkT} \right)^2}{2!} + \frac{\left( \frac{qV_D}{nkT} \right)^3}{3!} + \dots + \frac{\left( \frac{qV_D}{nkT} \right)^p}{p!} \right) \quad (1.7)$$

Equation (1.7) shows us that for small enough signals, a second-order approximation is sufficient. This shows that for small signals we can say that the diode detector is working in its square-law region.

The square-law detection region is relatively small. For a typical packaged diode, the square-law detection region holds from the noise level up to approximately -20dBm. A transition region ranges from approximately -20 dBm to 0 dBm input power, while the linear range extends above approximately 0 dBm. As a result the input dynamic range of this type of power detector is limited. Typically a dynamic range of 20-25 dB can be realized.

For the linear region when operating at higher signal levels we have to take a look at a more complex model of the diode. The more complex model of the diode is depicted in Figure 1.5(b).



**Figure 1.5** The (a) ideal diode and (b) the more realistic diode model

As shown in Figure 1.5(b) the more realistic diode model includes an internal series resistance  $R_S$  and a parasitic capacitance  $C_D$ . However, when we look at Equation (1.5) it is shown that the diode equation doesn't describe the influence of these elements. So, actually, this diode equation is only an approximation of a more complex I-V characteristic of a diode.

The linear operation of the diode detector at higher signal levels can now be explained as follows. At high input signals the small signal resistance of the diode will be very small. From the model in Figure 1.5(b) it can be shown that in this situation the resistor  $R_S$  will start to dominate. In this situation the current will be limited by the internal resistance  $R_S$ . Since the resistance  $R_S$  is  $V/I$  the resulting signal will be linear.

Real-world diodes exhibit a small amount of capacitance between their two terminals [18]. The capacitor  $C_D$  parallel with the intrinsic diode as shown in Figure 1.5(b) models the parasitic capacitance. This so-called parasitic capacitance of a diode is important to take into account, because it limits the maximum frequency of the signal that can be measured accurately by the diode detector. At higher frequencies, the impedance of the capacitance is low, resulting that current will leak away through the capacitance instead of the low-pass filter of the detector ( $R_2$  and  $C$  from Figure 1.2). Because some of the current flows through capacitance  $C_D$  and never reaches the low-pass filter, the detected voltage will be reduced.

The forward voltage is another important characteristic of a diode. A large forward voltage limits the sensitivity for very small signals, because the detector only works when the peak RF voltage is greater than this voltage. Therefore, the best choice for the diode seems to be a very low barrier device.

The characteristics as described previously depend on the type of diode that is used [19].

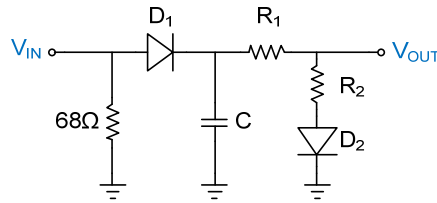


One of these types is the so-called point-contact diode. An advantage of this type of diode is that it has a very low forward voltage and has very small parasitic capacitance. However it also has a disadvantage: it is quite fragile and is difficult to manufacture in a repeatable manner.

A type of diode that has a larger forward voltage but is easier to be manufacture is the pn junction diode. However, compared to a point-contact diode, the junction capacitance of a pn diodes can be an order of magnitude higher.

Another type of diode is the Silicon Schottky diode [20]. It is commercially available in four different versions, offering forward voltages of approximately 600 mV for high barrier, 330 mV for medium barrier, 280 mV for low barrier, and 180 mV for zero-bias detectors. GaAs Schottky diodes produce a forward voltage of approximately 700 mV. Because a Schottky diode's junction can be made very small, therefore, the junction capacitance would be quite small.

Besides the drawback of their limited range as was described earlier, diodes have another problem, which becomes clear when we look again at Equation (1.5). This equation shows that the current through the diode not only depends on the voltage  $V_D$  across the diode but also on its junction temperature. Consequently, the output rectified voltage of the diode detector, will vary with temperature. Since detectors are also used in feedback loops, this temperature dependence is highly undesirable. However, with additional components, the temperature dependence can be minimized. [21] [22] [3] When we implement a second identical diode and resistor, as shown in Figure 1.6, we can, in principle, eliminate the temperature variation.



**Figure 1.6** A temperature compensated diode detector

That this implementation eliminates the temperature variation can be shown with following analysis. When we assume the currents entering en leaving the  $V_{OUT}$  node are the same and resistor  $R_1$  and  $R_2$  are identical, we can say

$$\frac{V_{R1}}{R_1} = \frac{V_{R2}}{R_2} \Rightarrow \frac{\hat{V}_{IN} - V_{D1} - V_{OUT}}{R_1} = \frac{V_{OUT} - V_{D2}}{R_2} \quad (1.8)$$

Because both resistors are identical, we can simplify the equation to

$$\hat{V}_{IN} - V_{D1} - V_{OUT} = V_{OUT} - V_{D2} \quad (1.9)$$

Then, solving for  $V_{OUT}$  leads to

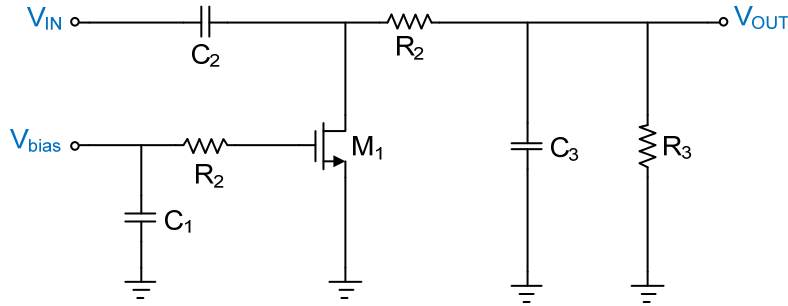
$$V_{OUT} = \frac{V_{D1} - V_{D2} + \hat{V}_{IN}}{2} \quad (1.10)$$

Since diode  $D_1$  and  $D_2$  are identical, a temperature variation will cause equal voltage drop over both diodes. Because voltage  $V_{D1}$  and  $V_{D2}$  are matched, Equation (1.10) can be simplified to

$$V_{OUT} = \frac{\hat{V}_{IN}}{2} \quad (1.11)$$

From Equation (1.11) it is clear that the temperature dependence of the diode detector is eliminated. From the same equation it becomes clear that diode detectors actually measure the peak power instead of the RMS power. So, because of their non-RMS measure, their response will depend on the signal shape or modulation as was discussed in Section 1.1.

There is one practical note for the temperature compensated circuit we discussed. A sensing circuit at  $V_{OUT}$  should not load this node too much, because this will lead to a different current through the diodes which will defeat the temperature compensation.



**Figure 1.7** A power detector with one FET

Earlier in this section we already mentioned the non-linear characteristic of a FET. This non-linear characteristic can also be used to implement power detection [23] [24]. The circuit implementation of a power detector with one FET is shown in Figure 1.7.

In this circuit the drain voltage of  $M_1$  is close to zero. So if the gate-source voltage  $V_{GS}$  is set slightly higher than  $V_{TH}$ , it will bias  $M_1$  at the borderline between the triode and saturation region.

The standard equation for the drain current of a FET transistor in saturation region is

$$I_D = \frac{K}{2} (V_{GS} - V_{TH})^2 \quad (1.12)$$

where  $K$  is the device parameter that includes the physical dimensions of the device, electron mobility and oxide capacitance.

Since the drain voltage of  $M_1$  is close to zero and  $V_{GS}$  is set slightly higher than  $V_{TH}$  we can say  $V_{GS} = V_{DS} + V_{TH}$ . In this situation we can simplify Equation (1.12) to

$$I_D = \frac{K}{2} (V_{DS}^2) \quad (1.13)$$

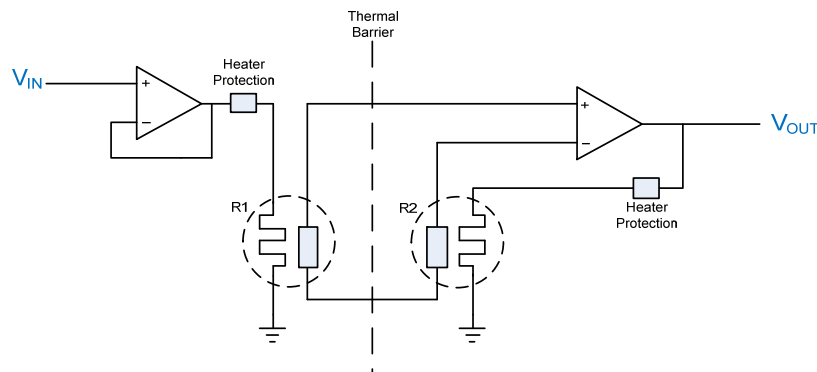
Equation (1.13) shows that a square law relationship between input RF signal,  $V_{DS}$ , and output rectified current  $I_D$  is established. This is why the RF input is applied at the drain of  $M_I$  and not at its gate. The rectified output current goes through load resistor  $R_3$  to establish the output voltage.  $R_3$  and  $C_3$  form the output low pass filter.

### 1.7.2 RMS Detector

As we can conclude from the previous section, the disadvantage of diode detectors, when used as control for transmitted power, is that they are sensitive to input signals with high and time varying crest-factors, such as CDMA and W-CDMA. The sensitivity on crest factor of a detector can be made independent when its operation is based on direct determination of the average power and not – like the diode detector – on the peak power. A detector that makes use of this operation principle is the so-called true RMS detector. These detectors provide a ‘DC’ output voltage equal to the RMS value of its input voltage, independently of the input signal crest factor.

There are different approaches to implement the true RMS measurement principle. The first approach to be discussed is measuring power by thermal detection . [4] [6]

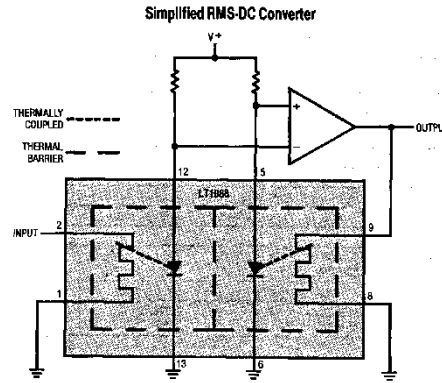
Thermal detection essentially involves the implementation of the practical definition of RMS that was discussed in the introduction [3]. “Thermal detectors like bolometers (e.g. thermistors or thermo-couplers) convert the electrical power of RF signal into thermal energy using a resistive component, and then measure the temperature variation with respect to the ambient temperature.” [4]. Figure 1.8 shows a thermal based approach with thermal detectors, wherein a thermal measurement and control circuit is used to measure the heating power dissipation of the input RF signal.



**Figure 1.8 Thermal based approach with thermal detectors**

“In this circuit, an unknown signal and a known calibrated reference voltage each heat identical resistors. Adjacent to each resistor are thermocouples the output voltages of which are proportional to the respective temperatures. The voltage difference between the two sensors represents a scaled measure of the unknown power relative to the reference power. A similar result can be achieved using two thermistors in a bridge configuration. These schemes can be very accurate and provide RMS detection since the temperature difference is proportional to the power dissipation. Because operation depends on thermal symmetry, care must be taken in matching the sensors and keeping them thermally isolated while electrically connected. This system is also sensitive to temperature gradients caused by adjacent objects, or circuits. Furthermore, the response time is limited by the slow thermal time-constants and the system is not readily integrated” [4].

An integrated thermal detection method is shown in Figure 1.9.

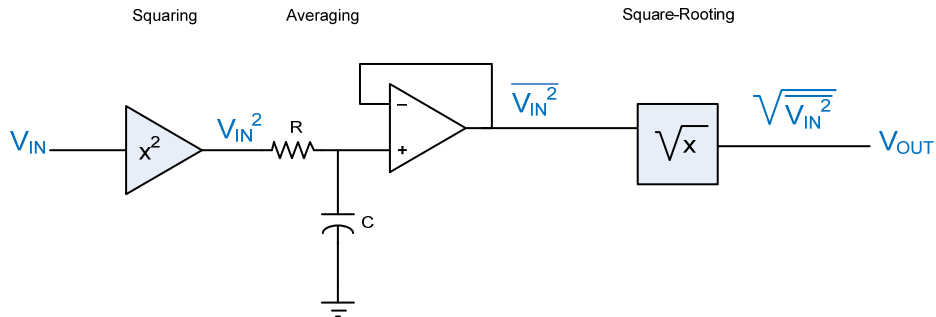


**Figure 1.9** Integrated thermal detection method [25]

A simpler method to implement the RMS-DC conversion is to put the mathematical definition of RMS, as shown by Equation (1.3), in silicon. According to Equation (1.3), we have to build a circuit that squares the signal, takes the average, and obtains the square root.

RMS detectors typically fall into one of two categories; explicit or implicit. [6]

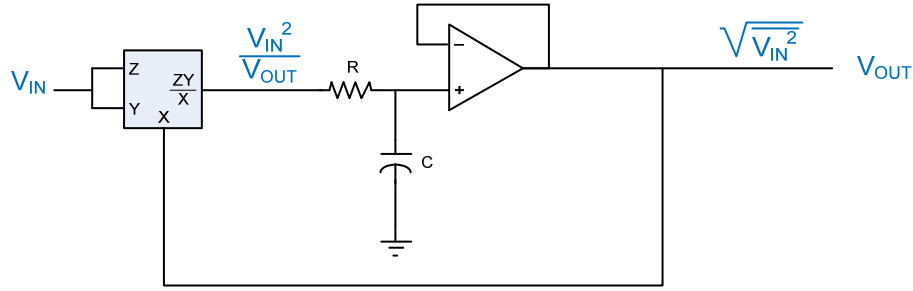
The explicit RMS detector can be recognised by its straight-forward manner of performing the functions of squaring, averaging, and square rooting.



**Figure 1.10** Computation method used in explicit RMS detectors

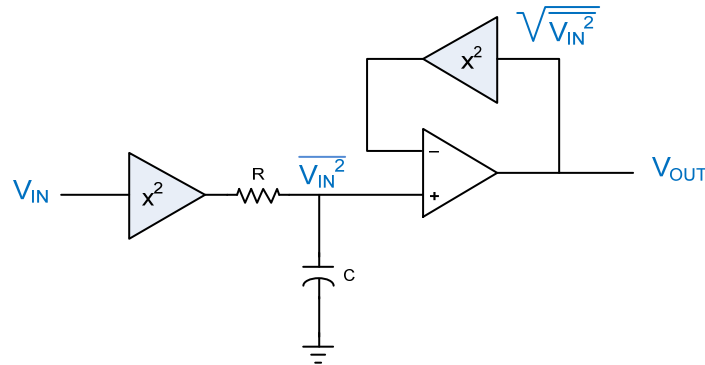
The explicit RMS detector circuitry is shown in Figure 1.10. As shown by this figure it explicitly perform the RMS calculation by first squaring the input signal by a squarer, then averaging it by the filter, and finally computing the square root by the square root block. Although the explicit computation seems to be the most obvious method, it has its disadvantage. Squaring the input signal reduces the dynamic range of the detector, because the stages following the squarer must try to deal with a signal that is twice as large in dB. On the other hand, this method can achieve excellent bandwidth.

A generally better approach is the computation method used in implicit RMS detectors. Implicit RMS detectors incorporate indirect computation of the square root, accomplished, for example, by means of feedback and analog division at the input of the circuit as shown in Figure 1.11. [6]



**Figure 1.11** Computation method used in implicit RMS detectors

Divided by the average of the output, the average signal level now varies linearly (instead of quadratically) with the RMS level of the input. The feedback mechanism considerably increases the dynamic range of the implicit circuit, as compared to explicit RMS circuits. Unfortunately, because of the negative feedback topology the high frequency performance of the implicit detector is limited. As a consequence the practical bandwidth of these types of detectors is generally less than the thermal or the explicit computation method.

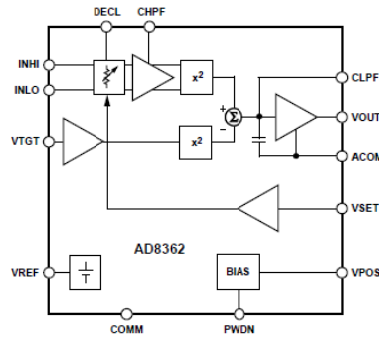


**Figure 1.12** RMS responding detector

An RMS detector that uses squaring-cells is shown in Figure 1.12. [4] [26] [27]

The high gain of the op-amp forces the signal delivered from the feedback squaring-cell detector to become equal to the mean voltage of  $V_{IN}$  squared across the low-pass filter. As a consequence the voltage at the input of the feedback squaring cell has to be equal to the root of the mean squared value of  $V_{IN}$ . This results in an output that represents the RMS value of the input. Thus, in an implicit manner, the op-amp forces the detected output to be precisely the RMS value of the input signal.

When both squaring cells are identical, several benefits arise. First, scaling effects in these cells cancel; thus, the overall calibration may be accurate. Furthermore, the response of both cells is very similar over temperature, leading to excellent temperature stability.

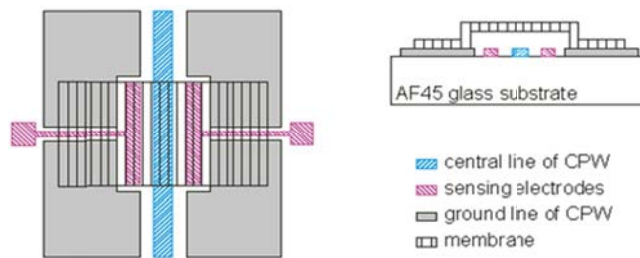


**Figure 1.13** RMS responding detector with a linear-in-dB characteristic

An evolution on this theme shown in Figure 1.13. inserts a linear-in-dB variable gain amplifier (VGA) ahead of the front-end detector. [4] [28] “A second detector is driven with a reference voltage. An AGC loop is formed that adjusts the VGA gain until the detected output is equal to the reference detector output through an integrator. The RMS measure of the detected signal level is captured in the VGA gain control voltage, which is made to scale linear-in-dB.” [4]

The linear-in-dB response is very useful for measuring RF power as will become clear when we discuss the log detector in Section 1.2.3. “As the input signal level varies, the AGC loop adjusts the VGA gain so as to keep the detector input at fixed level. Now the detector only copes with the signal peaks, and not its dynamic range.” [4]

In literature a new approach found is a power sensor for RF signals, based on capacitive detection. [29] The power measurement is based on the movement detection of a grounded membrane suspended above a planar transmission line where the signal is travelling, as can be seen in Figure 1.14. The movement of the grounded membrane is measured capacitively.

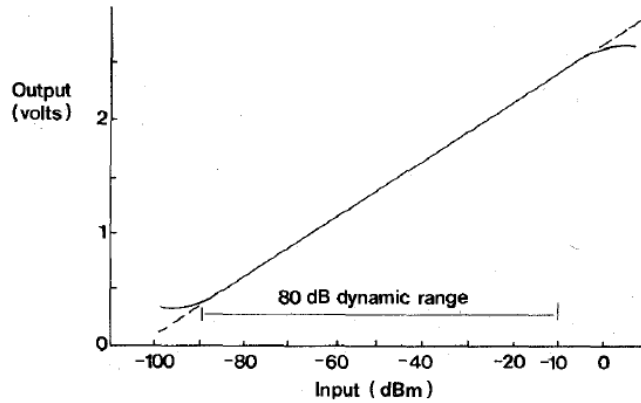


**Figure 1.14** RF Power sensor based on capacitive detection

### 1.7.3 Logarithmic Detector

For applications that have to measure very low level RF signals, a high dynamic range detector with high sensitivity is necessary. A type of detector that can meet those requirements is the so-called successive detection logarithmic amplifier or in short log detector [30]. Compared to diode detectors, a well-designed log detector can have a much higher input dynamic range. Log detectors have superior sensitivity to measure low-level RF input signals and can operate over wide frequency range, with the top end reaching several GHz.

A log detector has a linear relationship between the RF input power in dBm and the output voltage, as shown in Figure 1.15. As shown by this figure, the output voltage changes in a linear-in-dB (mV/ dB) fashion when the input power increases.



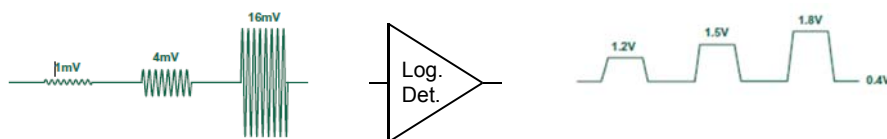
**Figure 1.15** Log Detector input/output transfer [31]

This linear in dB response makes this detector very useful for measuring RF power levels in communications systems, because most communication standards specify transmit power levels in dBm, as was already mentioned in Section 1.3

Actually a log detector itself does not respond to power levels, but to the voltage applied to its input. The reason that the input level can be stated as equivalent power, in dBm, is because the input power level is inferred from a measurement of the RMS voltage across the input impedance of the detector. As a consequence the input impedance has to be known. For example, with the use of Equation (1.2), we can see that for an input impedance of  $50\Omega$ , 0 dBm (1mW) corresponds to a sinusoidal amplitude of 316.2 mV (223.6 mV RMS).

When we look at the input/output transfer as was shown in Figure 1.15, we can see that the essential purpose of a log detector is to compress signals of wide dynamic range to its decibel equivalent. When the input/output transfer of the log detector is fixed we can actually say it's a measurement device, which expresses the AC amplitude of the input signal in the logarithmic domain.

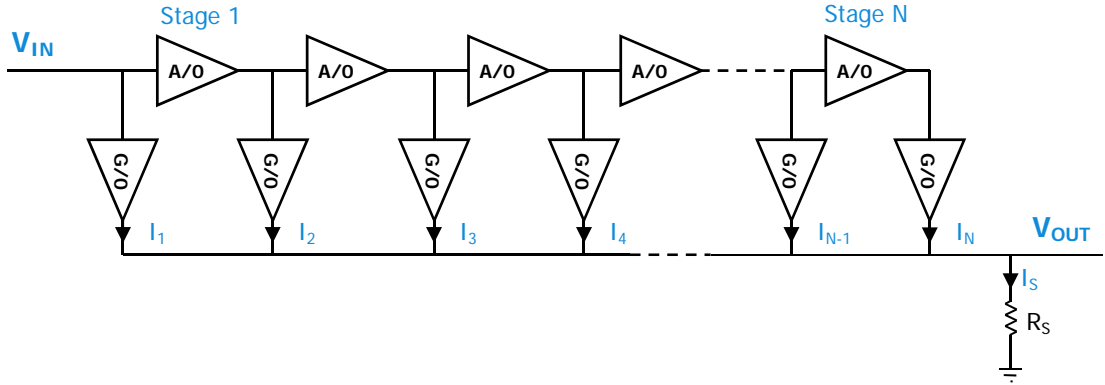
An advantage of the logarithmic detection compared to square-law detection is that large changes in input-signal voltages can be represented by relative small changes in detector output voltages, as is shown in Figure 1.16.



**Figure 1.16** Input burst and their associated log output [32]

The operation of log detectors does not depend on the nonlinearity of a semiconductor device, like diode detectors. To achieve the desired logarithmic conversion, most high speed high dynamic range detectors use the combined outputs of a cascade of low-gain high-frequency nonlinear limiting gain stages, so-called A/O cells, to approximate the logarithmic transfer function [33]. Figure 1.17 shows a simplified architecture of a so-called successive approximation log detector. Actually, in literature more names are used for this type of structure. Progressive

compression log-amp, demodulating log amp and successive compression logarithmic amplifier are some examples of names, which are used in literature. From now on we will use the name successive detection logarithmic amplifier or simply log detector.



**Figure 1.17** Simplified architecture of a successive approximation logarithmic detector

With the structure as shown in Figure 1.17, the input signal of the detector is subjected through a process of progressive compression, which leads to an approximation of the logarithmic transfer in a piecewise linear manner.

The operation of this system can be explained as follows:

As the amplitude of the input signal,  $V_{IN}$ , is increased, each of the A/O stages goes into compression. This compression starts at the output stage and progresses toward the input stage. The detectors stages, so-called G/O stages that are connected to the outputs of the A/O stages and at the input of the first A/O stage, produce currents that are proportional to the signal voltages at these points. These currents,  $I_1, I_2, \dots, I_N$ , are summed simply by connecting the outputs of all the G/O stages in parallel. The sum of these output currents,  $I_S$ , is logarithmically related to the input signal's magnitude, which is converted back to voltage by using resistor  $R_S$ .

As was already mentioned, the architecture of the successive detection logarithmic amplifier used in this example is actually a simplified architecture. This architecture will only work for a quasi-DC input voltage. Practical RF power detectors convert an AC input signal into a pulsed DC output as was shown in Figure 1.16. To include this functionality in the system, most commonly full-wave rectification of the signals  $I_1, I_2, \dots, I_N$  is applied. To implement the rectification function, the G/O stages are modified such that they will output the absolute value of their AC input voltage. The output current is now a strictly positive current which is still fluctuating. Low-pass filtering is then used to remove the ripple of the rectified signal at the output. The RC time constant of this filter determines the maximum rise time of the output. More in-depth information about the operation of this log detector can be found in Chapter 2 of this report.

The high gain needed to achieve operation down to low signal levels is distributed over the cascade of low-gain stages. The individual gain stages are set at low gain, typically between 6 and 12 dB, to achieve a high small-signal bandwidth. As a consequence, the overall bandwidth can be very high. As a result of the high overall gain and high overall bandwidth, the gain bandwidth product (GBW) of the cascade architecture can be much higher than that of a typical op amp. This very high GBW is essential for accurate operation under small signal conditions and at high frequencies.



The manufacturer can choose the dynamic range and dynamic performance of each stage to achieve a good compromise in overall performance; by using enough stages in the cascade, it is possible to build an architecture that achieves a dynamic range greater than 100 dB. The low end of this dynamic range is limited by the internally generated noise of the cascade. The cascaded amplification of this noise causes that the output stage is already near compression, even if there is no input signal applied to the first amplifier stage. The top end is limited due to voltage limitations.

A log detector can have a fast response time, but it is not difficult to see that it will have a slower response than the diode detector. While the diode detector only consists of one detector diode, the log detector described above is built by a cascade of limiting amplifiers. Because the signal has to pass through all  $N$  limiting amplifiers, the signal will suffer from a delay in each stage.

A successive approximation logarithmic detector is not RMS-responding. As we know from Section 1.1 this will mean that the output response of this detector will be waveform dependent. The waveform-dependence is a consequence of the internal peak detection mechanism and the averaging behaviour of the post-detection low-pass filter, as will be shown in more detail in Section 2.1. A different waveform will result in a vertical shift of the log detector's transfer function, which means the shift will not affect the logarithmic slope [26]. In Table 1.2 the output shift for several waveforms is represented as relative error in dB compared to the transfer function when using a DC input waveform.

**Table 1.2** *The relative horizontal shift in dB of the log detector's transfer for different signal waveforms*

<b>Input waveform</b>	<b>Peak or RMS</b>	<b>Error (relative to a DC input)</b>
Square Wave	Either	0.00dB
Sine Wave	Peak	-6.02dB
Sine Wave	RMS	-3.01dB
Triangular wave	Peak	-8.68dB
Triangular wave	RMS	-3.91dB
Gaussian Noise	RMS	-5.52dB

#### 1.7.4 Conclusion

In previous sections we have discussed the different detector types. From this discussion became clear that each detector type has its advantages and disadvantages. Table 1.3 shows an overview of these fundamental differences.

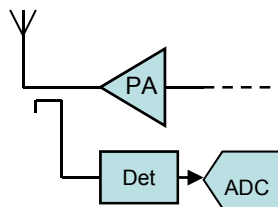
**Table 1.3** *Fundamental differences between power detector types [77]*

Fundamental differences between power detector types		
Diode Detector	Log Detector	RMS Detector
Detector output is proportional to RF envelope amplitude	Detector output is proportional to RF envelope amplitude in dB	Detector output is proportional to root-mean-square of RF signal power (in dB)
Small input dynamic range	Large input dynamic range	Large input dynamic range
Poor temperature stability without temperature compensation	Good to excellent temperature stability	Good to excellent temperature stability
Dependent on input signal wave shape and/or PAR	Dependent on input signal wave shape and/or PAR	Insensitive to input signal wave shape and/or PAR
Fastest responding	Relatively fast response time	RMS integrator slows response time

## 1.8 Applications

In the introduction it has already been stated that a power detector is used to monitor signals inside transceivers. [34] [35] In this section we will explain how detectors are applied to receivers and transmitters in more detail and give some other applications where detectors can be used.

### 1.8.1 Measuring of the output of a transmitter



**Figure 1.18** *Detector used for the power measurement at the output of a power amplifier*

Figure 1.18 shows a simple power measurement setup to measure the output of a power amplifier.

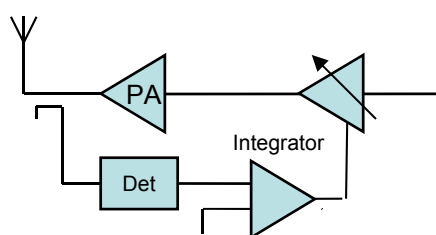
This configuration is used to monitor the power that is radiated from a radio antenna. Precise output power monitoring is important because the maximum emission of power may not exceed

officially prescribed limits, e.g., for the United States, levels specified in FCC (Federal Communications Commission) regulations.

For base stations inside a cellular network, minimizing transmit power is necessary to maintain the size of its cell to be precisely set to enhance coverage. This is necessary because otherwise interference will occur, which results when the same frequencies are reused in adjacent neighboring cells. Limiting the emission power will also ensure that the Power Amplifier (PA) will not transmit too much RF power or consumes an excessive amount of current which will damage the PA by overheating. Because the RF power detector lowers the uncertainty about the actual transmitted power the mechanical structure necessary to sink the heat of the RF power amplifier can be reduced. For example, if a 50W (47 dBm) power amplifier inside a base station has a transmit power uncertainty of just 1 dB, the amplifier must be dimensioned so that it can safely (i.e. without overheat) transmit 63 W (48 dBm) [11].

The operation of the system can be explained as follows:

A directional coupler is used to collect a part of the energy from the output line of the PA to the detector circuit, while having minimal effect on the original RF signal. The detected power is digitized by an analog to digital converter (ADC). Once the power measurement is available as a digital level, a decision is made based on the measured output power vs. desired output power.



**Figure 1.19** Dynamic power control

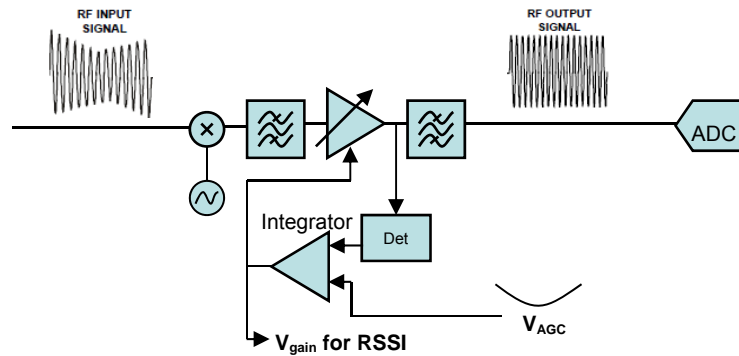
An alternative approach is dynamic control of the bias. Figure 1.19 shows a method for controlling transmitted power using a feedback control circuit. The power detector is incorporated within the control loop to control the output power within specified design limits over a wide range of conditions. This control system allows the amplifier to maintain the required bias condition for optimized performance, despite changes in voltage, temperature, and other environmental parameters. In other words, the feedback control eliminates the transfer function of the PA from the overall transfer.

The control loop must be stable under varying environmental conditions. Given the detector is part of the control loop, the output power level accuracy depends on the RF detector accuracy and stability. This dependency puts accuracy requirements on the RF detector. Because temperature plays an important role in introducing unwanted deviation in the output of detectors it's important that it is temperature compensated. Detector gain should also be stable over all operating conditions. As a side note, for dynamic control considerations, only a detector with relative small dynamic range, like a diode detector, is needed if the purpose is to fix the final output power level.

Now, let's examine how this circuit works: to begin with, the output power of the PA is detected using a directional coupler. The detected signal is measured by the log detector, which generates an output signal that is compared to a reference voltage. The difference between this measured

value and the reference voltage drives an error integrator. The output signal of the integrator drives the gain of the amplifier in front of the PA. The output power of the PA will impose the measured output from the log detector equals the reference voltage. The reference voltage can be used to set the output power at the required level.

### 1.8.2 Measuring of the input of a receiver



**Figure 1.20** Power detector used as part of automatic gain control to maintain a constant signal at ADC

At the receiver side, the strength of input signals appearing at the antenna can vary over a large dynamic range [31] [36] [3]. For this reason, receivers must be capable of processing signals of varying strength. The variation in signal strength is usually caused by movement of the source toward or away from the receiver, or by changes in weather conditions [37].

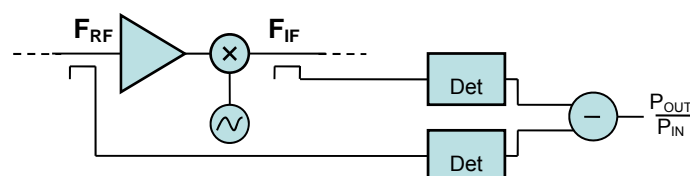
When the signal is too large it will overdrive the ADC input or waste valuable dynamic range when the input signal is too small. To get the highest possible signal-to-noise ratio (SNR) performance of the ADC, it is important to have a constant signal power level using the full dynamic range of the ADC [11]. In addition, a constant signal level makes it also more suitable for demodulation. [14] [38]

To obtain signal levelling in receivers, power detectors are used as part of automatic gain control (AGC) loop. An example of a receiver that uses a AGC loop to obtain a constant signal level is shown in Figure 1.20.

Power measurement in receivers is usually referred to as received signal strength indicator (RSSI). The RSSI signal typically is used to control the receiver-channel gain with an AGC or automatic level control (ALC) circuit to maintain a constant signal level.

As a side note; a typical receiver AGC requires 80 dB or higher gain control, so an RF detector with high dynamic range is needed.

### 1.8.3 Power gain calculation

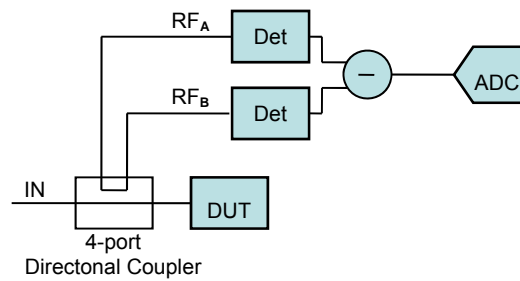


**Figure 1.21** Power gain calculation circuit

Power gain calculation is another possible application for logarithmic power detectors [14]. In theory the power gain is calculated by dividing the output power reading by the input power reading. Dividing is a difficult math operation to implement in analog circuits. Logarithmic power detectors can be used to simplify this implementation. When both output power reading and input reading are logarithmic quantities, the power gain of a circuit can be calculated by simply subtracting the input from the output reading. An example of such an implementation is shown in Figure 1.21

The operation of the system can be explained as follows: One directional coupler is used to provide a signal proportional to the RF input signal,  $F_{RF}$ , and a second coupler provides a signal proportional to the IF output signal,  $F_{IF}$ . The outputs of both RF log detectors are subtracted from each other.

### 1.8.4 Voltage standing-wave ratio measurement



**Figure 1.22** Voltage standing-wave ratio (VSWR) measurement.

Figure 1.22 shows a simplified configuration of a voltage standing-wave ratio (VSWR) measurement. The VSWR is a measure of impedance mismatch in a circuit [39]. For transmissions in RF systems it is important to have matched termination. Matched termination is achieved by proper characteristic impedance at transmitter and receiver side of a link. However, in wireless systems this is difficult to achieve. This is because, the surroundings of an antenna can change. This is the case, for example, in a cellular phone, which may or may not be next to a person's head during transmission. The surroundings of an antenna can have significant impact on the impedance seen at the antenna input port [40] and it's therefore difficult to ensure a constant optimum load towards the amplifier output. A large VSWR can cause many problems in RF circuits. For example, when there is no constant optimum load towards the amplifier output, a part of the transmitted power will be reflected and bounced back towards the power amplifier. This will lead to loss of transmitted power or in worse case the amplifier will be damaged. Furthermore, standing waves, which are a result of interaction between transmitted and reflected power, can attain unacceptable levels which will damage a transmission line. It is essential to protect the power amplifier from such problems. To detect these problems a Voltage Standing Wave Ratio (VSWR) measurement is used. Where VSWR is defined as the ratio of the maximum voltage divided by the minimum voltage at a certain point on the transmission line:

$$\Gamma = \frac{V_{REFLECTED}}{V_{FORWARD}} \quad (1.14)$$

Where  $\Gamma$  denotes the reflection coefficient.

In other words, the reflection coefficient is the reflected power level divided by the forward (transmitted) power level.

The operation of the configuration can be explained as follows: A directional coupler is used to separate the forward and reflected power waves on the transmission line between the PA and the antenna. One secondary output of the coupler provides a signal proportional to the forward power wave; the other secondary output provides a signal proportional to the reflected power wave. The outputs of both RF logarithmic detectors are subtracted from each other. As already mentioned before, subtracting two logarithmic quantities is equal to dividing.

## **1.9 Project definition**

The stability of the transfer of logarithmic power detectors is of critical importance. After a thorough investigation of the operation of the successive detection logarithmic amplifier, a new method was found that could be used to stabilize the Log transfer of the successive detection logarithmic amplifier (and possible other log devices) over important parameters like temperature, offset, part-to-part variation and frequency, which would normally alter the transfer. The method depends on a novel switching algorithm that is used to do continuous slope, intercept and dynamic range correction on the transfer of the successive detection logarithmic amplifier. When accurate enough, the method would make calibration of each individual device unnecessary. As this method seemed to be promising, we decided to do a feasibility study on this new method. For the feasibility of the implementation a step by step analysis has to be provided. After verification at system level the method has to be implemented and simulated at circuit level. The circuit simulations in the end should give an indication about the accuracy and usefulness of the method.

## **1.10 Outline**

### ***Chapter 2***

In this chapter the operation of a successive detection logarithmic amplifier is explained, followed by a theoretical description of the detector's operation. Furthermore a theoretical explanation of the important logarithmic detector transfer characteristics will be discussed

### ***Chapter 3***

This chapter is dedicated to a new slope and dynamic range fixation method used for the overall stabilization of the log transfer. First the operation of a method to fixate the so-called intercept of the log transfer is explained. This method that was invented by National Semiconductor [41] will be followed by a step by step explanation of the new slope and dynamic range fixation method. In same chapter a new dynamic range extension method will be introduced.

### ***Chapter 4***

Inside this chapter the new transfer stabilization method and dynamic range extension method is verified at system level. This verification will include system level simulations to show the viability of the proposed methods together with sensitivity calculations for non-idealities at the system when the system is implemented on circuit level. With the results of the calculation the most sensitive parts of the system will be indicated.

### ***Chapter 5***

The gathered knowledge about the sensitivity will be used for the implementation strategy discussed in Chapter 5. The content of this chapter will be dedicated to the circuit level implementation of the most critical system part, which will include some new topologies, used to realize the new transfer fixation method. Each circuit will be discussed in detail. To ease the understanding of its operation, some of these circuits will first be introduced by its system level implementation.

### ***Chapter 6***

Chapter 6 will discuss the circuit simulation results of the system which was treated in Chapter 5.

### ***Chapter 7***

Last chapter will be dedicated to the conclusions and recommendations about the results of the proposed fixation method will be discussed.



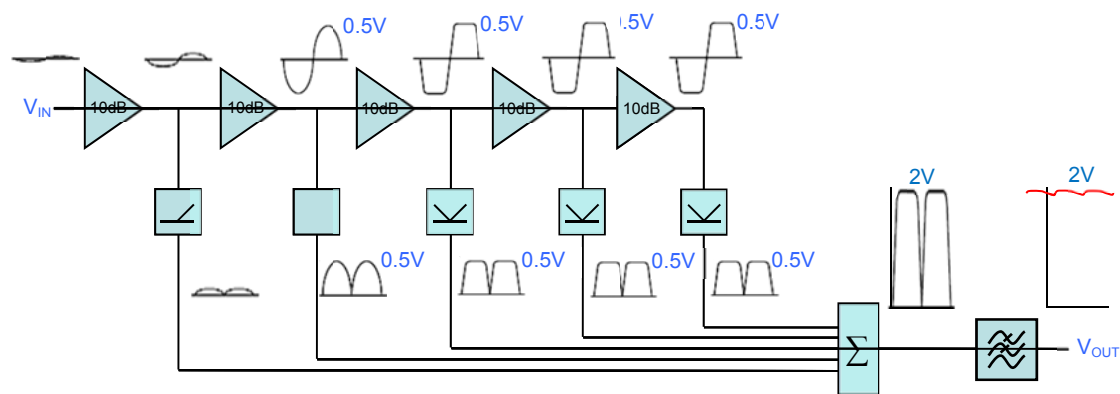


## 2 Successive Detection Logarithmic Amplifier

In Section 1.2.3 the structure and characteristics of the Successive Detection Logarithmic Amplifier have already been briefly described. This structure actually only worked for DC input values. In this chapter we will go into more detail on the operation of this type of log detector. Furthermore the definition of the so-called Log slope and intercept will be considered with a step by step mathematical analysis. Furthermore we will discuss the practical limitations of the detector. Before we try to understand the behaviour of the response of the successive approximation log detector mathematically, we first will look how the logarithm of the input signal is obtained by a simple practical example.

### 2.1 Operation of a Successive detection logarithmic amplifier

To get an understanding of how the logarithm of an RF input signal's envelope is constructed, the operation of the log detector will now be explained by a simple example [42]. For this explanation we will make use of the cascaded chain of 5 gain stages as shown in Figure 2.1. Each of these stages has a gain of 10 dB, corresponding to a factor of 3.16x, and have equal clipping or limiting output level. As shown in Figure 2.1 we assume a 0.5V<sub>peak</sub> clipping level in this example.



**Figure 2.1** Block Diagram of the Successive Detection Logarithmic Amplifier

When we apply a small sine wave voltage at the input of the Successive Detection Logarithmic Amplifier as shown in Figure 2.1, the signal will be amplified by 10 dB in the first stage and will be amplified by an additional 10 dB in each subsequent stage. As the signal grows when it travels through the cascade, it will at some point become so large that output of that stage will reach the 0.5V<sub>peak</sub> limiting level. In our example the signal has reached this critical level at the input of the 3rd stage, resulting in a clipped signal at the output of that stage. Because the output signal of this limiting stage is large enough to saturate its proceeding stage, all subsequent stages will also clip. As result we have 2 stages with a non-limited output signal and 3 stages with limited output signals. As shown in Figure 2.1 each of these output signals are fed into a full wave rectifier. The outputs of these rectifiers are summed together as shown, and the summer's output is applied to a low-pass filter to remove the ripple of the rectified signal.

As shown the full-wave rectifiers actually perform an absolute function on their input. As a result the output signal has twice the carrier frequency of the RF input signal. The higher frequency is an advantage, as it reduces the residual carrier feed-through at the output of the low-pass filter, yielding to a better recovery of the modulation components. This results in a steady state dc

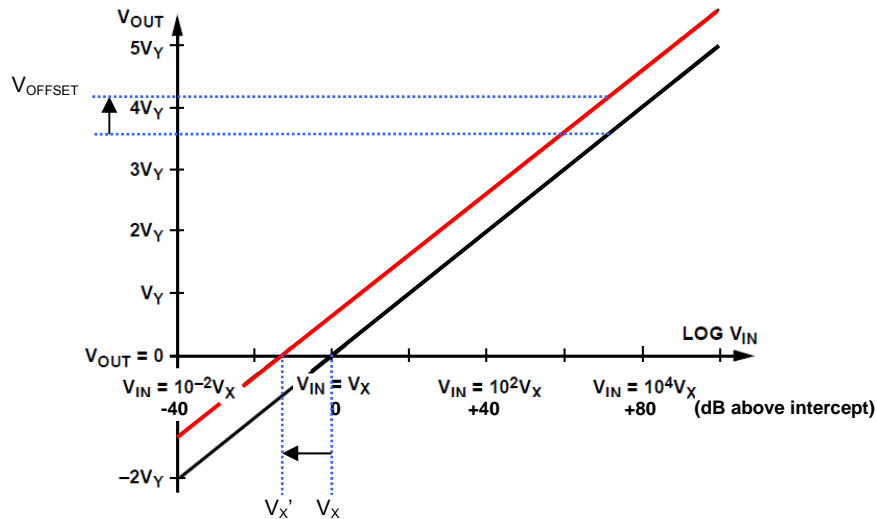
output voltage which represents the input envelope value of a particular steady-state AC input signal.

Till now we didn't show how the logarithmic response is developed. To show how the logarithm of the input signal's envelope is constructed, let's consider what happens if the input signal is reduced by 10dB. As shown in Figure 2.1, the unfiltered output of the summer is about 2 V<sub>peak</sub> (from 3 stages that are limiting and a fourth that is just about to limit.) If we reduce the input signal by a factor of 3.16, one less stage will be limiting. The voltage from this stage will reduce the output of the summer to approximately 1.5 V. If we reduce the input signal by a further 10 dB, the summer's output will drop to about 1 V. As the output is changing by 0.5 V for each 10 dB change at the input, we can state that the log detector is having a slope of 50 mV/dB. This finally shows the linear-in-dB response of a log detector.

In Section 1.2.3 we already noted the waveform dependence of the intercept of this type of detector. This waveform dependency is because of the internal peak voltage detection mechanism of the Successive Detection Logarithmic Amplifier and averaging behaviour of the post-detection low-pass filter.

## 2.2 The Ideal log detector transfer function

Figure 2.2 shows an idealized response of a logarithmic detector.  $V_{IN}$  is the input voltage and  $V_{OUT}$  is the output voltage.  $V_{IN}$  is represented along a logarithmic axis. It is shown that over a range of several decades, each ratio increase in  $V_{IN}$  causes a unit change of  $V_Y$  in the output  $V_{OUT}$ . As can be seen the ideal transfer is linear for logarithmic inputs, in which  $V_Y$  is the slope. At the value  $V_{IN}=V_X$  the output passes zero. This value  $V_X$  is called the intercept voltage. The intercept voltage is an important variable, since only by knowing the intercept voltage we can determine the actual input level [43]. The logarithmic function is valuable because it uniquely provides an output which changes by the same amount over any given ratio of input amplitudes. This makes the output easy to interpret.



**Figure 2.2** Idealized response of a logarithmic detector. Adding an offset voltage to the output will lower the effective intercept voltage.

In the usual case where all the variables are voltages, and regardless of the particular structure, the relationship between the variables can be expressed as

$$V_{OUT} = V_Y \log \left( \frac{V_{IN}}{V_X} \right) \quad (2.1)$$

Where  $V_{OUT}$  is the output voltage,  $V_Y$  is the slope voltage,  $V_{IN}$  is the input voltage and  $V_X$  is the intercept voltage.

The choice of logarithmic base is arbitrary. A change in base merely results in a change in slope voltage  $V_Y$ . When the logarithm is to base ten, that statement translates to ‘for each decade change in  $V_{IN}$ ’, so in that particular case  $V_Y$  has the meaning of ‘volts per decade’.

From Equation (2.1), we can see that all log detectors implicitly require two references, in this example,  $V_X$  and  $V_Y$ , to determine the scaling of the circuit. The absolute accuracy of a log detector cannot be any better than the accuracy of these two scaling references. A well-designed log detector has at least one high-accuracy DC reference source, from which both  $V_Y$  and  $V_X$  are ultimately derived.

We have to note that Equation (2.1) is mathematically incomplete in representing the behaviour of a successive detection logarithmic amplifier. However, the basic principles are unaffected, and this can be safely used as the starting point in the analyses of log detector scaling.

As can be seen, the idealized log detector function described by Equation (2.1) differs from that of a linear amplifier. When we calculating the gain by taking the derivative of equation (2.1) for the case where the logarithmic base is  $\delta$

$$\frac{\delta V_{OUT}}{\delta V_{IN}} = \frac{V_Y}{V_{IN}} \quad (2.2)$$

As shown the gain  $\delta V_{OUT}/\delta V_{IN}$  of the log detector is a very strong function of the instantaneous value of  $V_{IN}$ . The incremental gain is inversely proportional to the instantaneous value of the input voltage. This remains true for any logarithmic base, which is chosen as 10 for all decibel related purposes. [44]

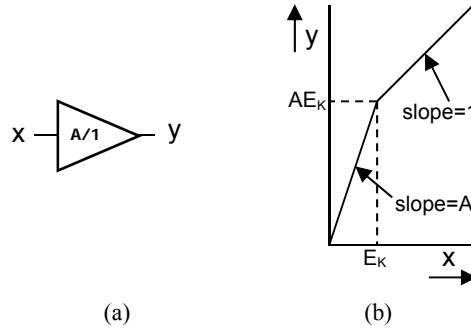
The highly nonlinear conversion of a log detector has some consequences which may be unexpected if the log transformation is not kept clearly in mind. While an attenuator inserted in front of a linear amplifier would change the ‘slope’ at the input, it would not affect the slope of the output of a log detector. Similarly, an offset voltage at the output of a linear amplifier has no relevance to the amplitude of an AC signal, while an offset added to the output of a log detector alters the apparent magnitude of its input

**Example [44]:** The red solid line in Figure 2.2 shows that the effect of adding an offset voltage,  $V_{OFFSET}$ , to the output is to lower the effective intercept voltage,  $V_X$ . Exactly the same change at the output can be achieved by raising the gain (or signal level) ahead of the log detector by the factor,  $V_{OFFSET}/V_Y$ . For example, if  $V_Y$  is 500 mV per decade (25 mV/dB), an offset of 150 mV added to the output appears to lower the intercept by two-tenths of a decade, or 6 dB. Adding an offset to the output is thus indistinguishable from applying an input level that is 6 dB higher.

## 2.3 Piecewise Linear Approximation of the LOG-function

The principle of successive approximation logarithmic detectors is to approximate a logarithmic transfer by a piece-wise linear function. To develop the theory, we first will consider a scheme slightly different from that employed in a typical successive approximation log detector, but simpler to explain and mathematically more straightforward to analyse. This approach is based on a nonlinear amplifier unit, called an A/1 cell [31]. Due to the design difficulties of A/1 cell, designers use a different type of amplifier stage, called A/0 gain stages. In a later section we will focus on the architecture of the detector built from A/0 stages.

### 2.3.1 Implementation with A/1 gain-cells



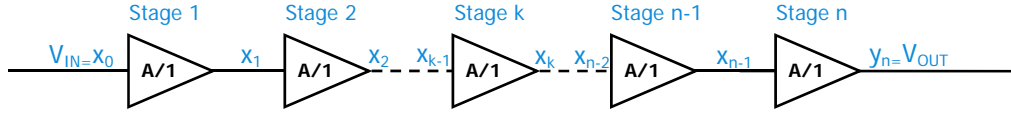
**Figure 2.3** (a) The symbol of the A/1 cell and (b) the transfer function of a A/1 cell.

The transfer characteristic of an A/1 cell is shown in Figure 2.3(b). As shown by this figure the local small signal gain  $\delta y/\delta x$  of an A/1 cell is  $A$ , and is maintained for all inputs up to the knee voltage  $E_K$ . Above  $E_K$  the incremental gain of an A/1 cell drops to unity. Actually the function of the A/1 cell is symmetrical: the same drop in gain occurs for instantaneous values of  $V_{IN}$  less than  $-E_K$ . So, the large signal gain has a value of  $A$  for inputs in the range  $-E_K \leq x \leq +E_K$ , but falls asymptotically toward unity for very large inputs.

$$y = -x + (1 - A)E_k \quad \text{for } x < -E_K \quad (2.3a)$$

$$y = Ax \quad \text{for } -E_K \leq x \leq E_K \quad (2.3b)$$

$$y = x + (A - 1)E_k \quad \text{for } x > E_K \quad (2.3c)$$



**Figure 2.4** An  $n$ -cell cascade built with  $A/1$  cells

Now we start to analyse the overall nonlinear behaviour of an  $n$ -stage cascade built with  $A/1$  cells, as is shown in Figure 2.4. When the signal travels through the cascade it will be amplified by  $A$  each time it passes a non-saturated gain cell. From this knowledge, it's not difficult to see that from all gain stages in the cascade, the  $n$ -th gain stage will experience the highest input value and will be the first that saturates. For a very low input signal at the cascade none of the  $n$  gain cells will saturate. In this situation all cells delivering a gain of  $A$ , resulting in an overall gain of  $A^n$ , which leads to an output voltage of  $V_{OUT} = A^n V_{IN}$ .

At a certain value of  $V_{IN}$ , the input to the  $n$ -th stage,  $X_{n-1}$ , is exactly equal to its knee voltage  $E_K$ . Using Equation (2.3b) the output voltage can be calculated to be  $V_{OUT} = AE_K$ .

Because there are  $n-1$  non-saturated cells with gain of  $A$  in front of  $n$ -th cell, the input voltage for which the  $n$ -th cell starts to saturate can be calculated as follows

$$V_{IN} = \frac{E_K}{A^{n-1}} \quad (2.4)$$

As the gain of the  $n$ -th cell drops to unity for signals higher than its knee voltage a transition of the overall gain from  $A^n$  to  $A^{n-1}$  will occur. Another transition in the overall gain will be reached as the input is increased further to a signal level for which input to the  $(n-1)$ -th stage exceeds its knee voltage, that is, when  $V_{IN} = E_K/A^{n-2}$ . More theoretically speaking we can say that the  $k$ -stage is the stage that starts to saturate when the input of this stage,  $X_{k-1}$ , reaches the value  $E_K$ . Because there are  $k-1$  stages of gain  $A$  in front of the  $k$ -th stage, the input value for which the  $k$ -stage saturates is,

$$V_{IN_k} = \frac{E_K}{A^{k-1}} \quad (2.5)$$

As the output of each stage is connected to the input of a proceeding stage we can calculate the overall transfer function of the complete system by substituting the transfer functions of the individual gain stages. Noting that we have a total of  $n$  stages, in which  $k$  stages are non-saturated and  $n-k$  stages that are saturated,

$$V_{OUT_k} = x_k + (n-k)(A-1)E_K = A^k V_{IN_k} + (n-k)(A-1)E_K \quad (2.6)$$

Combining Equation (2.6) and (2.5) simplifies (2.6) to

$$V_{OUT_k} = [(n-k+1)A + (k-n)]E_K \quad (2.7)$$

Equation (2.5) and (2.7) can be used to calculate the input and output value of the transition point when the  $k$ -th stage starts to saturate.

If we take a cascade of 4 gain stages ( $n=4$ ) it's not difficult to see that the transfer will be characterized by a total of 4 transitions. As already stated the last stage, in this case the 4th stage, is the first that reaches its  $E_K$  saturation level. Substitution of  $k = n = 4$  into Equation (2.5) and (2.7), leads to

$$V_{IN_1} = \frac{E_K}{A^{n-1}} = \frac{E_K}{A^3} \quad V_{OUT_1} = AE_K \quad (2.8)$$

When we further increase the input value a level will be reached for which the  $(n-1)$ -th stage starts to saturate.

Substitution of  $k = n - 1$  into Equation (2.5) and (2.7) leads to

$$V_{IN_2} = \frac{E_K}{A^{n-2}} = \frac{E_K}{A^2} \quad V_{OUT_2} = (2A-1)E_K \quad (2.9)$$

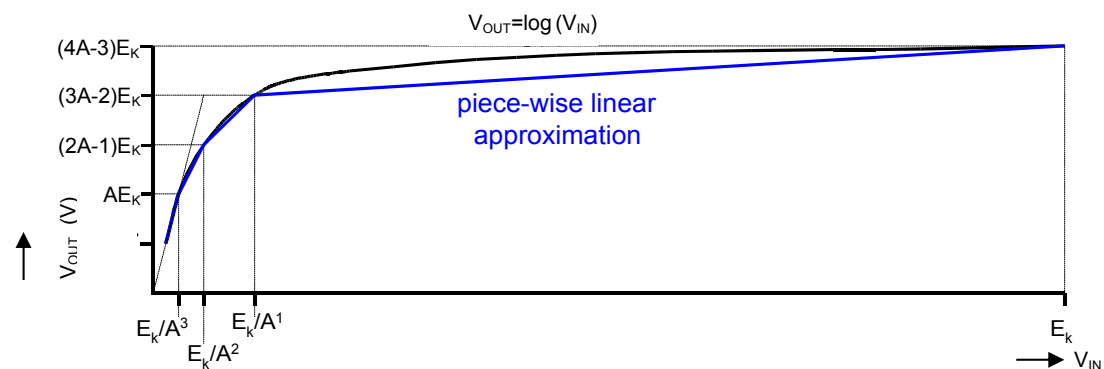
Continuing this line of reasoning, the next input and output of the transitions will be

$$V_{IN_3} = \frac{E_K}{A^{n-3}} = \frac{E_K}{A^1} \quad V_{OUT_3} = (3A-2)E_K \quad (2.10)$$

and,

$$V_{IN_4} = \frac{E_K}{A^{n-4}} = E_K \quad V_{OUT_4} = (4A-3)E_K \quad (2.11)$$

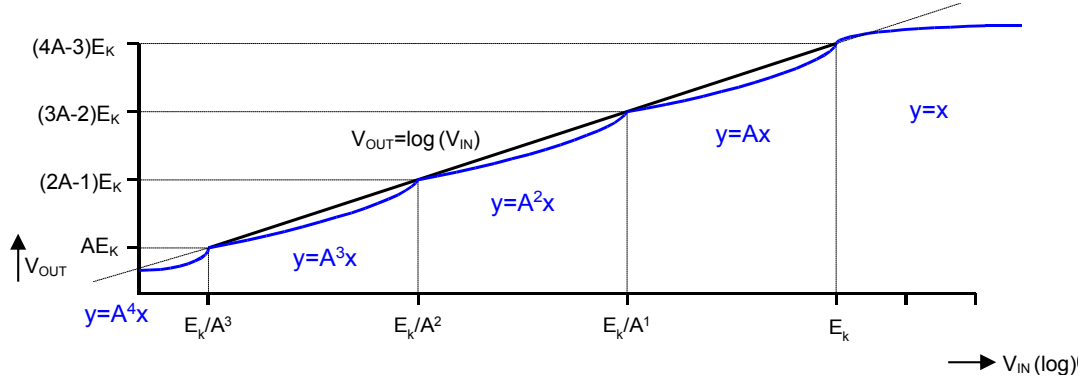
If we take these input values with corresponding output value of the transition points and interpolate linearly in between these points an piece-wise linear curve can be constructed as depicted in Figure 2.5 (blue line). From this figure it becomes clear that the piece-wise linear curve is an approximation of a logarithmic transfer where the transition points match the ideal log transfer (black curve).



**Figure 2.5** Piece-wise linear approximation of a logarithmic transfer

As shown in Figure 2.5 the gain of the logarithmic detector equals the slope of the various segments in the piece-wise linear curve. From Figure 2.5 and the previous analysis, it becomes clear that  $V_{OUT}$  changes by an amount  $(A-1)E_K$  for each ratio change of  $A$  in  $V_{IN}$ .

If we now represent  $V_{IN}$  along a logarithmic axis, the transitions occur at equal linear increments on that axis as shown in Figure 2.6. Represented along a logarithmic axis, the deviation of the device's piece-wise transfer function to the ideal log function becomes clearer. In later sections we will discuss this deviation, the so called conformance error, in more detail.



**Figure 2.6** Piece-wise linear approximation for logarithmic representation of  $V_{IN}$

When we discussed the ideal log detector transfer in Section 2.2 we already mentioned the importance of the intercept voltage  $V_X$  and slope voltage  $V_Y$ . To calculate the intercept voltage  $V_X$  and slope voltage  $V_Y$  of the piece-wise linear curve, we can simply use the values of the transition points, that are known to be matching the ideal log transfer.

If we use base 10 logarithms for the logarithmic axis, the ‘ratio change of  $A$ ’ can now be read as a ‘decade change’. We can therefore state that for a decade change of  $\log_{10}(A)$  in  $V_{IN}$ , the output voltage  $V_{OUT}$  will change with an amount of  $(A-1)E_K$ .

From this knowledge we can develop the slope function of the output, which is

$$V_Y = \frac{\text{linear change in } V_{OUT}}{\text{decades change in } V_{IN}} = \frac{(A-1)E_K}{\log_{10}(A)} \quad (2.12)$$

This shows that the slope voltage  $V_Y$ , which now can be read as ‘volt per decade’, depends only on the cell gain  $A$  and the knee voltage,  $E_K$ , while  $n$ , the number of stages, is unimportant.

To develop an equation for the intercept, we first need to substitute Equation (2.12) into Equation (2.1), which leads to

$$V_{OUT} = \frac{(A-1)E_K}{\log_{10}(A)} \log_{10}\left(\frac{V_{IN}}{V_X}\right) \quad (2.13)$$

As the output voltage  $V_{OUT}$  for corresponding  $V_{IN}$  is known at the transition points, we can take the  $V_{IN}$  and  $V_{OUT}$  at one of these  $n$  transition points to complete Equation (2.13)

Using the first transition point corresponding to  $V_{IN}=E_K/A^{n-1}$  and  $V_{OUT}=AE_K$ , results in

$$AE_K = \frac{(A-1)E_K}{\log_{10}(A)} \log_{10}\left(\frac{E_K}{V_X A^{n-1}}\right) \quad (2.14)$$

Solving for intercept voltage  $V_X$  leads to

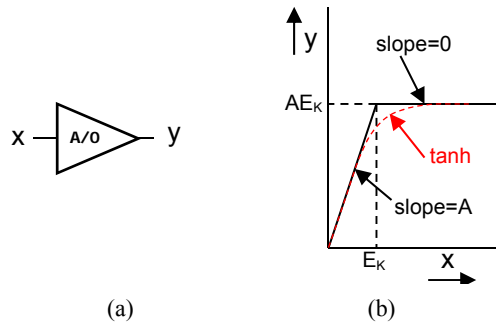
$$V_X = \frac{E_K}{A^{\left(n + \frac{1}{A-1}\right)}} \quad (2.15)$$

We have to be careful about the interpretation of this intercept voltage. In section 2.2 it was defined as the input voltage at which the output passes through zero (see Figure 2.2). Closer analysis, in Section 2.4.1, will show that the voltage given by Equation (2.15) actually represents the extrapolated, rather than actual, intercept.

### 2.3.2 Implementation with A/0 gain-cells

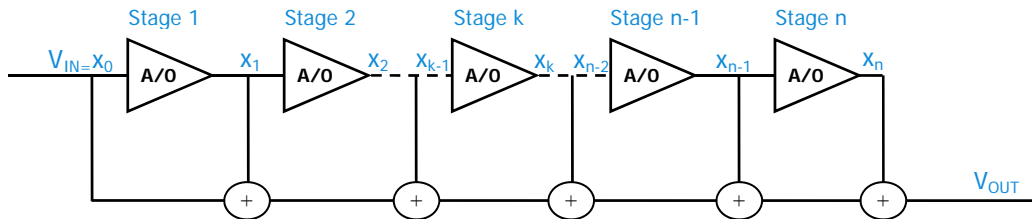
As noted earlier a typical successive approximation log detector is not constructed out of A/1 gain stages. Due to the design difficulties of these gain stages, designers use a different type of amplifier stage, called A/0 gain stages. Before we discuss the design difficulties, we will first focus on the architecture of the detector built out of A/0 stages.

The transfer function of the A/0 cell differs from that of an A/1 cell. Instead of falling to a gain of 1 above the knee voltage  $E_K$ , the gain of an A/0 cell falls to zero, as shown by the black solid line in Figure 2.7(b).



**Figure 2.7** (a) The symbol of the A/0 cell and (b) the transfer function of a A/0 cell.

When we replace the A/1 gain stages of the previous discussed log detector by A/0 gain stages, the output of the last stage can no longer provide the logarithmic output, as the output will be insensitive for all inputs at the cascade for which the input of the last stage is above its knee voltage. The logarithmic approximation is now developed by summing the outputs of all of the stages, as shown in Figure 2.8



**Figure 2.8** Logarithmic approximation by summing the outputs of all of the stages



As the input signal of each A/0 cell is added to its output signal a linear path with unity gain is created around the cell. As a result the transfer after each summation point becomes similar to the transfer of the A/1 gain stage. This results in a transfer that has a gain  $(A+1)$  below the knee-voltage,  $E_K$ , and unity gain above.

With the same procedure as for the A/1 log-detector, the slope voltage,  $V_Y$ , and intercept voltage,  $V_X$ , of this circuit can be found. Analogous to the A/1-based amplifier, the  $k$ -th gain stage in the chain saturates at an input signal level

$$V_{IN_k} = \frac{E_K}{A^{k-1}} \quad (2.16)$$

Noting that we have a total of  $n$  stages, in which ' $k$ ' stages are non-saturated and  $n-k$  stages are saturated, the log detector output signal at this level equals:

$$V_{OUT_k} = \sum_{i=0}^k A^i V_{IN_k} + (n-k)AE_K = \frac{A^{k+1}-1}{A-1}V_{IN_k} + (n-k)AE_K \quad (2.17)$$

Combining Equation (2.16) and (2.17) simplifies this equation to

$$V_{OUT_k} = \left[ \frac{A^{k+1}-1}{(A-1)A^{k-1}} + (n-k)A \right] E_K \quad (2.18)$$

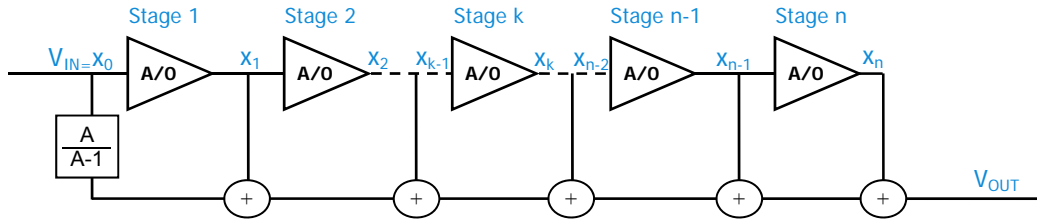
The slope and intercept are then found to be:

$$V_Y = \frac{V_{OUT_k} - V_{OUT_{k+1}}}{^{10}\log\left(\frac{V_{IN_{k+1}}}{V_{IN_k}}\right)} = \frac{(A - A^{-k})E_K}{^{10}\log(A)} \quad (2.19)$$

$$V_X \approx \frac{E_K}{A^{\frac{n+1}{A-1}}} \quad (2.20)$$

This implementation has one problem. When we look at Equation (2.19), we can see that the slope is dependent on the index ' $k$ '. As a consequence the slope voltage  $V_Y$  slightly reduces at the top-end of the range.

This problem can be solved by modification of the weighing coefficient of the signal bypass around the first A/0 gain stage, as depicted in Figure 2.9.



**Figure 2.9** Weighing coefficient of the signal bypass around first A/O stage for top-end correction of the dynamic range

With this modification, the log-slope and intercept can now be found to equal exactly:

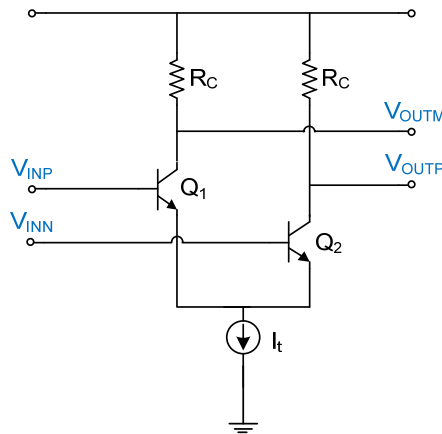
$$V_Y = \frac{V_{OUT_k} - V_{OUT_{k+1}}}{10 \log \left( \frac{V_{IN_{k+1}}}{V_{IN_k}} \right)} = \frac{AE_K}{10 \log(A)} \quad (2.21)$$

$$V_X = \frac{E_K}{A^{n + \frac{1}{A-1}}} \quad (2.22)$$

Equation (2.21) and (2.22) show that for a logarithmic amplifier based on A/O cells, both the slope voltage and the intercept voltage depend on the voltage  $E_K$ . As a consequence we cannot set the slope and intercept voltage separately by simply adjusting the voltage  $E_K$ . Furthermore the voltage  $E_K$  will be temperature dependent, as will be shown in next Subsection. To achieve the separation of the basic references used to determine  $V_Y$  and  $V_X$  the so-called G/O cells can be used. Before we will discuss the G/O cell we first will look at the circuit implementation of an A/O cell.

### 2.3.3 Circuit implementation of an A/O cell

At the beginning of Subsection 2.3.2 we noted the preference for the A/O style of log detector over one using A/1 cells. One of the considerations to choose for the A/O cell style is because the circuit of an A/O cell can be very simple. In its simplest form it can be constructed by a (bipolar transistor) differential pair, having resistive loads,  $R_C$ , and a tail current source,  $I_t$ , as shown in Figure 2.10



**Figure 2.10** Differential amplifier is used as A/O cell

For ideal transistors, the small-signal gain of this differential amplifier is

$$A = R_C I_t / 2V_T \quad (2.23)$$

And the peak differential output is

$$\pm V_{OUT\_max} = \pm R_C I_t \quad (2.24)$$

Substituting Equation (2.23) into Equation (2.24) results in

$$\pm V_{OUT\_max} = \pm 2V_T A \quad (2.25)$$

An amplifier with a gain of  $A$ , which limits at an output of  $2V_T A$ , leads to a knee voltage

$$E_K = 2V_T = 2 \frac{kT}{q} \quad (2.26)$$

It is well-known that the full form of the transfer function is

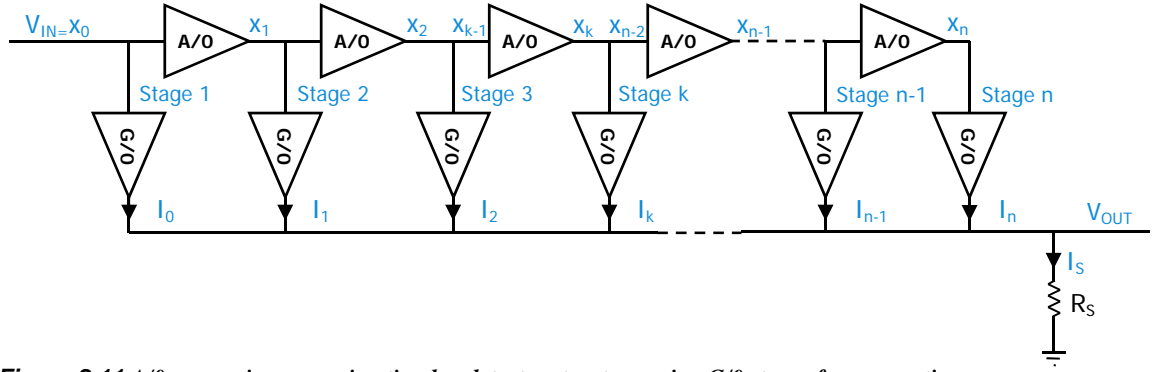
$$V_{OUTdiff} = R_C I_t \tanh\left(\frac{V_{INDiff}}{2V_T}\right) \quad (2.27)$$

This shows that the large signal transfer function is the hyperbolic tangent. As a consequence there will be a deviation from the ideal A/0 cell ( see red dashed line in Figure 2.7(b) ). This deviation is not detrimental for the operation of the log detector. In fact, the  $\tanh$  function is highly desirable as it results in a lower ripple in the logarithmic transfer than that obtained using an ideal A/0 function, as will be shown in Section 2.4.2 of this report. A less desirable property is that the transfer function is temperature dependent.

A valuable property of the differential structure is that these cells can be directly connected to one another without using coupling capacitors between the stages. Coupling capacitors, which typically have a chip area equal to that of a basic gain cell, can considerably increase die size and lower the bandwidth of the system. Because a successive approximation log detector composed of these cells is fully differential in structure it can be rendered very insensitive to disturbances on the supply lines and, with careful design, to temperature variations.

### 2.3.4 G/0 stages to decouple the slope calibration

From Equation (2.26) it is shown that the knee voltage  $E_K$  of A/0 stages, constructed with the transistor differential pair, is proportional to the absolute temperature. As in all the structures considered so far the knee voltage  $E_K$  is part of the slope equation, the slope will be sensitive to variation in temperature. This highly undesirable property can be solved with a simple modification. By adding a transconductance (G/0) stage at each node along the chain, as shown in Figure 2.11, complete control over the magnitude and temperature behaviour of the logarithmic slope becomes possible. This will become clear from the following analysis.



**Figure 2.11** A/0 successive approximation log detector structure using G/0 stages for summation

The transfer function of the G/0 stages is similar to that of the A/0 gain stages. For a G/0 stage the parameter corresponding to the gain  $A$  is now the transconductance  $G$ . A voltage input  $V_j$  at the input of a G/0 stage generates a current output,  $GV_j$  at its output. Furthermore, the maximum output current of a G/0 stage is  $GE_K$ , which is fully analogous to the maximum output voltage  $AE_K$  of the A/0 stage.

An advantage of the current mode output of the G/0 stages is that they can be summed by simply connecting the output of all stages together. The total current is converted back to a voltage by a transresistance stage or a simple load resistor to generate the logarithmic output, as shown in Figure 2.11.

The knee voltage,  $E_K$ , at which this G/0 abruptly drops to zero might differ from the corresponding voltage for the A/0 amplifier stage, but for the clarity of the mathematics the G/0 stages in this example have exactly the same knee voltage as the A/0 stages.

The analysis is very similar to that previously presented. The input to the last G/0 cell stage is the output from the  $n$ -th A/0 stage. Since this G/0 stage also has a knee at  $E_K$ , the first transition occurs at a system input  $V_{IN}$  which now is  $A$  times lower than in either of the two earlier log detector structures. The next transition occurs when the input to the  $n$ -th A/0 stage reaches its knee voltage, which is also the voltage at which the  $n$ -th G/0 stage reaches its knee voltage.

The system input for which the  $k$ -th stage reaches its knee voltage is:

$$V_{IN_k} = \frac{E_K}{A^k} \quad (2.28)$$

We have a total of  $n$  G/0 stages, in which ' $k$ ' stages are non-saturated and  $n-k$  stages are saturated. As the currents of these stages are summed and converted back to a voltage by a load resistor  $R_S$ , the output voltage at a saturation level can be calculated by:

$$V_{OUT_k} = R_S \left( \sum_{i=0}^k A^i V_{IN_k} G + (n-k)GE_K \right) = R_S \left( \frac{A^{k+1}-1}{A-1} V_{IN_k} G + (n-k)GE_K \right) \quad (2.29)$$

Substituting Equation (2.28) into Equation (2.29) leads to

$$V_{OUT_k} = R_s \left( \frac{A^{k+1} - 1}{A - 1} \frac{GE_K}{A^k} + (n - k)GE_K \right) \quad (2.30)$$

This can be simplified to

$$V_{OUT_k} = R_s GE_K \left( \frac{A^{k+1} - 1}{(A - 1)A^k} + (n - k) \right) \quad (2.31)$$

Equation (2.31) shows that the slope would have the same dependency on the index 'k' as was discussed earlier. A small adjustment to the transconductance of the first G/0 cell can be used to improve the linearity of the log transfer at the top-end of the range. With this modification, the slope voltage and intercept voltage can now be found to be equal exactly:

$$V_Y = \frac{R_s GE_K}{\log(A)} \quad (2.32)$$

$$V_X = \frac{E_K}{A^n + \frac{A}{(A - 1)}} \quad (2.33)$$

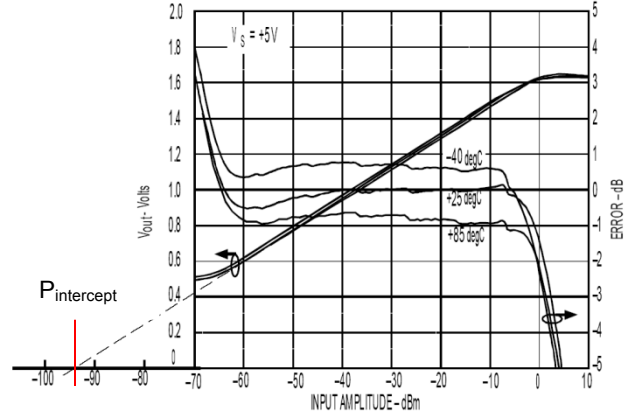
This shows that the intercept  $V_X$  remains traceable to the knee voltage of the A/0 and G/0 stages; while the slope voltage  $V_Y$  now depends on a decoupled peak current  $GE_K$  of the G/0 stages. Because the peak current  $GE_K$  can be controlled by the bias current of the G/0 cells, the slope voltage can be controlled through a proper choice of the bias current.

Instead of only performing summation, the G/0 stages can also be altered to implement the rectification function of the detectors as was discussed in Section 2.1. This will produce an output current independent of the sign of the voltage applied to the input of each stage, implementing the absolute value function. An example of an detector cell implementation of the G/0 cell and its operation can be found in Appendix B of this thesis report.

## 2.4 Important transfer function characteristics

### 2.4.1 Slope and Intercept

From previous sections we know that the log slope is the change in the output voltage per change in the input power. Figure 2.12 shows an example of a real log detector transfer. Over the linear operating range of this transfer, which is from about -65 dBm to about 0 dBm in this case, the output voltage changes by about 180 mV for a 10dB change at the input. Therefore we can state that the slope of this transfer function is 18mV/dB.



**Figure 2.12** Example of a practical log detector transfer [34] [42] [45]

At the end of subsection 2.3.1 we developed the equation to calculate the intercept voltage  $V_X$ . The intercept of an ideal log transfer, discussed in Section 2.2, was defined as the input for which the output is zero, knowing the ideal response is a straight line over infinite input range. This interpretation is not valid for non-ideal transfers, as is the case for a real life log detector. If we look at the non-ideal transfer in Figure 2.12, we can see that for input signals below about -65 dBm, the transfer begins to deviate from the straight line response. Therefore the early definition of the intercept cannot be used anymore. In our example, the intercept is the extrapolated point at which the transfer function would intersect the horizontal axis, if it were capable of doing so. With this knowledge, the intercept of the transfer shown in Figure 2.12, depicted by  $P_{intercept}$ , is about -94 dBm.

The curved response of the transfer at small signals is caused because of the following reasons. At the end of Section 2.2 we noted that the incremental gain was inversely proportional to the instantaneous value of the input voltage. For an ideal transfer this would mean that for an infinitely small input signal the gain of the log detector should be infinite. As infinite gain is not practically feasible this already shows why a deviation from the ideal transfer will happen. In practice the output of a log detector will never reach zero. Because of the very high gain, even with no input signal, a very small amount of thermal noise at the input of a log amp causes a finite output [46].

The slope of a log detector is determined by doing a simple two-point calibration [42]. For the two-point calibration the output voltage is measured for two known input levels that are within the linear operating range. The slope is simply,

$$slope = \frac{V_{OUT2} - V_{OUT1}}{P_{IN2} - P_{IN1}} \quad (2.34)$$

The intercept is given by the equation,

$$P_{intercept} = P_{IN1} - \frac{V_{OUT1}}{slope} \quad (2.35)$$

Once we know the slope and intercept of a particular device we can calculate the ideal output voltage of the log detector for any input level within the linear range using the simple equation,

$$V_{OUT\_ideal} = slope(P_{IN} - P_{intercept}) \quad (2.36)$$

If we take for example an input signal of -30dBm the ideal output voltage of the log detector will be equal to,

$$V_{OUT\_ideal} = 18mV / dB \cdot (-30dBm - (-94dBm)) = 1.15V$$

In a practical system we will be using the log detector to estimate an (unknown) input signal based upon the measured output voltage.

With the knowledge of Equation (2.36) we can develop the following equation to estimate the input signal power from the measured output voltage,

$$P_{est} = \left( \frac{V_{OUT\_measured}}{slope} \right) + P_{intercept} \quad (2.37)$$

## 2.4.2 Log-conformance error

The measuring quality of a logarithmic detector is referred to as the log linearity. It seems to be somewhat confusing to talk about linearity of a log, knowing it is actually a highly non-linear function. However, if we again represent the logarithmic input function along a logarithmic axis it immediately becomes clear where the name log linearity is coming from. When we talk about the log linearity of a log detector, we actually say that we are interested in the conformance of its transfer function to the ideal  $\log(x)$  mathematical function. More specifically, the Log Conformance error is a measure of how much the amplitude, in decibels, of the actual response of the log detector deviates from the ideal straight line response.

An example of a Log Conformance error measurement result is also shown in Figure 2.12. In this figure the Log Conformance at 3 different temperatures of the actual log detector over the full dynamic range are shown. From this figure it becomes clear that the actual response of the device under test shows some deviation from the ideal response and changes over temperature.

When  $P_{est}$  denotes the actual response and  $P_{IN}$  denotes the ideal straight response, the log conformance error can be calculated as follows:

$$E_{LCE} = P_{est} - P_{IN} \quad (2.38)$$

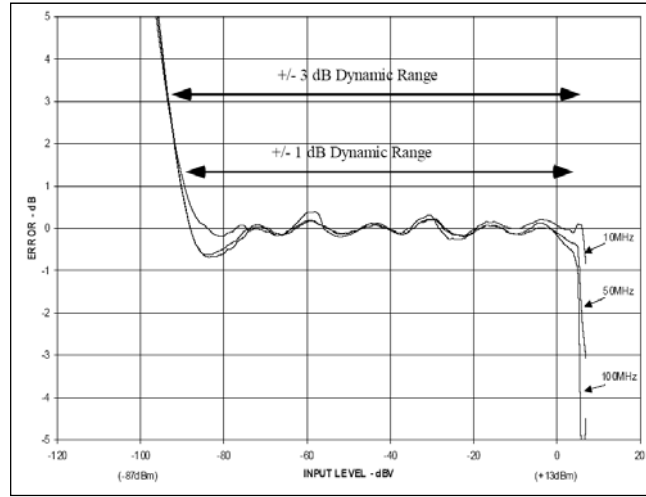
Substituting Equation (2.37) into Equation (2.38) we obtain

$$E_{LCE} = \frac{V_{OUT\_measured}}{slope} - (P_{IN} - P_{intercept}) \quad (2.39)$$

Substituting Equation (2.36) into Equation (2.39) yields

$$E_{LCE} = \frac{V_{OUT\_measured} - V_{OUT\_ideal}}{slope} \quad (2.40)$$

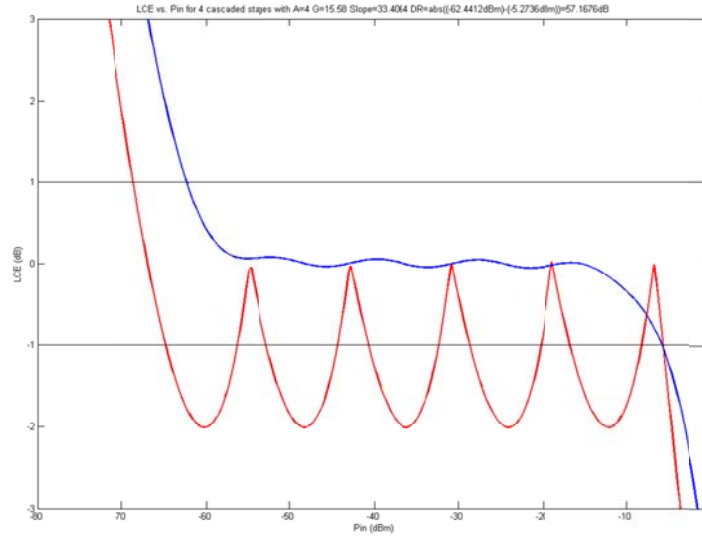
The conformance error curve serves to more closely examine the logarithmic detector's performance. It shows the range over which the device maintains its constant slope and also shows the ripple or any non-linearity over the input range. This range is called the dynamic range of the log detector. As the output of the log detector always exhibits some ripple over the range, the dynamic range is usually defined as the power range for which the log-conformance error is smaller than a specified error band for which the deviation from the  $\log(x)$  function is still acceptable. For the industry, a log linearity of  $\pm 1.0$  dB is commonly used. In Figure 2.13 for example, the 1 dB dynamic range is approximately 95 dB.



**Figure 2.13** Log Conformance example shows a dynamic range of approximately 95 dB for a log linearity of  $\pm 1$  dB [4] [42]

In Section 2.3.1 we already talked about the deviation of the piece wise linear curve from the straight line of the ideal log curve, as was shown in Figure 2.5. The Log Conformance of a piece-wise linear curve for which the gain A of the A/0 cells is set to 4 is shown (red line) in Figure 2.14.





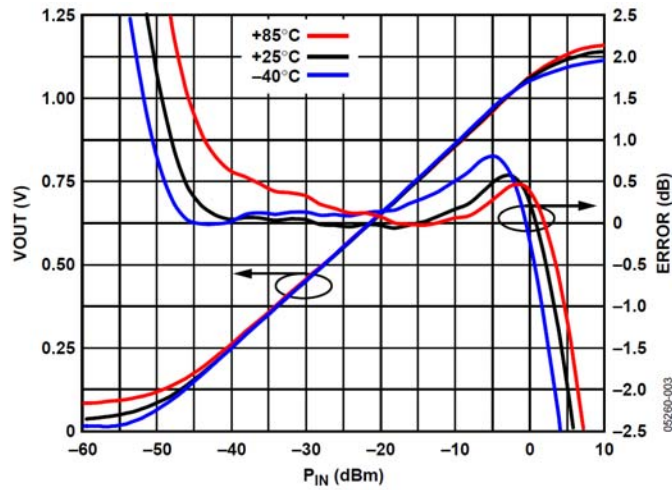
**Figure 2.14** Log conformance using A/0 cells (red curve) and tanh cells (blue curve)

The conformance error of the piece wise linear curve shows some equal parabolic ripples in between the transition points of the piece wise linear curve. The maximum deviation of these ripples occurs at the mid-point between the transitions. When the transition points are chosen equi-distant on a log-log scale, known to be a ratio change of  $A$ , a constant maximum conformance error over the full range of the approximation is obtained. So, the error expressed in decibels is dependent only on the stage gain  $A$ . As a result designers have the possibility to create a better approximation of the log by using more stages with less gain in cascade.

In Section 2.3.1 we also mentioned that using a log detector based on bipolar transistor differential pair amplifier cells is better than that using ideal A/0 cells. Where the ideal A/0 stages have abrupt gain transitions, the large signal transfer function of the bipolar transistor differential pair is a hyperbolic tangent ( $\tanh$ ). That the  $\tanh$  function is more desirable than the function obtained using an ideal A/0 function, is shown (blue line) in Figure 2.14. The log conformance shows that the ripple is much lower in amplitude and roughly sinusoidal in form, rather than a series of parabolic sections, as was the case for the implementation with A/0 cells.

The conformance error is not only used to examine the non-linearity of the transfer but it also serves to show the drift of the detector transfer function over various environmental conditions, most importantly temperature.

To show the effects of temperature on the detector transfer, the transfer at different temperatures is compared with an idealized transfer of the device at a known temperature. The most common temperature used for comparison is the room temperature  $25^\circ\text{C}$  [9] [47]. At this temperature, two known RF input signal strengths are chosen in the linear range of the detector, to find the slope and intercept characteristics of the response to form the simple linear equation, as was described in Section 2.4.1. This linear equation is then used to compare with the actual response of the logarithmic amplifier at different temperatures to generate the log conformance error curves.

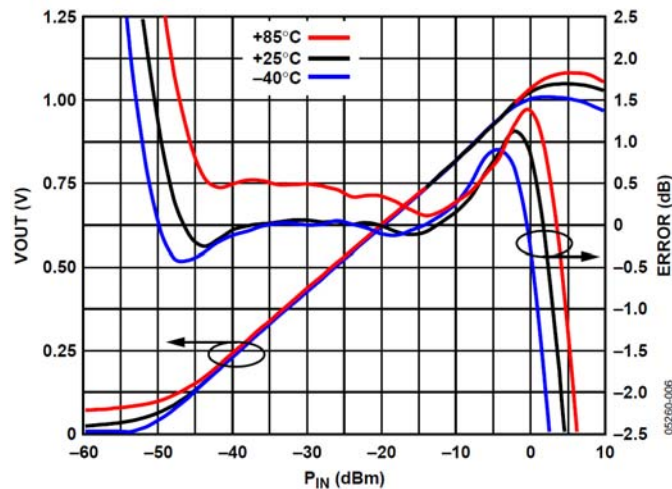


**Figure 2.15** Response of a logarithmic detector at a temperature of  $-40^{\circ}\text{C}$ ,  $25^{\circ}\text{C}$  and  $+85^{\circ}\text{C}$  [48]

Figure 2.15 shows the transfer function of a logarithmic detector at a temperature of  $-40^{\circ}\text{C}$ ,  $25^{\circ}\text{C}$  and  $+85^{\circ}\text{C}$ . Inside the same figure the logarithmic conformance error curves of each transfer is plotted.

As the linear equation was calculated from the transfer at  $25^{\circ}\text{C}$ , it speaks for itself that the conformance curve at  $25^{\circ}\text{C}$  shows the smallest deviation from the 0 dB error line. At the other temperature conditions the log conformance show some minor slope and intercept shifts. The figure shows that over temperature the log conformance error of this single device stays within  $\pm 0.5$  dB across the detection range of 0dBm till -40dBm. At a temperature of  $+85^{\circ}\text{C}$ , the transfer function will fall out of the detection range.

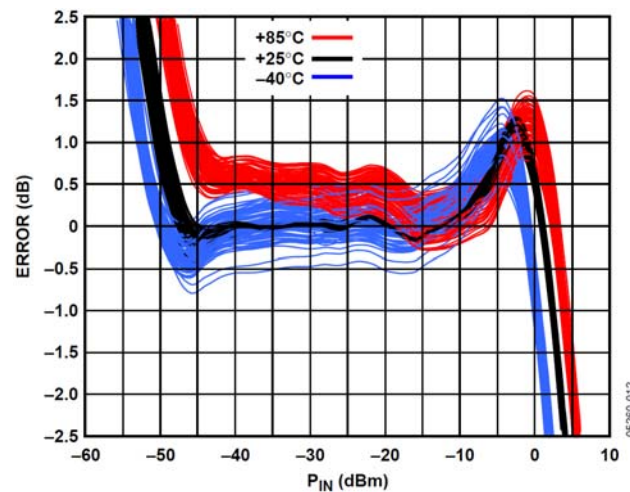
As was stated at the end of Section 1.2.3, the logarithmic slope is in principle, independent of the waveform. In practice, we have to note it usually falls off somewhat at higher frequencies as is shown in Figure 2.16. The cause of this effect can be found in the declining gain of the amplifier stages and some other effects in the detector cells at higher frequencies.



**Figure 2.16** Response of the logarithmic detector at a temperature of  $-40^{\circ}\text{C}$ ,  $25^{\circ}\text{C}$  and  $+85^{\circ}\text{C}$  at higher frequency input signal [48]

Because of temperature compensation techniques used in log detectors individual devices may have high accuracy over temperature; however, minor part-to-part variations inherent in semiconductor processing can be an obstacle to precise RF power management.

The log conformance error caused by part-to-part variations can be greatly reduced by means of calibration of each device, i.e. if the slope and intercept are determined for each individual detector device (at room temperature). Figure 2.17 shows the distribution of logarithmic conformance error curves of 80 individually calibrated log detectors. The sampling of log detectors spans various lots to demonstrate process variations. Although there is a clear variation from part to part, the distribution is very tight.



**Figure 2.17** Distribution of logarithmic conformance error curves of 80 individually calibrated log detectors. [48]



### 3 Stabilizing the Log Detector Transfer

In Section 2.2 we noted that the accuracy of a logarithmic amplifier transfer relies on the accuracy of the parameters  $V_X$  (intercept voltage) and  $V_Y$  (slope voltage). As shown in Section 2.3.3, the derived equations for  $V_X$  and  $V_Y$  are both depending on knee voltage  $E_K$ . When we consider A/0 stages implemented by a differential pair Equation (2.26) showed us that  $E_K$  is temperature dependent. As a result  $V_X$  and  $V_Y$  will be PTAT (Proportional to Absolute Temperature). For accurate operation of the log detector it is important to stabilize this temperature dependency. Different approaches for stabilizing the intercept voltage and the slope of the transfer over temperature have been proposed in the past [49] [50].

In Section 2.3.3 it was shown that by the addition of the G/0 cells at the output of each A/0 cell (shown in Figure 2.11) we created a possibility to control the slope voltage  $V_Y$  through the choice of an appropriate bias current for those G/0 cells. Because the bias current sets the peak current  $GE_K$  of the G/0 stages, the PTAT dependency of the peak current  $GE_K$  can be corrected by controlling the transconductance  $G$  with a PTAT bias current. So the addition of G/0 cells not only opened the possibility to set the transfer's slope at the wanted position but also makes it possible to correct for temperature.

The intercept voltage  $V_X$  is more difficult to stabilize over temperature. Different attempts have been made to stabilize  $V_X$ . One attempt was done by making  $V_{IN}$  PTAT [49].  $V_{IN}$  can be made to be PTAT by using a resistive divider with a PTAT transfer or an amplifier with a PTAT transfer. This method is capable of making the log conformance temperature independent, but the circuits used for this method also needed to cope with the full bandwidth of the circuit. Another method uses output compensation [51] [49], which relies on adding an offset voltage with the required temperature behaviour.

To observe that this is possible, consider that  $V_X$  can be expressed as

$$V_X = \left( \frac{T}{T_R} \right) V_{XR} \quad (3.1)$$

Where  $T$  is the actual temperature,  $T_R$  is the reference temperature at which  $V_X$  is specified and  $V_{XR}$  is the desired fixed intercept. Substituting (3.1) into (2.1) will give us

$$V_{OUT} = V_Y \log \left( \frac{V_{IN}}{V_{XR}} \right) - V_Y \log \left( \frac{T}{T_R} \right) \quad (3.2)$$

This shows that compensation can be achieved by adding at the output a voltage equal to the second term. This immediately shows the difficulty of this method, as it requires that the temperature behaviour of the correction voltage is dependent on  $\log(T/T_R)$ , and for accurate compensation the log-slope  $V_Y$  has to be accurately known. In practice, the log-slope is also subject to small part-to-part variations (and variations over other operating conditions such as temperature, frequency, etc.)

In Section 2.4.2 we showed the log conformance of a temperature compensated log detector exhibits still some error over temperature variations, and also an error caused by part to part variations, and frequency dependency. We mentioned that calibration of each device can minimize the error caused by part to part variations.

### 3.1 Intercept fixation algorithm

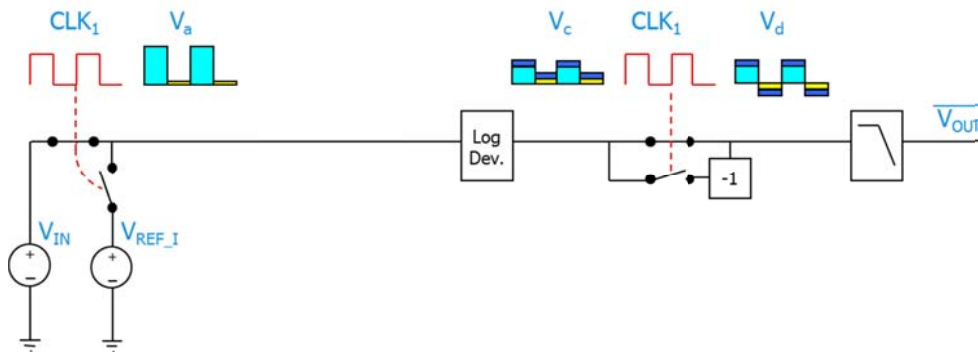
To reduce the error, affecting the intercept of the logarithmic device, a new compensation method [41] is used by the company ‘National Semiconductor’. This method requires no knowledge of the precise temperature behaviour of the intercept and can be used to compensate for all of the above described error contributions. As this method will be used in combination with the slope stabilization method, which will be discussed in following section, we first start to introduce the new intercept fixation method .

In the example at the end of Section 2.2 we showed that an offset voltage at the output or a gain error (deviation of the actual input signal level) ahead of the log detector, changes the effective intercept voltage. With this knowledge it’s not difficult to see, that errors which affect the intercept, can be modelled as either an output offset ( $V_{OS}$ ) or an input gain error ( $\delta$ ). As will become clear later in this section, the intercept fixation method to be described relies on the relationship between an input gain error and its corresponding offset error observed at the output. Because of this we will now find the relation between the output offset voltage and the input gain error.

By a simple modification of Equation (2.1), the input gain error can modelled as follows

$$V_{OUT} = V_Y \log\left(\frac{V_{IN}(1 + \delta)}{V_X}\right) \quad (3.3)$$

The first operation of the intercept fixation method is to switch the input of the logarithmic device between the actual input signal and an accurate and known reference voltage  $V_{REF\_I}$ , as visualized in Figure 3.1



**Figure 3.1** System of the intercept fixation method

Because of this switching the logarithmic device will experience two states at different time instants.

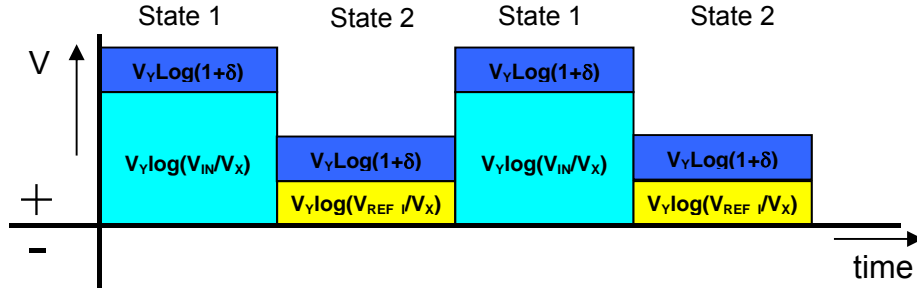
During State 1 the output of logarithmic device can be expressed as:

$$V_{OUT1} = V_Y \log\left(\frac{V_{IN}(1+\delta)}{V_X}\right) \quad (3.4)$$

And during State 2 the output can be expressed as

$$V_{OUT2} = V_Y \log\left(\frac{V_{REF\_I}(1+\delta)}{V_X}\right) \quad (3.5)$$

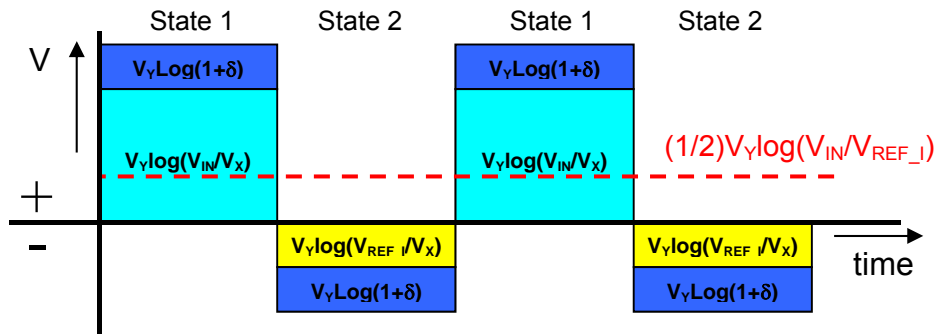
The signal after the switching operation is shown in Figure 3.2



**Figure 3.2** Signal  $V_c$  seen at output of logarithmic device

Using the logarithmic identity  $\log_b(AC) = \log_b(A) + \log_b(C)$  the gain error at both states can be written as a separate component  $V_Y \log(1+\delta)$  as is shown in Figure 3.2. As the input signals,  $V_{IN}$  and  $V_{REF\_I}$ , experience the same gain error at the input of the logarithmic device, both will have equal addition of  $V_Y \log(1+\delta)$  at the output. From this figure it can be seen that the gain error at the input translates to an output offset equal to  $V_Y \log(1+\delta)$ . Although the gain error  $\delta$  in the picture is visualized as a positive quantity it could also be negative.

The next operation of the method is to switch the polarity of the output signal of logarithmic device at the moment that the logarithmic device is receiving  $V_{REF\_I}$  at its input. This results in a signal which is graphically represented by Figure 3.3.



**Figure 3.3** Signal  $V_d$  seen at output of the inverting switch

Finally the last operation of the method is to produce the DC equivalent of this alternating signal. To produce the DC equivalent of the signal, the high-frequency components of the signal are removed by a low pass filter. The low-pass filter approximately averages the signal over each period, which can be simplified to the average of state 1 and state 2 of the signal.

To find the average, first state 1 and state 2 signals are summed:

$$V_{OUT} = V_Y \log\left(\frac{V_{IN}}{V_X}\right) + V_Y \log(1 + \delta) - V_Y \log\left(\frac{V_{REF\_I}}{V_X}\right) - V_Y \log(1 + \delta) \quad (3.6)$$

Because the  $V_Y \log(1 + \delta)$  components are opposite in sign, Equation (3.6) can be simplified to

$$V_{OUT} = V_Y \log\left(\frac{V_{IN}}{V_X}\right) - V_Y \log\left(\frac{V_{REF\_I}}{V_X}\right) = V_Y \log\left(\frac{V_{IN}}{V_{REF\_I}}\right) \quad (3.7)$$

Because the output signal at each state is available for only 50% of period time (with 50% duty cycle) the signal is divided in half as a result of the averaging process, leaving the output of low-pass filter to be:

$$\overline{V_{OUT}} = \frac{1}{2} V_Y \log\left(\frac{V_{IN}}{V_{REF\_I}}\right) \quad (3.8)$$

Equation (3.8) shows that the resulting output is completely independent of any input gain error ( $\delta$ ) or output offset. Furthermore, the device parameter dependent intercept voltage ( $V_X$ ) is eliminated from the transfer and replaced by the accurately known reference voltage  $V_{REF\_I}$ .

This method enables the correction of errors in logarithmic devices without the need to accurately reproduce and/or compensate individual error effects and requires no knowledge of the precise temperature and device dependence of the errors

## 3.2 Slope fixation

In this section we will introduce a new method that can be used to fixate the slope and intercept of a logarithmic device. The method is used to fixate the slope and intercept at an accurate and known value, without the need for manual calibration. This method would make it possible to have an identical transfer for each individual logarithmic device. The method relies on a continuous automatic calibration algorithm which makes the transfer insensitive to mismatches, temperature- and process variations. The method allows compensating for the frequency dependency of the input signal that it processes.

To explain the method we first have to look at Equation (2.34). This equation shows how to determine the slope of the transfer of a logarithmic device. For two known input values the corresponding output levels are measured. With the input and output values known the slope can be derived. The method to be described is related to this procedure. The basic principle of the

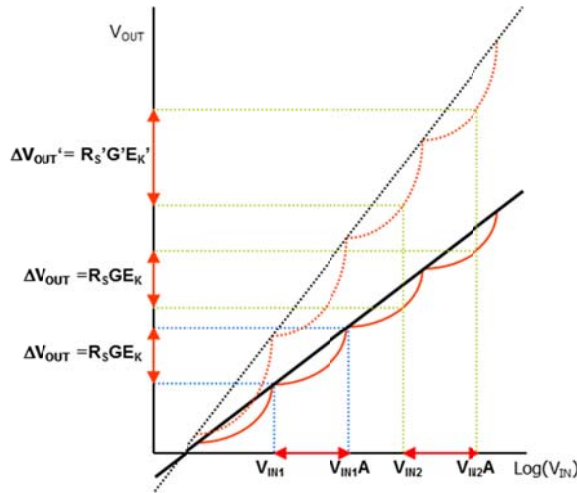


method is that it monitors the change at the output of the log device, from now to be called  $\Delta V_{OUT}$ , for an input signal which is changed with an accurately known and fixed multiplication factor.

Using Equation (2.34) we can write

$$\Delta V_{OUT} = V_{OUT2} - V_{OUT1} = \text{slope}(P_{IN1}\alpha - P_{IN1}) \quad (3.9)$$

By comparing the actual output change,  $\Delta V_{OUT}$ , with the expected value change, the correctness of the slope can be checked. Any deviation from the expected change means that the slope is not correct. With a control loop the deviation is corrected, leading to a slope which is continually corrected for non-idealities.



**Figure 3.4** The output change,  $\Delta V_{OUT}$ , in response to an accurately known input multiplication,  $A$ , depends on the slope of the transfer.

In Figure 3.4 the basic principle of the method is shown. To explain the operation of the method we first have to take an arbitrary input signal. Assume the input signal is,  $V_{IN1}$ , as is shown in Figure 3.4.

When we substitute Equation (2.32) into Equation (2.1) the output value for input signal  $V_{IN1}$  can be calculated as follows

$$V_{OUT} = \frac{R_S G E_K}{\log(A)} \log\left(\frac{V_{IN1}}{V_X}\right) \quad (3.10)$$

The next operation of the method is to multiply the input with a known multiplication factor. The multiplication factor used for this method is equal to the small signal gain of the A/O stages, known as  $A$ . When we multiply the input  $V_{IN1}$  with this factor  $A$  the output now will be,

$$V_{OUT} = \frac{R_S G E_K}{\log(A)} \log\left(\frac{V_{IN1} A}{V_X}\right) \quad (3.11)$$

The output change,  $\Delta V_{OUT}$ , in response to the input change  $V_{IN1}A - V_{IN1}$ , is the difference between Equation (3.11) and Equation (3.10)

$$\Delta V_{OUT} = \frac{R_S G E_K}{\log(A)} \left( \log \left( \frac{V_{IN1}A}{V_X} \right) - \log \left( \frac{V_{IN1}}{V_X} \right) \right) = R_S G E_K \quad (3.12)$$

The reason to choose for a factor equal to the small signal gain  $A$  is because it makes the method insensitive to the ripples in between the transition points of the transfer function. To see this, consider that we have  $V_{IN2}$ , shown in Figure 3.4, as our input signal. When we multiply  $V_{IN2}$  with a factor  $A$ , it happens to be that  $\Delta V_{OUT}$  is exactly same as it was for  $V_{IN1}$ , even when the real transfer (red solid line) at  $V_{IN2}$  deviates from the ideal transfer (black solid line). This shows that  $\Delta V_{OUT}$  is insensitive to the ripples of the real transfer.

From Equation (2.32) it is shown that the slope of the transfer was sensitive to the parameters  $R_S$ ,  $G$  and  $E_K$ . As we don't know the exact value of  $R_S$ ,  $G$ , and  $E_K$ , because of deviations caused by non-idealities, like process and/or temperature variations etc. deviations in  $R_S$ ,  $G$  and  $E_K$  cause the slope of the transfer to deviate from the expected slope.

The red dotted line in Figure 3.4 represents one example of a transfer that deviates from the expected transfer (red solid line). Now, if we use the same multiplication factor  $A$  for this deviated transfer,  $\Delta V_{OUT}$  will be bigger, as indicated by  $\Delta V_{OUT}'$  in Figure 3.4. Using Equation (3.12) and representing the deviated values of  $R_S$ ,  $G$  and  $E_K$  by respectively  $R_S'$ ,  $G'$  and  $E_K'$ ,  $\Delta V_{OUT}$  becomes equal to  $R_S' G' E_K'$ . In other words,  $\Delta V_{OUT}$  provides some useful information on the present slope of the transfer.

To show how the method uses this information to correct the slope, we first have to define a wanted slope and the gain of the individual A/O stages of the logarithmic device.

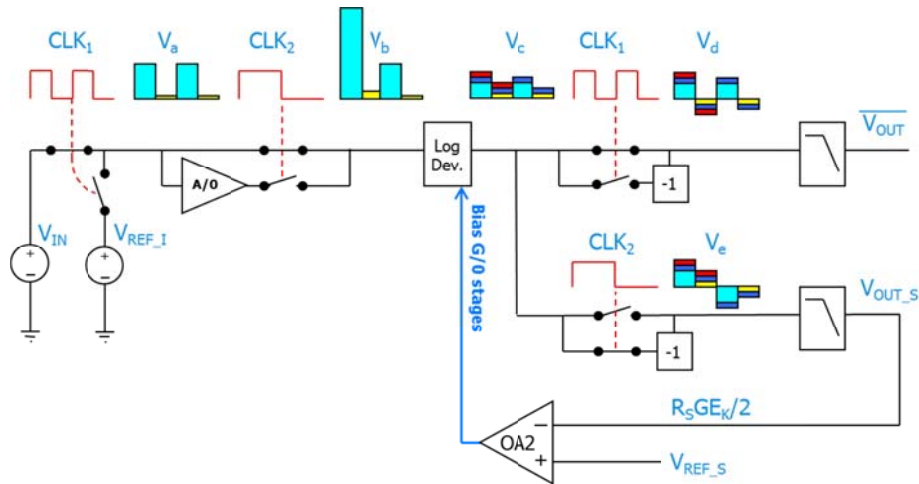
Let's assume we want to have a slope with a sensitivity of 40mV/dBm. As the gain of the A/O stages is limited by the needed bandwidth of the log device we for example have to use gain stages with a maximum gain of 3.16x or 10dB. As explained before, the method uses this gain also as its multiplication factor at the input. So, with a multiplication factor of 10dB, the expected output change,  $\Delta V_{OUT}$ , for a transfer with a 40mV/dB slope will be exactly 400 mV.

The idea of the correction method is to represent this expected output change by an accurate 400mV voltage reference and use it to compare it with the actual  $\Delta V_{OUT}$  measured at the output of the non-ideal log device. Any deviation from the 400mV voltage reference means a deviation from the required 40mV/dB slope.

At the beginning of Chapter 3 we showed the possibility to correct the slope over temperature by controlling the transconductance  $G$  of the G/O cells by PTAT current sources. The method proposed in this paragraph also corrects the slope by controlling the transconductance  $G$ , but now by means of a control loop which acts upon the deviation from the expected  $\Delta V_{OUT}$ . This results in a system which continually nullifies the overall error caused by deviation in  $R_S$ ,  $G$  and the temperature dependent parameter  $E_K$ .

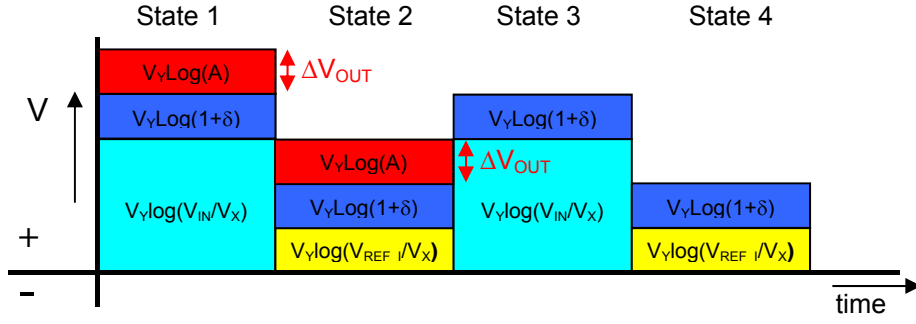
The explanation so far is a simplified version of the final operation of the method. At this moment we have not yet explained how to measure  $\Delta V_{OUT}$ . Furthermore, because the input signal is subjected to a multiplication of  $A$  the normal output readout of the log device will change during the multiplication.

A procedure to measure  $\Delta V_{OUT}$  at the output and at the same time restore the normal readout is found by combining the slope fixation method explained so far with the intercept fixation method that was explained in Section 3.1. The procedure is visualized in Figure 3.5.



**Figure 3.5** System including intercept and slope fixation method

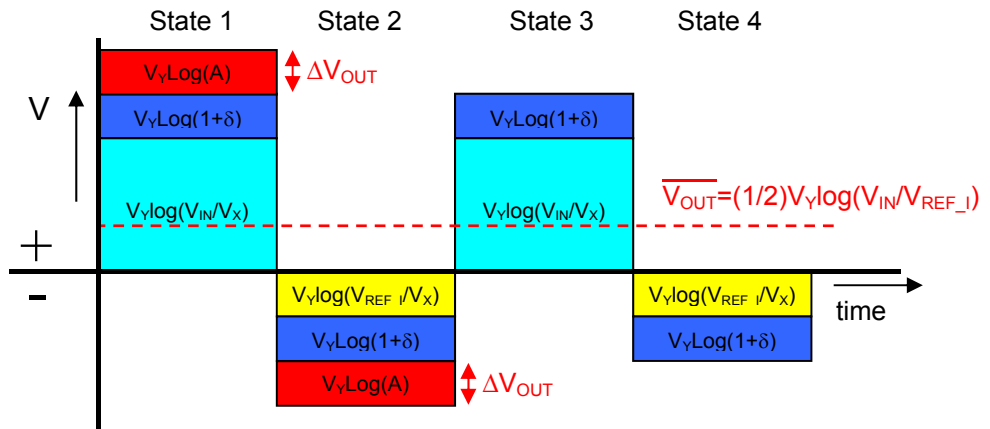
In Section 3.1 we showed that the intercept fixation method relies on switching the input of the logarithmic device between the actual input signal and an accurate and known reference voltage  $V_{REF\_I}$ . This led to the output signal at the output of the log device as was shown in Figure 3.2. Taking this figure in mind, we now start to explain how to combine the slope fixation and the intercept fixation method into an overall method, which is capable to continually calibrate the transfer's intercept, slope and dynamic range.



**Figure 3.6** Signal  $V_c$  seen at the output of the logarithmic device

As discussed in this section and shown by Equation (3.12) the slope fixation method relies on the multiplication of the actual input signal of the log device by a factor  $A$  and compare the output with the situation without the input multiplication. The same procedure can be integrated into the intercept fixation method by subsequently multiplying input signals  $V_{IN}$  and  $V_{REF\_I}$  by a factor  $A$ , as shown in Figure 3.5. With the knowledge gained from Section 3.1 it can be shown that this will result in a signal at the output of the log device which has an additional component  $V_Y \text{Log}(A)$  at State 1 and State 2 as graphical represented by the red blocks in Figure 3.6. As shown in this figure, the output will experience 4 states at different time periods. From this figure we can immediately see that the difference between State 1 and State 3 is equal to  $V_Y \text{Log}(A)$ . The same story holds for the difference between State 2 and State 4. As indicated by Figure 3.6 and shown by Equation (2.32) and Equation (3.12) the additional components  $V_Y \text{Log}(A)$  in the signal represents the  $\Delta V_{OUT}$  in which we are interested.

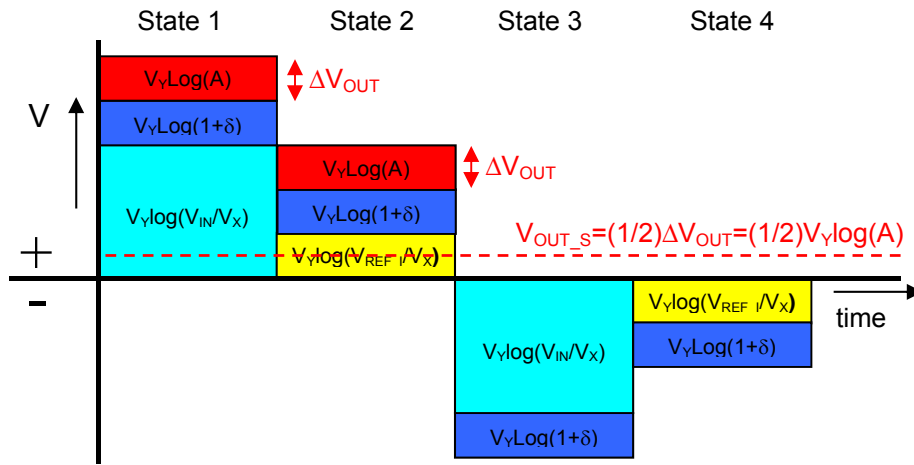
Before we will explain how  $\Delta V_{OUT}$  can be measured, we first show how the intercept method actually safeguard the multiplication factor modulation from the log readout,  $\overline{V_{OUT}}$ . As we know from the intercept fixation method, a switching device followed by a low-pass filter, is positioned at the output of the logarithmic device. Furthermore we know that the switching device is used to switch the polarity at the moment that the logarithmic device receives  $V_{REF\_I}$  at its input. If this same procedure is applied to the signal shown in Figure 3.6 the resulting signal will be as shown in Figure 3.7.



**Figure 3.7** Signal  $V_d$  seen at the output of the inverting switch

Looking at this figure, we can see that the two components  $V_Y \text{Log}(A)$  now have opposite sign. Here the beneficial property is becoming clear. When this signal passes through the low pass filter, the resulting output signal happens to be equal to the output as it was for the intercept fixation method. This shows that the readout becomes insensitive to the multiplication routine at the input. Furthermore the intercept fixated method is still working.

So, now we have an output which can be used for normal readout. But, what about  $\Delta V_{OUT}$ , in which we are also interested? To measure  $\Delta V_{OUT}$  we have to add an extra switching device and low pass filter to the output of the logarithmic device, as shown in Figure 3.5. The newly added switching device switches the polarity at the moment that the logarithmic device receives the input signals that are not modified by the multiplication factor. This results in a signal as shown in Figure 3.8.



**Figure 3.8** Signal  $V_e$  seen at the output of second inverting switch

As shown by this figure the  $V_Y \text{Log}(A)$  components represents the  $\Delta V_{OUT}$  as discussed earlier. Now, when we average this signal with the low pass filter, all pairs of equivalent components but with opposite polarity found at state 1 till 4 will cancel out. This results in an average signal which is defined by the two residual positive  $V_Y \text{Log}(A)$  components. As the period of the signal is equal to the time span of the 4 states, the resulting average signal at the output of the filter happens to be equal to

$$V_{OUT\_S} = \frac{2V_Y \log(A)}{4} = \frac{1}{2}V_Y \log(A) = \frac{1}{2}R_s G E_K \quad (3.13)$$

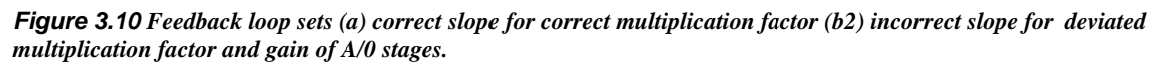
When we look at Equation (3.12), it can be seen that the voltage  $V_{OUT\_S}$  shown by Equation (3.13) actually represents the half of  $\Delta V_{OUT}$ . With this knowledge in mind and looking back at Figure 3.5 we can see that we have created two simultaneous outputs from the same measurement structure: the normal log read-out output  $\overline{V_{OUT}}$  and the voltage output  $V_{OUT\_S}$  which gives us information about the slope. Another important thing to note is that the use of the actual input  $V_{IN}$  for the two point measurement makes that the calibration can work continuously over time.

The next operation of the method is to compare the slope information voltage  $V_{OUT\_S}$  with a reference value  $V_{REF\_S}$  which represents the wanted slope information voltage. So, the next operation of the method is to control the transconductance of the G/0 stages, to nullify the

deviation between  $V_{OUT\_S}$  and  $V_{REF\_S}$ . This is accomplished by implementing the control loop as also shown in Figure 3.5. As can be seen, the loop is configured as a negative feedback loop. The difference between the actual output change,  $V_{OUT\_S}$ , and  $V_{REF\_S}$  drives a high gain error amplifier, OA2. The output signal of OA2 is used to bias the transconductance of the G/0 stages, localized inside the LOG-device. Figure 3.9 shows the configuration inside the log-device.

**Figure 3.9** *G/0 cells are biased with output signal of error amplifier OA2*

### 3.2.1 Fixing the multiplication factor

[illegible]

**Figure 3.11** Slope fixation system including the multiplication fixation system

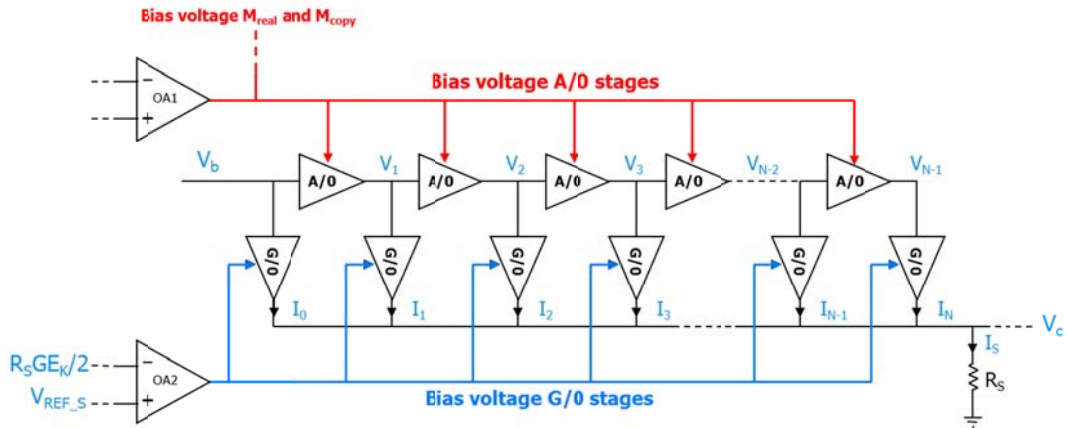
The operation of the procedure can be explained as follows. The input of the multiplication cell, which is in essence an A/0 cell, is sensed by the positive input of a high gain error amplifier, OA1. The output of the multiplication cell, followed by an accurate voltage divider, is sensed by

the negative input of OA1. The divider has an attenuation factor,  $B$ , which has to be equal to the required multiplication factor of the multiplication cell.

The output of OA1 controls the bias of the A/O cells including the multiplication cell. Due to the negative feedback configuration the bias is controlled such that the gain of the multiplication cell is forced to be exactly the attenuation factor  $B$ , which is the required multiplication factor. When we neglect the finite gain of OA1 and other non-idealities such as offset at the input of the multiplication cell, the accuracy of the procedure will depend only on the accuracy of the voltage divider block. In Section 4.3 we will discuss offset, which can influence the accuracy of the system as well.

The proposed multiplication fixation system shows an interesting feature. Because the signal path of the multiplication cell is measured, the control circuit is capable to compensate for variances in temperature changes but also over various frequencies of the signal the cell processes. Additional systems inside the multiplication cell, such as a level shifter or buffer, are also compensated when using this method. Of course we have to keep in mind that the extent to which this loop is able to compensate for these variances depends on the quality of the loop.

As shown in Figure 3.11, the bias voltage that is controlled by OA1 is also used to bias the A/O cells inside the log device. Here the use of an identical A/O cell for the multiplication cell becomes clear. Because we share the same bias for identical A/O cells we make sure the gain of the cells is equal to the multiplication factor. As we know from Section 3.2, this will make the method insensitive for the ripple of the transfer. The complete bias architecture for slope and gain (and dynamic range) control of the log device is shown in Figure 3.12.



**Figure 3.12** The complete biasing structure of the logarithmic device

As we explained in Section 1.2.3 the gain of the A/O cells defines the dynamic range of the log device. This system approach seems to have an extra beneficial property. With this system approach not only the multiplication cell can be fixed over frequency and temperature but also the gain of the other A/O cells. This implies that also the dynamic range of the system will be fixated.

There are several considerations when implementing the system for an AC input signal. Actually, the feedback topology as shown in Figure 3.12 will not work for an AC input signal. When looking to this figure we can see that the system will have positive feedback during negative input voltages. In other words, the bipolar RF input signal will change the sign of the control loop when it is negative. Furthermore, the error amplifier in this configuration has to be capable of





As result of the DC reference the error amplifier can now be optimized for DC operation. As high DC loop gain is much easier to realize, the quality of the loop can be much higher.

When we look at this architecture we can see that the divider block is now positioned in front of the multiplication cell instead of at the its output. The reason to put it in front of the multiplication cell is because DC reference  $V_{REF\_A}$  can now be  $B$  times higher than it was for the architecture depicted in Figure 3.11. As a result the input voltages of amplifier 0A1 will be  $B$  times higher than in the previous architecture, making it less sensitive to its input offset voltage. This method allows a  $B$  times higher  $V_{REF\_A}$ , without increasing the linearity error of the multiplication cell. Linear operation of the multiplication cell is important as will become clear in the following discussion

At the start of the discussion on the last architecture we mentioned the lower offset sensitivity as result of the higher and fixed DC input voltage, which was defined as  $V_{REF\_A}/B$ .

We have to note that in this configuration we still have to take the offset into account. This is because there is a limitation on the maximum voltage level the reference voltage,  $V_{REF\_A}$ , can have.  $V_{REF\_A}$  is limited because the copy of the multiplication cell,  $M_{copy}$ , has to operate in the linear range. This linear range is only valid at relatively small input signals, as will become clear later in this section. When the input signal of  $M_{copy}$  is too large the gain of  $M_{copy}$  will drop. As the control loop will compensate for this gain the small signal gain of the other A/O cells, including the multiplication cell  $M_{real}$ , will rise to a wrong value.

To get a clear understanding of the linear range of the multiplication cells we now will start to analyse the transfer of the A/O cells.

In Section 2.3.2 we discussed the implementation of practical A/O cells. From that section we learned that the large signal transfer function of an actual A/O cell is the hyperbolic tangent. Because of this hyperbolic tangent function, the real A/O cell does not have a linear transfer till it reaches its knee voltage  $E_K$ , as was the case for ideal A/O cells. Instead it already loses small signal operation for much lower input signals [53]. This can be shown by following analysis.

First we have to convert the output voltage in Equation 2.27 towards an output current, by neglecting the load resistors  $R_C$ :

$$I_{OUTdiff} = I_t \tanh\left(\frac{V_{INdiff}}{2V_T}\right) \quad (3.14)$$

The differential definition of the transconductance is:

$$g_m = \frac{dI_{OUTdiff}}{dV_{INdiff}} \quad (3.15)$$

Substituting Equation (3.14) into (3.15), we find:

$$g_m = \frac{I_t}{2V_T} \text{sech}^2 \left( \frac{V_{INdiff}}{2V_T} \right) \quad (3.16)$$

From Equation (3.16) it is shown that the transconductance of the differential pair is anything but constant, depending both on temperature and input voltage.

As  $V_{INdiff}$ , in our situation is actually the voltage defined by  $V_{REF\_A}/B$ , we can rewrite Equation (3.16) to

$$g_m = \frac{I_t}{2V_T} \text{sech}^2 \left( \frac{V_{REF\_A}}{B2V_T} \right) \quad (3.17)$$

The mathematical function,  $\text{sech}^2$ , of Equation (3.17) is a bell shaped curve that equals 1 at zero input, falling off rapidly at both sides and asymptotically approaches zero.

Because there is no linearity error for zero input we can use this as reference to calculate the linearity error for a particular input by the following equation

$$\mathcal{E}_{g_m} = \left( \frac{1}{\text{sech}^2 \left( \frac{V_{REF\_A}}{B2V_T} \right)} \right) - 1 \quad (3.18)$$

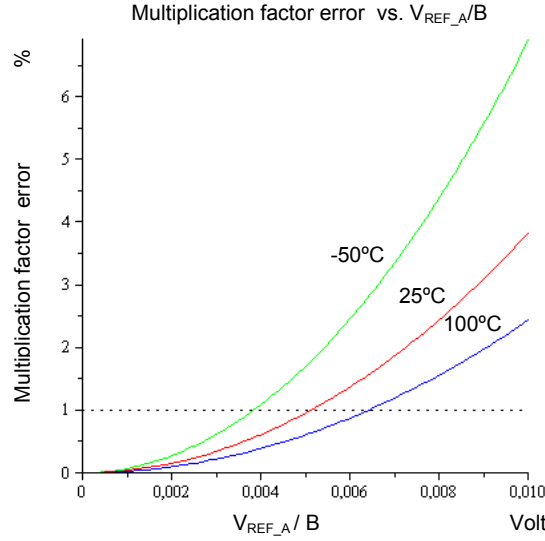
The small signal gain equation of the bipolar transistor differential pair shown in Figure 2.10 is

$$A_d = g_m \cdot R_C \quad (3.19)$$

As  $g_m$  is part of this equation, the small signal gain  $A_d$ , which is in our case the wanted multiplication factor, will have the same non-linearity behaviour as described by Equation (3.18)

$$\mathcal{E}_{mf} = \mathcal{E}_{g_m} \quad (3.20)$$

Therefore we can use Equation (3.18) to plot the error in the multiplication factor for different input values, as shown in Figure 3.14.



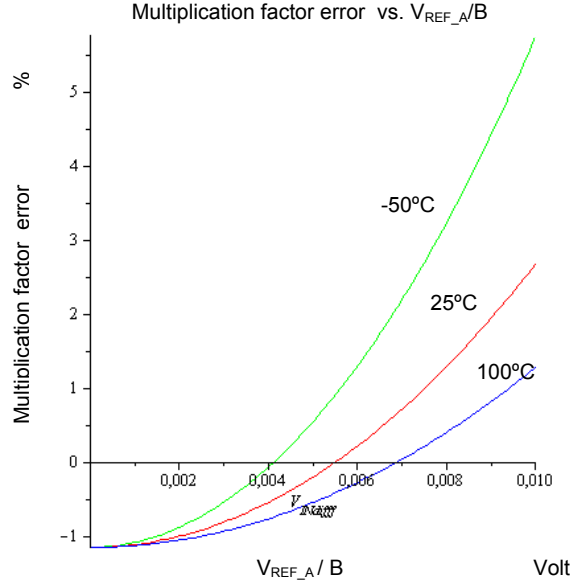
**Figure 3.14** The error in percentage of the multiplication factor vs. the normalized input voltage  $V_{REF\_A}/B$

To show the temperature dependency of the multiplication factor error we plotted in the same figure the non-linearity for the temperatures  $-50^{\circ}\text{C}$ ,  $25^{\circ}\text{C}$  and  $100^{\circ}\text{C}$ . From this we find for example that to keep the error below 1%, the differential input voltage defined by  $V_{REF\_A}/B$ , is limited to 5mV at  $25^{\circ}\text{C}$ , and is limited to approximately 3.75mV at  $-50^{\circ}\text{C}$ . Which means that reference voltage,  $V_{REF\_A}$ , is limited to a voltage level which is  $B$  times higher than those voltages. Where  $B$  is the attenuation factor, which is known to be equal to the wanted multiplication factor.

Figure 3.14 shows us that the input linear range of real implemented A/0 cells is much smaller than the knee voltage,  $E_K$ , of the differential pair, defined by Equation 2.26.

From the discussion above we can conclude that the value to choose for  $V_{REF\_A}$  depends on how much error we are willing to tolerate. The maximum error that can be tolerated is part of the discussion in Chapter 4.

Now that we know the error spread over temperature for a particular input voltage, we can use this knowledge to minimize the error in the multiplication factor by slightly modifying the attenuation factor  $B$  of the attenuation block. For example, when looking at the graphs at Figure 3.14, we can see that for a 5mV input signal the error in the multiplication factor will range from 0.6% at  $-50^{\circ}\text{C}$  to 1.7% at  $100^{\circ}\text{C}$ . Now, by making the attenuation factor  $B$  1.15% lower than the wanted multiplication factor  $(0.6\% + (1.7\% - 0.6\%)/2)$ , the error in the multiplication factor for a input voltage of 5mV will now be shifted to -0.55% at  $-50^{\circ}\text{C}$  and +0.55% at  $100^{\circ}\text{C}$ , as shown in Figure 3.15



**Figure 3.15** The error in percentage of the multiplication factor with correction of 1.15% in  $B$  vs. the normalized input voltage  $V_{REF\_A}/B$

This shows that the error at the temperature extremes for an input of 5mV is considerably lower than the situation without the modification of  $B$  and can be even zero for a temperature which is somewhere in the middle of the temperature range of -50 °C and 100 °C.

When we look at Figure 3.14 and 3.15 again, it can be derived that the operation of the multiplication cell is almost linear for an input signal  $V_{REF\_A}/B$  smaller than 1mV. So, why not using an input voltage which is lower than this level? As was already mentioned the input voltage level should not be too small because of the expected input offset levels of the amplifiers. In Chapter 5 it will become clear that we have to use an offset cancelation technique to lower the effective offset, such that we can lower the input voltage of the multiplication cell.

Because the control loop will be affected by the non-linear operation of the multiplication cell, we have to see how much this effect will disturb the slope fixation method. As we know now, for too large input signals, the multiplication factor starts to decrease. This will result in a smaller than expected slope information voltage  $V_{OUT\_S}$ .

The equation of the slope information voltage, including the non-linearity equation results in

$$V_{OUT\_S}' = \frac{1}{2} \frac{R_S G E_K}{\log(A)} \left( \log \left( \frac{V_{IN1} (A(1 - \varepsilon_{mf}))}{V_{REF\_I}} \right) - \log \left( \frac{V_{IN1}}{V_{REF\_I}} \right) \right) \quad (3.21)$$

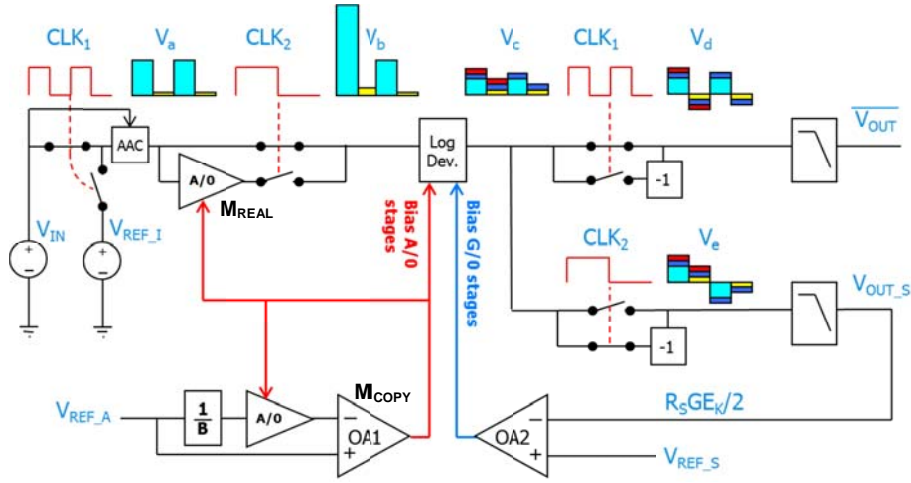
The percentage error in  $V_{OUT\_S}$  will be

$$\varepsilon_{V_{OUT\_S}} = \left( \frac{V_{OUT\_S}'}{V_{OUT\_S}} - 1 \right) \cdot 100\% = \left( \frac{\log(A(1 - \varepsilon_{mf}))}{\log(A)} - 1 \right) \cdot 100\% \quad (3.22)$$

Equation (3.22) shows us that an percentage error in the multiplication factor results in a fractional smaller percentage error in slope voltage compared with the multiplication error. This is a result of the logarithmic transfer. As previously discussed the error in the multiplication factor can be greatly reduced if we slightly alter value of the attenuation factor  $B$ .

### 3.2.2 Extending dynamic range

In this section we propose a simple extension to the slope and intercept fixation method which can be used to extend the dynamic range in a totally new approach which at the same time minimizes the problem of the large signal effect, which was discussed at the end of the previous section.



**Figure 3.16** Automatic Attenuating Control (AAC) circuit lowers large signal effect and extends the dynamic range of the logarithmic device

The idea is to put an Automatic Attenuating Control (AAC) circuit in-between the first switching device and the multiplication switching device as shown in Figure 3.16. This AAC circuit will be used to measure the input signal level,  $V_{IN}$ . When it measures an input level that would put the multiplication cell  $M_{real}$  in large signal range, it has to start attenuating the signal by a factor equally to the multiplication factor or a multiple of it. With this mechanism the input can be kept in the small signal range of  $M_{real}$ .

The first thought when we think about this mechanism is that it would influence the output  $\overline{V_{OUT}}$  and  $V_{OUT\_S}$  of our system. But if we take a closer look, it can be shown that the intercept fixation method is actually the one that makes that this mechanism can be used, without disturbance of the output  $\overline{V_{OUT}}$  and  $V_{OUT\_S}$ . As we know the intercept fixation method is actually removing the gain error at the input of the log device. As the attenuation can be seen as a gain error (gain below 0dB), it become clear why the attenuation method does not influence the output  $\overline{V_{OUT}}$ .

Using the calculation strategy as used in Section 3.1 it is shown that we can simply rewrite Equation (3.8) to

$$\overline{V_{OUT}} = \frac{1}{2} V_Y \log \left( \frac{\left( \frac{V_{IN}}{M} \right)}{\left( \frac{V_{REF\_I}}{M} \right)} \right) = \frac{1}{2} V_Y \log \left( \frac{V_{IN}}{V_{REF\_I}} \right), \quad (3.23)$$

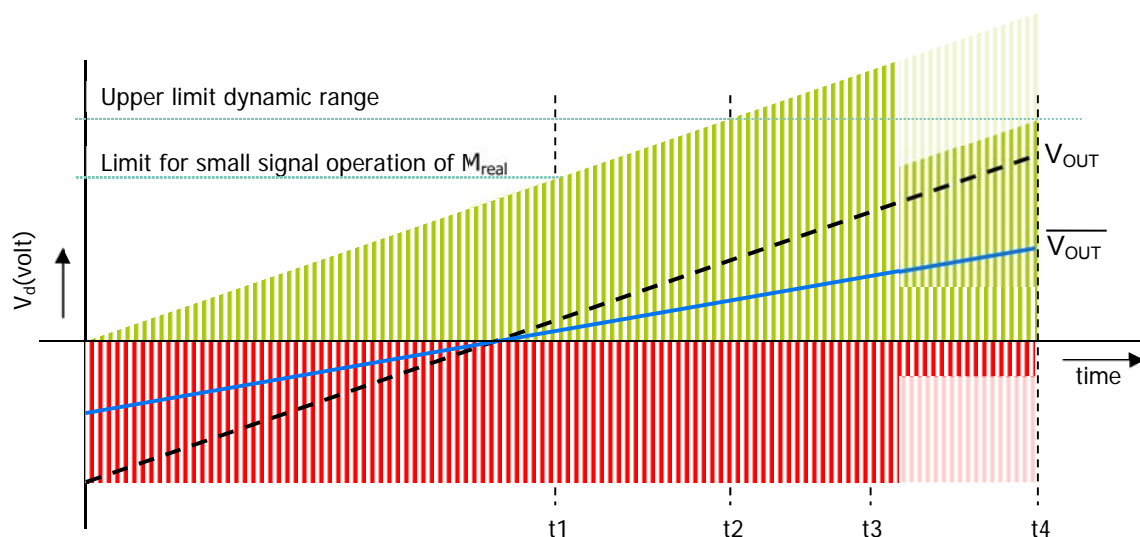
where  $M$  is the attenuation factor off the AAC. As already stated, the attenuation factor has to be chosen equal to the multiplication factor  $A$ , or a multiple of it. The reason for this will be discussed later in this section

From this simple math it is shown that Equation (3.8) and Equation (3.23) both lead to the same output. So, the output and thus also the intercept fixation method are not influenced

When we calculate the expected slope information voltage including the attenuation method

$$V_{OUT\_S} = \frac{1}{2} \frac{R_s G E_K}{\log(A)} \left( \log \left( \frac{\left( \frac{V_{IN}}{M} \right) A}{\left( \frac{V_{REF\_I}}{M} \right)} \right) - \log \left( \frac{\left( \frac{V_{IN}}{M} \right)}{\left( \frac{V_{REF\_I}}{M} \right)} \right) \right) = \frac{1}{2} R_s G E_K \quad (3.24)$$

This shows that the slope fixation method is also not influenced.



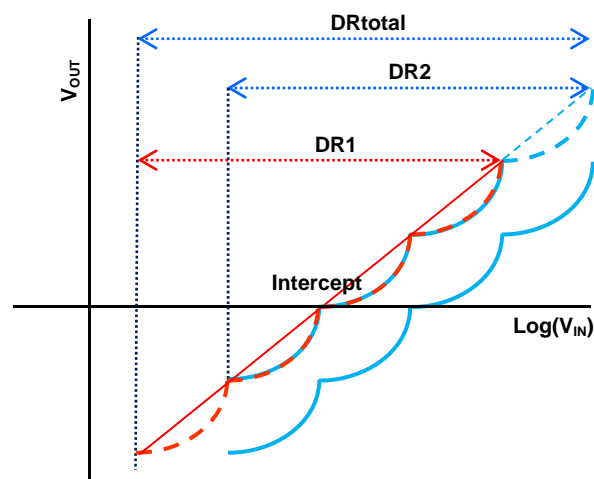
**Figure 3.17** Attenuation by ACC will result in a decrease of  $\log(V_{REF\_I})$  (red) and  $\log(V_{IN})$  (green) by same amount. Due to filtering with a relative high time constant the effect on  $V_{OUT}$  will be negligible.

To have a more clear understanding of the internal mechanism of this AAC method we will take a look at the signal example shown in Figure 3.17. This signal represents the signal at the output of the upper right switching device of Figure 3.16, for the situation in which the input of the logarithmic device is switched between an input signal  $V_{IN}$  that is logarithmically increased over time, and the fixed intercept reference voltage  $V_{REF}$ .

For simplicity of the signal the multiplication factor system and gain error are excluded from this signal example. The red part of the signal in Figure 3.17 denotes the result of the negatively switched reference voltage  $V_{REF\_I}$  and the green linearly changing signal part is the result of the logarithmically increasing switched input signal  $V_{IN}$ . As can be seen, at time  $t1$  the AAC starts to attenuate the reference signal (red) and input signal (green) because the input signal almost reached the non-linear range of the multiplication cell,  $M_{real}$ . As a result of the logarithmic operation, the attenuation will cause both signal parts to be decreased by the same amount, as can be seen at time  $t1$ . Now, when we subtract the green signal part from the red signal part we will get the signal as depicted by the black dotted line. As we already mentioned before the whole signal is actually an alternating signal with a duty cycle of 50%. Because of this duty cycle the output of the filter will result in a signal,  $\overline{V_{OUT}}$ , as depicted by the solid blue line. Because the integration time of the filter normally is much longer compared to the duration of the pulses, the effect of switching the attenuation on both outputs will be very small, resulting in a transfer without interruption.

As we pointed out earlier, there is an interesting and useful side-effect when using this attenuation method. Looking at time  $t2$  we can see that when we not attenuate, the upper end of the dynamic range would be reached. While attenuation results in that the upper dynamic range is shifted to the input value that is reached at time  $t4$ .

Now that we have shown the basic consequences of the mechanism on the small signal and dynamic range, we still have to take a closer look at the effect on the log transfer itself. When looking into what is actually happening with the transfer we can show why we have to choose an attenuation factor equal to the multiplication factor or a multiple of it. When the attenuation factor is chosen equal to the multiplication factor, the levels of  $V_{IN}$  for which an A/O cell starts clipping will be shifted exactly one multiplication factor,  $A$ , higher. This can be seen on logarithmic scale as a shift to the right of the transfer (blue solid line) as shown in Figure 3.18. Now, because the intercept fixed is still functioning and unaltered with the attenuation procedure the transfer will be shifted upward to joining the same intercept as was for the non-attenuated transfer. This is visualised with the blue dotted line in Figure 3.18.



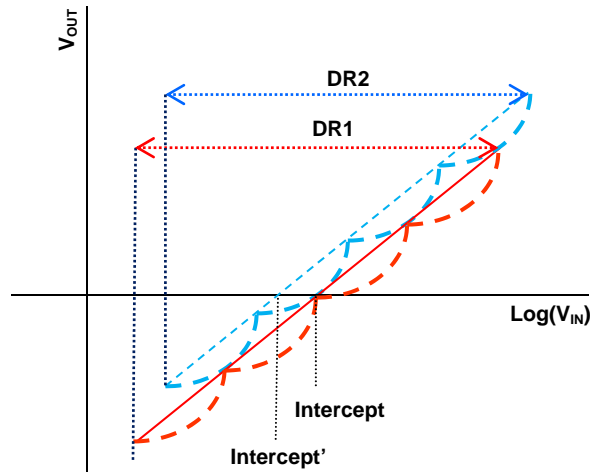
**Figure 3.18** Dynamic range shift when attenuation with value of  $A$  is used. Dynamic range in higher range will be extended by a factor  $A$



So, the red dotted line shows the transfer without attenuation and the blue dotted line shows the transfer with an attenuation factor equal to  $A$ . For input values below the attenuation activation input value the output will follow the red dotted transfer and for values higher than the activation value the output will follow the blue dotted transfer. As a result the total dynamic range, is extended.

As shown, there will be no interruption in the rippled shape of the transfer. The reason that there is no interruption in the ripple shape can be found in the attenuation value we used. As we have chosen this value to be equal to the multiplication factor, both transfers will have equal transition point values in the dynamic range they share. As the transition points are the values for which the transfer has exactly the value of the ideal straight line response, as shown in Figure 3.18, the intercept stays unchanged.

However, when the attenuation value does not correspond to the multiplication factor, the transfer would show an interruption. This can be shown when we take a look at Figure 3.19. In this figure the attenuation is chosen to be smaller than the multiplication factor. As a result the shift to the right will be smaller than  $A$ . Because of the intercept fixation the transfer will again shift upward such that this transfer has the wanted intercept. As shown by Figure 3.19, the transfers will have the same intercept, but the transition points in the combined dynamic range now don't overlap. When we look to Figure 3.19 we can see that because of the ripple the ideal straight line transfer will be shifted up to high. While both transfers intersect the horizontal axes at the wanted intercept, the actual intercept of the straight line response is now shifted to a lower value. It is not difficult to see that, when switching between both transfers an interruption of the ripple shaped transfer will occur.



**Figure 3.19** Interruption of transfer will occur when attenuation with value different than  $A$  is used.

Of course we have to mention that the ripple in the transfer for the piecewise approximation log detector implemented with  $\tanh A/0$  cells is much smaller than the one implemented by ideal  $A/0$  cells. In that situation an attenuation with a different factor than the multiplication factor will not lead to a large unwanted intercept shift. But for best results we still have to take the right attenuation factors which because of the sinusoidal shape of the log conformance transfer is now  $A(\sqrt{A})^K$ , with  $K$  is 0 or a positive integer. This is possible because the sinusoid intercepts the ideal log transfer 2 times per period, while the parabolic shaped transfer only hits the ideal line at the transition points, which is one time per period.

Actually there is a limit on the maximum upper range of the dynamic range to which it can be extended by the attenuation switching method. This is because we have to be sure that the lower end of the dynamic range of the attenuated transfer does not exceed the fixed intercept value. Otherwise the transfer will start to shift to the right. So, switching to other attenuation factor, to extend the transfer to higher range, is only possible as long as the fixed intercept is in the linear log range of the attenuated detector transfer.

There is one extra consideration that has to be taken into account: we have to prevent rapid switching between the transfers when the input voltage,  $V_{IN}$ , drifts around the attenuation switching point. We can solve this problem by introducing hysteresis, i.e., with a mechanism that uses two attenuation switching points; let's say at voltage  $V_{IN1}$  and a slightly higher voltage  $V_{IN2}$ . The attenuation has to turn on when the input voltage rises above input voltage  $V_{IN2}$ , but not turn off until the input voltage drops below input voltage  $V_{IN1}$ . This means that the on/off switching of the attenuation, when the voltage is between  $V_{IN1}$  and  $V_{IN2}$ , depends on the history of the input voltage.

From this section we can conclude that the attenuation method not only can be used to keep the multiplication cell,  $M_{real}$ , in small signal operation but can also be used to extend the dynamic range to higher input regions.

### 3.3 Switching frequency considerations

As we know, the slope and intercept fixation method is based on switching of the signal that the log device processes. Although the log device itself has a relatively high bandwidth there is a limit for the switching frequency that can be used. We have to be sure that the frequency used to switch between  $V_{IN}$  and  $V_{REF\_I}$  should be such that the sum of the switching frequency and the highest frequency of interest in  $V_{IN}$  is lower than the highest frequency that the log device can reliably process. This criterion also holds for the sum of the switching frequency and the frequency of the reference signal  $V_{REF\_I}$ . In practice, the switching frequency will be chosen several decades above the highest intended output signal, which in the case of a log detector is the envelope frequency of the RF input signal. This allows for effective removal of unintended output signal frequency components at the switching frequency (e.g. the DC output offset of the log detector is converted to this frequency by the output polarity switch). The filter should pass the highest intended output signal frequency of interest in the log detector output signal, but suppress frequency components introduced by the chopping/polarity switch.

Finally we have to discuss the error in the slope information voltage  $V_{OUT\_S}$  in relation with the switching frequency. In Equation (3.12) we considered a constant input voltage. However, if we consider the real implementation it is shown that we actually have an input signal  $V_{IN}$  which is changing over time. So, if  $V_{IN}$  changes to  $\alpha V_{IN}$  during the second switching period,  $V_{OUT\_S}$  will be defined by a input change of  $V_{IN} - (V_{IN}\delta)A$  instead of  $V_{IN} - V_{IN}A$ . With the knowledge that the value of  $V_{OUT\_S}$  actually represents  $\Delta V_{OUT}$  the effect on  $V_{OUT\_S}$  can be calculated with the use of Equation (3.12),

$$\Delta V_{OUT}' = \frac{R_S G E_K}{\log(A)} \left( \log \left( \frac{(V_{IN}\delta)A}{V_X} \right) - \log \left( \frac{V_{IN}}{V_X} \right) \right) \quad (3.25)$$

This can be simplified to

$$\Delta V_{OUT}' = R_s G E_K \frac{\log(A\delta)}{\log(A)} \quad (3.26)$$

The percentage error can be calculated as follows

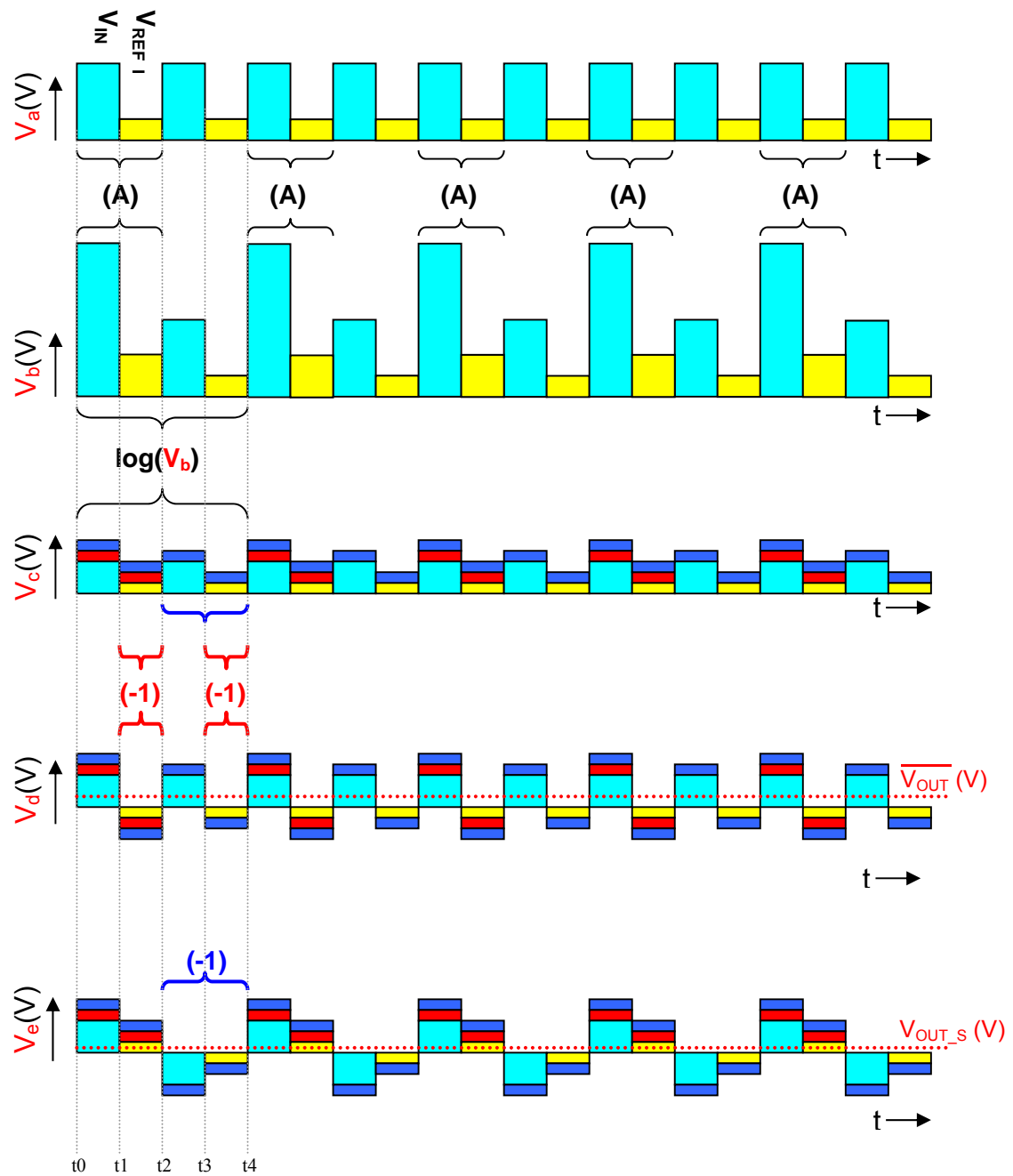
$$\varepsilon_{V_{OUT\_S}} = \varepsilon_{\Delta V_{OUT}} = \left( \frac{\Delta V_{OUT}'}{\Delta V_{OUT}} - 1 \right) \cdot 100\% = \left( \frac{\log(A\delta)}{\log(A)} - 1 \right) \cdot 100\% \quad (3.27)$$

We now need to see how large we can expect the change in  $V_{IN}$ ,  $\delta$ , to be. When we take a look at Figure 3.7 it was shown that only state 1 and 3 depend on the input signal  $V_{IN}$ . For best results both states should have equal value of  $V_{IN}$ . To get a small difference in  $V_{IN}$  we have to ensure to make the duration of the states as small as possible, such that the change in  $V_{IN}$  between both stages is small. This shows that a fast switching frequency is necessary. As the switching frequency will be chosen several decades larger than the frequency of the envelope of  $V_{IN}$ , the parameter  $\delta$  in Equation 3.20 will be very small. Actually, the influence of  $\delta$  will be even smaller than discussed. When we look again at Figure 3.7 we can see that the signal not only includes the varying  $V_{IN}$  but also includes the fixed reference voltage,  $V_{REF\_I}$ . Hence  $V_{REF\_I}$  will not generate an input error between state 2 and 4, because it has a constant value.

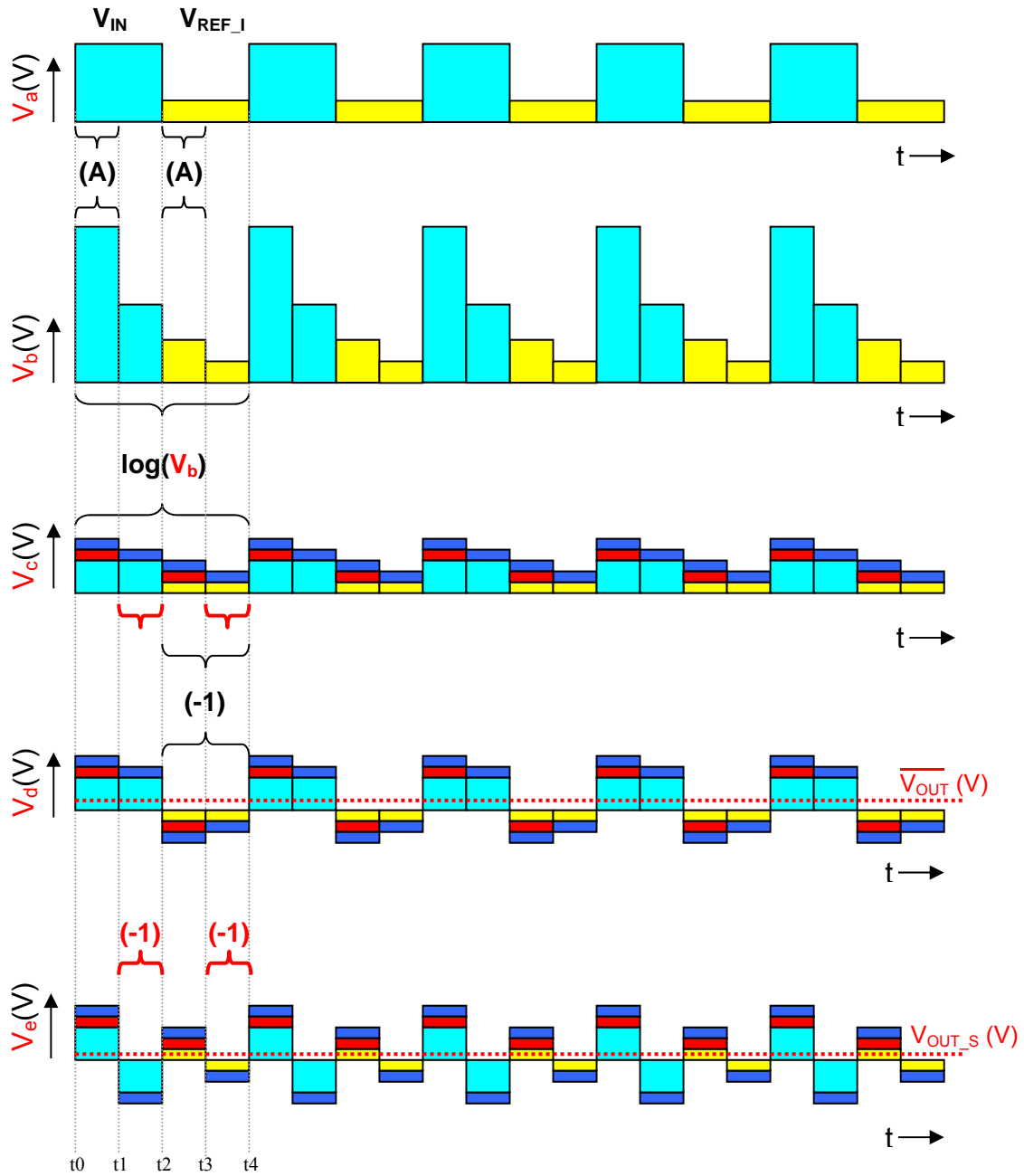
This means that after filtering the mean value of the error will be two times lower.

$$\varepsilon_{V_{OUT\_S}} = \frac{\left( \frac{\log(A\delta)}{\log(A)} - 1 \right)}{2} * 100\% \quad (3.28)$$

Although this error will be already very small a last choice can be made to make it even smaller. First we have to look at Figure 3.20, which shows an overview of the signal modulation of the complete method as described in this chapter. Now, when we exchange the switching frequency of the clocks  $CLK_1$  and  $CLK_2$  in Figure 3.16 the signal modulations will be as shown in Figure 3.21. When we compare Figure 3.20 and 3.21 we can see that the values of the states between  $t1$  and  $t3$  of signal  $V_e$  are exchanged. As a result the states including  $V_{IN}$  (the states which include the light blue component) are placed side by side. This will lead to a smaller difference in  $V_{IN}$  during both states.

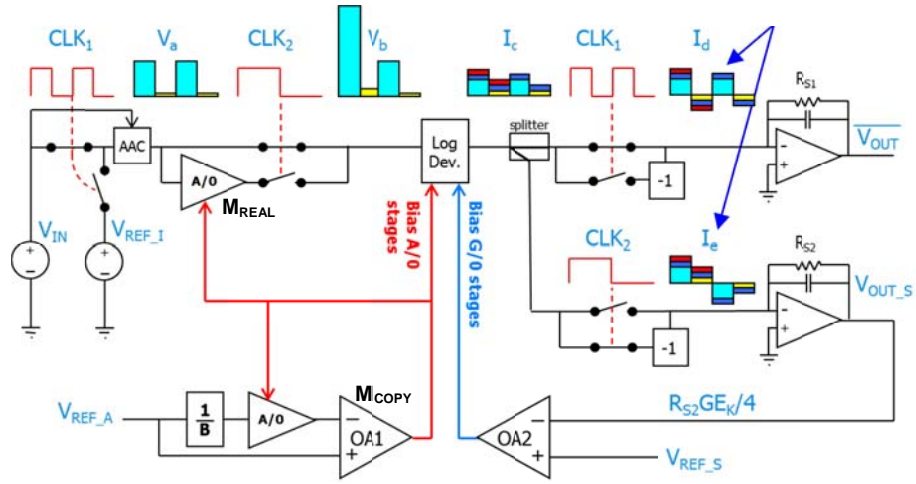


**Figure 3.20** Overview of signalling of the overall intercept and slope fixation method



**Figure 3.21** When clock frequency  $CLK_1$  and  $CLK_2$  are exchanged, the values of the states between  $t_1$  and  $t_3$  of signal  $V_e$  will exchange

### 3.4 Final system overview



**Figure 3.22** Low-pass filters realized using an op-amp based integrator

Figure 3.22 shows the final system architecture. This architecture has some modifications compared with that of Figure 3.16. The load resistor  $R_S$  is removed from the log device such that it has a current output instead of a voltage. This current is split into two output currents. The low pass filters, which were depicted as ideal building blocks, are replaced by active low-pass filters realized using an op-amp RC integrator. Parallel to each capacitor of the integrator, a resistor is placed. So, instead of one load resistor  $R_S$  we now have two resistors,  $R_{S1}$  and  $R_{S2}$ . These resistors will form the time constant of the active filter (together with the capacitors) but also the steady state DC output voltage. The integrators form a buffer at the output of the circuit.

With use of Equation (2.32) and Equation (3.8) and the knowledge about the current split the real output of the device is now defined as

$$\overline{V_{OUT}} = \frac{1}{4} V_Y \log \left( \frac{V_{IN}}{V_{REF\_I}} \right) = \frac{1}{4} \frac{R_{S1} G E_K}{\log(A)} \log \left( \frac{V_{IN}}{V_{REF\_I}} \right), \quad (3.29)$$

where the factor change from  $\frac{1}{2}$  to  $\frac{1}{4}$  is a result of the current splitter. As can be seen the real log device output is now set by resistor  $R_{S1}$ .

Besides the buffering capability of the integrators this architecture now also enables a way to set the expected slope information voltage  $V_{OUT\_S}$  for a particular slope of the log transfer without altering the real output  $\overline{V_{OUT}}$  of the log device. By changing the value of  $R_{S2}$ , the voltage  $V_{OUT\_S}$  can be set to an arbitrary value

$$V_{OUT\_S} = \frac{1}{4} R_{S2} G E_K \quad (3.30)$$

Which can be rewritten as

$$V_{OUT\_S} = \frac{1}{4} \alpha R_{S1} G E_K \quad (3.31)$$

where

$$\alpha = \frac{R_{S2}}{R_{S1}} \quad (3.32)$$

The ratio  $\alpha$  can be accurately set with matched resistors. The ability to set the slope information voltage  $V_{OUT\_S}$  to higher value without altering the output voltage  $\overline{V_{OUT}}$  makes it possible to increase the reference voltage  $V_{REF\_S}$  to favourable values which will set the accuracy of the system, as will be clarified in the next chapter.

The slope through which the ideal slope fixation system should settle can be configured with the use of following equation.

$$Slope = \frac{V_{REF\_S}}{\alpha \cdot 20 \log(B)} \quad (3.33)$$

This equation shows that the slope can be set by three accurate parameters: the ratio  $\alpha$  between the resistor value of  $R_{S1}$  and  $R_{S2}$ , the voltage reference  $V_{REF\_S}$  and the attenuation factor  $B$  of the divider block. The equation also shows that the ratio between the resistors can be used to set the reference voltage  $V_{REF\_S}$  to an arbitrary value.





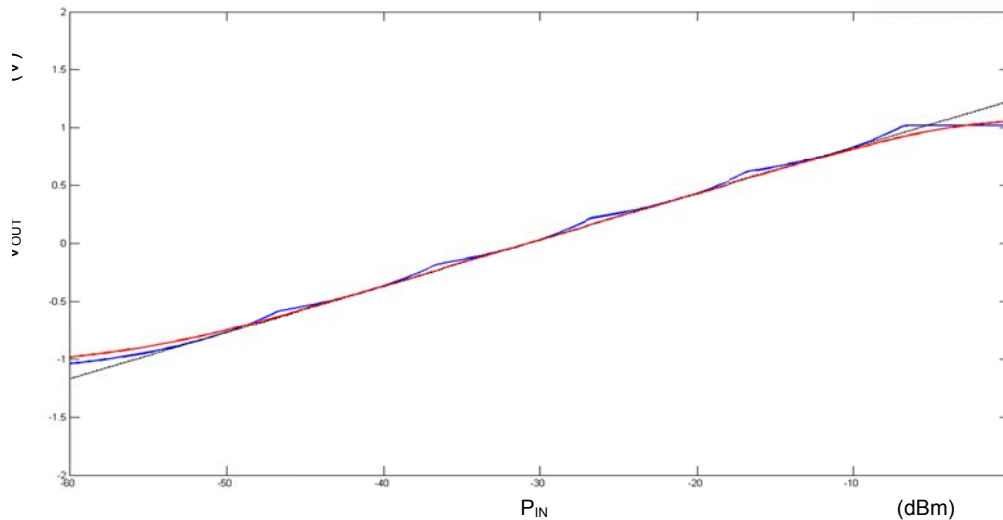
## 4 System level verification

In the previous chapter we have focused on the operation of the overall fixation method. In this chapter we will verify the operation of the overall fixation method by looking at the system level simulation results. As non-idealities in the real implementation of the method will limit the performance, we will also investigate the sensitiveness for the errors that alter the accuracy of the method. From Subsection 2.4.2 we know that the accuracy or log linearity of logarithmic devices is examined by the conformance error. In that section we pointed out that the conformance error has to stay between +1.0dB and -1.0dB. So, to make calibration after production unnecessary, we have to make sure that the error contributions of the non-idealities in the system are low enough, such that the log device does not exceed the log conformance requirements.

### 4.1 Defining the ideal transfer

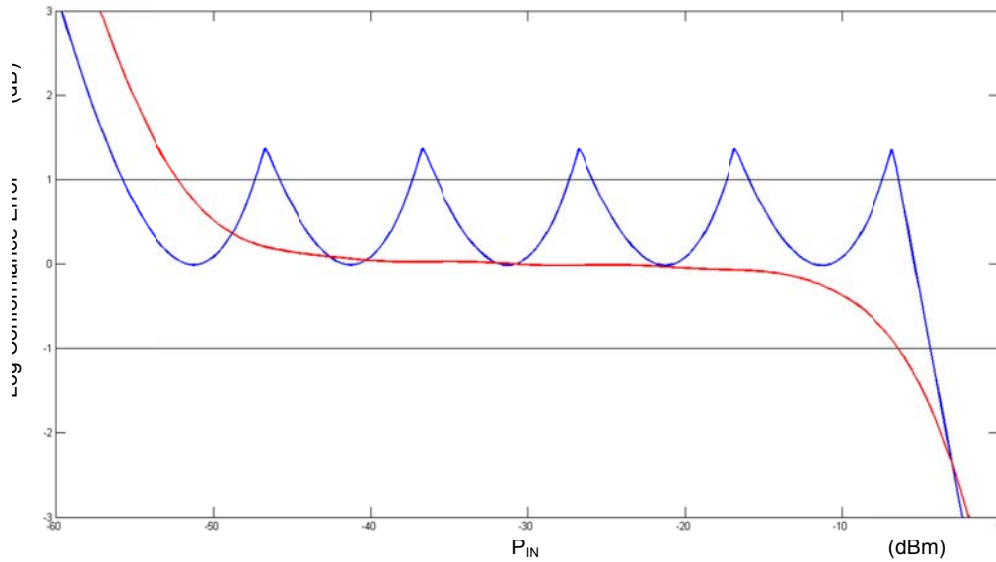
As explained in Sub Section 2.4.2 the ideal straight line logarithmic transfer of the log device is used to construct the log conformance curve of a log device. In this section we will first construct the log conformance curve of a log device with ideal bias conditions, where after we can start to examine the conformance sensitivity to deviations in the two bias signals of the log device. To develop the log conformance curve of the ideal biased log device we first assume the situation in which the log device is incorporated inside the intercept fixation system as was shown by Fig 3.1.

Let's say that the transfer of the log device under test is characterized by a cascade of four A/O cells and five detector cells in a configuration as was shown by Figure 3.12. The resistor  $R_S$  is chosen to be 24K $\Omega$ . The A/O cells are biased to a small signal gain of 10 dB or 3.16x and the G/O cells are biased to a transconductance  $G$  of 1.29mS. With these bias conditions and assuming a temperature of 27°C the slope of this device will be 40mV/dB. The intercept fixation system is configured in such a way that the intercept of the transfer is fixed at -30.75dBm. A simulation of the configuration results in the (blue) transfer as shown in Figure 4.1.



**Figure 4.1** Piece-wise linear log transfer (blue curve) with a slope of 40 mV/dB generated by a cascade of four ideal A/O cells each having a gain of 10 dB and the log transfer (red curve) when ideal A/O cells are replaced by tanh cell's

Now, when we replace the ideal A/O cells by tanh cells as was discussed in Section 2.4.2 it will result in the smoothened transfer (red line) as shown in Figure 4.1. The idealized straight line transfer with a slope of exactly 40mV/dB and an intercept of -30.75dBm is shown by the black solid line in Figure 4.1. Using this straight line transfer, the log conformance curve of both transfers can be constructed as shown in Figure 4.2.



**Figure 4.2** Log Conformance Error for the log device implemented with the ideal A/O cells (blue curve) and the Log Conformance Error for the log device implemented with tanh cells (red curve).

The blue curve, representing the log conformance of the device with the ideal A/O cells, is lifted by the intercept method such that it correctly crosses the -30.75dBm intercept value. Because of the parabolic sections in the shape of this transfer it will exceed the 1dB log conformance requirements. However, for the device implemented with tanh cells the intercept value is also correctly set to -30.75dBm, but now the log conformance error (red curve) is much smaller (close to 0 dB) over the full dynamic range. From Figure 4.2 we can conclude that we chose the right bias conditions to set the slope at the wanted 40mV/dB and that the intercept fixation method is working properly.

## 4.2 Verification of the idealized Sloop fixation method

In previous section we have gathered the log conformance plot of the device under test with ideal bias conditions. The close to 0 dB conformance reading told us that the transfer of the device under test implemented with tanh cells has a very well defined 40mV/dB slope.

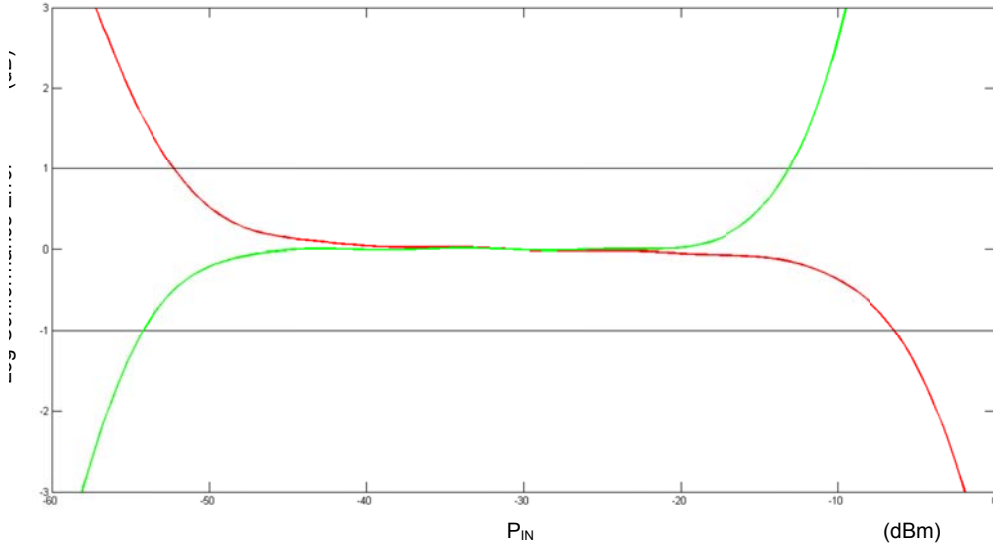
Now we will start to verify the operation of the overall fixation system on the device under test. This system, used to fixate the slope and the intercept, but also used to extend and fixate dynamic range, was shown in Figure 3.22.

To configure the slope to which the system has to control the transfer of the log device we can make use of Equation (3.33), which we developed in Subsection 3.4. The divider block is set to an attenuation factor of 3.16. The resistor ratio  $\alpha$  between  $R_{S1}$  and  $R_{S2}$  is set to 5 and the reference  $V_{REF\_S}$  is set to 2V.

According to Equation (3.33) this would result in the wanted 40mV/dBm slope, as shown by

$$Slope = \frac{V_{REF\_S}}{\alpha \cdot 20 \log(B)} = \frac{2V}{5 \cdot 20 \log(3.16)} = \frac{2V}{5 \cdot 10 dB} = 40mV / dB$$

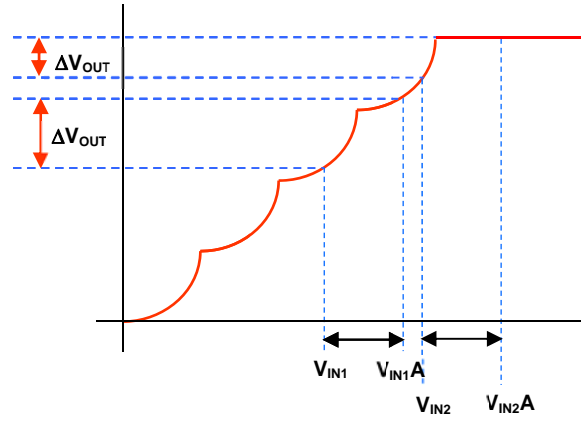
When we turn on the overall fixation system with these settings and use the ideal straight line response gathered in previous section to construct the log conformance it results in the green curve as shown in Figure 4.3.



**Figure 4.3** Transfer of the slope and intercept fixated logarithmic device

As shown by this figure the log conformance of the fixated transfer hovers even closer around the 0 dB log conformance reading. This shows that the slope is perfectly set to the 40mV/dBm. To test the fixation mechanism we have plotted the transfer for several different values of load resistance  $R_{S1}$  in which the resistor ratio  $\alpha$  was assumed to be fixed to 5. Each plot resulted in exactly in the same response, which confirmed that the slope fixation system is working properly.

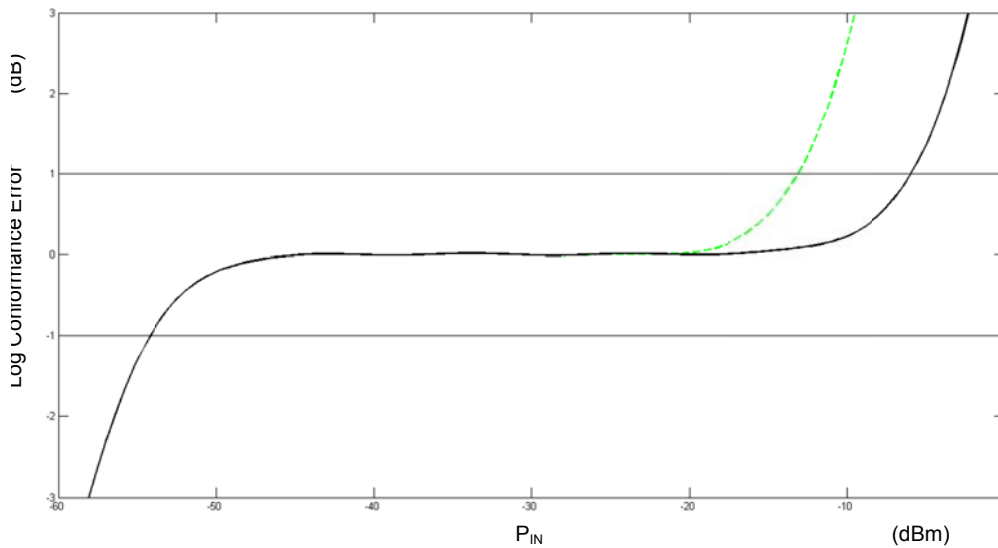
In Figure 4.3 we also have plotted the log conformance curve of the intercept fixated device with ideal bias conditions, which was developed in previous section. When we compare this plot with that of the overall fixated transfer (green curve), we can see one side-effect of the slope fixation procedure. Figure 4.3 shows that the slope and intercept fixated transfer correctly follows the ideal biased transfer till it reaches the last 10dB of the upper dynamic range. At around -20dBm it loses the ability to control the signal slope to correct values. This is of course a highly undesirable effect. The loss in the upper part of the dynamic range can be explained when we take a look at Figure 4.4.



**Figure 4.4** Smaller than expected output change caused by upper limit of dynamic range

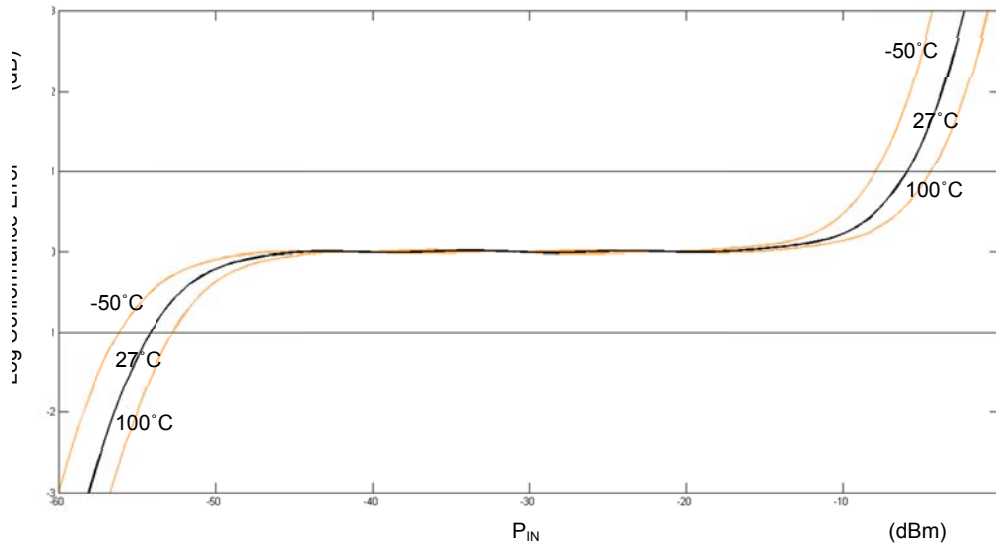
Figure 4.4 shows two signal values,  $V_{IN1}$  and  $V_{IN2}$ , and two multiplied versions of those input signals which are both multiplied by an equal multiplication factor,  $A$ . In both situations we would expect an equal change at the output of the log device. However, instead of an equal change in the output voltage, they differ from each other. This is due to a limit on the input signal for which the method works properly. When the input signal value is higher than the value of the second last transition point, as shown by  $V_{IN2}$  in Figure 4.4, the signal after multiplication will fall outside the dynamic range of the log device. This will result in a smaller than expected output change. As the feedback system tries to force this output change to be equal to the expected output change, the feedback loop will start to increase the transconductance of the detector cells, resulting in a transfer that increasingly deviates from the wanted transfer when the input signal is increased further.

The problem in the loss of dynamic range can be solved when using the proposed AAC method as was discussed in Section 3.2.2. When for example the attenuation method is used with a attenuation factor equal to the multiplication factor  $A$ , which was chosen to be 3.16, the transfer will be extended as shown by the simulation result (black line) in Figure 4.5.



**Figure 4.5** Dynamic range extension obtained by the proposed AAC method

Finally, we have to test the overall fixation system over temperature variation. The plots which are depicted in Figure 4.6 are showing the log conformance curves for a temperature of -50, 27, and 100 degrees Celsius.

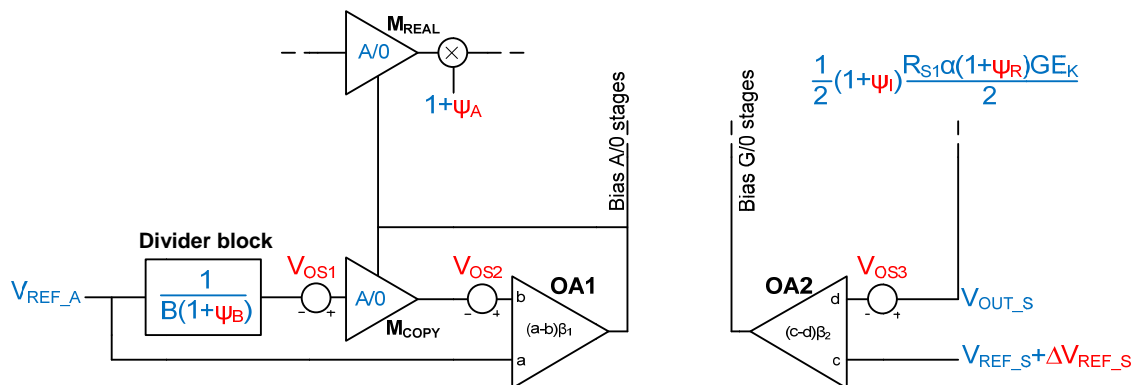


**Figure 4.6** Log conformance error deviation over temperature change

The log conformance hovers nicely around the 0 dB log conformance reading over the full temperature range. This shows that the system also correctly compensates the slope and intercept for temperature. It also shows that the dynamic range is fixed. But note that the input range itself shifts horizontally to the lower input for low temperature and to the higher input range for higher temperature. The temperature dependent input range shift becomes clear when we take a look at Figure 2.6. In this figure we can see that the temperature dependent clipping voltage  $E_K$  of the G/O stages together with a fixed gain  $A$  will result in a shift of the transfer over temperature.

### 4.3 The log conformance sensitivity to deviations in the slope fixation system

In this section we will focus on the non-idealities that alter the accuracy of the slope fixation system.



**Figure 4.7** Slope fixation system part including non-idealities

In Figure 4.7 we have depicted the most important parts of the proposed overall fixation system. On the left side of this figure we see the control system of the A/0 stages and at the right side the control system of the G/0 stages. In this figure we have included the error sources which will alter the accuracy of the overall system. These error sources originate from the non-idealities that the system faces when implemented by transistors.

For the control system of the A/0 stages system, which has to control the multiplication cells  $M_{COPY}$ ,  $M_{REAL}$  and the cascaded A/0 cells to a gain of  $A$ , we can list the following non-idealities:

- ***Deviation in the attenuation factor***  
The attenuation that has to be performed by divider block should be equal to  $B$ . However we can expect some deviation in the wanted attenuation caused by mismatch between resistive elements inside the divider as will be shown in Chapter 5. To model the deviation error in the divider block we have included parameter  $\psi_B$  as shown in Figure 4.7
- ***Input offset of the multiplication cell  $M_{COPY}$***   
When we implement the multiplication cell  $M_{COPY}$  at transistor level we can expect mismatch in the amplifiers internal transistors and resistors. To account for this, the net error is modelled as an input referred offset voltage. As shown in Figure 4.7 we will model this offset with parameter  $V_{OS1}$
- ***Input offset of the error amplifier OA1.***  
The error amplifier OA1 has to compare both of its input voltages and force them by means of negative feedback to be equal. However, as it was for the multiplication cell  $M_{COPY}$ , the error amplifier will also suffer from mismatch of internal components, when implemented by transistors. This error is also modelled by an input referred offset. Taking this offset into account, as indicated by  $V_{OS2}$  in Figure 4.7, it is not that difficult to see that the error amplifier will force the output of  $M_{COPY}$  to a wrong value.
- ***Mismatch between  $M_{REAL}$  and  $M_{COPY}$***   
In ideal case the gain stage  $M_{REAL}$  will be an exact copy of  $M_{COPY}$  and both should be independent of their load conditions. In this situation an equal bias voltage at both gain stages would result in exactly the same multiplication factor. However in reality this situation will not occur. We can expect a mismatch between the multiplication cell  $M_{COPY}$  and  $M_{REAL}$  and different load conditions for both stages. Because of this both stages will have different gain for the same bias signal, leading to a wrong multiplication factor of  $M_{REAL}$ . In our system we will model this error source with parameter  $\psi_A$

At the control system of the G/0 stages, which is used to control the transconductance of the G/0 stages, the non-idealities are represented by

- ***The input offset of the error amplifier OA2***

As it was for the other amplifiers, the error amplifier OA2 will also suffer from internal mismatch of its components leading to an input referred offset. In our system this error is represented by parameter  $V_{OS3}$

- ***Deviation in the voltage reference  $V_{REF\_S}$***

The reference voltage  $V_{REF\_S}$  at the input of the error amplifier OA2 is supposed to be equal to the expected reference voltage. In reality this reference can also deviate from the expected value. This error is modelled by parameter  $\Delta V_{REF\_S}$

- ***Deviation of the resistor ratio between the integrator resistors  $R_{S1}$  and  $R_{S2}$ .***

Resistor mismatch in the ratio  $\alpha$  between the resistors  $R_{S1}$  and  $R_{S2}$  is another issue which will alter the accuracy of the slope fixation system. As the resistor ratio  $\alpha$  is one of the parameters that is used to set the slope of the log device it should be accurately set. How accurate the ratio can be set depends on the layout technique used as will be discussed in Subsection 5.2.2.3. This error is modelled by the expression  $R_{S1}\alpha(1+\psi_R)$ , where the parameter  $\psi_R$  is the relative mismatch error, between the both resistors.

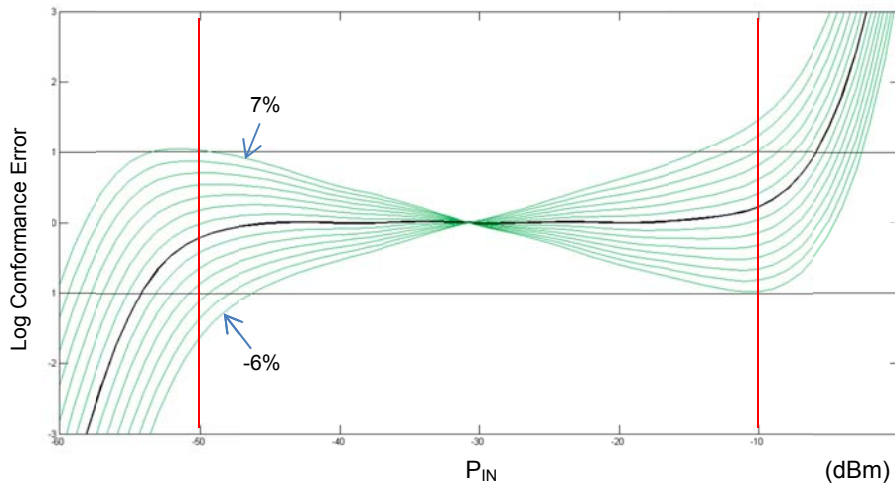
- ***Unbalanced current splitting***

The output current of the log device should be split exactly by 50% such that the ratio between both currents is 1. Any deviation would lead to an error in the slope control. The splitting error is modelled by the parameter  $\psi_I$ .

#### 4.3.1 Sensitivity to deviations in the control systems

Because the accuracy of logarithmic devices is examined by the conformance error which is expressed in dB we first have to translate deviations in the control system of the A/0 cells to a log conformance error. The same holds for the deviation in the control system of the G/0 cells.

As we know from Section 3.2.1 the accuracy of the slope fixation method relies on how accurately we can set the multiplication factor  $A$ . We will first investigate how sensitive the log conformance or accuracy is for a deviation in  $A$ . As reference we will use the log conformance curve of the device under test which was controlled by the ideal control system, which was shown by the black solid line in Figure 4.5. This log conformance curve (black line) is now also plotted in Figure 4.8. When we change the multiplication factor  $A$  by some percentage, the log conformance will start to deviate from the log conformance (black line) of the transfer with the wanted 40mV/dB slope, as can be seen from the change in log conformance (green lines) depicted in Figure 4.8.

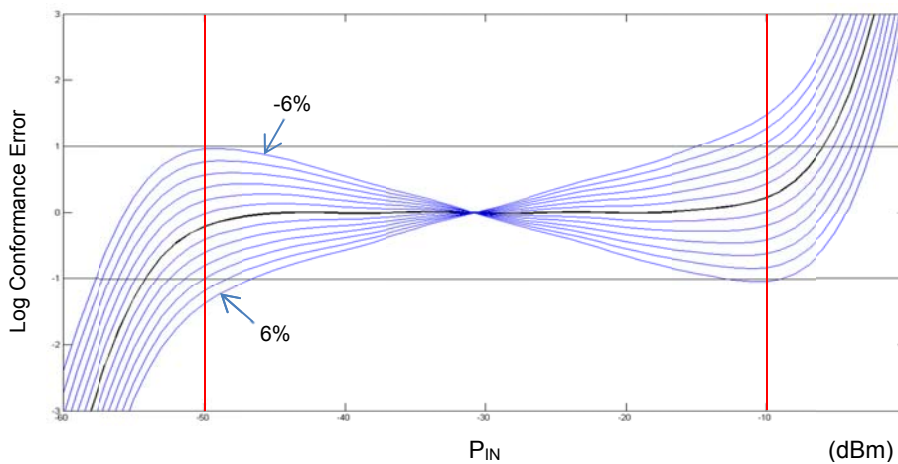


**Figure 4.8** Deviation of log conformance caused by a -6% to 7% change in the multiplication factor  $A$

As a side note, if we look at this figure we now even can see more clearly the effectiveness of the intercept fixation method. At the predefined intercept value of -30.75dBm the log conformance is 0dB and stays there unchanged. As can be seen the log conformance deviates the most at the two ends of the dynamic range. To examine the accuracy of the system we have to look at one of these ends. However, before we use Figure 4.8 to examine the sensitivity to the deviations in the multiplication factor  $A$ , we first will look at the dependency of the log conformance for changes in the transconductance  $G$ .

As we know, the transconductance of the G/0 cells are defining the parameter  $G$  of Equation (3.29) and Equation (3.30). From these equations we can see that that the accuracy of the system also relies on how accurately the bias control system of the G/0 cells can control to the right bias of these cells.

To see the sensitivity on the log conformance for a deviation in the transconductance of the G/0 cells we have plotted the conformance for several transconductance values  $G$ . The change in transconductance  $G$  of the G/0 cells results in the log conformance deviations (blue lines) as depicted in Figure 4.9

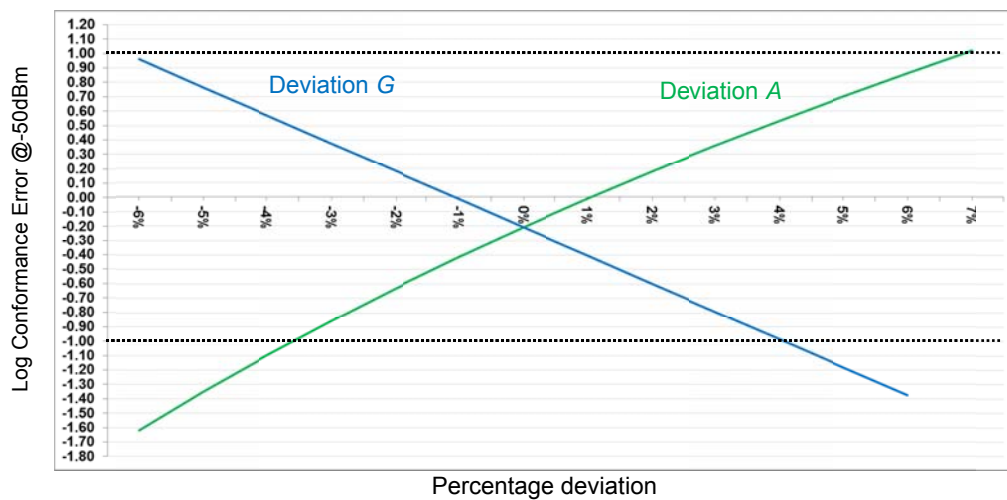


**Figure 4.9** Deviation of log conformance caused by a -6% to 6% change in transconductance  $G$



Again we can see that the intercept is correctly fixated. Furthermore we can see that again the log conformance deviates the most at the upper and lower end of the dynamic range. The upper end and lower end of the dynamic range define the total dynamic range. As the intercept is placed in the middle of the dynamic range the log conformance at both ends deviates almost symetrically but in opposite directions. Because of the symmetrical behaviour we can investigate the sensitivity of the log conformance for deviations in the multiplication factor and the bias of the G/0 cells by looking only at the lower or upper end of the dynamic range. Let's assume that the lower end of the dynamic range is defined at -50dBm, as indicated by the left red vertical line in Figure 4.8 and 4.9. From both figures we can see that as long as the log conformance at the input power -50dBm stays between +1 and -1dB the log conformance requirements over the full dyanamic range (-50dBm till -10dBm) will be obtained.

By taking the values of the intersection point of the logconformance curves with the vertical red line at -50dBm in Figure 4.8 and 4.9 we can construct the graph as shown in Figure 4.10.



**Figure 4.10** Log conformance @ -50dBm, for deviations in multiplication factor A (green line) and transconductance G (blue line)

The green line in this figure represents log conformance over percentage deviations in the multiplication factor (and gain of the A/0 cells) at the -50dBm input power, while the blue line represents log conformance over percentage deviations in the transconductance  $G$  at an input power of -50dBm.

The horizontal black dotted lines in Figure 4.10 depict the -1dBm and +1dBm log conformance boundaries. Now when we look at this figure, we can clearly see that at the -50dBm input power the multiplication factor  $A$  is allowed to deviate between -3.7% and +7% to obtain a logconformance between -1dB and +1dB. In same figure it is shown that the detector biasing system is allowed to deviate between 4% and -6.3% in transconductance  $G$  to obtain a log conformance between +1dB and -1dBm.

From Figure 4.10 we can conclude that the accuracy of the fixation method is most sensitive for negative deviations in the multiplication factor  $A$  and positive deviations in the transconductance  $G$ . With this knowledge we can observe a possible accuracy improvement: we can lift both graphs in Figure 4.19 0.20dB upward such that the figure becomes more symatrical around the 0dB Log Conformance Error. This can be obtained when we modify the attenuation parameter  $B$  of the

divider block by 1.7% such that the modified multiplication factor  $A'$  is set to a 1.7% higher value than  $A$ . With a +0.2dB correction at the graph of  $A$  in Figure 4.10 we can see that the allowed +7% deviation will be decreased to +5.5%. However for a negative deviation the maximal -3.7% deviation in  $A$  is now increased to -4.5% for  $A'$ . A similar reasoning can be applied for the maximum allowed deviation in  $G$  for the transconductance control system. For the maximal deviation in  $G$  the positive deviation is increased from 4.1% to 5.2% while the -6.2% is decreased to -5.2%. So with the +0.2dB correction we now can allow a deviation between -4.50% and +5.50% from the modified multiplication factor  $A'$  and a deviation of -5.2% and +5.2% from the modified transconductance  $G'$  to obtain a log conformance between -1dB and 1dB.

Of course we should expect that a possible deviation in multiplication factor  $A$  and transconductance  $G$  will be present at the same time. So, deviations at both system parts will contribute to an overall deviation. So, to put the accuracy of the method within the 1 dB log conformance error band without the need for manual calibration, it is important that both control system parts contribute less than the maximum allowed deviations as just stated.

Let's assume that it is possible to minimize the maximum expected deviation of the modified multiplication factor ( $A' = A + 0.017A$ ) between +2.5% and -2.5%. From the graph in Figure 4.7 it is shown that a -0.8% deviation in  $A'$  (a result of +1.7%-2.5%) represents a log conformance error (at an input of -50dBm) of -0.37dB. This means that an extra contribution to the log conformance error caused by a positive deviation in the transconductance is limited to -0.63dB to put the system at the edge of the -1dB error band. From Figure 4.7 we can use the graph of the deviation in  $G$  to find the maximum percentage deviation in transconductance for an additional log conformance error of -0.63dB. The graph shows that -0.63dB represents a +2.2% deviation in transconductance  $G$ . So, by using the graphs in Figure 4.7 we found that a -2.5% deviation in the multiplication system and a +2.2% deviation in the transconductance control system will put the system at the edge of the -1dB error band.

Not discussed, but also possible, is to modify the allowed deviation is by modifying the reference voltage  $V_{REF\_S}$ .

The procedure to convert from the dB scale towards a percental change of both system parts, as was explained above, will be used in reversed manner in the following subsections to translate the percentage deviation caused by a non-ideality to the log conformance dB scale.

#### 4.3.1.1 Sensitivity of the system accuracy to the individual error sources

The effect of the non-idealities on the accuracy of the overall system will be discussed in this and the following subsections. From the previous section we got some insight into the sensitivity of the method for deviations in the A/0 control system and the G/0 control system. With that knowledge in mind we now will start looking into the dominance of the individual error sources that are causing these deviations.

#### 4.3.1.1.1 Sensitivity to the individual error sources of the A/0 control system

At first we start by analysing the control loop of the A/0 cells shown on the left side of Figure 4.7.

The open loop transfer from  $V_{REF\_A}$  to  $Y_I$  is

$$Y_I = \left[ \left( \left( \frac{V_{REF\_A}}{B(1+\Psi_B)} + V_{OS1} \right) A + V_{OS2} \right) - V_{REF\_M} \right] \beta_1 \quad (4.1)$$

and the closed loop equation is

$$-AY_I + (-AY_I + V_{OS2})\beta_1 = Y_I \quad (4.2)$$

Solving for  $Y_I$  leads to

$$Y_I = \frac{V_{OS2}\beta_1}{1 + A + A\beta_1} \quad (4.3)$$

Now, by substituting Equation (4.3) into Equation (4.1) and isolating  $V_{REF\_A}$  the resulting equation becomes

$$V_{REF\_A} = \frac{V_{OS1}A + V_{OS2} + \frac{V_{OS2}}{1 + A + A\beta_1}}{1 - \frac{A}{B(1 + \Psi_B)}} \quad (4.4)$$

When assuming a high loop gain, so  $\beta_1 \gg 1$ , Equation (4.4) can be simplified to

$$V_{REF\_A} = \frac{V_{OS1}A + V_{OS2}}{1 - \frac{A}{B(1 + \Psi_B)}} \quad (4.5)$$

Now, by isolating the multiplication factor,  $A$ , from Equation (4.5), we get the final equation

$$A = f_A(V_{OS1}, V_{OS2}, V_{REF\_A}, \Psi_B) = \frac{V_{REF\_A} - V_{OS2}}{V_{OS1} + \frac{1}{B(1 + \Psi_B)} V_{REF\_A}} \quad (4.6)$$

This equation shows the dependency of the multiplication factor of the multiplier cell  $M_{COPY}$  on the errors in the system.

In the ideal case, i.e., if there are no errors, we can simplify Equation (4.6) to

$$A_0 = f_A(V_{OS1} = 0, V_{OS2} = 0, V_{REF\_A} = 0, \Psi_B = 0) = \frac{V_{REF\_A}}{\frac{1}{B}V_{REF\_A}} = B \quad (4.7)$$

So, as expected, in the ideal case the multiplication factor will be forced to be exactly equal to the attenuation factor  $B$  of the divider block.

Now that we have Equation (4.6) and Equation (4.7) we can start to examine the individual error contributions of the non-idealities to the deviation in the multiplication factor  $A$ .

### Input offset voltage at error amplifier OA1

First we will look at the contribution to the deviation of the multiplication factor caused by the input offset voltage of amplifier OA1. As indicated by Figure 4.7 we model the input offset of amplifier OA1 by parameter  $V_{OS2}$ .

Taking only offset voltage  $V_{OS2}$  into account, Equation (4.6) simplifies to

$$A_1 = \frac{V_{REF\_A} - V_{OS2}}{\frac{1}{B}V_{REF\_A}} = \left(1 - \frac{V_{OS2}}{V_{REF\_A}}\right)B \quad (4.8)$$

Using Equation (4.7) and (4.8) we can calculate the relative change in the multiplication factor

$$\delta A_1 = \frac{A_1}{A_0} = \frac{\left(1 - \frac{V_{OS2}}{V_{REF\_A}}\right)B}{B} = \left(1 - \frac{V_{OS2}}{V_{REF\_A}}\right) \quad (4.9)$$

This can be represented in a percentage deviation by

$$\varepsilon_1 = (\delta A_1 - 1) \cdot 100\% = \left( \left(1 - \frac{V_{OS2}}{V_{REF\_A}}\right) - 1 \right) \cdot 100\% \quad (4.10)$$

From this equation it becomes clear that  $V_{REF\_A}$  should be chosen as high as possible to minimize the influence of  $V_{OS2}$  on the deviation of the multiplication factor. As discussed in Section 3.2.1 the magnitude of the DC reference  $V_{REF\_A}$  should not be too high because it has to be limited to put  $M_{COPY}$  in its small signal operating range. For example when we look at the graphs in Figure 3.15 it was shown that we should not go higher than an input voltage of approximately 5mV to have an error contribution of maximally 0.55% in the multiplication factor at the temperature

extremes of -50 °C and 100°C. Note that we obtained these relative low error values for an input of 5mV by reducing the value of  $B$  by 1.15%, as was discussed in Section 3.2.1.

Knowing that the input voltage at the input of  $M_{copy}$  has to be limited to 5 mV and the attenuation factor, including the reduction, of the divider block equals  $B(1-0.0115)$ , voltage  $V_{REF\_A}$  is limited to

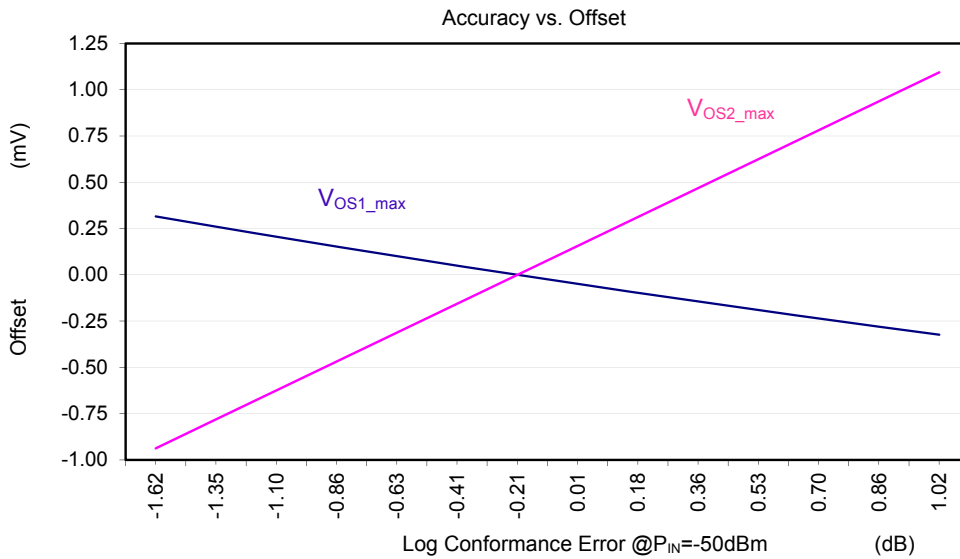
$$V_{REF\_A\max} = B(1-0.0115) \cdot 5mV \quad (4.11)$$

In our example of Section 4.1, the attenuation factor was chosen to be equal to 10dB or 3.16x. Using Equation (4.11) shows us that the reference voltage  $V_{REF}$  is thus limited to 15.62mV.

By isolating  $V_{OS2}$  from Equation (4.10) we now can calculate the maximum allowable offset voltage  $V_{OS2}$

$$V_{OS2\_max} \Big|_{V_{OS1}=0, \Delta B=0} = \frac{\varepsilon_1}{100\%} V_{REF\_A\max} = \frac{\varepsilon_1}{100\%} 15.62mV \quad (4.12)$$

Now, the graph for the multiplication factor in Figure 4.10 can be used to convert the percentage values obtained in Equation (4.12) to the log conformance error contribution in dB. With this knowledge the graph for the maximal allowable offset for a typical accuracy in dB can be plotted as shown by the pink line in Figure 4.11.



**Figure 4.11** Sensitivity of the accuracy for  $V_{OS1}$  and  $V_{OS2}$

Before we investigate this graph we first will take a look at the offset voltage  $V_{OS1}$  of the multiplication cell  $M_{COPY}$

### Input offset voltage of the multiplication cell $M_{COPY}$

The same mathematical procedure as was we used in previous sub section can be used to find the dependence of the multiplication factor,  $A$ , on the input offset voltage at the multiplication cell  $M_{COPY}$ . As was shown by Figure 4.7 we will model this offset by parameter  $V_{OS1}$ .

When we only take  $V_{OS1}$  into account Equation (4.6) can be rewritten as

$$A_2 = \frac{V_{REF\_M}}{\frac{1}{B}V_{REF\_M} + V_{OS1}} = \frac{1}{\frac{1}{B} + \frac{V_{OS1}}{V_{REF\_M}}} \quad (4.13)$$

The percentage deviation of the multiplication factor caused by  $V_{OS1}$ , becomes

$$\varepsilon_2 = \left( \frac{A_2}{A_0} - 1 \right) * 100\% = \left( \left( \frac{1}{1 + \frac{V_{OS1}}{V_{REF\_M}} B} \right) - 1 \right) * 100\% \quad (4.14)$$

Rewriting Equation (4.14), the maximal allowed offset of  $V_{OS1}$  for a particular accuracy will be

$$V_{OS1\_max} \Big|_{V_{OS2}=0, \Delta B=0, V_{OS3}=0, \Delta V_{REF\_S}=0} = \frac{V_{REF\_M}}{-B \left( 1 + \frac{100\%}{\varepsilon_2} \right)} = \frac{15.62mV}{-3.16 \left( 1 + \frac{100\%}{\varepsilon_2} \right)} \quad (4.15)$$

Translating the percentage error to the log conformance error by using the graph in Figure 4.10 we can construct the blue graph as shown in Figure 4.11. When we compare  $V_{OS1}$  and  $V_{OS2}$  in this graph, we can see that the fixation method is  $B$  times more sensitive to offset  $V_{OS1}$  than to  $V_{OS2}$ . More importantly, what we can learn from this graph is that the values of allowed offsets, for accuracy below 1dB, is small even when we consider only one of the offsets at a time. Especially offset  $V_{OS1}$  will limit the fixation system accuracy when we don't take care of this offset. In Chapter 5 it will be shown how the sensitivity to these offsets can be considerably lowered.

### Deviation in the attenuation factor of the divider block

Now we will look into the effect of a deviation in the multiplication factor caused by an error in the divider block. As shown by Figure 4.7 we will model this error by the parameter  $\psi_B$ .

Taking only this error into account Equation (4.6) can be rewritten as

$$A_3 = \frac{V_{REF\_A}}{\frac{1}{B(1+\psi_B)} V_{REF\_A}} = B(1+\psi_B) \quad (4.16)$$

The percentage error caused by a deviation in the divider block will be

$$\varepsilon_3 = \left( \frac{A_3}{A_0} - 1 \right) \cdot 100 = (\psi_B) \cdot 100\% \quad (4.17)$$

The maximal allowed relative error from wanted attenuation factor  $B$  for particular percentage accuracy, neglecting the other errors, can become

$$\Psi_{B\_max} \Big|_{V_{OS1}=0, V_{OS2}=0, V_{OS3}=0, \Delta V_{REF\_S}=0} = \frac{\varepsilon_3}{100\%} \quad (4.18)$$

Equation (4.18) shows that the attenuating factor is highly sensitive to a deviation in the multiplication factor. This observation is of course not that strange because the attenuation factor  $B$  itself is used to set the multiplication factor  $A$ . We have to note that in practice a divider block can be constructed with a relatively high precision, which means that this should not be the bottleneck to get a high accuracy fixation system.

### Mismatch between the two multiplication cells

The last error source to be discussed is the possible mismatch between the two multiplication cells,  $M_{REAL}$  and  $M_{COPY}$ .

In ideal case the loop will set the multiplication cells  $M_{copy}$  and  $M_{real}$  at identical multiplication factors. But in reality both cells will differ from each other due to process variations. So, we can expect a difference in the gain of both cells. As  $M_{real}$  is the cell that is doing the real multiplication operation of the log device input, we have to take the possible deviation between the two multiplication cells into account. As shown by Figure 4.7 the deviation is modelled by parameter  $\psi_A$ . The error in the multiplication factor caused by this deviation can be calculated by following equation

$$\varepsilon_{multiplication\_cell} = \left( \frac{A_{M_{copy}}}{A_{M_{real}}} - 1 \right) 100\% = \left( \frac{A_0}{A_0(1 + \Psi_A)} - 1 \right) 100\% \quad (4.19)$$

This equation shows that the error in the multiplication factor of the real multiplication cell is proportional to the percentage deviation between the gains of both cells.

#### 4.3.1.1.2 Error sources that alter the accuracy of the bias control system of the G/0 cells

Now that we have examined the error sources in the multiplication system we now will examine the error sources in the bias control system of the G/0 cells. This system including the error sources is shown at the right hand side of Figure 4.7

When assuming  $\beta_2 = \infty$  the operation of the bias control system can be described by the following equation.

$$\frac{1}{2}(1 + \psi_I) \frac{R_{S1} \alpha (1 + \psi_R) G E_K}{2} - V_{OS3} = V_{REF\_S} + \Delta V_{REF\_S} \quad (4.20)$$

Isolation of transconductance  $G$  results in

$$G = f_G(V_{REF\_S}, \Delta V_{REF\_S}, V_{OS3}) = \frac{4(V_{REF\_S} + \Delta V_{REF\_S} + V_{OS3})}{(1 + \Psi_I)R_{S1}\alpha(1 + \Psi_R)E_K} \quad (4.21)$$

This equation shows the dependency of the transconductance on the errors in the G/0 control system.

In the ideal case, i.e., if there are no errors, we can simplify Equation (4.21) to

$$G_0 = f_G(V_{REF\_S}, \Delta V_{REF\_S} = 0, V_{OS3} = 0, \Psi_\alpha = 0) = \frac{4V_{REF\_S}}{R_{S1}\alpha E_K} \quad (4.22)$$

Now that we have Equation (4.21) and Equation (4.22) we can start to examine the individual error contributions of the non-idealities to the deviation of the transconductance  $G$ .

### Deviation in reference voltage of OA2

The first non-ideality we will investigate is the possible deviation in the reference voltage  $V_{REF\_S}$ . When only the deviation in reference voltage  $V_{REF\_S}$  is taken into account the transconductance will be forced to

$$G_1 = \frac{4(V_{REF\_S} + \Delta V_{REF\_S})}{R_{S1}\alpha E_K} \quad (4.23)$$

The percentage error caused by the deviation will be

$$\varepsilon_4 = \left( \frac{G_1}{G_0} - 1 \right) 100\% = \left( \left( 1 + \frac{\Delta V_{REF\_S}}{V_{REF\_S}} \right) - 1 \right) 100\% \quad (4.24)$$

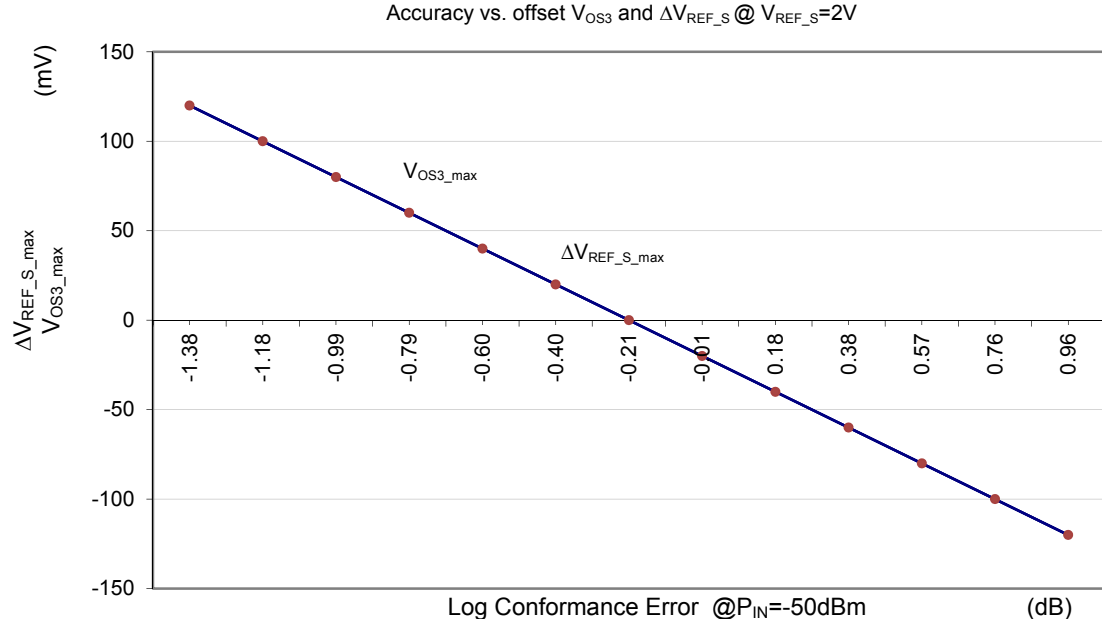
When we isolate  $\Delta V_{REF\_S}$  from this equation we will get

$$\Delta V_{REF\_S\_max} \Big|_{V_{OS1}=0, V_{OS2}=0, V_{OS3}=0, \Delta B=0} = \frac{\varepsilon_4 V_{REF\_S}}{100\%} \quad (4.25)$$

Equation (4.25) shows us that the allowed deviation of  $V_{REF\_S}$  is proportional to  $V_{REF\_S}$  itself. So, when  $V_{REF\_S}$  is chosen to be high, a higher deviation  $\Delta V_{REF\_S}$  is allowed, to still meet the accuracy requirements. At the end of Chapter 3 we have shown that by replacing resistor  $R_S$  by the two resistors,  $R_{S1}$  and  $R_{S2}$  the two outputs  $V_{OUT\_S}$  and  $\overline{V_{OUT}}$  can be set independently. With this feature it was shown that we can set  $R_{S2}$  to a higher value in comparison with  $R_{S1}$ , resulting in a higher slope information voltage  $V_{OUT\_S}$ , without changing the actual log detector output  $\overline{V_{OUT}}$ . As the wanted slope information voltage  $V_{OUT\_S}$  can be increased by the resistor ratio between  $R_{S1}$  and  $R_{S2}$ ,  $V_{REF\_S}$  can also be set to higher values. According to Equation (4.25) this will result in much less sensitivity to offset in the reference voltage. When, for example  $R_{S2}$  is set to a value such that



$V_{REF\_S}$  can be set to 2 volt, we can reach very low sensitivity in the log conformance error for deviations in  $V_{REF\_S}$  as shown by the blue curve in Figure 4.12



**Figure 4.12** Sensitivity of the accuracy for offset voltage  $V_{OS3}$  and deviation in reference voltage  $V_{REF\_S}$

### Input offset at OA2

Next, the sensitivity of the transconductance for the input offset at error amplifier OA2 is investigated. As shown by Figure 4.7 this is modelled by parameter  $V_{OS3}$ .

When we only include offset  $V_{OS3}$  in Equation (4.21) the transconductance will be forced to

$$G_2 = \frac{4(V_{REF\_S} + V_{OS3})}{R_{S1}\alpha E_K} \quad (4.26)$$

The percentage deviation in transconductance caused by offset voltage  $V_{OS3}$  will be

$$\varepsilon_5 = \left( \frac{G_2}{G_0} - 1 \right) 100\% = \left( \left( 1 + \frac{V_{OS3}}{V_{REF\_S}} \right) - 1 \right) 100\% \quad (4.27)$$

Isolation of  $V_{OS3}$  from Equation (4.27) leads to

$$V_{OS3\_max} \Big|_{\Delta V_{REF\_S}=0, \Psi_B=0, V_{OS1}=0, V_{OS2}=0, \Psi_R=0} = \frac{\varepsilon_5 V_{REF\_S}}{100\%} \quad (4.28)$$

$V_{OS3}$  shows exactly the same sensitivity to system accuracy as it was for a deviation in  $V_{REF\_S}$ . The maximum allowed  $V_{OS3}$ , to meet a required accuracy also depends on the magnitude of  $V_{REF\_S}$ . As we know from the previous discussion,  $V_{REF\_S}$  can be chosen to be relatively high, which means that the dependency on the system accuracy for  $V_{OS3}$  can be made very low. When we for

example chose again  $V_{REF\_S}$  is 2 volt, the sensitivity to the log conformance will be as indicated by the red dotted graph in Figure 4.12. This graph shows that the offset voltage  $V_{OS3}$  will show exactly the same small sensitivity to the log conformance as it was for the deviation in  $V_{REF\_S}$

### Deviation in the expected ratio between resistors $R_{S1}$ and $R_{S2}$

Apart from the property to drastically lower the sensitivity to offset and deviation in  $V_{REF\_S}$  by implementing two separate resistors, we have to consider the possible deviation in the expected ratio between the two resistors,  $R_{S1}$  and  $R_{S2}$ . The mismatch will result in a deviation from the expected ratio. From Equation (3.31) and Equation (3.32) we know that in the ideal case  $R_{S2} = \alpha R_{S1}$ , where  $\alpha$  is the wanted resistance ratio between both resistors. When the ratio is not  $\alpha$ , but  $\alpha(1+\psi_R)$  we can construct the equation to calculate the percentage error caused by a deviation from the expected ratio,

$$\varepsilon_{\alpha R} = \left( \frac{\left( \frac{4(V_{REF\_S})}{R_{S1}\alpha(1+\Psi_R)E_K} \right)}{\left( \frac{4(V_{REF\_S})}{R_{S1}\alpha E_K} \right)} - 1 \right) 100\% = \left( \frac{1}{(1+\Psi_R)} - 1 \right) 100\% \quad (4.29)$$

From this we can conclude that the sensitivity of the transconductance is proportional to the error in the wanted ratio between resistor  $R_{S1}$  and  $R_{S2}$ . In Chapter 5 it will be shown that the resistors, when proper layout techniques are used, are expected to match very closely.

### Splitting error of the current divider

The last error to be considered is the possible deviation in splitting operation of the current splitter. As already indicated earlier and shown in Figure 4.7, this error will be modelled by parameter  $\psi_I$ .

With the same analysis procedure used earlier we can develop the following equation for the percentage error in the current division

$$\varepsilon_I = \left( \frac{\left( \frac{4(V_{REF\_S})}{(1+\Psi_I)R_{S1}\alpha E_K} \right)}{\left( \frac{4(V_{REF\_S})}{R_{S1}\alpha E_K} \right)} - 1 \right) 100\% = \left( \frac{1}{(1+\Psi_I)} - 1 \right) 100\% \quad (4.30)$$

From this we can conclude that the sensitivity of the deviation in transconductance  $G$  is proportional to the percentage deviation in the wanted 50% current division.

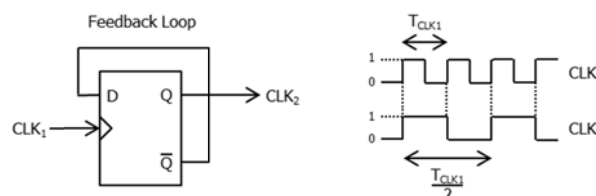
## 5 Implementation of the logarithmic transfer stabilization method

In this chapter we will discuss the most critical parts of the circuit implementation of the logarithmic transfer stabilization method.

### 5.1 Clock circuitry

From the final system overview as was shown in Figure 3.22 it can be seen that we have to use two different clock signals,  $CLK_1$  and  $CLK_2$ . From the same figure we can see that  $CLK_1$  is working at twice the frequency of  $CLK_2$ .

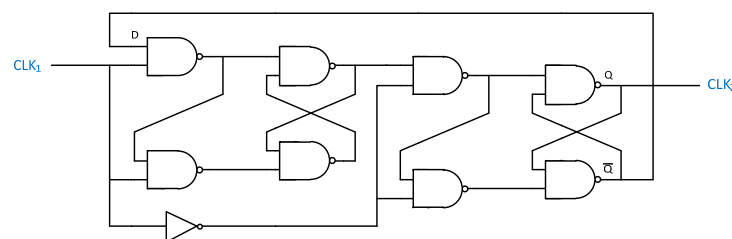
To generate a clock signal that has a frequency which is half of a faster clock signal a so-called clock divider is used. The faster clock signal will originate from an oscillator output with an accurate duty cycle of 50% while the slower clock signal will be generated from the faster clock signal by using a basic clock divider. The most basic clock divider is the so-called Toggle Flip Flop (T-FF). The architecture of the T-FF is shown in Figure 5.1a



**Figure 5.1** Data Flip Flop configured as Toggle Flip Flop to operate as clock divider

The architecture of this T-FF consists of a so-called D-Flip Flop (D-FF), with its  $D$  input fed from its own inverted output. A D-FF copies the value at the data input terminal  $D$ , on every rising edge of the input clock, to the data output  $Q$ . Because we feed back the inverse of this output, the flip-flop will toggle on every rising edge of the input clock signal, resulting in a square wave output with half the frequency of the input clock,  $CLK_1$ . Figure 5.1b shows the two resulting synchronized control signals,  $CLK_1$  and  $CLK_2$ , both having a duty cycle of 50%. The input signal and the output signal of the D-FF can be used for controlling the switches of the system as was shown in Figure 3.22

In Figure 5.2 the system diagram of the clock divider is shown.



**Figure 5.2** System diagram of the clock divider

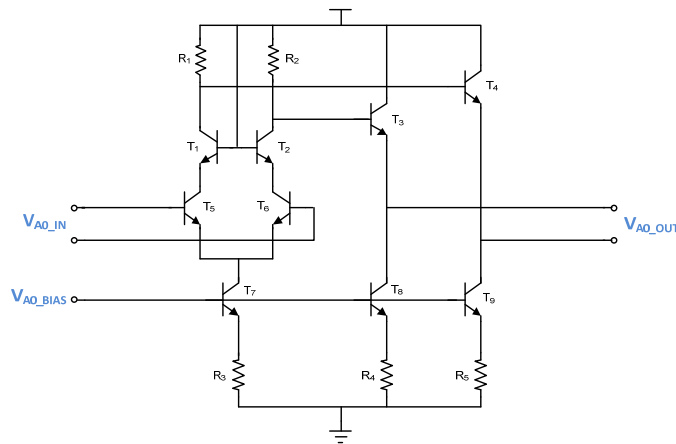
## 5.2 Multiplication/gain fixing circuitry

In this section we will discuss the implementation of the system which is used to fixate the multiplication action of  $M_{\text{REAL}}$  and the small signal gain of the cascaded A/O cells. In 5.2.1 we will focus on a simplified circuit implementation of the multiplication cell  $M_{\text{REAL}}$ , which will be later modified to the final multiplication cell implementation as will be discussed in Subsection 5.2.6. In 5.2.2 the implementation of the divider block will be discussed. This subsection will be followed by subsections in which we will discuss the implementation of the error amplifier and its negative feedback configuration. In these sections we will also introduce the so-called chopper stabilization technique, which is used to reduce the sensitivity of the fixation system to input offset voltages. As this technique results in a modulated output signal, it will be shown that a low pass filter is needed to convert the rippled output signal into a useful DC bias voltage. We have dedicated one subsection to the implementation of a new filter concept which can be used to completely remove the ripple from the modulated output signal. The filter, which can be called a synchronized switched capacitor notching filter, uses control signals. The system used to generate these control signals will be discussed in a separate subsection. Thereafter a modification to the system will be discussed which is used to increase the common-mode rejection of the system. And finally in subsection 5.2.6 the fixation system will be extended to its final implementation. We will propose in the last section an switching architecture to switch  $M_{\text{REAL}}$  between two bias conditions to obtain the fixed multiplication action of the RF input signal

### 5.2.1 The multiplication cell (A/O cell)

In Section 2.3.2 we already introduced the basic A/O cell which was based on the architecture of a bipolar differential pair. As stated in earlier sections the A/O cell architecture will not only be used for the limiting gain stages in the cascade of the successive approximation log detector but also for  $M_{\text{COPY}}$ , and the multiplication cell,  $M_{\text{REAL}}$ , itself.

In this section we will discuss a simplified A/O cell architecture. As will be shown it will be a modified version of the one discussed in Section 2.3.2. However this will not be the final implementation. In section 5.2.6 the final implementation which we used for testing will be discussed. Figure 5.3 shows the simplified multiplication cell architecture.



**Figure 5.3** The circuit implementation of the multiplication cell (A/O cell)

Transistor  $T_7$  together with  $R_3$  is used as current source, and provides the tail current for transistor pair  $T_5$ - $T_6$ . As was shown in Figure 3.12 the A/O cells share the same voltage node for biasing. This means that the base of each A/O current source will be driven from the same node. To ensure accurate matching of the tail currents of all those A/O cells an emitter degeneration resistor  $R_3$  is placed. Besides providing better matching the degeneration resistor also raises the output resistance of the current source.

To enlarge the driving capability of the differential pair at higher frequencies, the differential pair, which in essence comprises two emitter coupled CE stages in a differential fashion, are loaded by common base stages  $T_1$  and  $T_2$ . With the knowledge that a CB stage has a low input impedance and high output impedance, the loading of a CE stage by an CB stage instead of the resistors  $R_1$  or  $R_2$ , considerably increases the cut-off frequency of the circuit.

As already stated in Section 2.3.2 a favourable property of the A/O cell based on the bipolar differential pair is when configured for normal values of gain (for example 10dB) they can be easily DC-coupled and cascaded without saturation problems. However, as can be seen from the final A/O architecture we added emitter follower buffers  $T_3$ - $R_4$  and  $T_4$ - $R_5$  at the output. One beneficial property of the emitter-followers is that the output impedance of the A/O cell will be improved. This will make the gain less sensitive to the mismatch and temperature-dependence of the current gain factors of consecutive bipolar transistors. In our situation this will improve the gain match between the multiplication cells  $M_{\text{COPY}}$  and  $M_{\text{REAL}}$ , as it will decrease the sensitivity to the different loading conditions between both cells. When looking at the level shifting property of the emitter followers it can also be seen that the bandwidth of the cascaded A/O cell structure will usually be higher, because it leads to an higher collector base voltage of the input pair of the preceding A/O cells. However, a disadvantage of including the emitter followers will be their extra power consumption.

One may have noticed that during the explanation of the fixation system we didn't use the differential form of the A/O cell's. As will become clear in following sections the actual system will be in differential form.

## 5.2.2 The divider block

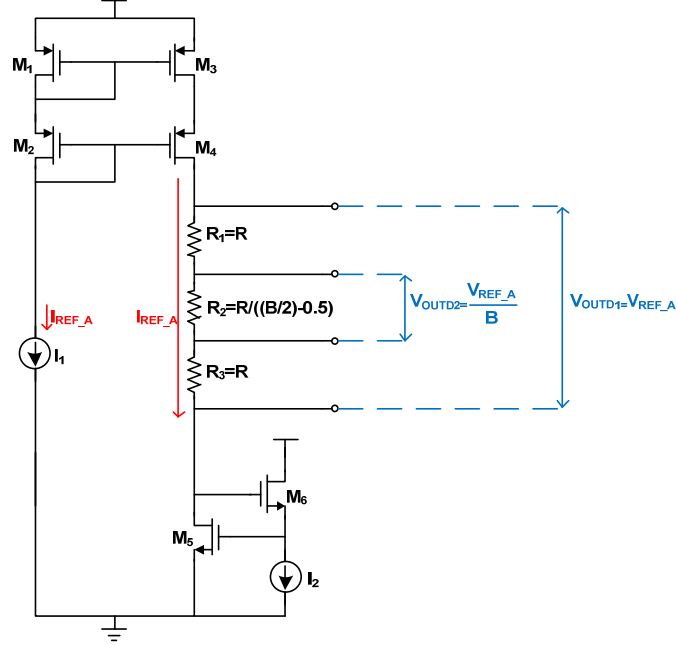
In this section we will discuss the divider block. From earlier sections it was shown that the divider block is used to produce an output voltage that is a known and fixed fraction of the reference voltage,  $V_{\text{REF\_A}}$ . In foregoing sections this fraction was called the attenuating factor  $B$ . Furthermore, in Section 3.2.1, we showed by Equation (4.18) that the wanted multiplication factor of  $M_{\text{copy}}$  is set by this attenuating factor. In same section it was shown that the accuracy of the multiplication factor depends on how accurate the attenuation factor can be set. So it is important to design a divider block that has a precise attenuation factor  $B$ .

As noted in the previous subsection, we actually deal with a differential form of the fixation system. This means that our system needs a differential reference voltage  $V_{\text{REF\_A}}$  from which the divider block has to generate the differential reference voltages  $V_{\text{REF\_A}}/B$ .

### 5.2.2.1 Circuit implementation

In this subsection we will discuss the circuit implementation of the divider block.

The proposed circuit architecture of divider block is shown in Figure 5.4.



**Figure 5.4** Circuit implementation of the divider block

In short the circuit operation can be explained as follows. The circuit consists of a current source which delivers a reference current  $I_{REF\_A}$  to a cascoded current mirror. The current mirror supplies the mirrored reference current to a resistive voltage divider to set the output voltages of the divider. A common mode voltage adjustment circuit is placed to set the common mode voltages of the differential output voltages. Later it will be shown that the common mode adjustment circuit can be made self-controllable by means of a feedback signal extracted from the error amplifier OA1 that will control current source  $I_2$ .

After this brief explanation we now will discuss the circuit in more detail

#### 5.2.2.1.1 The resistive ladder

The main building block inside the divider block is the resistive ladder. As shown in Figure 5.4 the resistive ladder consists of 3 resistors connected in series. The resistive ladder is used as voltage divider and will set the attenuation factor.

As we deal with the differential form, the attenuation factor  $B$  has to be defined by the ratio between the two differential output voltages,  $V_{OUTD1}$  and  $V_{OUTD2}$ .

$$B = \frac{V_{OUTD1}}{V_{OUTD2}} \quad (5.1)$$

where

$$V_{OUTD1} = V_{REF\_A} \quad (5.2)$$

and

$$V_{OUTD2} = \frac{V_{REF\_A}}{B} \quad (5.3)$$

These two differential output voltages are generated by configuring the resistors of the voltage divider to

$$R_2 = \frac{R}{\frac{B}{2} - 0.5} \quad (5.4)$$

and

$$R_1 = R_3 = R \quad (5.5)$$

such that the total series resistance is  $B$  times higher than that of the middle resistor,  $R_2$ . By sending the current  $I_{REF\_A}$  through this configuration it is not difficult to see that this will result in two differential output voltages with a ratio of  $B$ .

#### 5.2.2.1.2 The reference current

Figure 5.4 shows that the reference current  $I_{REF\_A}$  is delivered by current source  $I_1$  and is mirrored by the cascoded current mirror consisting of  $M_1$ - $M_4$ . The cascoded current mirror will be necessary to make the reference current of the ladder less dependent of the upper node voltage of the ladder.

When we assume that the current  $I_{REF\_A}$  is sent through the full resistive ladder (no loading effects), the ratio between the two differential voltages  $V_{OUTD1}$  and  $V_{OUTD2}$  can be calculated as follows.

$$\frac{V_{OUTD1}}{V_{OUTD2}} = \frac{R \cdot I_{REF\_A} + \left( \frac{B}{2} - 0.5 \right) \cdot I_{REF\_A} + R \cdot I_{REF\_A}}{\frac{R}{\left( \frac{B}{2} - 0.5 \right)} \cdot I_{REF\_A}} = B \quad (5.6)$$

As shown by Equation (5.2) the resulting ratio between both differential voltages is exactly the wanted attenuation factor  $B$ . The magnitude of  $I_{REF\_A}$  seems not to be that important for the ratio, however there is an issue that has to be taken into account.

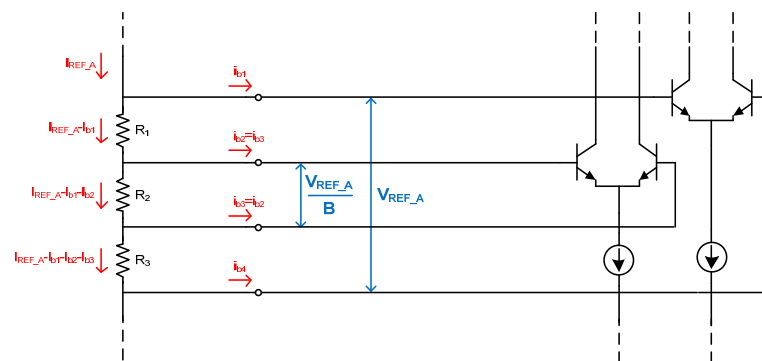
As will become clear in Section 5.2.3 the differential output voltage  $V_{OUTD1}$  will be used to provide the input voltage of a so-called DDA (till now indicated by OA1) while the differential voltage  $V_{OUTD2}$  will be used to provide the input voltage of the multiplication cell  $M_{copy}$ . From Section 3.2.1. we know that the input voltage of  $M_{copy}$  is limited to a maximum voltage of around 5mV to ensure its linear operation. So, this means that for our divider block the current  $I_{REF\_A}$  and the value of  $R_2$  should be chosen in such a way that the voltage  $V_{OUTD2}$  does not exceed this 5 mV. This shows that there is a limitation on the magnitude of the reference current, which depends on the resistor values of the resistive ladder. The resistors values itself should be chosen low to obtain low resistance output impedance seen by the preceding voltage amplifier stages.

### 5.2.2.1.3 Common mode range bias

As explained in the previous subsection the differential outputs of the resistive ladder will be loaded by  $M_{COPY}$  and error amplifier OA1. To shift the differential output voltages  $V_{OUTD1}$  and  $V_{OUTD2}$  into the input common mode range of the multiplication cell  $M_{copy}$  and OA1, transistors  $M_5$ ,  $M_6$  and current source  $I_2$  were added. It can be seen that the common mode voltage in this arrangement will be set by the sum of the gate-source voltages of  $M_5$  and  $M_6$ . The gate-source voltage of  $M_5$  is determined by the reference current  $I_{REF\_A}$  and the dimensions of  $M_5$ , while the gate source voltage of  $M_6$  is determined by the current delivered by current source  $I_2$  and the dimensions of  $M_6$ . Later it will be shown that this current source can be replaced by a controlled current source, which than can be used to enhance the so-called CMRR of the system.

### 5.2.2.2 Loading effect

As the multiplication cell,  $M_{copy}$ , and OA1 are loading the two differential output ports of the divider block the effect of their input impedance has to be investigated. We already know that  $M_{copy}$  has BJT input pairs. In the following section it will be shown that also the input stage of the OA1 will consist of BJT input pair. When dealing with BJT's the finite beta (or finite input impedance) has to be taken into account. Because of the finite beta of these BJT's we have to deal with base currents which will affect the current that goes through each resistor of the resistive ladder. This effect is shown by Figure 5.5



**Figure 5.5** Current through resistive voltage divider is effected by the beta's of the bipolar loads

From Figure 5.5 it looks like the currents flowing through each individual resistor will considerably affect the ratio between the two differential output voltages. But it can be shown that because of its configuration the voltage divider proposed here is not that sensitive to the base currents of the bipolar loads.



To show this we have to rewrite equation 5.2 to following equation.

$$\frac{V_{OUTD1}}{V_{OUTD2}} = \frac{R \cdot (I_{REF\_A} - I_{b1}) + \frac{R}{\frac{B}{2} - 0.5} \cdot (I_{REF\_A} - I_{b1} - I_{b2}) + R \cdot (I_{REF\_A} - I_{b1} - I_{b2} - I_{b3})}{\frac{R}{\frac{B}{2} - 0.5} \cdot (I_{REF\_A} - I_{b1} - I_{b2})} \quad (5.7)$$

This equation can be simplified to

$$\frac{V_{OUTD1}}{V_{OUTD2}} = \frac{I_{REF\_A} - I_{b1} - I_{b3}}{I_{REF\_A} - I_{b1} - I_{b2}} \left( \frac{B}{2} - 0.5 \right) + 1 + \left( \frac{B}{2} - 0.5 \right) \quad (5.8)$$

From this equation we can see that the ratio  $V_{OUTD1}/V_{OUTD2}$  is independent from the base currents  $i_{b1}$  and  $i_{b4}$ . This does not hold for the base currents  $I_{b2}$  and  $I_{b3}$ . However, when we for example assume that  $V_{OUTD2}$  is almost zero and loaded by an ideal differential input pair, the base current  $i_{b3}$  can be assumed to be almost equal to  $i_{b2}$ . With this assumption Equation (5.4) tells us that the ratio of the two differential voltages will closely match to the wanted attenuation factor  $B$ . Of course the almost zero differential voltage assumption is not a realistic assumption. However, the input of the multiplier cell  $M_{copy}$  will be provided by a voltage of not more than 5mV, which still can be assumed to be relatively small. As the voltage difference at the input is limited to 5 mV and the gain of  $M_{copy}$  will be relatively low (will be forced to be equal to  $B$ ) the base current difference between  $I_{b2}$  and  $I_{b3}$  can be expected to be relatively small. From Equation 5.4 we can also see that the sensitivity to the difference in base currents can be lowered by increasing the current  $I_{REF\_A}$ . A disadvantage of the increase of  $I_{REF\_A}$  will be the increase of power consumption. Furthermore we have to note that for an increase of  $I_{REF\_A}$  the resistor values of the ladder have to be lowered because of the 5mV input limit of  $M_{copy}$ .

One would notice that we also could choose for MOS input pairs instead of BJTs, as MOS transistors don't have a gate current at DC input voltages. But as discussed earlier the A/0 cells are chosen to be BJT input pairs to obtain the tanh transfer. Furthermore there are several advantages to choose for BJTs input pair for the implementation of error amplifier OA1 as will be discussed later.

### 5.2.2.3 Resistor mismatch

The resistive voltage divider is an extremely simple circuit which can be used to obtain a very accurate attenuation factor. The level of accuracy depends on the layouting technique used. This is because the accuracy of the resistive voltage divider is determined by the matching of the ratio of the resistors instead of the absolute values of the resistors. The absolute value of on chip resistors cannot be accurately determined. Depending on the type of resistor used, the absolute value of the resistor may be off as much as 40% [54]. Fortunately in case of a resistive divider the accuracy is determined by the ratio (or matching) accuracy of resistors. The ratio accuracy between resistors can be high because it will only depend on the local variation of parameters, which in sub-micron IC technology can be very small. With proper layout techniques the

sensitivity to these local variations can be minimized such that the mismatch between two resistances can be as low as 0.1% [55] .

To improve matching of resistors the following layouting techniques can be used [55]:

- Construct matched resistors from a single material
- Make matched resistors the same width
- Make matched resistors sufficiently wide
- Place matched resistors in close proximity
- Interdigitated arrayed resistors
- Place dummies on either end of a resistor array
- Avoid short resistor segments
- Where practical, use identical geometries for resistors
- Orient matched resistor in the same direction
- If possible, place matched resistors in low stress areas
- Place matched resistors well away from power devices
- Use poly resistors in preference to diffused ones
- Choose P-type poly resistors in preference to N-type poly resistors

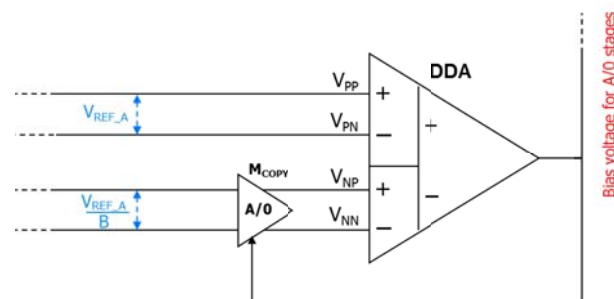
As an extra note we can point out an interesting observation. As the two differential outputs of our proposed divider block share the resistor  $R_2$ , the sensitivity to mismatch is decreased.

### 5.2.3 The error amplifier

In this section we will describe the implementation of the error amplifier (indicated by OA1 in previous sections). From previous chapters we know that this amplifier will be responsible for biasing the multiplier cell  $M_{copy}$  in such a way that it fixes the gain (multiplication factor) of  $M_{copy}$ . A matched duplicate of  $M_{copy}$ , called  $M_{real}$  which uses the same bias will then be used for the actual multiplication of the RF input signal.

In previous sections, we have shown that the fixation of the multiplication factor is accomplished by the negative feedback configuration of the error amplifier. Or more precisely, OA1, which is part of a negative feedback system, will control the bias of  $M_{copy}$  such that the multiplication factor or gain of  $M_{copy}$  is forced to be equal to the attenuation factor  $B$  of the divider block.

#### 5.2.3.1 The DDA used as error amplifier



**Figure 5.6** The negative feedback configuration of the Differential Difference Amplifier (DDA)

In Figure 5.6 a more detailed picture of the proposed feedback system is shown. As shown the two differential output voltages  $V_{REF\_A}$  and  $V_{REF\_A}/B$  of the divider block, which was described in a previous section, are used as inputs of the feedback system.

As was already discussed in previous sections we are dealing with a differential form of the system. Therefore the feedback system differs from the simplified system topology as was shown in Figure 3.22. Because of the differential structure of the system the operational amplifier (op-amp) OA1, used in previous sections, is replaced by a so-called Differential Difference Amplifier (DDA) [56]. The feedback operation of the DDA is similar to that of the op-amp, but there are some differences which have to be taken into account. For instance, we know that a classical op-amp acts as a device which, if completed with a negative feedback loop, adjusts its output in order to reduce its differential input voltage to a negligible value. When assuming the op-amp to be ideal, the infinite gain will force this input voltage to zero.

This means that when calling the non-inverting input  $V_P$  and the inverted input  $V_N$  the operation principle of the ideal op-amp can be described with following equation

$$V_P = V_N \quad (5.9)$$

This equation shows that the op-amp operation is useful when we want to compare two single-ended input voltages. But, since we are dealing with two differential input voltages, the single op-amp configuration is not useful. To compare two differential inputs the so-called DDA is more practical. The symbol of the DDA is shown in Figure 5.6. As can be seen the DDA has 4 input terminals. The two input terminals denoted by  $V_{PP}$  and  $V_{PN}$  form the non-inverting differential input port, and the input terminals  $V_{NP}$  and  $V_{NN}$  form the inverting differential input port.

The operation of the DDA is to amplify the difference between its two differential input voltages as described by the following equation

$$V_{OUT\_DDA} = A_0((V_{PP} - V_{PN}) - (V_{NP} - V_{NN})) \quad (5.10)$$

Where  $A_0$  is the open loop gain of the DDA. For an ideal DDA this open loop gain will be infinite. In this ideal situation the difference between the differential voltages will be amplified by an infinite amount. When completed with a negative feedback loop, it will adjust its output in order to reduce the difference between the two differential input voltages to zero. Thus, when  $A_0$  approaches infinity the operation principle of the DDA with negative feedback can be described by

$$V_{PP} - V_{PN} = V_{NP} - V_{NN} \quad (5.11)$$

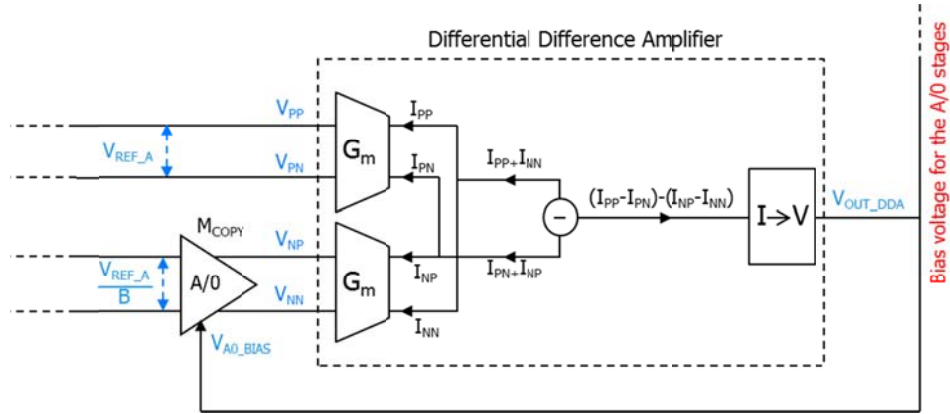
Here we can see that, instead of comparing two single-ended input voltages, as it was for a classical op-amp, the DDA can be used to compare two differential input voltages.

An issue that has to be taken into account is the difference between the differential input condition at a normal opamp and that of the differential inputs of the DDA when used in negative feedback configuration. [57]

When an op-amp is used in negative feedback configuration, its differential input is always operating at a differential voltage close to zero. The transconductance of the differential input pair in this situation will therefore be approximately  $g_m$ . This property doesn't hold for the DDA.

As was shown by Equation (5.11), the DDA in feedback configuration forces the differential voltage  $V_{NP}-V_{NN}$  to be equal to  $V_{PP}-V_{PN}$ . This means in our system that both differential inputs will be operating at differential voltage equal to  $V_{REF\_A}$  instead of an almost zero differential input voltage. So our DDA has to deal with non-zero differential input voltages. As will be shown in following sections the DDA will also consist of differential input pairs. Because of the non-zero differential voltages the non-linearity of both differential stages has to be taken into account. From section 3.2.1 it was shown that due to the non-linearity of a differential pair an increase of the input differential voltage will result in a reduction of the transconductance. As a result of this transconductance reduction it may significantly degrade the open loop gain of the DDA.

### 5.2.3.2 System level operation of the DDA in the feedback loop



**Figure 5.7** Detailed block diagram of the gain fixation system

Figure 5.7 shows again a block diagram of the negative feedback configuration, but now it also includes the internal operation structure of a basic DDA. Using this block diagram, the operation of the differential comparison principle of the DDA can be shown.

As shown by Figure 5.7, the input of the DDA consists of two transconductance cells. These two transconductance cells are used to convert the floating differential voltages  $V_{PP}-V_{PN}$  and  $V_{NP}-V_{NN}$  into two differential output currents. Then, because of the direct and cross connection of the two differential current outputs, the two currents  $I_{PP}+I_{NN}$  and  $I_{PN}+I_{NP}$  are generated. These two currents are then subtracted by a subtraction element resulting in the single-ended current  $(I_{PP}+I_{NN})-(I_{PN}+I_{NP})$ , which can be rearranged to  $(I_{PP}-I_{PN})-(I_{NP}-I_{NN})$  as indicated by Figure 5.7. This current is then converted by a trans-impedance block to the DDA's output voltage  $V_{OUT\_DDA}$ . As shown by Figure 5.7 this output voltage is fed back to the bias node of the gain stage  $M_{COPY}$ , such that  $V_{A0\_BIAS}$  equals  $V_{OUT\_DDA}$ . Because of the negative feedback configuration, the bias voltage  $V_{A0\_BIAS}$  will be forced to a value such that the input  $V_{NP}-V_{NN}$  satisfies the condition of Equation 5.7.

As the voltage at the positive input port of the DDA is  $B$  times higher than that of the input of  $M_{COPY}$  the condition of Equation (5.11) will only be true for a bias value which sets the multiplication factor  $A$ , of  $M_{COPY}$ , equal to the attenuation factor  $B$  as indicated by

$$V_{PP} - V_{PN} = V_{NP} - V_{NN} \Rightarrow V_{REF\_A} = \frac{V_{REF\_A}}{B} A \quad (5.12)$$

### 5.2.3.2.1 Loop gain of the feedback configuration

The high loop-gain, necessary for accurate comparison of both differential inputs, can be obtained by choosing high conversion factors for the transconductance and transimpedance blocks. But, these are not the only parameters that contribute to the loop gain; in addition there is actually another loop gain parameter. The loop gain also depends on the conversion factor of the internal bias source inside  $M_{COPY}$ , since it is also part of the loop.

For example, when we assume that the internal structure of  $M_{COPY}$  is a simple bipolar architecture as was shown in Figure 2.10 and take the knowledge from Figure 5.7 that its input is defined by  $V_{REF\_A}/B$  and the output by the differential voltage  $V_{NP}-V_{NN}$  we can rewrite Equation (2.27) to

$$V_{NP} - V_{NN} = R_C I_t \tanh \left( \frac{\left( \frac{V_{REF\_A}}{B} \right)}{2V_T} \right) \quad (5.13)$$

in which the tail current of  $M_{copy}$  is defined as

$$I_t = I_S e^{\frac{V_{BE}}{V_T}} = I_S e^{\frac{V_{A0\_BIAS}}{V_T}} \quad (5.14)$$

Inserting Equation (5.14) into Equation (5.13) leads to

$$V_{NP} - V_{NN} = R_C I_S e^{\frac{V_{A0\_BIAS}}{V_T}} \tanh \left( \frac{\left( \frac{V_{REF\_A}}{B} \right)}{2V_T} \right) \quad (5.15)$$

By taking the derivative to the bias voltage,  $V_{A0\_BIAS}$ , the extra gain delivered by the conversion factor of internal current source of  $M_{copy}$  can be calculated

$$\frac{d(V_{NP} - V_{NN})}{d(V_{A0\_BIAS})} = \frac{1}{V_T} R_C I_S e^{\frac{V_{A0\_BIAS}}{V_T}} \tanh \left( \frac{\left( \frac{V_{REF\_A}}{B} \right)}{2V_T} \right) \quad (5.16)$$

This equation shows that the additional gain to the overall loop gain equals the output voltage of  $M_{COPY}$  divided by the thermal voltage  $V_T$ .

As our system forces the output voltage of  $M_{COPY}$  to be equal to the reference voltage  $V_{REF\_A}$ , Equation (5.16) can be simplified to

$$\frac{d(V_{NP} - V_{NN})}{d(V_{A0\_BLAS})} = \frac{V_{REF\_A}}{V_T} \quad (5.17)$$

This shows that the additional gain is proportional to  $1/PTAT$ . Furthermore, the higher the reference voltage, the higher the loopgain will be. For a temperature of for example  $27^\circ\text{C}$  and a  $V_{REF\_A}$  of  $15.62\text{mV}$ , an additional loopgain of approximately 0.58 times is contributed to the overall loopgain. This last observation shows that the conversion factor of the internal current source actually leads to a decrease of the overall loop gain.

### 5.2.3.3 The importance of matched input transconductance cells

For the derivation of Equation (5.10) we assumed that the differential transconductance stages were identical to each other. This implies that this equation can be used, even when the transconductance of both identical stages are non-linear and time or temperature dependent. This shows that, apart from the loop gain, the system will work properly as long as they are identical to each other. Thus it is critical for proper operation of a DDA to match the transconductances of both input stages as accurately as possible.

When we deal with differential stages which are not identical to each other and exhibit different gains  $A_P$  and  $A_N$  Equation (5.10) has to be rewritten as

$$V_{OUT\_DDA} = A_P(V_{PP} - V_{PN}) - A_N(V_{NP} - V_{NN}) \quad (5.18)$$

From [56] it can be shown that, when  $A_P \neq A_N$ , it will lead to a reduction of the common mode rejection CMRR.

### 5.2.3.4 CMRR of the DDA

When talking about the common mode rejection of the DDA we can actually distinguish three CMRRs. The actually non-linear output voltage of the DDA including all CMRR components can be written as follows after linearization [56]:

$$V_{OUT\_DDA} = A_0[(V_D - V_{off}) + \frac{1}{CMRR_P}(V_{CP} - V_{CP0}) + \frac{1}{CMRR_N}(V_{CN} - V_{CN0}) + \frac{1}{CMRR_D}(V_{CD} - V_{CD0})] \quad (5.19)$$

where

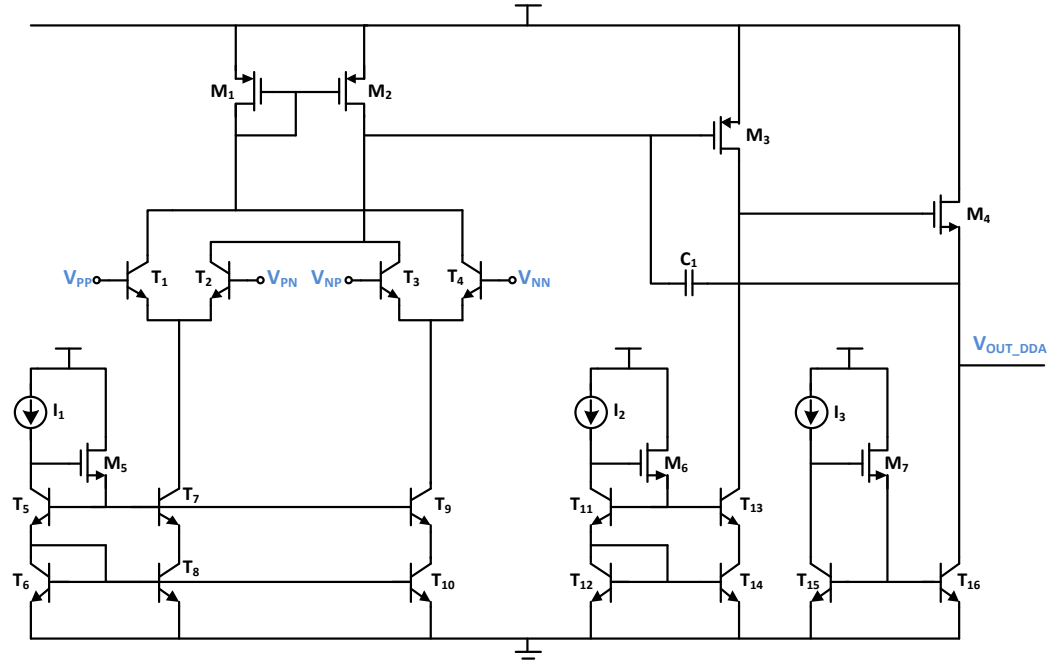
$$V_D = (V_{PP} - V_{PN}) - (V_{NP} - V_{NN}) \quad (5.20)$$

represents the voltage difference between the two differential input voltages of the DDA,  $V_{off}$  the offset voltage at the input of the DDA.  $V_{CP0}$  and  $V_{CN0}$  represent the common-mode voltages at the linearization point for the Positive and Negative input ports of the DDA respectively. Furthermore  $V_{CD0}$  represent the equal floating voltages at the two input ports and  $V_{CP}$ ,  $V_{CN}$  and  $V_{CD}$  are the deviations from  $V_{CP0}$ ,  $V_{CN0}$  and  $V_{CD0}$ . The P- and N-common-mode rejection ratios ( $CMRR_P, CMRR_N$ ) in Equation (5.19) describe the effect of the common mode voltages at the two input ports, whereas the D-common-mode rejection ratio ( $CMRR_D$ ), measures the effect of equal floating voltages at the two input ports of the DDA. While the dependence of  $CMRR_P$ ,  $CMRR_N$  are well known from the ordinary op amp, the  $CMRR_D$  is not. This parameter originates from the DDA structure and depends on the matching of the transfers of both differential stages. From [56] it was shown that this common mode error leads to a constant closed loop gain error. To lower the effect of this error one could take a higher loopgain but better is to go for a proper circuit implementation to match the transfers of both differential stages.

### 5.2.3.5 Circuit implementation of the DDA

In previous section we have discussed the basic DDA operation at system level and showed some differences between the operation of an op-amp and a DDA, which were important to know before we start to implement a DDA at transistor level. Now that we have discussed the characteristics of the DDA we can focus on the circuit implementation of the DDA. In this section we start with an introduction of a simplified circuit implementation, which will form the basis for the more complex DDA circuit that can fulfil the accuracy requirements as were discussed in Section 4.3. The more complex circuit will be discussed in a later section.

Figure 5.8 shows the simplified circuit architecture of the implemented DDA.



**Figure 5.8** Simplified circuit architecture of the used DDA implementation

As shown in Figure 5.8 the circuit consists of two differential input stages  $T_1-T_2$  and  $T_3-T_4$  both biased by a cascoded current source  $T_7-T_{10}$ . The differential input stages are cross-connected and loaded by the active load  $M_1-M_2$ . A transimpedance stage is implemented by a standard integrator

architecture, consisting of a gain stage  $M_3$ , which is biased and loaded by a cascode current source ( $T_{13}, T_{14}$ ), a buffer stage ( $M_4$ ) which is biased and loaded by a current source ( $T_{16}$ ) and a feedback capacitor ( $C_1$ ). In the following sections the circuit will be discussed in more detail.

### 5.2.3.5.1 The differential input stages

The two differential inputs stages  $T_1$ - $T_2$  and  $T_3$ - $T_4$  in Figure 5.8 form the transconductance blocks, as was shown in the system diagram of Figure 5.7. As shown in Figure 5.8 we have chosen bipolar junction transistors (BJTs) as our differential inputs. The reason not to choose MOS but BJT transistors depends on several characteristics that are essential when considering differential input stages. The most important are the input offset voltage, matching, transconductance, input impedance, frequency response, and noise contribution.

Let's first look at the input offset. In Section 4.3.2 the importance of low input offset in our multiplication fixation system was shown. It was shown that the offset degrades the accuracy of the multiplication fixation system considerably. So it is very important to choose the right input device when aiming for low offset.

First let's consider the input offset voltage of BJTs. For a BJT differential stage the input offset can be described by following equation [58]

$$V_{IO} = \left( \frac{kT}{q} \right) \ln \left( \frac{I_{C1}}{I_{C2}} \cdot \frac{I_{S2}}{I_{S1}} \right) \quad (5.21)$$

The error introduced in Equation (5.21) by the  $I_C$  terms is due to the mismatch in the different loads seen at both collectors of the input transistors. The error by the  $I_S$ -terms is mainly due to mismatches in the area of the emitter and the width and doping of the base. The value of  $kT/q$  is temperature dependent (e.g., approximately 26 mV at 27 °C). This term has the largest influence on the input offset and its drift with temperature. The offset drift over time is low for bjt input stages and typically ranges from a few uV/month down to a few nV/month [58].

For an MOS differential pair the input offset can be described by following equation

$$V_{IO} = (V_{TH1} - V_{TH2}) + \sqrt{\left( \frac{2 \cdot I_{D1}}{\mu C_{OX}} \cdot \frac{L_1}{W_1} \right)} - \sqrt{\left( \frac{2 \cdot I_{D2}}{\mu C_{OX}} \cdot \frac{L_2}{W_2} \right)} \quad (5.22)$$

As shown by this equation the input offset for MOS differential pair is primarily due to difference in the threshold voltage,  $V_{TH}$ , caused by variation in the width, length, thickness and doping levels of the channel in the transistors [58]. Typically, the offset drift over time is of the order of nano volts per month.

The primary reason we have chosen BJTs as input is that MOS transistors are more sensitive to layout mismatch in terms of their threshold voltage (for BJTs the cut-in voltage is determined by the thermal voltage). Because of the threshold voltage variations from device to device, the MOS differential stage often exhibits a higher input offset and an poorer common-mode rejection ratio



when compared to the BJT differential stage [58]. For balanced BJTs the input offset can be in the order of 0.2mV and for MOS transistors in weak inversion in the order of 2mV [59]

As discussed earlier, the BJT normally exhibits better matching than MOS and therefore lower offset voltage. There are several techniques to improve matching of the input pair such that even lower offsets can be achieved. We used large input transistor sizes to achieve better matching characteristics in the differential input pair [60]. Another way, which can be done on layout level, is to use a common centroid configuration, where the devices are symmetrically arranged so that their centre of mass lies in the centre [61]. This is typically implemented in combination with cross coupled multiple transistors in parallel. Emitter degeneration is yet another technique for improving matching at the expense of transconductance degradation, thus lowering the loop gain [62].

Another reason to choose for BJT's instead of MOS transistors can be the fact that a significantly higher transconductance can be achieved for the same bias current. This is because the  $g_m$  of the BJT is directly proportional to the bias current as opposed to the square root relation of the MOS transistor [62]. The higher transconductance can be used for higher loop gain or for lower power consumption when a lower current is used.

When the differential stages consist of MOS input pairs we have to take the geometry-dependent transconductance into account. In these circumstances matching of both differential stages is not only important for reducing the input offset but also to have improved matching of the transconductance. As was discussed earlier this can be accomplished by special layout techniques. However, as discussed before we have chosen for bipolar input pairs. In the case of bipolar input pairs the matching is of less importance for matching of the transconductance because the transconductance of each BJT stage depends mainly on its bias current and thermal voltage. While temperature differences between both differential stages in submicron IC technology can be expected to be very small a deviation between the bias currents delivered by the two tail-current sources can be expected due to the finite resistance of a practical current source, as will be discussed in the following subsection.

Another advantage of BJT is the lower noise for low  $R_s$  signal sources. As the voltage divider in our system is actually used as voltage source knowing to have a low source resistance  $R_s$  the BJT input pair will be to our advantage. When considering noise the significant higher transconductance of the bipolar differential stage as discussed earlier, can be also an advantage. A high gain at the input stages makes the noise of the intermediate stages less important, such that it improves the minimal detectable input signal range. As the operation of BJT is normally underneath the surface the input referred noise voltage is already lower than that of MOS transistors (For MOS,  $1/f$  noise dominates at low frequency). Fortunately the limit on the minimal input will not be an issue in our system, because we use constant DC references which have considerably higher voltages levels than the expected noise floor of the BJT input pairs. However something what can take into account is the effect of the noise from the input pair to the noise at the output of the DDA. As we know the output signal of the DDA is used to bias also the cascaded A/O cells inside the successive approximation RF power detector. When there is excessive noise at the bias of the cascaded A/O cells, it may influence the performance of the RF power detector as it will multiply into the signal that the RF power detector processes.

As the differential input stages of the DDA are used as voltage sensors the high input impedance of a MOS input pair would have the advantage over its bipolar counterpart. However for our implementation the finite input impedance of the BJT can be used in our advantage, because it can be used to increase the precision to which the loop controls to the right gain of  $M_{\text{REAL}}$ . To be more precisely,  $M_{\text{REAL}}$ , the one that is placed outside the control loop and is used for the actual multiplication of the RF input signal, is loaded by the BJT input pairs of the first stage of the cascaded A/0 cells and a G/0 cell. When the loading and sinking conditions of  $M_{\text{copy}}$  and  $M_{\text{real}}$  can be made comparable the gain behaviour of both cells will be the same when controlled with same bias signal.

In Table 5.1 an overview of the differences between MOS and BJT differential pair is shown.

**Table 5.1 Differential Pair Comparison [62]**

Quality Comparison	MOS	BJT
High $g_m$		X
High $R_{in}$	X	
Matching		X
Voltage Offset		X
Better Frequency Response		X
Noise		X

### 5.2.3.5.2 The tail current sources

The output impedance of a current source can be defined as

$$Z_o = \frac{\delta V_o}{\delta I_o} \quad (5.23)$$

This definition shows that an ideal current source, knowing to have an infinite output resistance, provide a constant output current  $I_o$  over different output voltages. However, the assumption of infinite output resistance doesn't hold for practical current sources.

When dealing with the practical current sources as in our DDA their finite output resistance has to be taken into account [63]. The finite output resistance of these current sources determines the sensitivity to the common-mode voltages on the input port that it biases. Because of the finite resistance unequal common-mode voltages on the two input ports will lead to a difference between both tail currents which ultimately results in a mismatch between the transconductance elements. As we discussed earlier a mismatch between both transconductance elements should be minimized for optimal performance of the DDA.

From literature [64] we know that the output impedance of a current source can be greatly increased by applying the cascoding principle. As shown in Figure 5.8 we implemented BJT cascode current sources ( $T_7, T_8$ ) and ( $T_9, T_{10}$ ). The reason to choose for the BJT instead of MOS is the possibility for better matching between both current sources [59]. As shown, the current  $I_1$  to be delivered by the current sources is mirrored from the transistors  $T_5, T_6$ . However, when mirroring is accomplished with BJT transistors the base currents has to be taken into account [63].

Because of the base currents there will be a current mirroring error between cascoded current source  $T_5$ - $T_6$  and the cascoded tail current sources. Fortunately this error will not alter the accuracy of our system that much, because matching is more important than absolute value of the common-mode output current. When the tail current sources are matched and have very high output impedance both tail currents will be matched. The current mirroring error will only lead to a lower or higher tail current at both input stages. It only influences the closed-loop gain because of change in the matched transconductance of both input pairs. When loop gain is high the current mirroring error will not influence the accuracy of the system that much. To reduce the sensitivity of loopgain over temperature for the temperature dependent base impedance an MOS transistor  $M_5$  is placed from the collector to the base of  $T_5$ . In this configuration the temperature dependent base currents of  $T_5$ ,  $T_7$  and  $T_9$  are supplied by  $M_5$  such that the full current  $I_1$  is forced through transistor  $T_5$ . Of course the error caused by base currents of the transistor  $T_6$ ,  $T_8$  and  $T_{10}$  can be solved with the same method. But this will be at the expense of an extra voltage drop  $V_{GS}$  which will lowering the input voltage swing.

### 5.2.3.5.3 The Active load

Next sub-circuit to be discussed is the active load ( $M_1, M_2$ ). As shown in Figure 5.8 this active load loads the cross-coupled differential pairs  $T_1$ - $T_2$  and  $T_3$ - $T_4$ . The active load, which actually operates as a current mirror, is used to obtain the subtraction action to convert the differential current into a single-ended current, as was performed by the subtraction block in the system block diagram depicted Figure 5.7. For the implementation of the active load we have chosen for MOS devices. The reason to choose for MOS was to solve the current error, as was discussed earlier. Now it's not only about the finite output impedance of the current mirror but also about another error that dominates. This additional error, as we already discussed at previous subsection, originates from the base current. As we know the MOS transistor has no DC gate current due to the isolated gate. Overall the MOS transistor seems to be the best choice for the active load.

To achieve better matching, for this current mirror, we used large MOS transistor sizes. A disadvantage of the large geometries, as we propose, can be bandwidth limitation caused by the increased parasitic capacitance. Fortunately, in the system discussed till now the low bandwidth will be no problem, as the system has to process a signal that is close to DC.

### 5.2.3.5.4 The trans-impedance stage

The next part to be discussed is the trans-impedance stage. As can be seen in Figure 5.8, the trans-impedance stage is implemented by a standard integrator, consisting of the gain stage  $M_3$ , which is biased and loaded by the cascode current source ( $T_{13}, T_{14}$ ), a buffer stage ( $M_4$ ) which is biased and loaded by the current source ( $T_{16}$ ) and the feedback capacitor ( $C_1$ ). When looking at this configuration, one will notice that we actually implemented an integrating trans-impedance amplifier.

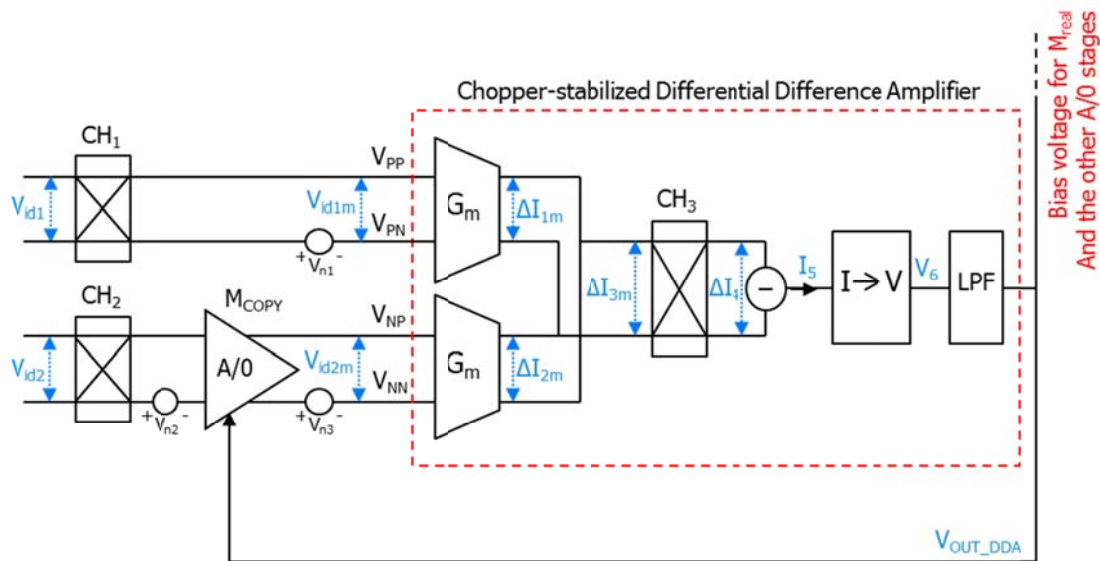
The gain stage is constructed by a MOS input transistor to obtain very high input impedance for the DC signal it has to process such that a high DC loop gain for our DC signal is obtained. The buffer stage minimizes the loading effects from the proceeding stage by provides a low-impedance output such that the operation point of the gain stage is much less dependent of the output current of the DDA. This is necessary because the output has to supply the base currents of the BJT current sources of  $M_{copy}$ ,  $M_{real}$  and all the cascaded A/O stages of the log detector. The

feedback capacitor  $C_1$  connected around the gain stage and the buffer is used for so-called Miller compensation. At DC, this feedback capacitor acts like an open circuit blocking any feedback voltage resulting in very little negative feedback from the output back to the input of the trans impedance. So, for DC the transimpedance stage is connected as a normal open-loop amplifier which has high open-loop gain. As we deal with DC input signals, the very high open-loop gain at DC is beneficial for the operation of our system.

## 5.2.4 Reducing the sensitivity to non-idealities in the gain fixation system

In Section 4.3 it was shown that the fixation system will be sensitive to non-idealities like offset. It was shown that, when not taken into account, these non-idealities will degrade the accuracy of system to unacceptable log conformance levels. To lower the sensitivity to the non-idealities of the circuit discussed in previous section we will now incorporate the so-called chopper stabilizing technique [65] [66] into the fixation system. [67] [68] [69] By using this technique the system can tolerate much higher input port mismatch, thus attaining low input offset. At the same time this technique reduces  $1/f$  noise and attains a high CMRR. In other words, with the chopping technique the sensitivity to offset can be reduced as will be discussed in following section. As the so-called chopper technique will lead to a more complex circuit than the one discussed earlier we first will start the discussion of the chopped gain fixation circuit at system level. Thereafter the extra circuitry incorporated into the system will be discussed.

### 5.2.4.1 Chopping to reduce offset in the gain fixation system

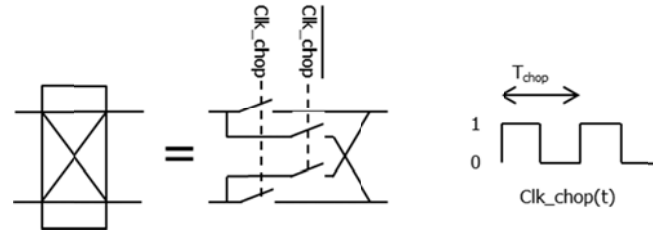


**Figure 5.9** System overview of the chopped gain fixation system

To explain how the chopping principle reduces the influence of non-idealities in our system, we will make use of the system block diagram as shown in Figure 5.9. The source  $V_{n2}$  in this figure represents the input referred DC offset and  $1/f$  noise of the high bandwidth gain stage  $M_{copy}$ . The same applies for  $V_{n1}$  and  $V_{n3}$ , which model the DC offset and  $1/f$  noise of the DDA.

The two blocks at the differential inputs ( $CH_1$  and  $CH_2$ ) and the block ( $CH_3$ ) in front of the subtraction block represents the chopper symbol. The action of the so-called chopper is to transform a differential input signal, applied to the input terminals of the chopper into an alternating output voltage at the output node of the chopper.

The internal structure of a chopper, can be described as shown in Figure 5.10



**Figure 5.10** The chopper symbol (a) represents a configuration with 4 switches (b) which are controlled by a rectangular control signal (c)

As shown by this figure the chopper consists of 4 switches. These switches are driven by a binary control signal,  $Clk\_chop$ , with chopper frequency  $1/T_{chop}$ . This results in an alternating output node voltage, whereby the differential output voltage of the chopper switches its polarity.

In our system choppers  $CH_1$  and  $CH_2$  are switching simultaneously and switch the polarity of both differential DC input signals  $V_{id1}$  and  $V_{id2}$ , representing the two differential voltages from the divider block, in an alternating fashion. As they are modulating the input signals,  $CH_1$  and  $CH_2$  are also called modulators.

The operation of these modulators can be modelled by multiplying the input signals with a rectangular signal  $m(t)$  with unity amplitude, 50% duty-cycle and zero average.

When applied to the input signals  $V_{id1}$  and  $V_{id2}$ , the input situation of the DDA can be written as

$$V_{id1m}(t) = V_{id1} \cdot m(t) + V_{n1}(t) \quad (5.24)$$

$$V_{id2m}(t) = (V_{id2} \cdot m(t) + V_{n2}(t)) \cdot A + V_{n3}(t) \quad (5.25)$$

Where the time-domain definition of  $m(t)$  can be described as follows

$$m(t) = \begin{cases} 1, & 0 < t < (T_{chop}/2) \\ -1, & (T_{chop}/2) < t < T_{chop} \end{cases} \quad (5.26)$$

where  $T_{chop} = 1/f_{ch}$

The Fourier series of this time-domain definition is given as

$$m(t) = 2 \sum_{k=1}^{\infty} \frac{\sin\left(\frac{k\pi}{2}\right)}{\frac{k\pi}{2}} \cos(2\pi f_{ch} kt) \quad (5.27)$$

When we incorporate Equation (5.27) into Equation (5.24) and (5.25) we get

$$V_{id1m}(t) = V_{id1} \cdot 2 \sum_{k=1}^{\infty} \frac{\sin\left(\frac{k\pi}{2}\right)}{\frac{k\pi}{2}} \cos(2\pi f_{ch} kt) + V_{n1}(t) \quad (5.28)$$

and

$$V_{id2m}(t) = A \cdot \left( V_{id2} \cdot 2 \sum_{k=1}^{\infty} \frac{\sin\left(\frac{k\pi}{2}\right)}{\frac{k\pi}{2}} \cos(2\pi f_{ch} kt) + V_{n2}(t) \right) + V_{n3}(t) \quad (5.29)$$

This shows that the differential DC input signals  $V_{id1}$  and  $V_{id2}$  are modulated to the fundamental and every odd harmonics of the chopper frequency  $f_{ch}$  while  $V_{n1}(t)$ ,  $V_{n2}(t)$  and  $V_{n3}(t)$  still reside at baseband.

When looking at the first term of Equation (5.25), an important result of the modulation action of modulator CH<sub>2</sub>, can be seen. As will be shown by further analysis the superposition of the noise sources will hold for all linear amplifiers inside the system and is the fundamental idea behind the chopping technique.

According to Equation (5.24) and (5.25) we now have two modulated differential voltages  $V_{id1m}(t)$  and  $V_{id2m}(t)$  in front of the DDA. These modulated voltages are transformed to currents via the transconductance cells with a transconductance  $G_m$ . When using the time domain expression from Equation (5.24) and (5.25) these two differential currents can be written as

$$\Delta I_{1m}(t) = G_m [V_{id1} \cdot m(t) + V_{n1}(t)] \quad (5.30)$$

$$\Delta I_{2m}(t) = G_m [A(V_{id2} \cdot m(t) + V_{n2}(t)) + V_{n3}(t)] \quad (5.31)$$

As shown in Figure 5.9 the direct and cross connection of the two differential current outputs results in the modulated differential current,

$$\Delta I_{3m}(t) = \Delta I_{1m}(t) - \Delta I_{2m}(t) \quad (5.32)$$

at the input of demodulator CH<sub>3</sub>.

With Equation (5.30) and (5.31) this differential current can be rewritten as

$$\Delta I_{3m}(t) = G_m[V_{id1} \cdot m(t) + V_{n1}(t)] - G_m[A(V_{id2} \cdot m(t) + V_{n2}(t)) + V_{n3}(t)] \quad (5.33)$$

From Figure 5.9 it is shown that chopper CH<sub>3</sub> demodulates this current into a differential current  $\Delta I_4$  which subsequently will be converted to a single ended current  $I_5(t)$  by the subtraction block. This will result in the single ended current

$$I_5(t) = m(t) \cdot G_m([V_{id1} \cdot m(t) + V_{n1}(t)] - [A(V_{id2} \cdot m(t) + V_{n2}(t)) + V_{n3}(t)]) \quad (5.34)$$

This can be rearranged into

$$I_5(t) = G_m([V_{id1} \cdot m(t) \cdot m(t) + V_{n1}(t) \cdot m(t)] - [A(V_{id2} \cdot m(t) \cdot m(t) + V_{n2}(t) \cdot m(t)) + V_{n3}(t) \cdot m(t)]) \quad (5.35)$$

From Equation (5.26) we know that

$$m(t) \cdot m(t) = 1 \quad (5.36)$$

With this knowledge we can simplify Equation (5.35) to

$$I_5(t) = G_m([V_{id1} + V_{n1}(t) \cdot m(t)] - [A(V_{id2} + V_{n2}(t) \cdot m(t)) + V_{n3}(t) \cdot m(t)]) \quad (5.37)$$

This can be rewritten as

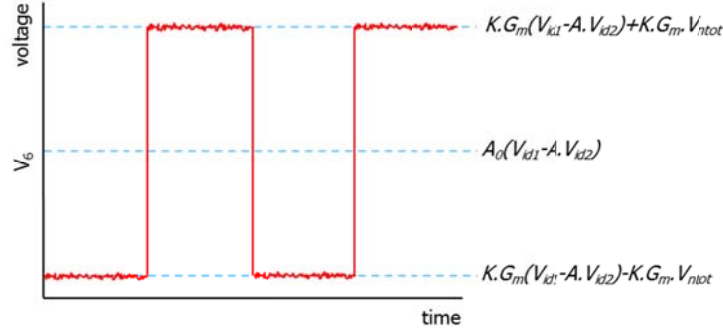
$$I_5(t) = G_m[V_{id1} - A(V_{id2})] + G_m[V_{n1}(t) - AV_{n2}(t) - V_{n3}(t)] \cdot m(t) \quad (5.38)$$

This shows that the current  $I_5$  is composed of two parts. The first term represents the wanted signal at baseband, while the second term contains the contribution of the noise sources, which are now located at the chopping frequency  $f_{ch}$  and every odd harmonics of  $f_{ch}$  as indicated by (5.27)

When assuming an linear trans-impedance (for simplicity of the analysis we neglect the integration action of the trans impedance) with a trans impedance factor of  $K$  the current  $I_5(t)$  is converted into voltage signal  $V_6(t)$  as shown by following equation

$$V_6(t) = K \cdot G_m[V_{id1} - A(V_{id2})] + K \cdot G_m[V_{n1}(t) - AV_{n2}(t) - V_{n3}(t)] \cdot m(t) \quad (5.39)$$

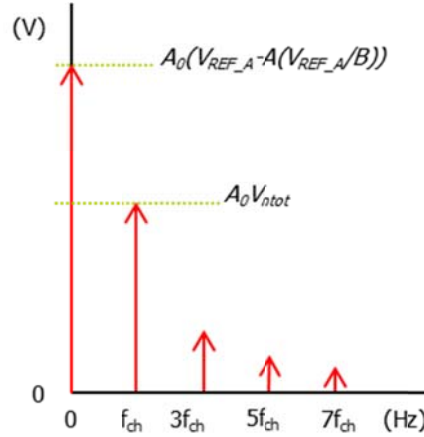
In time, the signal described by Equation (5.39), can be depicted as shown by the red solid line in Figure 5.11.



**Figure 5.11** Ripple of modulated output signal depends on amount of noise and offset in the system

As shown by this figure the ripple amplitude of the rectangular signal  $V_6$  depends on the amount of offset and noise in the system part that is chopped.

The terms  $K.G_m$  which are shown in Figure 5.11, represent the open-loop gain,  $A_0$ , of the DDA. From previous analysis we know that the ripple of  $V_6$  has the same frequency as the chopper clock. We also know that in our fixation system  $V_{id1}$  corresponds to  $V_{REF\_A}$  and  $V_{id2}$  to  $V_{REF\_A}/B$ . With this knowledge the square wave  $V_6$  shown in Figure 5.11 can be depicted by its frequency spectrum as shown in Figure 5.12 [66]



**Figure 5.12** Frequency spectrum of the modulated output signal of the chopped system

Now, when we assume that the low pass filter (LPF) shown in Figure 5.9, removes the frequency-translated DC offset and  $1/f$  noise at the odd harmonics, the resulting signal at the output of the DDA will be

$$V_{OUT\_DDA} = A_0 \left( V_{REF\_A} - \frac{A(V_{REF\_A})}{B} \right) \quad (5.40)$$

From Equation (5.40) it is shown that with the chopping technique the DDA only amplifies the differential voltages of interest and is insensitive for input offsets and the low frequency flicker noise. This means that resulting output signal is a pure DC signal. So, we can conclude that the system can be made insensitive for the introduced non-idealities of the DDA and that of the amplifier  $M_{copy}$  when the chopper stabilizing technique is used. As the system is continuously chopped it also eliminates offset temperature drift, and the long-term offset drift.

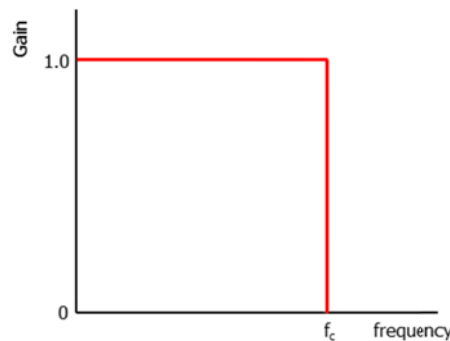


### 5.2.4.2 The low pass filter

As we know from the previous subsection the low-pass filter at the output of the transimpedance stage as was shown in Figure 5.9 is used to recover the signal. With recovering we actually mean that the filter has to remove the unwanted ripple and spikes from the output voltage  $V_6$  of the trans-impedance stage such that only the wanted DC output  $A_0(V_{REF\_A}-A(V_{REF\_A}/B))$  will remain. To recover this signal to the DC component,  $A_0(V_{REF\_A}-A(V_{REF\_A}/B))$ , all the higher harmonics of modulated output signal as have been shown in Figure 5.12 have to be removed by the low pass filter. That the DC value only remains is of great importance because we want to use this signal as bias signal for the multiplication cell  $M_{real}$  and  $M_{copy}$  and all the other A/0 cells. A ripple free bias signal is necessary because any ripple or spike left on the bias signal would otherwise multiply into the signal output of  $M_{copy}$ , which will lead to a less accurate fixation system, while a ripple on the bias of the cascaded A/0 cells will introduce ripple in the signal path of the Successive Compression Logarithmic Amplifier itself. Beside the ripple free bias the system should also have an acceptable start up time, which means that the DC bias signal retrieved from the filter should be available as soon as possible. The response time and ease of integration into the feedback loop of the fixation system depends on the filtering approach that is used.

#### 5.2.4.2.1 The ideal low pass filter

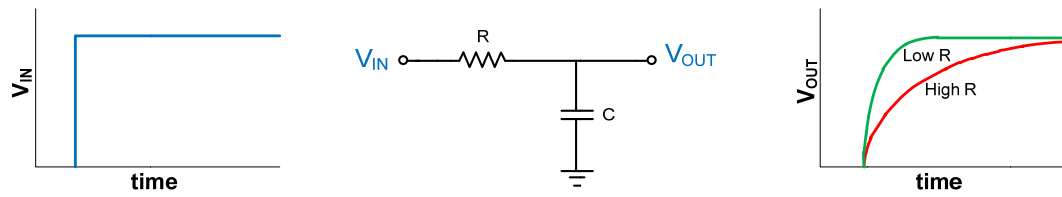
To recover the output signal of the chopped DDA to the output signal as indicated by Equation 5.35 we first will assume an ideal low pass filter. [70] The frequency response of an ideal low pass filter is depicted in Figure 5.13.



**Figure 5.13** The frequency response of an ideal low pass filter

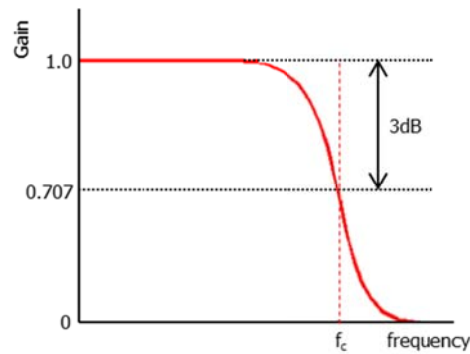
This figure shows that the response of an ideal low pass filter obtains an abrupt blocking of the frequency components higher than the frequency  $f_c$ . The frequency  $f_c$  is the so-called cut-off frequency of the filter. When the cut-off frequency  $f_c$  of the ideal filter is put lower than the first odd harmonic of the modulated output signal  $V_6$ , for which the frequency spectrum was shown in Figure 5.12, all the higher harmonics will be removed. This means that only the DC component,  $A_0(V_{REF\_A}-A(V_{REF\_A}/B))$ , will remain. However, in reality an ideal filter doesn't exist. For real world implementations we have to deal with more practical filters. One of these types of filters is the well-known RC filter.

### 5.2.4.2.1.1 The Low pass RC filter



**Figure 5.14** The step response (a) applied to the first order RC low pass filter (b) for two different values of  $R$  results in output response (c)

A first-order low-pass RC filter is shown in Figure 5.14(b). In same figure the step response for different values of the resistor  $R$  is shown. When a practical RC low pass filter is used an abrupt blocking capability of frequency components higher than  $f_c$ , is not realizable. Instead of an abrupt blocking at the frequency of interest these types of low pass filters will have a transfer which would look more like the response as depicted in Figure 5.15.



**Figure 5.15** Non-ideal Low pass filter response

Because of the so-called roll-off, the frequency components higher than  $f_c$  will be suppressed but in theory will never be totally blocked. The amount of suppression of the frequency components after the cut-off frequency depends on the order of the filter that is used. For a first order filter it is known that it has a roll-off of 20dB/decade, which means that it attenuates the amplitude of a component by 20dB for each decade the frequency of the component is higher than the cut-off frequency. This would mean that for the best suppression of the unwanted frequency components we should put the cut-off frequency as low as possible, by increasing the  $R$  and/or  $C$  of the filter. However, because of the high time constant added by such approach the speed of our control loop will get very slow and the values of  $R$  and  $C$  can become too large for monolithic integration.

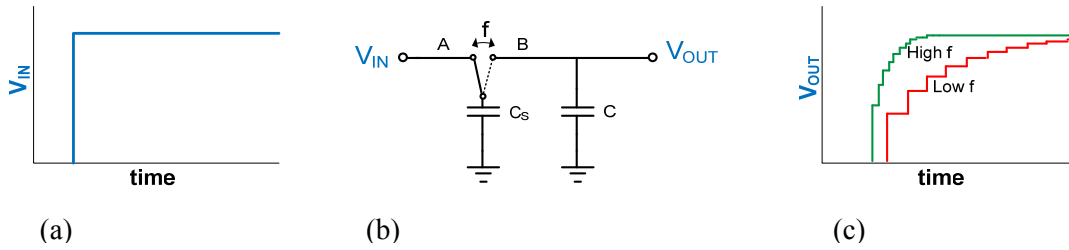
To make the loop faster and still maintain the same rejection of high frequency components one could think of using a higher order filter, which is known to have much steeper roll-off as each increase in filter order will add 20 dB per decade to the roll-off of the filter. When used in open loop configuration a higher order filter will certainly improve the rejection but as each added order to an RC filter will also add a phase shift to their output signal, this approach would make a negative feedback loop architecture with large amounts of loop gain difficult or impossible to realize.

Another approach to have better suppression of the unwanted components can be the use of a higher chopping frequency. This approach would shift the unwanted frequency components to higher frequencies such that the filter can suppress them more. However a higher chopper frequency would introduce other difficulties as will discussed in a later section.

As we know, the time constant of the RC filter depends on the product of the resistance and a capacitor value. In sub-micron IC technology resistance and capacitance values do not track each other. As a result the time constant of a RC filter is not well defined over variations in process, supply and temperature. Furthermore, as already stated earlier, for very low cut off frequencies the feature size of the resistor and capacitor would get much too big for monolithic integration. A type of filter that doesn't have these short comes is the so-called Switched Capacitor filter

#### 5.2.4.2.1.2 Switched capacitor filter

[70] A switched capacitor filter can have a very low cut-off frequency, while maintaining small feature sizes. Another advantage of this type of filter is that it has an accurate and easy tuneable cut-off frequency and can have low sensitivity to temperature changes. This allows consistent, repeatable filter designs. The operation principle of a switched capacitor will be shown by following example.



**Figure 5.16** The step response (a) applied to a switched capacitor low pass filter (b) for two different switching frequencies results in the output response (c)

A simple switched capacitor filter is shown in Figure 5.16. Briefly said the operation of this filter is based on a track and hold operation of sampling capacitor  $C_S$  followed by a charge-redistribution to capacitor  $C$ . As shown by Figure 5.16 this operation is performed by alternately connecting node A and B with an accurate and predefined frequency  $f$  to the upper plate of capacitor  $C_S$ .

The average current flowing from A to B is then determined by the charge moved in one clock period.

$$\overline{I_{AB}} = \frac{C_S(V_A - V_B)}{f^{-1}} \quad (5.41)$$

This can be rearranged as

$$\frac{(V_A - V_B)}{\overline{I_{AB}}} = \frac{1}{C_S f} \quad (5.42)$$

So actually by switching capacitor  $C_S$  with a frequency  $f$  we mimic a resistor with a value equal to

$$R_{SC} = \frac{1}{C_S f} \quad (5.43)$$

Capacitor  $C$  together with the resistance  $R_{SC}$  forms the switched capacitor low pass filter's time constant. When comparing Figures 5.14(c) and 5.16(c) it shows an equivalent step response. This shows that two capacitors and one switch can perform the same function as a RC network.

From the previous discussion we can see that a switched-capacitor filter is actually a clocked, sampled-data system. The input signal is sampled at a high rate and is processed in discrete time, rather than continuously as it was for the RC filter.

The time constant of a SC filter is determined by the ratio of capacitor values and the clock frequency. If the capacitors have the same properties, the ratio is well controlled even when the absolute values are poorly controlled. As the time constant is determined by the ratio of capacitors, very high time constants can be obtained with low capacitance values. This shows that switched-capacitor integrator can be well implemented in sub-micron IC technology. The clock frequency of an SC filter can be set by an external clock with accurate frequency, for example a crystal oscillator.

As will be shown in a later section the switched capacitor filter will form the basis of a new filter concept that we have implemented. Since the clock frequency can be precisely set by the chopping clock we use for our fixation system, it will be shown that a crystal oscillator will be not necessary. But before we introduce our new switched capacitor filter we first will discuss the limitations and non-idealities of the chopped fixation system.

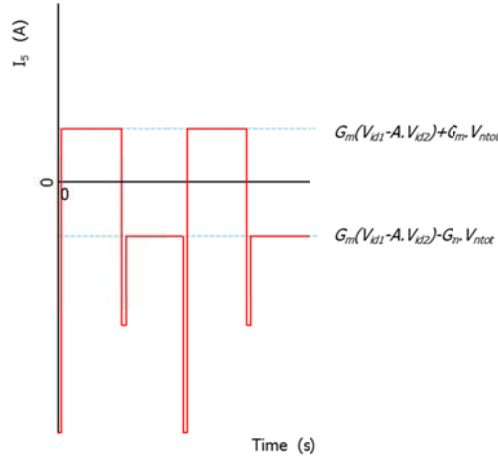
#### 5.2.4.3 Limitations and non-idealities of the chopping circuit

When we look at Figure 5.11, we can see that the chopping action resulted in an ideal rectangular signal (neglecting the noise) with a duty-cycle of 50%. With this assumption the extraction of the mean value of the signal by an ideal filter will lead to the correct DC component. Of course the assumption of an ideal rectangular signal is not correct, when dealing with the practical implementation of the system. The signal shown in Figure 5.11 is actually an idealized waveform, resulting from the ideal chopping and filtering conditions. For practical implementation of the chopping and filter circuit we have to examine some of the limitations and non-idealities that are known from chopping.

##### 5.2.4.3.1 Limited bandwidth of the system

One of the limitations is the limited bandwidth of the system that has to be chopped. When we implement the chopper architecture around a system with finite bandwidth the system will attenuate the higher order harmonics of the square wave signal which lie higher than this system bandwidth. Secondly, a possible non-linear transfer of the system will introduce some spectral components around the odd harmonics of chopper frequency. As was shown by Equation 5.22, a pure rectangular signal should only consist of odd harmonics of the chopping frequency. Existence of attenuated odd harmonics and/or other spectral components will undoubtedly result in a non-rectangular output signal. Furthermore a limited bandwidth of the system in between the

choppers is a fundamental cause of so-called switching glitches. [66] These glitches arise when for example the input signal is modulated almost ideally, while the amplified signals in reality will be slightly delayed by the chopped system before it is demodulated. When there is for example an excessive delay and we assume only an offset  $V_{ntot}$  at the input of the DDA, the signal  $I_5$  in Figure 5.9 would look like as shown in Figure 5.17.

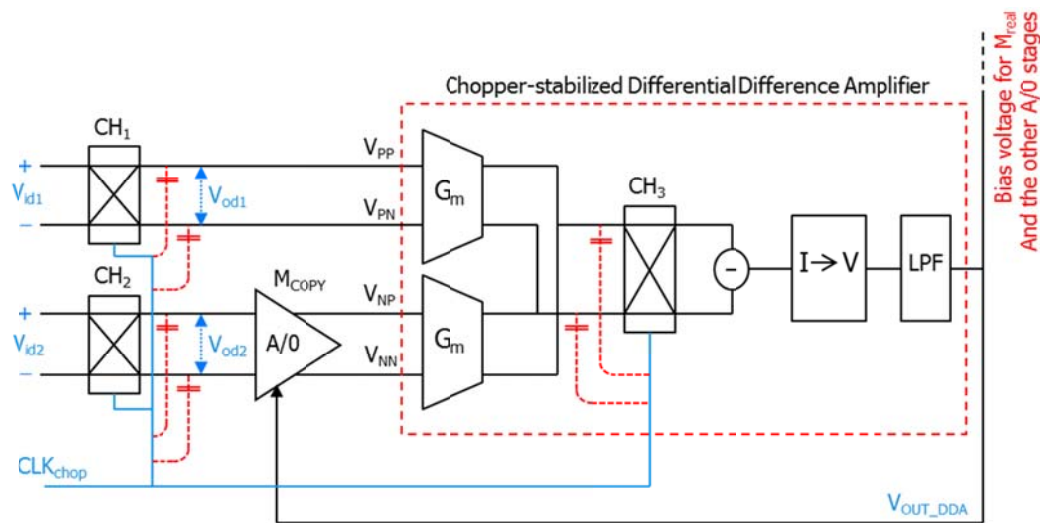


**Figure 5.17** Switching glitches as result of the finite bandwidth of the chopped system

#### 5.2.4.3.2 Residual offset caused by clock feed-through

Another issue which has to be discussed is the so-called residual offset caused by charge injection, arising from the switching operation of the chopping technique.

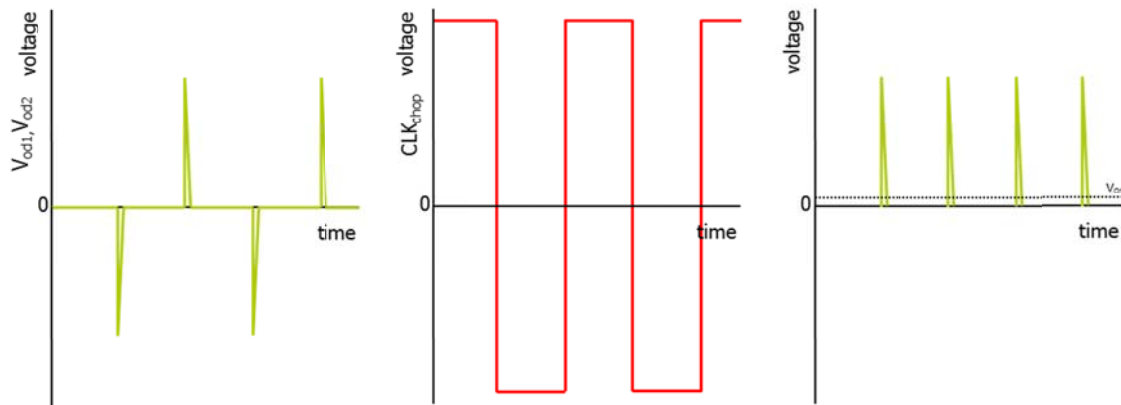
At [66] it is shown that one of the sources of the residual offset is charge injection mismatch from the clock lines to the input and output of the system that is chopped. The phenomenon which causes this so-called clock feed-through is known as crosstalk. When we include the clock lines in our system this crosstalk can be modelled with capacitances as shown in Figure 5.18. These are not physical capacitors and are only used to model the differences in the capacitance between the clock lines and the signal paths.



**Figure 5.18** Clock feed-through caused by the capacitance between clock lines and the input and output of the chopped fixation system modelled by cross talk capacitors (depicted red).

The residual offset generated by these crosstalk capacitances is a result from the fast voltage transitions they experience at the clock line during switching. This is because during switching the impedance of the crosstalk capacitances are finite for the high frequency components of the clock signal, resulting in voltage spikes at both output nodes of the choppers. When both nodes are loaded with identical crosstalk capacitances this only will result in a common mode spike. As the differential architecture is insensitive to common-mode signals these spikes will not contribute to the so-called residual offset. However, when there is a slight mismatch between the crosstalk capacitances at the output of a chopper, a differential voltage will appear as a spike.

In what way the spikes result in a residual input offset can be seen from the following example. Let's assume that there is a zero differential input voltage at chopper  $CH_1$  and  $CH_2$ . When there is a mismatch in the crosstalk capacitors at the output of these choppers, clock feedthrough for a clock signal as shown in 5.19(b) will lead to spikes at the differential output of the chopper  $CH_1$  and  $CH_2$  as shown in Figure 5.19(a).



**Figure 5.19** Voltages spikes at the output of the input choppers (a) as result of the fast transitions of the chopper control signal (b) can be translated to an input referred residual input offset  $V_{os}$  (c)

As these spikes are actually demodulated by the corresponding input chopper towards the input [66], this will translate into an input referred residual offset at  $V_{id1}$  and  $V_{id2}$ , as has been visualized by  $V_{os}$  in Figure and 5.19(c).

As the spikes are generated at each clock transition the residual offset will increase with increasing chopper frequency. This indicates that clock feedthrough leads to a trade-off between speed and precision. However, as a result of the shared control signal  $CLK_{chop}$  at both input choppers it is interesting to note that the residual offset contributed to  $V_{id1}$  and  $V_{id2}$  are in the ideal case exactly in phase and will have the same polarity. Thus, an advantage of using a DDA instead of a classical opamp, is that the spikes occur at the same time at each differential input of the DDA. We thus can expect that the sensitivity to the residual offset caused by crosstalk at the input choppers is less than that for the single chopper situation of a classical op-amp.

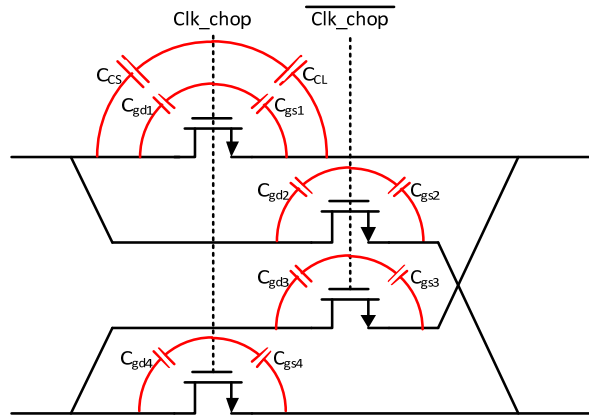
The crosstalk capacitors at the input nodes of the output chopper  $CH_3$  are also causing spikes. From [66] we know that the extra residual input offset, as a result of these spikes, can be decreased by choosing higher transconductance amplifiers.

### 5.2.4.3.3 Non-idealities of MOS transistors switches

In Figure 5.10 we showed the internal structure of the chopper. The chopper switches were represented by ideal switches. In reality MOS transistors are used as switch. As MOS transistors behave differently from ideal switches a discussion on their second-order behaviour is in order.

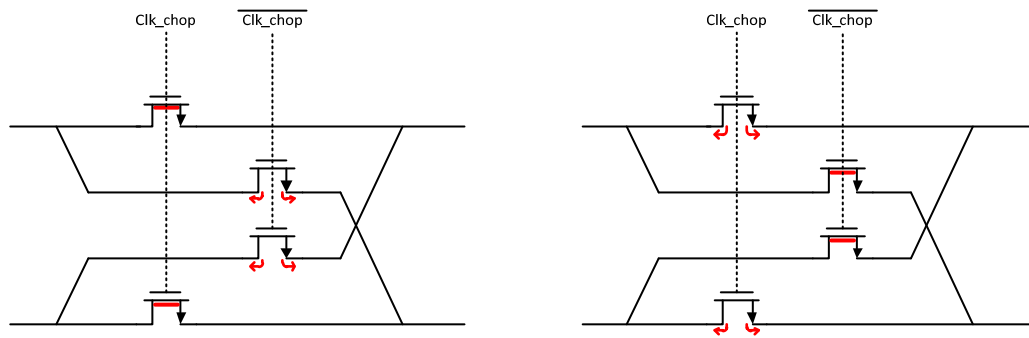
One of the differences is that a CMOS switch has a finite impedance when it is turned off and a non-zero impedance when it is turned on. The on-resistance of a MOS switch depends on the input level and its aspect ratio  $W/L$ . A PMOS switch exhibits an on-resistance that decreases as the input voltage at the drain becomes more positive, whereas the on-resistance of an NMOS decreases for inputs at the drain that becomes more negative. When a current is flowing through a closed MOS switch with a too high on-resistance it will lead to a non-negligible voltage drop. The on-resistance will also limit the maximum switching speed.

Other non-idealities of the MOS switch are the clock feed-through caused by its parasitic capacitances and the redistribution of channel charge when it is turned off. These two non-idealities will contribute to a residual offset as explained previously.



**Figure 5.20** The clock feed-through generated by a MOS implemented chopper modelled by the gate-drain and gate source capacitances  $C_{gd}$  and  $C_{gs}$

Besides the clock feedthrough between the clock line and signal path known as crosstalk a MOS switch itself is also a cause of clock feedthrough. The clock feedthrough generated by a MOS switch is caused by the clock transitions that couple into the signal path through the gate-drain or gate-source overlap capacitance. This means that the clock feedthrough caused by these parasitic capacitances can be modelled by the gate-to-source and gate-to-drain capacitance,  $C_{gs}$  and  $C_{gd}$ , as shown in Figure 5.20. The crosstalk capacitance as discussed earlier is also included in this model. As shown in this figure we can model the crosstalk capacitance between clock line and the input path of the chopper by capacitor  $C_{cs}$  and the crosstalk capacitance between clock line and the output path of the chopper by capacitor  $C_{cl}$ . Both are placed in parallel with the parasitic capacitances of one of the chopper transistors [71]. This clarifies that, as it was for the cross talk capacitors, the gate-to-source and gate-to-drain parasitic capacitance will also contribute to the residual offset. Because of parasitic capacitances the gate signal not only drives the on or off state of the transistor but it also disturbs the drain, source and bulk of the transistor.



**Figure 5.21** *Redistribution of channel charge each time the chopper clock switches polarity.*

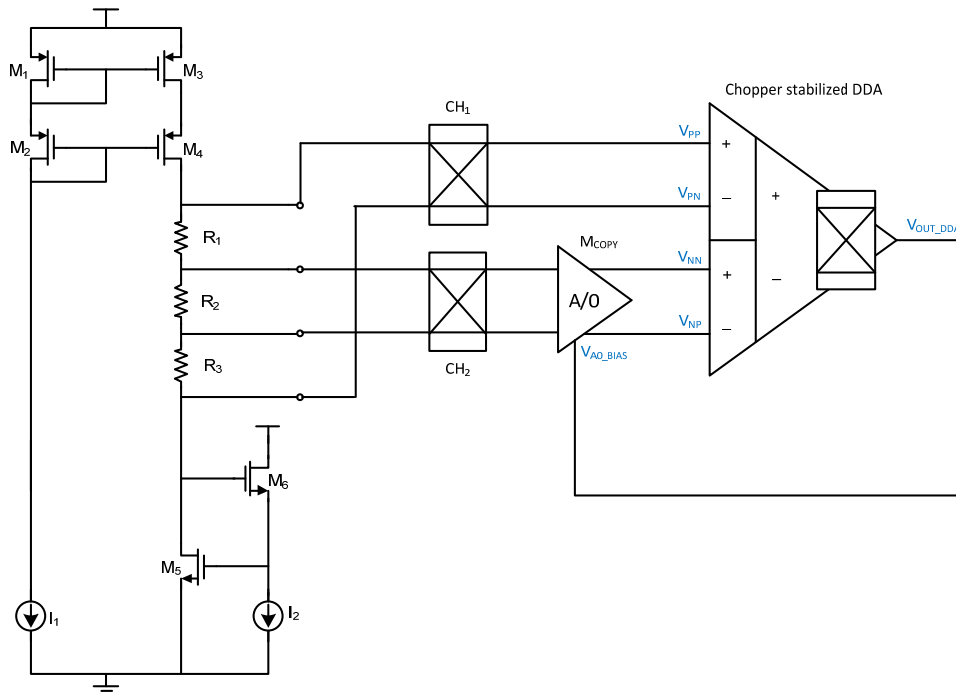
The other non-ideality of the MOS switch is the redistribution of channel charge during switching. The redistribution of channel charge of the MOS switches is graphically depicted in Figure 5.21. This figure shows that when a MOS transistor is on, a layer of channel charge exists under the gate between the source and drain of the transistor. When the transistor is turned off the channel charge has to go somewhere. Depending on the structure of the switch and the load at the drain or source, it will partially flow to the input of the chopper and partially flow to the output of the chopper. As both nodes of the input port and both nodes of the output port contain two MOS transistors these injections will happen each time the chopper clock switches. This means that this charge is applied two times per clock period, as can be shown in Figure 5.21.

This again shows the trade-off between speed and accuracy.

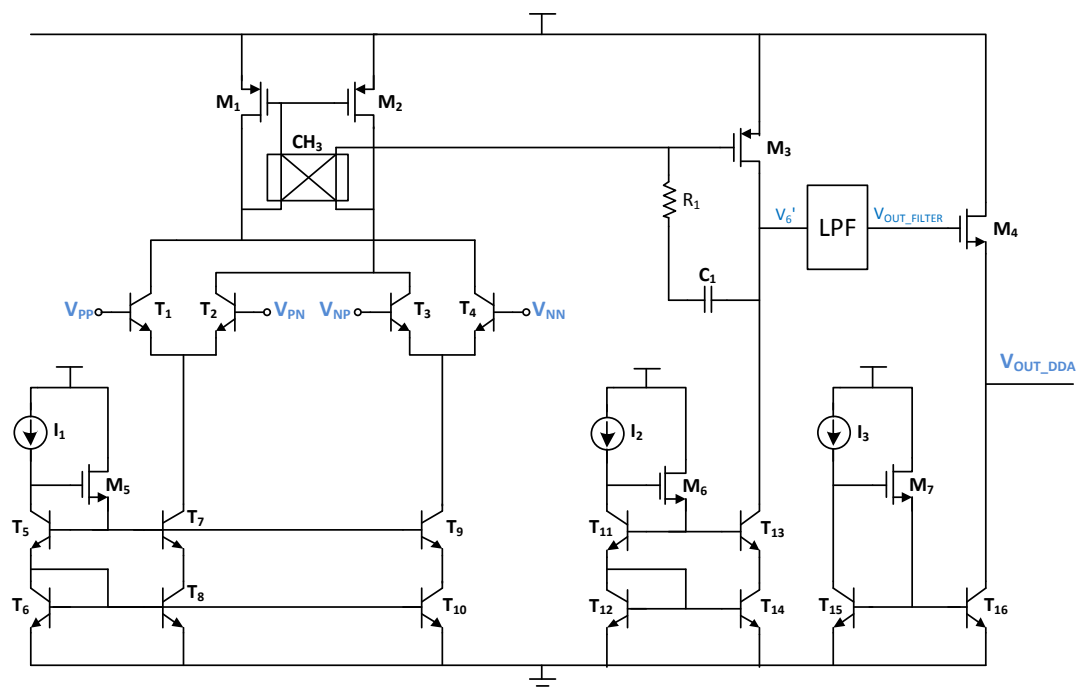
As it was for crosstalk the charge injection caused by the channel charge distribution should have no influence, since the switches of the input choppers, when assumed identical, inject or withdraw the same amount of charge at both inputs. But, there is actually a condition that will make this assumption not fully correct. This is because both the capacitive coupling and the redistribution of the channel charge effect has a non-linear dependency on the gate-source voltage,  $V_{GS}$ , of the MOS transistor. As both nodes of the differential input will have a different voltage, the  $V_{GS}$  of the MOS switches will differ from each other, such that the charge injection caused by capacitive coupling and channel charge contribution will not be exactly common mode.



### 5.2.5 Circuit implementation of the chopped gain fixation system



**Figure 5.22 Chopped Gain fixation system**



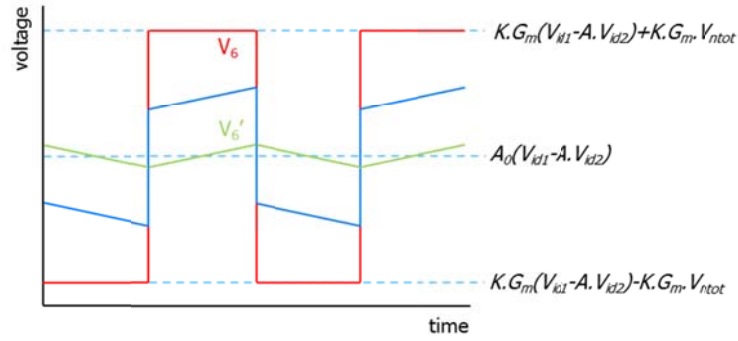
**Figure 5.23** Implementation of the chopper stabilized DDA

Figures 5.22 and 5.23 show the complete gain fixation system discussed so far. It is interesting to note that we used the chopping technique in such a way that we only use 3 choppers in total to remove the input offset and noise from the DDA and gain stage  $M_{\text{copy}}$ .

### 5.2.5.1 Integrating trans-impedance amplifier

In the system level operation of our fixation system, discussed in previous sections, we did not include the consequences of implementing the I-V block using the transimpedance circuit shown in Figure 5.22. The local feedback of this amplifier is constructed using a combination of a resistor  $R_1$  and a capacitor  $C_1$ . Without the capacitor the amplitude of the ripple of  $V_6$  would be defined by the open loop gain  $A_0$  of the DDA, as indicated by the red curve in Figure 5.24. With a high open loopgain it is not that difficult to see that this will result in a clipping output of the DDA when dealing with its real transistors implementation.

When we only take the integrating nature of  $C_1$  into account, the output of the trans-impedance stage will result in a triangular voltage signal instead of the rectangular signal  $V_6$  discussed earlier. An example of the triangular output signal is depicted by the green curve in Figure 5.24.



**Figure 5.24** Modulated output signal ( $V_6$ ) of idealised system and modulated output signal ( $V_6'$ ) of the real gain fixation circuit implementation.

The steady state triangular output of the integrator is a result of the negative feedback operation of the DDA, in which the feedback system is assumed to use the DC component of the triangular signal as its feedback control signal. As the feedback capacitor  $C_1$  takes some time to charge up, the voltage over  $C_1$  will rise and fall at a limited rate at reaction of the rectangular shaped input current  $I_5$ . This means that the amplitude of the triangle output voltage depends on the slew rate of the trans-impedance stage which is set by the capacitance of the feedback capacitor.

The maximum rate of voltage change over the capacitor  $C_1$  is

$$\left[ \frac{dV_{C_1}}{dt} \right]_{MAX} = \frac{I_5}{C_1} \quad (5.44)$$

Where,  $I_5$  is the rectangular input current of the transimpedance stage as was shown in Figure 5.9. The amplitude of the triangular output signal will be inversely proportional to the capacitance of feedback capacitor  $C_1$  and proportional to the (error) current  $I_5$ . Looking at it from a practical point of view it can be shown that the feedback capacitor  $C_1$  prevents clipping of the system while maintaining the high DC open loop gain.

When we incorporate the feedback resistor  $R_f$  into the loop, as was shown in the DDA circuit depicted in Figure 5.22, the output will approach a more rectangular signal instead of the triangular signal. An example of the final output signal of the trans-impedance stage, from now on called  $V_6'$ , is depicted by the blue curve shown in Figure 5.24. The resulting signal shape of  $V_6'$  is caused by the frequency compensation we applied to the system. The resistor  $R_f$  in series with the integrating capacitor  $C_f$  leads to a so-called zero in the frequency response of the overall fixation loop. At a particular frequency the resistor  $R_f$  will start to dominate such that the frequency components of the rectangular shaped input current higher than the zero experience a flat band frequency response instead of a -20dB/Decade roll off by the capacitor  $C_f$ . This is why this procedure is also known as frequency compensation. Frequency compensation is necessary to make the feedback loop of the chopped fixation system stable. The positive phase shift added to the higher frequency components, as a result of the frequency compensation, leads to a bigger phase margin, which was necessary for stable operation of the feedback loop [72]. The voltage ramp-up and ramp-down of  $V_6'$  is still defined by Equation (5.44) while the magnitude of the fast voltage transitions is defined by the voltage drop across  $R_f$ . The value of the voltage up and down transitions depends on the direction and magnitude of the rectangular input current  $I_5$ .

As indicated by the middle dotted line in Figure 5.24 we can see that an averaging action of  $V_6'$  by an ideal low pass filter will still lead to the same DC bias voltage as was for the rectangular shaped input signal  $V_6$  discussed earlier. However, as already discussed earlier an ideal filter doesn't exist. In next section a new filter approach will be proposed which will show a possibility to reconstruct a pure DC component from the modulated input signal  $V_6'$ .

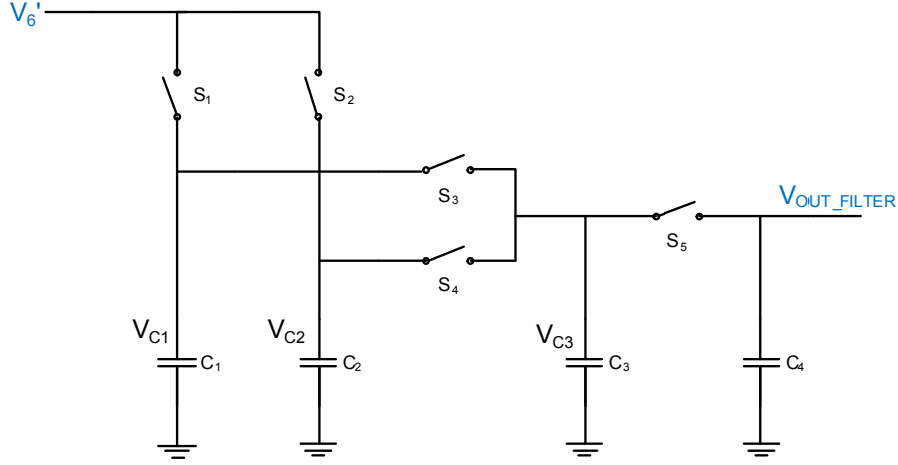
### 5.2.5.2 Novel output ripple blocking system for chopped systems

In Subsection 5.2.4.2.1.2 we introduced the switched capacitor filter and showed the advantages over the RC filter. It was shown that the operation was based on sampling the input signal with a high rate and processing it in discrete time. In this section we will propose a new Switched-Capacitor (SC) filter including a so-called notching operation. A fundamental difference between the switched capacitor operation discussed earlier and the new filter that will be proposed now is that it takes two synchronized samples of its input signal instead of one un-synchronized sample before it is processed. It will be shown that when the two sample values of the input signal are synchronized with the chopping control signal followed by discrete-time processing it can completely notch the unwanted frequency components from the modulated input signal. Furthermore the filter will include a modification to suppress spikes and other non-ideal effects from the output of the filter. The proposed filter has a fast response time, which is necessary for the biasing of the chopped fixation system. The filter can easily be implemented with on-chip capacitors and maintains the benefits of chopping while notching the ripple at  $f_{ch}$  from the output signal of the chopped system.

The switched capacitor filter will make use of a switching algorithm which is exactly synchronized with the chopper control signal, which means that the system doesn't need an external highly accurate off-chip oscillator.

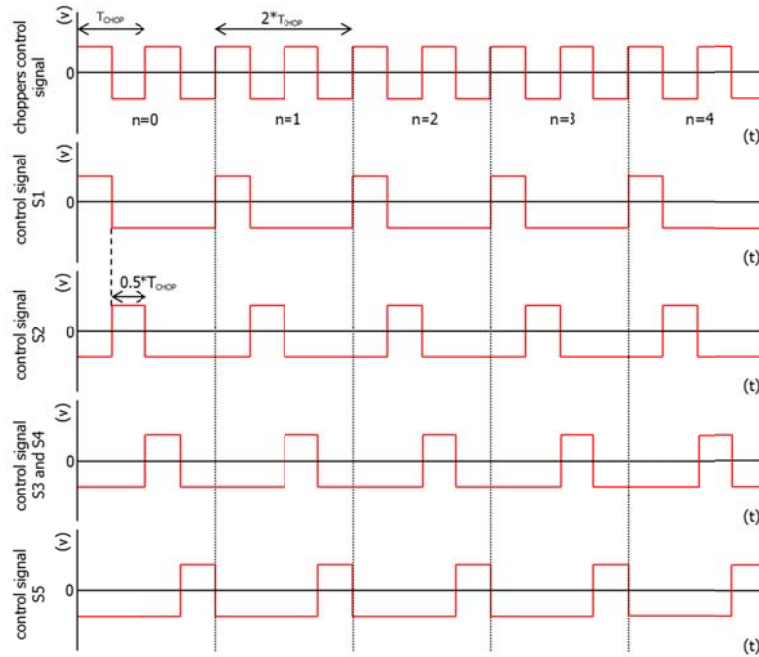
### 5.2.5.2.1 System level operation ripple blocking system

In Figure 5.25 the system overview of the new filter concept for chopped systems is shown.



**Figure 5.25** The new notching switched capacitor low pass filter for output ripple blocking of chopped systems

As shown by this figure, the system consists of 5 switches and 4 capacitors. For the most accurate operation of this switched capacitor filter the capacitors  $C_1$  and  $C_2$  should be matched. However, as this filter is incorporated inside the feedback loop of the DDA, which is assumed to have a high loop gain, it later will be shown that the matching of the capacitors  $C_1$  and  $C_2$  is of much less importance. As will be shown in Subsection 5.2.5.2.6.1 the matching of the capacitors  $C_3$  and  $C_4$  is of more important than the matching of  $C_1$  and  $C_2$ . It will be shown that when switch  $S_5$  is replaced by its MOS counterpart, matching of the two capacitors will define better 50% channel charge redistribution to each side of the switch. In a later part of this section we will show that this defined charge distribution can be used to cancel charge injection onto output capacitor  $C_4$  by using so-called dummy switches.



**Figure 5.26** The timing diagram for the switches of the notching switched capacitor low pass filter

As will become clear during the following explanation of the new filter concept, switches  $S_1$ - $S_5$  will follow a predefined on and off switching sequence. It will perform two synchronized sample and hold phases followed by a time discrete charge-sharing/charge-redistribution phase.

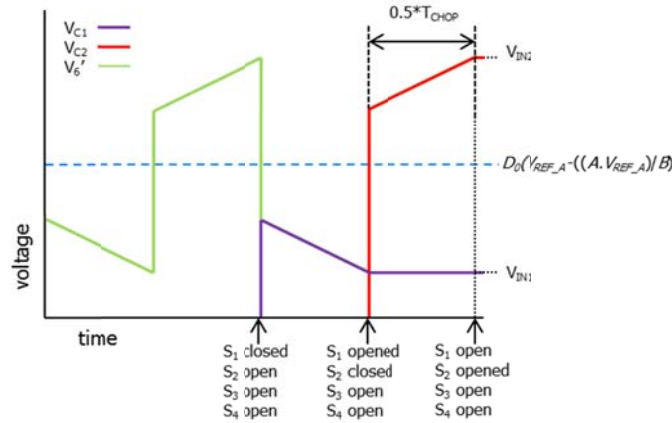
In Figure 5.26 the graphical representation of the control signals for the 5 switches is shown. The signals represent differential voltages. For the analyses to follow we assume that a switch will be closed (conducting) when its differential control signal is positive.

As denoted by the period counter  $n$  in Figure 5.26 (shown in the upper part of the figure) the signals sequence is repeated after 2 clock cycles of the chopper control signal. From the foregoing description we can conclude that the duration of  $n$  periods of the switching sequence equals

$$t_n = n \cdot 2 \cdot T_{chop} = n \cdot \frac{2}{f_{ch}} \quad (5.45)$$

To show how the switching sequence, as represented in Figure 5.26, is used to block the ripple of the input signal, we now start a step by step analysis of the new filter operation. For the sake of simplicity we assume ideal switches and a zero output impedance of the integrating trans-impedance stage which is the voltage source that delivers the voltage  $V_6'$  to the switched capacitor filter.

The first part of the operation will be explained by making use of Figure 5.27. The green line in this figure represents the output voltage  $V_6'(t)$  of the integrating trans-impedance stage which is known to be the input signal of the filter. The purple line in same figure represents the voltage over capacitor  $C_2$  and the red line the voltage over  $C_1$ .

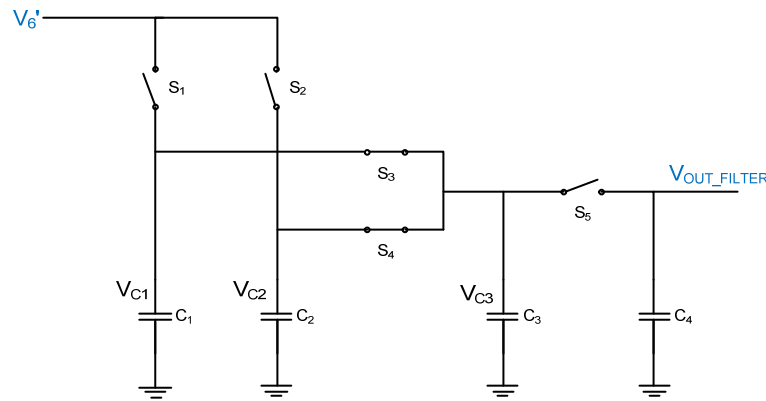


**Figure 5.27** Timing of the track and hold operation of the capacitors  $C_1$  (purple) and  $C_2$  (red)

As denoted by Figure 5.27 and already indicated by Figure 5.26 switch  $S_1$  is the one that closes at first. When switch  $S_1$  is closed capacitor  $C_1$  will start tracking the input signal  $V_6'(t)$ , resulting in a charge  $C_1 V_6'(t)$  on the top plate of  $C_1$ . At the next clock transition of the chopper control signal the switch  $S_1$  will be opened. When  $S_1$  is opened the charge  $Q_1 = C_1 V_{IN1}$  will remain on the top plate of capacitor  $C_1$ , where  $V_{IN1}$  is the sampled value of the input signal  $V_6'$  at the moment that switch  $S_1$  was opened. Immediately after  $S_1$  is opened switch  $S_2$  is closed such that  $C_2$  starts to track the input signal  $V_6'$ , resulting in a charge  $C_2 V_6'(t)$  on the top plate of  $C_2$ . At the following

chopper clock transition, switch  $S_2$  is opened, such that a charge  $Q_2 = C_2 V_{IN2}$  will remain on the top plate of capacitor  $C_2$ , where  $V_{IN2}$  is the sampled value of  $V_6'$  at the moment switch  $S_2$  opens. So, in this situation capacitors  $C_1$  holds a sampled value  $V_{IN1}$  and  $C_2$  holds a sampled value  $V_{IN2}$  of the input signal  $V_6'(t)$ . From Figure 5.27 we can see that the value corresponding to the DC component of the input signal  $V_6'$  is located exactly in the middle of the sampled values  $V_{IN1}$  and  $V_{IN2}$ . So this shows that after one clock cycle of the chopper control signal the mean value of the sampled voltages is already the wanted DC component of the input signal  $V_6'$ .

Now that we know the principle to get two sampled values exactly mirrored around the DC component of the input signal, the following is to examine the operation procedure of the filter that results in the mean value of two sampled voltages at the output of the filter.



**Figure 5.28** The configuration for charge balancing operation between the capacitors  $C_1$ ,  $C_2$  and  $C_3$

As indicated by Figure 5.26, at the moment that switch  $S_2$  is opened the switches  $S_3$  and  $S_4$  will be closed simultaneously. This will result in the situation as shown by Figure 5.28. We can see that in this situation both capacitors,  $C_1$  and  $C_2$ , will be connected to capacitor  $C_3$ . So charge redistribution between the capacitors  $C_1$ ,  $C_2$  and  $C_3$ , will occur till a charge balance between the three capacitors is reached.

When after a short time the charge is equally distributed over the three capacitors a steady state voltage will be reached which equals

$$V_{C3}(n) = \left( \frac{Q_1 + Q_2 + Q_3}{C_1 + C_2 + C_3} \right) = \left( \frac{V_{IN1}C_1 + V_{IN2}C_2 + V_{C3}(n-1)C_3}{C_1 + C_2 + C_3} \right) \quad (5.46)$$

Where  $V_{C3}(n-1)$  in Equation (5.46) denotes the voltage over  $C_3$  before it was connected to capacitors  $C_1$  and  $C_2$ .

Next operation of the system is to open switch  $S_3$  and  $S_4$  simultaneously, such that capacitor  $C_3$  will hold the steady state voltage,  $V_{C3}(n)$ . When  $S_3$  and  $S_4$  are opened,  $S_5$  will be closed such that charge redistribution between capacitors  $C_3$  and  $C_4$  is accomplished.

When the charge is balanced the steady state voltage over  $C_3$  and  $C_4$  will be

$$V_{OUT\_FILTER}(n) = V_{C_3}(n) = \left( \frac{V_{C_3}(n)C_3 + V_{OUT\_FILTER}(n-1)C_4}{C_3 + C_4} \right), \quad (5.47)$$

where  $V_{OUT\_FILTER}(n-1)$  denotes the voltage over the output capacitor  $C_4$  before  $S_5$  was closed.

From Equation (5.46) and (5.47) we can see that after the first cycle ( $n=1$ ), assuming that the voltages  $V_{C_3}(0)$  and  $V_{OUT\_FILTER}(0)$  were initially zero, capacitor  $C_4$  is only charged to a fraction of the final output value of the filter. However, it can be shown that when repeating the foregoing switching procedure the output of the filter will approach the DC component of the input signal.

We can show this by first rewriting Equation (5.46) to

$$V_{C_3}(n) = \left( \frac{V_{C_1}C_1 + V_{C_2}C_2 + V_{OUT\_FILTER}(n-1)C_3}{C_1 + C_2 + C_3} \right) \quad (5.48)$$

As can be seen we have replaced  $V_{C_3}(n-1)$  by  $V_{OUT\_FILTER}(n-1)$  as they are actually representing the same voltage. With the use of Equations (5.47) and (5.48) we can now build an overall equation for  $V_{OUT\_FILTER}(n)$ .

$$V_{OUT\_FILTER}(n) = \frac{\left( \frac{V_1C_1 + V_2C_2 + V_{OUT\_FILTER}(n-1)C_3}{C_1 + C_2 + C_3} \right)C_3 + V_{OUT\_FILTER}(n-1)C_4}{C_3 + C_4} \quad (5.49)$$

This can be rewritten to

$$V_{OUT\_FILTER}(n) = V_{OUT\_FILTER}(n-1) \frac{(C_3^2 + C_4(C_1 + C_2 + C_3))}{(C_1 + C_2 + C_3)(C_3 + C_4)} + \frac{(V_1C_1 + V_2C_2)C_3}{(C_1 + C_2 + C_3)(C_3 + C_4)} \quad (5.50)$$

Now, when we assume

$$\frac{C_3^2 + C_4(C_1 + C_2 + C_3)}{(C_1 + C_2 + C_3)(C_3 + C_4)} = A \quad (5.51)$$

$$\frac{(V_1C_1 + V_2C_2)C_3}{(C_1 + C_2 + C_3)(C_3 + C_4)} = B, \quad (5.52)$$

equation (5.50) can be simplified to

$$V_{OUT\_FILTER}(n) = V_{OUT\_FILTER}(0)A^n + B \sum_{k=0}^n A^{k-1} (1 - 0^n) \quad (5.53)$$

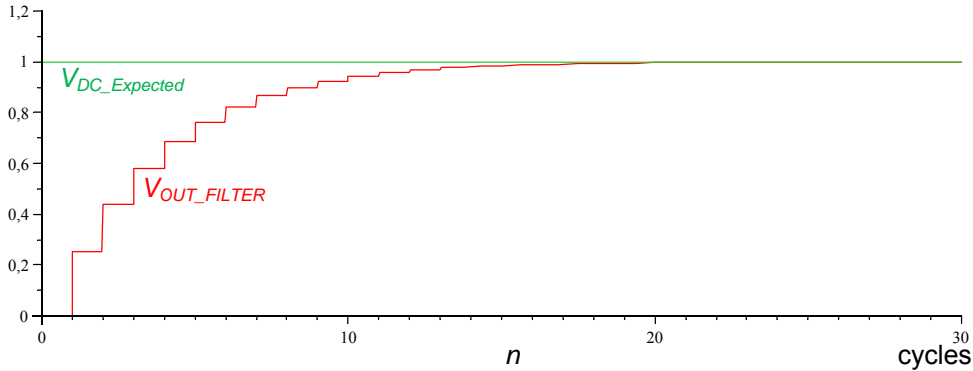
The difference in percentage, from the expected DC output voltage  $V_{DC\_Expected}$ , after  $n$  cycles, can be calculated by

$$\delta V_{DC\_Expected} = \frac{V_{OUT\_FILTER}(0)A^n + B \sum_{k=0}^n A^{k-1}(1-0^n)}{V_{DC\_Expected}} \cdot 100\%, \quad (5.54)$$

where

$$V_{DC\_Expected} = \left( \frac{V_{IN1} \cdot C_1 + V_{IN2} \cdot C_2}{C_1 + C_2} \right) \quad (5.55)$$

Now let's put Equations (5.53) and (5.54) into practice. Let's assume that the values of the capacitors are chosen to be  $C_1=C_2=0.5\text{pF}$  and  $C_3=C_4=1\text{pF}$  and that the input signal is a 10MHz chopper modulated voltage with an modulation amplitude of 300mV superposed on top of a DC voltage of let's say 1V. Furthermore, assume that the sampled values of the input signal are exactly mirrored around the 1V DC component of the input signal. Let's say  $V_{IN1}=1.2\text{V}$  and  $V_{IN2}=0.8\text{V}$ .



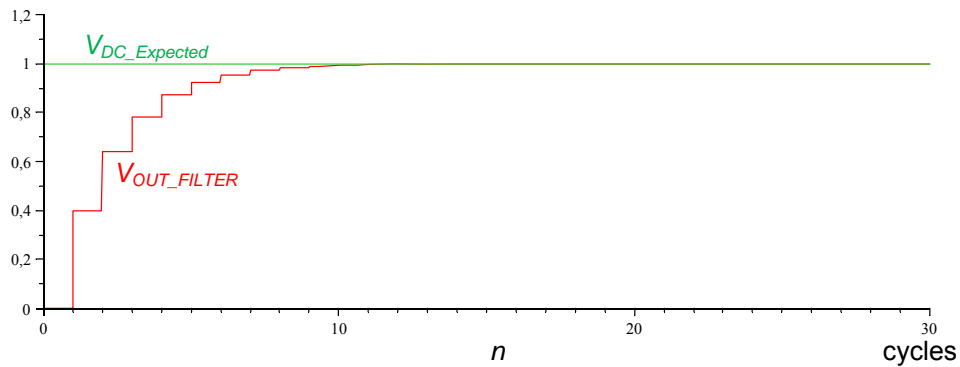
**Figure 5.29** Idealized filter response for  $C_1=C_2=0.5\text{pF}$  and  $C_3=C_4=1\text{pF}$

Now, when we plot the result of Equation (5.53) and (5.55) into Figure 5.29, we can see that after some cycles the filter converges towards the wanted 1V DC component of the input signal.

Equation (5.54) shows us that the filter will take about  $n=18$  cycles to get to 99.4% of the final value. With a chopping frequency of 10MHz, Equation (5.45) will show us that in this situation the filter response would take around  $3.6\mu\text{s}$  to reach the ripple free DC output voltage of 1V.



### 5.2.5.2.2 Response time



**Figure 5.30** Idealized filter response for  $C_1=C_2=1\text{pF}$  and  $C_3=C_4=0.5\text{pF}$

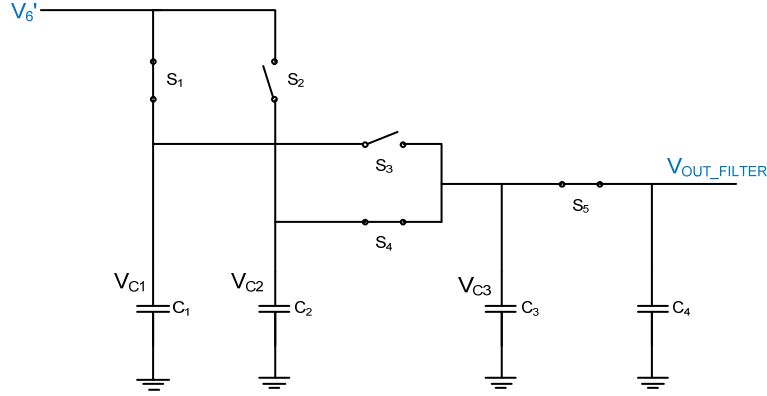
When we repeat the procedure of the previous example, but now with capacitor values of  $C_1=C_2=1\text{pF}$  and  $C_3=C_4=0.5\text{pF}$ , the filter will take about  $n=10$  cycles to get to 99.4% of the final DC output voltage, as shown in Figure 5.30. With a chopping frequency of 10MHz the filter would take in this situation around  $2\mu\text{S}$  to converge towards its final value.

As expected from the knowledge we gathered from the section about switched capacitor filters, the response time will depend on the ratio between the capacitors that are used. The values taken for the examples above were arbitrary. For the condition  $(C_1+C_2)>C_3>C_4$  the amount of charge delivered per cycle  $n$  to  $C_4$  will be higher than for the condition  $(C_1+C_2)<C_3<C_4$ . It is not difficult to see that first condition will lead to a faster response time. Not shown, but already discussed in the section about switched capacitor filters, is that an increase of the chopper frequency will also result in a faster response.

As the response depends on the ratios rather than on the capacitor values, the ripple blocking can be obtained with relatively small sized capacitors. This shows that a low pass filter with a fast response time and very low cut-off frequency can easily be implemented with on chip capacitors.

Of course when incorporated inside the DDA feedback loop the time constant of the filter has to be taken into account. The time constant of the integrating trans-impedance stage and ripple blocking system together has to be chosen in such a way that a stable feedback system is realized. This shows that when implemented inside the negative feedback system we don't have all the freedom to choose the capacitor ratio.

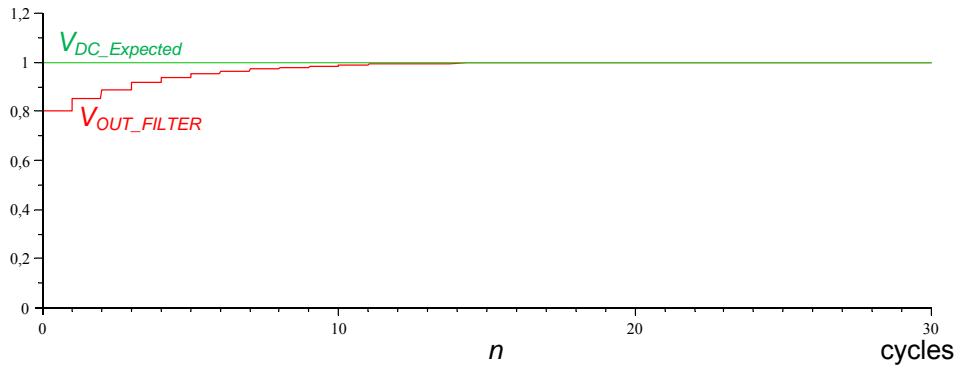
Fortunately we can expect a considerably faster start-up time of the filter when placed inside the loop of the feed-back system, even for the condition  $(C_1+C_2)<C_3<C_4$ . This is a result of the overshoot of the filter input signal when incorporated in the DDA feedback system. As the overshoot at the input is higher than the final input signal the amount of charge transported to capacitor  $C_4$  during this overshoot can be expected to be much higher than when there is no overshoot. So, the voltage build up at  $C_4$  is increased during the overshoot at the input, which will lead to a faster approach of the final filter output signal, in comparison with a critically damped system.



**Figure 5.31** Start-up configuration to boost response time of the notching switched capacitor filter.

We have to note that there is a small modification possible in the switching algorithm which can possibly give a faster response time during start up. This performance boost can be obtained by closing switch  $S_1, S_3$  and  $S_5$  for a small time before the switching cycle, as discussed earlier, is started. The start situation is shown in Figure 5.31. As can be seen from this figure the capacitors  $C_1, C_3$  and  $C_4$  are put in tracking mode during start up. Because of the tracking mode, the initial voltages  $V_{C3}(0)$  and  $V_{OUT\_FILTER}(0)$  will already be charged to the input voltage  $V_6'(t)$ . In this situation the output of the filter can be set closer to the expected DC output voltage before the switching algorithm is started. This method can give a tremendous response time boost when relatively small rippled input signals have to be filtered or when it is known how an initial value close to the final output voltage can be obtained.

For example when we used this method for second last example ( $C_1=C_2=0.5\text{pF}$   $C_3=C_4=1\text{pF}$ ) by assuming an initial voltages of  $0.8\text{V}$ , a start-up response as shown in Figure 5.32 will be obtained. Where it first took 18 cycles to reach 99.4% of its output voltage it will now only take 12 cycles. Let's say we take 1 clock cycle of the  $10\text{MHz}$  chopper clock to initialise, known to be  $T_{chop}$ , the total time to converge towards its final value will now take around  $2,5\mu\text{s}$  instead of  $3.6\mu\text{s}$ . This shows that the start-up time can be decreased with this modification.

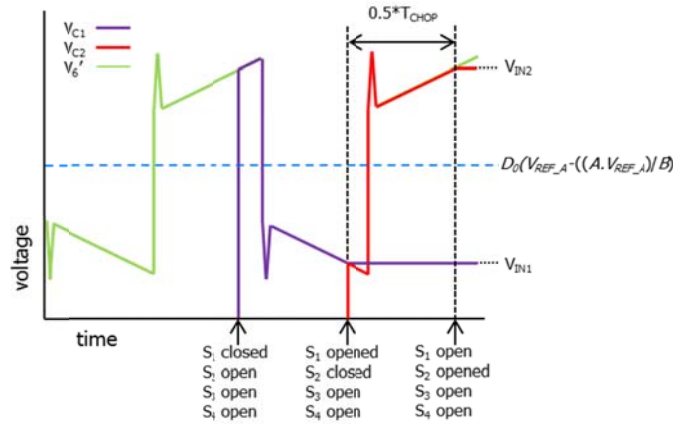


**Figure 5.32** Output response (red) of the notching switched capacitor filter with boosted response time.

### 5.2.5.2.3 Insensitiveness to switching effects of the chopped system

In Figure 5.27 it was shown that the sample values  $V_{IN1}$  and  $V_{IN2}$  were exactly taken during the fast voltage transitions of  $V_6'$ . For the practical implementation we have to be sure that sampling doesn't take place at these fast transition. Sampling during a transition can result in in-accurate sample values as the characteristics of the signal during these transition depends too much on non-idealities of the switches and chopper control signal. Furthermore, as noted earlier a higher chopping frequency will lead to a faster start-up time of the filter but also to greater and more spikes over time. This indicates that switching side-effects, caused by these non-idealities, normally lead to a trade-off between speed and precision.

Fortunately, the new filter concept can sample the input signal during the spike-free intervals, making it less sensitive to spikes and other non-idealities caused by switching. The best results can be obtained when  $V_6'$  is sampled just before a transitions occurs, as is shown in Figure 5.33.



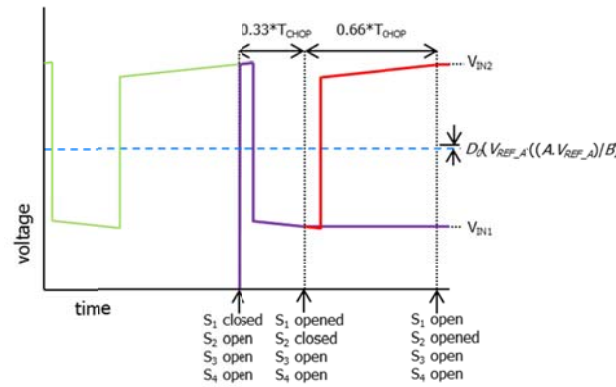
**Figure 5.33** Output response of filter can be made in-sensitive for chopper switching effects when signal is sampled just before transitions

As shown by Figure 5.27 the sampled values  $V_{IN1}$  and  $V_{IN2}$  will be in-sensitive to the switching effects caused by the chopper switches. Fortunately, because of the integrating action of our trans-impedance stage the needed delay is already implemented, as will be shown by the simulation results which will be discussed in Chapter 6 of this thesis

### 5.2.5.2.4 Low sensitiveness to duty cycle variations of chopper clock

As the timing of the switches is extracted from the chopper control signal the switches of the filter will follow the same duty cycle as the chopper control signal. As the method is based on the mean value of the two sample values instead of the average value of signal  $V_6'$  the filtering method will have a much lower sensitive to duty cycle variations. From the signal example shown in Figure 5.34 it can be seen that even for a duty cycle of 66% the mean value of the sampled values will still be close to the wanted DC component. The sensitiveness on the duty cycle depends on the voltage ramps of signal  $V_6'$ . From Equation (5.44) it was shown that the voltage ramp is defined by capacitor  $C_1$  and error current  $I_5$ . In the extreme case when there is no voltage ramp the filter system could be made insensitive to duty cycle variations. This property can be interesting for open loop chopped systems with relatively low gain. However as our filter is incorporated in the feedback loop of the DDA and the output of the integrator inside the DDA is

still depending on the duty cycle of its input signal the feedback system will still be sensitive to the duty cycle.

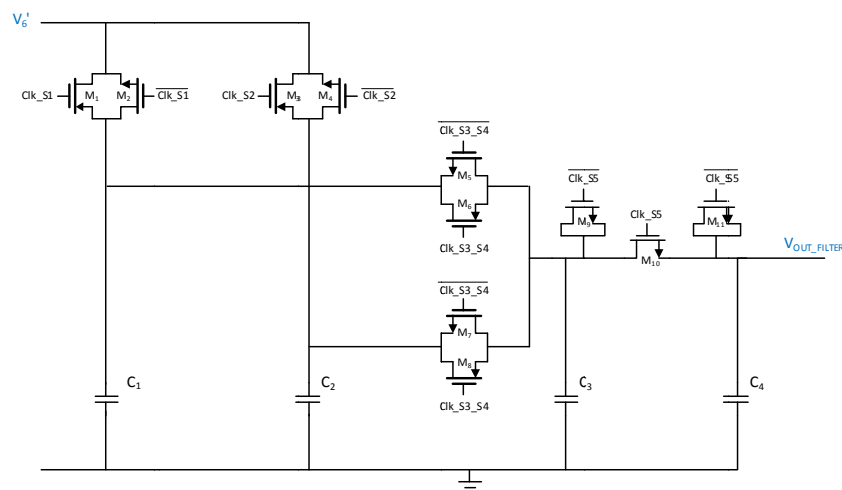


**Figure 5.34** Output response of filter has low sensitivity to duty cycle variations of the chopper clock

### 5.2.5.2.5 A Power efficient and low noise approach

A final note about the circuit. As the filter uses capacitors as memory cells the output voltage over capacitor  $C_4$  can be held for a while. As was shown by Figure 5.22 we use a MOS transistor  $M_4$  configured as source follower to buffer the output of the ripple blocking system. The ideally infinite gate impedance at DC of this MOS transistor will prevent that current is leaking away from output capacitor  $C_4$ . Because of the discrete nature of the system and the minimal current leakage from capacitor  $C_4$ , the output voltage of the filter can be locked up easily. As the filter is incorporated inside the loop the lock up principle can be used to keep the multiplication cell  $M_{real}$  and the cascaded A/D cells biased while the rest of the fixation system can be turned off for a predefined time. The maximum lockup time depends on the fastest changing parameter over time for which the fixation system has to be corrected, which is in our case the temperature. This shows a possibility to save much power for this fixation system, as temperature normally is a relatively slowly changing parameter. When the system is in lock-up mode the bias voltage of  $M_{real}$  and the cascaded A/D cells will only be supplied by a buffered capacitor configuration which can have a very low noise contribution when relatively big MOS buffer geometries are used.

### 5.2.5.2.6 Final circuit implementation of the ripple blocking system



**Figure 5.35** Final circuit implementation of the new ripple blocking system

Figure 5.35 shows the final circuit implementation of the new filter concept. As shown by this figure the switches  $S_1$  and  $S_2$  are replaced by transmission gates  $M_1$ - $M_2$  and  $M_3$ - $M_4$ . These transmission gates obtain low on-resistance and decrease the amount of charge injection. With the same reasoning the switches  $S_3$  and  $S_4$  were replaced by a transmission gate. The output switch  $S_5$  is replaced by three single MOS switches,  $M_9$ ,  $M_{10}$  and  $M_{11}$ , where  $M_9$  and  $M_{11}$  are used as dummy switches, to circumvent that channel charge of  $M_{10}$  is injected into capacitor  $C_4$ .

#### 5.2.5.2.6.1 Non-idealities in the ripple blocking system

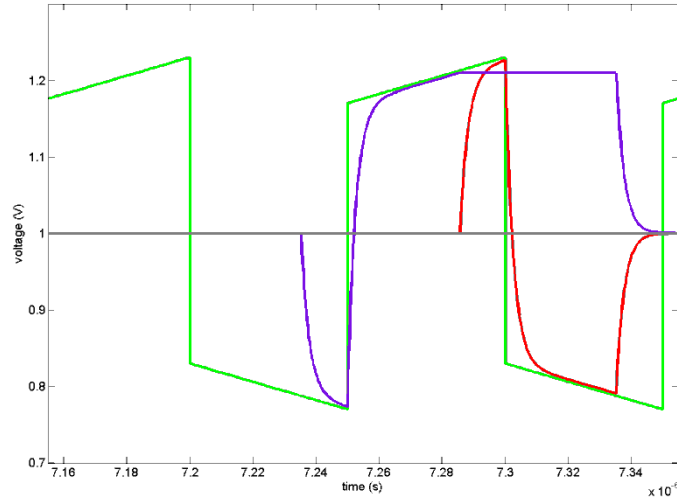
As already indicated in the previous circuit description, we have to deal with component non-idealities in the system. In following sub sections more of these non-idealities and the way how we solved them will be discussed.

#### On resistance of the track and hold switches

One of the various non-idealities which have to be taken into account is the on-resistance of the track and hold switches. In Subsection 5.2.5.2.1 we assumed ideal switches with zero on-resistance and a zero output impedance of the trans-impedance stage. In this circumstance the track and hold capacitors  $C_1$  and  $C_2$  are charged infinitely fast to the voltage of interest. However, when switch  $S_1$  and  $S_2$  are replaced by real MOS switches, which are known to have non-zero on-resistance, the characteristics of the filter system will change.

The on-resistance of a MOS switch together with the capacitance of the track-and-hold capacitor  $C_1$  or  $C_2$  will form a time constant. The bigger the capacitance of the track and hold capacitor and/or on-resistance of the MOS switch the longer the charging time of the capacitor will be. In other words the time constant increases. When the frequency of the chopper clock is too fast in comparison with this time constant, the capacitors will not completely charge. This will lead to a slower response than that of the ideal filter because the amount of charge delivered to  $C_4$  per cycle  $n$  will be lower.

It is very interesting to note that the accuracy of the system itself will not decrease with large time constants. The output will still get to the correct DC component of the input signal. When the capacitors  $C_1$  and  $C_2$  cannot exactly track the input signal at the moment of sampling this will result in sampled values which will still be exactly mirrored around the wanted DC component of the modulated input signal, as is shown in Figure 5.36. This means that the capacitor values for  $C_1$  and  $C_2$  can be relatively big.

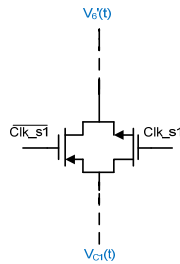


**Figure 5.36** The slow tracking response as result of big but equal time constants seen at the upper plates of  $C_1$  (red line) and  $C_2$  (purple line) doesn't lead to a wrong final output signal (gray signal).

We have to note that both time constants in this situation should be equal to each other. As the time constant will add a phase shift to the tracked signal, different time constants will lead to sampled values which are not exactly mirrored around the DC component.

In the previous explanation the on-resistance of the switches were assumed to be constant. However, when the switches  $S_1$  and  $S_2$  are replaced by a simple MOS switch, the on-resistances of the switches during tracking depend very much on their  $V_{GS}$ . As we deal with an input signal with unknown ripple values, the sample values can be almost anywhere in-between  $V_{DD}$  or  $V_{SS}$ . As the  $V_{GS}$  of a single MOS switches depends on the input signal  $V_6'(t)$  and the control signal value at the gate, the on-resistance of a single MOS switch will greatly vary with the input voltage. This would mean that both track and hold switches would have different on-resistance at the moment of sampling resulting in different time constants. To guarantee a low on-resistance and thus acceptable and matched time constants over a broad input signal range transmission gates were implemented.

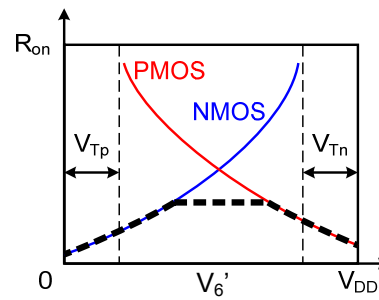
The transmission gate implementation of switch  $S_1$  is shown in Figure 5.37.



**Figure 5.37** Switch  $S_1$  implemented as transmission gate to guarantee low on-resistance over the full voltage range of the filter input signal  $V_6'$ .

Instead of one MOS transistor the transmission gates uses two MOS transistors in parallel. The control signal of both transistors are complimentary. Because of the complimentary control signal, both transistors will be on or off at the same time. Knowing that the PMOS has low on-resistance for high values of  $V_6'$  while the NMOS has low on resistance for low values of  $V_6'$  the parallel

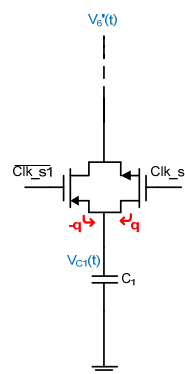
connection of both devices, will result in a more constant and low on resistance over the full voltage range of  $V_6'$ , as shown in Figure 5.38.



**Figure 5.38** On-resistance of transmission gate (black dotted line) shows more constant and low on-resistance over the full voltage range of  $V_6'$

### Charge injection by the sample and hold switches

Charge injection originating from clock feedthrough and channel distribution, as discussed in the section about the chopper switches, can be another concern. When  $S_1$  and  $S_2$  are replaced by their MOS counterparts they will generate spikes during their switching operation. The spikes itself will not be seen at the output of the filter. However, the output is affected in a different way. The charge spikes lead to an additional voltage at capacitors  $C_1$  and  $C_2$ . In this case the sampled values will not exactly mirror around the DC component of the input signal  $V_6'$ . The additional voltages on both track and hold capacitors translate into a disturbance of the filter output voltage in the form of a DC shift. To decrease this voltage shift error we can increase the capacitance of capacitor  $C_1$  and  $C_2$ . However there is another possibility that can help to decrease the problem. Actually the problem is already decreased by the implementation of the complimentary switch discussed in the previous subsection. From the previous subsection we know that the complimentary switch structure is used to lower the on-resistance. Fortunately the complimentary architecture of the switch is also useful to lower its charge injection. How the complimentary switches reduce the charge injection can be seen at the implementation of switch  $S_1$  in Figure 5.39.



**Figure 5.39** Transmission gate reduces the effect of charge injection which is a result of the recombination of opposite charged channel carriers

As shown by this figure the opposite charge packets (positively charged holes and negatively charged electrons) injected by the two MOS transistors cancel each other. However, from [64] we know that complete cancellation will only occur for one particular input level.

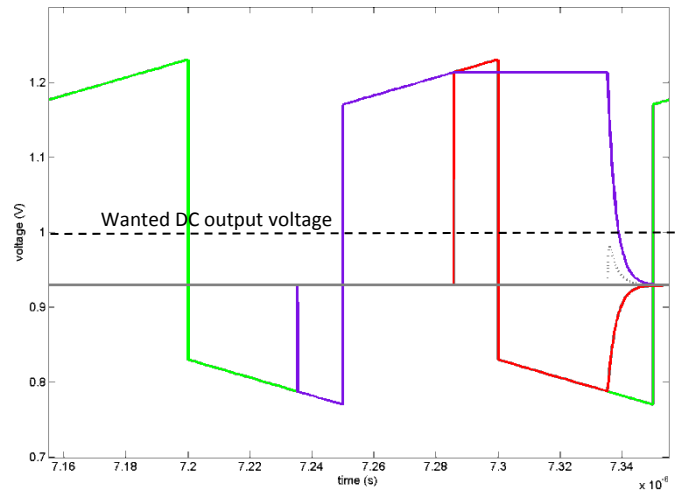
Another feature of transmission gates is that it suppresses spikes originating from clock feed-through. As the clocking signal of the PMOS and NMOS are complimentary the spikes resulting from the fast clock transitions will be in opposite direction such that they will cancel each other. However, as it was for charge cancelation operation of the transmission gate the cancelation of the spikes will only occur at one particular input voltage. To reduce spike and charge injection in this situation one could think about using so-called bootstrapping.

### Mismatch between the track and hold capacitors

Another point of concern can be the possible mismatch between capacitors  $C_1$  and  $C_2$ . Mismatch can be reduced at layout level by using big geometry capacitors, interleaving, cross coupling and common centroid structures. As we can conclude from earlier discussions mismatch between the two track and hold capacitors  $C_1$  and  $C_2$  will lead to different time constants during both tracking moments. But, more importantly, it will result in a deviation of the wanted DC output in the form of a DC voltage shift. The percentage error from a matched situation can be calculated by the following equation.

$$\varepsilon_{DCout} = abs \left( \left( 1 - \frac{\frac{abs(V_{IN1} - V_{IN2})}{2} + \min(V_{IN1}, V_{IN2})}{\left( \frac{V_{IN1} \cdot C_1 + V_{IN2} \cdot C_2}{C_1 + C_2} \right)} \right) 100\% \right) \quad (5.56)$$

As shown by Equation (5.56), the amount of error caused by un-equal capacitor values depends on the sampled values. The closer the sampled values are mirrored around the DC component of the filter input signal the smaller the error caused by the mismatch. As we know, the sampled values itself depend on the amplitude of the modulation ripple and the moment that it is sampled.



**Figure 5.40** Input signal  $V_0'$  (green line) correctly tracked and sampled by  $C_1$  (purple line) and  $C_2$  (red line). Final output signal (gray line) shows a 7 percentage deviation from wanted DC output signal (black dotted line) for a 200 percentage mismatch between the capacitors  $C_1$  and  $C_2$

When for example the capacitance of  $C_1$  is two times bigger than that of  $C_2$  (mismatch of 200%) while the sampled values are correctly mirrored around the wanted DC value, for example



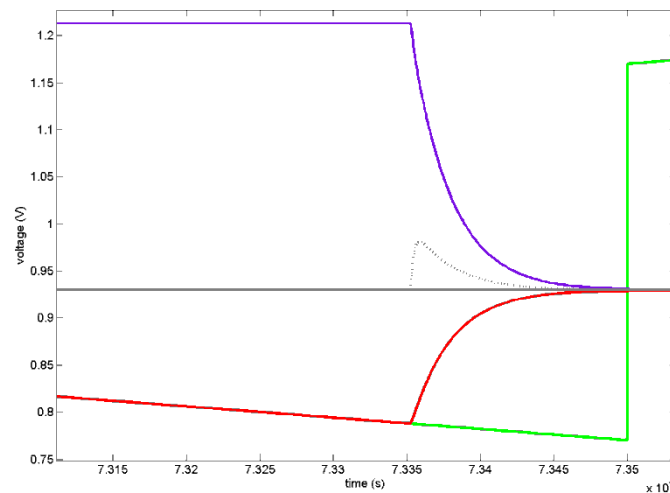
1.213V and 0.787V, the DC output voltage of the filter will deviate 7% from the 1 volt DC component. The signal and resulting output of the filter is shown in Figure 5.40. As shown by this figure a (unrealistic) big mismatch ( $C_2/C_1=0.5$ ) between both capacitors doesn't have to mean that the deviation from the expected DC component will be that big. It all depends on the ripple magnitude and the moment of sampling. Fortunately, the DC shift error at the output of the filter, caused by capacitor mismatch, will be tremendously reduced because of the negative feedback configuration of the DDA, as will be shown later.

### On-resistance of the charge redistribution switches

As we know from previous the switches  $S_3$  and  $S_4$  are used for redistributing the charge of capacitors  $C_1$ ,  $C_2$  and  $C_3$ . When implemented by their MOS counter parts their on resistance has to be taken into account. As was the case for the track and hold switches the voltages that switches  $S_3$  and  $S_4$  have to process can be anywhere in between  $V_{DD}$  and  $V_{SS}$ . So, to ensure low on-resistance over the full voltage range of the possible sample values we implemented transmission gates as switches.

### A-symmetrical discharge of the track and hold capacitors

When the capacitors  $C_1$  and  $C_2$  have different values the voltage change over both capacitors during their charge redistribution to  $C_3$  will not proceed symmetrically around the final value before charge balance occurs. When we take a closer look at previous figure we can see that during the a-symmetric discharge the voltage on  $C_3$  jumps shortly.



**Figure 5.41** Voltage jump at capacitor  $C_3$  (gray dotted line) as a result of unequal charge distribution between capacitor  $C_1$  and  $C_2$

In Figure 5.41 we have zoomed in on this phenomenon.

Beside that differences in capacitance of  $C_1$  and  $C_2$  will lead to this phenomenon, more non-idealities (such as unequal switching timing and difference in on-resistance of the complimentary

MOS switches  $M_5$ - $M_6$  and  $M_7$ - $M_8$ ), will lead to a-symmetrical discharge. Fortunately, as long as the capacitors  $C_1$  and  $C_2$  are matched these non-idealities will not lead to a corrupted value of the steady state DC at the output of the filter.

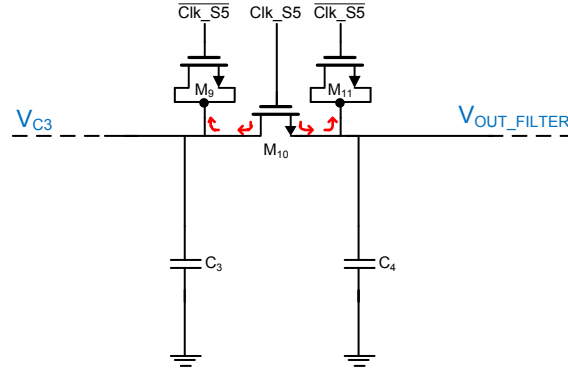
To prevent that the voltage jump at  $C_3$  is passing through the output of the filter, switch  $S_5$  and capacitor  $C_4$  have been added. How this can help to prevent the jump not to reach the output of the filter can be explained as follows.

From earlier discussions we know that  $S_5$  is still open during charge balancing of  $C_1$ ,  $C_2$  and  $C_3$ . As switch  $S_5$  is open during this operation it actually isolates the output of the filter from capacitors  $C_1$ ,  $C_2$  and  $C_3$ . So, with this implementation we give these capacitors the time to reach their steady state voltage value before the charge of  $C_3$  is redistributed to output capacitor  $C_4$ . When at the next clock cycle switches  $S_3$  and  $S_4$  are opened, immediately followed by a closing action of switch  $S_5$ , charge balancing will now only occur between capacitors  $C_3$  and  $C_4$ . Once the output of the filter has reached its final DC value there will be in the ideal case no longer charge balancing between  $C_3$  and  $C_4$ . This will result in a ripple-free output, as shown by the grey solid line in Figure 5.41.

When the final output voltage of the filter is reached there will be a charge balance between the matched capacitors  $C_3$  and  $C_4$ . In this situation there will be no current flowing through MOS switch  $M_{10}$ . As in this situation the on-resistance of this switch will be of no concern in terms of voltage drop one could think to implement the switch by a single transistor. However as already introduced earlier the output switch  $S_5$  is replaced by the MOS switches  $M_9$ ,  $M_{10}$  and  $M_{11}$ . The reason to use 3 switches to implement the operation of the output switch will be explained in the following section.

### **Charge injection caused by the output the switch**

One of the non-idealities of switch  $S_5$  we have to take into account is the charge injection when it is replaced by its real MOS implementation. When  $S_5$  is replaced by a single MOS transistor, it will inject a part of its channel charge onto capacitor  $C_4$  when it is switched off. This injected charge will add an additional voltage onto capacitor  $C_4$  resulting in a wrong value at the output of the filter. As the filter is incorporated inside the loop of the fixation system, the feedback loop will try to correct for this wrong output value. However, because of the discrete nature of the loop it will not be able to nullify this error, resulting in an alternating output, where the resulting ripple will depend on the amount of charge injected by the MOS switch. One solution to lower this ripple would be the choice of a bigger capacitance of  $C_4$ . Fortunately there was another solution found which showed a better performance and can be implemented with a relatively small capacitor value. The solution, as already note earlier, is to add so-called dummy switches and ensure that  $C_3$  and  $C_4$  are properly matched [65]. Note that capacitors can be matched with high accuracy, even better than 0.1% [55]. The ultimate configuration is shown in Figure 5.42.



**Figure 5.42** When the impedances at both sides of MOS switch  $M_{10}$  are equal the injected channel charge during switching will be forced to split almost equally between the source and the drain. Half sized dummy switches  $M_9$  and  $M_{11}$  will use these halve sized channel charge packages to create their own channel.

During the fast clock transitions of  $Clk\_S5$  the impedance levels of capacitors  $C_3$  and  $C_4$  will dominate. Because of the matched low impedance levels of the capacitors during the switching action the channel charge of  $M_{10}$  will be forced to split almost equally between the source and drain of  $M_{10}$ . By adding half-sized dummy switches  $M_9$  and  $M_{11}$  (in comparison with MOS switch  $M_{10}$ ), controlled by a clock signal, which is complementary to the clock signal of MOS switch  $M_{10}$ , the injected 50% channel charge of switch  $M_{10}$  will be completely used to generate a channel in dummy switch  $M_9$  and  $M_{11}$ . As a result no additional charge will be injected into  $C_4$ . Furthermore, for even better matching the capacitor values of  $C_3$  and  $C_4$  should be chosen much bigger than the expected parasitic capacitances connected at each node of the source and the drain of  $M_{10}$ .

### Switching timing of the track and hold switches

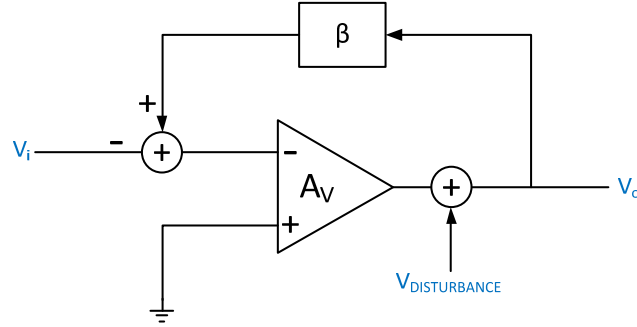
Apart from a precise timing of the control signal itself, non-ideal switches will have a finite turn-on and turn-off switching time which can deviate per switch. So, in reality, very precise timing between the opening of switch  $S_1$  and the opening of switch  $S_2$  will be difficult to obtain. As we explained earlier this timing is important, in order to have two sampled values,  $V_{IN1}$  and  $V_{IN2}$ , which are exactly mirrored around the wanted DC output.

An interesting property of the new filter concept is that when the input of the filter approaches a rectangular waveform the timing of the switches doesn't have to be that accurate, because the value to be sampled will not change that much over small deviations of the switches closing time. So, according to Equation (5.44) the DDA circuit shown in Figure 5.23 can lower the effect of switching timing error by increasing the value of its integrating capacitor  $C_1$ .

### Voltage offset at the output of the filter

For the most accurate operation it is important to have as less as possible voltage offset at the output of the filter. However it can be shown that this mainly holds when it is used in an open loop configuration. The voltage disturbance at the output of the filter, caused by for example the charge injection or unmatched capacitors  $C_1$  and  $C_2$ , will be of much less concern when the filter is incorporated in the feedback loop of the DDA. This is because, when incorporated inside the loop of the negative feedback system, the high loopgain will decrease the effect of this error

considerably. The favourable effect of high loop gain can be explained by the following simple example. In Figure 5.43 an example of a negative feedback loop configuration is shown. As shown in this system we included a disturbance voltage at the output of the error amplifier.



**Figure 5.43** Voltage offset  $V_{DISTURBANCE}$  at the output of an high gain differential amplifier in negative feedback configuration.

When analysing the system the following equation can be constructed

$$V_o = V_{DISTURBANCE} - A_v(\beta V_o - V_i) \quad (5.57)$$

Solving for the output voltage  $V_o$  leads to

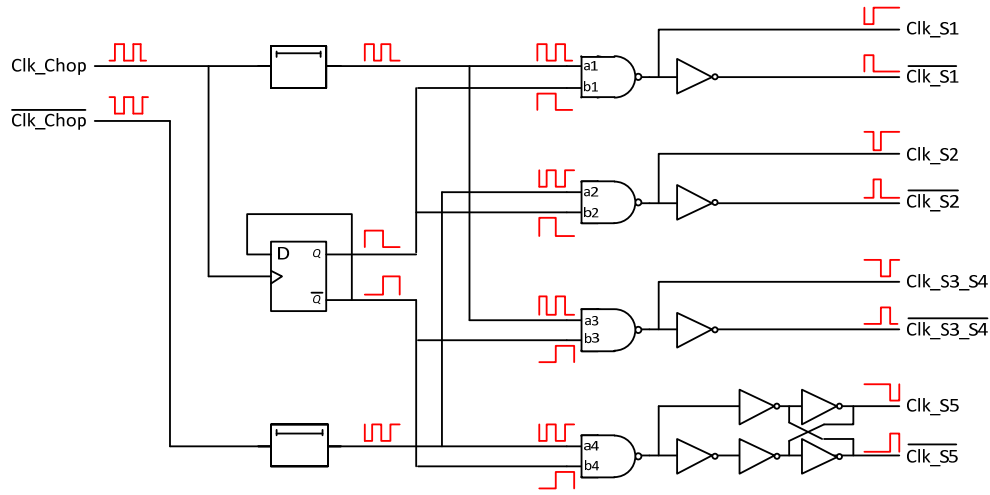
$$V_o = \frac{A_v}{(1 + A_v\beta)} V_i + \frac{1}{(1 + A_v\beta)} V_{DISTURBANCE} \quad (5.58)$$

This equation shows that  $V_{DISTURBANCE}$  is suppressed by factor  $1/(1+A_v\beta)$ , where  $A_v\beta$  is the loopgain. This means that the effect of an additional voltage shift at the output of the filter will be reduced by the loop gain of the system. Thus, the high loop gain of the negative feedback configuration relaxes the need of matching the capacitors  $C_1$  and  $C_2$  and the need of accurate charge compensation of both capacitors.

Now that we have discussed the operation principle of the new filter we will now start to discuss the implementation of the timing circuit that we used to generate the needed switching sequence.

### 5.2.5.3 Clock generator (CG) circuit for the notching switch capacitor filter

In this section the Clock Generator (CG) circuit, used for controlling the switches of the Notching Switched Capacitor Filter (NSC-F), will be discussed. As we discussed in the previous section the switches of the notching switched capacitor filter, as was shown in Figure 5.35, has to follow a predefined turn-on and turn-off sequence, which has to be synchronized with the chopper clock. The logic circuitry to generate this synchronized turn on and turn off sequence is shown in Figure 5.44



**Figure 5.44** The proposed control circuit for the notching switched capacitor filter

As shown in this figure, we have implemented two delay blocks. Furthermore we implemented a Data Flip Flop (D-FF) configured as Toggle Flip Flop such that it acts as a clock divider. The clock divider configuration we used is the same as was discussed in Section 5.1. Furthermore we have implemented 4 NAND ports followed by an inverter, to generate 4 complimentary clock outputs.

The cross coupled inverter configuration at the complimentary output of NAND 4 is implemented to obtain a more symmetrical differential clocking signal with faster transitions at the switch  $M_{10}$  and the two dummy switches  $M_9$  and  $M_{11}$  shown in Figure 5.35. This implementation will increase the chance of the 50% channel redistribution to both sides of the MOS switch  $M_{10}$ , such that it increases the effectiveness of the charge cancellation by the dummy switches [65].

One critical property of the circuit is that it can produce glitches at differential outputs. These glitches which usually are unwanted voltage spikes are a result of the unbalanced propagation delays of the gates [73]. The voltage spikes can corrupt the on-off states of the switches of the switched capacitor filter. However it can be shown that by the implementation of the delay blocks the glitches can be removed from the critical outputs nodes. Without the delay blocks the spike would happen at capacitor  $C_1$  (Figure 5.35), at the moment that  $C_1$  is already holding the sampled voltage  $V_{IN1}$ . In this situation the spike will add extra charge to capacitor  $C_1$  which will result in an additional voltage superimposed on voltage  $V_{IN1}$ . However, with the delay blocks, the spike and thus charge injection will not happen at  $C_1$  but at capacitor  $C_2$ . Fortunately in this situation the charge injection will occur at the moment that the sampling capacitor  $C_2$  is still waiting for its tracking operation. As the tracking mode of  $C_2$  will be activated at the next clock transition of the chopper clock, the added voltage caused by the charge injection will be nullified during this mode. The spike at NAND 4 will not harm because of another reason. The spike processed by NAND 4 is blocked by the cross coupled inverter configuration at the output of NAND 4.

Now that we have discussed the full architecture of the clock generator we now can look at the rest of its operation principle. As shown in Figure 5.44 one side of the delayed control signal is connected to NAND-port  $a1$  and NAND-port  $a3$  while the other side of the delayed clock signal is connected to NAND-port  $a2$  and NAND-port  $a4$ . In same figure it is shown that the clock divider will impose half of the time a positive input at NAND-port  $b1$  and NAND-port  $b2$  and the

other half at NAND-port b3 and NAND-port b4. This will cause the output of NAND1 and NAND2 to convey the delayed control signal at the input terminal to the output for half of the period of the divided clock signal, while NAND3 and NAND4 will do the same during the other half. This results in the wanted complementary control signals for the 5 switches shown in Figure 5.35.

## 5.2.6 Final circuit implementation

In this section the final circuit implementation of the multiplication fixation system will be discussed. Figure 5.45 shows the top level of the final implementation of the gain stabilization circuit. The circuit implementation of the chopper stabilized DDA is shown in Figure 5.46

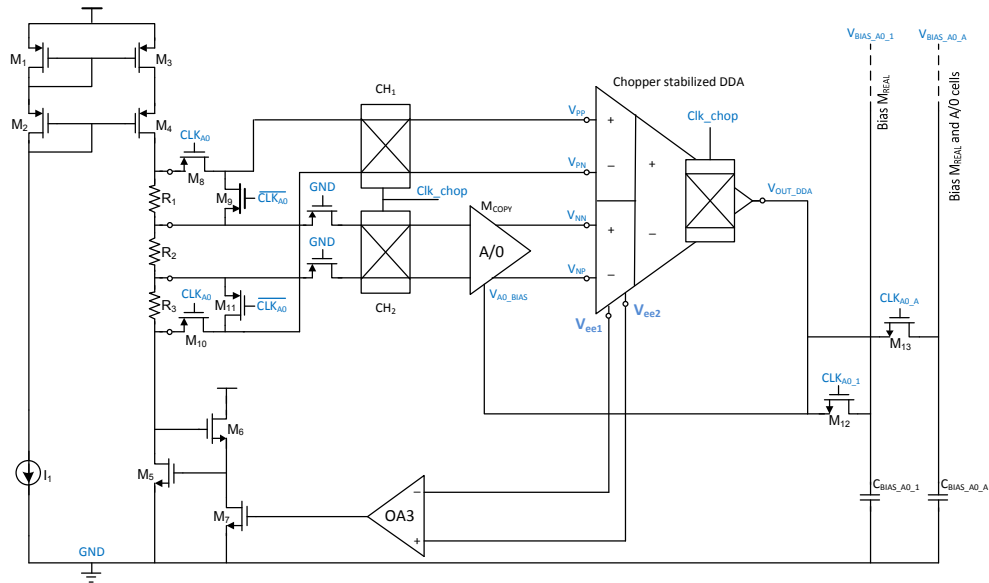


Figure 5.45 Final circuit implementation of the gain fixation system

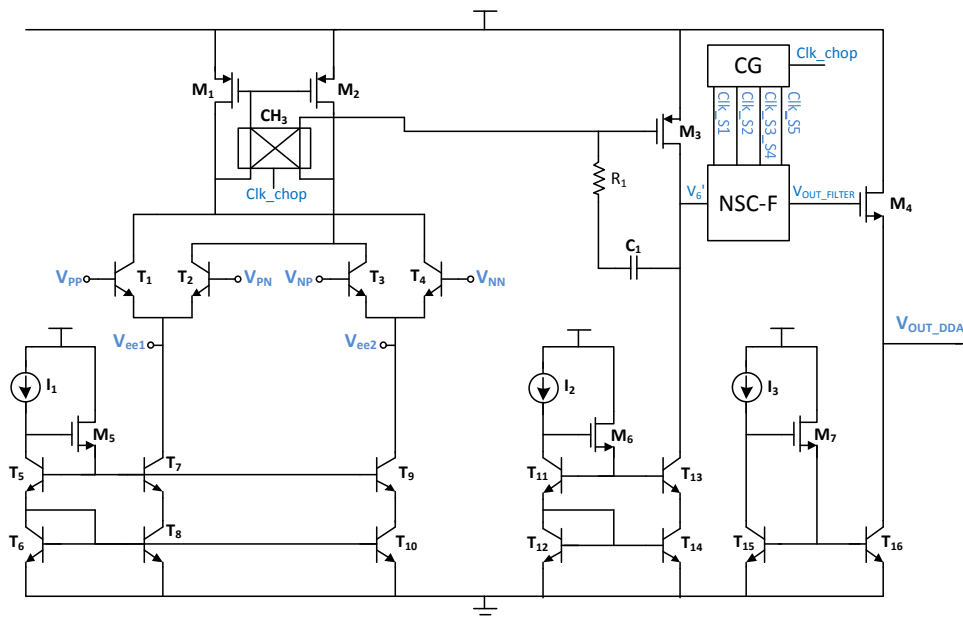


Figure 5.46 Final circuit implementation of the DDA

The final circuitry of the Clock Generator and Notching Switched Capacitor Filter indicated by CG and NSC-F in Figure 5.46 were already discussed in previous sections and shown in Figure 5.44 and Figure 5.35.

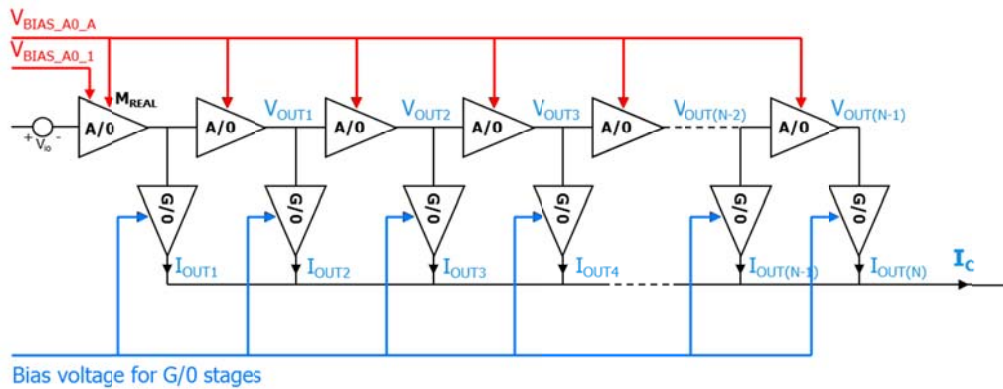
When we look at the top level of the final circuit design of the gain fixation system in Figure 5.45 and compare it with that of Figure 5.23, we can identify the following additional circuitry. At the resistive ladder we have added the MOS switches  $M_8$ - $M_{11}$ . At the output of the DDA we have added the two MOS switches  $M_{12}$  and  $M_{13}$  and the two capacitors  $C_{BIAS\_A0\_1}$  and  $C_{BIAS\_A0\_A}$ . Furthermore we have added the op-amp OA3 which is used to drive the MOS current source  $M_7$ . The positive input port of OA3 is connected to the emitters of the input transistors  $T_1$  and  $T_2$ , as indicated by  $V_{ee2}$  in the DDA circuitry shown in Figure 5.46, while the negative input port of the op-amp is connected to the emitter of the input transistors  $T_3$  and  $T_4$ , denoted by  $V_{ee1}$  in same figure.

In following sub sections we will explain the intended operation of the additional circuitry and we will discuss the final circuit implementation of the cell  $M_{COPY}$  (also used as A/0 cell) and the final circuit implementation of the multiplication cell  $M_{REAL}$ .

### 5.2.6.1 Input offset insensitive multiplication action method without switches in the RF path.

The six newly added switches  $M_8$ - $M_{13}$  together with the two capacitors, as mentioned in the introduction of the final circuit implementation, are placed to perform an operation that results in two different (bias) voltages on top of capacitors  $C_{BIAS\_A0\_A}$  and  $C_{BIAS\_A0\_1}$ . As will be shown, one of these bias voltages will be used to set the gain of an A/0 cell to  $A$ , while the other bias voltage will be used to set the gain of an A/0 cell to a gain of unity. We propose this configuration to obtain an input offset insensitive multiplication operation of the multiplication cell  $M_{REAL}$  and to obtain an multiplication switching action without switches in the RF signal path of the logarithmic detector.

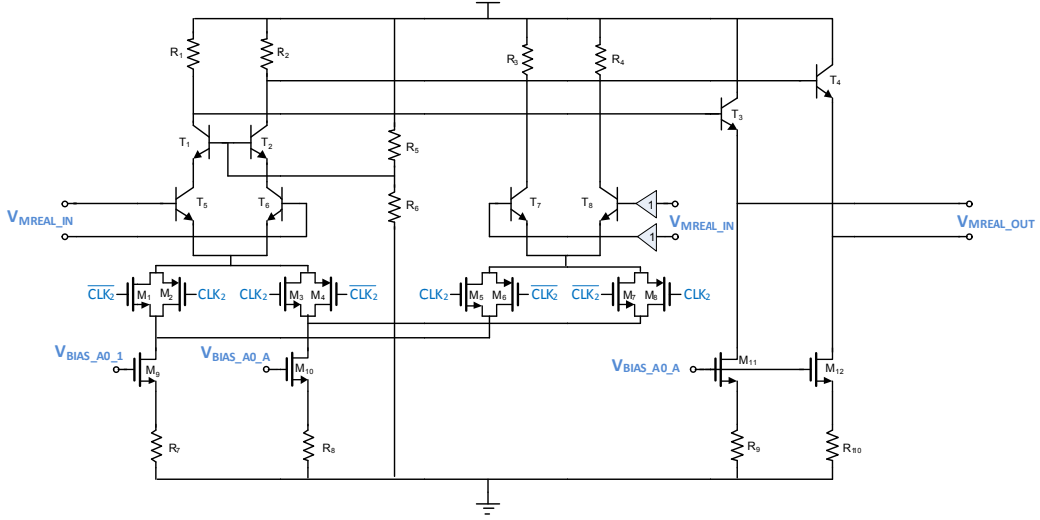
The top level of proposed biasing method is shown in Figure 5.47



**Figure 5.47** The proposed biasing scheme of the successive approximation logarithmic power detector

As shown in this figure all cascaded A/0 cells share the bias voltage,  $V_{BIAS\_A0\_A}$ , to obtain the gain  $A$ . As they share the same bias voltage the stages have to be matched. The first A/0 cell, known as the multiplication cell  $M_{REAL}$ , has an extra bias voltage which will be used to obtain a gain of unity. The two bias voltage of the multiplication cell  $M_{REAL}$  are used to internally drive two

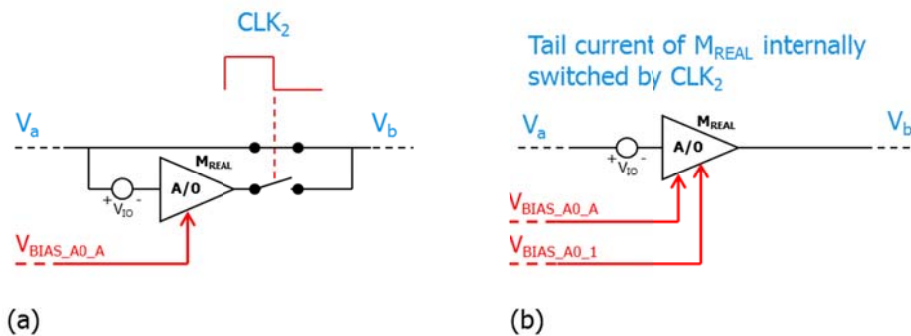
separated MOS current sources as shown in the final circuit implementation of  $M_{REAL}$ . By alternately switching one of these tail current sources off the multiplication cell  $M_{REAL}$  can be switched between a multiplication and a buffering operation. The final circuit implementation of the multiplication cell  $M_{REAL}$  is shown in Figure 5.48.



**Figure 5.48** Final circuit implementation of the multiplication cell  $M_{REAL}$

The current of the tail current sources  $M_9$ - $R_7$  and  $M_{10}$ - $R_8$  in Figure 5.48 are alternately used to bias the input pair  $T_5$ - $T_6$  of the multiplication cell, by alternately switching the complimentary switches  $M_1$ - $M_2$  and  $M_3$ - $M_4$  on and off. The extra switches  $M_5$ - $M_6$  and  $M_7$ - $M_8$  are added to switch the current of the current source, which is not used for biasing, to a dummy input pair  $T_7$ - $T_8$ . As the unused biasing current is diverted to a dummy input pair with same input conditions as the other input pair the unused current source will stay in the ideal case at the same operating point. As the operation point of the relatively big current source transistors (to increase matching with the other A/O cell current sources) are kept constant the switching mechanism between the two biasing situations of the multiplication cell  $M_{REAL}$  can be fast and results in smaller gain error during the switching operation. Another benefit of this architecture is that the channel charge density of the current sources is kept constant. Because of the constant channel charge density of the current sources the sampled voltages on top of the sampling capacitors  $C_{BIAS\_A0\_A}$  and  $C_{BIAS\_A0\_1}$ , which are connected to the gate of the current sources, will not be effected. Which means that the size of these capacitors can be kept relatively small.

That the operation of two biasing voltages will result in an input offset insensitive multiplication action can be explained by Figure 5.50.



**Figure 5.49** The (a) input offset sensitive biasing approach and (b) the input offset un-sensitive biasing approach



Figure 5.49(a) shows the system level approach as was used in Section 3.4, but now including an input referred offset  $V_{IO}$  of the multiplication cell  $M_{REAL}$ . Figure 5.49(b) shows the architecture with two bias voltages as discussed in this section.

With the approach as shown in Figure 5.49(a) we can expect the two output conditions

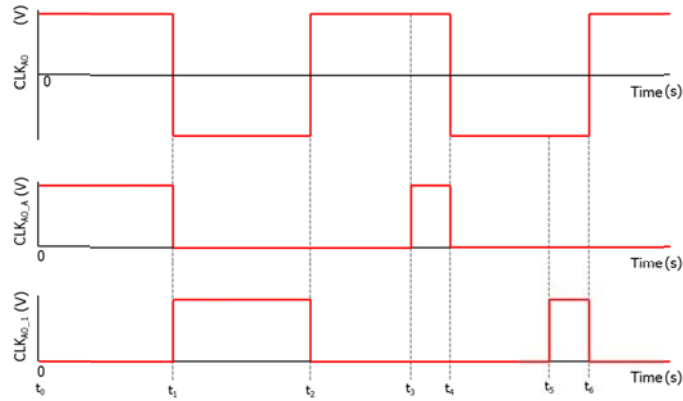
$$V_b = V_a \quad \text{and} \quad V_b = (V_a + V_{IO}) \cdot A \quad (5.59)$$

while in the situation of Figure 5.49(b) it will result in the two outputs

$$V_b = (V_a + V_{IO}) \cdot 1 \quad \text{and} \quad V_b = (V_a + V_{IO}) \cdot A \quad (5.60)$$

Equation (5.59) and (5.60) show that the difference in the output conditions of the architecture in Figure 5.49(b) obtained the wanted multiplication  $A$  while the difference of the output conditions of configuration in Figure 5.49(a) shows a multiplication which is highly dependent on the input offset  $V_{IO}$

How the circuit in Figure 5.45 obtains the two different bias voltages can be explained by the timing diagram of the switches  $M_8$ - $M_{13}$  depicted in Figure 5.50.

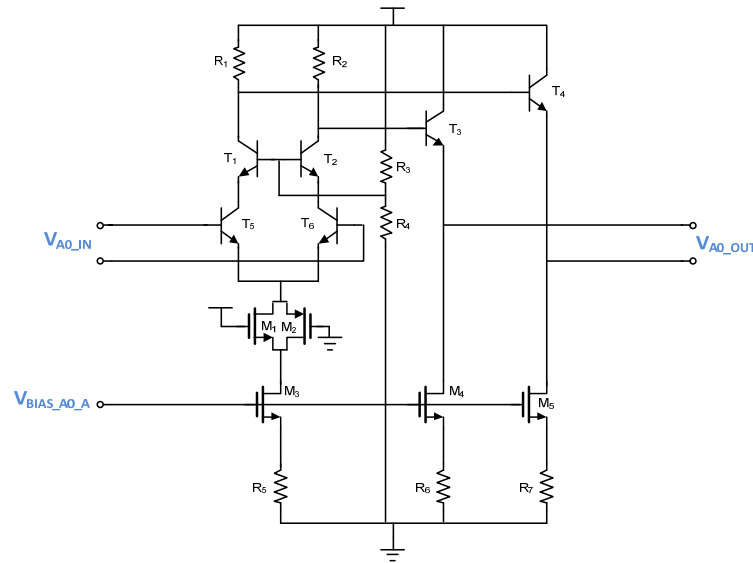


**Figure 5.50** Timing diagram of the switches  $M_8$ - $M_{13}$

Using Figure 5.50 it can be shown that that during the period  $t_0$  till  $t_1$  the MOS switches  $M_9$ ,  $M_{11}$  and  $M_{13}$  depicted in Figure 5.45 are turned on while the other three MOS switches are turned off. In this situation the resistive divider is connected in the same configuration as was discussed in previous sections. This means that the bias voltage  $V_{A0\_BIAS}$  of the multiplication cell  $M_{copy}$  will be forced to a voltage that will set the gain of the multiplication cell equal to  $A$ . As the output switch  $M_{13}$  is turned on, the voltage over capacitor  $C_{A0\_BIAS\_A}$  will be equal to that of  $V_{A0\_BIAS}$ . At time  $t_1$  the MOS switches  $M_8$ ,  $M_{10}$  and  $M_{13}$  are turned off. In this situation the bias voltage  $V_{A0\_BIAS}$  will be held by capacitor  $C_{A0\_BIAS\_A}$ . From Figure 5.50 we can see that the turn-off action of  $M_8$ ,  $M_{10}$  and  $M_{13}$  at time  $t_1$  is followed by a turn-on action of the MOS switches  $M_9$ ,  $M_{11}$  and  $M_{12}$ . In this situation the resistive divider will be connected in such a way that the input voltage at the multiplication cell  $M_{copy}$  is equal to that of voltage,  $V_{PP}$ - $V_{PN}$ , at the positive input port of the DDA. As the DDA, in negative feedback, will force both of its input ports to be equal, the gain of  $M_{copy}$  will be set to unity. Now that the MOS switch  $M_{12}$  is turned on, the voltage over capacitor  $C_{A0\_BIAS\_1}$  will be equal to the bias voltage  $V_{A0\_BIAS}$ . When at time  $t_2$  the MOS switches  $M_8$ ,  $M_{10}$  and

$M_{13}$  are turned off, the bias voltage  $V_{A0\_BIAS}$ , will be held on capacitor  $C_{A0\_BIAS\_1}$ . So, now capacitor  $C_{A0\_BIAS\_1}$  is holding the correct bias voltage for the buffering operation of the multiplication cell  $M_{REAL}$ , while capacitor  $C_{A0\_BIAS\_A}$  is holding a correct bias voltage for the multiplication action of  $M_{REAL}$  and the right gain  $A$  of the cascaded A/0 cells.

The foregoing procedure can be repeated to refresh both bias voltages. However, the moment that a capacitor can be connected to the loop should be limited at predefined periods. This is necessary to isolate the response of the loop from the capacitors during the stabilization time of the loop when the resistive divider is switched. As capacitors  $C_{A0\_BIAS\_A}$  and  $C_{A0\_BIAS\_1}$  are already charged in a forgoing charging period we can expect relatively less disturbance of the loop when the voltage over the capacitors  $C_{A0\_BIAS\_1}$  or  $C_{A0\_BIAS\_A}$  are refreshed during the stable periods of the loop.



**Figure 5.51** Final circuit implementation of the A/0 cells

Figure 5.51 shows the final circuit implementation of the A/0 cells and  $M_{COPY}$ . As shown by this figure we also use MOS current sources inside these cells. Furthermore we have used an dummy switch  $M_1$ - $M_2$ . With this A/0 cell configuration we obtain a matched gain stage structure with the multiplication cell  $M_{REAL}$ .

With the use of (matched) MOS current sources for  $M_{COPY}$ ,  $M_{REAL}$  and the other A/0 cells we can conclude another possible feature of the refreshing system. As frequently refreshing of the sampling capacitors  $C_{A0\_BIAS\_1}$  or  $C_{A0\_BIAS\_A}$  is only necessary for time variant parameters as for example temperature and leakage of the bias capacitors it is plausible that the fixation system can be completely turned off till refreshment is expected to be needed. As temperature is a relatively slowly varying parameter and leakage of the capacitors is minimized by the MOS current sources (draw no DC gate current), the frequency of refreshments can be set relatively very low. This shows an opportunity to lower the mean power consumption of the gain/multiplication fixation system tremendously. Furthermore, a low noise contribution to the bias voltage can be obtained when relatively big geometries of the MOS current sources are used.

### 5.2.6.2 Automatic common mode input voltage adjustment circuit

The common mode voltage at the negative input port of the DDA is defined by the internal structure of the multiplication cell  $M_{COPY}$ , while the common mode voltage at the positive input port of the DDA is defined by the divider block. For better performance of the DDA the common mode voltage at both inputs of the DDA should be placed close to each other such that the closely matched tail current sources of both DDA input pairs are affected by the same load conditions. The matched load conditions of both current sources will lead to closely matched tail currents, which is an important design issue as was discussed in Sub Section 5.2.3.5.2. From Figure 5.46 we can see that both tail current sources of the DDA are implemented as cascodes which actually already lowers the effect of different load conditions. However, beside equal input common mode voltages of both input pairs of the DDA the input common mode voltage of the multiplication cell  $M_{COPY}$  is also important. The input common mode voltage of  $M_{COPY}$  should be close to the input common mode voltages of the other cascaded A/O cells, such that the effect of finite output impedance of the current sources on the gain of these cells is the same as it is for  $M_{COPY}$ , leading to a better gain match of the stages.

To obtain closely matched common mode voltages at both differential inputs of the DDA and obtain equal common mode voltages at the multiplication cell  $M_{COPY}$  and the other A/O cells the circuitry of the fixation system is modified as shown in Figure 5.45 and Figure 5.46

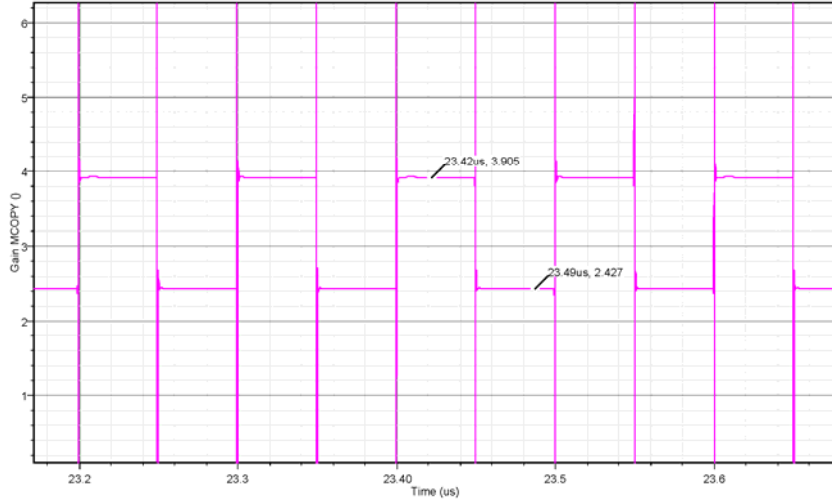
As already noted in the introduction of the final circuit implementation, opamp OA3 is part of a negative-feedback configuration which forces the magnitude of the voltages  $V_{ee1}$  and  $V_{ee2}$  (Figure 5.46) to be close to each other by adjusting the gate voltage at  $M_7$  (Figure 5.45). When we take a closer look at the circuit depicted in Figure 5.45 we can see that the control of the gate of  $M_7$  by opamp OA3 will lead to an adjustment of the current delivered by current source  $M_7$ . As this current is sent through  $M_6$  it will set the  $V_{GS}$  voltage of  $M_6$ . This  $V_{GS}$  together with the  $V_{GS}$  of  $M_5$ , which is defined by reference current  $I_1$ , will define the voltage at the bottom of the resistive divider. So, while the current source  $I_1$  still defines the two differential output voltages of the divider block, the  $V_{GS}$  of  $M_6$  plus that of  $M_7$  will now define the common mode voltage of both differential voltages of the divider. From above explanation we can see that the common mode voltage of the positive input port of the DDA and that of  $M_{COPY}$  is controlled by opamp OA3. The output common mode voltage of  $M_{COPY}$  and thus the input common mode voltage at the negative input of the DDA is still defined by the internal structure of  $M_{COPY}$ . Because of the negative feedback configuration of opamp OA3 the voltage  $V_{ee1}$  and  $V_{ee2}$  will be forced to be close to each other, which will result in the matched input common mode voltages of  $M_{COPY}$ , the other A/O cells and both input pairs of the DDA.



## 6 Simulation results

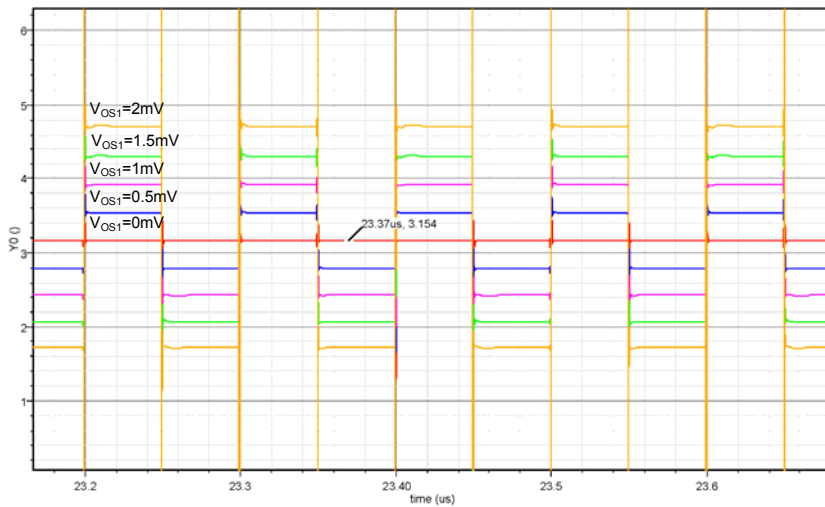
In this chapter we will discuss the simulation results of the final circuit implementation which was discussed in Chapter 5. For the simulation setup we used a chopper clock frequency of 10MHz. Furthermore we configured the resistive divider of the divider block to generate a differential voltages of 4.3mV and 13.60mV such that an attenuation factor  $B$  equal to 3.162 is obtained. With the following simulation results we will show how close the gain of  $M_{COPY}$ , the gain of the A/O cells and the multiplication factor of  $M_{REAL}$  are set to their expected value of 3.162 over input offset, temperature and power supply variations.

Figure 6.1 shows the gain of  $M_{COPY}$  over time for an input offset  $V_{OSI}$  of 1mV during the 3.162 attenuation mode of the divider block. Note that the input voltage of  $M_{COPY}$  is 4.3mV



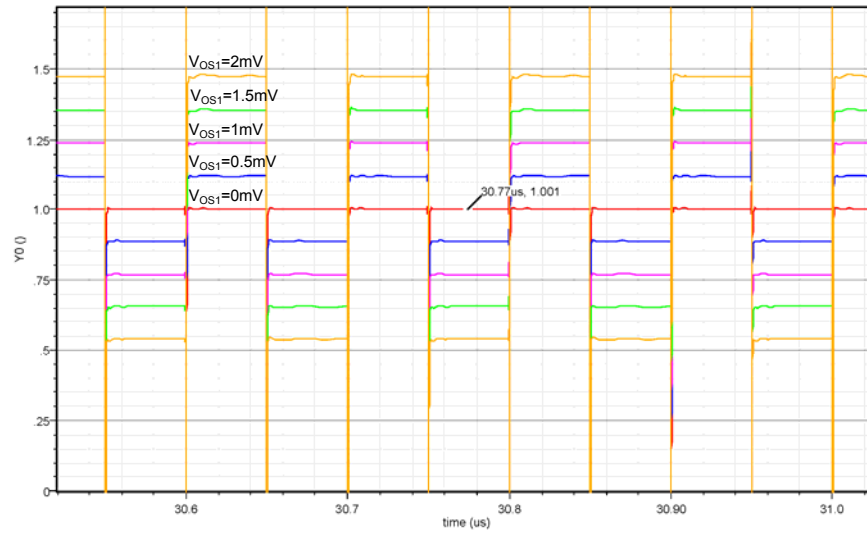
**Figure 6.1** Gain of  $M_{COPY}$  over time for an input offset voltage  $V_{OSI}$  of 1mV at  $M_{COPY}$

As shown by this figure the gain doesn't look constant at all. However from the chopper technique discussed in Section 5.2.4.1 we know that this is a result of the frequency translated DC offset caused by the modulation of the chopper at the input of  $M_{COPY}$ . For the real gain of  $M_{COPY}$  we have to look at the mean value of the gain in Figure 6.1.



**Figure 6.2** The gain of  $M_{COPY}$  for different input offsets at the input of  $M_{COPY}$  over time during the 3.16 gain mode

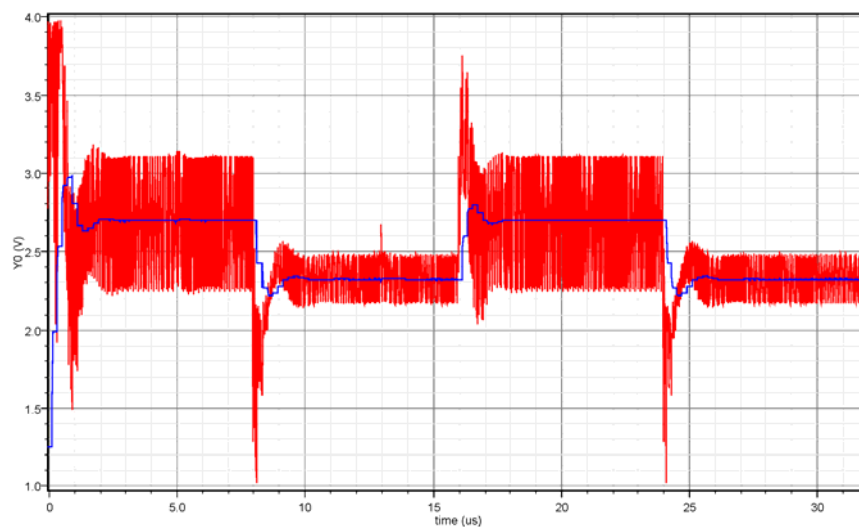
Figure 6.2 shows the gain of  $M_{COPY}$  for different input offsets when the divider block is configured in the 3.162 attenuation mode. As shown by this figure the mean gain value approaches the expected 3.162 gain with 0.25% error.



**Figure 6.3** The gain of  $M_{COPY}$  for different input offsets at the input of  $M_{COPY}$  over time during the unity gain mode

Figure 6.3 shows the gain of  $M_{COPY}$  for different input offsets when the divider block is configured in the unity gain mode. Here we can clearly see that the mean gain of  $M_{COPY}$  approaches unity gain with a 0.1% error. Side note: The big spikes in above figures are a result of the mathematical operation obtained to calculate the gain of  $M_{COPY}$ . As the output is a little delayed in comparison with the input signal as a result of the finite bandwidth of  $M_{COPY}$ , the output/input division resulted in the spikes.

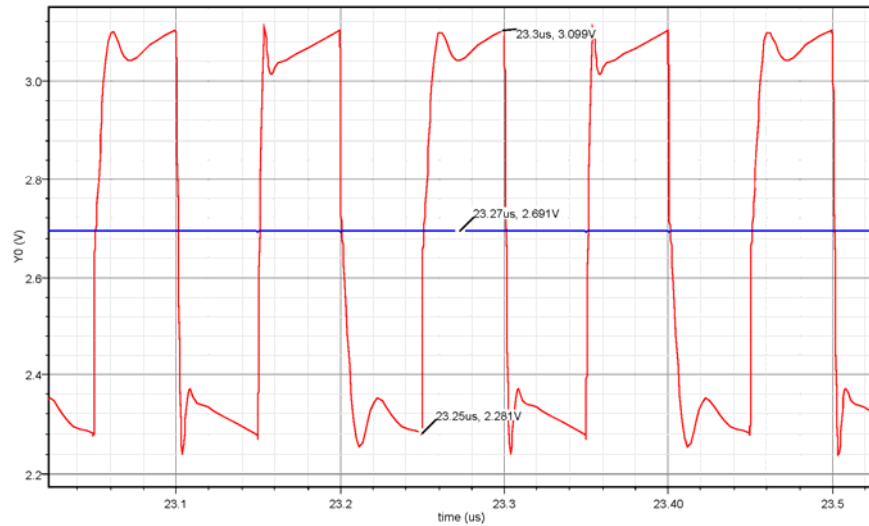
Before we analyse the gain and multiplication operation of  $M_{REAL}$  we will first look at simulation that verify the operation of the new Notching Switched Capacitor Filter.



**Figure 6.4** Input signal (red curve) and output signal (blue curve) of the new Notching switched Capacitor Filter for an input offset of 1.5 mV at the input of  $M_{COPY}$

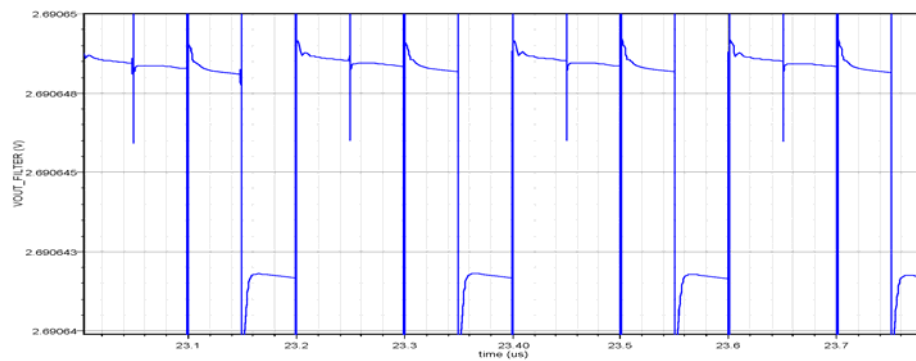
Figure 6.4 shows the input signal (red curve) and output signal (blue curve) of the filter for an input offset  $V_{OSI}$  of 1.5mV at the input of  $M_{COPY}$ .

In Figure 6.4 we can clearly see the two different biasing modes over time. The difference in the ripple between both modes is a result of the input offset that is amplified by  $M_{COPY}$ . The lower ripple amplitude is a result of the unity gain amplification of the offset at  $M_{COPY}$  during the unity gain biasing mode, and the higher magnitude ripple results from the 3.162 amplification of the offset during the 3.162 gain biasing mode.

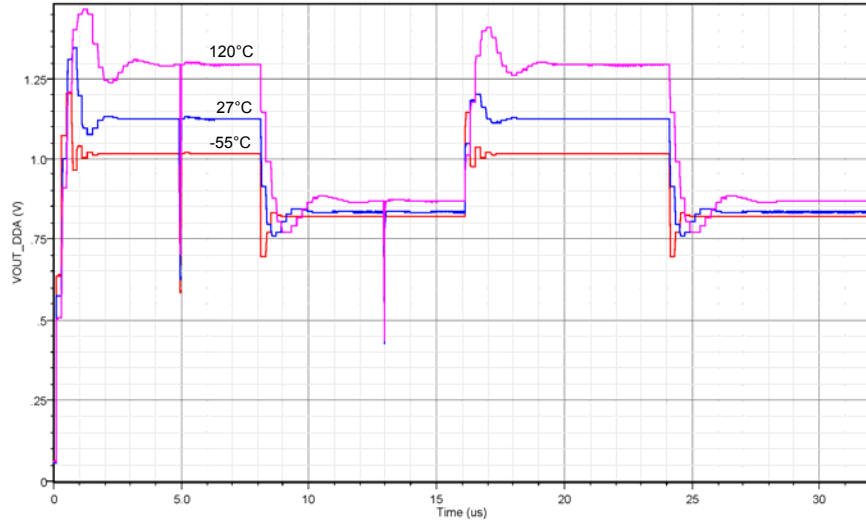


**Figure 6.5** A close up view of the input voltage (red) and output voltage (blue) of the Notching Switched Capacitor Filter for an input voltage of 1.5 mV at the input of  $M_{COPY}$

Figure 6.5 shows a close up of the input signal (red curve) and output signal (blue curve) of the filter during the 3.162 amplification mode. The input signal shows the expected shape as was discussed in Section 5.2.5.1. As shown by the input signal the modulators used for chopping are introducing spikes during the switching operation. The effect of the slowdown in voltage transitions is a result of the changing time constant during the tracking modes of the track-and-hold capacitors of the filter. When we look at the output voltage of the filter in Figure 6.5 it looks like that the output signal contains no ripple. Close inspection of the output signal of the filter showed an residual peak to peak ripple of around 6uV as shown in Figure 6.6. The low residual ripple is a cause of the small charge injection that is left after the imperfect charge cancelation by the dummy switches, which we discussed in Subsection 5.2.5.2.6.1.

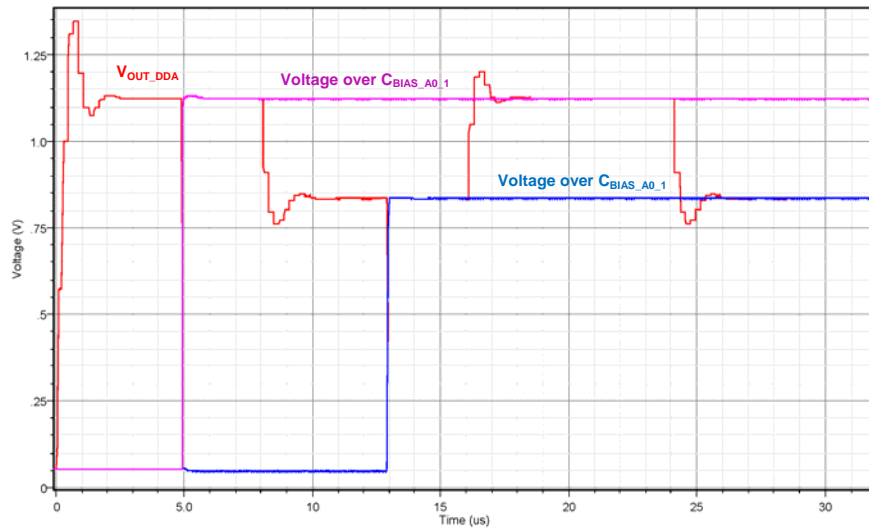


**Figure 6.6** The close up view of the output signal of the Notching Switched Capacitor Filter shows a very low residual ripple



**Figure 6.7** Transient of the DDA output voltage for different temperatures.

Next to be investigated is the loop response over temperature. Figure 6.7 shows the transient of the output signal of the DDA for the temperatures  $-55^{\circ}\text{C}$ ,  $27^{\circ}\text{C}$  and  $120^{\circ}\text{C}$ . As we know from a previous chapter the output signal of the DDA is the actual biasing signal of the multiplication cell  $M_{\text{COPY}}$ . From the output responses of the DDA as shown in Figure 6.7 we can see that the chopper stabilized fixation system reaches its stable output in less than 5us over the full temperature range of  $-55^{\circ}\text{C}$  to  $120^{\circ}\text{C}$ . The maximum time needed to stabilise at the temperature extreme of  $120^{\circ}\text{C}$  was used to set the turn-on timing of the biasing capacitors switches. When we look in Figure 6.7 at 5us and 13us we can clearly see the response of the loop as result of the switching mechanism of the capacitors switches.



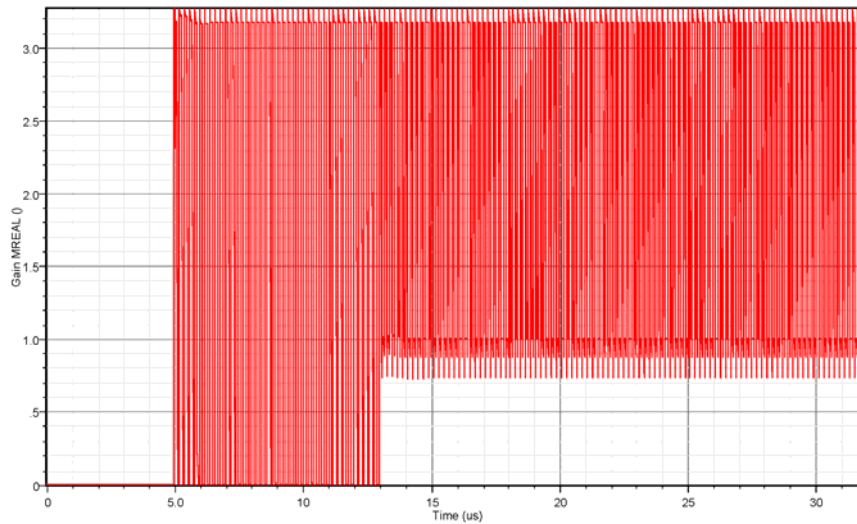
**Figure 6.8** Loop response at output DDA (red curve) and the voltage over the sampling capacitors  $C_{\text{BIAS\_A0\_1}}$  (blue curve) and  $C_{\text{BIAS\_A0\_A}}$  (pink curve)

Figure 6.8 shows the loop response including the sampling action of the sampling capacitors at a temperature of  $27^{\circ}\text{C}$ . The pink transient is the voltage over  $C_{\text{BIAS\_A0\_A}}$  while the blue transient is the voltage over biasing capacitor  $C_{\text{BIAS\_A0\_1}}$ . In Figure 6.8 we can clearly see that the correct timing of the sampling switches result in sampling voltage over both capacitors that are sampled during the stable region of the loop responses. From Figure 6.8 we can also see that the



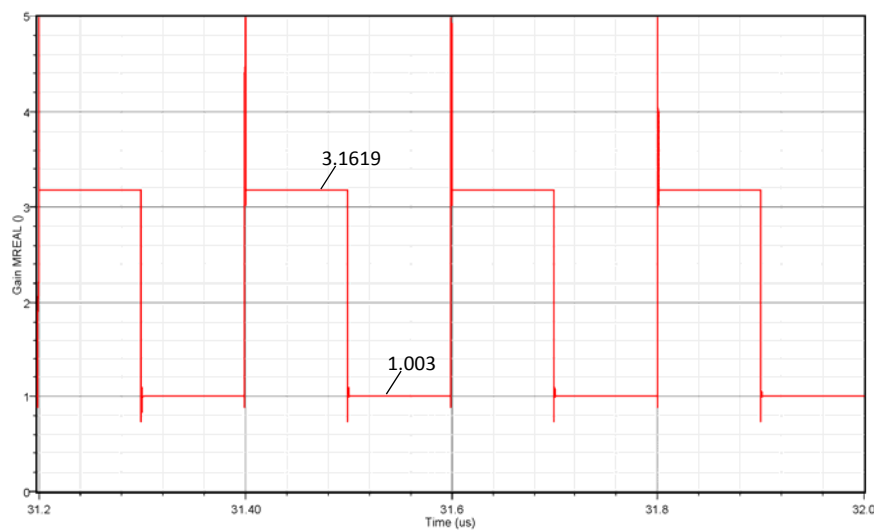
refreshment of capacitor  $C_{BIAS\_A0\_A}$  at 21 $\mu$ s does not disturb the loop response as it already charged during the previous charging cycle.

As we know from Section 5.2.6.1, both sampled bias voltages are used to bias the multiplication cell  $M_{COPY}$  alternately to an gain of 3.162 and unity gain. Furthermore we know that the sampled bias voltage over capacitor  $C_{BIAS\_A0\_A}$  will also be used for the bias of the other cascaded A/0 cells. To see that the alternating bias condition result in the wanted multiplication operation of  $M_{REAL}$ , we have to look at the simulation results of the differential gain of  $M_{REAL}$  as shown in Figure 6.9. Note that for this simulation we used an input voltage at  $M_{REAL}$  of 10 $\mu$ V.



**Figure 6.9** The alternating differential output voltage of  $M_{REAL}$  during an 1.5 mV offset at  $M_{COPY}$

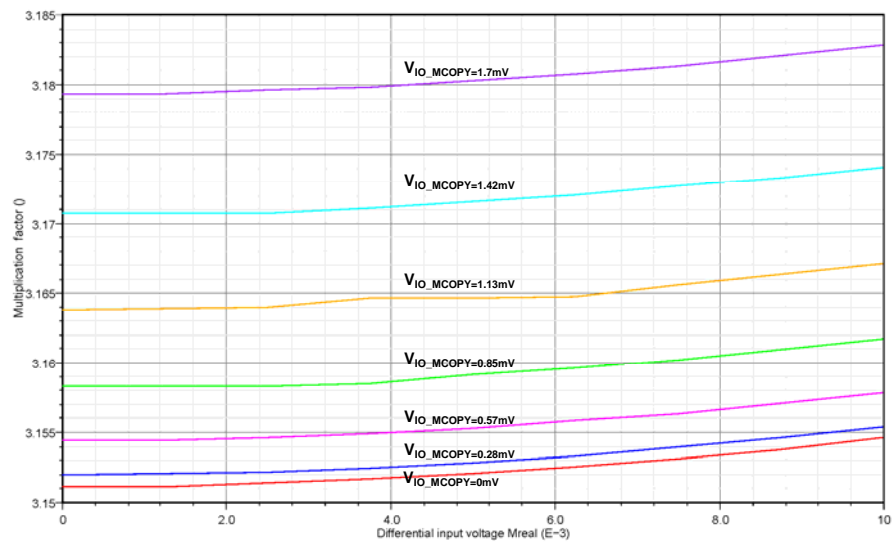
As expected from Figure 6.8, the gain of  $M_{REAL}$  start to switch alternately between the two gain modes at the moment that both sampling capacitors have sampled the correct bias voltages from the loop response. That both gain modes closely match the expected 3.162 gain and unity gain is shown in Figure 6.10



**Figure 6.10** Close up view of the alternating gain of  $M_{REAL}$

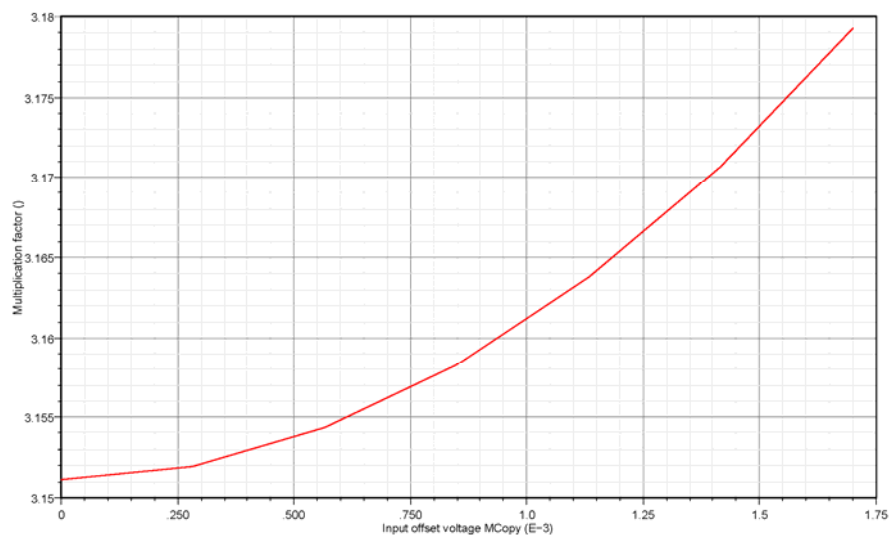
Now that we have shown the correct operation of the gain/multiplication fixation procedure. We now will investigate the sensitivity of the multiplication factor obtained by  $M_{REAL}$ , and the gain obtained by the A/0 cells to the 3 input offsets in the gain/multiplication fixation system. Furthermore we will look at the sensitivity to temperature and power supply variation. The results of these simulations will now be discussed.

Figure 6.11 shows the sensitivity of the multiplication factor for different input offsets at  $M_{COPY}$  over the differential input voltage of  $M_{REAL}$



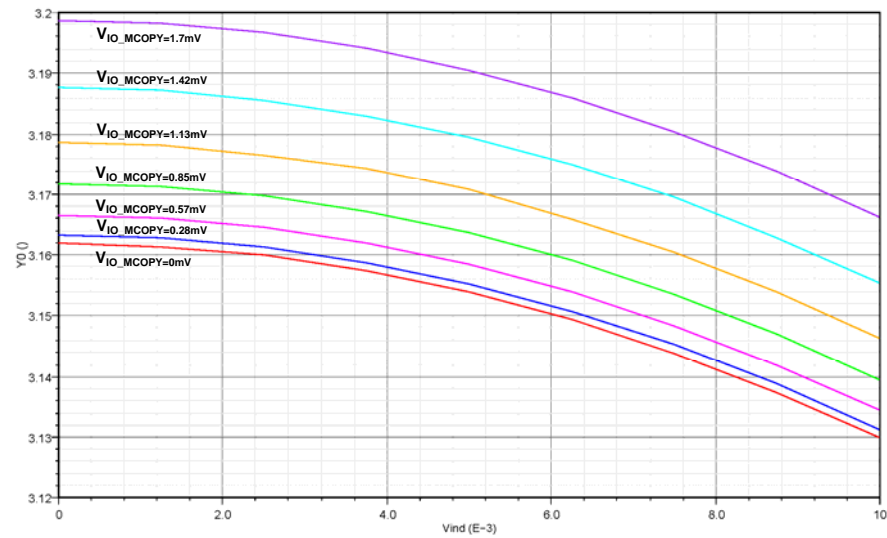
**Figure 6.11** The multiplication factor of  $M_{REAL}$  over its differential input voltage for different input offsets at the cell  $M_{COPY}$

Figure 6.12 shows the sensitivity of the multiplication factor for different input offsets at  $M_{COPY}$  for an differential input voltage of 10uV at  $M_{REAL}$



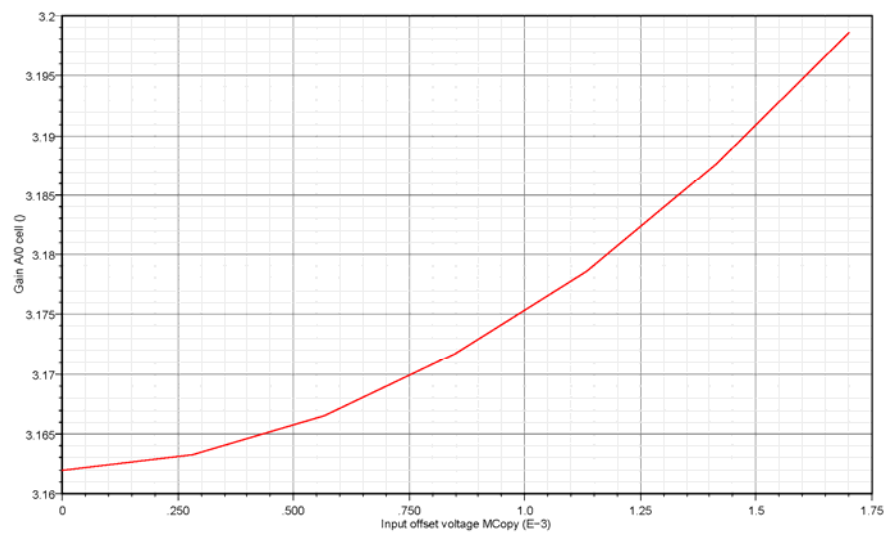
**Figure 6.12** The multiplication factor of  $M_{REAL}$  for an input voltage of 10uV over the input offset at the cell  $M_{COPY}$

Figure 6.13 shows the sensitivity of the gain for different input offsets at  $M_{COPY}$  over the differential input voltage of an A/O cell



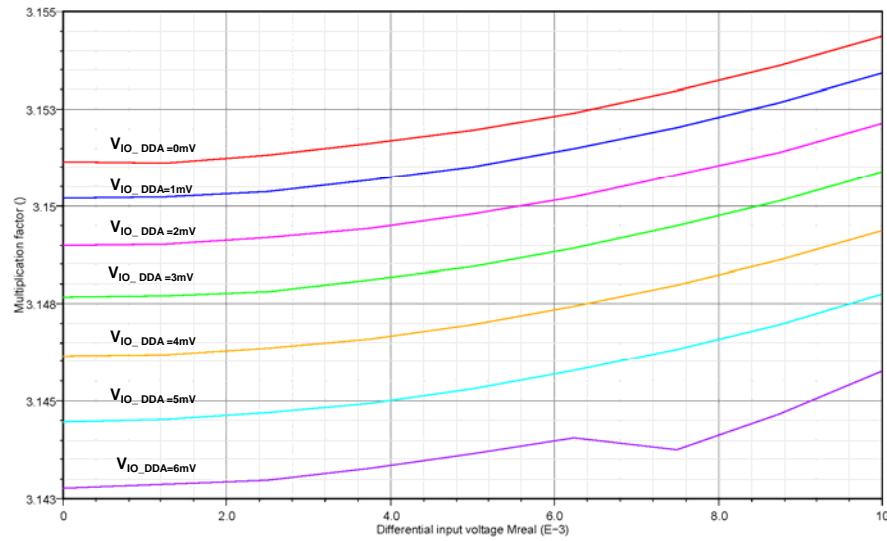
**Figure 6.13** The gain of an A/O cell over its differential input voltage for different input offsets at the cell  $M_{COPY}$

Figure 6.14 shows the sensitivity of the gain over input offset at  $M_{COPY}$  for an differential input voltage of 10uV at an A/O cell



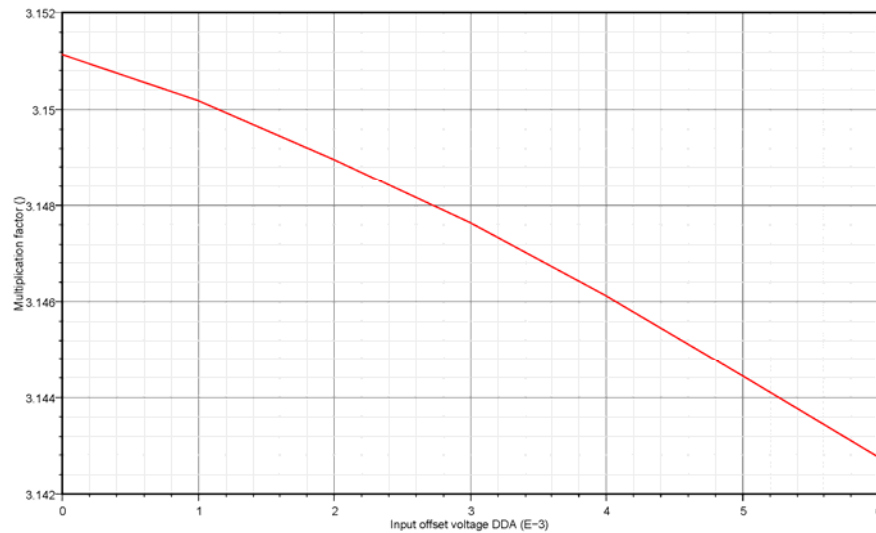
**Figure 6.14** The gain of an A/O cell for an input voltage of 10uV over the input offset at the multiplication cell  $M_{COPY}$

Figure 6.15 shows the sensitivity of the multiplication factor obtained by  $M_{REAL}$  for different input offsets at the negative input of the DDA.



**Figure 6.15** The multiplication factor of  $M_{REAL}$  over its differential input voltage for different input offsets at the negative input port of the DDA

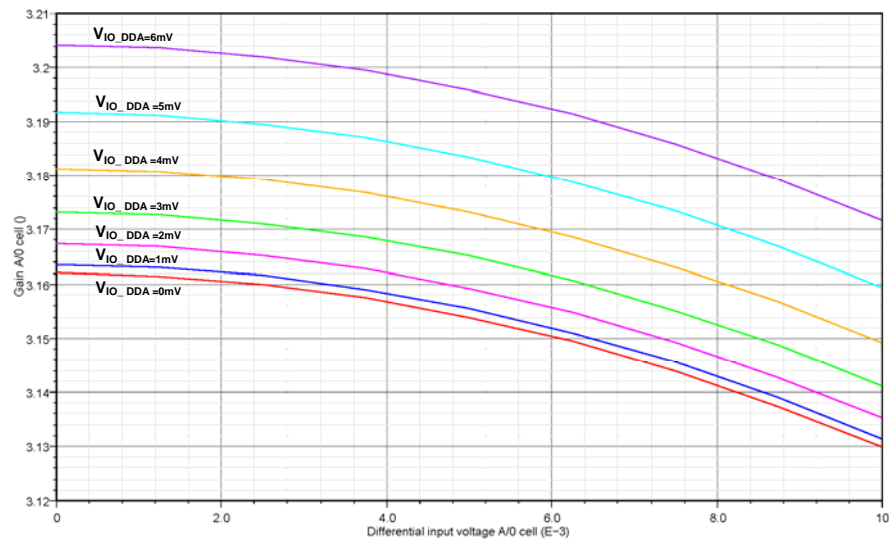
Figure 6.16 shows the sensitivity of the multiplication factor over input offset at the negative input port of the DDA for an differential input voltage of 10uV at  $M_{REAL}$



**Figure 6.16** The multiplication factor of  $M_{REAL}$  for an input voltage of 10uV over the input offset at the negative input port of the DDA

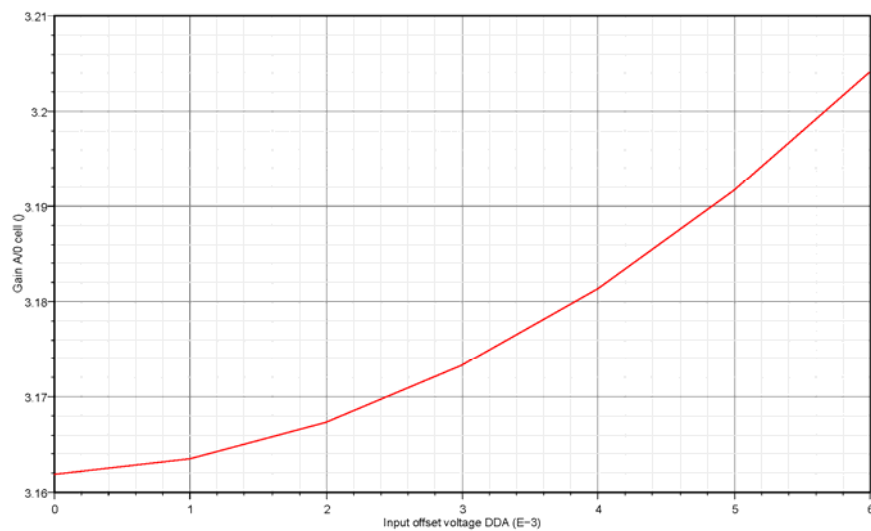
Figure 6.16 shows that the multiplication factor  $A$  is highly in-sensitive for input offsets at the DDA.

Figure 6.17 shows the sensitivity of the A/O cell gain for different input offsets at the negative input port of the DDA over the differential input voltage of an A/O cell



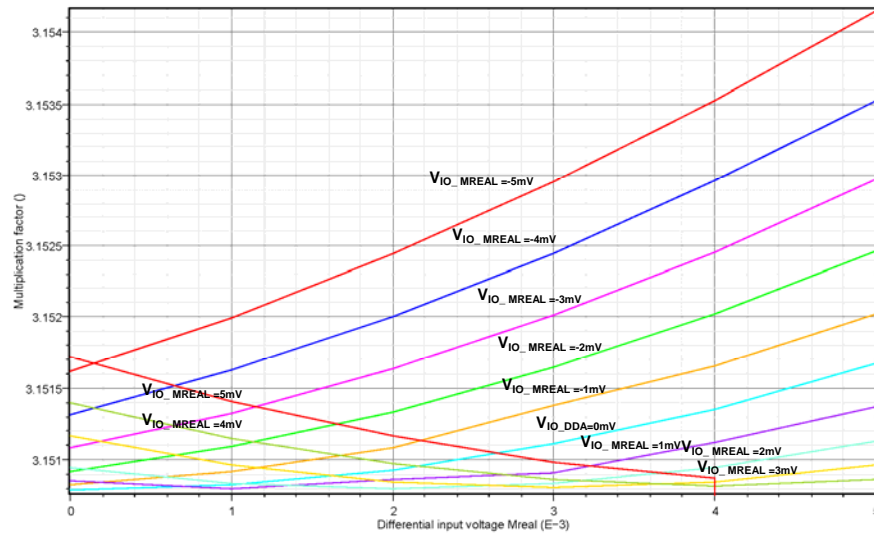
**Figure 6.17** The gain of an A/O cell over its differential input voltage for different input offsets at the negative input port of the DDA

Figure 6.18 shows the sensitivity of the gain over input offset at the negative input port of the DDA for an differential input voltage of 10uV at an A/O cell



**Figure 6.18** The gain of an A/O cell for an input voltage of 10uV over the input offset at the negative input port of the DDA

Figure 6.19 shows the sensitivity of the multiplication factor obtained by  $M_{REAL}$  for different input offsets at  $M_{REAL}$ .

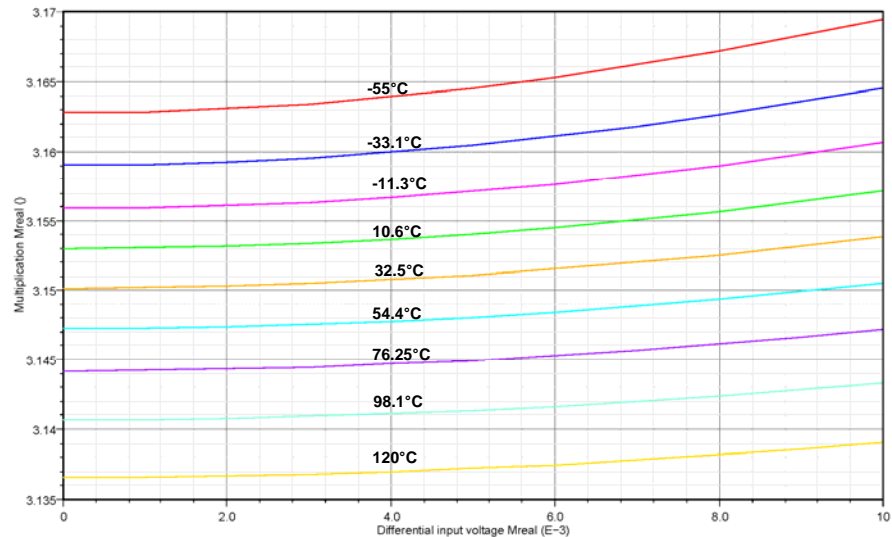


**Figure 6.19** The multiplication factor of  $M_{REAL}$  over its differential input voltage for different input offsets at  $M_{REAL}$

As shown by Figure 6.19 the multiplication factor obtained by  $M_{COPY}$  is very in-sensitive for its input offset.

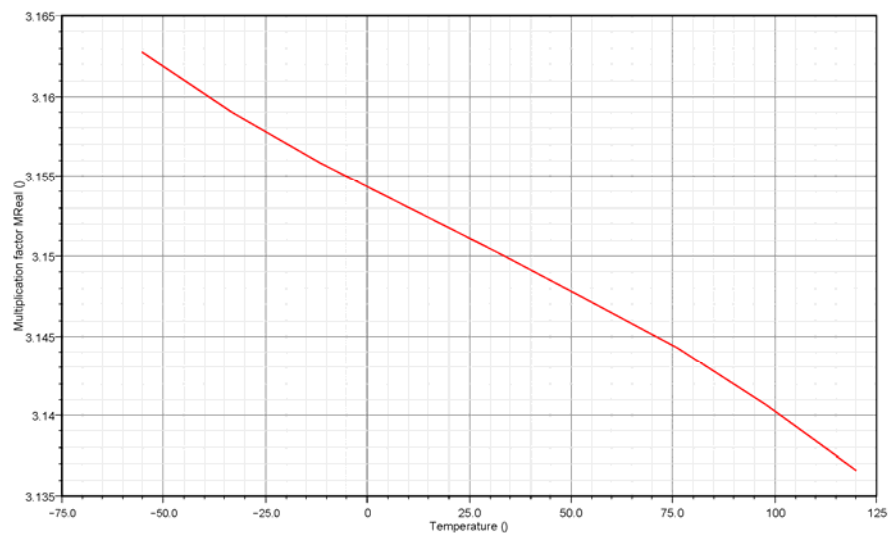
From the change in the responses of the control loop showed in Figure 6.7 we already observed the change in the two biasing voltages over temperature. That these bias voltages resulted in the wanted multiplication of  $M_{COPY}$  and gain of the A/0 cells can be seen by the following figures.

Figure 6.20 shows the resulting multiplication factor obtained by  $M_{REAL}$  for different temperatures.



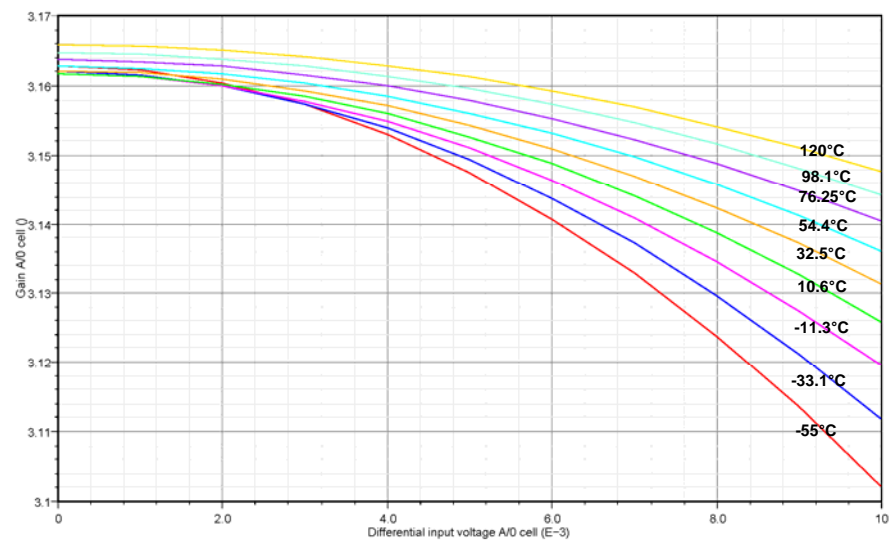
**Figure 6.20** The multiplication factor of  $M_{REAL}$  over its differential input voltage for different temperatures

Figure 6.21 shows the resulting multiplication factor obtained by  $M_{REAL}$  over the temperature range from  $-55^{\circ}\text{C}$  to  $120^{\circ}\text{C}$ .



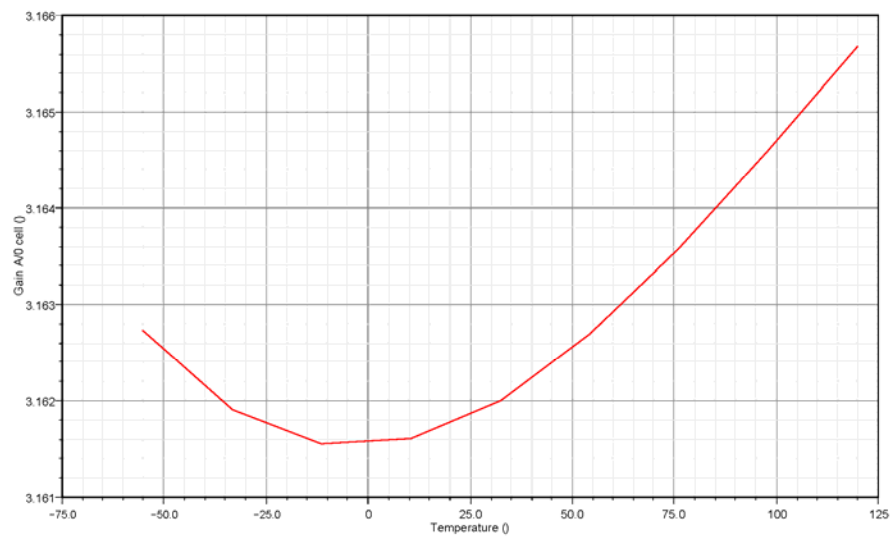
**Figure 6.21** Multiplication factor of  $M_{REAL}$  for an input voltage of 10uV over the temperature range from  $-55^{\circ}\text{C}$  to  $120^{\circ}\text{C}$

Figure 6.22 shows the sensitivity of the A/0 cell gain for different temperatures.



**Figure 6.22** The gain of an A/0 cell over its differential input voltage for different temperatures

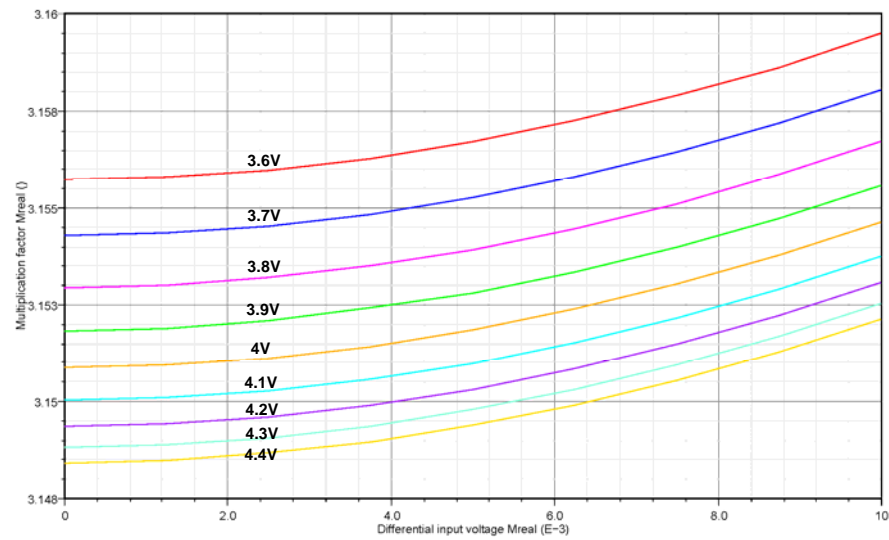
Figure 6.23 shows the sensitivity of the A/0 cell gain over the temperature range -55°C to 120°C.



**Figure 6.23** The gain of an A/0 cell for an input voltage of 10uV over the temperature range from -55°C to 120°C

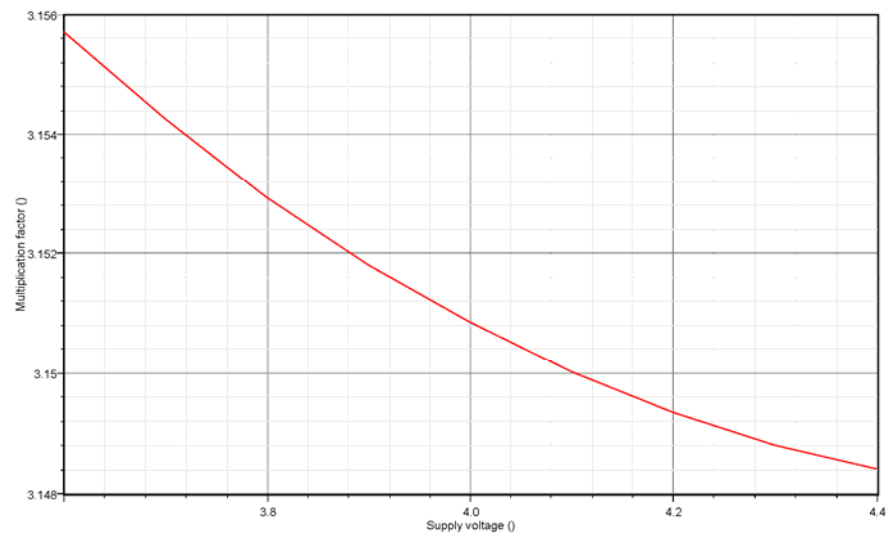


Figure 6.24 shows the resulting multiplication factor obtained by  $M_{REAL}$  for different power supply voltages.



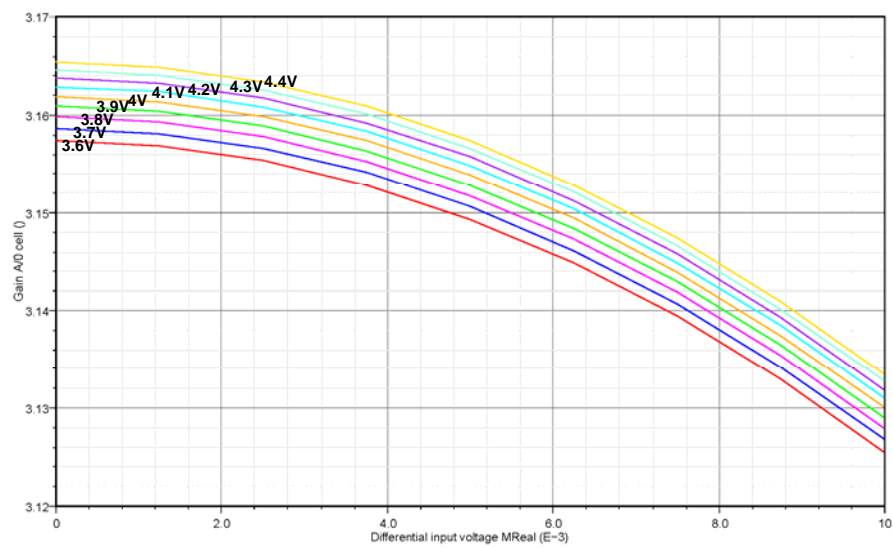
**Figure 6.24** The multiplication factor of  $M_{REAL}$  over its differential input power for different supply voltages

Figure 6.25 shows the resulting multiplication factor obtained by  $M_{REAL}$  over the power supply voltage range 3.6V to 4.4V.



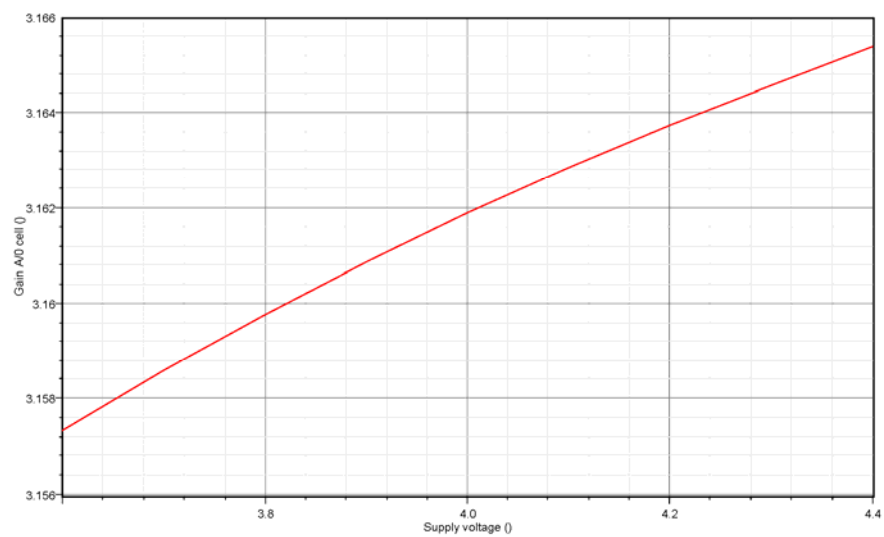
**Figure 6.25** Multiplication factor of  $M_{REAL}$  for an input voltage of 10uV over the power supply range from 3.6V to 4.4V

Figure 6.26 shows the sensitivity of the A/0 cell gain over different power supply voltages.



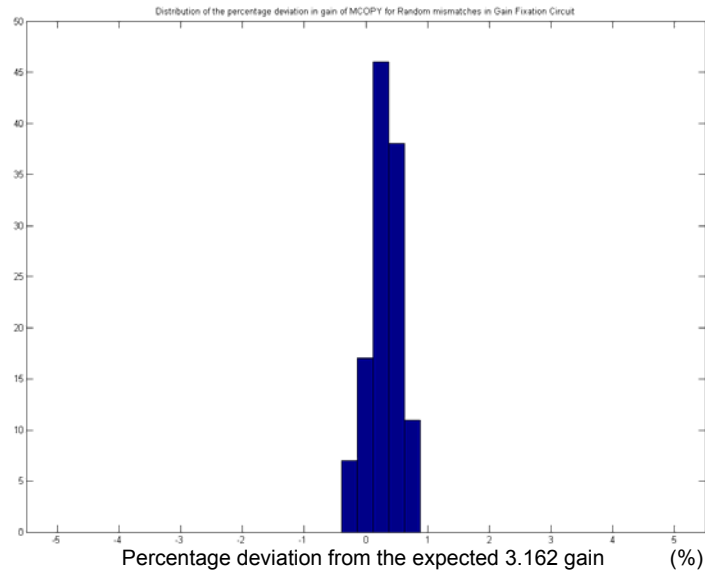
**Figure 6.26** The gain of an A/0 cell over its differential input voltage for different power supply voltages

Figure 6.27 shows the sensitivity of the A/0 cell gain for an input voltage of 10uV over the power supply voltage 3.6V to 4.4V.



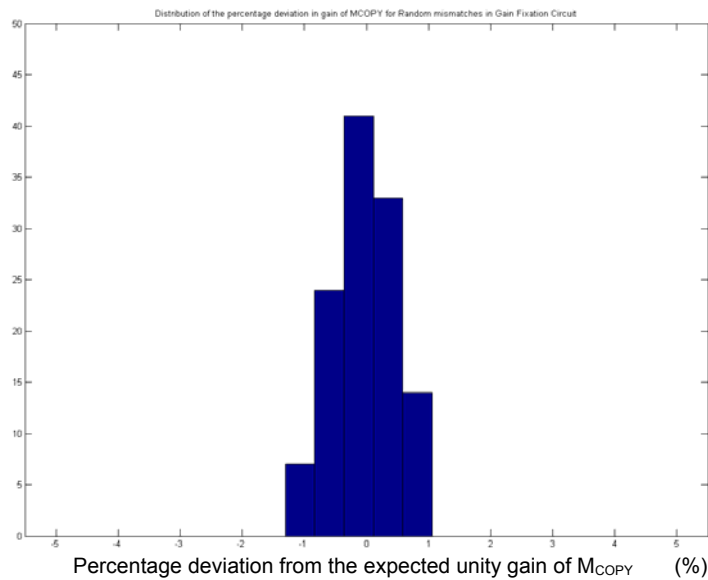
**Figure 6.27** The gain of an A/0 cell for an input voltage of 10uV over the power supply range from 3.6V to 4.4V

Figure 6.28 shows the bar graph gathered from a 119 runs Monte Carlo simulation of the gain of  $M_{COPY}$  during the 3.162 gain mode.



**Figure 6.28** Bar graph of the percentage deviation from the expected gain (3.162) of  $M_{COPY}$

As we already observed from Figure 6.6 the gain fixation system obtained a fixation around 3.154x for  $M_{COPY}$  instead of the expected 3.162x. This static error resulted in a shift from the zero percentage in Figure 6.27. [74] The static error can be solved by altering the attenuation factor  $B$  of the divider block.



**Figure 6.29** Bar graph of the percentage deviation from the expected unity gain of  $M_{COPY}$

Both plots show accurate operation of the gain fixation system over the 119 montecarlo runs. The overall error is much lower than the maximum allowed deviation in the multiplication factor  $A$  which is -4.5% and 5.5% as was discussed in Section 4.3.1



## 7 Conclusions

In Subsections 1.5, 1.6, and 2.4.2 the importance of an accurate log transfer of the RF power detector was explained. We have shown that the precise measurement ability of the RF power detector is very important because for example it determines the accuracy of the output power of the system that it controls. For the precise predictability of the output power of such a system it was shown that the log transfer of the RF power detector has to be fixed and accurately known.

In Chapter 3 we have proposed a new method that possibly can be used to continuously calibrate the transfer of a RF power detector to a predefined and fixed position over mismatch, part to part spread, temperature and input frequency. It was shown (Figure 3.22) that this calibration method is based on a smart switching algorithm around a log device. With the inclusion of the switching algorithm it was shown that we can obtain two simultaneous output voltages (denoted in Figure 3.22 by  $\overline{V_{OUT}}$  and  $V_{OUT\_S}$ ) from one single log device, both containing different information content. It was shown that the voltage  $\overline{V_{OUT}}$  resulted in a slope, dynamic range and intercept fixated log read-out while the voltage  $V_{OUT\_S}$  at the same time gives a measure about the slope of the device log transfer. It was stated that the slope information voltage  $V_{OUT\_S}$ , which is obtained by an accurate multiplication switching operation (Section 3.2) at the switched input of the log device, can be used to automatically control the slope of the log device transfer to correct values. This multiplication used for the multiplication switching operation was called the multiplication factor A.

The system level simulations in Section 4.2 have proved that the slope, intercept and dynamic range of the log device transfer can be fixed by the new calibration method. However in Section 4.2 it was also shown that the slope fixation procedure, without further modification, introduced a negative side effect. Namely, it decreased the dynamic range at the higher input range. Fortunately a new dynamic range extension method (Section 3.2.2) was found that can be used to extend the dynamic range to higher input levels.

The new dynamic range extension method showed us the capability to extend the dynamic range without the use of two highly matched log devices which is normally used to obtain a higher dynamic range. As was shown in Figure 3.16 the dynamic range extension can be obtained by placing a so-called Automatic Attenuation Control (AAC) circuit after the switched input of the logarithmic device. The system simulation (Figure 4.5) in Section 4.2 proved the operation of the new extension method. It was shown that the AAC can be automatically switched to attenuation operation when the input of the logarithmic device reaches a critical level. With the graphical representation of the dynamic range extension procedure depicted in Figure 3.17 we have shown that the switching procedure will result in a negligible disturbance of the log read-out. Furthermore we have shown that the exact level for which the attenuation can be activated was not critical. In the same section we have shown that the limit to which the dynamic range can be extended is limited by the magnitude of the intercept reference voltage  $V_{REF\_I}$  that is used.

Equation (3.33), which we have developed in Section 3.4, described the slope calibration parameters of the overall fixation system depicted in Figure 3.22. This equation showed us that we can set the slope of the log transfer, by setting the parameters  $\alpha$ ,  $B$  and  $V_{REF\_S}$ , where parameter  $\alpha$  represented the ratio between the two resistance values of the resistors  $R_{S1}$  and  $R_{S2}$ ,  $B$  represented the attenuation factor  $B$  which is set by the differential resistor ratio of the resistors inside the divider block and  $V_{REF\_S}$  represented the reference voltage which is used to set the

wanted slope information voltage  $V_{OUT\_S}$ . In Subsection 5.2.2.3, where we discussed the resistor mismatch of the new proposed divider block, we have explained that the ratio between resistors can be obtained with very high accuracy. With the knowledge that very high accuracy in resistor ratios can be obtained, Equation (3.33) showed us that the slope calibration accuracy will mostly depend on how accurate the reference voltage  $V_{REF\_S}$  can be set. However in Section 3.2.1 we have shown that this assumption can only come true when we obtain an accurate multiplication factor  $A$ .

We explained that when  $V_{REF\_S}$  is delivered by an accurate off chip voltage reference the slope can be manually set to an accurate and arbitrary value while in the meantime the fixation system will maintain the slope, intercept and dynamic range fixation. From this we concluded that a possible deviation in the expected multiplication factor  $A$  can be compensated. However as was stated in Section 4 the slope fixation system can also be used to automatically set the slope to a correct fixed and predefined value without the use of manual calibration if the slope fixation system can be made less sensitive to non-idealities. From Subsection 2.4.2 we know that the accuracy or log linearity of logarithmic devices is examined by the conformance error. In that section we pointed out that the conformance error has to stay between +1.0 dB and -1.0 dB. So, to make calibration after production unnecessary, we have to make sure that the error contributions of the non-idealities in the system are low enough, such that the log device does not exceed these log conformance requirements.

With the system level simulations in Section 4.3 we have investigated the sensitivity to the non-idealities like input offsets, deviations in reference voltages and resistor ratios. It was shown (Figure 4.7) that for the analysis of the sensitivity to these non-idealities, the system can be divided into two system parts; the control system that is responsible for setting the multiplication factor  $A$  (and the gain of the cascaded A/O cells) and the system part which is responsible for controlling the transconductance of the G/O cells. The graphs in Figure 4.10 showed us the maximum allowed deviation of the multiplication factor and the maximum allowed deviation in G/O cell transconductance, for a particular limit in the conformance error. From this figure we concluded that, to reach a log conformance between the -1dB and 1dB band over the full dynamic range, the effect of non-idealities in the multiplication control system should be minimized to levels that result in a maximum of 3.8% deviation in the multiplication factor  $A$ . Fortunately we found a procedure (Subsection 4.3.1) to increase this maximum allowed deviation. It was shown that by slightly modifying the attenuation factor  $B$  of the divider block the maximum deviation of the multiplication factor can be extended to 4.5%. Furthermore it was shown that, to obtain the better than 1 dB log conformance over the full dynamic range, the effect of non idealities in the transconductance control system should be limited to levels which will minimize the deviation in the transconductance of the G/O cells below 5.2%.

In Subsection 4.3.1.1.2.1 and 4.3.1.1.2.2 we have shown that the sensitivity to input offset of the error amplifier OA2 and deviation in the reference voltage  $V_{REF\_S}$  can easily be reduced. For this reduction we have proposed an architecture (Figure 3.22) that made it possible to increase the reference voltage  $V_{REF\_S}$  to much higher magnitudes than the expected input offset of the error amplifier OA2. It was shown that with the proposed architecture the reference voltage  $V_{REF\_S}$  can be increased with the same ratio as the resistance ratio  $\alpha$  between the resistors  $R_{S1}$  and  $R_{S2}$  without altering the actual slope of the log transfer. As was shown by the graphs in Figure 4.12 the system can reach negligible sensitivity for input offset and deviation of the reference voltage when for example  $V_{REF\_S}$  is set to 2V.

The accuracy of the multiplication system was more difficult to obtain as we were constrained by the limited input voltage of the multiplication cell  $M_{COPY}$ . The limited input of  $M_{COPY}$  was necessary to make the error amplifier OA1 sensing the small signal gain of the cell  $M_{COPY}$ . As was shown by Figure 4.11, the limited input signal resulted in a multiplication control system which was highly sensitive for input offsets in the multiplication control system.

To reduce the sensitivity to input offset in the multiplication control system we have developed an control system in which the offset sensitivity is minimized. To reach low sensitivity for the input offsets we incorporated the chopping technique into the circuit implementation of the fixation system (Figure 5.9). For the implementation of the chopping architecture we came up with a new output demodulation concept. It was shown that the output chopper (CH<sub>3</sub> in Figure 5.23) can be used to switch the gate connected node and output node of the active load (M1-M2 in Figure 5.23) in such a way that it resulted in a single ended demodulated output signal. However, later literature showed that this implementation was already used in another work.

We have shown that the resulting signal of the chopped system contains a residual ripple from which the magnitude of the ripple depends on the offsets inside the chopped gain fixation system. To remove the residual ripple from the demodulated signal we have introduced in Section 5.2.5.2 a new filter concept. System simulations in Subsection 5.2.5.2.2 have shown that the new filter (Figure 5.35) is capable of completely removing the residual ripple from the demodulated output signal of the chopped system while attaining a fast response and small feature sizes.

As was stated earlier the effect of the expected input offsets at the multiplication cell  $M_{COPY}$  and the DDA had to be minimized to obtain a maximum deviation in the control signal well below 5.5%. Simulation results (Chapter 6) of the final gain fixation circuit implementation (Figures 5.45-5.46) have shown that we could limit the deviation to much lower levels than this maximum allowed deviation. Furthermore it was shown that the circuitry is stable and accurate over the temperature range from -55°C to 125°C. With the knowledge that the maximum deviation in the control signal obtained by the G/0 control system can be minimized easily with the use of an high reference voltage  $V_{REF\_S}$  (Figure 4.12) we can conclude that the deviation in the G/0 transconductance control system can be minimized to levels much below the maximum allowed deviation (Subsection 4.3.1) of 5.2%

As both system parts show a possibility for very low sensitivity to non-idealities in comparison with the allowed deviations we expect that the new overall fixation system can be implemented to obtain a slope, intercept and dynamic range fixated transfer of the log device which falls in-between the 1dB and -1dB log conformance band without the need for manual calibration.





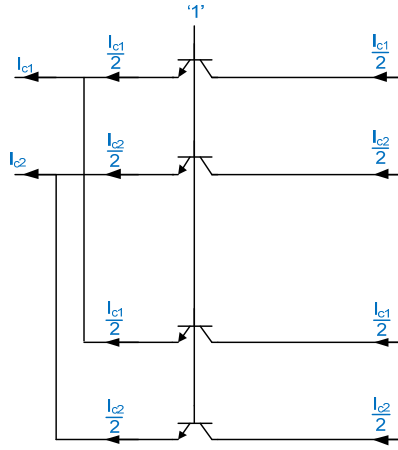
## 8 Recommendations

### 8.1 Preventing hang up of detector control system

In Appendix B the circuitry of the detector cell is discussed. When using this cell we recommend to ensure that during start-up of the G/0 control loop the base of BJT  $Q_4$  (Figure B.) does not exceed the value for which the transistor starts to work in saturation region. When  $V_{be}$  of this transistor exceeds the  $V_{CE}$  voltage of  $Q_4$  the control loop will switch to feed forward operation instead of negative feedback, resulting in a latch up of the system

### 8.2 Current Splitting

In Figure 3.22 we have shown that the current output of the log device has to be split into two equal currents. For the implementation of the current splitter we recommend the configuration as shown in Figure 8.1.

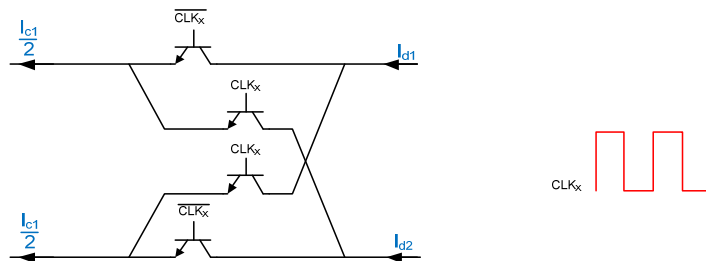


**Figure 8.1** Current splitting architecture

The 4 bipolar transistors (in Figure 8.1 assumed to have infinite beta) are configured as common base stages, knowing to have low input impedance and high output impedance.

### 8.3 Commutating switch

For the commutating switches as shown in Figure 3.22, we recommend the circuit configuration as shown in Figure 8.2

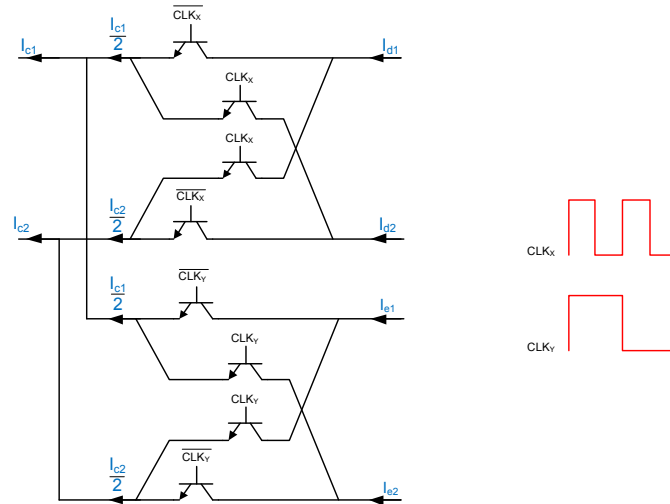


**Figure 8.2** Example of the commutating switch in Figure 3.22

[75] For the bipolar switches to work correctly in the fixation system the clock has to switch between levels for which the npn-transistors switch between their forward active and cut-off region.

## 8.4 Current split/commutating switches

For the current split operation and inverting operation we recommend the investigation of an architecture that can combine the split and commutating operation. The proposed architecture is shown in Figure 8.3



**Figure 8.3** Current splitting architecture with inverting operation

This architecture maybe helpfully when more voltage headroom in the signal path is required.

## 8.5 Ripple reduction of the output signals

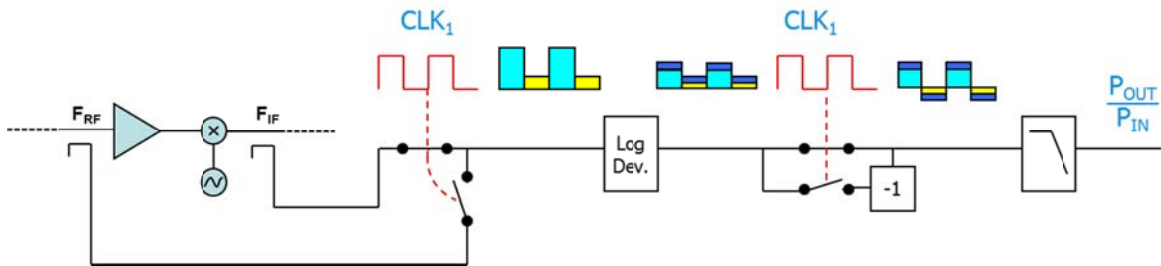
In Section 3.2 we assumed that the resulting output signal  $\overline{V_{OUT}}$  and  $V_{OUT,S}$  were pure DC output signals. However a pure DC signal is only obtained when the frequency components of the modulated input currents ( $I_d$  and  $I_e$  in Figure 3.22) are fully suppressed by the integrators. For high suppression of the ripple the integrator capacitors sizes have to very be big. For a significant reduction of these capacitors sizes and still obtain complete suppression we recommend to investigate the possibility to place the new ripple blocking system (discussed in Section 5.2.5.2) at the output of each of the integrators. In this situation the allowed ripple magnitude at the output of the integrators can be increased, which shows a possibility for much smaller capacitor sizes. The residual ripple at the output of the integrator can be blocked by the ripple blocking system.

## 8.6 Full CMOS implementation

We recommend the investigation of a full MOS implementation of the system. This may result in a more accurate system as the system will not suffer from base currents. Several tanh cell implementations in MOS technology exist. As MOS gates don't suffer from DC current leakage the sensitivity to loading effects may be solved

## 8.7 New power gain calculation architecture

Power gain calculation is normally obtained by using two log detectors in parallel, as was discussed in section 1.8.3. and shown in Figure 2.21. For a new method to obtain a possibly higher accurate gain calculation without the need of two highly matched log power detectors we recommend to investigate the implementation as given in Figure 8.4



**Figure 8.4** Proposed power gain calculation

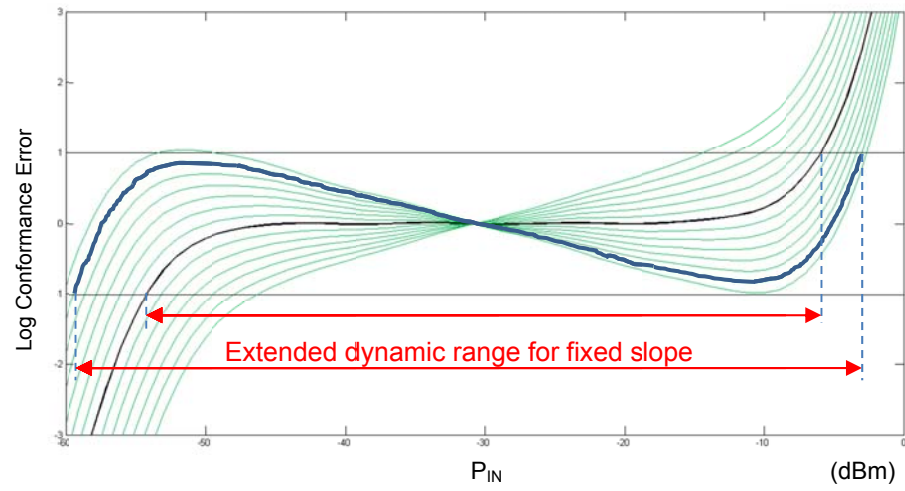
As shown by this figure the system looks like the intercept fixation system, discussed in Subsection 3.1. However, instead of a reference voltage for the fixation of the intercept the input is used for another power input. As only one single log detector is used for the input power and output power measurement, maybe a power calculation can be obtained without the need for two matched log detectors.

## 8.8 Linear gain stabilization

The slope fixation method described in this report shows applicable to be implemented for linear gain stages. In this situation a slope fixation may be obtained by alternately adding an accurate DC offset at the input of the linear stage instead of a multiplication as it was for the logarithmic device.

## 8.9 Method to extending the dynamic range when slope is fixation is guaranteed

When looking at Figure 4.8 and 4.9 we can observe an possible dynamic range extension when slope can be fixated at an guaranteed position. By adjusting the reference voltage  $V_{REF\_S}$  (Figure 3.22) the slope can be deviated from normally wanted 0dB log conformance position. From Figure 4.8 and 4.9 we can see that when the slope deviate from ideal position the log conformance curve will be tilted. When tilted to the correct direction the log conformance will getting worse for two input ranges, however the dynamic range itself will be extended. The proposed concept is shown in Figure 8.5. When slope fixation can be guaranteed by the fixation system the dynamic range can be extended by modifying  $V_{REF\_S}$ .



**Figure 8.5** When slope can be fixated at an guaranteed position dynamic range can be extended.

## Appendix A Overall accuracy analysis

In this appendix we will develop an overall equation that will include all errors treated in section 4.3.1.1.

To have a clear overview we will first obtain multiple equations to determine the deviation in the multiplication factor for each error. Hereafter we combine them to one overall equation.

We start by taking the derivative of Equation (4.6) to all the error parameters, followed by a multiplication with the value of the expected error. This result in the following equations

$$\delta_{A1} = f_A'(V_{OS1})\Delta V_{OS1} = \frac{(V_{OS2} - V_{REF\_M})}{\left(\frac{V_{REF\_M}}{B} + V_{OS1}\right)^2} \Delta V_{OS1} \quad (A.1)$$

$$\delta_{A2} = f_A'(V_{OS2})\Delta V_{OS2} = -\frac{1}{\left(\frac{V_{REF\_M}}{B} + V_{OS1}\right)^2} \Delta V_{OS2} \quad (A.2)$$

$$\delta_{A3} = f_A'(B)\Delta B = \left( \frac{(V_{REF\_M} - V_{OS2})}{\left(\frac{V_{REF\_M}}{B} + V_{OS1}\right)^2} \frac{V_{REF\_M}}{B^2} \right) \Delta B \quad (A.3)$$

Now, if we want to know the worst case of the possible change of the multiplication factor we could simply add the absolute values of Equations (A.1-A.3). But, because we are dealing with random errors, it is better to look for the expected change. To calculate the expected change, we first have to square Equation (A.1-A.3), after which we have to add them and then take the square root of the total sum. With this knowledge we construct the equation for calculating the percentage change in the multiplication when including all important errors.

$$\varepsilon_A = \frac{\sqrt{\delta_{A1}^2 + \delta_{A2}^2 + (\delta_{A3}B)^2}}{B} 100\% \quad (A.4)$$

The same procedure will be used to develop the equation to calculate the percentage change in the transconductance of the detectors.

So, again we take the derivative to all errors but now for Equation (4.21). Multiplying these derivatives with the expected error, we construct the equation for calculating the change caused by each error

$$\delta_{G1} = f'_G(V_{OS3})\Delta V_{OS3} = -\frac{V_{OS3}}{V_{REF\_S}}\Delta V_{OS3} \quad (A.5)$$

$$\delta_{G2} = f'_G(V_{REF\_S})\Delta V_{REF\_S} = \frac{\Delta V_{REF\_S}}{V_{REF\_S}}\Delta V_{REF\_S} \quad (A.6)$$

From which we can construct the equation to calculate the percentage change in the transconductance

$$\varepsilon_G = \frac{\sqrt{\delta_{G1}^2 + \delta_{G2}^2}}{\left(\frac{2 \cdot V_{REF\_S}}{R_{S2} E_K}\right)} 100\% \quad (A.7)$$

Section 4.32 and Section 4.33 showed the equations to calculate the error  $\varepsilon_{multiplication\_cell}$  caused by mismatch between the multiplication cells (Equation (4.19)) and the mismatch  $\varepsilon_{\Delta R}$  between the expected ratio of the resistors  $R_{S1}$  and  $R_{S2}$  (Equation (4.29)). Furthermore we developed the equation for the current splitting error  $\psi_I$  (Equation (5.23)). With those equations in mind we now have all the important equations to complete the overall equation. Because of the random nature of the deviations we can construct the overall formula as follows

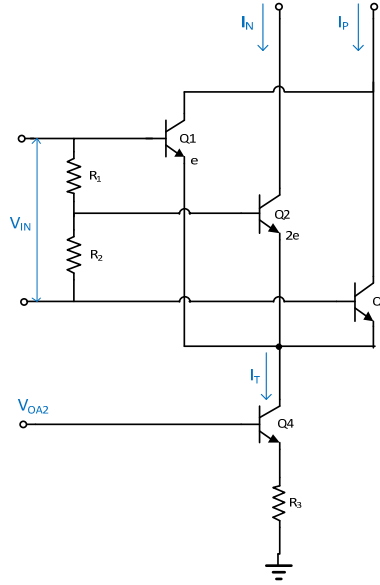
$$dB\_accuracy = \sqrt{\frac{(\varepsilon_A)^2 + (\varepsilon_{multiplication\_cell})^2}{4.5\%} + \frac{(\varepsilon_G)^2 + (\varepsilon_{\Delta R})^2 + (\varepsilon_I)^2}{5.2\%}} \quad (A.8)$$

Where the division by 4.5% and 5.2% are the percentage deviations in the multiplication control circuit and the G/0 control circuit respectively, for which the log conformance at -50dBm was 1 or -1dB as was discussed in Section 4.3.1

## Appendix B The detector cell

In this appendix we will discuss the detector cell. From Section 2.1 we know that the detector cells are used to perform the rectification or absolute function over their RF input voltage. With the absolute function we mean that the detector (in this case an rectifying transconductance cell) has to generate the same differential output current for differential input voltages which are equal in value but contrary in polarity.

A detector cell is shown in Figure B.1. This detector cell was invented by [76].



**Figure B.0.1** The implementation of a detector cell

As shown by Figure B.1 the differential input voltage  $V_{IN}$  is applied across the bases of transistor  $Q_1$  and  $Q_3$ . At the same time the base of  $Q_2$  is held at the midpoint of  $V_{IN}$  by the resistive voltage divider which is formed by matched resistors  $R_1$  and  $R_2$ .

The transistor  $Q_4$  is used as current source and provide the tail current,  $I_T$ , for the transistors  $T_1$ - $T_3$ . To ensure accurate matching of the tail currents of all detector cells a emitter degeneration resistor  $R_3$  is placed.

The current  $I_P$  together with current  $I_N$  constitute the differential output current of the detector. As shown by Figure B.1 the current  $I_P$  is the sum of the collector currents of transistor  $Q_1$  and  $Q_3$ , while the output current  $I_N$  is simply the collector current of  $Q_2$ .

To see how the resistive divider together with the tree transistors  $Q_1$ - $Q_3$  performs the actual rectification of the differential input signal, we will first examine the situation for zero differential input. When a zero differential input voltage is applied to the detector it should output a zero differential current. So, for zero differential input voltage,  $I_P$  should be equal to  $I_N$ . To obtain this, it can be shown that the emitter area of  $Q_2$  has to be two times bigger than that of the emitter area of  $Q_1$  and  $Q_3$ .

This can easily be seen, as for zero differential input voltage the base voltages of the three transistors will be equal. With a two times bigger emitter area of  $Q_2$  in comparison with that of  $Q_1$  and  $Q_3$ , the collector current of  $Q_2$ , and thus  $I_N$ , will be two times bigger than the collector currents of the other two transistors. As the collectors of  $Q_1$  and  $Q_3$  are connected to each other, the resulting summation of the collector currents makes that the current  $I_P$  and  $I_N$  will be equal.

Now, let's examine the rectification mechanism of the detector. When change the polarity of the input voltage  $V_{IN}$  and let the common mode voltage (midpoint voltage of  $V_{IN}$ ) the base voltages of the transistors  $Q_1$  and  $Q_3$  are actually exchanged. So the current which was first delivered by  $Q_1$  will now be delivered by  $Q_3$  and the current first delivered by  $Q_3$  is now delivered by  $Q_1$ . As the collectors of both transistors are connected to each other one can see that the resulting sum,  $I_P$ , of the currents will be the same for both polarities.

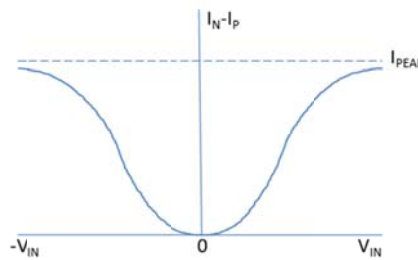
Furthermore, with the knowledge of Kirchhoff's current law the following equation will hold.

$$I_N + I_P = I_T \quad (5.59)$$

Assuming constant tail current  $I_T$  one can see that when  $I_P$  goes up  $I_N$  has to go down or vice versa. This shows that the detector output operates differential.

In Chapter 2 we examined that the maximum output current or peak current of a G/O stage is  $GE_K$ . By Equation (2.32) it was shown that the slope of the successive approximation logarithmic detector depends on this peak current.

As the transconductance  $G$  of the G/O cell can be set by the tail current the maximal differential output current,  $I_{PEAK}$ , available from the detector cell when the input signal is large is related to the bias current  $I_T$ .



**Figure B.0.2** *V-I response of the detector cell*

The level of bias current  $I_T$  is determined by the bias voltage applied to the base  $Q_4$ . As was discussed in chapter 3 and shown in Figure 3.12, the bias voltage to the detector cells will be adjusted by the error amplifier AO2 in response to the output  $V_{OUT\_S}$ . The slope, determined by  $I_{PEAK}$ , may be affected by factors such as the frequency of the input signal, process variations, temperature, power supply, etc. When  $I_{PEAK}$  compensated by a feedback loop the slope of the log detector may be stabilized.



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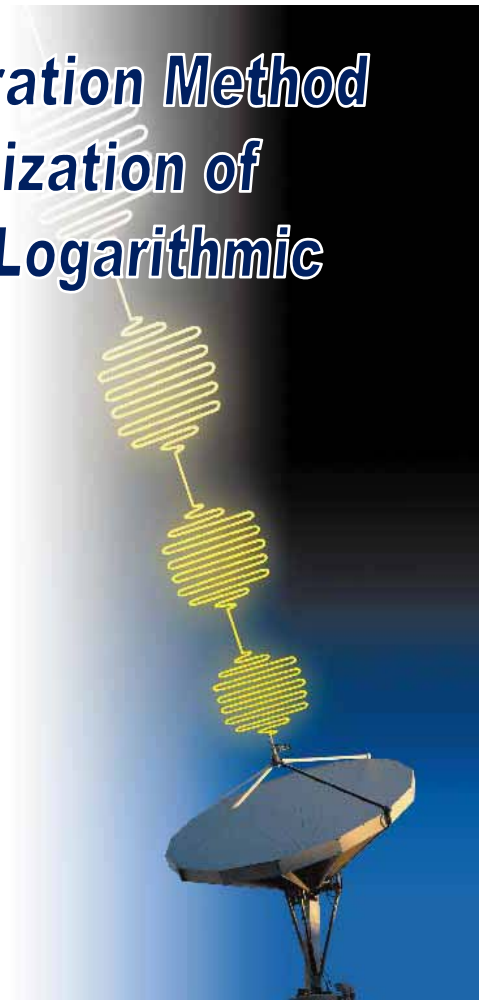
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# A Novel Continuous Calibration Method For the Transfer Stabilization of Successive Compression Logarithmic Amplifiers

*Vincent R. Bleeker B.Eng.*



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- *The Successive Compression Logarithmic Amplifier*

### **2. New method for the stabilization of the logarithmic transfer**

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- *Intercept fixation*
- *Dynamic range extension*
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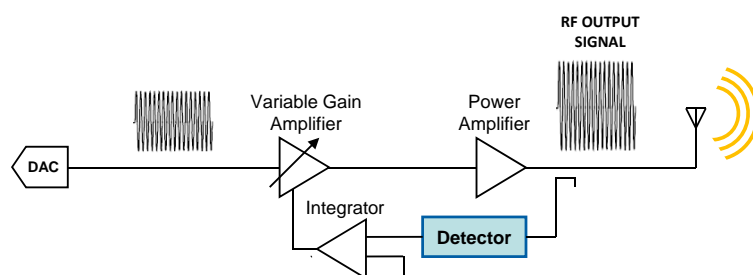
## 7. Questions

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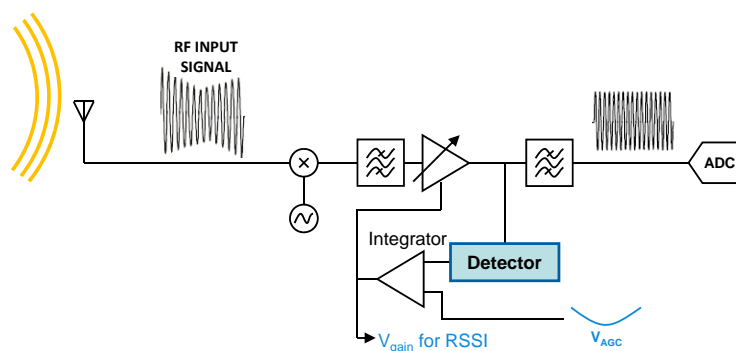
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## Introduction to RF power detectors

Transmitter



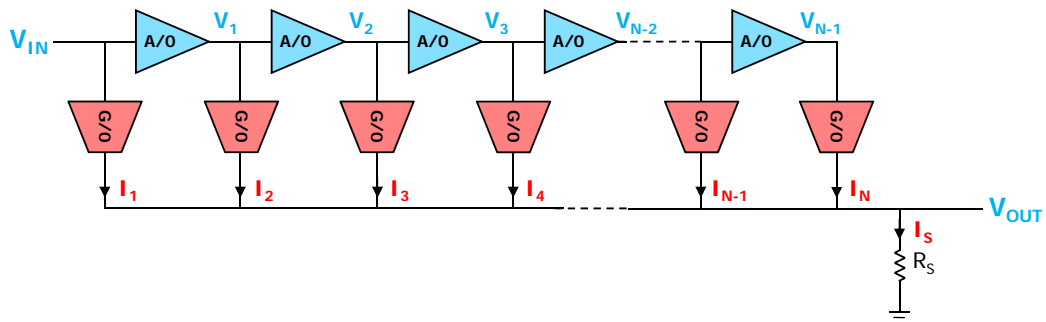
Receiver



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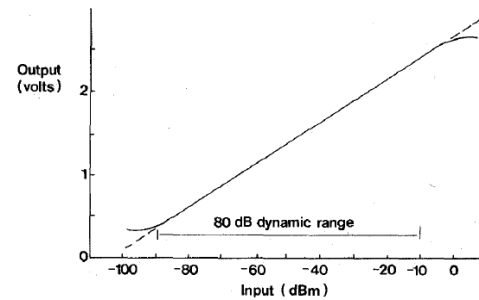
# Introduction to the Successive Compression Logarithmic Amplifier



Cascade of low-gain high-bandwidth stages obtains:

- High overall bandwidth
- High dynamic range

Logarithmic responding RF power detection

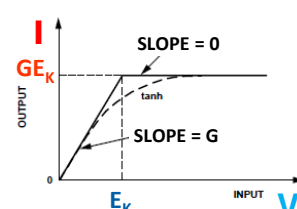
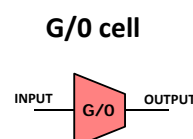
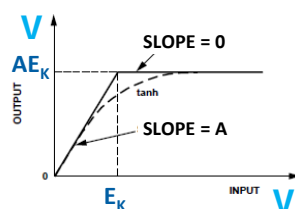
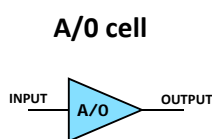
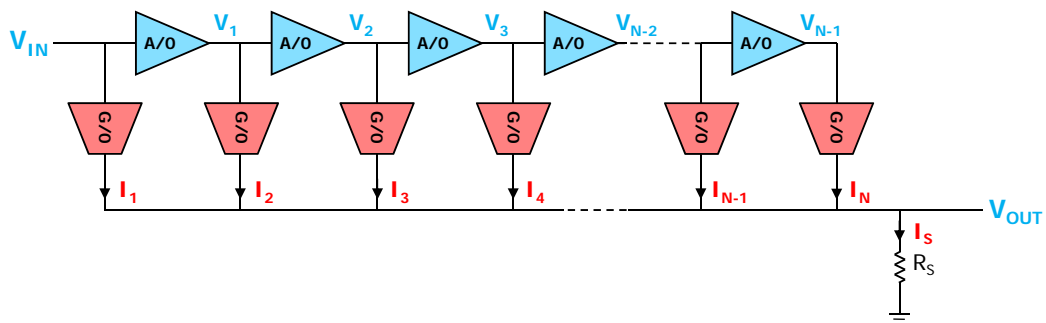


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## Introduction

Successive Compression Logarithmic Amplifier



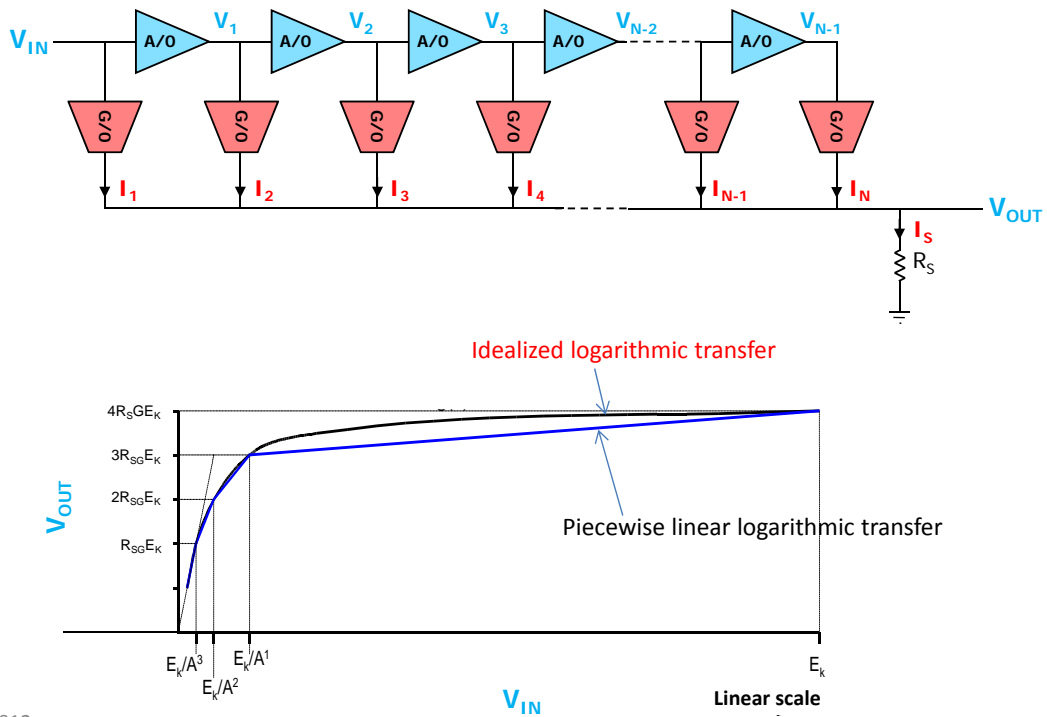
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# Introduction

## Successive Compression Logarithmic Amplifier

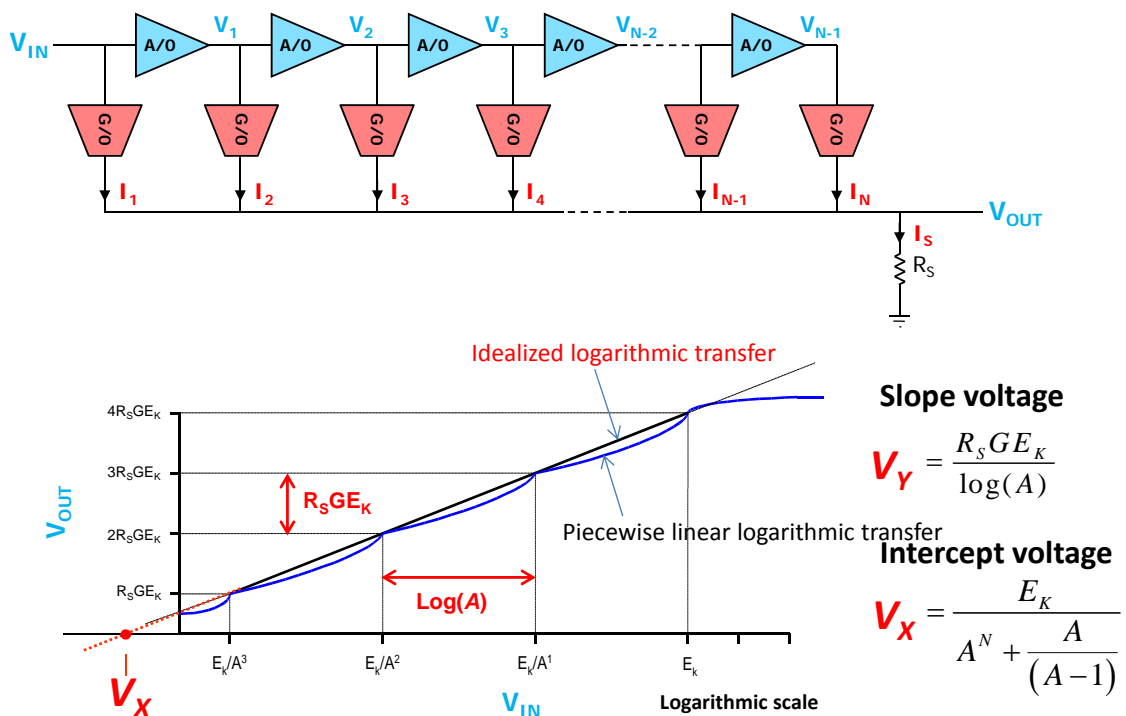


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# Introduction

## Successive Compression Logarithmic Amplifier

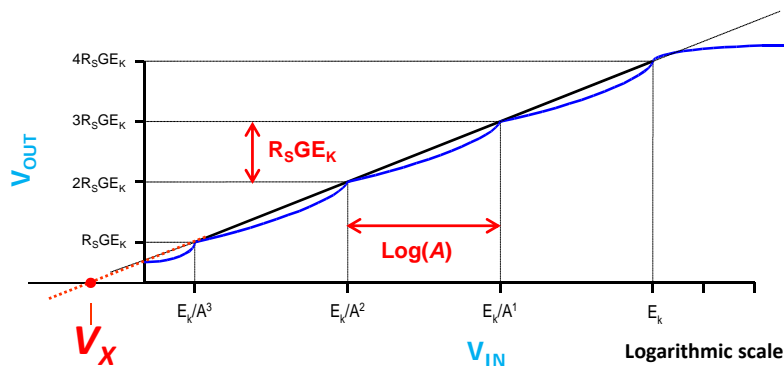
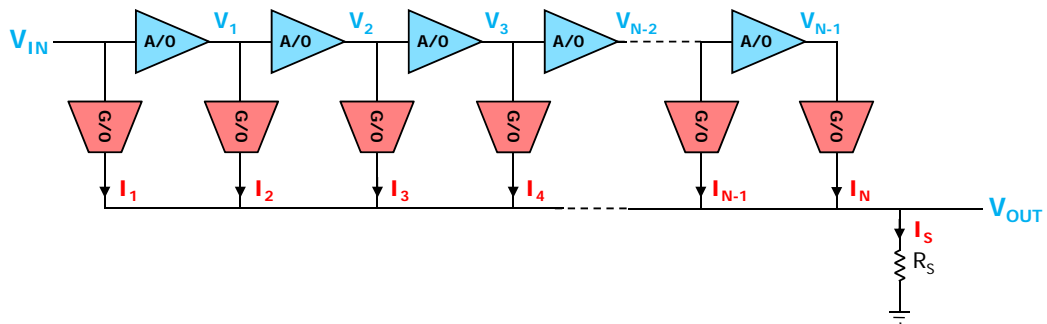


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# Introduction

## Successive Compression Logarithmic Amplifier



Slope voltage

$$V_Y = \frac{R_S G E_K}{\log(A)}$$

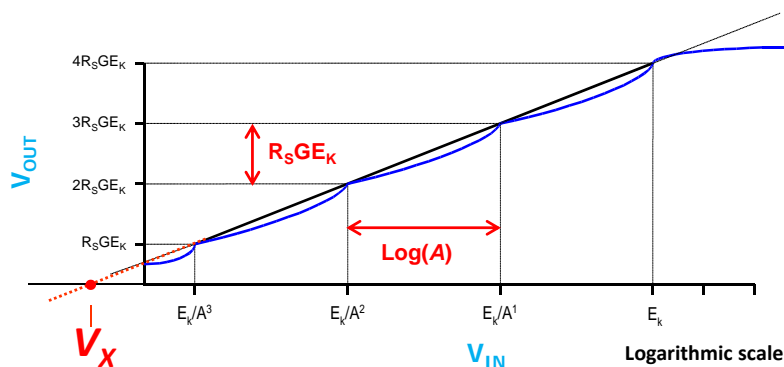
Intercept voltage

$$V_X = \frac{E_K}{A^N + \frac{A}{(A-1)}}$$

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# Introduction



Slope voltage

$$V_Y = \frac{R_S G E_K}{\log(A)}$$

Intercept voltage

$$V_X = \frac{E_K}{A^N + \frac{A}{(A-1)}}$$

Transfer is sensitive to variations in:

- Temperature ( $E_K$ )
- Gain  $A$
- Transconductance  $G$
- Resistance  $R_S$

$$V_{OUT} = V_Y \log \left( \frac{V_{IN}}{V_X} \right)$$

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## 5. Circuit simulation results

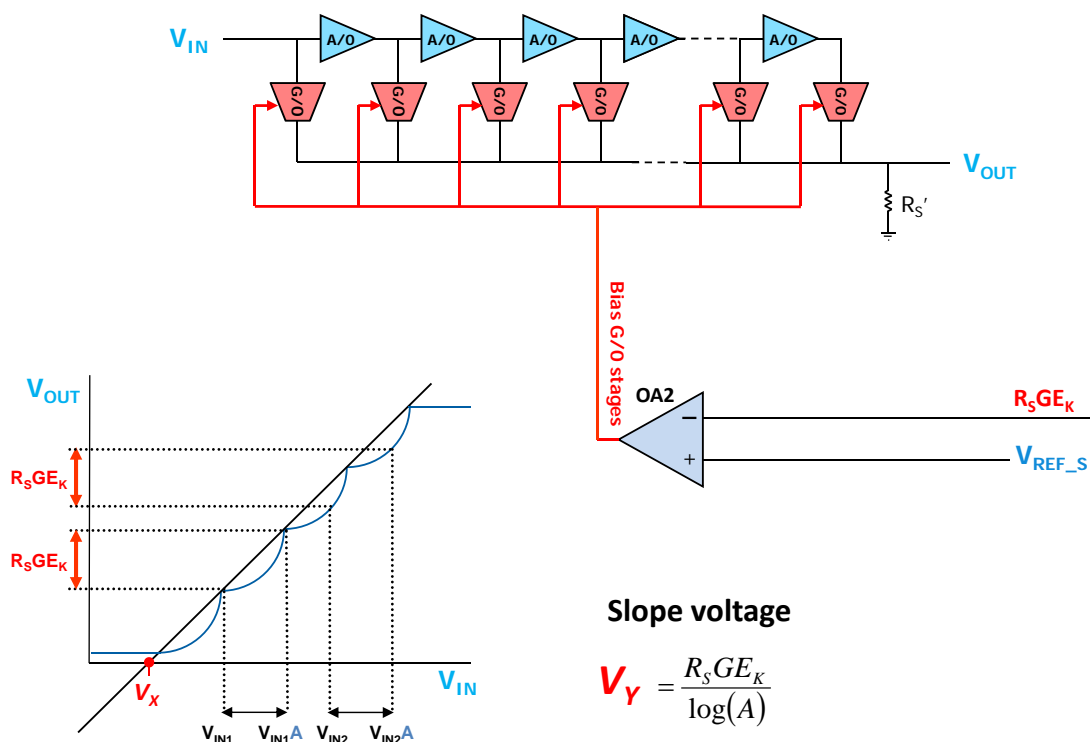
## 6. Conclusions

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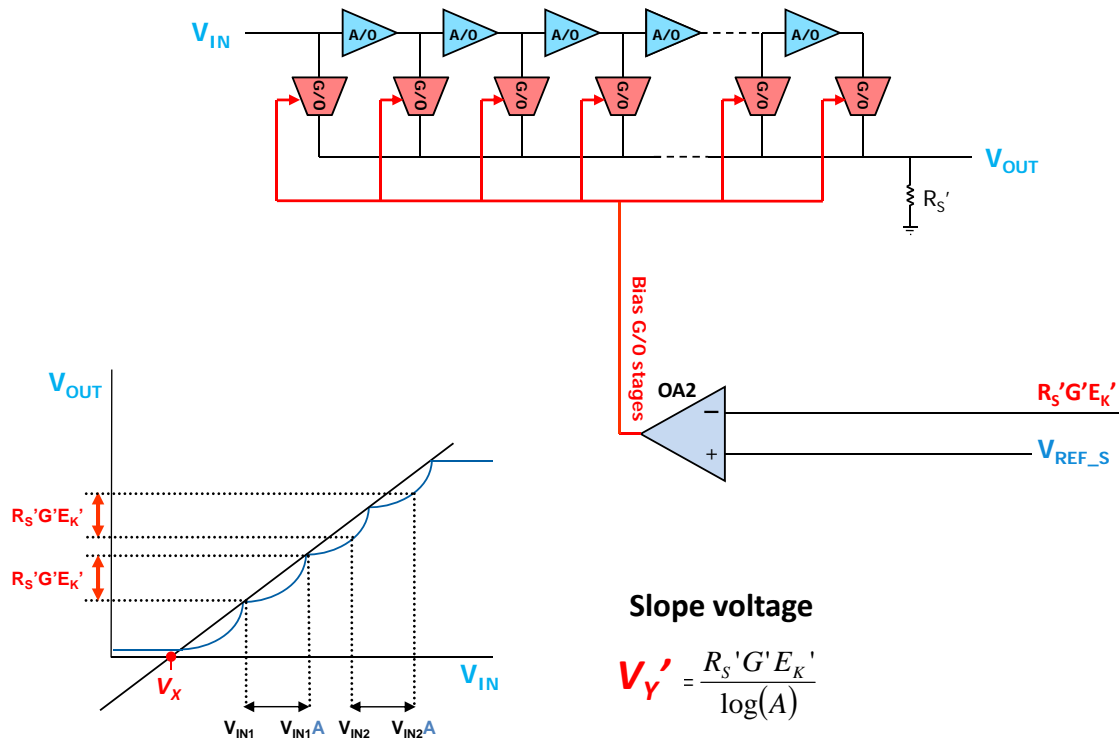
## Slope fixation



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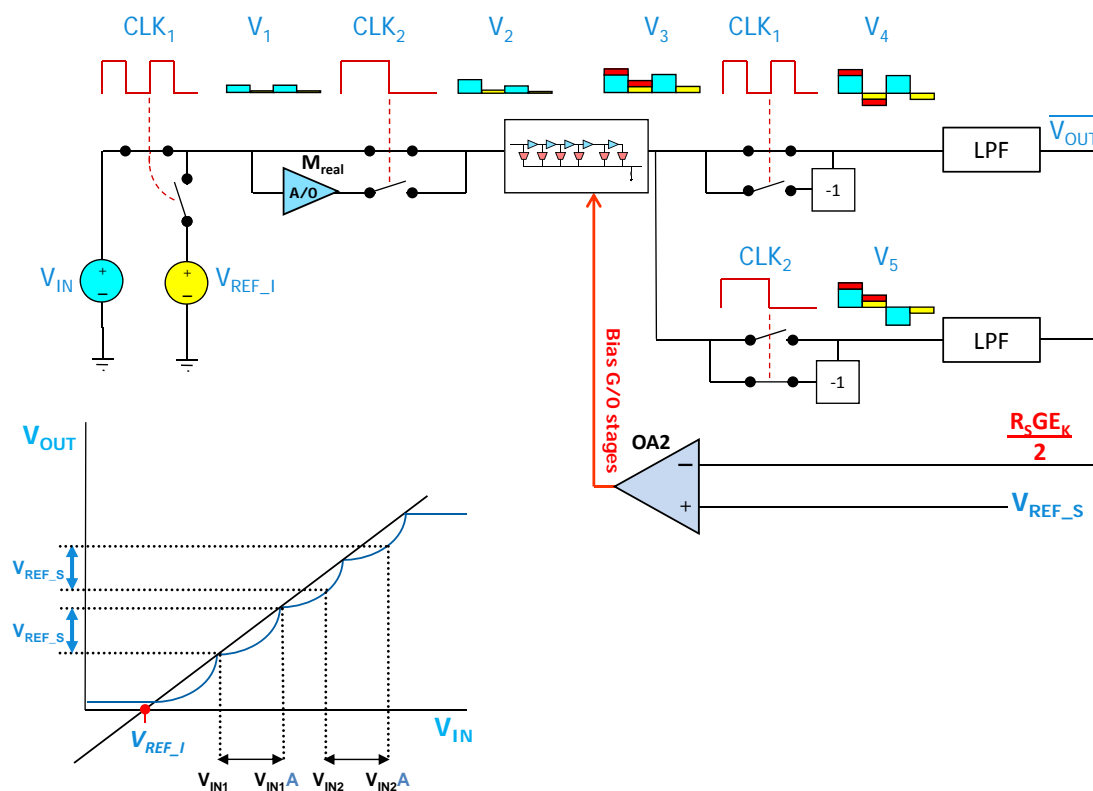
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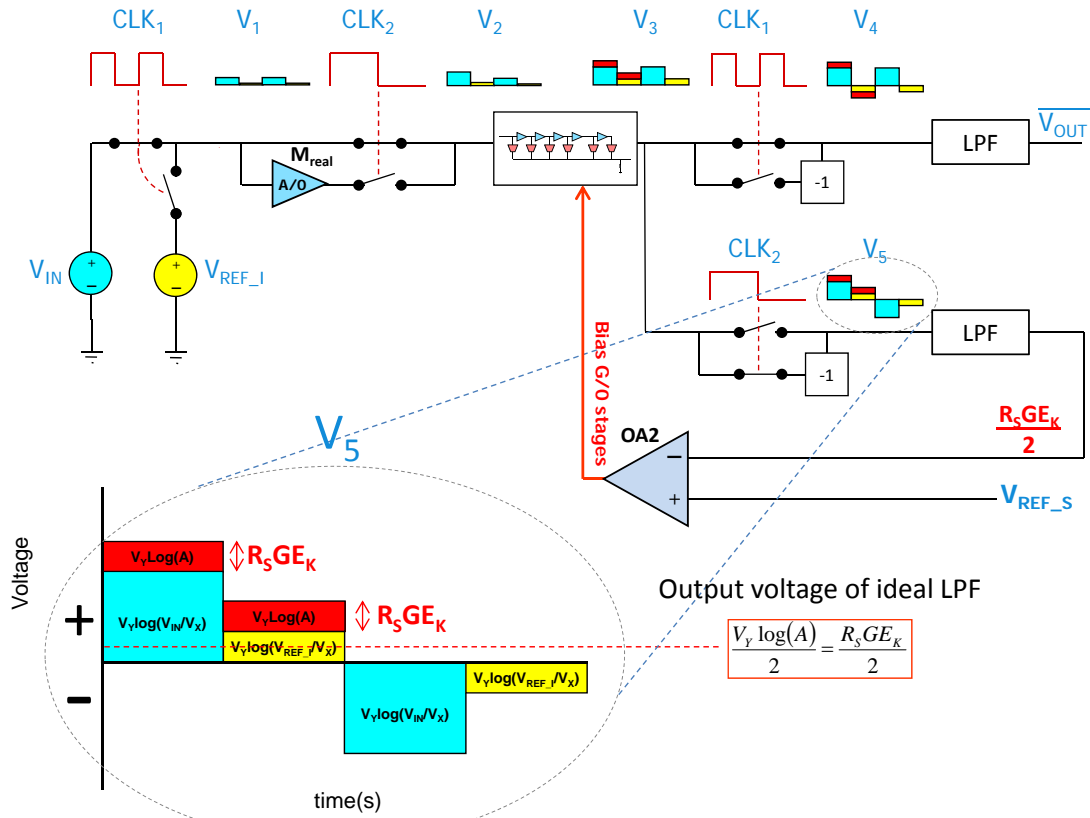
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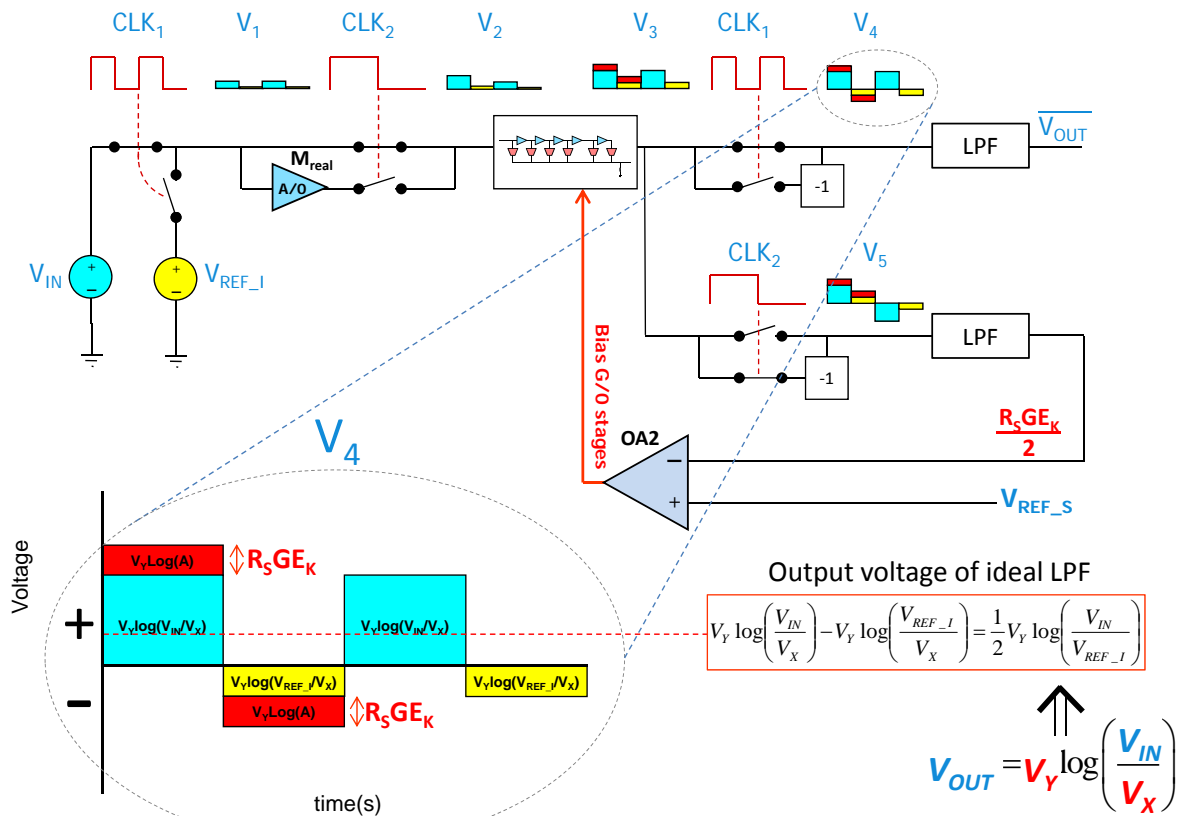
## Slope fixation



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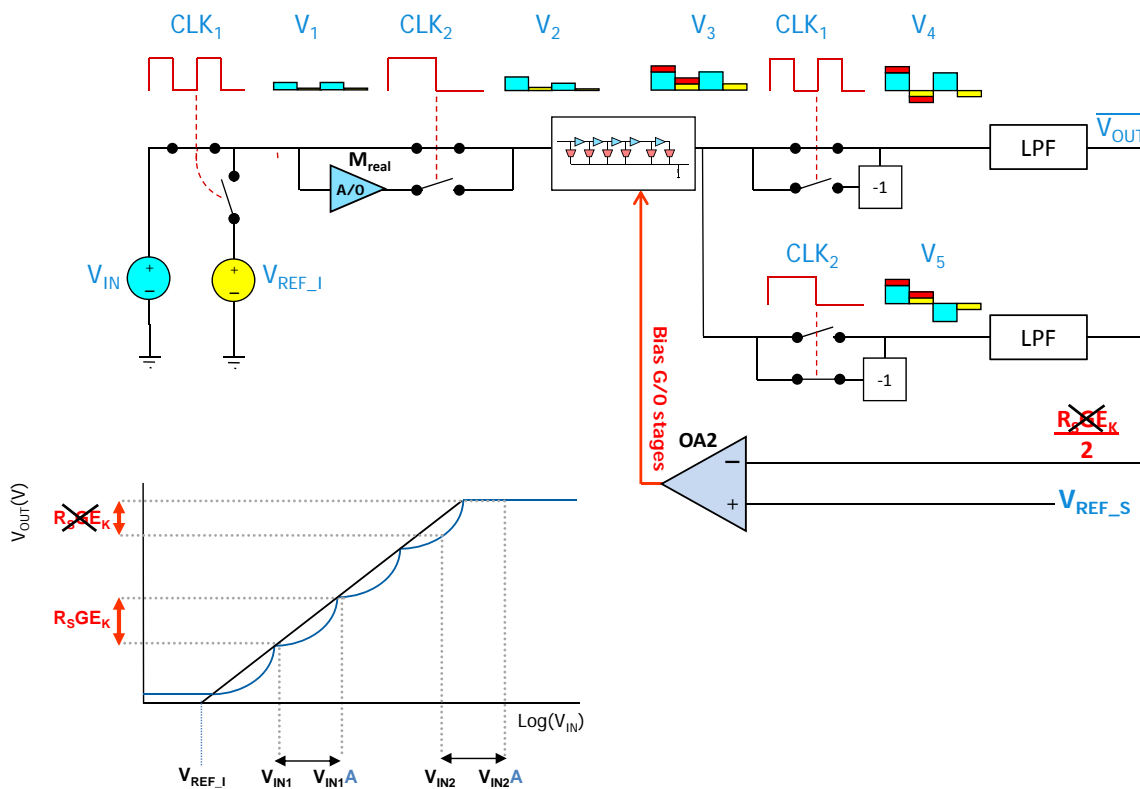
## Intercept fixation



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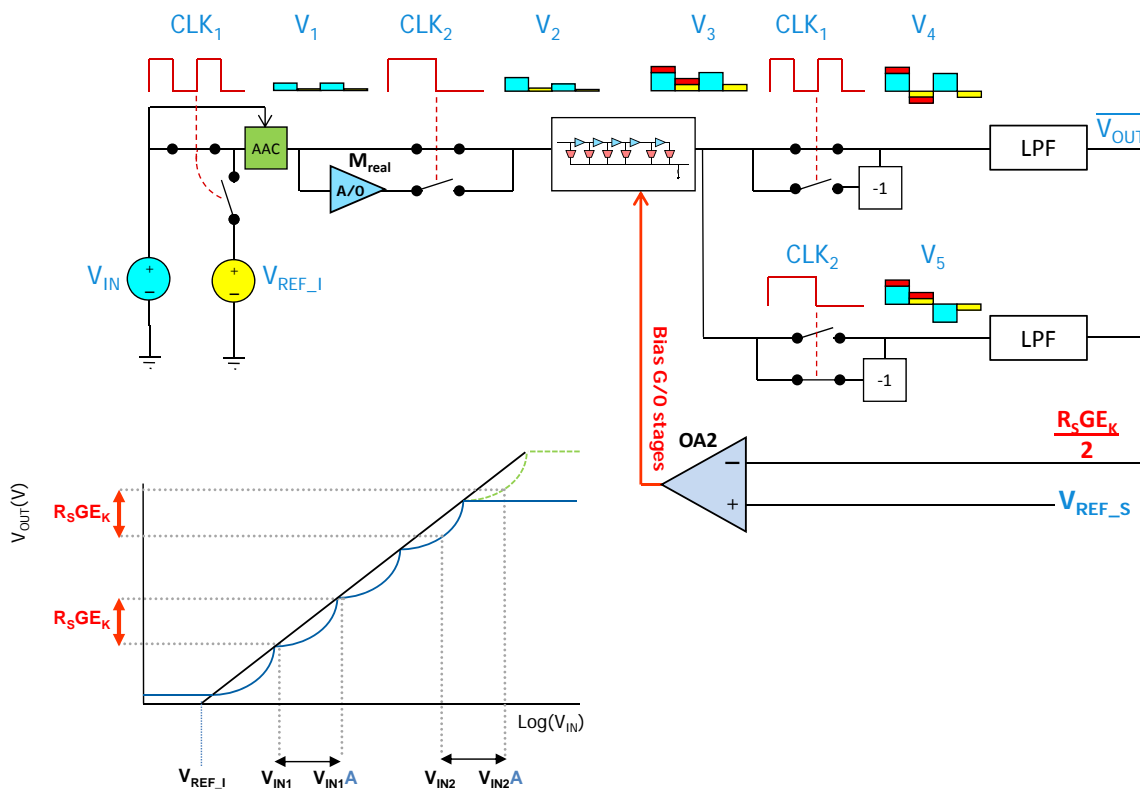
## Dynamic range extension



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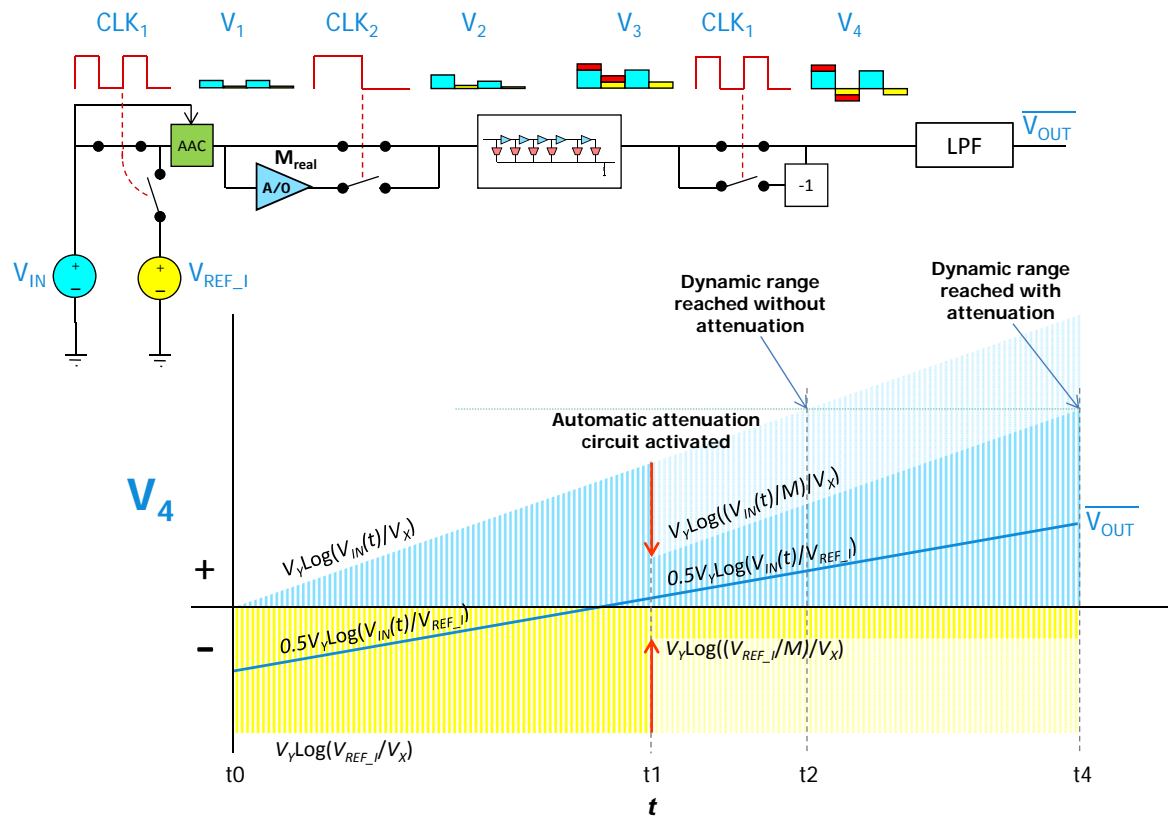
## Dynamic range extension



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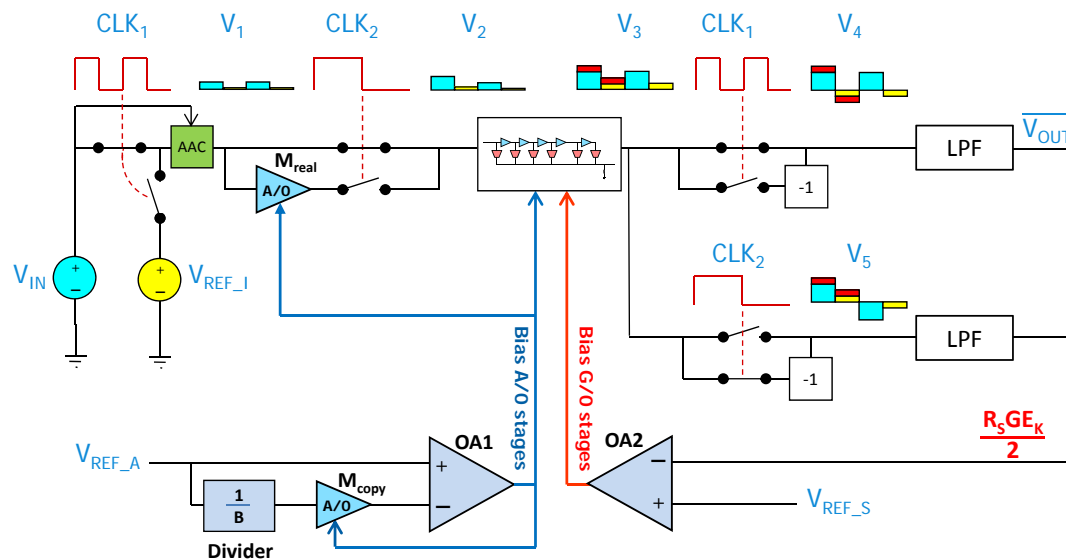
# Dynamic range extension



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# Gain fixation

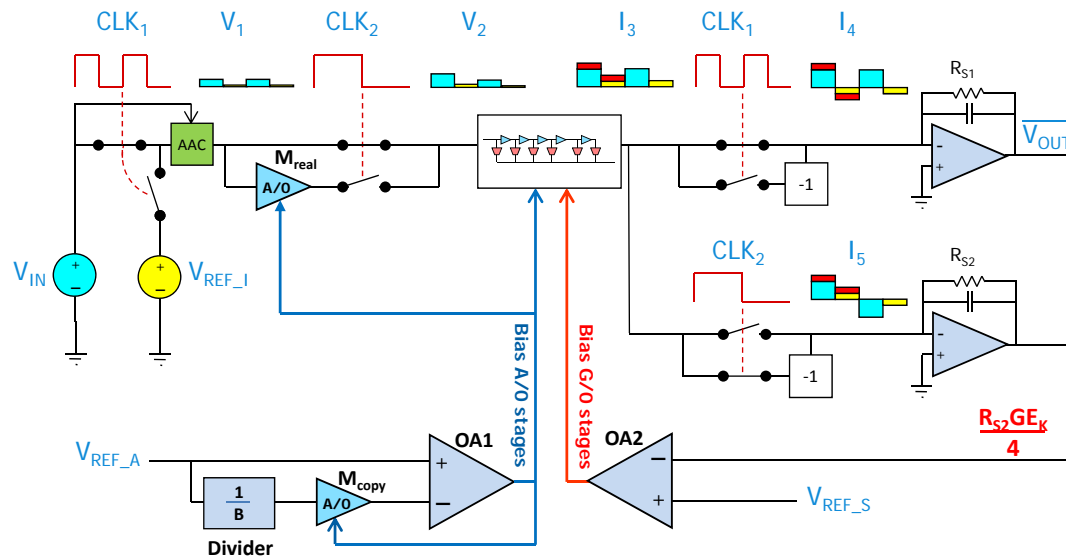


Gain  $A$  of  $M_{REAL}$  and the reference voltage  $V_{REF\_S}$  has to be accurately set to a known value to fixate the slope at wanted position.

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# Gain fixation



Value  $B$  of the divider block is used to set the gain  $A$  of  $M_{REAL}$ ,  $M_{COPY}$  and the cascaded A/O stages.

$$Slope = \frac{V_{REF\_S}}{\frac{R_{S2}}{R_{S1}} \cdot 20 \log(B)}$$

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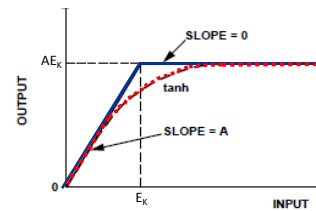
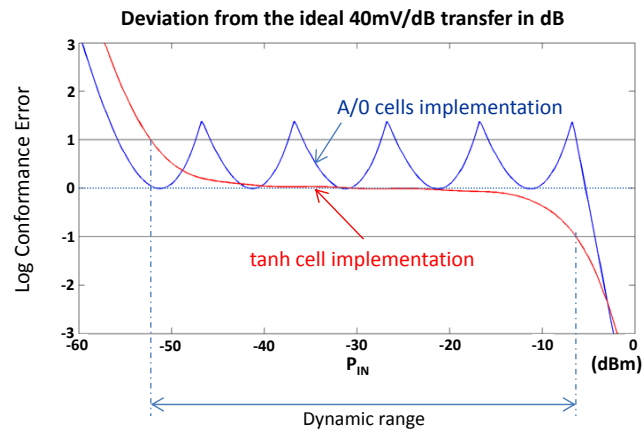
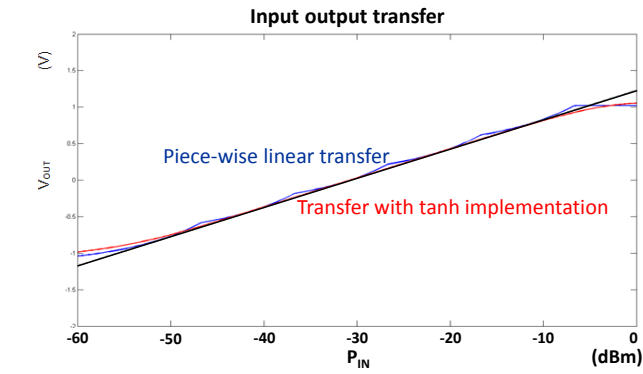
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# System simulation results

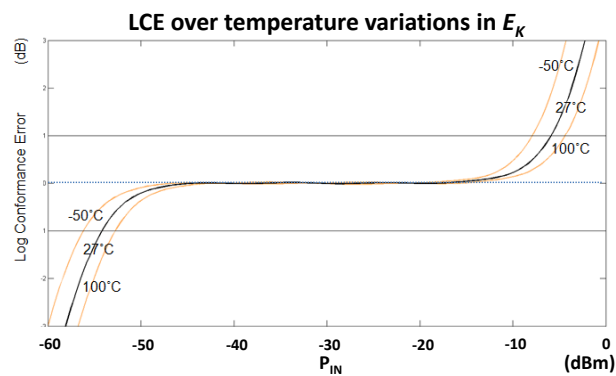
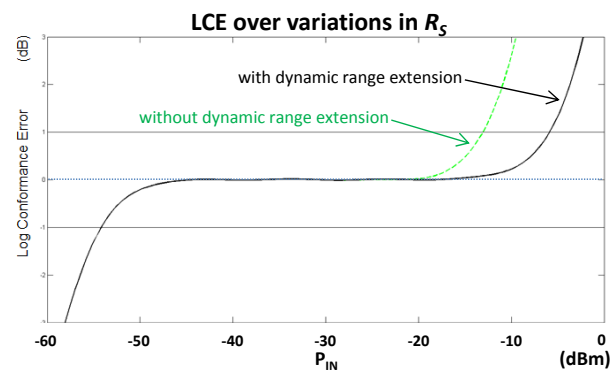
Slope set to 40mV/dB  
Intercept set to -30.75dBm



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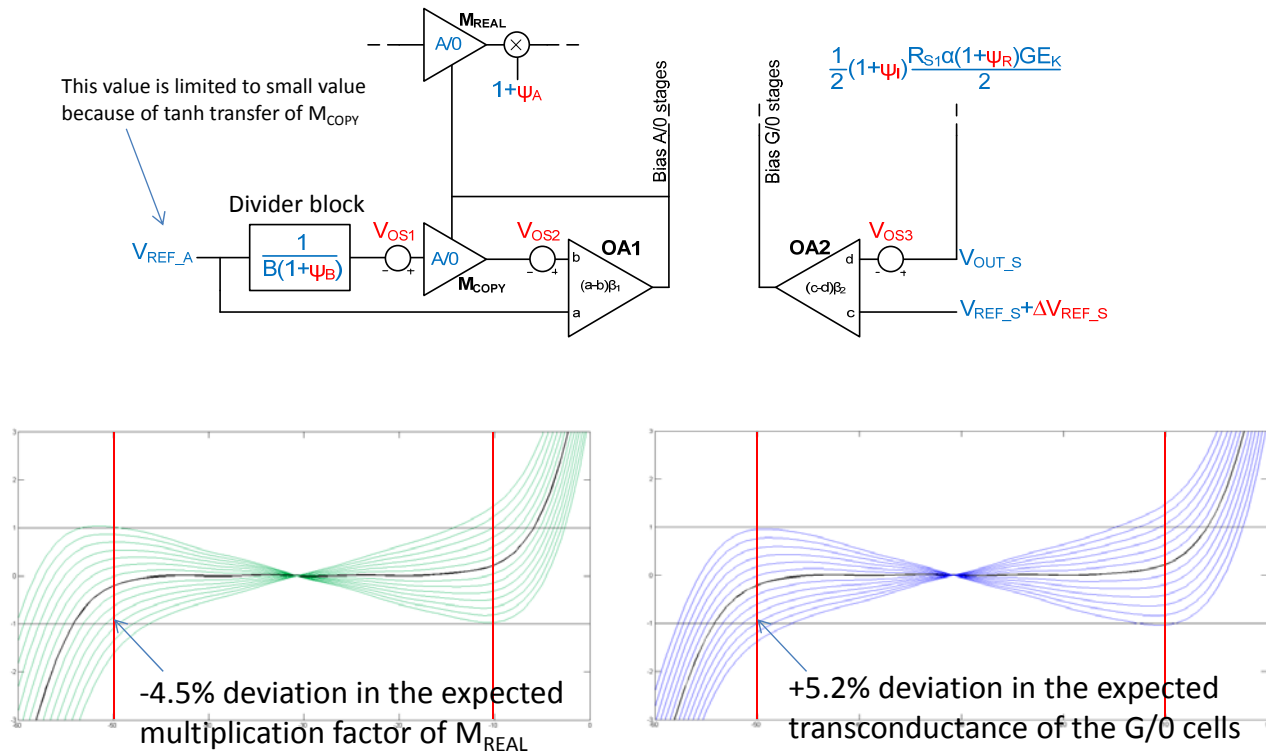
# System simulation results



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# System simulation results



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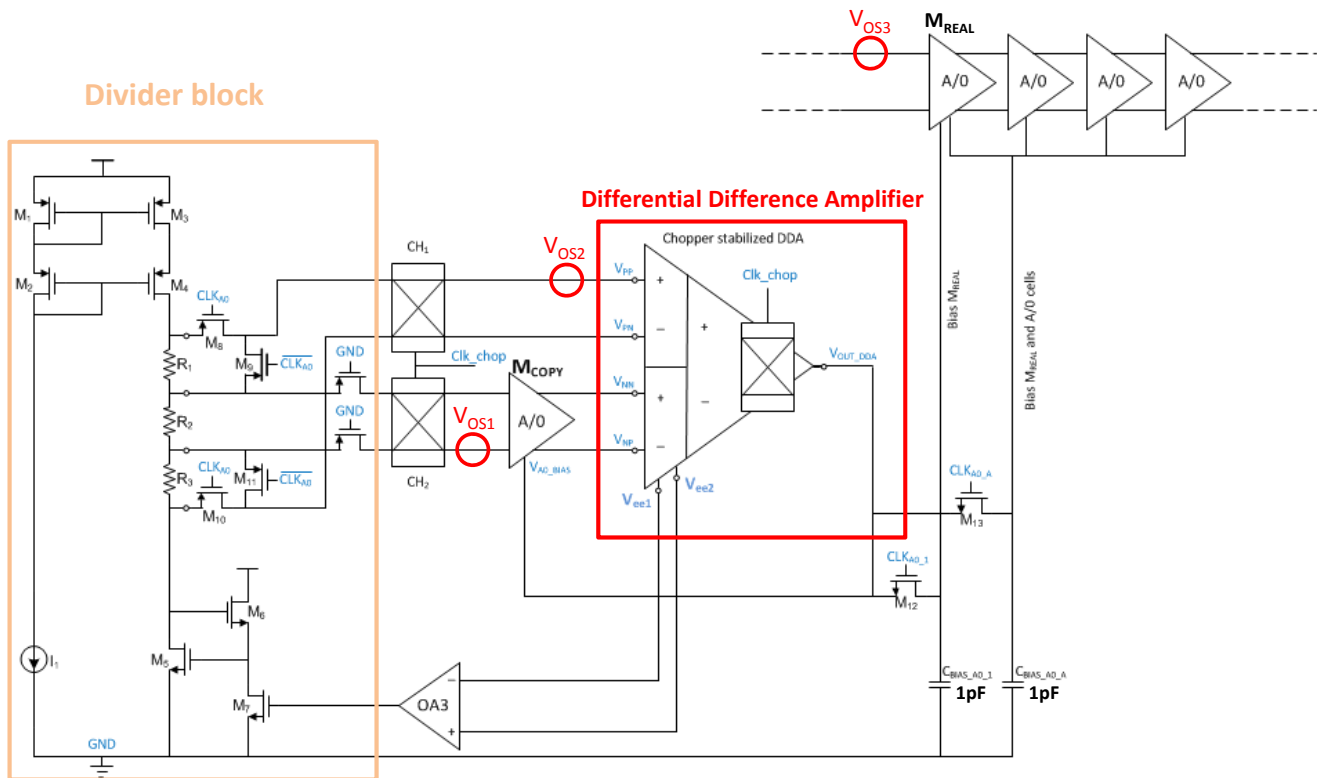
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# Circuit implementation of the gain fixation method

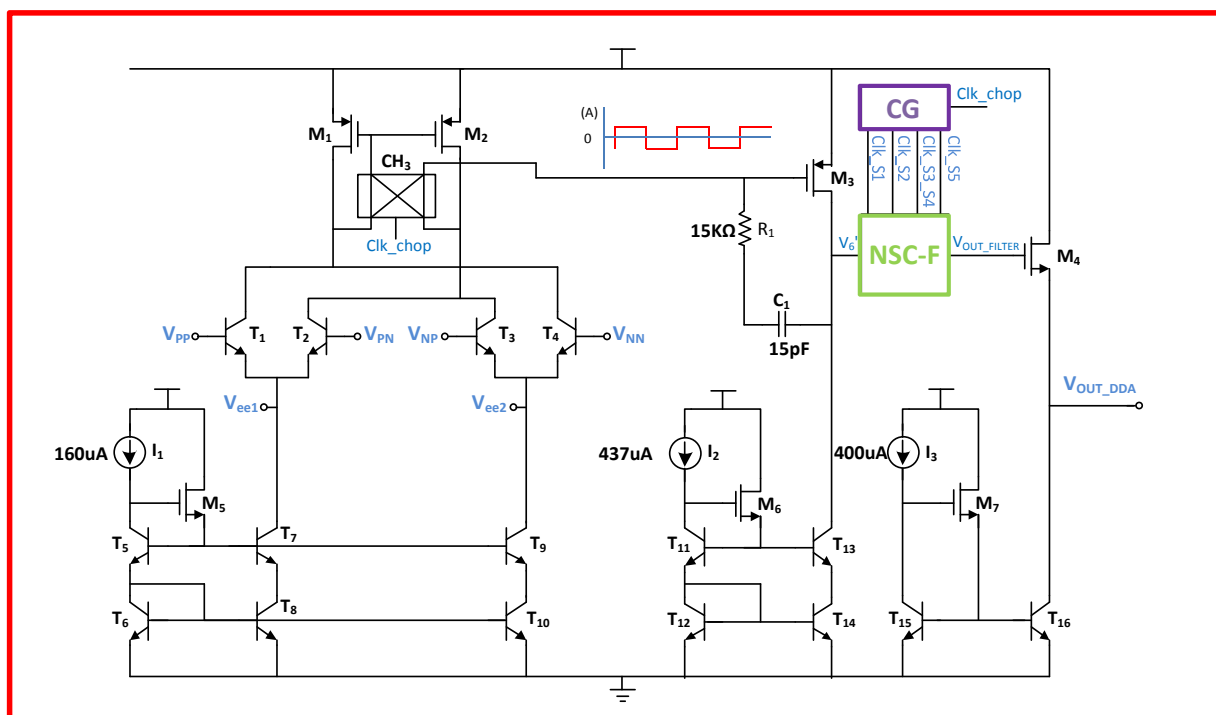


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# Circuit implementation of the gain fixation method

## Differential Difference Amplifier

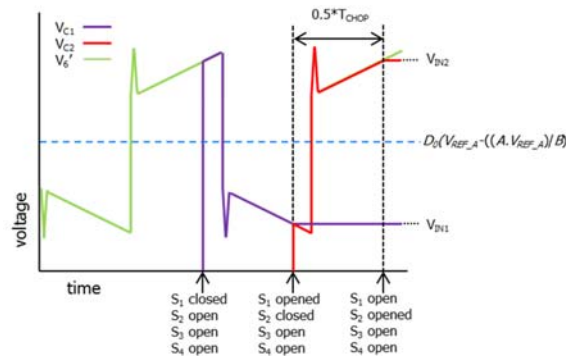
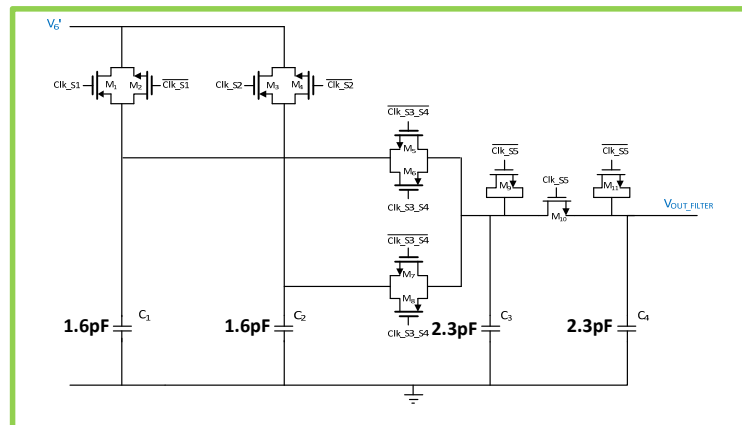


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# Circuit implementation of the gain fixation method

## Notching switched capacitor filter (NSC-F)



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## Contents

### 1. Introduction

- RF power detection
- The Successive Compression Logarithmic Amplifier

### 2. New method for the stabilization of the logarithmic transfer

- Slope fixation
- Intercept fixation
- Dynamic range extension
- Gain fixation

### 3. System simulation results

### 4. Circuit implementation of the gain fixation method

### 5. Circuit simulation results

### 6. Conclusions

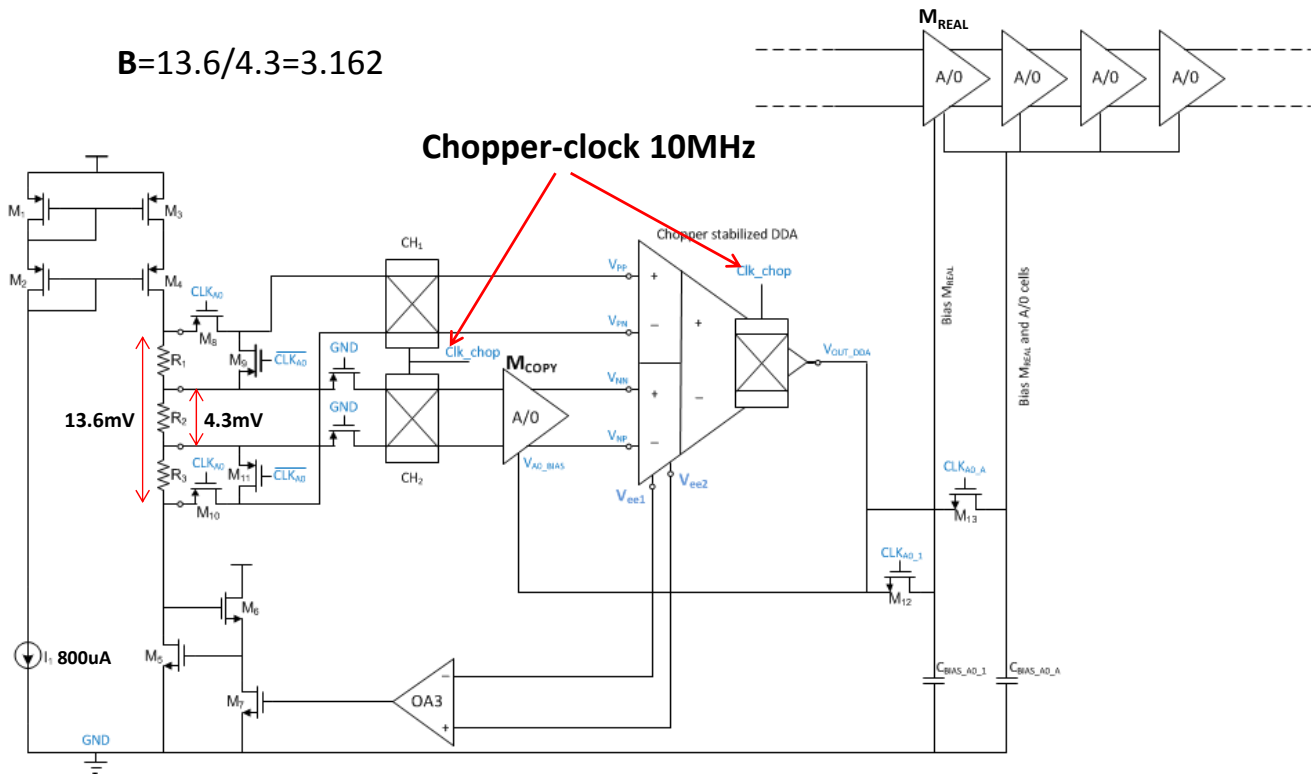
### 7. Questions

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# Simulation results

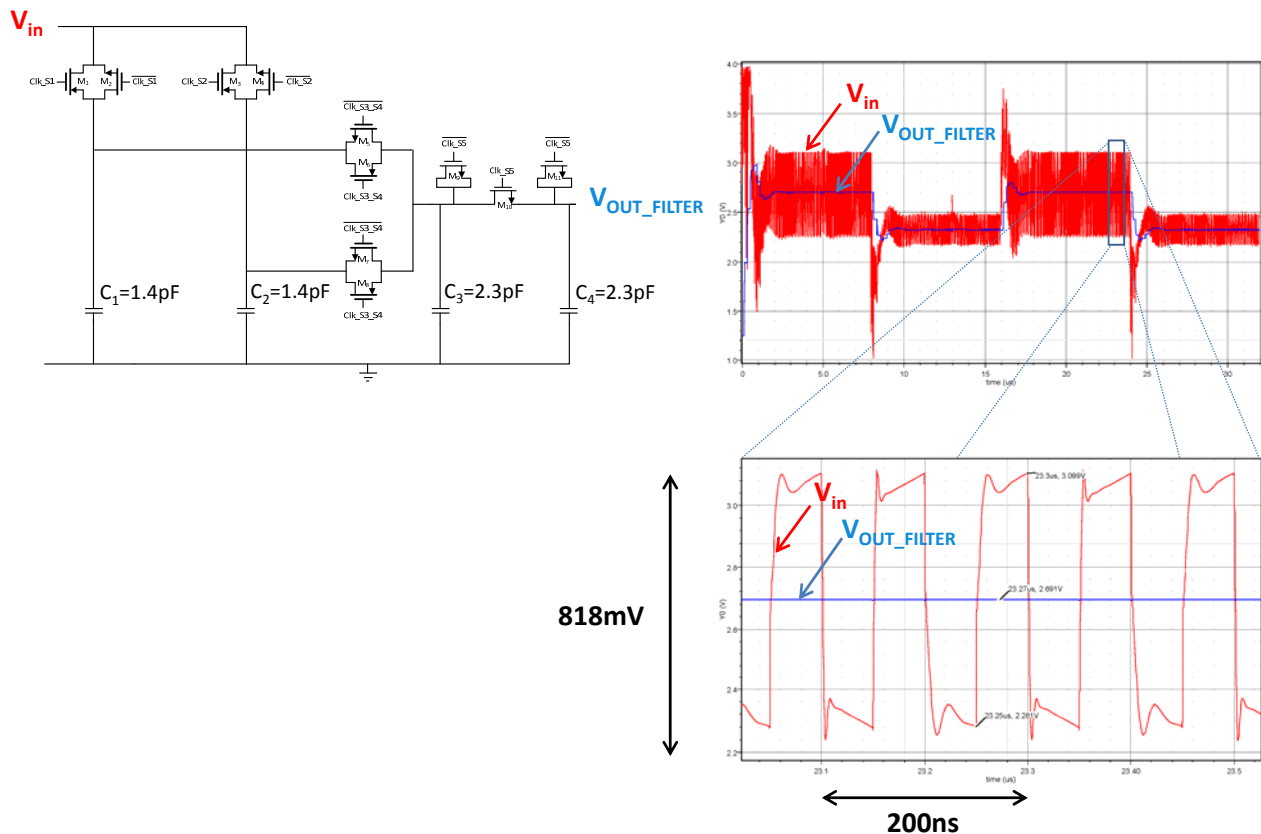
$$B=13.6/4.3=3.162$$



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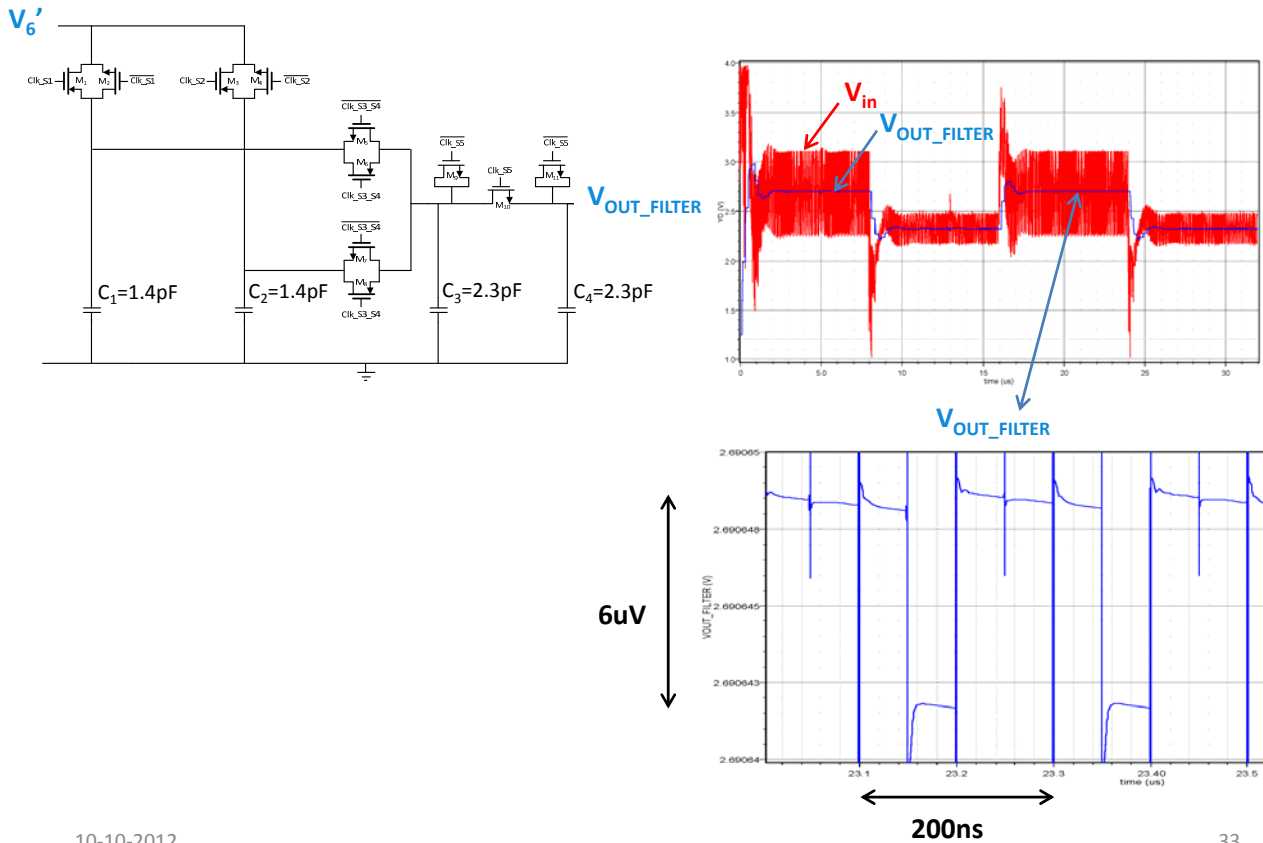
# Simulation results



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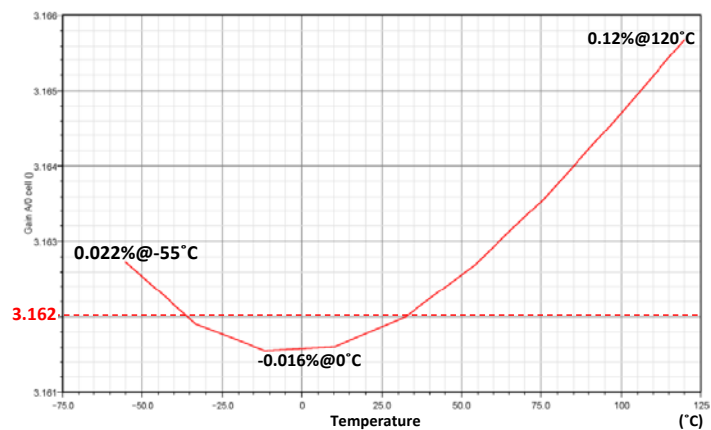
## Simulation results



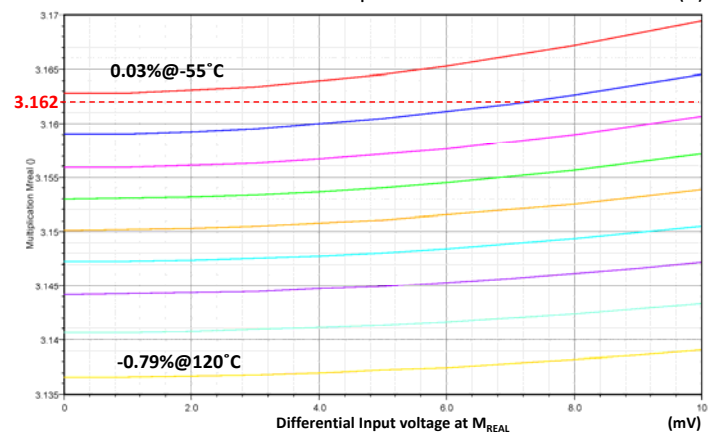
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## Simulation results of the gain fixation method

**Gain**  
A/O stages  
over temperature



**Multiplication**  
stage  $M_{REAL}$   
over temperature

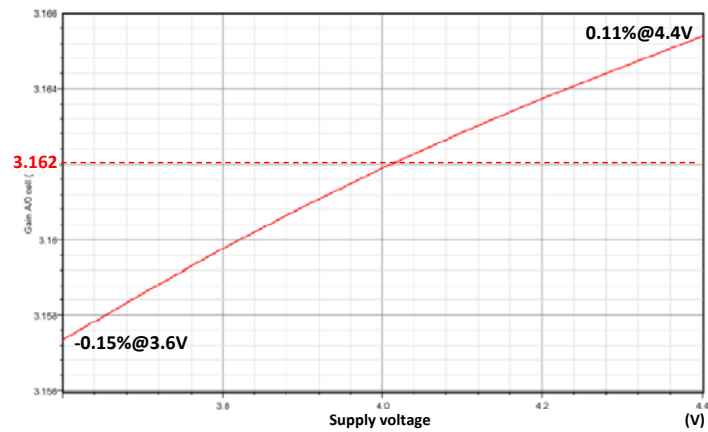


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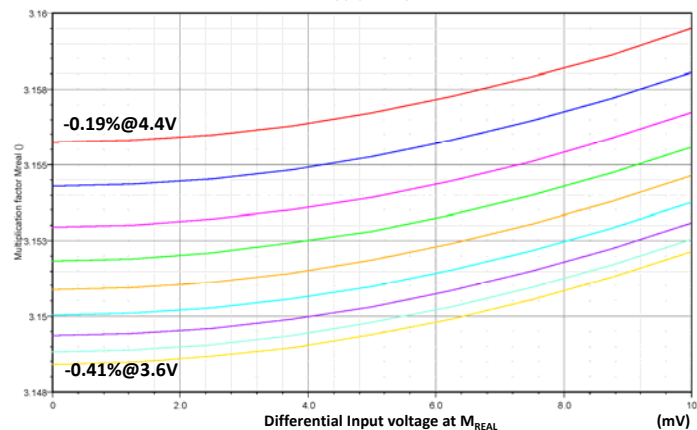
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## Simulation results of the gain fixation method

**Gain**  
A/0 stages  
over supply voltage



**Multiplication**  
stage  $M_{\text{REAL}}$   
over supply voltage

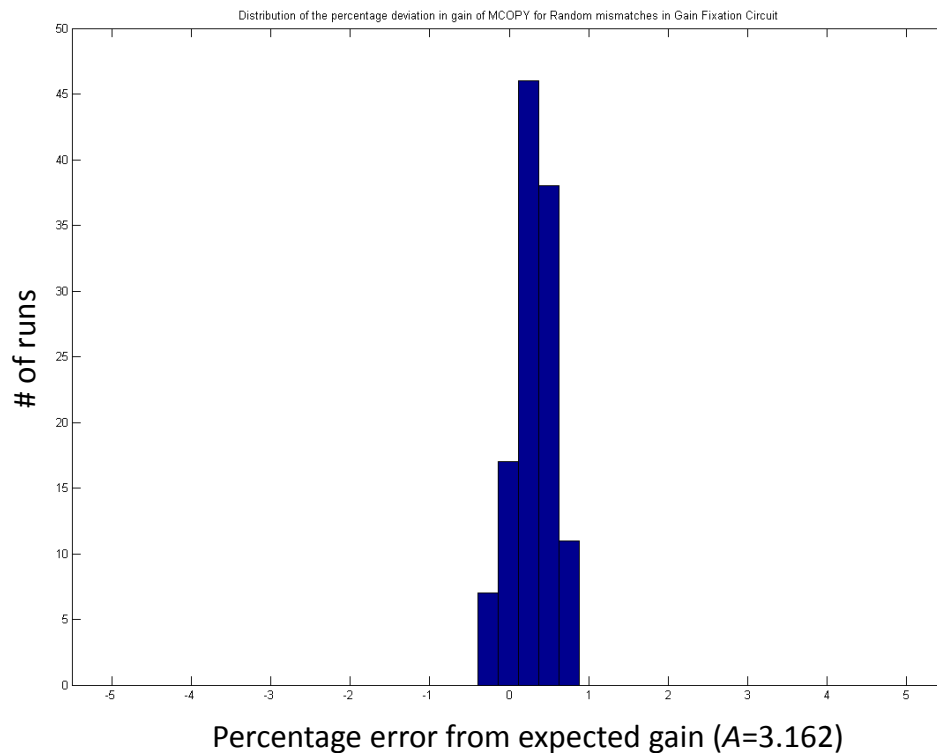


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## Simulation results of the gain fixation method

119runs random mismatches



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- *Slope fixation*
- *Intercept fixation*
- *Dynamic range extension*
- *Gain fixation*

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## 5. Circuit simulation results

## 6. Conclusions

## 7. Questions

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# Conclusions

## New logarithmic Transfer stabilization method

- Intercept fixation

### Original contribution

- Slope fixation
- Dynamic range extension
- Gain fixation
- **Dynamic range fixation**
- Ripple blocking

	Multiplication(<<4.5%)		Gain A/0 cells	
Temperature -55°C till 120°C	+0.03%	-0.79%	-0.016%	+0.12%
Power supply 3.6V till 4.4V	-0.41%	+0.19%	-0.15%	+0.11%

Low offset sensitivity

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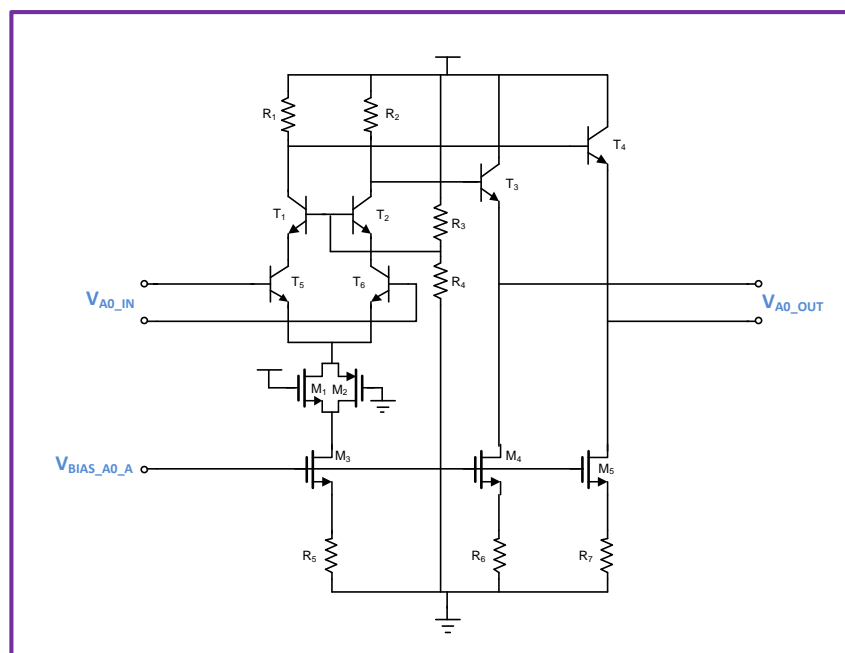


# Questions?

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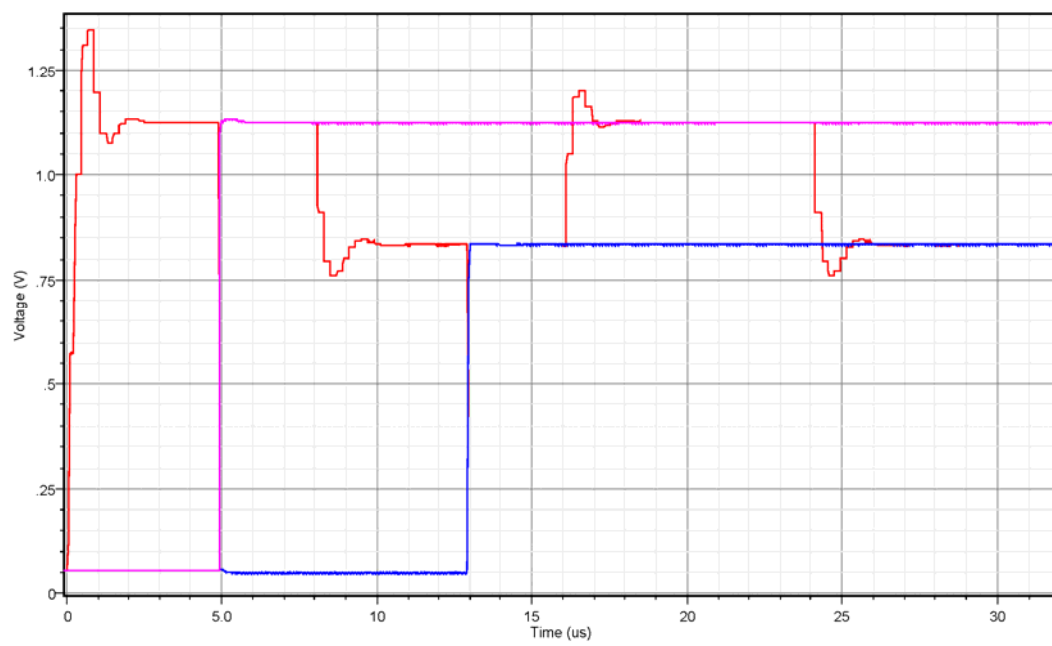
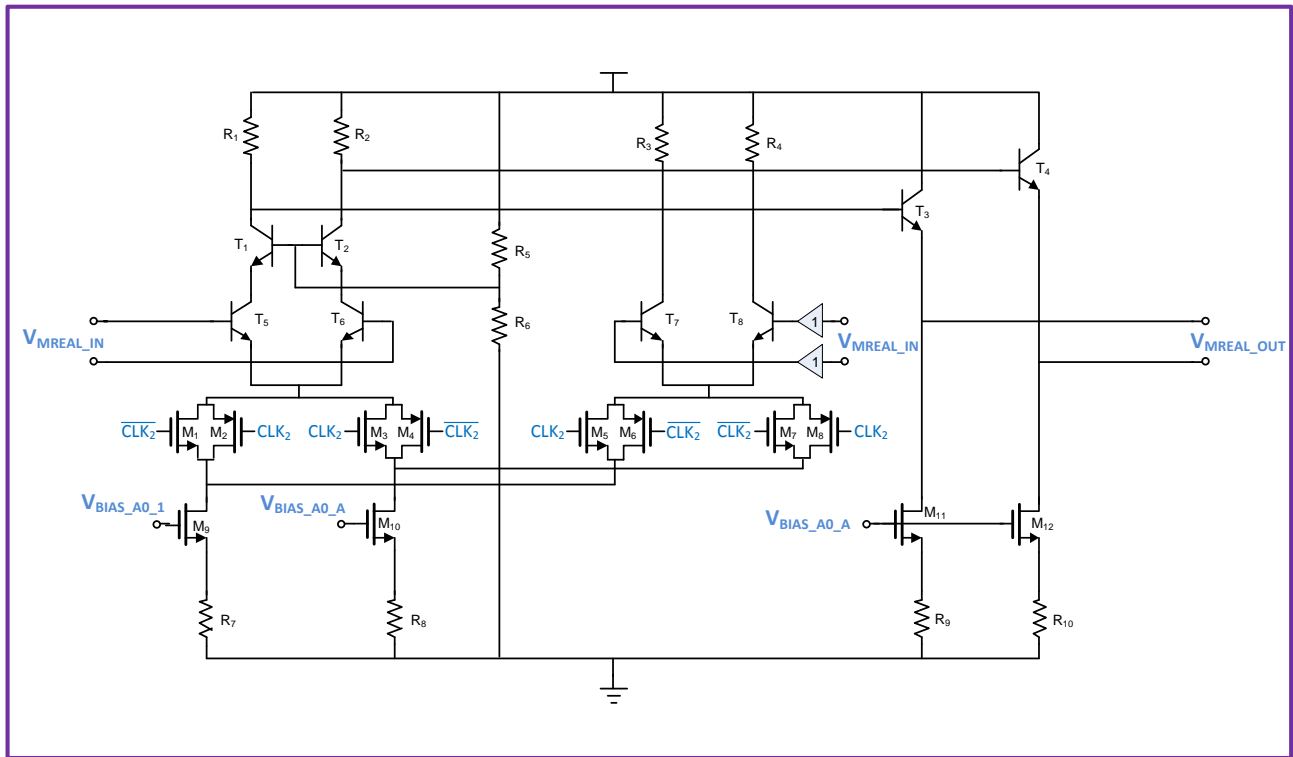
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$M_{COPY}$  (A/O cell)



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Gain obtained by  $M_{\text{REAL}}$

