A power-efficient Delta-Sigma ADC with a passive input stage for audio applications

by

Victor Pecanins Martínez

in partial fulfilment of the requirements for the degree of

Master of Science in Electrical Engineering

at the Department of Electronic Instrumentation,
Faculty of Electrical Engineering, Mathematics and Computer Science
Delft University of Technology

To be defended publicly on Monday, September 26, 2022, at 14:30.

Supervisor:	Prof. Dr. K. A. A. Makinwa	
Thesis Committee:	Prof. Dr. K. A. A. Makinwa,	TU Delft
	Dr. D. G. Muratore,	TU Delft
	Dr. R. H. M. van Veldhoven,	NXP Semiconductors

Summary

The majority of the capabilities in modern chips are implemented in the digital domain. However, physical signals, such as audio, have an analog nature. The conversion from analog to digital domain is accomplished by an Analog to Digital Converter (ADC). Because these circuits need to be used in mass-produced, battery-powered devices, such as mobile phones, they need to be scalable and power-efficient.

Over the last decade, Continuous-Time Delta-Sigma Modulators (CTDSMs) have demonstrated to be a very power-efficient ADC architecture for audio applications. In state-of-the-art designs, the power consumption of the first amplifier (also known as the input stage) dominates the power consumption of the overall ADC. Hence, much research has focused on reducing the power consumption of the input stage.

Recent works propose replacing the integrators of the loop filter with passive RC stages, reducing the number of amplifiers, and saving power. We found that a *fully passive* approach with no amplifiers at all is not scalable to high-resolution audio applications because it places stringent requirements on the comparator. A second approach adding an Operational Transconductance Amplifier (OTA), is still not scalable because it requires either high sampling frequency or high area.

In this thesis, we propose a new circuit using positive feedback around the OTA to overcome the main limitations of previous works. Due to the positive feedback, the capacitor area can be reduced and the loop filter can have complex-conjugated poles, reducing the in-band quantization noise. Furthermore, the new circuit is insensitive to parasitics and preserves the advantages of a passive input stage. Hence, the proposed design is simple to design, scalable, and power efficient.

A prototype chip has been designed and fabricated in 16nm FinFET technology. The measured Dynamic Range (DR) and peak Signal to Noise and Distortion Ratio (SNDR) are 99.46dB and 97.61dB respectively, with a power consumption of 89μW from 0.8V supply. This results in a DR and SNDR Figure of Merit (FOM) of 182.99dB and 181.16 dB respectively, marginally lower than the state of the art, but remarkable due to the simplicity of the circuit.

Acknowledgements

I would like to express my sincere gratitude to my thesis supervisor, professor Kofi Makinwa, who gave me the chance to work on this exciting topic. In key moments, his technical and non-technical advice gave me the perspective I needed to make the right decisions, while also letting me free to try new ideas and learn from them.

I am deeply indebted to my supervisor Robert van Veldhoven from NXP, who came up with the initial idea behind this project. From his technical discussions, I have learned so much about electronics and the job of an engineer. Thank you for teaching me that it is possible to come up with new ideas even with apparently simple things.

Many thanks to the design team at NXP, led by Robert and Vijay, for giving me the opportunity to fabricate a chip in a modern fabrication process and for helping me set up and use the tools. And very especially to Shaun and the layout team, who were able to put together an entire chip from scratch in record time, without their help this project could not have been possible. And thanks to NXP for funding this project.

It was a pleasure to work with the researchers and Ph.D. candidates at the Electronic Instrumentation Laboratory from TU Delft: Efraïm, Sundeep, Zhong, Sining, Shoubhik, Huajun, thanks for the insightful discussions and for reviewing my work providing constructive feedback. Thanks to Lukasz, Ron, and Zu Yao for their help with the PCB and the lab equipment. Special thanks to Shubham Mehrotra for the initial work on which this thesis builds.

I would like to extend my gratitude to my fellow students at TU Delft and my roommate Shreyan for the good times we had during the last 2 years. And a special mention to my family, friends, and Clara for their unconditional support and company despite the distance between Barcelona and Delft.

Contents

List of Figures

List of Tables

Acronyms

AAF Anti-Alias Filter. 9

ADC Analog-to-Digital Converter. 1–3, 7, 18–20, 30, 70

CMRR Common-Mode Rejection Ratio. 53

CT Continuous-Time. v, 3, 7, 9, 14, 15

CTDSM Continuous-Time Delta-Sigma Modulator. v, vii, 3–12, 15, 18, 20, 21, 23, 27, 29–31, 33, 55, 57–59

DAC Digital-to-Analog Converter. v, 7–9, 11, 13–15, 18, 19, 22, 25, 61

DC Direct Current. 36

DEM Dynamic Element Matching. 7

DR Dynamic Range. 6, 13, 49, 57

DSM Delta-Sigma Modulator. 1, 3, 4, 6–13, 15, 16, 21, 24, 25, 28, 32, 44, 49, 51, 53, 55, 59, 60

DT Discrete-Time. v, 7, 9, 10, 13–15

DTDSM Discrete-Time Delta-Sigma Modulator. vi, 3, 4, 7, 66

FFT Fast Fourier Transform. 22

FIR Finite Impulse Response. 61

$\mathbf{FOM_{SNDR}}$ Schreier's Figure of Merit based on SNDR. 2, 3, 6, 18, 19, 23, 60, 74

FS Full-Scale. 12, 15, 31, 60

IIR Infinite Impulse Response. 15

ISI Inter-Symbol Interference. 41, 42

LFSR Linear Feedback Shift Register. 42

MNA Modified Nodal Analysis. 14

MSA Maximum Stable Input Amplitude. 7, 19, 49

NRZ Non-Return to Zero. 7, 14, 15, 41

NTF Noise Transfer Function. 7, 10, 12, 15, 16, 21–23, 25, 27, 28, 51, 57, 58

OBG Out-of-Band Gain. 20

OSR Oversampling Ratio. 6, 7, 15, 20, 23, 25, 26, 57, 58, 60, 69

OTA Operational Transconductance Amplifier. v, 4, 24–29, 32, 34–39, 45, 51, 57–59, 61, 71, 72

PCB Printed Circuit Board. 48, 53

PD Pseudo-Differential. 34, 35

PDSM Passive Delta-Sigma Modulator. 4

PSD Power Spectral Density. 15, 20, 23, 28, 32, 36

PSRR Power Supply Rejection Ratio. 53

PVT Process, Voltage and Temperature. 7

RDAC Resistive DAC. 18

RTZ Return to Zero. 41

SC Switched-Capacitor. 4

SNDR Signal to Noise and Distortion Ratio. 2, 6, 18, 19, 46, 49, 57

SNR Signal to Noise Ratio. 18–20, 46, 49

SQNDR Signal to Quantization Noise and Distortion Ratio. 15, 22

SQNR Signal to Quantization Noise Ratio. 7, 16, 20, 26, 57, 70

STF Signal Transfer Function. 10, 55

THD Total Harmonic Distortion. 16, 19, 46

TRL Tail Resistor Linearized. 35, 49, 53

List of symbols

Symbol	Description	Unit
ω_1, ω_2	Angular frequency of 2nd order loop filter poles	rad/s
ω_0	Natural angular frequency of 2nd order loop filter	rad/s
Q	Quality factor of a 2nd order loop filter	-
ω_z	Angular frequency of a loop filter zero	rad/s
$H_{DAC}(s)$	Laplace transform from V_{DAC} to V_Y	-
$H_{IN}(s)$	Laplace transform from V_{IN} to V_Y	-
$H_{DAC}(z)$	DT equivalent of $H_{DAC}(s)$ assuming NRZ DAC	-
$H_{IN}(z)$	DT equivalent of $H_{IN}(s)$	-
k	Boltzmann's constant = 1.38×10^{-23}	$\mathrm{J/K^{-1}}$
T	Absolute temperature. Unless specified: T=300K	K
f_s	Sampling frequency = $1/T_s$	Hz
f_{BW}	Signal bandwidth	Hz
R_{IN}	Input resistor of a CTDSM with RDAC	Ω
R_{DAC}	Feedback resistor of a CTDSM with RDAC	Ω
R_P	Input node parallel resistance: $R_\mathrm{P} = (R_\mathrm{IN} \| \| R_\mathrm{DAC})$	Ω
g_m	Transconductance of a transistor	Ω^{-1}
G_m	Transconductance of an OTA	Ω^{-1}
OSR	Oversampling Ratio = $f_s/(2f_{BW})$	-

Chapter 1

Introduction

In modern integrated circuits, analog signal processing capabilities are being replaced by digital equivalents. The advantage of digital circuits is their ability to be easily ported across technology nodes, enabling design reuse, speeding up development and verification steps, and shortening the time to market. However, some key applications are inherently analog, for example, audio, radio, communication, and sensors. Analog signals must first be converted to the digital domain by an Analog to Digital Converter (ADC), which is typically integrated on the same chip next to the digital core.

Over the last years, much research has been done on new ADC architectures that are easily portable across technology nodes in the same way as digital circuits do, thus allowing mixed-signal integrated circuits to take full advantage of Moore's law. One of these research trends is to use a Delta-Sigma Modulator (DSM) with at least one passive integrator in the loop filter [1].

The goal of this thesis is to answer the question: Can a DSM with a partly passive loop filter be better than conventional designs based on active loop filters? To define what is *better*, we focus on the quality indicators shown in Table 1.1. As usual in engineering, ADC design is a trade-off between performance and cost. To ensure the final system is useful in real-world applications, we introduce another quality metric, *usability*.

The performance of an ADC is quantified by resolution, bandwidth, and power consumption. Resolution and bandwidth are usually very well-defined by the application. Power consumption should be as low as possible, especially in battery-operated devices. Due to the laws of physics, there is a fundamental limit on the minimum power required to reach a certain resolution and bandwidth. State-of-the-art circuits try to approach this fundamental limit.

Table 1.1: ADC quality indicators addressed in this work

Performance	Cost		Usability
	Production	Development	
Resolution	Silicon area	Complexity	Easy to drive
Bandwidth	Calibration	Portability	Interference
Power	Yield	Scalability	PVT variations

The costs of a system can be split in two: Production costs are incurred for each unit of the chip produced, and development costs are incurred only once. The most important contributors to production costs are silicon area, calibration, and yield, while the most important contributors to development costs are complexity, lack of portability, and lack of scalability. A complex design, with many sub-circuits that need to be designed and verified by several experts, is generally more costly than a simpler design. Having a design that can be easily ported between technologies also reduces cost, because it allows design reuse. For this same reason, a design should also be scalable: The same structure should be capable of fulfilling different specifications by just changing the values of some components.

The third quality indicator is usability. During the design process, decisions are made to optimize the relationship between performance and cost. We introduce the term usability to qualify the effect of such decisions when a chip is used in a real-world scenario. This is important when the chip has to be used in a commercial product, not only in a research experiment. For example, it is not desirable that an ADC is designed for having a very good performance but needs a very power-hungry amplifier to drive its input.

1.1 Motivation

The power efficiency of an ADC can be quantified by the Schreier's Figure of Merit based on SNDR ($\mathrm{FOM_{SNDR}}$) that combines bandwidth (f_{BW} in Hz), power consumption (P_{supply} in W), and resolution (SNDR in dB) in a single number:

$$\mathrm{FOM_{SNDR}\,(dB)} = \mathrm{SNDR\,(dB)} + 10\log_{10}\frac{f_{BW}}{P_{supply}} \tag{1.1}$$

where Signal to Noise and Distortion Ratio (SNDR) is defined as

$$\mathrm{SNDR\,(dB)} = 10\log_{10}\frac{P_{signal}}{P_{noise}+P_{distortion}} \tag{1.2}$$

To study the behavior of FOM_{SNDR} for different designs, a survey of ADC papers published in *IEEE Journal of Solid-State Circuits* (JSSC) and *Journal of VLSI Circuits and Systems* is shown in Figure 1.1 [2]. Signal bandwidth (f_{BW}) is shown on the x axis and FOM_{SNDR} on the y axis. Below $f_{BW} = 30\text{MHz}$, power consumption is dominated by the analog constraints on thermal noise, and the maximum achievable FOM_{SNDR} at the time of writing this thesis is about 183-184dB. Because power consumption and thermal noise are inversely proportional, the maximum FOM_{SNDR} stays almost constant. The maximum theoretically achievable FOM_{SNDR} at room temperature is around 192dB, although a more realistic maximum would be about 186dB [3]. Above $f_{BW} = 30\text{MHz}$ the power consumption of the circuits that do not directly reduce the thermal noise (such as digital parts, clock, and parasitic losses) becomes dominant and FOM_{SNDR} decreases rapidly as bandwidth increases.

As shown in Figure 1.1, Continuous-Time Delta-Sigma Modulators (CTDSMs) can be designed for a wide range of bandwidths while also achieving good power efficiency. Moreover, their CT input stage offers some usability and scalability advantages with respect to their DTDSM counterparts, such as implicit alias rejection, being easier to drive, and able to operate at higher speeds [4].

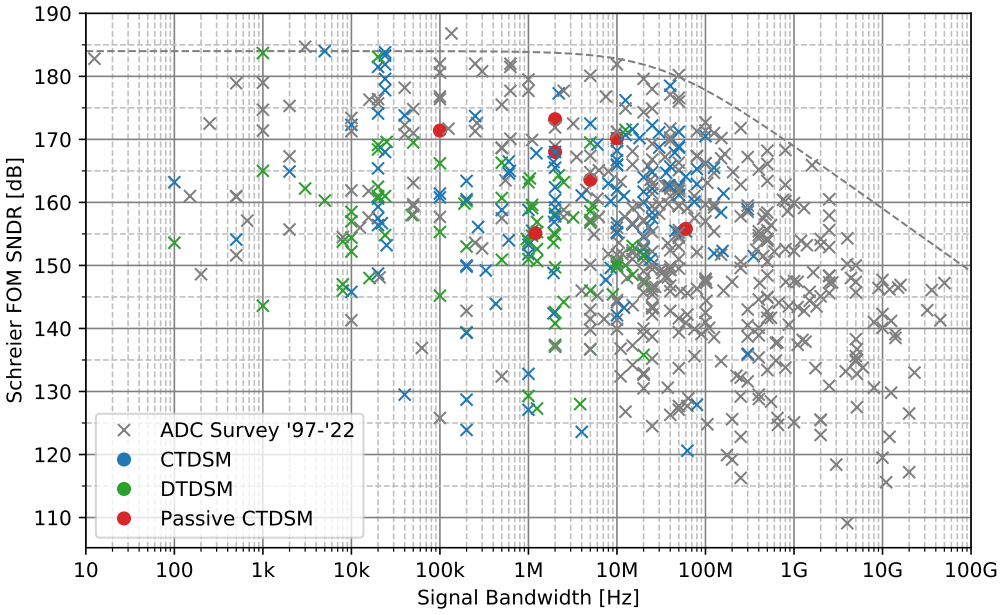


Figure 1.1: Survey of ADCs and CTDSMs with a passive input stage

In the best possible case, the power consumption of a DSM is dominated by the first amplifier of the loop filter, also known as the input stage, because the errors of further stages are suppressed by the gain of the first stage. The noise and nonlinearity of the input stage are critical for the performance of the DSM, therefore most power consumption is allocated to this amplifier. The idea behind passive (or semi-passive)

DSMs is to reduce the number of amplifiers in the loop filter, potentially saving power. Because it is the input stage that dominates the power consumption, it is interesting to replace this with a passive stage. Therefore, this thesis focuses on CTDSMs with a passive input stage.

In some discussions, the term *Passive Delta-Sigma Modulator (PDSM)* is used. From the ongoing argument, we conclude that the biggest advantage may be reached when the input stage is passive. So it should be understood that the term PDSM does not refer only to fully-passive DSMs, but to all DSMs where at least the input stage is passive. Although DSMs with a conventional input stage followed by passive stages (which should not be considered PDSMs) have been described, the power efficiency advantage is not huge [5, 6].

1.2 Previous work

A second-order CTDSM with a fully passive loop filter for audio applications was proposed as early as 1984 (Figure 1.2a). The authors noted that in the absence of amplifiers, the modulator's loop gain must be provided by the equivalent gain of a 1-bit quantizer [7, 8]. Another early work from 1997 proposes a DTDSM in which the loop gain is partly provided by a Switched-Capacitor (SC) network, to alleviate the noise requirements of the comparator [9]. The authors also propose a method to approximate the quantizer gain based on the frequency response of the loop filter.

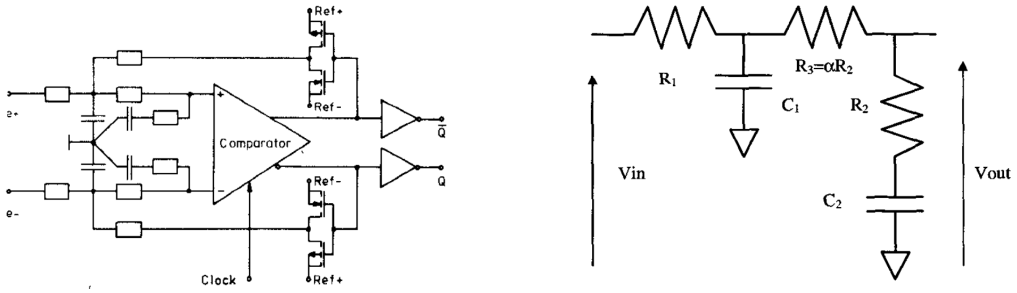
In an example of a fully passive CTDSM from 2002 (Figure 1.2b) [10, 11], the authors proposed the method of impulse invariance to analyze a CTDSM without making any assumption, based solely on the loop filter's Laplace transform. They focused on DC behavior, noticing the appearance of dead zones due to the finite DC gain of passive RC circuits, and added dithering to the comparator to mitigate this effect.

In 2010, a 1.2 MHz BW CTDSM was proposed [12]. This design has a passive RC input stage followed by an active G_m stage. The authors recognized that the low-pass filtering of the passive stage reduces the OTA input swing, allowing it to be designed for low power consumption. The gain provided by the G_m stage alleviates the noise requirements of the comparator. A similar design was proposed in [13].

A third-order CTDSM for Bluetooth applications with a passive input stage and simple differential pairs approached state-of-the-art power efficiency in 2016 (Figure 1.3) [14, 15]. The authors draw from circuits proposed in prior papers and a genetic algorithm optimization of the values of the components. A CT 2-1 MASH with capacitive DAC also approached the state-of-the-art [16]. A slightly different

input stage was used in [17, 18] also reached good results. Recently a passive input stage CTDSM with an FIR DAC has been published (Figure 1.4) [19].

A selection of passive input stage CTDSMs published after 2010 are shown in circles in Figure 1.1, and an overview of the specifications is given in Table 1.2. We observe that passive input stage CTDSMs can be constructed for a wide range of bandwidths (0.1 to 60 MHz). However, their FOM has never exceeded 180dB.



(a) Fully passive CTDSM [7, 8] (b) Single-ended loop filter [10, 11]

Figure 1.2: Prior Fully Passive CTDSMs

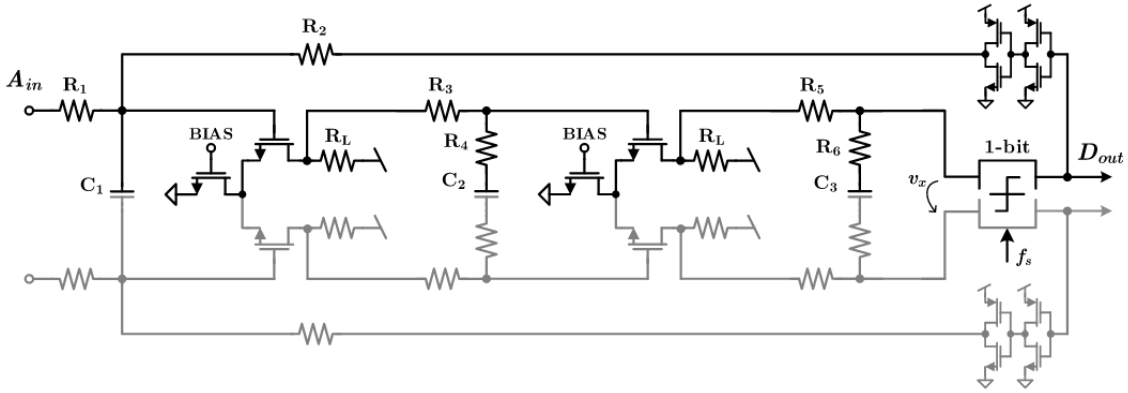


Figure 1.3: 3rd order RC-OTA CTDSM [14, 15]

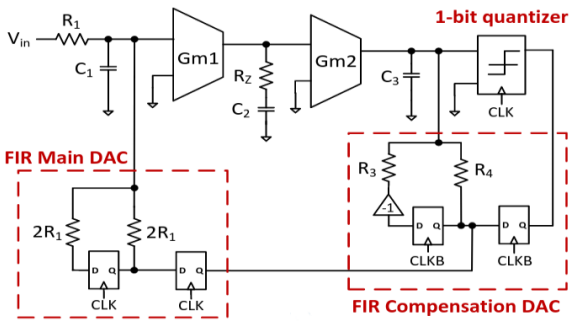


Figure 1.4: 3rd order RC-OTA CTDSM with FIRDAC [19]

Table 1.2: Previously published CTDSMs with a passive-RC input stage

	Bala-chandran 2010 [12]	Srini-vasan 2012 [13]	Melo 2015 [15]	Nowacki 2016 [16]	Li 2017 [17]	Li 2018 [18]	Mukherjee 2020 [19]
Process [nm]	65	45	65	65	180	180	40
Supply [V]	1.4	1.8/1.4	0.7	1	1.8	1.8	1.2
Power [mW]	1.16	20	0.256	1.57	0.124	0.059	0.79
BW [MHz]	1.2	60	2	10	2	0.1	5
f_s [MHz]	300	6000	320	1000	256	25.6	1024
OSR	125	50	80	50	64	128	102.4
Order	2	3	3	3	3	3	3
SNDR	65	61	69.1	72.2	71.1	79.1	65.6
DR	69	75	76.2	77	71.3	82.2	67.3
Area [mm^2]	0.1875	0.49	0.013	0.027	-	0.059	0.034
FoM_{SNDR} [dB]	155.2	155.7	168	170.2	173.1	171.4	163.6
FoM_{DR} [dB]	159.1	169.7	175.1	175	173.2	174.5	165.3

1.3 Thesis organization

This thesis describes the design of a power-efficient ADC for audio specifications: f_{BW} = 20kHz, peak SNDR = 100dB and FOM_{SNDR} > 180dB. The goal is to investigate if a passive input stage CTDSM can be designed for high-resolution and a power efficiency FOM exceeding 180dB, which has not been found in the published literature.

The remainder of this thesis is organized as follows. Chapter 2 reviews the possible architectural choices for a DSM, comparing the alternatives and justifying the choice of a 2nd order, 1-bit CTDSM with a passive input stage. A brief theoretical background introduces the notation and key concepts used in this thesis: Quantization noise, thermal noise, distortion, and power efficiency. Chapter 3 contains an in-depth analysis of two previously known loop-filter circuits with a passive input stage (Fully Passive and Passive RC-OTA) in terms of quantization noise, thermal noise, and power efficiency. A new loop filter topology (Single-OTA Resonator) is proposed to overcome the limitations of the prior art. Chapter 4 describes the circuit implementation of a practical CTDSM in 16nm FinFET technology, to validate the proposed Single-OTA Resonator topology. Chapter 5 shows the measured performance of the prototype chip and discusses the results. Chapter 6 concludes this thesis and presents future research directions.

Chapter 2

Theoretical background

There are many architectural choices in the design of DSM ADCs. An outline is presented in Table 2.1. To narrow the scope of this thesis, some of the choices made in this work were based on the published literature.

The first decision concerns the nature of the loop filter. As we have seen in Figure 1.1 CTDSMs are able to operate at higher frequencies than DTDSMs, offer intrinsic anti-aliasing, and are easier to drive [4]. However, CTDSMs may be harder to design because modeling requires transforming between CT and DT (section 2.1). In a CTDSM the NTF is more affected by PVT variations than in a DTDSM, where the NTF depends only on capacitor ratios. This can be solved by making the CTDSM components adjustable.

The next decision concerns the number of levels of the quantizer and the DAC. Although it might be tempting to choose more than 2 levels due to the increased Maximum Stable Input Amplitude (MSA) and improved SQNR without increased OSR, it complicates the design. It is well-known that multi-bit quantizers typically require Dynamic Element Matching (DEM) or calibration to overcome DAC element mismatch. Unfortunately, this requires extra digital logic and makes the current drawn from V_{REF} data-dependant [20]. Furthermore, the loop filter gain must be controlled, whereas 1-bit quantizers are insensitive to loop filter gain. Because this project is focused on proving the concept of semi-passive loop filters, and development time is limited, we decided on the simplest quantizer: 1-bit.

Following the same reasoning, we choose the simplest DAC, a resistive, Non-Return to Zero (NRZ) DAC, as well as a 2^{nd} order loop filter because this is the lowest order that is practically usable without compromising performance. Hence, the remainder of this thesis is focused on the analysis and design of 2^{nd} order, 1-bit CTDSMs with an NRZ, resistive DAC.

Table 2.1: Architectural choices for Delta-Sigma Modulators

Architectural choice	Advantages	Drawbacks
Loop filter type		
Discrete Time (DT)	Easy to analyze Robust to PVT	Hard to drive linearly Speed limited by settling
Continuous Time (CT)	Easy to drive linearly Can work at higher speed	Difficult to analyze Sensitive to PVT
Number of quantizer levels		
2 levels (1-bit)	Does not require DEM Insensitive to DC loop gain	Quantizer gain varies More intrinsic distortion
More than 2 levels (N-bit)	Quantizer gain constant Less intrinsic distortion	Requires DEM or calibration Sensitive to DC loop gain
DAC type		
Resistive (RDAC)	Simple to design No 1/f noise	Higher input-referred OTA noise
Current steering (IDAC)	Lower input-referred OTA noise	Not simple to design 1/f noise must be canceled
Capacitive (CDAC)	Robust to jitter and ISI [21]	Worse alias rejection [22]
DAC pulse shape		
Return to zero (RTZ)	Free from ISI	Worse jitter sensitivity
Non-return to zero (NRZ)	Better jitter rejection	Affected by ISI
Order of noise-shaping		
1st-order	Always stable	Tonal behavior
2nd-order	Easy to make stable	High OSR required
Higher order	Possibly lower OSR	Easy to make unstable

2.1 Basic CTDSM

In the standard approach to analyzing DSMs, the loop filter is composed of ideal integrators connected by scaling coefficients [23]. However, in this work integrators are very non-ideal and loading effects between stages are important. Therefore, we avoid the concept of ideal integrators and analyze the CTDSM using only the Laplace transform of the loop filter.

A CTDSM consists of a continuous-time filter, a clocked quantizer, and a DAC in a negative feedback loop (Figure 2.1). The loop filter has two inputs V_{IN}, V_{DAC} with respective transfer functions $H_{IN}(s)$, $H_{DAC}(s)$ to the output V_Y. The output

of the CT loop filter is sampled at a frequency $f_s = 1/T_s$ and quantized between N levels. In our case, the quantizer only has N=2 levels, typically implemented with a clocked comparator. The resulting bitstream D_{OUT} is converted back to CT by a DAC and fed back to the input of the loop filter.

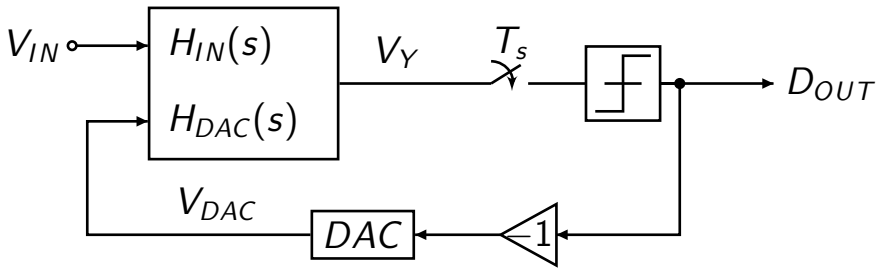


Figure 2.1: Block diagram of a CTDSM

Under certain conditions, the bitstream D_{OUT} can be digitally processed to recover the original signal V_{IN}. To see how the system must be analyzed in discrete time [24]. Firstly, the dual-input loop filter from Figure 2.1 may be regarded as two single-input systems with a summation node at their output. Pushing the summation node to the right of the sampler, and replacing the quantizer with a gain κ and additive error E_Q (section 2.2.1) we arrive at the equivalent model shown in Figure 2.2.

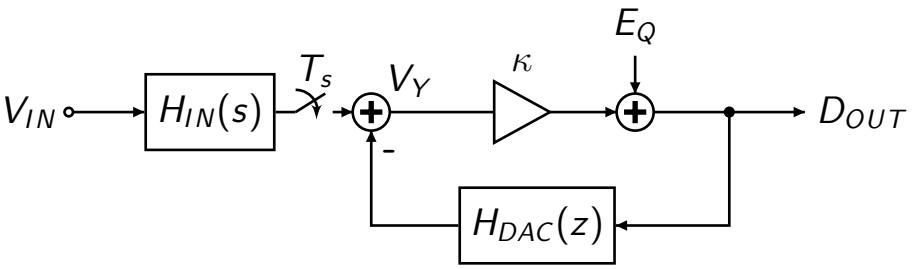


Figure 2.2: Mixed CT and DT model of a CTDSM

As shown in Figure 2.2, the input signal is filtered by $H_{IN}(s)$, typically a low-pass filter, before being sampled, acting as an implicit Anti-Alias Filter (AAF). For inband signals ($f << f_s/2$) there is no aliasing, and the filter $H_{IN}(s)$ can be moved after the sampler and replaced by its DT equivalent $H_{IN}(z)$. We obtain the fully DT approximation from Figure 2.3, which acts on the sampled input $V_{IN}[n] = V_{IN}(nT_s)$.

The conversion from $H_{IN}(s)$ to $H_{IN}(z)$ can be done by the impulse invariant method, which produces a DT system whose output coincides with that of the CT system at the sampling moments, which is what matters for a DSM loop.

$$H_{IN}(z) = \mathcal{Z}_{T_s}\left\{\mathcal{L}^{-1}\left[H_{IN}(s)\right]\right\} \tag{2.1}$$

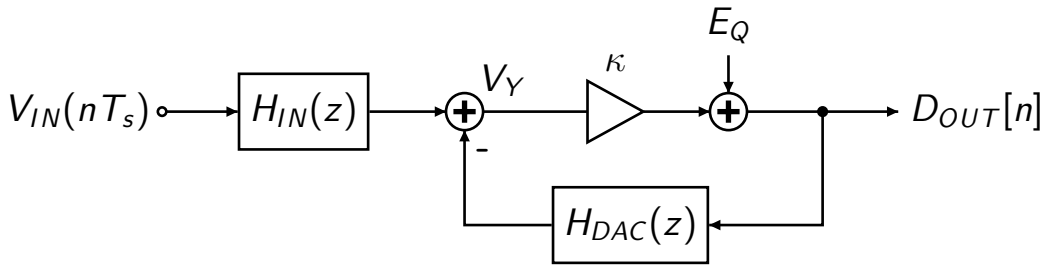


Figure 2.3: DT equivalent of a CTDSM assuming no aliasing

Similarly, $H_{DAC}(z)$ can be obtained by the impulse invariant method from $H_{DAC}(s)$ convolved with the impulse response of the DAC. For a NRZ DAC with impulse response $H_{NRZ}(s) = (1 - e^{-sT_s})/s$ [10]:

$$H_{DAC}(z) = (1 - z^{-1})\mathcal{Z}_{T_s}\left\{\mathcal{L}^{-1}\left[\frac{H_{DAC}(s)}{s}\right]\right\} \tag{2.2}$$

By analyzing the linear model, the resulting bitstream D_{OUT} contains the input signal V_{IN} and the quantization noise E_Q, respectively shaped by the Signal Transfer Function (STF) and the Noise Transfer Function (NTF):

$$D_{OUT} = V_{IN}\underbrace{\frac{\kappa H_{IN}(z)}{1 + \kappa H_{DAC}(z)}}_{STF} + E_Q\underbrace{\frac{1}{1 + \kappa H_{DAC}(z)}}_{NTF} \tag{2.3}$$

Assuming the loop filter $\kappa H_{DAC}(z)$ is a low-pass filter, the NTF is a high-pass filter that removes the in-band quantization noise, pushing it to the high frequencies, where it can be removed by a digital decimation filter. This requires that the poles from the loop filter are close to DC, to discriminate between signal and quantization noise and that the OSR is large enough to allow the spreading of the quantization noise to high frequencies.

Several observations can be made:

1. The poles p_i of $H_{DAC}(z)$ are related one-to-one with the poles ω_i of $H_{DAC}(s)$ by the expression $p_i = e^{j\omega_i T_s}$.
2. The zeros of NTF are the same as the poles p_i of $H_{DAC}(z)$.
3. The zeros z_i of $H_{DAC}(z)$ are **not** as easily derived, and depend on the poles and zeros of $H_{DAC}(s)$, the sampling frequency, and the shape of the DAC pulse.
4. The poles of the NTF depend on the poles p_i and zeros z_i of $H_{DAC}(z)$, and the quantizer gain κ.
5. The stability of the closed-loop DSM depends on the poles of the NTF.

2.2 Active and passive CTDSMs

Passive (or partly passive) DSMs are characterized by a low DC-gain loop filter and high-leakage integrators. Although these concepts also play a role in active DSMs, they are often overlooked so they will be reviewed in this section.

The lack of gain in the loop filter can be compensated by a high quantizer gain, which recovers the total loop gain needed to keep the DSM stable. If the quantizer only has 2 levels, its gain is adjusted automatically, resulting in a circuit that is insensitive to the loop filter DC gain.

Integrator leakage leads to increased quantization noise and non-linear effects due to dead zones. These can be mitigated by placing the poles of the loop filter close to DC, or alternatively by adding dithering at the input of the comparator.

2.2.1 Quantizer gain

The gain of a 2-level quantizer cannot be calculated from its input-output curve, because any slope would fit equally well. The equivalent gain of the quantizer is defined as:

$$\kappa = \frac{D_{\mathrm{OUT,rms}}}{V_{\mathrm{Y,rms}}} \tag{2.4}$$

Since the output of a 2-level quantizer D_{OUT} is either +1 or -1, $D_{\mathrm{OUT,rms}} = 1$. Thus, the gain of the quantizer is the inverse of its input voltage swing [9, 15].

If the input to the DSM is zero, the input to the quantizer is only coming from the DAC filtered by the loop filter. In this case, the comparator gain is fully determined by knowing $H(s)$ and f_s. There are two ways to estimate the quantizer gain:

1. Criterion of oscillation. With zero input, the CTDSM oscillates at $f_s/4$. Based on Barkhausen's oscillation criterion, the loop gain at that frequency must be 1. So, the quantizer gain κ is equal to the inverse of the loop filter gain at the oscillation frequency [9, 15]:

$$\kappa \approx |H_{DAC}(s = 2\pi j\ f_s/4)|^{-1} \tag{2.5}$$

   Based on the loop filter gain A_0, loop filter zero ω_z, and poles ω_1, ω_2, we can estimate the quantizer gain within one order of magnitude with the expression:

$$\kappa \approx \frac{2\pi \frac{f_s}{4} \omega_z}{A_0 \omega_1 \omega_2} \tag{2.6}$$

2. Criterion of total output power. The power at the output of a 2-level CTDSM is equal to 1. With zero input, this power comes entirely from the integrated power of the NTF [25]. Therefore, the quantizer gain κ is such that

$$\int_{-\pi}^{\pi} \frac{1}{|1 + \kappa H_{DAC}(z = e^{j\Omega})|^2} d\Omega = 1 \tag{2.7}$$

Although this criterion might provide a better estimation for the gain, the integral equation is difficult to solve so it is rarely used in practice.

The presented estimations of the quantizer gain hold only if the input of the DSM is zero. However, for nonzero input signals, the quantizer gain is reduced. This is illustrated in Figure 2.4. First, we recall that the signal V_Y at the input of the quantizer originates from the difference between the input to the DSM and the bitstream $(V_{IN} - D_{OUT})$ filtered through the loop filter, which is essentially a lowpass filter. For large input signals close to Full-Scale (FS), the bitstream will have long runs of same-sign outputs. These long runs are equivalent to low-frequency signals, which will be accentuated by the loop filter. Hence, the signal at the input of the quantizer has a higher swing, and since the power at the output of the quantizer is constant, the gain of the quantizer is reduced. This causes the poles of the NTF to depend on the input amplitude, a nonlinear effect that causes quantization noise to be correlated with the input amplitude, appearing as harmonic distortion. Because this distortion appears even with ideal components, we call it intrinsic distortion.

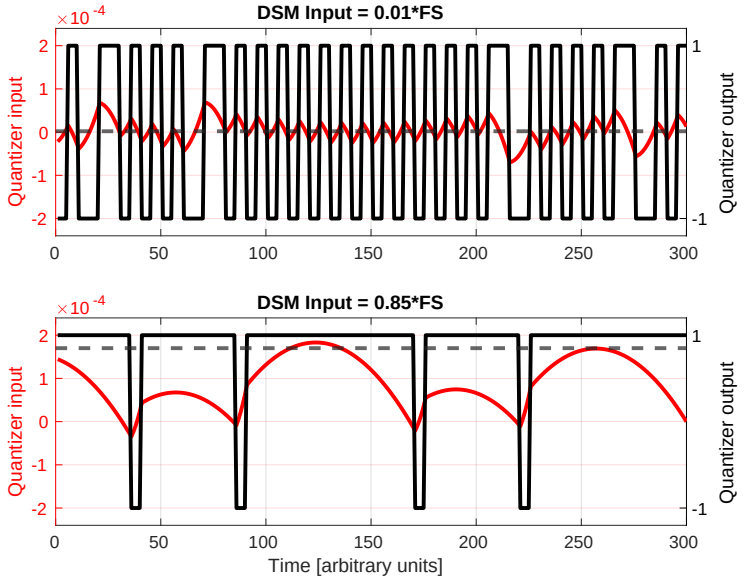


Figure 2.4: Quantizer signals for different input levels

2.2.2 Integrator leakage

Integrator leakage causes the DC transfer function of a DSM to be a nonlinear staircase-like function with dead zones. The biggest dead zone is around 0 and this makes the DSM unresponsive to small input signals. This puts a lower limit on the modulator's DR.

In [23] the width of the dead zone around 0 is predicted based on finite op-amp gain. However, we know that for a 1-bit quantizer, gain by itself makes no difference. More concisely, the width of the dead zones depends on the DT loop filter poles. Behavioral simulations show that for a first-order DSM with pole $p = e^{-\omega_p T_s}$, the width of the dead-zone is $2V_{REF}(1-p)/(1+p)$. For a second-order DSM with two real poles, we first approximate the loop filter by a single equivalent pole $\omega_{eq} = \omega_1\omega_2/\omega_z$, then the width of the dead-zone is given by $2V_{REF}(1-p_{eq})/(1+p_{eq})$ where $p_{eq} = e^{-\omega_{eq} T_s}$. If the poles are complex conjugated, the width of the dead zone is smaller than predicted in the previous expressions, and it decreases as Q increases.

The key point is that dead zones are smaller when the poles of the loop filter are close to DC. For this reason, they typically appear in passive DSM with loop filter poles far from DC or even out-of-band.

Dead zones can be mitigated by adding dither at the input of the comparator [10, 11]. This will change occasionally the decision taken by the comparator, adding a bit of error that displaces the signal out of the dead zone. Because dither is added at the output of the loop filter, it is noise-shaped and has minimal impact on in-band noise. However, the dither must have an amplitude comparable to that of the loop filter output. If the dither amplitude is too large, it will dominate the output of the loop filter and the comparator will produce only random transitions. The loop will become unstable due to a lack of negative feedback.

2.2.3 Simulation method

Due to integrator leakage and mutual loading, it is not practical to model the loop filters described in this work as a number of independent blocks. Hence, in this section, we describe a method for behavioral simulation based directly on the values of the components (R, C, and G) of the loop filter.

First, the loop filter must be expressed in a single-ended form in a SPICE netlist format, specifying the input (V_{in}), DAC (V_{DAC}), and quantizer input (V_y) nodes. It is always possible to find a single-ended equivalent of a fully differential circuit with the same transfer function, and since we are only concerned about the gain,

poles, and zeros, the single-ended circuit yields simpler equations that are faster to simulate.

Next, the s-domain transfer functions of the circuit are extracted from the SPICE netlist in symbolic form using Modified Nodal Analysis (MNA) [26] to avoid errors due to hand calculation. By superposition, the transfer functions $H_{IN}(s)$ and $H_{DAC}(s)$ are obtained by looking at the expression of node V_Y and shorting V_{DAC} and V_{IN} to ground respectively.

Then, these CT transfer functions are converted into DT (z-domain) by the impulse-invariant method, implemented in MATLAB® with the `c2d()` function. Assuming no aliasing and an NRZ DAC:

$$\begin{aligned} H_{IN}(z) &= \text{c2d}(H_{IN}(s), 1/f_s, \text{'impulse'}) \\ H_{DAC}(z) &= \text{c2d}(H_{DAC}(s), 1/f_s, \text{'zoh'}) \end{aligned} \tag{2.8}$$

The digitized transfer functions $H_{IN}(z)$ and $H_{DAC}(z)$ have the same denominator coefficients a_n because they belong to the same circuit, and they differ by the numerator coefficients b_n^{in} and b_n^{dac}. The resulting Z-transforms are:

$$H_{IN}(z) = \frac{V_Y(z)|_{V_{DAC}=0}}{V_{IN}(z)} = \frac{b_0^{in} + b_1^{in} z^{-1} + b_2^{in} z^{-2} + ...}{1 + a_1 z^{-1} + a_2 z^{-2} + ...} \tag{2.9}$$

$$H_{DAC}(z) = \frac{V_Y(z)|_{V_{IN}=0}}{V_{DAC}(z)} = \frac{b_0^{dac} + b_1^{dac} z^{-1} + b_2^{dac} z^{-2} + ...}{1 + a_1 z^{-1} + a_2 z^{-2} + ...} \tag{2.10}$$

Because the impulse-invariant method produces a DT signal that coincides with the CT signal at the sampling moments, which is when the quantizer takes a decision,

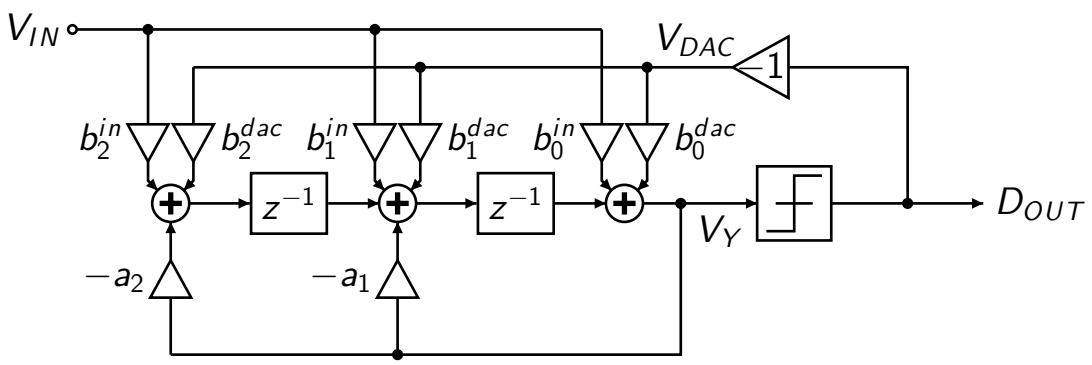


Figure 2.5: Direct-Form-II-Transposed representation of a 2nd-order DTDSM

a CT loop filter can be simulated as a DT Infinite Impulse Response (IIR) filter which can be implemented by acting on the current and previous input samples. In particular, the Direct Form II Transposed implementation is numerically robust [27]. The Direct Form II Transposed implementation (Figure 2.5) allows simulating the DSM directly using the coefficients a_n, b_n^{in} and b_n^{dac} from Equation 2.9 and Equation 2.10.

This simulation method has been shown to execute about 10 times faster than SIMULINK® producing almost the same results. Due to the numerical robustness of the Direct Form II Transposed realization, this simulation method works even in cases where the loop filter has unstable poles, and shows that even in this case, the closed-loop DSM can still be stable due to the action of negative feedback, in agreement with circuit-level transient simulations. The accuracy of this simulation method has been shown to be good enough for architectural validation, and its shorter runtime allows for quicker optimizations.

2.2.4 Optimal loop filter parameters

From behavioral simulations found in the literature (Figure 4.18 from [23]) we see that for a 1-bit, 2^{nd} order DSM the minimum power-of-two Oversampling Ratio (OSR) required to achieve SQNR > 100dB with sufficient margin is OSR=512. The resolution and stability of a DSM are mainly determined by the NTF. In this section, we determine the loop filter parameters that give the best resolution for a given OSR.

The loop filter of a 2^{nd} order CTDSM has two poles and one zero:

$$H_{DAC}(s) = \frac{A_0(1 + s/\omega_z)}{(1 + s/\omega_1)(1 + s/\omega_2)} \tag{2.11}$$

A loop filter zero at ω_z is needed to have a 20dB/dec roll-off at high frequencies, to make the closed-loop system stable. Its frequency determines a trade-off between resolution and stability. A widely accepted empirical optimum is $\omega_z = f_s/1.5$, assuming that the poles are close to DC and an NRZ DAC (Appendix A). Behavioral simulations (Figure 2.6) keeping OSR = 512 confirm that the optimum Signal to Quantization Noise and Distortion Ratio (SQNDR) is reached for $\omega_z = f_s/1.5$ assuming the poles are close to DC.

Having fixed OSR=512 and $\omega_z = f_s/1.5$ we now study the behavior of the CTDSM depending on the loop filter poles ω_1 and ω_2. Figure 2.7, Figure 2.8 and Figure 2.9 show the Bode plots for 3 different configurations of the loop filter poles and the PSD of the bitstream obtained by simulating the CTDSM with a 75% FS, 6.4kHz sine wave input signal. The signal bandwidth, indicated by dashed

vertical line is $f_{BW} = 20\text{kHz}$. The sampling frequency is $f_s = 20.48\text{MHz}$. The bins corresponding to the input tone and its harmonics are shown with markers.

Figure 2.7 shows the behavior with two almost ideal integrators. In practice, integrators always have leakage, which makes the poles $\omega_1, \omega_2 > 0$. However, the effect of leakage may be neglected if the poles are much smaller than the signal bandwidth. We observe that the shaped quantization noise grows by 40dB/dec both in-band and out-of-band until frequencies close to f_s. A third-order distortion component around 19.2kHz is due to the intrinsic non-linearity of the 1-bit quantizer.

Figure 2.8 shows the behavior when one of the poles is out-of-band. This is typical in DSMs with passive RC stages because making the poles close to DC requires a big capacitance, which is not suitable for chip integration. The effect is that the shaped quantization noise grows by 20dB/dec in-band, and by 40dB/dec out-of-band. The in-band quantization noise is increased, resulting in lower SQNR. Total Harmonic Distortion (THD) is significantly worse than the previous case because the intrinsic distortion is added on top of the quantization noise floor.

Figure 2.9 illustrates the behavior with complex-conjugated poles. The poles take the form $\omega_{1,2} = \omega_0 e^{\pm j\theta}$, where ω_0 indicates the frequency of the poles and θ determines the ratio between the real and imaginary part of the poles. For $\theta \approx \pi/2$, the poles are almost imaginary and the loop filter transfer function exhibits a peak around ω_0 with a peak height determined by the quality factor Q. This creates a notch in the NTF, which may be placed in-band to decrease the total integrated in-band quantization noise. In a 2^{nd} order DSM, the optimum frequency of the poles is $\omega_0 = 0.577 * 2\pi f_{BW}$ which gives the minimum in-band quantization noise [23]. Because the quantization noise floor is reduced, the intrinsic distortion has also been reduced, improving the THD.

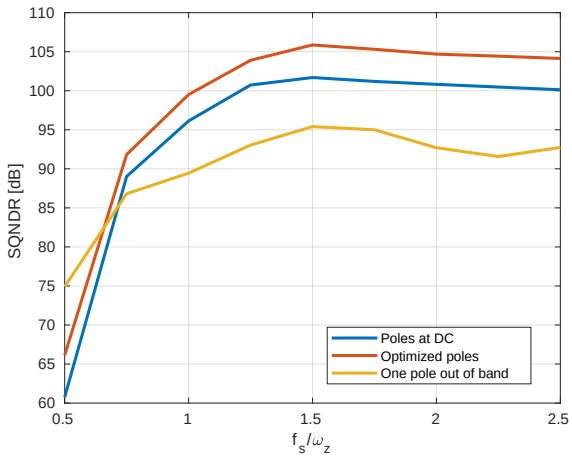


Figure 2.6: Optimal loop filter zero

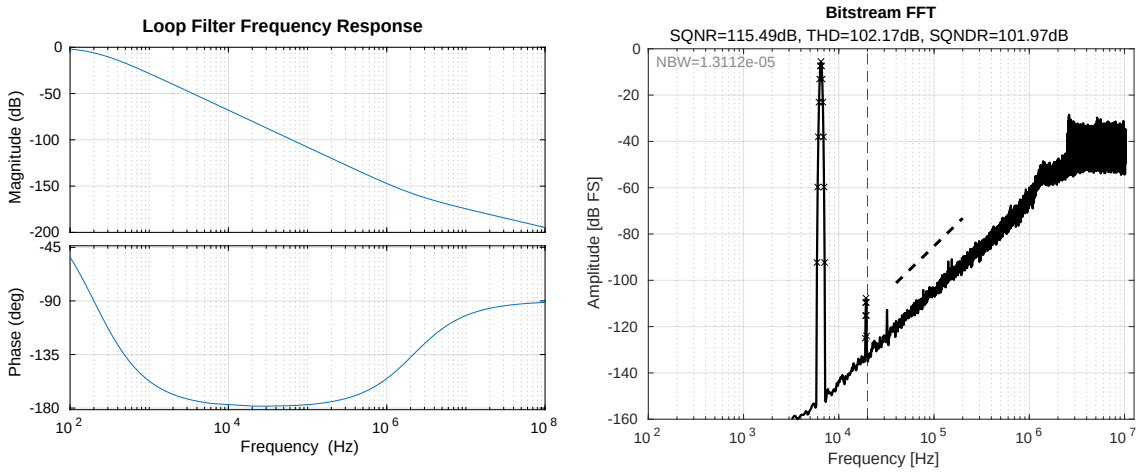


Figure 2.7: Loop filter with two real poles close to DC ($f = 0.01 f_{BW}$)

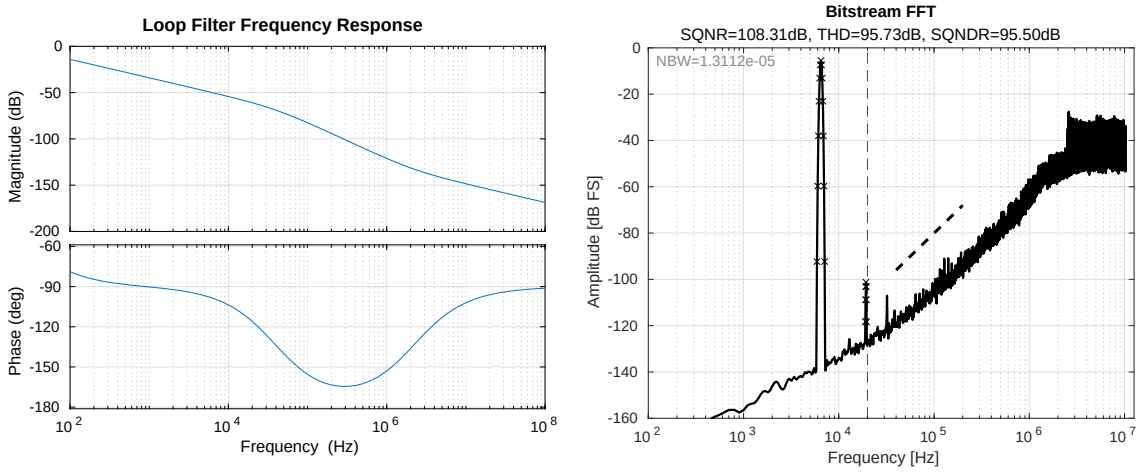


Figure 2.8: Loop filter with one out-of-band pole at $f = 2 f_{BW}$

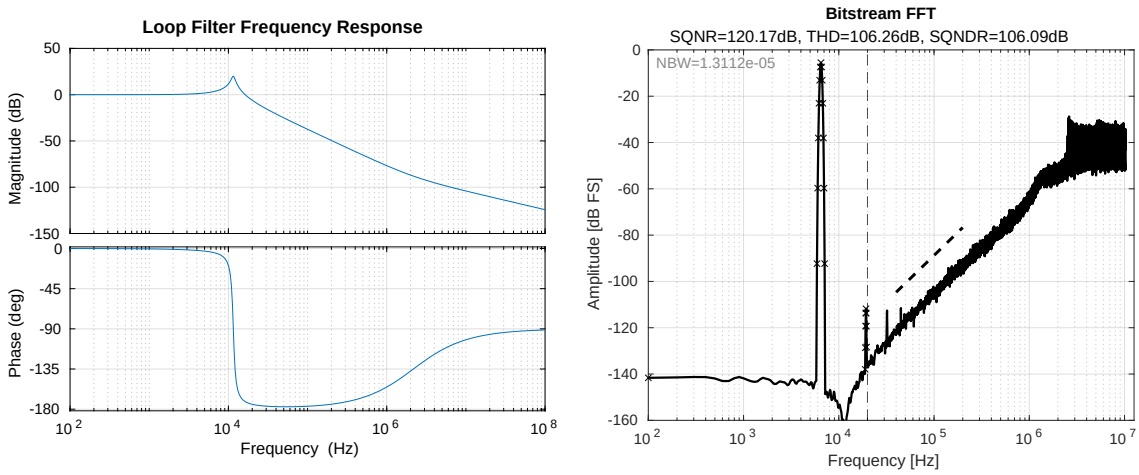


Figure 2.9: Optimal loop filter with two complex-conjugate poles

2.3 Power efficiency in CTDSMs

The power efficiency of high-resolution CTDSM is given by the Schreier's Figure of Merit based on SNDR (FOM_{SNDR}) that combines bandwidth (f_{BW} in Hz), power (P in W), and resolution (SNDR) in a single number:

$$\text{FOM}_{\text{SNDR}}\,(\text{dB}) = \text{SNDR}\,(\text{dB}) + 10\log_{10}\frac{f_{BW}}{P} \tag{2.12}$$

Equation 2.12 indicates that the FOM_{SNDR} stays constant when an increase in power consumption ($\approx V_{REF}^2/R$) results in a reduction in noise power (hence improvement in resolution or SNDR) by the same amount. This happens when the resolution is limited by thermal noise ($\approx 4kTR$) which is the case in well-designed high-resolution ADCs. This justifies the choice of FOM_{SNDR} over other existing figures of merit.

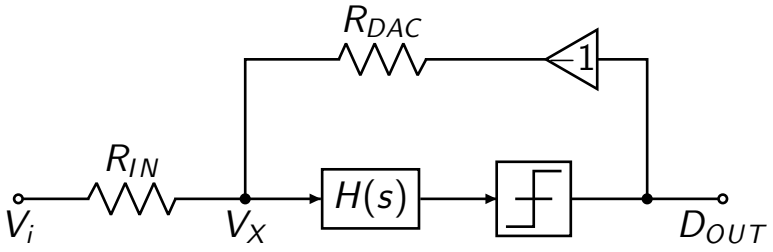


Figure 2.10: A generic CTDSM with resistive DAC

For a CTDSM with a RDAC (Figure 2.10) the input-referred thermal noise of R_{IN} and R_{DAC} is given by Equation 2.13 [28].

$$N_{DAC} = 4kTf_{BW}R_{IN}(1 + \frac{R_{DAC}}{R_{IN}}) \tag{2.13}$$

Assuming a sinusoidal input signal spanning the full range of the DAC without distortion, the maximum power of the signal is $P_{signal} = V_{REF}^2/2$. For simplicity, we assume $R_{IN} = R_{DAC}$. The value of R_{IN} that gives the desired peak SNR is:

$$R_{IN} = \frac{V_{REF}^2}{16kTf_{BW} \cdot SNR} \tag{2.14}$$

Due to negative feedback, the node V_X is held close to 0 during the operation of the CTDSM. Thus the power consumption of R_{DAC} is approximately $P = \frac{V_{REF}^2}{R_{DAC}}$.

A theoretical maximum of the FOM_{SNDR} can be found assuming that only R_{IN} and R_{DAC} produce noise, and that only R_{DAC} consumes power [1]. Combining Equation 2.12 and Equation 2.14, and assuming $T = 300\text{K}$:

$$\text{FOM}_{MAX} = -10\log_{10} 16kT \approx 192\text{dB} \tag{2.15}$$

This result is also valid for a fully differential circuit. In a fully differential implementation, resistors are split into two, and the voltage across the resistors is also split into two, thus the power consumption in each resistor will be $(V/2)^2/(R/2) = V^2/(2R)$. However, the number of resistors has doubled, so the total power stays V^2/R. Therefore, considering only the DAC, the maximum achievable FOM_{SNDR} is the same regardless of whether the implementation is single-ended or fully differential.

In practice, the maximum FOM_{SNDR} from Equation 2.15 cannot be reached due to additional sources of noise, distortion, and power consumption.

2.3.1 Maximum input amplitude and intrinsic distortion

The input signal cannot fully utilize the range of the DAC. To keep the modulator stable, the input cannot exceed the Maximum Stable Input Amplitude (MSA). Even if the modulator is stable, the input peak amplitude V_{PK} for which the ADC is useful must be further reduced, because, for inputs close to the MSA, the quantizer gain is not constant, which results in excessive intrinsic distortion (section 2.2.1). Because $V_{PK} < V_{REF}$, the thermal noise must be lower to reach the desired SNR. Thus R_{IN} and R_{DAC} must be smaller, increasing the power consumption:

$$R_{IN} = \frac{V_{PK}^2}{16kTf_{BW} \cdot SNR} \tag{2.16}$$

The increased power consumption reduces the FOM_{SNDR} by $10\log_{10}(V_{PK}^2/V_{REF}^2)$. For example, limiting the amplitude to 75% reduces the FOM_{SNDR} by 2.5 dB.

The third-harmonic distortion visible in Figure 2.9 is due to the intrinsic distortion of the DSM. Even if the amplitude has been limited to 75%, THD = 105.8dB. It can be shown that SNDR, SNR and THD (all in dB) are related by the equation:

$$\text{SNR} = -10\log_{10}(10^{\frac{-\text{SNDR}}{10}} - 10^{\frac{-\text{THD}}{10}}) \tag{2.17}$$

So to reach the desired SNDR = 100dB, the SNR should be at least 101.26 dB.

[1] The power consumed by R_{IN} is ignored, as done in all reviewed literature.

2.3.2 Partition between thermal and quantization noise

In oversampling ADCs, quantization noise can be easily pushed out of band in several ways. If f_s is relatively low compared to the limits of the particular CMOS technology, increasing the OSR has only a small impact on power consumption. Alternatively, we may adjust the zeros of the loop filter to increase the OBG [23].

However, reducing the thermal noise costs more power because it is a fundamental trade-off. Also, thermal noise is really white, but quantization noise might contain harmonics. Hence low-bandwidth, high-resolution ADCs are designed so that thermal noise dominates. Because quantization noise and thermal noise are uncorrelated, their powers are added, and the following equation holds:

$$\mathrm{SNR} = -10\log_{10}(10^{\frac{-\mathrm{SNR}_{\mathrm{Therm}}}{10}} - 10^{\frac{-\mathrm{SQNR}}{10}}) \tag{2.18}$$

A typical rule of thumb is to make the quantization noise at least 12dB lower than the thermal noise [23]. For example, a total SNR = 101.26dB can be achieved by making $\mathrm{SNR}_{\mathrm{Therm}}$ = 101.53dB and SQNR = 113.53dB.

2.3.3 Noise and distortion of the loop filter

The noise PSD of the loop filter $v^2_{\mathrm{n,loop}}$ appears multiplied by $(1 + R_{IN}/R_{DAC})^2$ when referred to the input of the CTDSM (Figure 2.11) due to the attenuation of the resistive divider formed by R_{IN} and R_{DAC}.

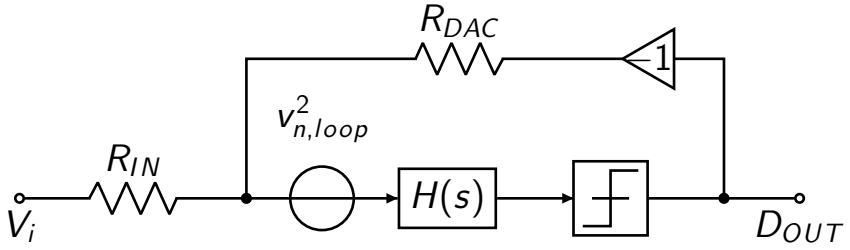


Figure 2.11: Loop filter noise in a generic CTDSM

With a 2-level quantizer, integrator nonlinearity does not cause quantization noise fold-back and appears only as harmonic distortion at the output [29, 30]. The distortion in a differential pair appears when the small-signal assumption begins to fail and depends on how large the differential voltage swing at its input is compared to the V_{GT} of the transistors. For power efficiency, we need the transistors to be in weak inversion which means low V_{GT}, thus the input swing must be low (tens of mV) to achieve linearity [28, 31].

Chapter 3

Passive-input loop filters

In this chapter, we review two loop filters with passive input stages from literature: Fully Passive and Passive RC-OTA. A novel topology, which has been named Single-OTA Resonator, solves the main limitations of the prior art and is the main innovation proposed in this thesis.

The analysis of each topology begins with the transfer function, relating component values to gain, poles, and zeros, which determine the quantizer gain and NTF, finally resulting in the in-band quantization noise and stability bounds of the DSM. Next, the noise sources are input-referred to determine the dominant thermal noise contributors. The power consumption of the DSM can be estimated using reasonable assumptions. Finally, the trade-offs between quantization noise, thermal noise, power consumption, and silicon area are evaluated.

3.1 Fully passive loop filter

An early study of a CTDSM using only passive components in the loop filter was presented in [11], with the circuit shown in Figure 3.1. This circuit behaves like a 2^{nd} order DSM exhibiting 40dB/dec quantization noise shaping. Since the loop filter has no gain, all the loop gain comes from the 1-bit quantizer.

The loop filter transfer function $H_{DAC}(s)$ is found by superposition. Shorting V_{IN} to ground and solving the Kirchoff equations to find the transfer function from V_{DAC} to V_Y, results in Equation 3.1:

$$\frac{V_Y(s)}{V_{DAC}(s)} = \left(\frac{R_{IN}}{R_{IN}+R_{DAC}}\right)\frac{1+sC_2R_3}{1+s(C_2[R_S+R_P]+C_1R_P)+s^2C_1C_2R_SR_P} \tag{3.1}$$

where $R_P = (R_{IN}||R_{DAC})$ and $R_S = (R_2 + R_3)$.

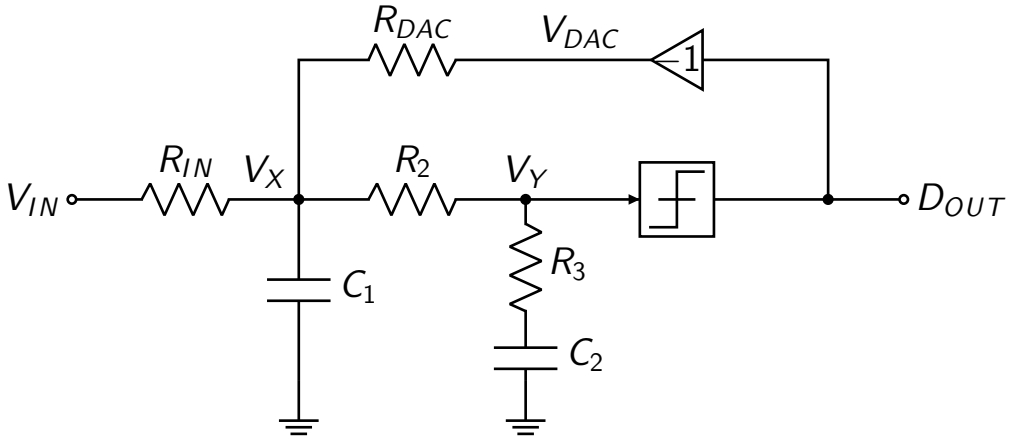


Figure 3.1: CTDSM with a fully passive loop filter

The transfer function has a zero at $\omega_z = (C_2R_3)^{-1}$, which can be designed to be $\omega_z \approx f_s/1.5$ for optimum SQNDR as shown in Figure 2.6. The two poles are given by the roots of the denominator. Due to the nature of the RC filter, the poles lie on the real axis, resulting in the FFTs shown in Figure 2.7 or Figure 2.8. Under the assumption that $R_S >> R_P$, the frequencies of the poles are easily derived as $\omega_1 = (C_1R_P)^{-1}$ and $\omega_2 = (C_2R_S)^{-1}$. Without assuming $R_S >> R_P$, the frequencies of the poles are given by a more complicated expression shown in Appendix B.

The noise from R_{IN} and R_{DAC} is directly referred to the input as in Equation 2.13. The input-referred noise from R_3 is negligible at DC because it is high-passed by C_2. The input-referred noise from R_2 is multiplied by the attenuation of R_{IN} and R_{DAC}, and increases for $\omega > (R_PC_1)^{-1}$ due to the additional attenuation by C_1. The expression for the input-referred noise from R_2 is:

$$v^2_{n,R_2,in}(\omega) = 4kTR_2\left(1 + \frac{R_{IN}}{R_{DAC}}\right)^2(1 + \omega^2R_P^2C_1^2) \tag{3.2}$$

Because the input-referred noise from R_2 increases for $\omega > (R_PC_1)^{-1}$, it is desirable to place $(R_PC_1)^{-1} > 2\pi f_{BW}$ so that this noise does not fall in-band. This allows the size of C_1 to be reduced, saving circuit area. Unfortunately, this results in a sub-optimal NTF (Figure 2.8). Note that $(R_PC_1)^{-1}$ does not necessarily correspond to a transfer function pole (this happens only if $R_S >> R_P$).

From the analysis in Appendix B we can see that the loading effects between the two stages introduce complicated design tradeoffs. To meet the total noise target, the noise from R_{IN} and R_{DAC} must be reduced, which in turn increases the power consumption of the DAC. With all resistors limited by thermal noise, the capacitors become large to place the poles at a low frequency. Furthermore, the

NTF is likely to have out-of-band poles (Figure 2.8) which requires a high OSR to reach the desired resolution. This results in a higher f_s which increases the quantizer gain (Equation 2.6) or equivalently, the comparator has to operate with a very small signal swing, making its design challenging. We conclude that the design of a high-resolution CTDSM based on a fully passive loop filter requires a large chip area, and its ability to achieve high power efficiency is uncertain.

3.1.1 Variation with one extra resistor

Recent literature proposes the use of fully-passive loop filters for biomedical applications targeting low resolution and area [32–34]. The proposed circuit is shown in Figure 3.2. The only difference with respect to Figure 3.1 is the addition of an extra resistor R_C in the input stage. The expression of the resulting transfer function is the same as in Equation 3.1 replacing $R_P = (R_{IN}||R_{DAC}) + R_C$. This shows that the size of C_1 can be reduced because the effective resistance is larger, saving area.

To have the same poles and zeros, R_{IN} and R_{DAC} must be reduced, which increases the power consumption. Their input-referred noise is reduced, but now we have also the noise of R_C, whose input-referred PSD is multiplied by 4 (assuming $R_{IN} = R_{DAC}$). The result is that the total input-referred noise and power consumption increase, degrading the FOM_{SNDR}.

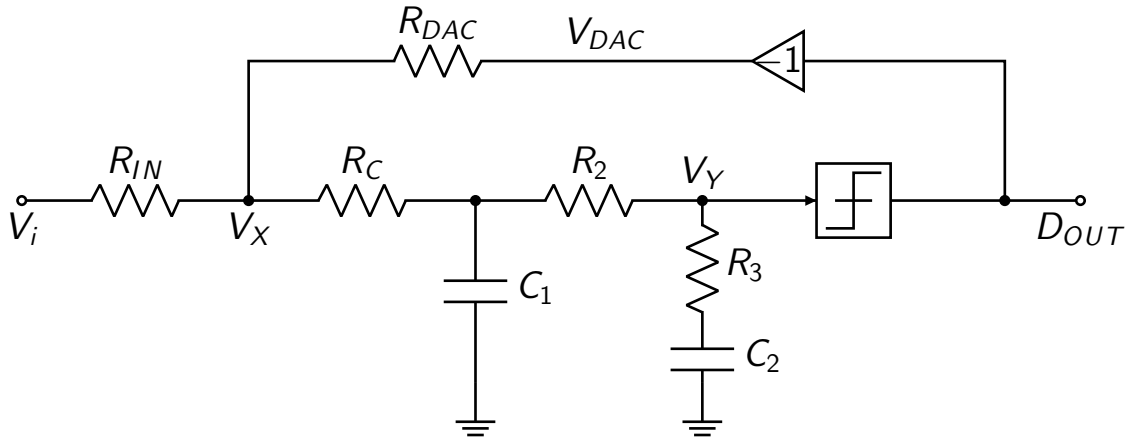


Figure 3.2: CTDSM with a fully passive loop filter variation

3.2 Passive RC-OTA

An improved loop filter consists of a passive RC input stage followed by an Operational Transconductance Amplifier (OTA), as proposed by [15, 17–19] with the circuit shown in Figure 3.3.

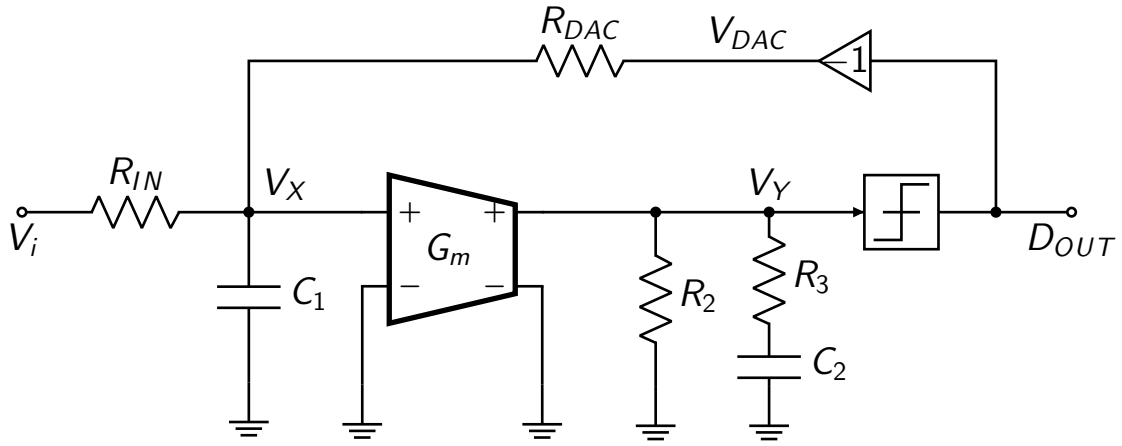


Figure 3.3: CTDSM with a Passive RC-OTA loop filter

The loop filter transfer function is shown in Equation 3.3:

$$H_{DAC}(s) = \frac{V_Y}{V_{DAC}} = \left(\frac{R_{IN}}{R_{IN} + R_{DAC}}\right) \frac{G_m R_2 (1 + sC_2R_3)}{(1 + sR_PC_1)(1 + sR_SC_2)} \tag{3.3}$$

where $R_P = (R_{IN}||R_{DAC})$ and $R_S = R_2 + R_3$.

The addition of an amplifier solves some of the problems of the fully passive loop filter. Firstly, the increased DC gain G_mR_2 increases the voltage swing at the input of the comparator, reducing the probability of metastability and reducing the influence of the comparator noise when referred to the input of the DSM. Secondly, the OTA avoids loading effects between stages so the resulting transfer function has two clearly defined poles at $\omega_1 = (R_PC_1)^{-1}$ and $\omega_2 = (R_SC_2)^{-1}$ simplifying the design process. Furthermore, R_2 can be the output resistance of the OTA, which can be very large, allowing the size of C_2 to be reduced.

The advantage of a passive input stage is preserved: The low pass filter formed by $R_{IN}||R_{DAC}$ and C_1 attenuates the high frequencies where most of the power from the shaped quantization error is concentrated. As a result, the input of the OTA (V_X) has a low swing and can be processed by transistors biased in weak inversion without adding distortion. This allows the OTA to be sized according to thermal noise requirements, resulting in high power efficiency.

The main thermal noise contributors are R_{IN}, R_{DAC}, and the OTA. The PSD of the noise from the OTA referred to the input of the DSM is given in Equation 3.4 [19]:

$$v_{n,OTA,in}^2(\omega) = \frac{4kT\,\Gamma_{OTA}}{G_m}\left(1+\frac{R_{IN}}{R_{DAC}}\right)^2(1+\omega^2R_P^2C_1^2) \tag{3.4}$$

Again, the noise from the OTA is amplified due to the attenuation from R_{IN}, R_{DAC} and increases for $\omega > (R_PC_1)^{-1}$ due to the lack of gain of the passive input stage. If $f_{BW} << (2\pi R_PC_1)^{-1}$, and assuming for simplicity $R_{IN} = R_{DAC}$, integrating Equation 3.4 over the signal bandwidth f_{BW}:

$$N_{OTA,in} = \frac{16kT\,\Gamma_{OTA}}{G_m}f_{BW} \tag{3.5}$$

Still assuming $R_{IN} = R_{DAC}$, we know the input-referred noise from R_{IN}, R_{DAC} using Equation 2.13, and can express the ratio between the noise power from the DAC and the OTA:

$$\alpha = \frac{N_{DAC,in}}{N_{OTA,in}} = \frac{R_{DAC}G_m}{2\,\Gamma_{OTA}} \tag{3.6}$$

The total noise $N_{DAC,in} + N_{OTA,in}$ is fixed to reach the desired SNR specification. We may ask ourselves, is there an optimum α such that the total noise specification is reached with minimum power consumption? Knowing that the power consumption of the DAC is $V_{DD}^2/(2R_{DAC})$ and the power consumption of the OTA is given by a parameter (G_m/I_{VDD}) which depends on the topology of the OTA, the optimum α is derived in Appendix C. Interestingly, with a current-reuse OTA, it is possible to achieve higher power efficiency than with a fully passive loop filter, subject to silicon area and OSR limitations.

However, this loop filter topology still suffers from one limitation. If we wish to reduce the in-band quantization noise, the first pole $\omega_1 = (R_PC_1)^{-1}$ should be close to DC. Because R_{IN} and R_{DAC} dominate thermal noise, this can only be done by increasing C_1, requiring a large area. Even if we allow a large area for C_1, having ω_1 in-band would exacerbate the thermal noise of the OTA when referred to the input of the DSM. The result is that in practical designs, ω_1 is typically designed to be out-of-band, achieving a sub-optimal NTF (Figure 2.8).

3.3 Single-OTA Resonator

The main drawback of the Passive RC-OTA topology is that the product $R_P C_1$ determines a pole in $H_{DAC}(s)$ also determines the frequency after which the input-referred noise from the OTA is exacerbated due to attenuation of the passive input stage. Furthermore, C_1 requires a large area. This trade-off can only be broken by connecting an element to V_X which provides some extra gain at this node.

Because we don't want to increase DC attenuation in V_X, we cannot connect a resistor, so we may connect a capacitor C_3. Connecting the other end of the added capacitor to the output of the OTA V_Y creates a feedforward path around it, replacing R_3 creating a zero in the transfer function. Interestingly, this arrangement not only breaks the dependence of the poles on $R_P C_1$, and also allows the poles to be complex-conjugated.

As discussed in section 2.2.4, a loop filter with in-band complex-conjugated poles achieves the maximum SQNR for a given OSR. In this section, we describe a novel circuit capable of realizing complex-conjugated poles, simultaneously breaking the trade-off from previous sections where the frequency of the poles can only be reduced by increasing capacitance. This circuit has been named the Single-OTA resonator (Figure 3.4).

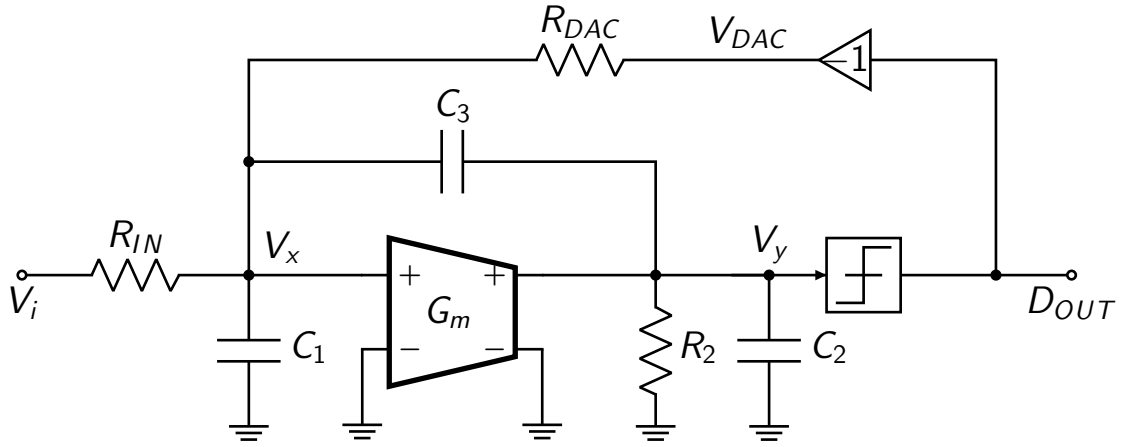


Figure 3.4: CTDSM with a Single-OTA Resonator loop filter

The transfer function of the loop filter is:

$$H_{DAC}(s) = \frac{V_y(s)}{V_{DAC}(s)} = \left(\frac{R_{IN}}{R_{IN} + R_{DAC}}\right) \frac{G_m R_2 (1 + sC_3/G_m)}{1 + s/(\omega_0 Q) + s^2/\omega_0^2} \tag{3.7}$$

$$\frac{1}{\omega_0^2} = R_P R_2 (C_1 C_2 + C_1 C_3 + C_2 C_3) \tag{3.8}$$

$$\frac{1}{\omega_0 Q} = R_P(C_1 + C_3) + R_2(C_2 + C_3) - G_m R_2 R_P C_3 \tag{3.9}$$

where $R_P = (R_{IN}||R_{DAC})$.

The numerator from Equation 3.7 shows the frequency of the zero $\omega_z = G_m/C_3$. Assuming $R_{IN} = R_{DAC}$, the gain at DC is $G_m R_2/2$, the factor of 2 coming from the resistive divider. The poles of the circuit are given by the roots of the second-order denominator, a long expression that depends on parameters ω_0 and Q.

To obtain the optimal NTF, the poles of the loop filter must be complex-conjugate, which happens when $Q > 1/2$. In this case, the frequency of the poles is given by ω_0 from Equation 3.8. Notably, ω_0 does not depend on G_m. The product $R_P R_2$ indicates that ω_0 can be lowered without increasing the capacitors and keeping R_{IN} and R_{DAC} small for thermal noise. R_2 can be made very large because its noise is attenuated by the gain of the OTA.

The loop filter will become unstable when $Q < 0$, equivalently when Equation 3.9 is negative. If this happens, due to component variability, we can ensure the system stays stable by reducing G_m until Q is positive. This can be done by changing the bias current of the OTA. A side-effect is that the frequency of the zero G_m/C_3 will also become lower, but its exact frequency is not critical as long as it's close to the optimal value Figure 2.6. Thermal noise from the OTA will also increase slightly, but this can be solved by designing with some extra margin for thermal noise.

An intuitive explanation of the resonance effect is the following. At the resonance frequency, the impedance from R_{IN}, R_{DAC} and C_1 cancels with the impedance seen into the left leg of C_3 (Figure 3.4). It is observed that the impedance seen into C_3 is real and negative in the mid-frequency range. This is not the first time that a negative resistance is connected to the virtual ground to enhance the performance of a CTDSM [35], although its interaction with a passive input stage was not reported before.

The voltage swing at the input of the OTA must be kept small to achieve sufficient linearity. The swing at V_X is caused by the high-frequency quantization noise coming from the DAC filtered through the transfer function from V_{DAC} to V_X (Equation 3.10). We observe that it has a zero at $\omega = [R_2(C_2 + C_3)]^{-1}$. It is desirable to keep the frequency of this zero high, to get high attenuation of high frequencies. As described previously, R_2 has to be big. Thus we conclude that C_2 and C_3 must be small.

$$\frac{V_{\mathrm{x}}(s)}{V_{\mathrm{DAC}}(s)} = \left(\frac{R_{IN}}{R_{IN}+R_{DAC}}\right)\frac{1+R_2(C_2+C_3)s}{1+s/(\omega_0 Q)+s^2/\omega_0^2} \tag{3.10}$$

The noise from R_{IN} and R_{DAC} appears directly referred at the input as in Equation 2.13. The input-referred noise of the OTA is given in Equation 3.11. Neglecting the effect of the pole G_m/C_3, which is typically out of band, the noise behavior is somewhat similar to that of a Passive RC-OTA (Equation 3.4).

$$v_{n,OTA,in}^2(\omega) = \frac{4kT\,\Gamma_{OTA}}{G_m}\left(1+\frac{R_{IN}}{R_{DAC}}\right)^2\left(\frac{1+\omega^2R_P^2(C_1+C_3)^2}{1+\omega^2C_3^2/G_m^2}\right) \tag{3.11}$$

The input-referred noise PSD increases for $\omega > [R_P(C_1+C_3)]^{-1}$. Notably, this frequency is out-of-band because R_P is small. However, the noise-shaping defining pole is different than this frequency and can be made in-band. This independence between the frequency of the noise-shaping pole and the frequency at which the noise of the OTA starts increasing breaks a fundamental limitation of the Passive RC-OTA topology.

To sum up, the advantages of the Single-OTA Resonator versus the Passive RC-OTA topology are summarised as follows:

1. The frequency of the pole associated with R_P and C_1 can be lowered without increasing C_1, hence saving area, to reduce in-band quantization noise.
2. The poles can be made complex-conjugated to obtain the optimal NTF, essentially the same NTF that can be achieved by a conventional loop filter using active integrators.
3. The noise from the OTA referred to the input of the DSM starts increasing at a frequency that is different from the frequency of the loop filter poles and can be made out-of-band.
4. The capacitor C_3 creates a first-order feedforward path that is insensitive to the parasitic poles of the OTA.

We might also ask ourselves what would happen if C_3 was connected from positive input to negative output of the OTA, contrary to what is shown in Figure 3.4. On one hand, this would change the sign of the feedforward path, creating a right half plane (RHP) zero on the loop filter transfer function. This would decrease the phase margin of the closed loop, requiring another feedforward path to keep the loop stable. On the other hand, all the terms from the right-hand side of Equation 3.9 would be positive, not allowing to make $Q \to \infty$ and the circuit would not have

complex-conjugated poles. Hence, it would not be a good candidate for a CTDSM loop filter.

One limitation of the Single-OTA Resonator is that to implement the fully differential circuit, the capacitor C_3 must be doubled in value and added on each side of the OTA, requiring 4 times the area. Because the frequency of the zero $\omega_z = G_m/C_3$ is fixed, if we wish to reduce C_3 to save area, we also have to reduce G_m, which will increase the input-referred thermal noise. To break this dependence, a variation of the circuit adds two resistors R_{Z2} and R_{Z3} in series with capacitors C_2 and C_3 (Figure 3.5). Behavioral simulations show that with the right component values, a similar 2^{nd} order transfer function can be realized, but due to limited time, this architecture has not been explored further.

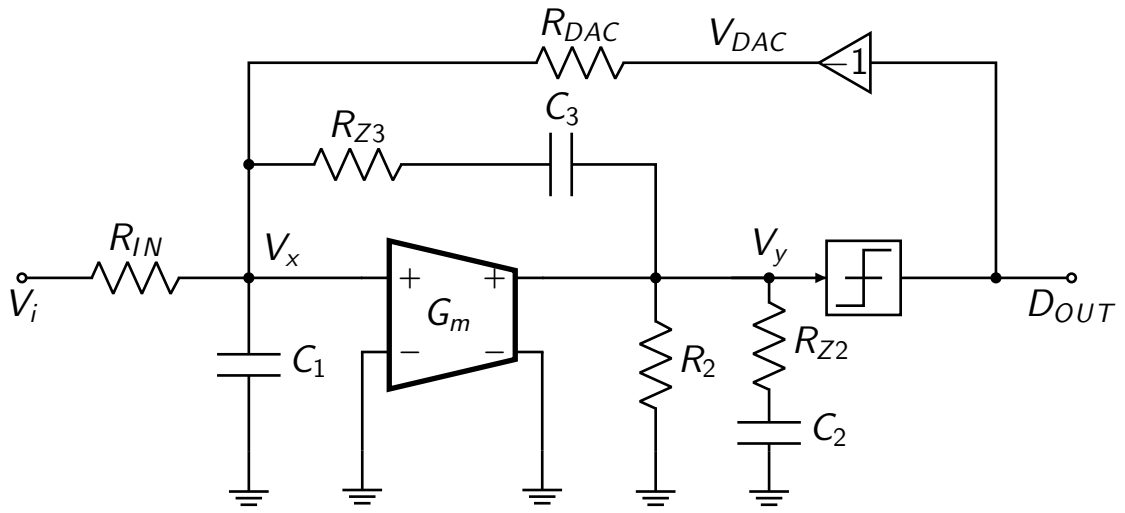


Figure 3.5: CTDSM with a Single-OTA Resonator loop filter variation

Chapter 4

Circuit design

To demonstrate the feasibility of the newly proposed Single-OTA Resonator loop filter, a 2nd-order CTDSM has been implemented in 16nm FinFET technology. This section describes the choice of component values and detailed implementation of the blocks, which have been simulated individually and in connection with each other to understand their nonidealities. Techniques to overcome component variability are described. Finally, a layout has been created and verified by simulation prior to the fabrication of the chip.

4.1 Technology overview

The selected 16nm technology has two types of transistors: Core transistors can support 0.8V and high-voltage transistors 1.8V. The minimum channel length 16nm is only available in core devices. To make use of minimum-length devices when needed, it has been decided to use $V_{DD} = 0.8$V for all parts of the ADC. Furthermore, a library of standard digital cells is only available with 0.8V devices.

The process offers PMOS and NMOS core transistors, with two possible threshold voltage (VT) options: Ultra-Low VT ($|V_T| \approx 250$mV) and Standard VT ($|V_T| \approx 300$mV). Whenever possible, ULVT devices are used for maximum headroom in analog parts and the lowest on-resistance in switches. Only in cases where leakage is a problem, are SVT devices used. FinFET transistors have three parameters: Channel length (between 16nm and 240nm), number of fins (analogous to width, but only in integer steps from 2 to 20), and number of fingers. The number of fingers is always kept to 1 in this design because edge effects have been observed when simulating multi-finger devices which complicate the design of matched pairs. As shown in Figure 4.1, FinFET devices with $L > 80$nm offer high transconductance efficiency and intrinsic gain, and are thus, good candidates for analog circuit design.

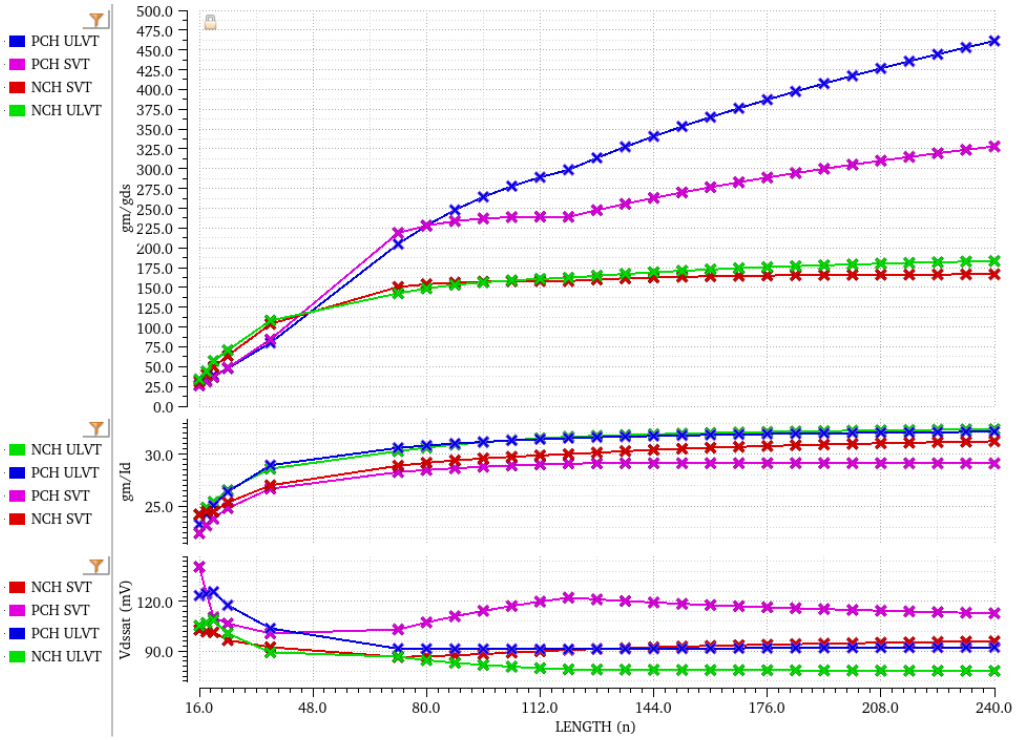


Figure 4.1: Simulated FinFET transistor characteristics

Whenever possible, transistors working in saturation (current sources and amplifying devices) use the maximum channel length 240nm, having the highest intrinsic gain and the lowest short-channel effects. For switches (for example choppers) the minimum channel length 16nm is used because it gives the lowest on-resistance with the lowest parasitic capacitance.

Capacitors used in the loop filter and for decoupling power supplies are realized with the Fringe Metal-Oxide-Metal (crtmom) capacitors available in the standard PDK. These use metal layers from 1 to 7, and have a maximum capacitance density of 9 fF/μm^2. Resistors are realized with high-resistivity, standard PDK resistors (rhim) with a resistivity of 613.06 Ω/square.

4.2 Loop filter design

The selection of the loop filter component values begins by choosing R_{IN} and R_{DAC} based on thermal noise considerations. To keep the intrinsic distortion of the 1-bit CTDSM under control, we limit the input signal to 0.6Vpk, equivalently 75% of FS, as we have seen in prior behavioral simulations. Selecting $R_{IN} = R_{DAC} = 15\text{K}\Omega$ limits the SNR to 102.58dB.

$$\mathrm{SNR_{IN,DAC}} = 10\log_{10}\left(\frac{0.6^2}{16kTR_{IN}f_{BW}}\right) = 102.58\mathrm{dB} \tag{4.1}$$

A G_m stage based on a current-reuse OTA has been designed. Simulations show that with a transconductance of 260μS, the PSD of the OTA integrated over f_{BW} = 20kHz is 9.47×10^{-13} V^2, which is amplified by a factor of 4 when referred to the input of the DSM. This limits the SNR to 102.18dB, allowing some margin with respect to the required 101.53dB derived in section 2.3.2.

Having selected G_m, the value of C_3 = 20pF is chosen to place the loop filter zero ω_z slightly lower than $f_s/1.5$, to accommodate component variability. The remaining components C_1, C_2 and R_2 are determined by solving the equations from section 3.3 to make the poles ω_1, ω_2 complex-conjugated and place the NTF notch at the optimum frequency while making the capacitors large enough to reduce the signal swing at the input of the OTA. The resulting component values are summarized in Table 4.1.

Table 4.1: Nominal values for the loop filter components

Single-ended		Fully-differential		Fully-differential with split capacitors	
R_{IN}	15KΩ	$R_{IN,D}$	7.5KΩ	$R_{IN,D}$	7.5KΩ
R_{DAC}	15KΩ	$R_{DAC,D}$	7.5KΩ	$R_{DAC,D}$	7.5KΩ
R_2	2.7MΩ	R_2	2.7MΩ	R_2	2.7MΩ
G_m	260μS	G_m	260μS	G_m	260μS
C_1	226.8pF	C_1	226.8pF	$C_{1,G}$	151.2pF
				$C_{1,F}$	151.2pF
C_2	20pF	C_2	20pF	$C_{2,G}$	13.3pF
				$C_{2,F}$	13.3pF
C_3	20pF	$C_{3,D}$	40pF	$C_{3,D}$	40pF

4.2.1 Fully differential implementation

Until now, the loop filter has been designed in a single-ended manner for simplicity, but the real implementation is fully differential (Figure 4.2). To preserve the same input-referred thermal noise and frequency response, R_{IN} and R_{DAC} are split into $R_{IN,D}$ and $R_{DAC,D}$, and C_3 must be doubled, resulting in $C_{3,D}$.

To improve rejection to out-of-band common-mode interferers, capacitor C_1 is partitioned into one floating capacitor $C_{1,F}$ and two grounded capacitors $C_{1,G}$

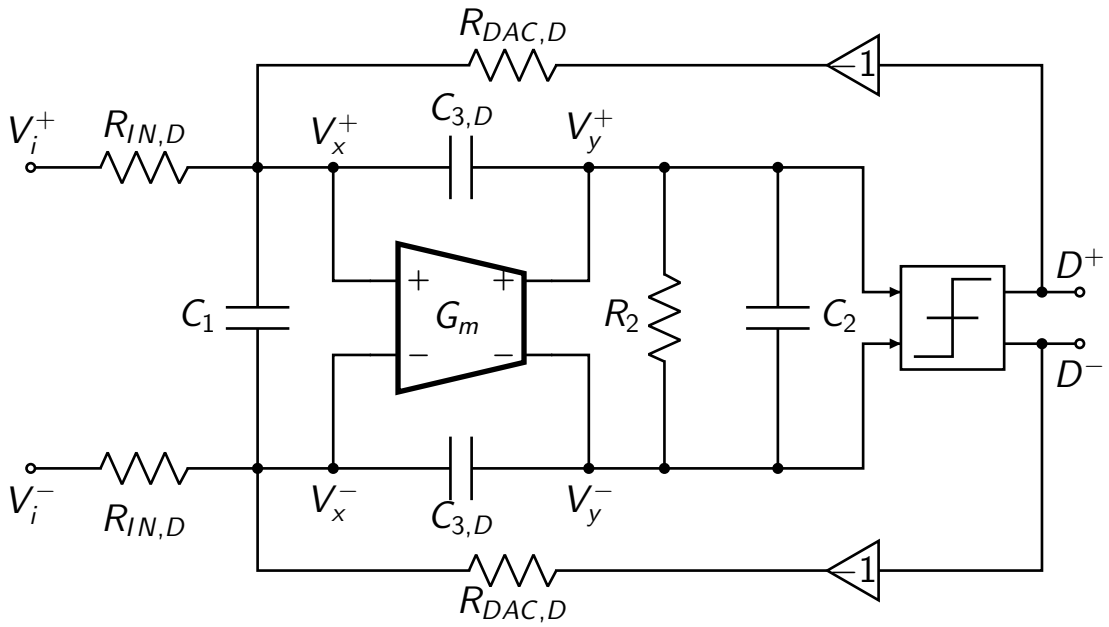


Figure 4.2: Fully differential CTDSM with Single-OTA Resonator

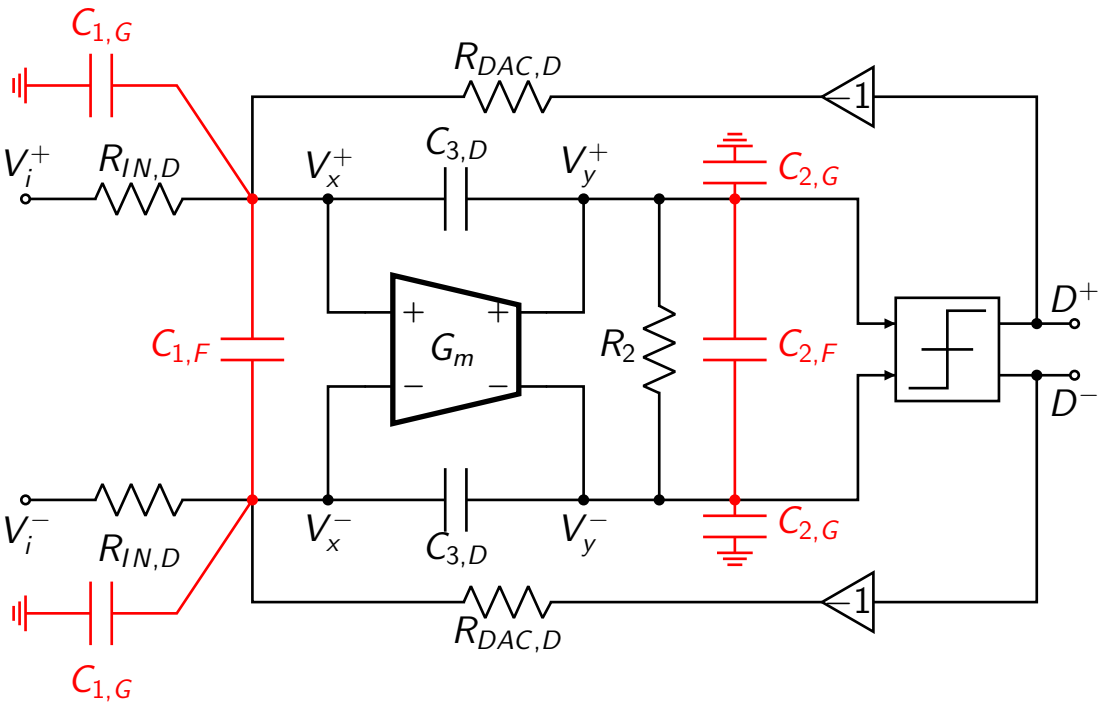


Figure 4.3: Fully differential Single-OTA Resonator with split capacitors

(Figure 4.3). The common-mode interferers are partly absorbed by $C_{1,G}$. The effective capacitance seen by the differential loop filter is preserved if $C_1 = C_{1,F} + 0.5C_{1,G}$. Similarly, capacitor C_2 is partitioned into $C_{2,F}$ and $C_{2,G}$, so that $C_{2,G}$ absorbs the common-mode kick-back current spikes from the comparator. These changes are summarised in Table 4.1.

4.2.2 Tunable RC banks

Simulations show that the R and C values may spread by up to ±15% over corners. To counteract manufacturing variation, some loop filter components have been implemented as a binary array of components that can be switched on and off to adjust their effective value. Resistors R_{IN} and R_{DAC} are excluded because linearity is critical and switches may behave as non-linear resistors. Capacitors C_1, C_2, and C_3 can be varied in 16 steps, selected by switching 4 binary-sized parallel capacitors using 4 bits on the SPI bus. Resistor R_2 has an extended tuning range of 32 steps or 5 bits, which selectively short segments of a chain of series-connected resistors. The switches used are L=16nm with $R_{ON} \approx 40$ to 60Ω. The transconductance G_m of the OTA can also be tuned in 16 steps. Because $G_m \propto 1/R_{bias}$ (Figure 4.8), R_{bias} is implemented as a bank of parallel switchable resistors, so that G_m can be linearly tuned. The switches are L=240nm to reduce leakage.

Table 4.2: Tuning ranges for the loop filter components

Component	No. bits	Arrangement	Minumum	Typical	Maximum
C_1	4	Parallel	182.88pF	228.6pF	297.18pF
C_2	4	Parallel	16.07pF	20.35pF	26.79pF
C_3	4	Parallel	32.37pF	40.8pF	53.66pF
R_2	5	Series	1.98MΩ	2.77MΩ	4.18MΩ
R_{bias}	4	Parallel	15.3KΩ	17.5KΩ	20KΩ

4.3 Operational Transconductance Amplifier (OTA)

Designing an OTA with sufficient linearity and output impedance seems challenging with a supply voltage of only 0.8V. Fortunately, the voltage swings at both the input and the output of the OTA are low. Recent designs have proposed the use of a Pseudo-Differential (PD) OTA which is more linear than a differential pair [36]. Stacking only 4 transistors between V_{DD} and ground, we may allow roughly $V_{DS} = 200$mV for each device, keeping them well in the saturation region.

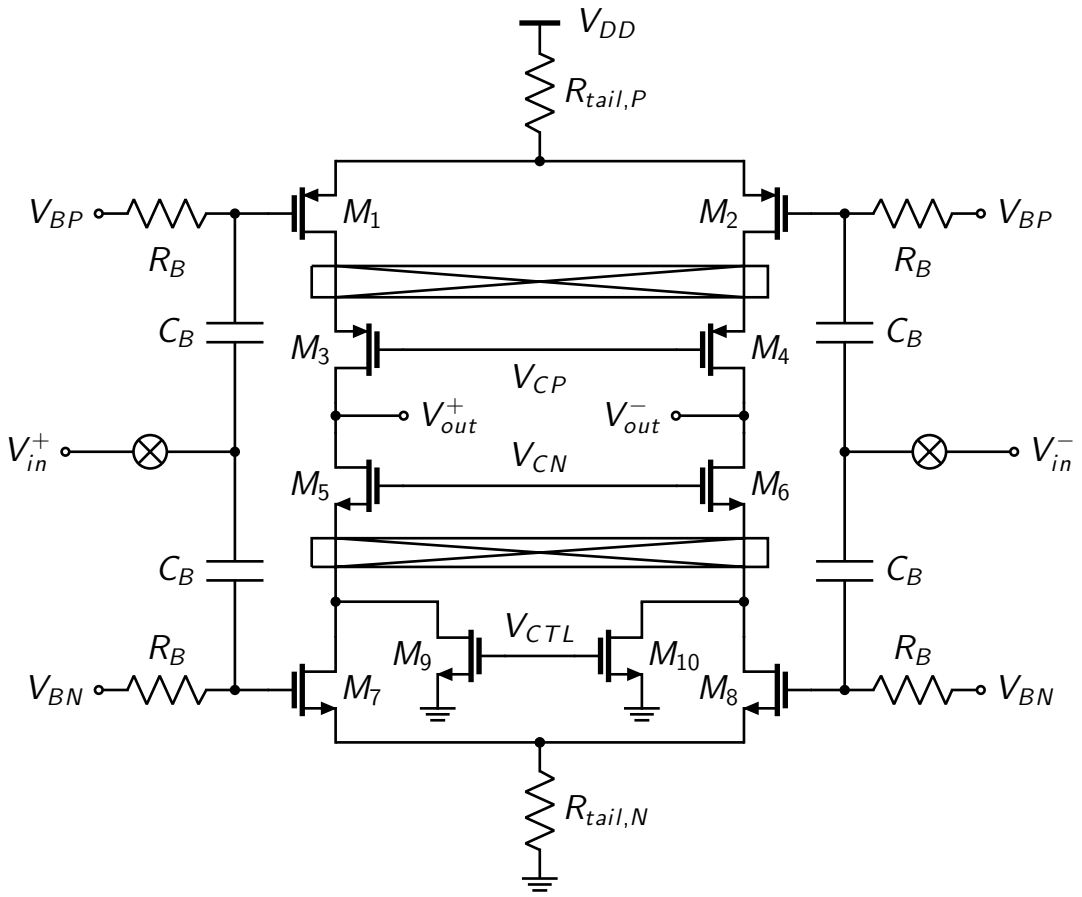


Figure 4.4: Tail-Resistor Linearized (TRL) pseudo-differential OTA

The linearity of a pseudo-differential OTA can be further improved by adding two resistors at the sources of the differential pairs, resulting in a Tail Resistor Linearized (TRL) OTA [37]. The schematic of the realized OTA is shown in Figure 4.4.

The values of the tail linearization resistors $R_{tail,N}$ and $R_{tail,P}$ are chosen to cancel the 3^{rd} order distortion on each differential pair at the TT corner (Figure 4.5). In the chip implementation, these resistors can be optionally shorted by a switch, resulting in a conventional PD OTA.

$$R_{tail,N} = \frac{nV_T}{2 \times 0.7 I_{Tail,N}} = \frac{1 \times 26\text{mV}}{2 \times 14\mu\text{A}} = 928\Omega \tag{4.2}$$

$$R_{tail,P} = \frac{nV_T}{2 I_{Tail,P}} = \frac{1 \times 26\text{mV}}{2 \times 20\mu\text{A}} = 650\Omega \tag{4.3}$$

To reject the 1/f noise from the input pairs, the OTA is chopped. Chopping at a frequency equal to f_s avoids increasing the noise floor due to intermodulation with

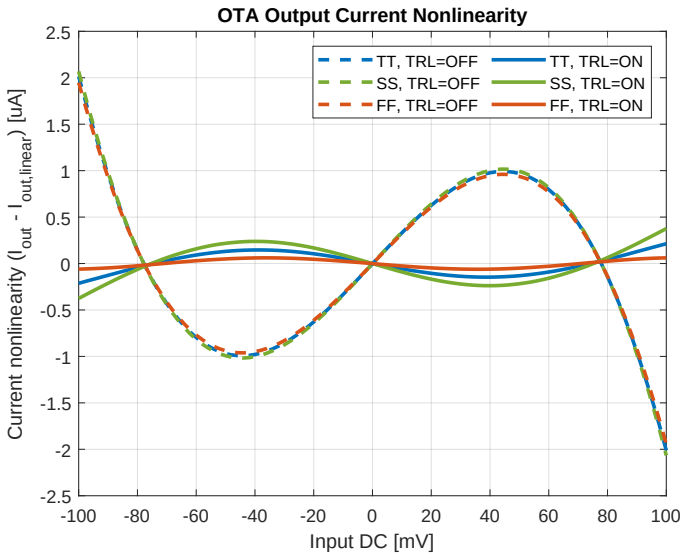


Figure 4.5: Simulated DC nonlinearity of the OTA

the quantization noise [38]. Assuming there is no mismatch between the two halves of the differential circuit, chopping at $f_s/2$ will also not increase the noise floor. In the implementation, the chopping frequency can be selected to be f_s or $f_s/2$ via SPI.

Because chopping up-modulates the input signal, it will be passed through a high-pass filter formed by C_B and R_B. The up-modulated signal is then demodulated by the output choppers, allowing a capacitively-coupled chopper OTA to have gain at DC.

The DC bias voltage of the input transistors is set via resistors R_B. Because the bias voltage coupled through R_B can be chosen freely, the input signal can be coupled to both the PMOS and NMOS differential pairs, improving the power efficiency of the OTA by to current reuse.

The high-pass coupling network is formed by $R_B = 500\text{K}\Omega$ and $C_B = 1\text{pF}$, giving a cutoff frequency of 318 kHz, well below the chopping frequency. The thermal noise introduced by R_B is low-pass filtered by R_B and C_B. Only the PSD of this filtered noise around the chopping frequency will be de-modulated back to DC by the output choppers. Therefore, R_B and C_B must be large enough to sufficiently filter this noise. With the chosen values, the noise introduced by R_B accounts for less than 2% of the total noise introduced by the OTA (Figure 4.6)

To generate the required bias voltages V_{BP} and V_{BN} for the respective input pairs, and V_{CP} and V_{CN} for the cascodes, a replica bias network has been used (Figure 4.7). Each branch of the bias network carries $1/10^{th}$ of the current carried by each of the two branches of the OTA. This scaling factor is preserved for the tail

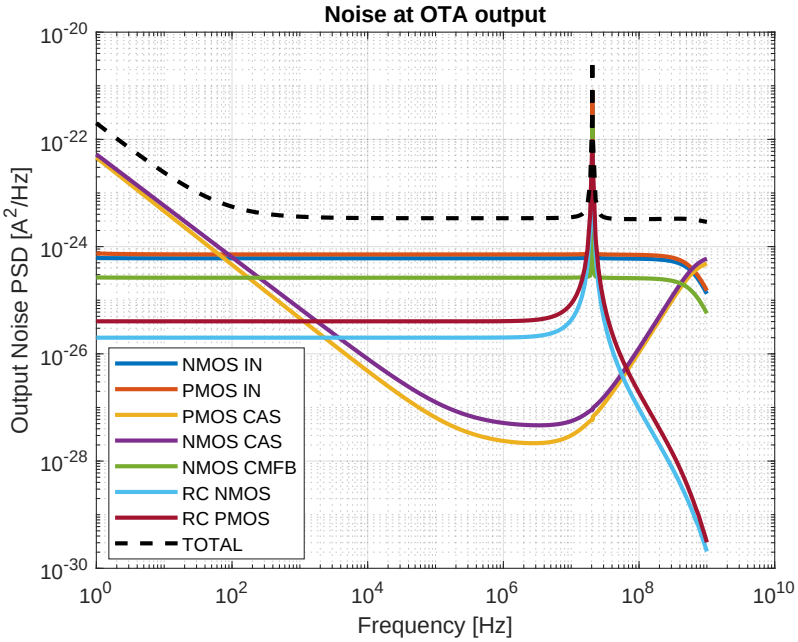


Figure 4.6: PSD of the noise sources within the OTA

linearization resistors $R_{tail} = 13\text{K}\Omega$, which are also included in the bias network and can be optionally shorted. The sizes and operating points for all transistors from the OTA and the biasing network are detailed in Table 4.3.

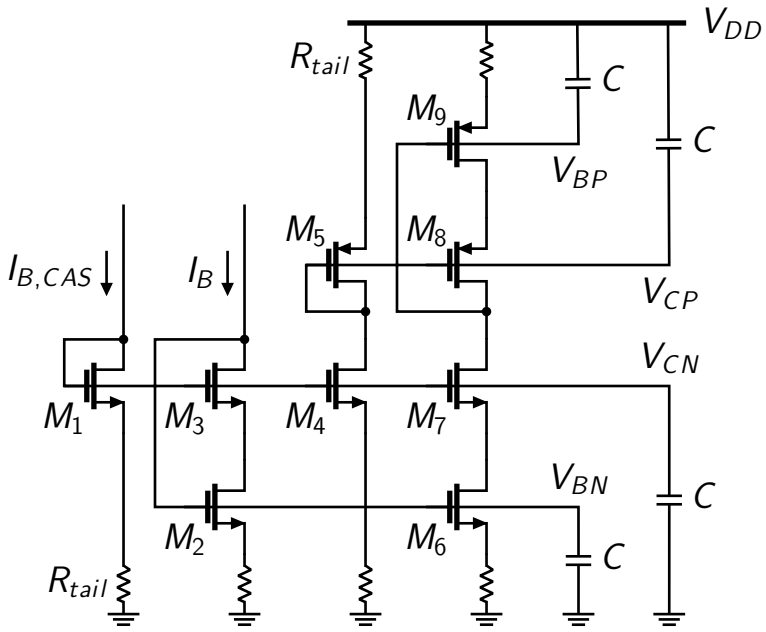


Figure 4.7: OTA bias generator

Table 4.3: OTA transistor sizing and operating point

Device	L [nm]	N_{FIN}	M	g_m [uS]	r_0 [MΩ]	I_D [uA]	V_{ds} [mV]
Main OTA							
M_1, M_2	240	20	10	332.7	0.98	10.32	201.2
M_3, M_4	240	20	10	331.4	0.84	10.32	184.5
M_5, M_6	240	20	10	326.4	0.33	10.06	209.5
M_7, M_8	240	20	7	234.1	0.36	7.22	177.5
M_9, M_{10}	192	16	3	92.7	0.96	2.84	190.8
Bias circuit							
$M_{1,4}$	6x240	3	1	-	-	1.03	-
M_5	6x240	3	1	-	-	1.02	-
$M_{2,3,6,7}$	240	20	1	-	-	1.04	-
$M_{8,9}$	240	20	1	-	-	1.02	-
Common-mode feedback							
M_{1-4}	80	10	1	18.1	13.5	0.508	420.1
$M_{5,6}$	80	10	1	32.9	1.7	1.01	180.2
Constant-g_m circuit							
M_1	240	20	7	73.36	1	2.06	158.4
M_2	240	20	1	33.37	2.8	1.03	191.38
M_3	240	20	1	32.62	6.6	1.002	550.5
M_4	240	20	1	32.47	13	1.002	250.4
M_5	240	20	1	33.25	14	1.03	608.5
M_6	240	20	2	66.5	7	2.06	605.5
$M_{7,8}$	240	20	1	33	13	1.02	-
M_9	240	5	1	-	-	-	-
M_{10}	240	20	1	-	-	-	-
$M_{11,12}$	240	2	1	-	-	-	-

4.3.1 Constant-gm bias

To generate the bias voltages to establish a certain G_m for the OTA, a Constant-G_m cell has been designed based on the one proposed in [37]. In the schematic shown in Figure 4.8, the currents through M_1 and M_2 are equal due to the current mirror outputs from M_5 and M_6. The gate voltages of M_1 and M_2 are also equal. Assuming all transistors are biased in weak-inversion saturation, the negative feedback loop through M_3 and M_4 establishes that the transconductance of M_2 is proportional to $1/R_{bias}$, as given by the expression:

$$g_{m,M_2} = \frac{0.93 \ln K}{M R_{bias}} \tag{4.4}$$

For $M = 2$ and $K = 3.5$, and the ranges of R_{bias} described in Table 4.2, I_B and $I_{B,CAS}$ are approximately 1uA. By sizing the OTA transistors with a certain ratio with respect to M_2, the G_m of the OTA is made controllable.

The remaining transistors from Figure 4.8 are a start-up circuit. When the circuit is turned on, the drain voltage of M_1 is close to 0. Through the inverter formed by M_{10} and M_{11}, this turns on M_9, increasing the current through M_4, which is mirrored by M_5 and M_6, charging the internal voltages. When the voltage at the drain of M_2 raises above the threshold of the inverter (which is made low by the voltage drop across M_{12}), M_9 turns off and the constant-gm cell continues its operation around the operating point. Capacitors $C_1 = C_2 = 50$fF are added to ensure loop stability and reduce glitches at start-up, respectively.

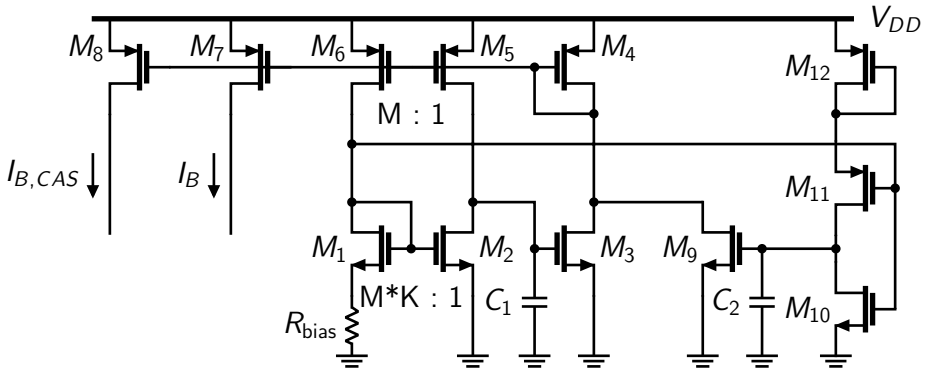


Figure 4.8: Constant-G_m bias generator

4.3.2 Common-mode feedback

A Common-Mode Feedback (CMFB) loop ensures that the outputs of the OTA are kept around $V_{DD}/2$. Shown in Figure 4.9, two differential pairs formed by M1-M4 sense the voltage at the outputs of the OTA and compare them with a reference voltage $V_{CM} = V_{DD}/2$, producing two differential currents proportional to $(V_{out}^+ - V_{CM})$ and $(V_{out}^- - V_{CM})$. These currents are added together, producing a control V_{CTL} voltage proportional to $(V_{out}^+ + V_{out}^-)/2 - V_{CM}$. The control voltage drives transistors M9 and M10 from Figure 4.4 closing the feedback loop.

In a conventional differential pair, common-mode interferers are rejected because the common-mode gain is degenerated by the output impedance of the tail transistor. However in a pseudo-differential amplifier, because there is no tail transistor, the

common-mode and differential-mode paths have in principle the same gain. The only mechanism to reject common-mode interferers in a pseudo-differential amplifier is the CMFB loop. Hence, it is desirable to increase the loop gain and speed of the CMFB loop. This is achieved by connecting M5-M6 as an active current mirror, as opposed to the common practice of using diode-connected loads.

The current mirror connection of M5-M6 increases the impedance at the node V_{CTL}, lowering the frequency of the associated pole. This makes the system unstable and requires frequency compensation. A fast path formed by C_{comp} = 100fF and R_{comp} = 1MΩ ensures stability with a phase margin higher than 60° across corners (Figure 4.10).

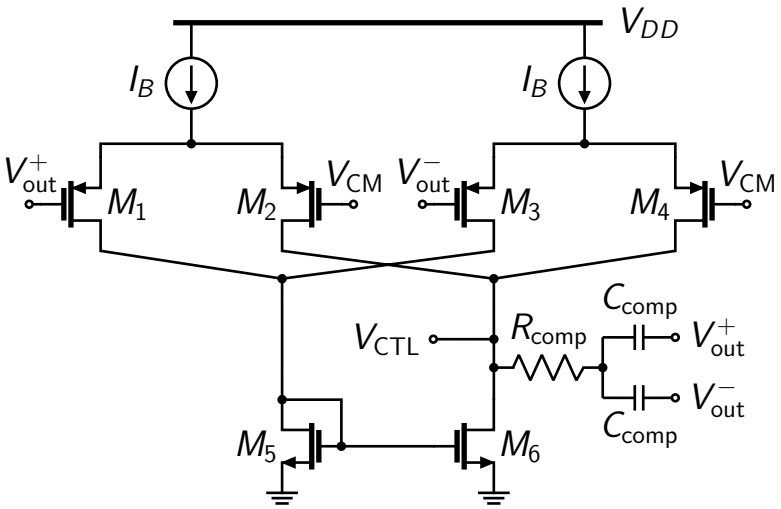


Figure 4.9: Common-Mode Feedback circuit

4.4 Comparator

For its simplicity, speed, and robustness, the StrongARM comparator is used in this design. The well-known circuit described in [39] has been implemented with an L=20nm NMOS input pair, the rest of the transistors with L=16nm. The average current drawn from V_{DD}=0.8V at f_s=20.48MHz is 2.2uA, 1.7uA, and 3.33uA at the typical, slow and fast corners respectively.

The input-referred noise of the comparator has been simulated using the method described in [39]. A small DC voltage is applied at the input of the comparator, and a transient noise simulation is run for 5000 clock cycles. The simulation is repeated sweeping the applied DC voltage from -250uV to 250uV in steps of 0.5uV. The average comparator output is saved for each simulation. The result is an erf() curve, whose derivative is a normal distribution whose variance is equivalent to the

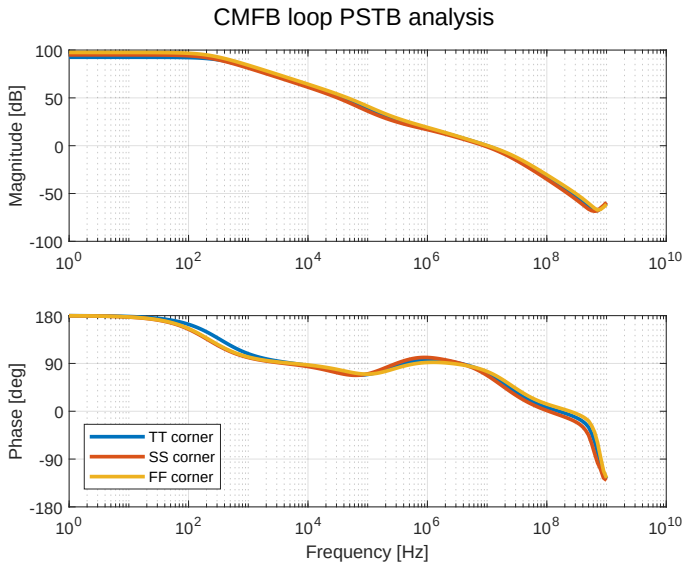
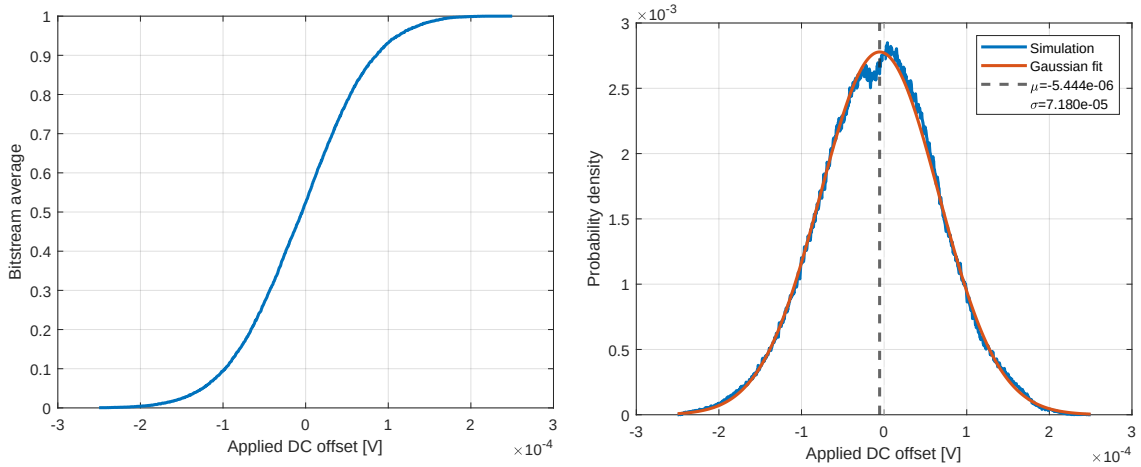


Figure 4.10: CMFB loop stability analysis

input-referred noise power. The simulated input-referred noise is observed to be about 10 times lower than the expected voltage swing at the input of the comparator, meeting and exceeding the requirements.



(a) Output probability 5000 clocks

(b) Probability density and Gaussian fit

Figure 4.11: Simulation of the Strong ARM comparator input-referred noise

4.5 Non-return to zero (NRZ) DAC

In this work, an Non-Return to Zero (NRZ) DAC is chosen for its simplicity and better jitter robustness compared to an Return to Zero (RTZ) DAC. The main concern about an NRZ DAC is Inter-Symbol Interference (ISI), which is caused by

the non-equal rise and fall times of the DAC signal. However, in a fully differential implementation, the rising edge of the differential DAC signal is the superposition of a rising edge and a falling edge from complementary sides of the circuit. The same is true for differential falling edges. Hence, if the two complementary halves of the circuit are perfectly matched, there is no Inter-Symbol Interference (ISI). The required matching can be achieved by sizing and careful layout [36].

4.6 Pseudo-random dither generator

A circuit that inserts dither at the input of the comparator has been incorporated into this design, to study its effects on the ADC performance. The dithering signal is a very-long pseudo-random sequence generated by a 20-bit, maximal length Linear Feedback Shift Register (LFSR) implemented in the Galois form (Figure 4.12). The dithering signal is added to the output of the loop filter by a capacitive coupling network (Figure 4.13) with attenuation selectable between -62dB and -76dB via SPI registers. The LFSR can be turned entirely off via SPI.

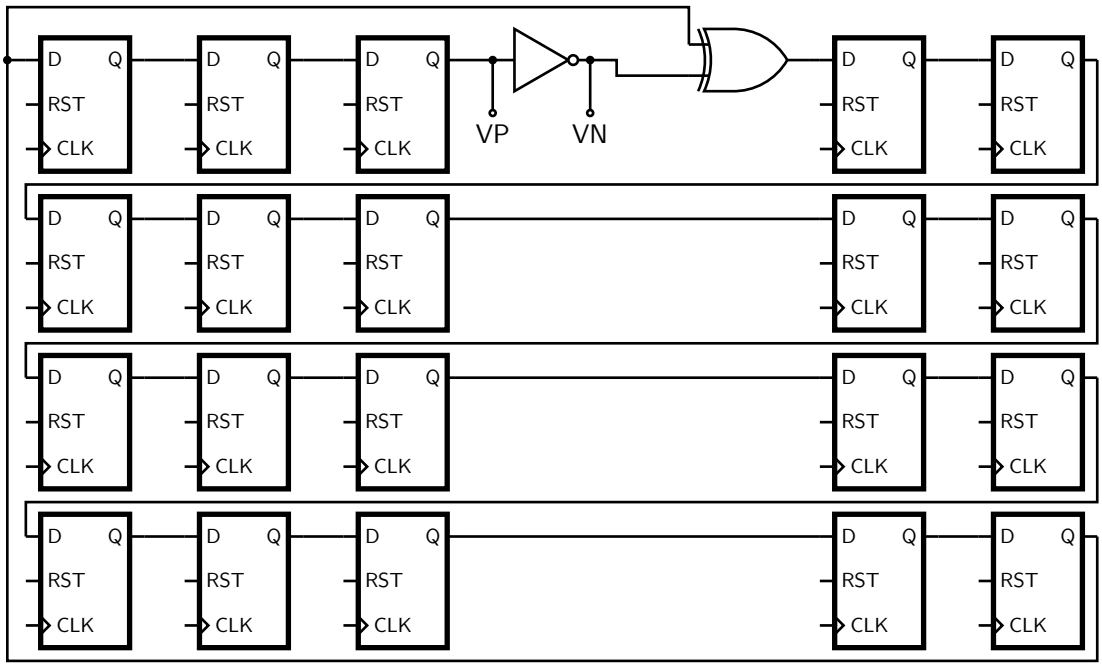


Figure 4.12: Linear-Feedback Shift Register (LFSR) dither generator

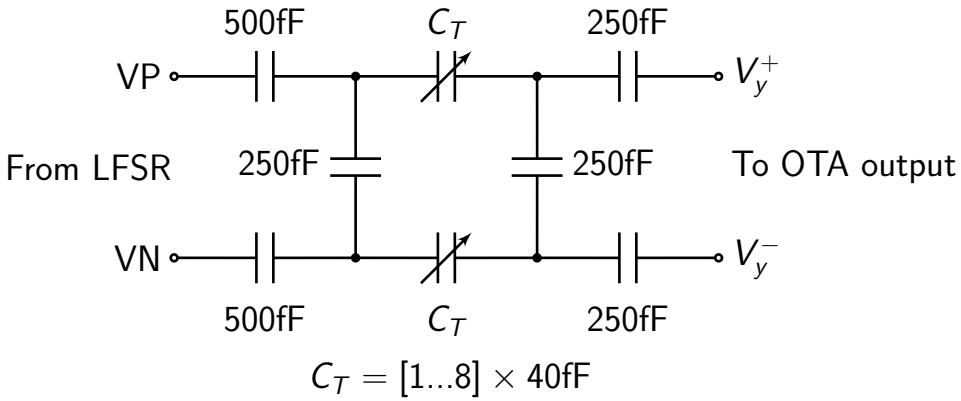


Figure 4.13: Capacitive coupling of the dither generator

4.7 Clock generator

An external 327.68MHz clock with is supplied to the chip. This is internally divided by an 8-stage Johnson Counter using flip-flops from the 16nm standard cell library, producing a 20.48MHz clock with different delayed phases (Figure 4.14). One of the phases is taken as the reference phase ϕ_0 and connected to the clock of the comparator. One of the next 4 phases $\phi_1...\phi_4$ with delays $[1, 2, 3, 4]T_s/16$ can be selected independently by two multiplexers to get the clock for the DAC and the choppers. The DAC delay ensures that the comparator is not in a metastable state and the chopper delay ensures that the signals have settled well before the comparator samples the output of the OTA. The chopper clock can be further divided by 2 to chop at $f_s/2$. All components from the clock generator use 16nm devices, consuming about 1.6uW from 0.8V when clocked at 327.68MHz.

This technique was adopted due to the lack of time to design and verify an RC-based delay cell, which would only have required an external 20.48MHz clock.

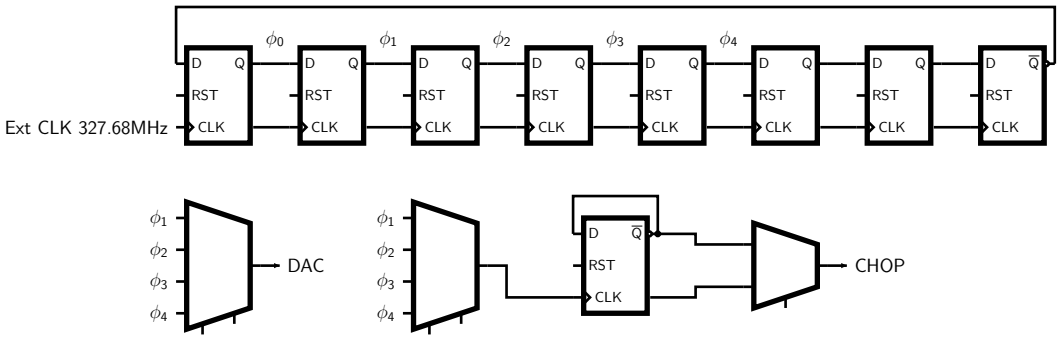


Figure 4.14: Clock generator

4.8 Layout

The design has been implemented in an area of $620 \times 250\mu$m, shown in Figure 4.15. The majority of the area is occupied by loop filter capacitors C_1, C_2, and C_3. To shield the devices from substrate noise, all blocks within the DSM are surrounded by individual deep-N wells. The DSM is only part of a 2×2mm multi-project die (Figure 4.16), in which all the projects share the same SPI block and clock receiver. Pins are shared with other IP blocks to fully utilize the number of pads available. All the IP blocks sharing pins can be turned on/off via SPI registers.

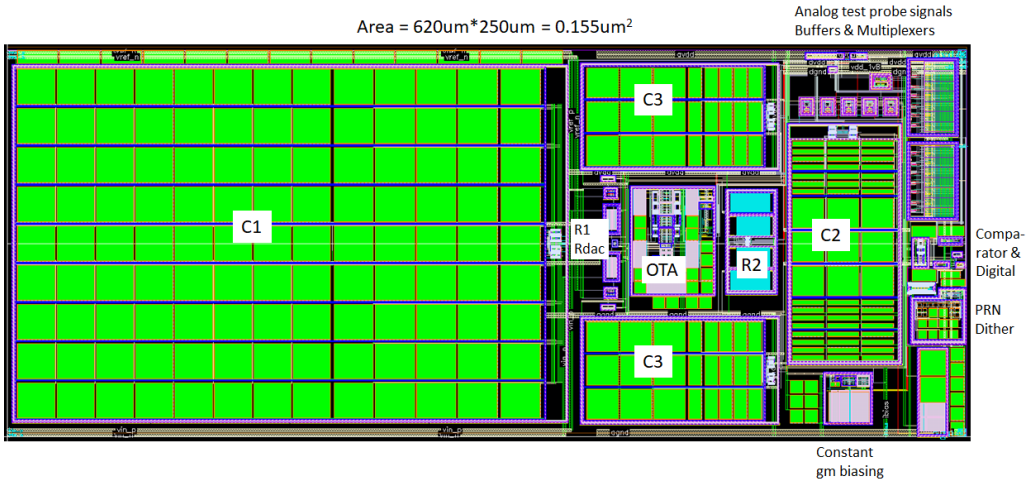


Figure 4.15: Layout of the DSM with main components indicated

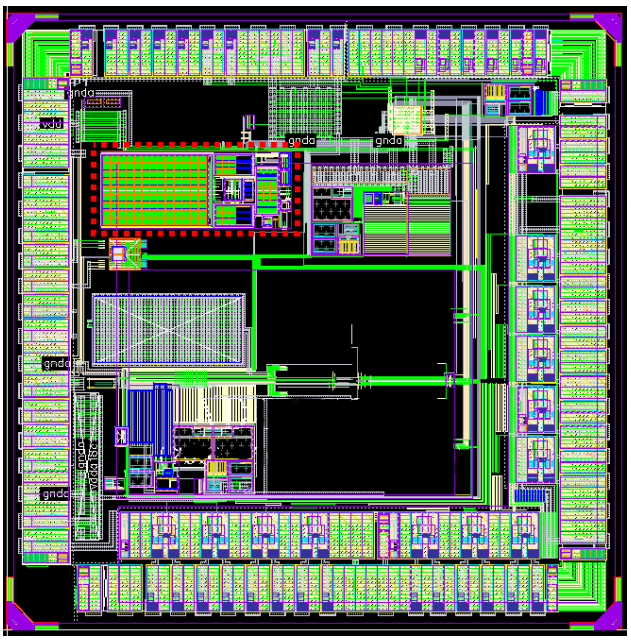
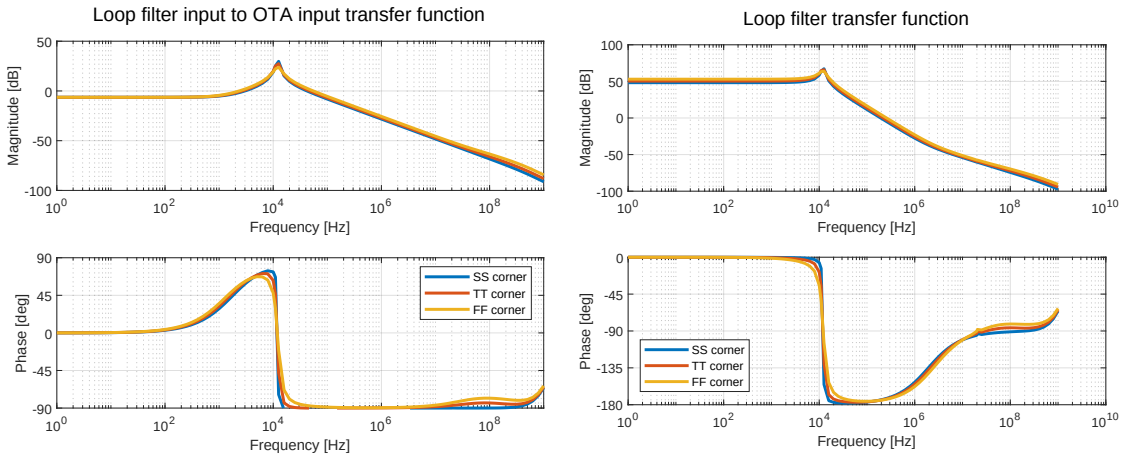


Figure 4.16: Location of the DSM within the fabricated die

4.9 Top-level simulations

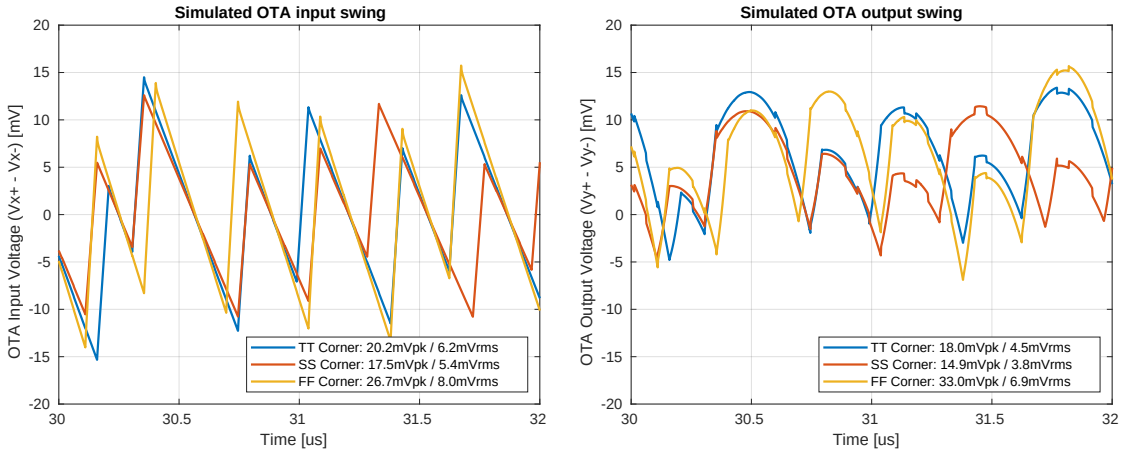
The functionality of the various blocks after layout has been verified by simulation prior to the fabrication of the chip. Figure 4.17 shows the periodic AC (PAC) simulation of the loop filter frequency response including real resistors, capacitor banks, and OTA over corners. In each corner, the appropriate bits from the SPI register are set, such that the transfer frequency behavior stays close to the expected.

Figure 4.18 shows the differential voltage swings at the input and output of the OTA in a transient noise simulation over corners. The voltage swings are very small, as expected. In Figure 4.18b, the dithering signal from the LFSR is visible as sharp steps at deterministic time instants.



(a) OTA input V_X (b) OTA output V_Y

Figure 4.17: Simulated loop filter transfer function over corners with trimming



(a) OTA input (b) OTA output

Figure 4.18: Simulated OTA differential voltage swings

Figure 4.19 and Figure 4.20 show, respectively, the FFT of the bitstreams obtained from simulating the complete design without and with layout parasitics. The input signal is a 6.4kHz sinewave with 75% FS amplitude. The only information that can be extracted from these figures is that the general functionality of the circuit is correct across corners. Due to time limitations, it was not possible to run simulations long enough to reliably estimate SNR, SNDR, and THD.

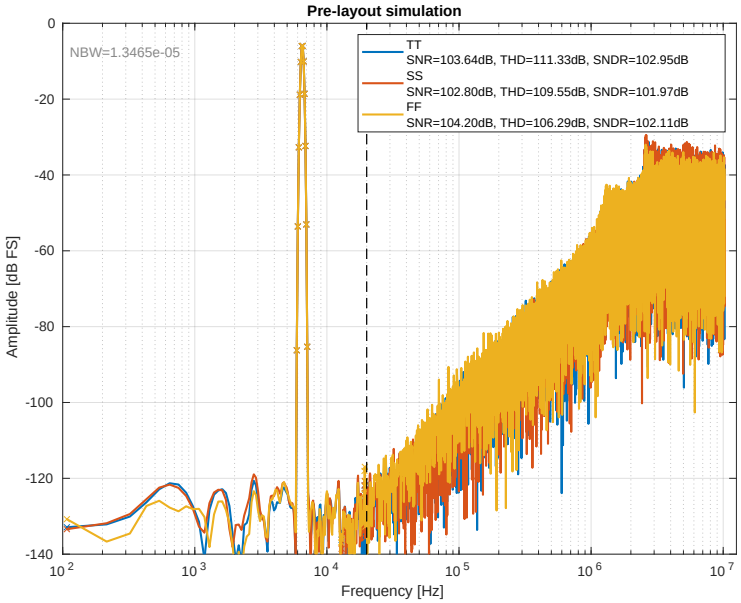


Figure 4.19: Pre-layout simulation of the DSM

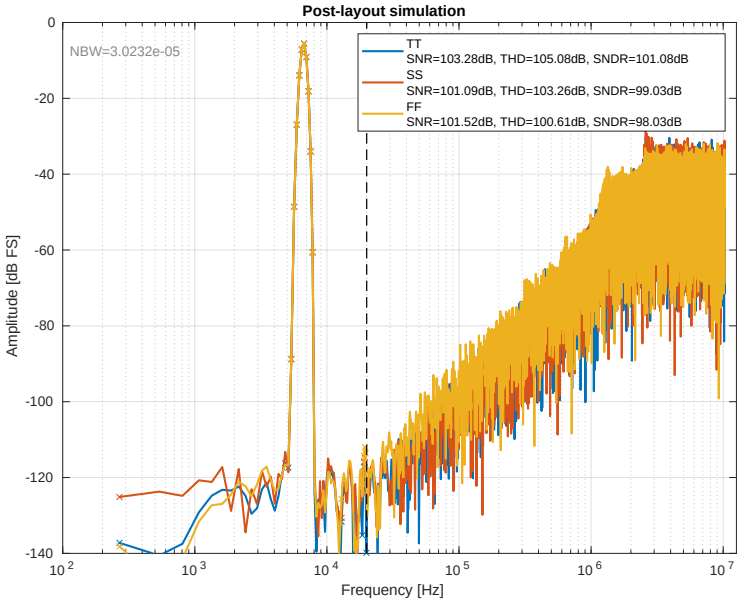


Figure 4.20: Post-layout simulation of the DSM including extracted parasitics

Figure 4.21 shows the FFT of the bitstream obtained from post-layout simulations in the TT corner, using the Monte Carlo method to simulate component mismatch. Due to limited run time, only two Monte Carlo cases are shown. As expected, DC offset appears due to the mismatch between the differential halves of the circuit. Again, the amount of information is not sufficient to judge the quantitative performance of the chip, but qualitatively it can be seen that the functionality is preserved.

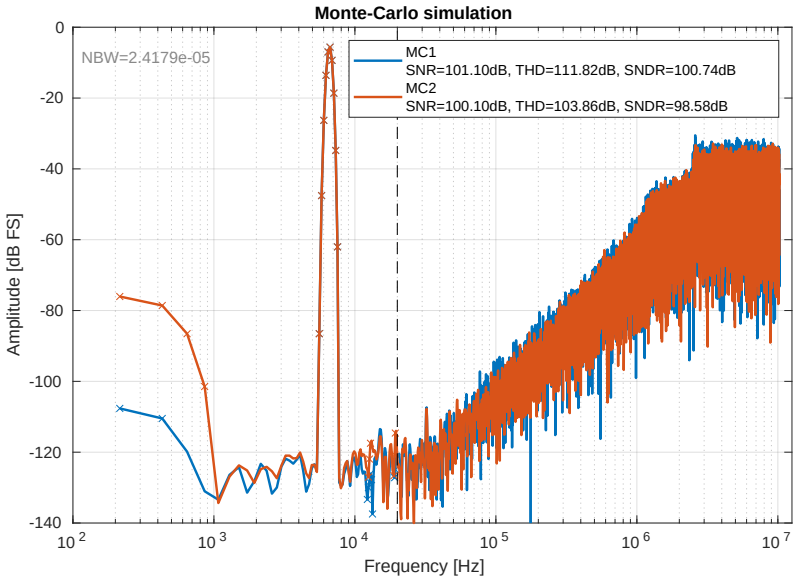


Figure 4.21: Monte Carlo simulation of the DSM (2 cases)

Chapter 5

Measurements

A Printed Circuit Board (PCB) has been designed to test the performance of the chip (Figure 5.1). The board includes high-linearity buffers (OPA1611) to drive the input of the ADC, although they were not needed in the end, because the ADC could be driven directly by the 40Ω differential output of an Audio Precision APx555 high-performance sinewave generator. The 327.68 MHz clock is generated differentially by a Si5338 clock generator and made single-ended by a balun (TC2-72T+). The digital interface is galvanically isolated with digital isolator ICs, and the bitstream is captured by LabVIEW (PCIe-6537), to be further processed in MATLAB.

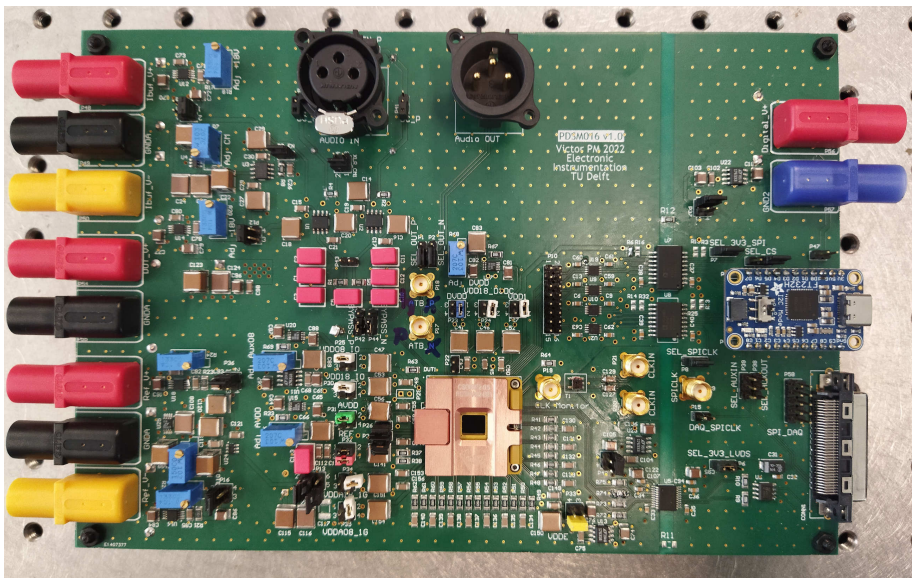


Figure 5.1: Test board built to measure the chip

5.1 DR, Peak SNR and Peak SNDR

To measure the performance of the chip over its dynamic range, a sine wave with an amplitude ranging from 6μV to 0.8V is applied to the differential input of the ADC. The frequency of the sine wave is kept constant at 6.4kHz, which ensures that the third harmonic at 19.2kHz will have its maximum amplitude (worst case HD3). The measurements are taken with Tail Resistor Linearized (TRL) ON and OFF, keeping the rest of the conditions the same. The SNR and SNDR are plotted in Figure 5.2.

The top limit of the DR is when the amplitude is 0dBFS (0.8V$_{pk}$), with a measured SNR of about 58dB. The lower limit is given by the point where SNR reaches 0dB. Under this definition, the measured DR is 99.46dB and 98.03dB with TRL ON and OFF respectively. The difference is because at small amplitudes, the SNR is about 1.5dB higher with TRL ON than with TRL OFF.

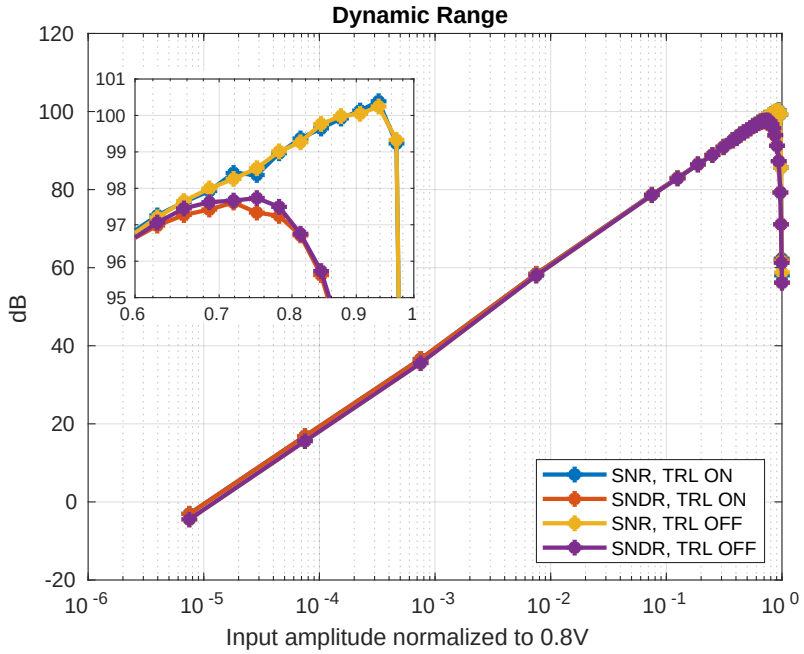


Figure 5.2: Measured Dynamic Range (DR)

However, the peak SNR is 100.39dB and 100.25dB for TRL ON and OFF respectively, and in both cases occurs for amplitudes around -0.54dBFS (0.75V$_{pk}$). We consider this point to be the Maximum Stable Input Amplitude (MSA), the maximum amplitude at which the DSM is usable in practice, after which distortion (Figure 5.3) increases rapidly. The peak SNDR is 97.47dB and 97.73 with TRL ON and OFF respectively (Figure 5.4) reached for a -2.5dBFS (0.6V$_{pk}$) input.

Both SNDR and SNR are about 3dB lower than expected, due to a higher-than-expected white noise floor. By ruling out other possibilities, this has been attributed

to jitter in the sampling clock, which cannot be changed because it is shared among other IP blocks on the chip. Jitter is observed as skirts around the main tone. To mitigate this effect, these bins are considered part of the signal and are not counted as in-band noise.

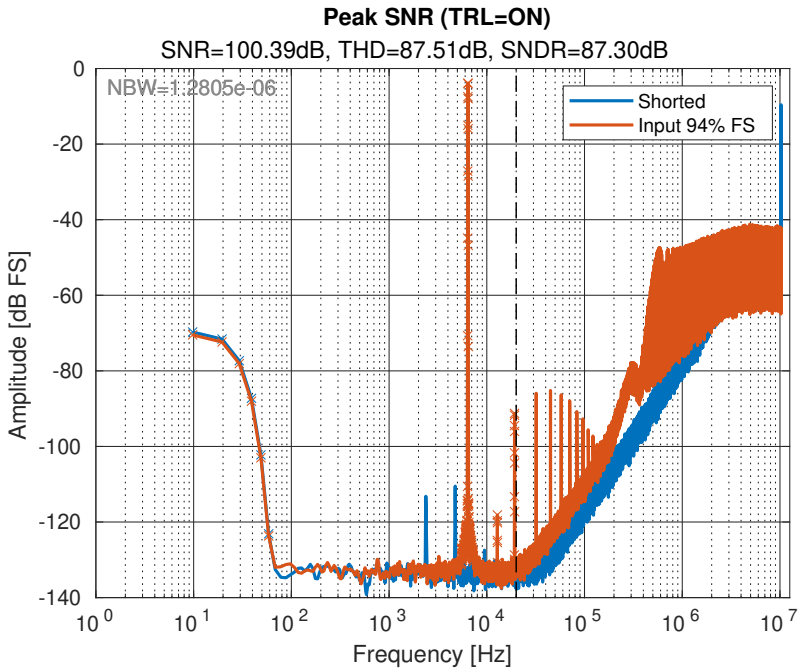


Figure 5.3: Measured MSA and Peak SNR

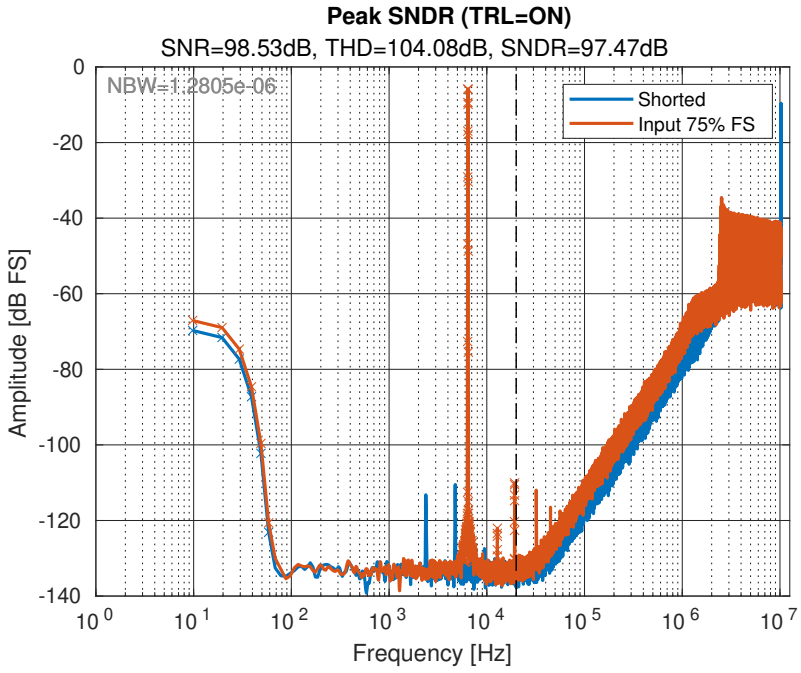


Figure 5.4: Measured Peak SNDR

5.2 HD3 over frequency

In Figure 5.5, a -2.5dBFS ($0.6V_{pk}$) sinusoid is applied at the input, and its frequency is swept from 20Hz to 15kHz. For each frequency, the HD3 (which goes from 60Hz to 45kHz) is measured. We observe that the HD3 has a notch at around 10kHz. For such high amplitude, the distortion is dominated by the intrinsic distortion of the quantizer, which "rides" over the NTF. This indicates that the loop filter is working as expected.

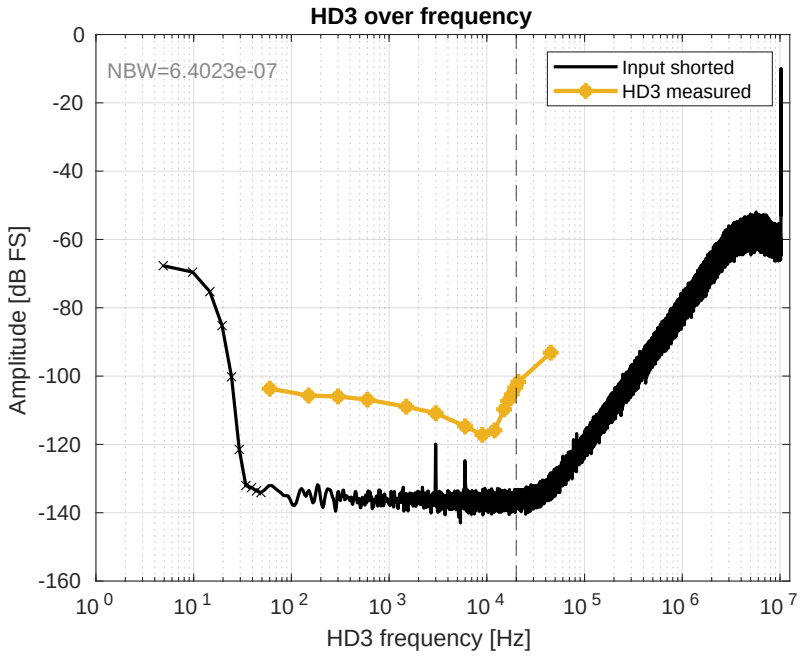


Figure 5.5: Measured HD3 over frequency

5.3 Power consumption

Unfortunately, due to the pin-sharing scheme with other IP blocks within the chip, the power consumption of the DSM cannot be measured directly. It must be estimated using indirect measurements and reasonable assumptions. The DSM block has three power supplies: AVDD, DVDD, and VREF.

Analog VDD (AVDD). Connected to the OTA and its bias circuits. This power supply is not shared with other IP blocks and is the only one whose power consumption can be measured directly. The measured power consumption is in agreement with post-layout simulations.

Digital VDD (DVDD). Connected to the comparator, LFSR, and clock generator. This power supply is shared with the SPI slave block, which handles the communi-

cation protocol and stores the registers' data for the entire chip. To estimate the power consumption at DVDD, first, the SPI clock is turned off. This decreases the measured current and brings it close to the simulation value, but there is still a discrepancy. With the SPI clock OFF, the clock frequency is varied to extrapolate what is the power consumption when $f_{CLK} = 0$. This corresponds to leakage, which is very unlikely to be coming from the comparator, LFSR, or clock generator, which are fully dynamic circuits with less than 50 logic gates in total. Hence, the leakage must be coming from the SPI block, a synthesized circuit that has thousands of gates. Hence, the leakage is subtracted from the measured current.

ADC Reference Voltage (VREF). Connected to R_{DAC} through NRZ DAC transistors. This power supply is shared with several other blocks within the chip and has a 100Ω resistor connected in parallel to suppress oscillations due to parasitic inductances of the bond wires. The power consumption by VREF is estimated by indirectly measuring $R_{DAC,D}$. First, the input of the OTA is shorted using a reset switch, and $R_{IN,D}$ is measured with a multimeter between both input pins. From $R_{IN,D}$ and the signal gain measured in the FFT, we infer that $R_{DAC,D} \approx 8\text{K}\Omega$. Thus, the power consumption is estimated as $V_{REF}^2/(2R_{DAC,D})$.

The measured power consumption after the above-mentioned adjustments is shown in Figure 5.6.

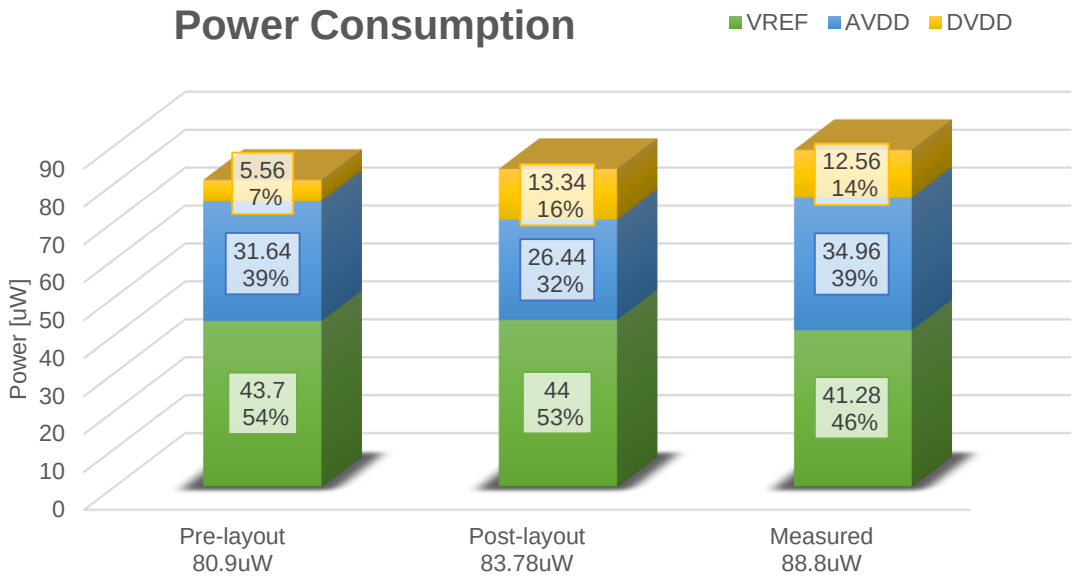


Figure 5.6: Simulated and measured power consumption of the chip

5.4 CMRR and PSRR

To measure Common-Mode Rejection Ratio (CMRR), the inputs of the DSM are shorted and connected to a common voltage with a DC value of 0.4V added with a sine wave with an amplitude of 100mV (-18dBFS) whose frequency is swept from 100Hz to 20MHz (Figure 5.7). Below 10kHz, the CMRR is about 65dB and does change upon enabling or disabling TRL. Above 10kHz, the CMRR decreases, although it is about 3dB better with TRL ON, because R_{Tail} acts as a degeneration resistor for common-mode signals. At high frequencies, the CMRR drops to about 32dB.

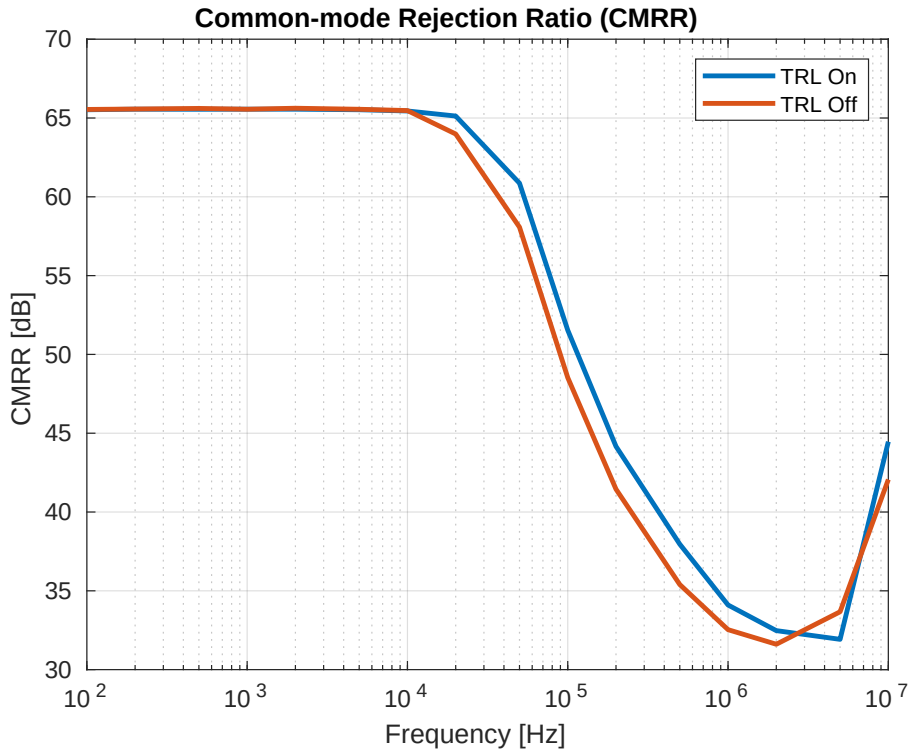


Figure 5.7: Measured Common mode rejection ratio

To measure Power Supply Rejection Ratio (PSRR), the inputs of the DSM are shorted and connected to a constant 0.4V DC voltage. Decoupling capacitors are removed from the PCB traces connected to AVDD, and a sine wave with amplitude 100mV (-18dBFS) is added to the nominal $V_{DD} = 0.8$V DC. The frequency is swept from 100Hz to 20MHz (Figure 5.8). The PSRR is around 70dB below 10kHz. Above 10kHz, its behavior is heavily dependent on whether TRL is enabled or not. With TRL ON, the PSRR slightly improves up to 72.5dB, before dropping to 40dB at high frequencies.

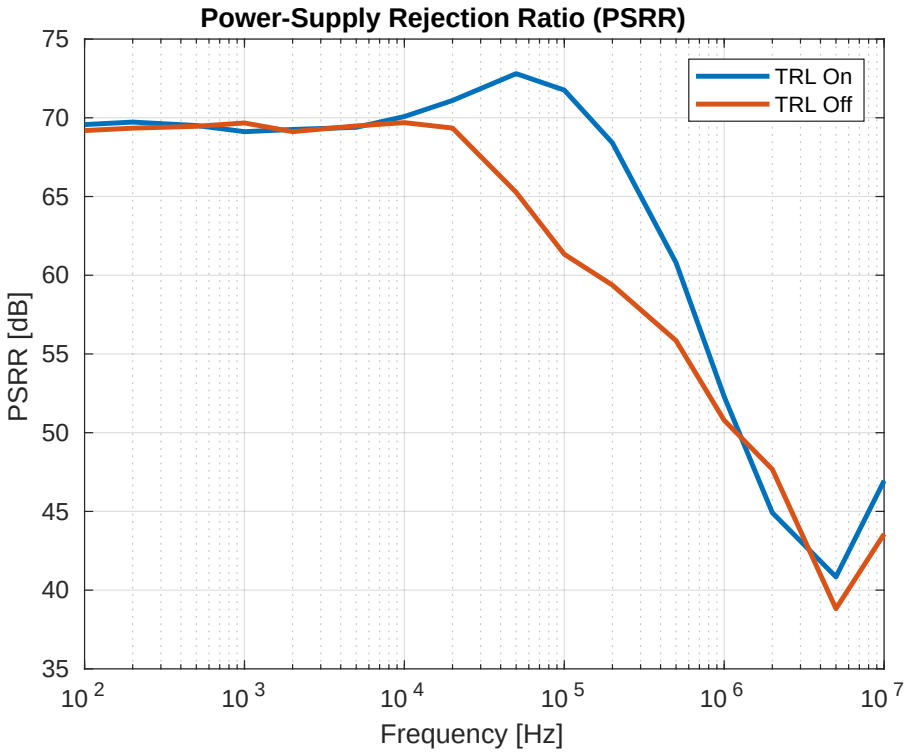


Figure 5.8: Measured Power supply rejection ratio

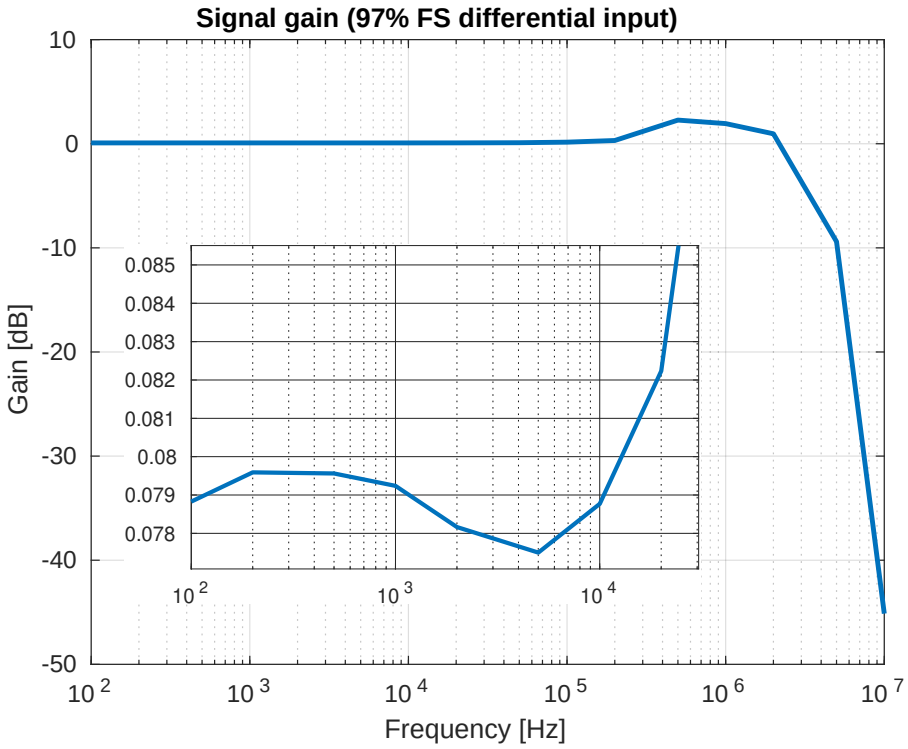


Figure 5.9: Measured STF gain over frequency

5.5 STF and alias rejection

In Figure 5.9, an almost full-scale sinusoid (-0.26dBFS, 0.775V_{pk}) is applied at the input sweeping the frequency from 100Hz to 20MHz. The inlay shows that the in-band gain variation is less than 0.01dB. The STF exhibits a 2dB out-of-band peaking characteristic of CTDSMs.

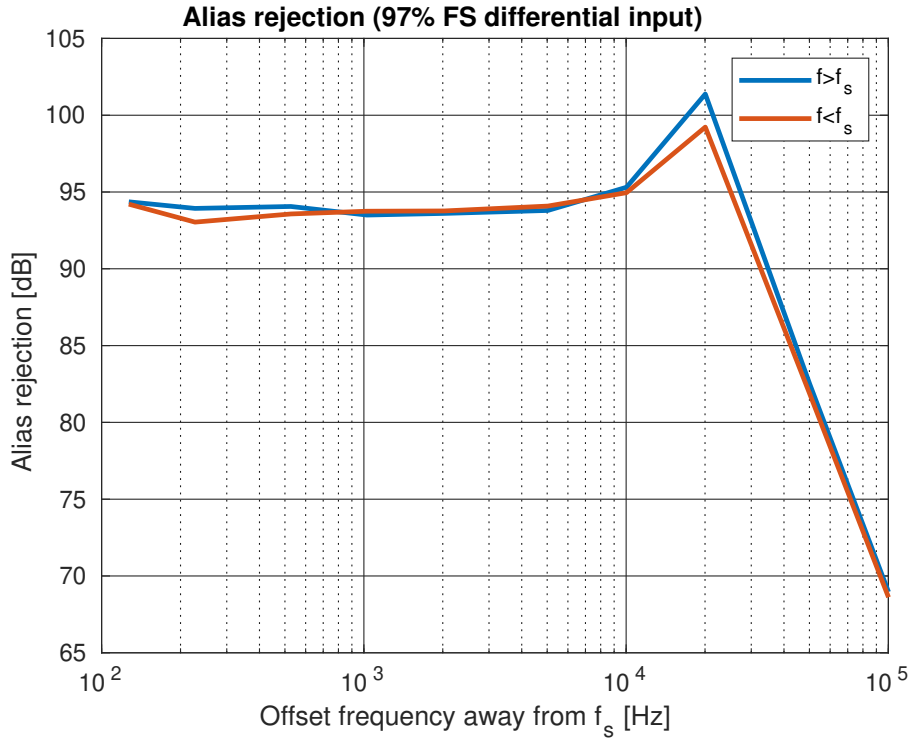


Figure 5.10: Measured Alias rejection around f_s

In Figure 5.10 an almost full-scale sinusoid (-0.26dBFS, 0.775V_{pk}) is applied at the input and its frequency is swept around $f_s = 20.48$MHz, with an offset frequency from 100Hz to 20MHz above and below f_s. The measured in-band alias rejection is roughly 94dB. Interestingly, the alias rejection goes up to 100dB around 20kHz, the cause of this behavior remains unknown.

5.6 Offset and idle tones

In Figure 5.11, the offset of 4 chip samples is measured. The input of the DSM is shorted and the bitstream is averaged for 2^{25} bits. It is observed that in all cases, the offset is negative, which indicates some asymmetry in the design. After chopping at f_s, the absolute value of the offset is higher than after chopping at $f_s/2$. This is due to different charge injection due to the mismatch between chopper switches.

In Figure 5.12, we observe idle channel tones when the input is shorted. By applying a small offset at the input, the frequency of the idle tones changes. Because changing the chopping frequency changes the offset, the idle tones also change with the chopping frequency.

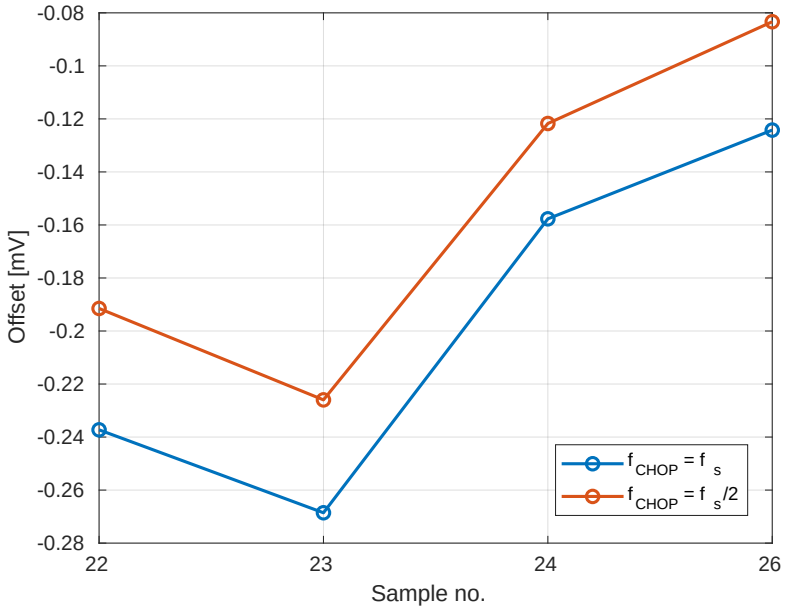


Figure 5.11: Measured offset for 4 chip samples

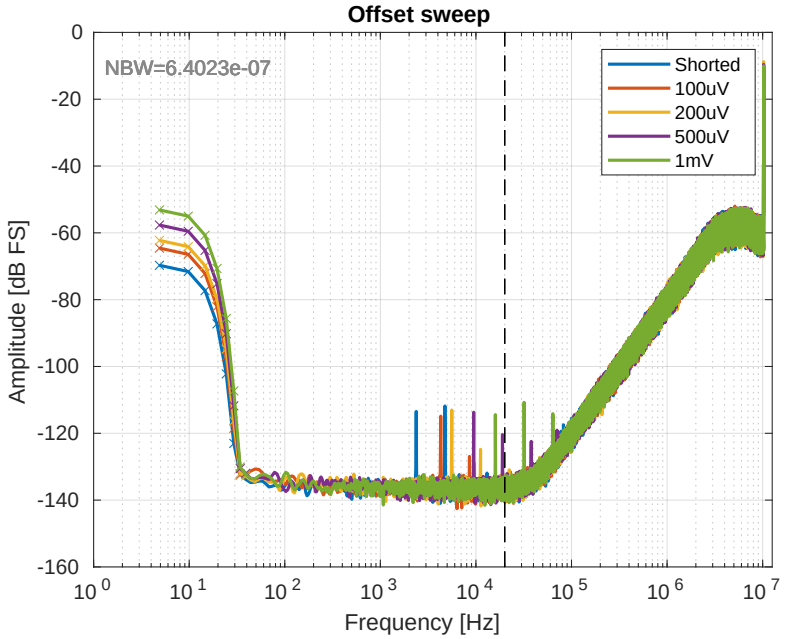


Figure 5.12: Measured idle tones

Chapter 6

Conclusion

In Table 6.1, the measured performance of the chip as measured in the lab is compared with state-of-the-art designs. This design is noticeably lower in terms of FOM (SNDR and DR). The primary hypothesis is that the FOM is lower than predicted due to jitter in the sampling clock.

However, the primary goal of this thesis, which is achieving more than 180dB FOM with a passive input stage, has been achieved. Furthermore, this thesis proposes a previously unreported loop filter topology with a single OTA, which considerably simplifies the design process, and has been proven to work as expected.

6.1 Main findings

We begin analyzing a second-order CTDSM with a *Fully Passive* loop filter. We found that it is not practically realizable for high-resolution, power-efficient applications because of the area and thermal noise constraints. Due to the lack of gain in the loop filter, the resistors must be small enough to not introduce too much thermal noise. Because of this, the capacitors must be large to make the loop filter poles close to DC. Typically to keep the area within practical limits, one of the poles is allowed to be out of band. The resulting design is not scalable because the out-of-band poles give a sub-optimal NTF, which necessitates a high OSR to meet the SQNR and intrinsic distortion requirements. Increasing the OSR reduces the swing at the input of the comparator, and the noise of the comparator must then be small compared to its input swing to keep the loop stable.

A first improvement comes by replacing the second-stage resistor with an OTA, which we refer to here as *Passive-RC OTA* topology. The gain of the OTA reduces the input-referred noise of the second stage and increases the voltage swing at the

Table 6.1: Comparison with state-of-the-art audio DSMs

	This work (TRL ON)	Lee [40] ISSCC 2022	Lo [41] ISSCC 2021	Mondal [42] ISSCC 2021	Eland [43] VLSI 2020
Process [nm]	**16**	180	28	65	160
Supply [V]	**0.8**	1.8/1.1	1.8/1.0	1.2	1.8
Area [mm^2]	**0.155**	0.0375	0.07	0.39	0.27
Architecture	**CT Single-OTA**	DT PPD	CT GLCOT	CT OTA Stack	DT Zoom
f_s [MHz]	**20.48**	5.8	6.144	7.2	3.5
BW [kHz]	**20**	20	24	24	20
Power [uW]	**88.8**	203.5	116	139	440
Peak SNR [dB]	**100.4**	106.7	-	102.0	107.5
Peak SNDR [dB]	**97.61**	105.4	100.6	100.9	106.5
DR [dB]	**99.46**	108.8	104.4	104.8	109.8
FoM SNDR [dB]	**181.16**	185.3	183.7	183.3	183.1
FoM DR [dB]	**182.99**	188.7	187.5	187.2	186.4

input of the comparator, putting less stress on the comparator noise requirement. The second pole can be easily located in-band because it depends on the large output resistance of the OTA. However, the pole of the input RC stage is still limited by thermal noise, and to lower this pole, the only alternative is to increase C. Even if we accept using more area to increase C, lowering the first-stage pole will exacerbate the noise of the OTA. The noise shaping is not optimal and this circuit still needs a high OSR.

A newly proposed loop filter topology, named *Single-OTA Resonator* breaks the main limitations of the previously known topologies. First, it allows making the loop filter poles complex conjugated, creating an in-band zero in the NTF. This results in the optimal NTF, which up to now was reported only with conventional Active-RC integrators. Hence, the noise-shaping properties are the same as a conventional CTDSM. Secondly, the mentioned poles can be made in-band without increasing the area of the capacitors. Thirdly, the noise of the OTA is not exacerbated despite having both loop filter poles in-band. And lastly, capacitive feedforward makes the loop filter less sensitive to parasitic poles in the OTA. The result is that the new topology is simple, scalable, and power efficient.

For the previously known *Fully Passive* and *Passive-RC OTA* topologies, we have derived a theoretical analysis based on thermal noise, quantization noise, area, and power consumption, which has not been found in prior literature.

6.2 Other possible applications

In this thesis, we developed a new loop filter topology and a simple CTDSM has been fabricated as a proof of concept. However, the design can be improved in many ways to build ADCs with a wide range of specifications.

6.2.1 Insensitivity to OTA parasitic poles

The capacitive feedforward around the OTA provides a direct path for high frequencies. Due to this, the loop stability is less affected by finite bandwidth and parasitic poles of the OTA. This suggests that the Single-OTA Resonator could be useful in high-bandwidth applications.

To verify this claim, we assume that the OTA has one parasitic pole at frequency ω_g. This can be modeled by making G_m frequency dependant, replacing in the previous expressions $G_m = G_{m0}/(1 + s/\omega_g)$. In Figure 6.1, the parasitic pole frequency ω_g is swept and the Bode plots of the resulting loop filter transfer functions are shown. It can be seen that the high-frequency roll-off is still 20dB/dec, and behavioral simulations show that the DSM is stable even with OTA parasitic poles at $f_s/10$.

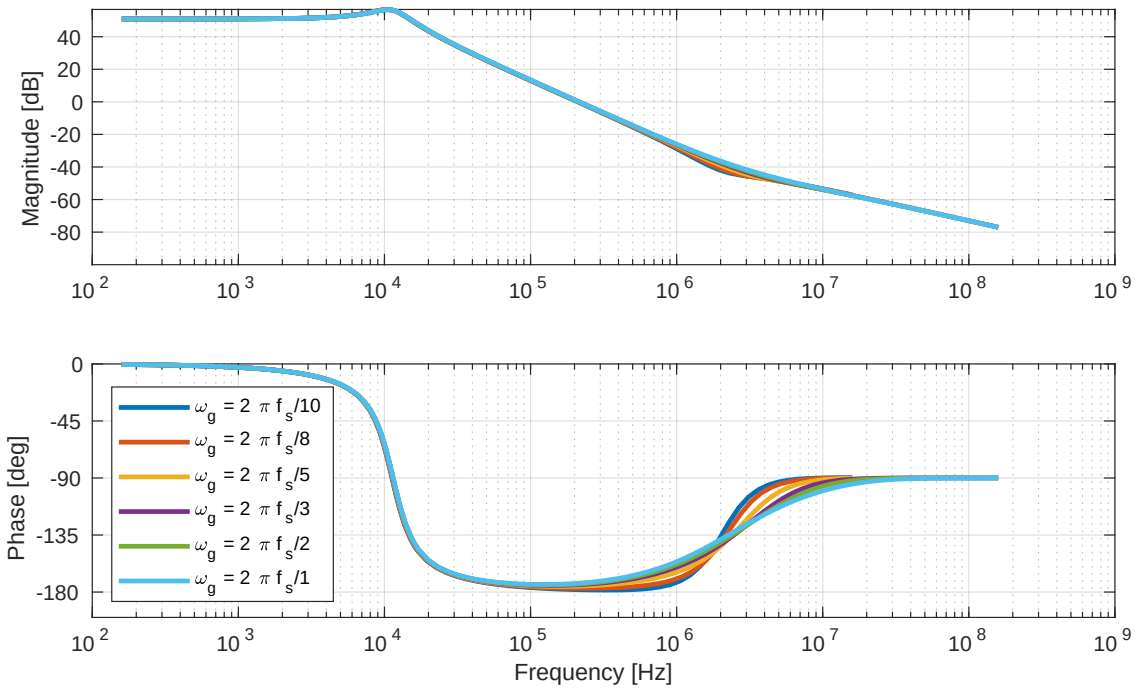


Figure 6.1: Loop filter transfer function with OTA parasitic pole

6.2.2 Third-order loop filter

Increasing the order of the loop filter will provide higher-order noise shaping, potentially reducing the in-band quantization noise and the intrinsic distortion while reducing the OSR. Because of the lower intrinsic distortion, a higher input amplitude can be tolerated, thus increasing the FOM_{SNDR}. A third-order loop filter has three poles and two zeros:

$$H_{DAC}(s) = \frac{A_0(1 + s/\omega_{z1})(1 + s/\omega_{z2})}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})(1 + s/\omega_{p3})} \tag{6.1}$$

One particular choice for the zeros, which has been shown to give a good trade-off between stability and in-band quantization noise is $\omega_{z1,2} = f_s/7.8 \times e^{\pm j\alpha_1}$ where $\alpha_1 = \pi/4$. The optimal pole frequencies for a 3rd order DSM are given in (Table 4.2. [23]). To include finite Q factor and leaky integrators we choose the poles as $\omega_{p1,2} = 0.7746 f_{BW} e^{\pm j\alpha_2}$ where $\alpha_2 = 1.52$, and $\omega_{p3} = 0.1 f_{BW}$.

In Figure 6.2 we show behavioral simulations with the above-mentioned zeros and poles, input amplitude 90% FS, dithering equal to 1% the amplitude of the loop filter output, and OSR=256.

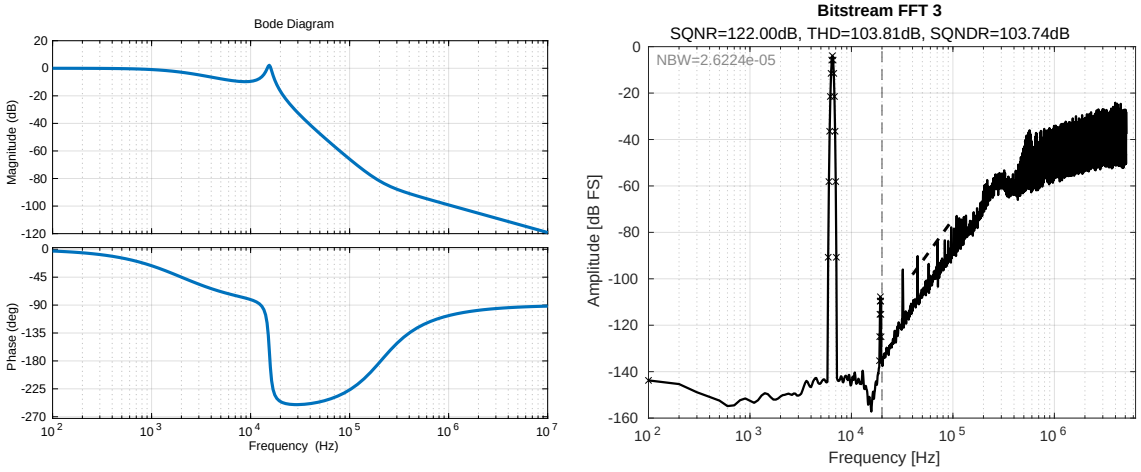


Figure 6.2: Behavioral simulations with 3rd order loop filter

Having determined the positions of the zeros and poles, the question now is how to modify the second-order Single-OTA Resonator loop filter circuit to realize the target transfer function. A pole and a zero need to be added. An obvious choice to realize another pole would be to add a G_m-C integrator at the output node V_Y. Having a high input impedance, this extra G_m-C integrator would not change the analysis of the poles from section 3.3. However, the realization of the loop filter

zeros is not so simple and requires exploration at the circuit level to find the optimal topology for a 3rd order loop filter.

6.2.3 Reducing capacitor area with FIRDAC

One of the advantages of the Single-OTA resonator topology is that the frequency of the poles can be made lower without increasing the size of the capacitors by making R_2 large, as shown in Equation 3.8. Because R_2 can be regarded as the output impedance of the OTA, it is relatively easy to make large. This could potentially allow reducing the size of capacitors C_1 and C_2 to save area.

However, one drawback of increasing R_2 and decreasing C_1, C_2 is that the OTA input swing becomes larger, potentially causing linearity problems (Equation 3.10).

To overcome this trade-off, the OTA input swing could be reduced by using an Finite Impulse Response (FIR) DAC [19] in combination with the techniques discussed in this thesis.

An FIR DAC attenuates the high frequencies of the signal that is fed by the DAC into the input of the OTA. This filtering supplements the action of the passive input stage filtering, greatly reducing the swing at node V_X despite using a smaller capacitor C_1.

Bibliography

[1] J. M. de la Rosa and R. del Río. *CMOS Sigma-Delta Converters: Practical Design Guide*. Mar. 2013. ISBN: 9781119979258. DOI: 10.1002/9781118569238.

[2] B. Murmann. *ADC Performance Survey 1997-2021*. URL: http://web.stanford.edu/~murmann/adcsurvey.html (Accessed: 10 July 2022).

[3] B. Murmann. "The Race for the Extra Decibel: A Brief Review of Current ADC Performance Trajectories". In: *IEEE Solid-State Circuits Magazine* (2015). DOI: 10.1109/MSSC.2015.2442393.

[4] H. Shibata et al. "A 9-GS/s 1.125-GHz BW Oversampling Continuous-Time Pipeline ADC Achieving -164-dBFS/Hz NSD". In: *IEEE Journal of Solid-State Circuits* (2017). DOI: 10.1109/JSSC.2017.2747128.

[5] T. Song, Z. Cao, and S. Yan. "A 2.7-mW 2-MHz Continuous-Time ΣΔ Modulator With a Hybrid Active–Passive Loop Filter". In: *IEEE Journal of Solid-State Circuits* (2008). DOI: 10.1109/JSSC.2007.914258.

[6] K. Matsukawa et al. "A Fifth-Order Continuous-Time Delta-Sigma Modulator With Single-Opamp Resonator". In: *IEEE Journal of Solid-State Circuits* (2010). DOI: 10.1109/JSSC.2010.2042244.

[7] H. Fiedler and B. Hoefflinger. "A CMOS pulse density modulator for high-resolution A/D converters". In: *IEEE Journal of Solid-State Circuits* (1984). DOI: 10.1109/JSSC.1984.1052256.

[8] U. Roettcher, H. L. Fiedler, and G. Zimmer. "A Compatible CMOS-JFET Pulse Density Modulator for Interpolative High-Resolution A/D Conversion". In: *ESSCIRC '85: 11th European Solid-State Circuits Conference*. 1985. DOI: 10.1109/ESSCIRC.1985.5468020.

[9] F. Chen and B. Leung. "A 0.25-mW low-pass passive sigma-delta modulator with built-in mixer for a 10-MHz IF input". In: *IEEE Journal of Solid-State Circuits* (1997). DOI: 10.1109/4.585244.

[10] P. Benabes and R. Kielbasa. "Passive sigma-delta converter design". In: *IMTC/2002. Proceedings of the 19th IEEE Instrumentation and Measurement Technology Conference (IEEE Cat. No.00CH37276)*. 2002. DOI: 10.1109/IMTC.2002.1006887.

[11] S. Guessab, P. Benabes, and R. Kielbasa. "A passive delta-sigma modulator for low-power applications". In: *The 2004 47th Midwest Symposium on Circuits and Systems, 2004. MWSCAS '04.* 2004. DOI: 10.1109/MWSCAS.2004.1354352.

[12] G. K. Balachandran et al. "A 1.16mW 69dB SNR (1.2MHz BW) continuous time ΔΣ ADC with immunity to clock jitter". In: *IEEE Custom Integrated Circuits Conference 2010.* 2010. DOI: 10.1109/CICC.2010.5617455.

[13] V. Srinivasan et al. "A 20mW 61dB SNDR (60MHz BW) 1b 3rd-order continuous-time delta-sigma modulator clocked at 6GHz in 45nm CMOS". In: *2012 IEEE International Solid-State Circuits Conference.* 2012. DOI: 10.1109/ISSCC.2012.6176958.

[14] J. L. A. de Melo, J. Goes, and N. Paulino. "A 0.7 V 256 μW ΔΣ modulator with passive RC integrators achieving 76 dB DR in 2 MHz BW". In: *2015 Symposium on VLSI Circuits (VLSI Circuits).* 2015. DOI: 10.1109/VLSIC.2015.7231294.

[15] J. L. A. de Melo, N. Paulino, and J. Goes. "Continuous-Time Delta-Sigma Modulators Based on Passive RC Integrators". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* (2018). DOI: 10.1109/TCSI.2018.2855649.

[16] B. Nowacki, N. Paulino, and J. Goes. "15.3 A 1V 77dB-DR 72dB-SNDR 10MHz-BW 2-1 MASH CT ΔΣM". In: *2016 IEEE International Solid-State Circuits Conference (ISSCC).* 2016. DOI: 10.1109/ISSCC.2016.7418013.

[17] D. Li et al. "Continuous-time delta-sigma modulator with an upfront passive-RC low-pass network". In: *2017 International SoC Design Conference (ISOCC).* 2017. DOI: 10.1109/ISOCC.2017.8368776.

[18] D. Li et al. "Improving Power Efficiency for Active-RC Delta-Sigma Modulators Using a Passive-RC Low-Pass Filter in the Feedback". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* (2018). DOI: 10.1109/TCSII.2017.2762325.

[19] A. Mukherjee et al. "Design Tradeoffs for a CT-ΔΣ ADC With Hybrid Active–Passive Filter and FIR DAC in 40-nm CMOS". In: *IEEE Solid-State Circuits Letters* (2020). DOI: 10.1109/LSSC.2020.3010985.

[20] B. Gönen et al. "A Low Power Continuous-Time Zoom ADC for Audio Applications". In: *2019 Symposium on VLSI Circuits.* 2019. DOI: 10.23919/VLSIC.2019.8778021.

[21] R. van Veldhoven. "A triple-mode continuous-time ΣΔ modulator with switched-capacitor feedback DAC for a GSM-EDGE/CDMA2000/UMTS receiver". In: *IEEE Journal of Solid-State Circuits* (2003). DOI: 10.1109/JSSC.2003.819165.

[22] S. Pavan. "The inconvenient truth about alias rejection in continuous time ΔΣ converters". In: *2011 IEEE International Symposium of Circuits and Systems (ISCAS)*. 2011. DOI: 10.1109/ISCAS.2011.5937618.

[23] S. Pavan, R. Schreier, and G. Temes. *Understanding Delta-Sigma Data Converters*. 2nd ed. John Wiley & Sons, Inc., 2017. ISBN: 978-1-119-25827-8.

[24] R. Schreier and B. Zhang. "Delta-sigma modulators employing continuous-time circuitry". In: *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications* (1996). DOI: 10.1109/81.488811.

[25] P. Maguire and Q. Huang. "Quantiser gain in Nth-order ΣΔ modulator linear models: its determination based on constant output power criterion". In: *1994 IEEE International Symposium on Circuits and Systems (ISCAS)*. 1994. DOI: 10.1109/ISCAS.1994.409376.

[26] E. Cheever. *SCAM: Symbolic Circuit Analysis in MATLAB*. URL: https://lpsa.swarthmore.edu/Systems/Electrical/mna/MNA6.html (Accessed: 10 July 2022).

[27] J. O. Smith. *Introduction to Digital Filters with Audio Applications. Transposed Direct Forms*. URL: https://ccrma.stanford.edu/~jos/fp/Transposed_Direct_Forms.html (Accessed: 10 Aug. 2022).

[28] B. Gönen and K. Makinwa. "The Zoom ADC: An Energy Efficient ADC for High Resolution". PhD thesis. Delft University of Technology, 2021. ISBN: 978-94-6384-229-7. DOI: https://doi.org/10.4233/uuid:5bea521a-d6ac-4f6a-b45f-d2a87fec53ed.

[29] P. Sankar and S. Pavan. "Analysis of Integrator Nonlinearity in a Class of Continuous-Time Delta–Sigma Modulators". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* (2007). DOI: 10.1109/TCSII.2007.905390.

[30] Breems, L.J. and van der Zwan, E.J. and Huijsing, J.H. "Design for optimum performance-to-power ratio of a continuous-time Σ Δ modulator". In: *Proceedings of the 25th European Solid-State Circuits Conference*. 1999.

[31] R. H. van Veldhoven and A. H. van Roermund. *Robust Sigma Delta Converters*. 2011. ISBN: 9789400706446.

[32] J. L. A. de Melo. "A low power 1-MHz continuous-time ΣΔM Using a passive loop filter designed with a genetic algorithm tool". In: *2013 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2013. DOI: 10.1109/ISCAS.2013.6571910.

[33] J. L. A. de Melo et al. "A 0.4-V 410-nW opamp-less continuous-time ΣΔ modulator for biomedical applications". In: *2014 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2014. DOI: 10.1109/ISCAS.2014.6865391.

[34] L. Somappa and M. S. Baghini. "A Compact Fully Passive Loop Filter-Based Continuous Time ΔΣ Modulator for Multi-Channel Biomedical Applications".

In: *IEEE Transactions on Circuits and Systems I: Regular Papers* (2020). DOI: 10.1109/TCSI.2019.2944272.

[35] M. Jang, C. Lee, and Y. Chae. "Analysis and Design of Low-Power Continuous-Time Delta-Sigma Modulator Using Negative-R Assisted Integrator". In: *IEEE Journal of Solid-State Circuits* (2019). DOI: 10.1109/JSSC.2018.2871111.

[36] B. Gönen et al. "A Continuous-Time Zoom ADC for Low-Power Audio Applications". In: *IEEE Journal of Solid-State Circuits* (2020). DOI: 10.1109/JSSC.2019.2959480.

[37] S. Pan and K. A. A. Makinwa. "A 10 fJ·K^2 Wheatstone Bridge Temperature Sensor With a Tail-Resistor-Linearized OTA". In: *IEEE Journal of Solid-State Circuits* (2021). DOI: 10.1109/JSSC.2020.3018164.

[38] S. Billa, A. Sukumaran, and S. Pavan. "Analysis and Design of Continuous-Time Delta–Sigma Converters Incorporating Chopping". In: *IEEE Journal of Solid-State Circuits* (2017). DOI: 10.1109/JSSC.2017.2717937.

[39] B. Razavi. "The StrongARM Latch [A Circuit for All Seasons]". In: *IEEE Solid-State Circuits Magazine* (2015). DOI: 10.1109/MSSC.2015.2418155.

[40] C. Y. Lee and U.-K. Moon. "A 0.0375mm2 203.5µW 108.8dB DR DT Single-Loop DSM Audio ADC Using a Single-Ended Ring-Amplifier-Based Integrator in 180nm CMOS". In: *2022 IEEE International Solid- State Circuits Conference (ISSCC)*. 2022. DOI: 10.1109/ISSCC42614.2022.9731606.

[41] C. Lo et al. "10.1 A 116μ W 104.4dB-DR 100.6dB-SNDR CT ΔΣ Audio ADC Using Tri-Level Current-Steering DAC with Gate-Leakage Compensated Off-Transistor-Based Bias Noise Filter". In: *2021 IEEE International Solid- State Circuits Conference (ISSCC)*. 2021. DOI: 10.1109/ISSCC42613.2021.9365807.

[42] S. Mondal, O. Ghadami, and D. A. Hall. "10.2 A 139 µ W 104.8dB-DR 24kHz-BW CT ΔΣM with Chopped AC-Coupled OTA-Stacking and FIR DACs". In: *2021 IEEE International Solid- State Circuits Conference (ISSCC)*. 2021. DOI: 10.1109/ISSCC42613.2021.9366002.

[43] E. Eland et al. "A 440μW, 109.8dB DR, 106.5dB SNDR Discrete-Time Zoom ADC with a 20kHz BW". In: *2020 IEEE Symposium on VLSI Circuits*. 2020. DOI: 10.1109/VLSICircuits18222.2020.9162856.

Appendix A

Optimal loop filter zero for a 2nd order CTDSM

The frequency of the loop filter zero in a 2nd order CTDSM gives a trade-off between quantization noise and stability. This is equivalent to choosing the 1st-order coefficient in a 2nd order DTDSM, an empirical optimum was proposed in a classic paper [1]. Using the impulse invariant method, we can translate this optimal coefficient into an angular frequency for a CTDSM loop filter zero.

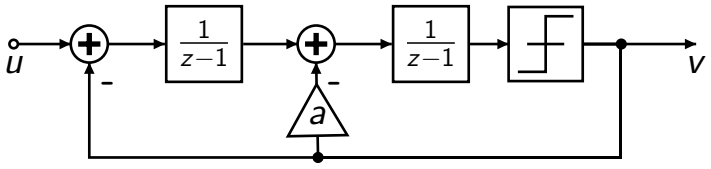


Figure A.1: Block diagram of a 2nd order DTDSM

Ignoring static gain that does not affect the result for a 1-bit quantizer, the loop filter transfer function from Figure A.1 is:

$$H_{DAC}(z) = \frac{az - a + 1}{(z-1)^2} \tag{A.1}$$

On the other hand, a CTDSM with both poles at DC has this loop filter transfer function:

$$H_{DAC}(s) = \frac{(1 + s/\omega_z)}{s^2} \tag{A.2}$$

Assuming a NRZ DAC pulse shape with impulse response $(1 - e^{sT_s})/s$, the discrete-time equivalent of Equation A.2 derived by the impulse invariant method is:

$$H_{DAC}(z) = (1 - z^{-1})\mathcal{Z}_{T_s}\left\{\mathcal{L}^{-1}\left[\frac{H(s)}{s}\right]\right\} \tag{A.3}$$

We begin by solving the inverse Laplace transform:

$$\mathcal{L}^{-1}\left[\frac{1 + s/\omega_z}{s^3}\right] = \mathcal{L}^{-1}\left[\frac{1}{s^3} + \frac{1}{\omega_z s^2}\right] = \frac{t^2}{2} + \frac{t}{\omega_z} \tag{A.4}$$

The resulting impulse response is sampled at $t = nT_s$ and its Z-transform is found by:

$$\mathcal{Z}_{T_s}\left\{\frac{(nT_s)^2}{2} + \frac{(nT_s)}{\omega_z}\right\} = \frac{1}{2}\frac{T_s^2 z^{-1}(1 + z^{-1})}{(1 - z^{-1})^3} + \frac{1}{\omega_z}\frac{T_s z^{-1}}{(1 - z^{-1})^2} \tag{A.5}$$

From Equation A.3 and Equation A.5:

$$H_{DAC}(z) = \frac{T_s}{(z-1)^2}\left(\frac{T_s}{2}(z+1) + \frac{1}{\omega_z}(z-1)\right) \tag{A.6}$$

Equating the zeros of the numerator from Equation A.1 and Equation A.6:

$$\omega_z = \frac{1}{T_s(a - 1/2)} = \frac{f_s}{a - 1/2} \tag{A.7}$$

The modulator proposed in [1] has a coefficient a=2 and is widely accepted as an optimum, which translates to $\omega_z = f_s/1.5$. A higher zero frequency gives more out of band gain (OBG), the inband quantization noise improves, but the maximum stable amplitude (MSA) deteriorates.

References

[1] Boser, B.E. and Wooley, B.A. "The design of sigma-delta modulation analog-to-digital converters". In: *IEEE Journal of Solid-State Circuits* (1988). DOI: 10.1109/4.90025.

Appendix B

Analysis of a 2nd-order RC lowpass network

The trade-offs between frequency response, noise, and power consumption of a fully passive 2nd order loop filter are analyzed in this section.

To simplify the analysis, R_3 is neglected because being small, its noise contribution is usually much less than that of R_1 and R_2. Furthermore, the effect of the zero has little influence on the inband thermal noise. The circuit from Figure B.1 has the same poles as the loop filter described in section 3.1.

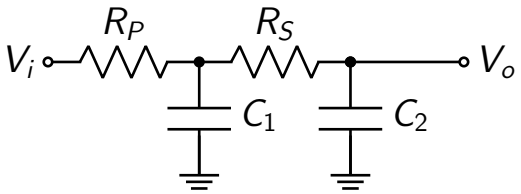


Figure B.1: A 2nd-order RC lowpass filter

The transfer function of the circuit can be mapped to the transfer function of a general second-order system with two poles:

$$H(s) = \frac{1}{1 + s(C_2[R_S + R_P] + C_1R_P) + s^2C_1C_2R_SR_P} = \frac{1}{1 + s/(\omega_0 Q) + (s/\omega_0)^2} \tag{B.1}$$

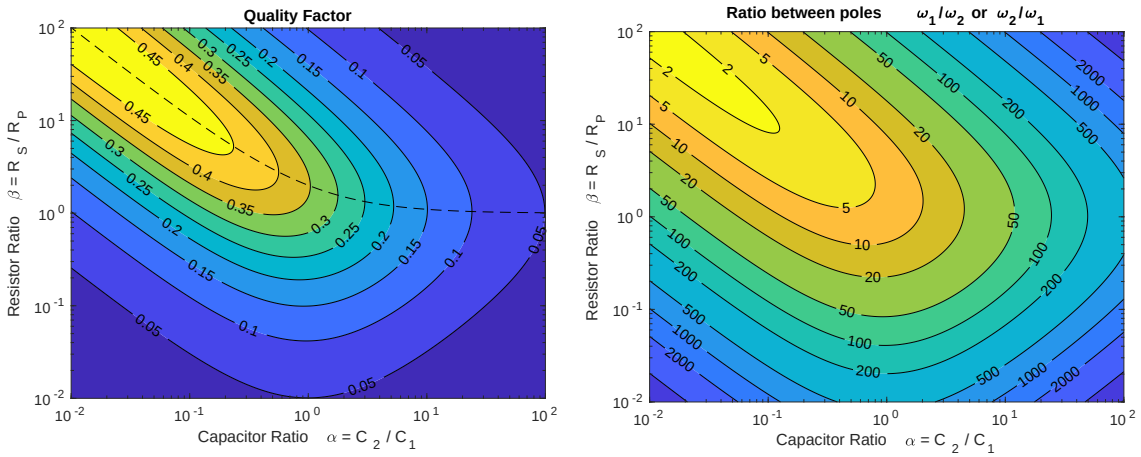
where ω_0 is the geometric mean of the poles and Q is the quality factor:

$$\omega_0 = \frac{1}{\sqrt{C_1C_2R_PR_S}} \qquad Q = \frac{\sqrt{C_1C_2R_PR_S}}{C_2[R_S + R_P] + C_1R_P} \tag{B.2}$$

Without loss of generality, setting $C_2 = \alpha C_1$ and $R_S = \beta R_P$:

$$\omega_0 = \frac{1}{C_1 R_P \sqrt{\alpha\beta}} \qquad Q = \frac{\sqrt{\alpha\beta}}{\alpha\beta + \alpha + 1} \tag{B.3}$$

The quality factor is determined only by the ratio of resistors and capacitors. It approaches 0.5 when $R_S > R_P$ and $C_2 < C_1$, always being less than 0.5 because the circuit is fully passive (Figure B.2a).



(a) Quality factor

(b) Pole ratio

Figure B.2: Quality factor and pole ratio for a 2nd order lowpass RC network

The ratio between the poles $R = \omega_1/\omega_2$ can be derived from the expression:

$$\frac{1}{Q\omega_0} = \frac{1}{Q\sqrt{\omega_1\omega_2}} = \frac{1}{\omega_1} + \frac{1}{\omega_2} \rightarrow Q = \frac{\sqrt{R}}{1+R} \tag{B.4}$$

Using the change of variable $R = e^M$:

$$Q = \frac{e^{M/2}}{1+e^M} = \left[2\cosh\left(\frac{M}{2}\right)\right]^{-1} \rightarrow R = e^{2\cosh^{-1}(\frac{1}{2Q})} \tag{B.5}$$

To make the poles close to each other, Q must be high. At the limit, both poles are at the same frequency when Q approaches 0.5, as illustrated in Figure B.2b.

For appropriate noise shaping, the poles must be at low frequency. Ideally, both poles should be in-band ($f < f_{BW}$), but for high-resolution and low-bandwidth this would require extremely large capacitors, not suitable for chip integration. Therefore, one pole is allowed to be out-of-band ($f > f_{BW}$), accepting that a higher OSR may

be used to reach the desired SQNR. At least one of the poles must be in-band, otherwise, the dead-band behavior would heavily degrade the ADC performance.

We conclude that ω_0 must be on the same order of magnitude as $2\pi f_{BW}$ so that at least one of the poles is in-band, but not too low because that would make capacitors too large and increase the effective gain of the comparator more than strictly needed, reducing the input swing and making comparator design challenging. In addition, $Q > 0.3$ so that the separation between poles is not more than one decade. In practice, ω_0, Q, and OSR must be determined by simulations to account for intrinsic distortion. In the remainder of this analysis, we shall assume that ω_0 and Q have been determined beforehand and focus now on the question of how to choose C_1, R_P, α and β.

From Equation B.3 and Figure B.2 it can be observed that a given quality factor Q may be achieved by different combinations of α and β. Is there an optimum choice that minimizes power consumption, thermal noise, and area?

The input-referred thermal noise power of R_P and R_S integrated over the bandwidth f_{BW} is given in Equation B.6.

$$v_{\mathrm{n,in}}^2 = 4kTf_{\mathrm{BW}}R_P\left[1+\beta\left(1+\frac{(2\pi f_{\mathrm{BW}})^2}{3\omega_P^2}\right)\right] \tag{B.6}$$

When the frequency defined by $\omega_P = (R_P C_1)^{-1}$ is higher than $2\pi f_{BW}$, Equation B.6 reduces to $v_{\mathrm{n,in}}^2 \approx 4kTf_{BW}R_P(1+\beta)$, being higher otherwise. We conclude that if one of the poles has to be out-of-band, it is better to do so with the pole formed by R_P and C_1 or equivalently, $\alpha\beta > 1$.

Assuming $R_{IN} = R_{DAC}$, the power of the DAC is $V_{DD}^2/(2R_P)$. If $\alpha\beta > 1$, the thermal noise power is approximately $16kTf_{BW}R_P(1+\beta)$. The Schreier FoM is proportional to $(\text{Power} \times \text{Noise})^{-1} = (1+\beta)^{-1}$. So for a good FoM, β must be kept small. In order to maintain the assumption $\alpha\beta > 1$, α must be maximised.

It is observed that there is a maximum α for a given Q (dashed line in Figure B.2b). This can be found by equating to zero the partial derivative of Q with respect to the variable β (Equation B.7).

$$\frac{\partial Q}{\partial \beta} = 0 \rightarrow 1+\alpha-\alpha\beta = 0 \rightarrow \alpha_{\max} = \frac{1}{(2Q)^2} - 1 \tag{B.7}$$

The total capacitor area is proportional to $C_1(1+\alpha)$. So, unfortunately, increasing α to obtain a better FoM also increases the area. Note that along this line, $\beta > 1$, implying at least a 6dB degradation in the FoM because $R_S > R_P$.

Appendix C

Optimal noise partition in a Passive RC-OTA input stage

The input-referred thermal noise of the loop filters described in section 3.2 and section 3.3 originates mostly from the R_{IN}, R_{DAC} and the OTA.

$$N_{TH} = N_{DAC} + N_{OTA} \tag{C.1}$$

The total input-referred thermal noise N_{TH} must be kept below a certain value to reach the desired SNDR. In this section we derive the partition of the noise between N_{DAC} and N_{OTA} that minimizes power consumption.

C.1 Power-Noise efficiency of an OTA

In this section, we first study the relationship between supply current I_{VDD} and transconductance G_m of an OTA. Next, we observe the relationship between the input-referred noise of an OTA $v^2_{n,OTA}$ and its transconductance G_m. Combining the two, we define a paratmeter η that relates the input-referred noise to the power consumption of the OTA.

Transconductance efficiency (g_m/I_D) is a useful design parameter of a transistor that determines a trade-off between speed and power efficiency. We may generalize this concept defining the transconductance efficiency of a complete OTA as the ratio between its transconductance and the power drawn from the supply (G_m/I_{VDD}).

The ratio $\epsilon = (G_m/I_{VDD})/(g_m/I_D)$ depends on the topology used. Assuming all transistors have the same current density, and neglecting the power of CMFB

and bias circuits, the highest efficiency can be reached with a current-reuse topology ($\epsilon \approx 1/2$), followed by telescopic ($\epsilon \approx 1/4$) and folded cascode ($\epsilon \approx 1/8$) topologies.

The input-referred noise of a transistor is $v_n^2 = 4kT\gamma/g_m$, where γ is a parameter that depends on the technology and the type of device. Assuming the OTA is driven by a relatively low-impedance, we may generalize this concept to a complete OTA:

$$v_{n,OTA}^2 = \frac{4kT\,\Gamma_{OTA}}{G_m} \tag{C.2}$$

Where Γ_{OTA} again depends on the topology of the OTA, the technology parameters γ_p and γ_n, and the individual g_m's of the transistors. Assuming all transistors have the same current density, $\gamma_p = \gamma_n = 1$ and neglecting the noise of the CMFB circuit, the lowest noise factor is achieved by a current-reuse OTA topology ($\Gamma_{OTA} \approx 1$), followed by telescopic ($\Gamma_{OTA} \approx 2$) and folded cascode ($\Gamma_{OTA} \approx 16$) topologies.

We now define a parameter η, combining the two concepts explained before, that relates the power consumption of an OTA $P_{OTA} = V_{DD}I_{VDD}$ to its input-referred noise voltage $v_{n,OTA}^2$:

$$\eta = v_{n,OTA}^2 P_{OTA} = 4kT\,\Gamma_{OTA}\,V_{DD}\left(\frac{I_{VDD}}{G_m}\right) = \frac{4kT\,\Gamma_{OTA}\,V_{DD}}{\epsilon(g_m/I_D)} \tag{C.3}$$

C.2 Input-referred noise of the loop filter

For simplicity, we assume that $R_{IN} = R_{DAC} = 2R_P$. The thermal noise from the OTA referred to the input of the loop filter is:

$$N_{OTA} = \int_0^{2\pi f_{BW}} 4v_{n,OTA}^2\,|1 + j\omega C_1 R_P|^2\,d\omega \tag{C.4}$$

The frequency determined by R_{IN}, R_{DAC} and C_1 is usually higher than the bandwidth f_{BW}, because the resistors and the capacitor cannot be too big, due to thermal noise and chip area considerations. Hence, the term $|1 + j\omega C_1 R_P|^2 \approx 1$ within the band of interest, and the integrated noise power is approximated as:

$$N_{OTA} \approx 4v_{n,OTA}^2 f_{BW} \approx \frac{16kT\,\Gamma_{OTA}}{G_m} f_{BW} \tag{C.5}$$

From section 2.3 the input-referred integrated thermal noise of the DAC resistors assuming $R_{\mathrm{IN}} = R_{\mathrm{DAC}}$ is:

$$N_{DAC} = 8kTf_{BW}R_{IN} \tag{C.6}$$

The ratio of noise powers is:

$$\alpha = \frac{N_{DAC}}{N_{OTA}} = \frac{R_{IN}G_m}{2\Gamma_{OTA}} \tag{C.7}$$

The total input-referred thermal noise is:

$$N_{TH} = N_{DAC} + N_{OTA} = N_{DAC}\left(1 + \frac{1}{\alpha}\right) = N_{OTA}(1+\alpha) \tag{C.8}$$

Hence the required input (and DAC) resistor to meet the noise requirements is:

$$R_{IN} = \frac{N_{TH}}{8kTf_{BW}}\left(1 + \frac{1}{\alpha}\right)^{-1} \tag{C.9}$$

And the G_m required to meet the noise requeriments is:

$$G_m = \frac{16kT\,\Gamma_{OTA}f_{BW}}{N_{TH}(1+\alpha)} \tag{C.10}$$

C.3 Loop filter power consumption

The power consumption of the OTA can be estimated from the current drawn from V_{DD}:

$$P_{OTA} = V_{DD}I_{VDD} = \frac{V_{DD}G_m}{\epsilon(g_m/I_D)} \tag{C.11}$$

Still assuming that $R_{IN} = R_{DAC}$ the power consumption of the DAC resistor can be estimated as:

$$P_{DAC} = \frac{V_{DD}^2}{R_{DAC}} = \frac{V_{DD}^2}{R_{IN}} \tag{C.12}$$

The total power consumption is $P_{VDD} = P_{DAC} + P_{OTA}$. Rearranging and replacing $G_m = (2\Gamma_{OTA}\alpha)/R_{IN}$ from Equation C.7:

$$P_{VDD} = \frac{V_{DD}^2}{R_{IN}} \left[1 + \frac{\alpha 2 \Gamma_{OTA}}{\epsilon (g_m/I_D) V_{DD}} \right] \tag{C.13}$$

Replacing R_{IN} from Equation C.9:

$$P_{VDD} = \frac{V_{DD}^2 8kTf_{BW}}{N_{TH}} \left(1 + \frac{1}{\alpha} \right) \left[1 + \frac{\alpha 2 \Gamma_{OTA}}{\epsilon (g_m/I_D) V_{DD}} \right] \tag{C.14}$$

Finding the optimum by $\partial P_{VDD}/\partial \alpha = 0$:

$$\alpha_{OPT} = \sqrt{\frac{\epsilon (g_m/I_D) V_{DD}}{2 \Gamma_{OTA}}} \tag{C.15}$$

Filling in the values for a Current-Reuse OTA, which is the most efficient, $\epsilon = 1/2$ and $\Gamma_{OTA} = 1$ and the typical values used in this project $(g_m/I_D) = 20\text{V}^{-1}$ and $V_{DD} = 0.8\text{V}$:

$$\alpha_{OPT} \approx 2 \tag{C.16}$$

Consider the power consumption under the conditions for the maximum theoretical $\text{FOM}_{\text{SNDR}} = 192\text{dB}$, that is when the OTA noise and power are zero:

$$P_{VDD,IDEAL} = \frac{V_{DD}^2 8kTf_{BW}}{N_{TH}} \tag{C.17}$$

The degradation of FOM_{SNDR} due to using a G_m stage can be quantified by the ratio of power consumptions:

$$\frac{P_{VDD}}{P_{VDD,IDEAL}} = \left(1 + \frac{1}{\alpha_{OPT}} \right)^2 \approx 3.52\text{dB} \tag{C.18}$$

Despite using a G_m stage, this degradation in FOM_{SNDR} is lower than the best-case 6dB degradation when using an amplifer-less loop filter. Furthermore, the gain provided by the G_m stage increases the voltage swing at the input of the comparator, simplifying its design.