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A Hybrid Magnetic Current Sensor With a Multiplexed Ripple-Reduction Loop

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***Abstract*— This article presents a hybrid magnetic current sensor for galvanically isolated measurements. It consists of a CMOS chip that senses the magnetic field generated by current flowing through a lead-frame-based current rail. Hall plates and coils are used to sense low-frequency (dc to 10 kHz) and high-frequency (10 kHz to 5 MHz) magnetic fields, respectively. With the help of on-chip calibration coils, the biasing current of the Hall plates is trimmed to match the sensitivity of the Hall and coil signal paths. The sensitivity drift of the coil path with temperature is compensated by using temperature-dependent gain-setting resistors, while the drift of the Hall path is compensated by biasing the Hall plates with a proportional-to-absolute-temperature (PTAT) current. The resulting sensitivity drift is less than 9% from –40 °C to 80 °C. The offset of the Hall plates is reduced by the current spinning technique, and the resulting ripple is suppressed by a multiplexed ripple-reduction loop (MMRL). Fabricated in a standard 0.18-μm CMOS process, the current sensor occupies 4.6 mm^2 and draws 7.8 mA from a 1.8-V supply. It achieves a gain variation of only ±2% in a 5-MHz BW. It also achieves high energy efficiency, with an figure of merit (FoM) of 1.6 fW/Hz.**

***Index Terms*— Galvanic isolation, hybrid current sensors, magnetic current sensing, ripple-reduction loop (RRL), temperature compensation, wide bandwidth.**

I. Introduction

INTEGRATED magnetic current sensors are widely used to control power converters, for motor health monitoring and in automotive electronics. Although shunt-based current sensors achieve high accuracy [1], [2], [3], [4], magnetic current sensors are preferred in high-power applications due to their inherent galvanic isolation and low insertion loss [5]. Furthermore, their wide intrinsic bandwidth (BW > 1 MHz) makes them well suited for sensing switching transients and short-circuit currents [6], [7].

Magnetic current sensors can be realized with the help of fluxgates and magnetoimpedance sensors [8], [9], [10], [11]. However, these cannot be implemented in standard CMOS technology, which increases their manufacturing cost. Furthermore, they have a limited linear input range and so are often used in closed-loop current sensing schemes, which then have limited BWs (<200 kHz). In [8], a current sensor based on a CMOS chip and a co-packaged integrated fluxgate (IFG) is presented. To keep the IFG in its linear operating region, the external magnetic field is locally canceled by a co-integrated compensation coil. The sensor achieves a resolution of 11 mA_{rms} in a 125-kHz BW and exhibits an input-dependent power consumption (100 mW at $B_{in} = 2$ mT).

Magnetic current sensors based on Hall plates can provide CMOS compatibility, low fabrication cost, and high linearity over a wide range [5], [12], [13], [14], [15]. Recently, the use of X-Hall sensors [13], [16], as well as the combination of a spinning-current Hall sensor and an un-spun Hall sensor [17], has been proposed as ways to extend their BW (up to 11.6 MHz [16]). However, this comes at the expense of resolution, due to the fundamental tradeoff between their thermal noise and their BW. In contrast, the differentiating characteristic of on-chip coils means that they can achieve much wider BW and higher resolution [17], [18], [19], but they cannot sense dc signals.

Combining Hall plates and coils enables the realization of CMOS-compatible hybrid sensors, which can achieve both wide BW and high resolution [17], [18], [19], [20], [21]. In [17] and [21], a hybrid sensor is used to detect the differential magnetic field produced by a current-carrying copper trace. However, its front end senses coil voltage, which limits its dynamic range (DR) at high frequencies. It also employs a large off-chip capacitor (10 μF) to suppress the dc offset of the coil path, which would otherwise contribute significant error to the dc-sensing Hall path. The sensor achieves a resolution of 480 mA_{rms} in a 3-MHz BW while consuming 38.5 mW.

In [19], a hybrid sensor based on a vertical Hall plate and a single optimized Rogowski coil is presented. It also senses coil voltage but achieves a wider BW (15.3 MHz). To obtain a flat frequency response, it employs a two-stage integrator with an on-chip pole-zero cancellation scheme. However, it requires trimming to compensate for pole-zero mismatch. Moreover, the outputs of the coil and Hall paths are combined by an off-chip crossover network. Compared to [17], it consumes more power (63.4 mW) and achieves worse resolution (710 mA_{rms}).

In [18], a hybrid current sensor senses coil current rather than coil voltage. It employs a two-stage low-pass filter (LPF) and a robust pole-zero cancellation scheme to suppress coil-path offset and sensitivity drift with temperature.

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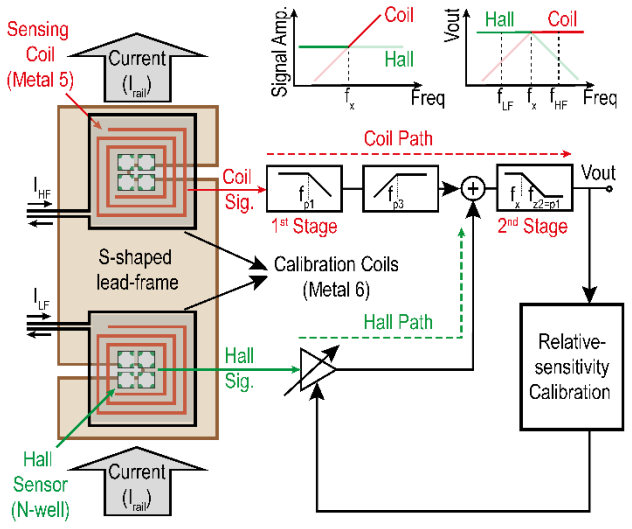

Fig. 1. Simplified system block diagram including the off-chip relative-sensitivity calibration scheme.

Compared to [17] and [19], it achieves 7.5× better resolution (64 mA_{rms}) and 2× less power dissipation (19.5 mW). However, the use of the spinning-current technique to reduce Hall plate offset causes a significant residual ripple, which is ∼4× larger than its resolution. In addition, the sensitivity of the Hall path is trimmed manually to match that of the coil path.

This article presents a hybrid magnetic current sensor that employs differential (gradiometric) coils and Hall plates to sense the magnetic field produced by a current-carrying lead frame. As in [18], a robust pole-zero cancellation scheme is used to suppress the offset of the coil path, while its sensitivity drift over temperature is compensated with the help of temperature-dependent gain-setting resistors. In contrast to [16], a multiplexed ripple-reduction loop (MRRL) is used to significantly suppress spinning ripple, while a proportional-to-absolute-temperature (PTAT) bias current compensates for the sensitivity drift of the Hall plates. Finally, the sensitivity of the Hall and coil paths is accurately matched by trimming the bias current of the Hall plates with the help of on-chip calibration coils.

This article is organized into three more sections. The proposed system, including the system architecture, the temperature compensation in both coil path and Hall path, the design of the MRRL, and the self-calibration scheme, is presented in Section II. Section III shows and discusses the measurement results. Finally, this article ends with conclusions.

II. Proposed Hybrid Magnetic Current Sensor

A. System Architecture

Fig. 1 shows a block diagram of the proposed current sensor. It consists of a CMOS chip mounted on an S-shaped current rail. The low-resistance (250 $\mu\Omega$) S-shaped lead frame concentrates the magnetic field seen by two coil/Hall plate pairs [18]. In addition, the current rail facilitates the use of a differential sensing scheme that rejects homogeneous interference, e.g., the Earth's magnetic field [17]. Each n-well Hall plate consists of four sub-plates connected in parallel, whose bias currents flow in four different directions to reduce their combined offset and sensitivity to mechanical stress [22]. In contrast to [18], the Hall plates are not stacked, which leads to higher sensitivity and lower offset and enables operation from a single 1.8-V supply. Since the induced coil current is proportional to frequency, the coil path is designed to have an integrating characteristic, which is realized by a two-stage pole-zero cancellation scheme [18], [19], [20]. The first stage is an LPF with a pole at f_{p1}, and the second stage introduces another pole at f_x together with a zero at f_{z2}. This zero cancels the pole of the first stage (f_{p1}), thus turning the coil path into a first-order LPF with a pole f_{p2} (= f_X) that defines the crossover frequency from the Hall to the coil paths. To suppress the offset of the first and second stages of the coil path, these stages are connected by an ac-coupling capacitor, which creates a parasitic pole at f_{p3}.

The output of the Hall plate is simply amplified and then added to the input of the coil path's second stage. In order to achieve a flat frequency response, the sensitivity of the Hall path must be adjusted to match the sensitivity of the coil path at f_x. As in [18], this is done by trimming the bias current of the Hall plates. The sensitivity of the coil and Hall path can be accurately determined by injecting known input currents I_{HF} (at $f_{HP} > f_X$) and I_{LF} (at $f_{LP} < f_X$) into two calibration coils located around the coil and Hall plates (Fig. 1).

A simplified schematic of the two sensor paths is shown in Fig. 2. As in [18], the coil path consists of two stages. The input stage reads out the coil current and implements a pole f_{p1} = 200 kHz ($1/2\pi R_1C_1$), thus limiting its output swing at higher frequencies. Compared to reading out the coil voltage, this approach greatly relaxes the design of the input stage.

As mentioned earlier, the 1st stage contributes a pole f_{p1}, while the 2nd stage contributes a pole f_{p2} ($1/2\pi R_4C_3$) = 10 kHz and a zero f_{z2} ($1/2\pi R_3C_3$) = f_{p1} = 200 kHz. This results in a coil path that behaves like a 1st-order LPF with a pole at 10 kHz (= f_X). To ensure robust pole-zero cancellation, R_1C_1 and R_3C_3 are realized by the same type of components.

Although a 1st-order LPF could be implemented with a single stage, R_1 would then be very large (6 MΩ, for C_1 = 25 pF). Since the coil resistance is small (∼3 kΩ), the resulting dc gain would be quite large, causing the 1st stage to clip on its own millivolt-level offset. The two-stage architecture allows R_1 to be 20 times smaller (f_{p1} = 20 f_X), thus ensuring that the input stage does not clip. Furthermore, its output offset will be blocked by C_2.

Together with R_2, however, the presence of C_2 introduces a parasitic pole f_{p3}, which causes a dip in the overall transfer function (TF) around f_X. For a given coil path sensitivity, large capacitors are then needed to make f_{p3} as low as possible. In [16], these were realized by MIM capacitors, which occupied about 10% of the chip area. In this work, 6× larger capacitors (1.5 nF) are realized in the same area by placing MOS capacitors under the MIM capacitors. The MOS capacitors are split into two halves, which are connected in an antiparallel fashion to reduce (by 9×) their voltage-dependent non-linearity. Over process corners, the resulting 230-Hz parasitic pole causes a 2.3% dip (worst case) in the sensor's TF.

Since the outputs of the Hall plates are quite small, they are first amplified by local capacitively coupled amplifiers (CCAs)

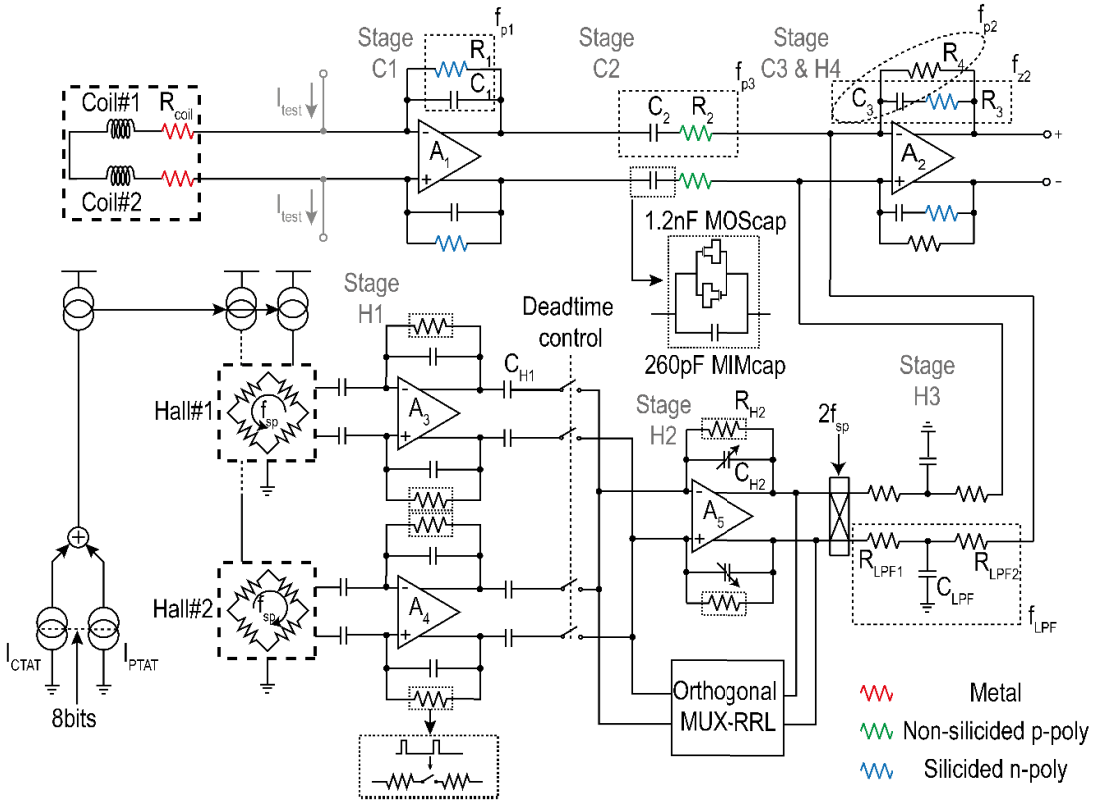

Fig. 2. Full system block diagram.

with a gain of 50 ($A_{3,4}$), as shown in Fig. 2. Their outputs are summed by another CCA (A_5) with a gain of 12 and converted back to dc by a chopper demodulator. The offset caused by spinning-induced transients is reduced by deadband switches [18]. The amplified Hall signal is then applied to the output stage via a passive *RC* LPF with a pole at f_X, which, when combined with the TF of the coil path, results in a flat TF from dc to 8 MHz (the BW of the output stage), with an in-band gain variation of less than ±2.1% (verified by Monte Carlo simulations). The Bode plots of the different stages of the coil and Hall paths are shown in Fig. 3.

B. Temperature Compensation

One drawback of Hall plates is their significant gain drift versus temperature (>20% from −70 °C to 170 °C [23]). In [23], this is compensated with the help of an on-chip temperature sensor. However, this requires (at least) a costly two-point trim. In [21], which employs a differential sensing scheme, on-chip calibration coils generate a common-mode magnetic field, with which the gain of the Hall plates can be continuously calibrated. An off-chip control loop then stabilizes their gain drift by adjusting their biasing current. This approach requires a separate readout for sensing the common-mode magnetic field and so consumes more power and chip area.

In this work, the TC of the Hall plates is approximately compensated by using a PTAT bias current (∼2.5 mA at room temperature). This current is implemented by forcing a PTAT voltage ΔV_{GS} (the difference in gate–source voltage between a pair of pMOS transistors biased at a fixed current ratio in their sub-threshold region) across a p-poly resistor.

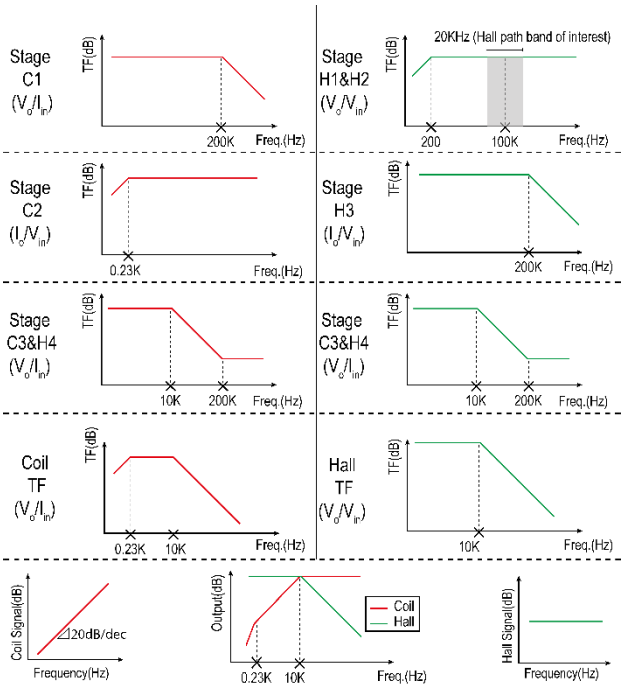

Fig. 3. TFs of different stages in the coil path (left) and Hall path (right).

The sensitivity of the coil path G_E can be expressed as

$$G_E = \begin{cases} \dfrac{R_1}{2\pi f x R_{\text{coil}} x R_2 x C_3}, & 10\text{ kHz} < f < 200\text{ kHz} \\ \dfrac{R_3}{2\pi f x R_{\text{coil}} x R_2 x C_1}, & f > 200\text{ kHz}. \end{cases} \quad (1)$$

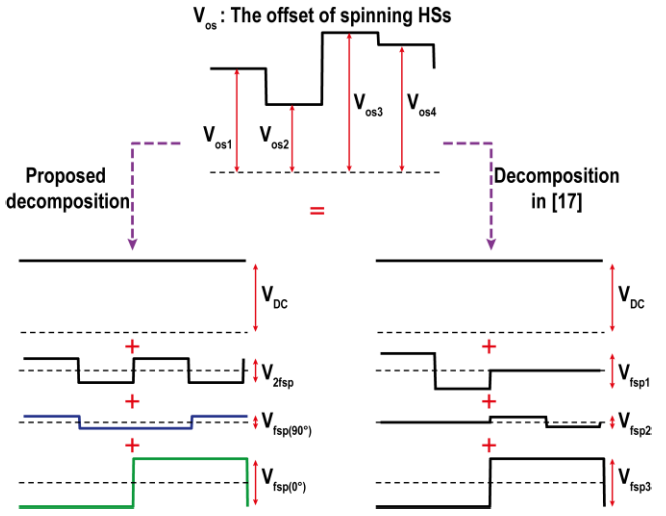

Fig. 4. Decomposition of a four-level Hall sensor offset into three orthogonal signals.

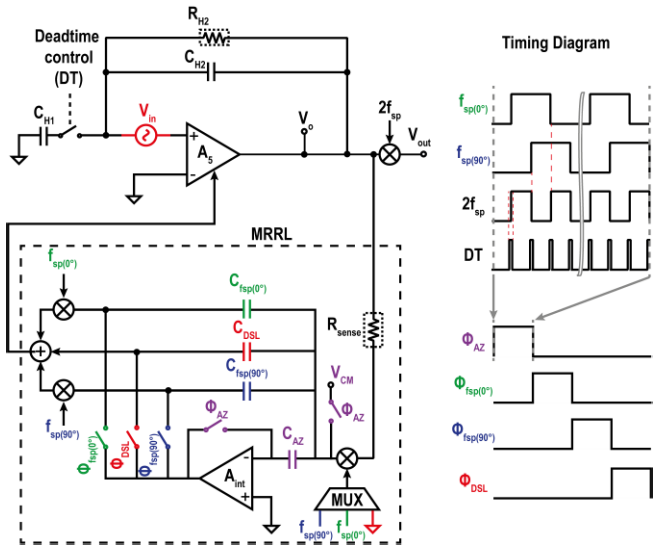

Fig. 5. Simplified single-ended multiplexing ripple-reduction loop (MRRL) and the timing diagram.

The sensing coil R_{coil} is made of metal with a large temperature coefficient (TC = 0.34%/K). By realizing $R_{1,3}$ with silicided n-poly resistors (TC = 0.29%/K) and R_2 with non-silicided p-poly resistors (TC = −0.02%/K), the coil path overall TC is reduced significantly, to about −0.03%/K.

C. Multiplexed Ripple-Reduction Loop

Although Hall plates can be easily realized in CMOS, they usually suffer from a large offset, typically about 10 mT [24]. This can be significantly reduced by the spinning-current technique, which involves changing the direction of the sensor's bias current periodically and thus converting offset into ac ripple [23], which can be suppressed by LPFs or by ripple-reduction loops (RRLs) [17]. The residual offset, which is mainly due to n-well inhomogeneity, can then be reduced to a few microteslas [12].

In this work, the modified spinning-current technique proposed in [25] is used to keep the Hall offset at dc, while the desired Hall voltage is upmodulated to twice the spinning frequency ($2f_{\text{sp}} = 200$ kHz). This ensures that most of the offset is blocked by the CCAs, leaving only some components at f_{sp} and $2f_{\text{sp}}$, which are again mainly due to n-well inhomogeneity. By ensuring that f_{sp} is much higher than f_X, this ripple will be significantly attenuated by the Hall-low-pass characteristic of the Hall path. However, the residual ripple is still quite significant and may limit sensor resolution [18].

To suppress the residual ripple further, RRLs can be used. As shown in Fig. 4, the residual ripple is a four-phase signal. This can be decomposed into three components, which are suppressed by three RRLs, [17]. In this work, however, we note that the spinning ripple can be decomposed into four different components: a dc offset, a square wave at $2f_{\text{sp}}$, and two quadrature square waves at f_{sp}. The amplitude of these signals can be expressed as

$$V_{\text{DC}} = \frac{1}{4}(V_{\text{os1}} + V_{\text{os2}} + V_{\text{os3}} + V_{\text{os4}}) \tag{2}$$

$$V_{2fsp} = \frac{1}{4}(V_{\text{os1}} - V_{\text{os2}} + V_{\text{os3}} - V_{\text{os4}}) \tag{3}$$

$$V_{fsp(0°)} = \frac{1}{4}(-V_{\text{os1}} - V_{\text{os2}} + V_{\text{os3}} + V_{\text{os4}}) \tag{4}$$

$$V_{fsp(90°)} = \frac{1}{4}(V_{\text{os1}} - V_{\text{os2}} - V_{\text{os3}} + V_{\text{os4}}). \tag{5}$$

The dc offset will be blocked by the CCA, while the ripple at $2f_{\text{sp}}$ cannot be distinguished from the desired Hall voltage. The other two ac components can then be suppressed by just two RRLs.

Since spinning ripple is a quasi-static error, the two RRLs can be efficiently realized by a single multiplexed RRL (MRRL) (Fig. 5). This is built around an opamp A_{int} and has four operating phases during which: 1) it auto-zeroes the offset of A_{int}, which would otherwise set the residual ripple amplitude; 2) it sequentially suppresses each of the two quadrature components; and 3) it suppresses the offset of A_5 with a dc servo loop (DSL), which would otherwise be converted into extra ripple by the output chopper. Each quadrature component is detected by a chopper demodulator, integrated on an integration cap C_{fsp} to generate a correction signal, which is then upmodulated and fed back to A_5 via an auxiliary input stage. The offset of A_5 is detected in a similar manner, but with the chopper disabled. The switched-resistor technique is used to realize a large sensing resistor ($R_{\text{sense}} >$ 100 MΩ), resulting in narrow RRL notches (<1 kHz) that do not impact gain flatness.

By applying KCL at the output node of A_5 (V_{o}) and the virtual ground of A_5, the DSL TF ((V_o/V_{in})) can be expressed as

$$\frac{V_o}{V_{\text{in}}} = \frac{g_1}{\frac{(sC_{H1}+g_1)(sC_{H2}R_{H2}+1)}{s(C_{H2}+C_{H1})R_{H2}+1} + \frac{1}{R_o \| R_s} + \frac{g_2}{\frac{1}{A_{\text{int}}}+sR_sC_{\text{DSL}}}} \tag{6}$$

where g_1 is the transconductance of A_5, g_2 is the DSL parallel input pair transconductance, and R_o is the load resistor of A_5. By assuming that R_{H2} is large enough, the high-pass corner frequency of the DSL can be approximated as

$$f_{\text{DSL}} = \frac{1}{2\pi R_s C_{\text{DSL}}} \cdot \frac{g_2}{g_1} \cdot \frac{C_{H1}+C_{H2}}{C_{H2}}. \tag{7}$$

Also, the DSL attenuation is

$$\text{Att.} = A_{\text{int}} \cdot \frac{g_2}{g_1}. \tag{8}$$

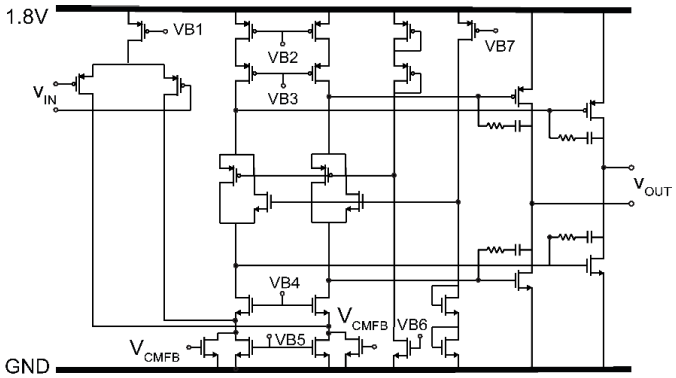

Fig. 6. Schematic of A1 and A2.

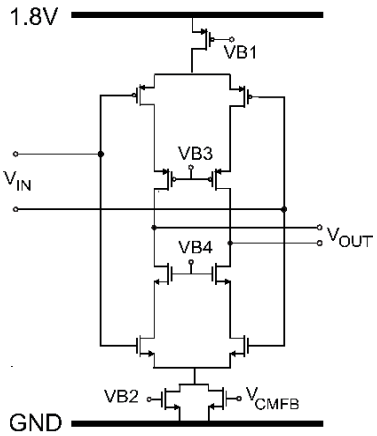

Fig. 7. Schematic of A3 and A4.

In this design, $g_2 = 0.1g_1$, $C_{\text{DSL}} = 5$ pF, $A_{\text{int}} = 60$ dB, $R_s = 100$ MΩ, and $C_{H2} = 12C_{H1}$, which leads to a DSL corner frequency $f_{\text{DSL}} = 400$ Hz and 40 dB attenuation.

By enabling the choppers before and after A_{int}, the DSL and its high-pass characteristic are converted to an RRL and a band-stop characteristic, respectively.

D. Amplifiers Implementation

A_1 and A_2 are two-stage amplifiers with a folded-cascode input stage and a class-AB output stage (Fig. 6). In A_2, the output stage is required to drive an external 20-pF load capacitance, while in A_1, it is required to handle the large coil input currents at high frequencies. The equivalent input-referred noise of A_1 is equal to the thermal noise resistance of R_{coil} (3.3 kΩ).

A_3 and A_4 are current reuse telescopic amplifiers (Fig. 7) to match their noise contribution equal to the noise of Hall plate resistance R_{Hall} (350 Ω) with maximum noise efficiency.

E. Self-Calibration Scheme

To obtain a flat frequency response, the gain of the Hall plates can be trimmed to match with the coil path. This is achieved by adjusting the Hall plate's biasing currents with the help of an 8-bit PTAT current digital-to-analog converter (DAC), which can be used to trim the sensitivity of the Hall plates in steps of 1%.

As shown in Fig. 8, to realize the calibration scheme, two square-wave fixed currents (8 mA_{pp}) at high (140 kHz) and

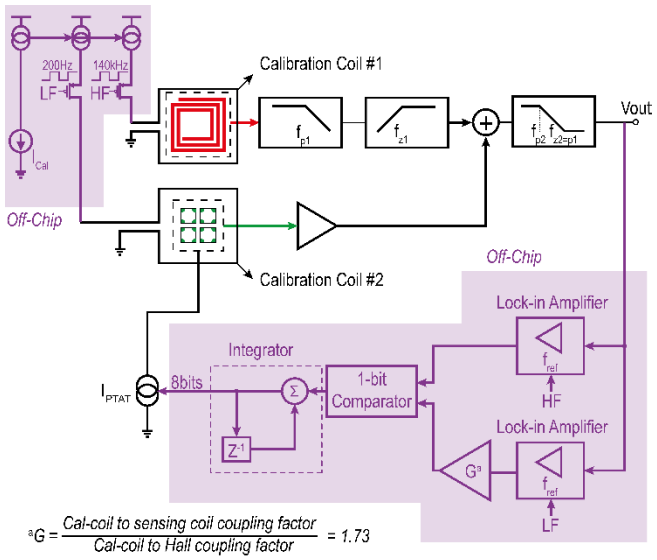

Fig. 8. Self-calibration scheme.

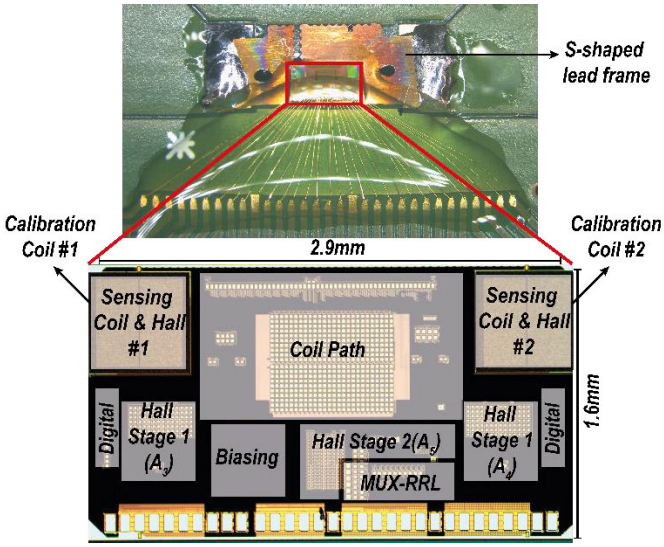

Fig. 9. Sensor die on a copper lead frame (top) and die micrograph (bottom).

low (200 Hz) frequencies are applied to the on-chip calibration coils. Since they are close to the sensors, these coils obviate the need to deliver large currents (∼ few amps) through the current rail for calibration. The magnetic fields generated by the calibration currents are detected by the sensing coils and Hall plates. The corresponding outputs are separated at the output of the final stage with two lock-in amplifiers. The outputs of the lock-in amplifiers are compared, and then, their difference is integrated to control the 8-bit current DAC. The large calibration-loop gain ensures that the difference is zero, and thus, the gain of the Hall and coil paths is matched. A 10-Hz measurement BW was used to achieve <1% trimming error. A G factor (1.73) is considered at the output of the low-frequency lock-in amplifier to compensate for the different coupling factors between the calibration coil (metal 6) with the sensing coil (metal 5) and the Hall plate (substrate).

It should be mentioned that applying temperature compensation in both paths makes the overall TF robust to temperature drift, and thus, it only requires room-temperature calibration.

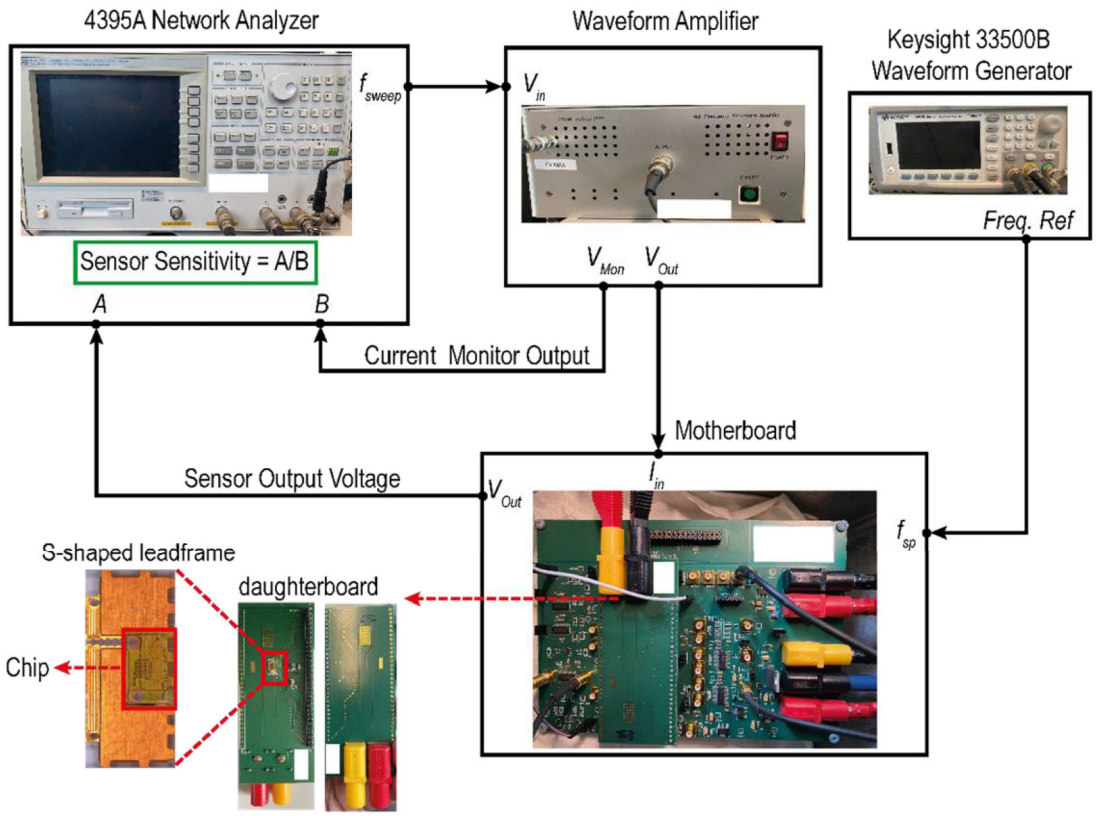

Fig. 10. Measurement setup.

To save the area, only the critical calibration coils were implemented on the chip, while the rest of the system was implemented off-chip.

III. Measurement Results

The hybrid current sensor is fabricated in a standard 0.18-μm CMOS process (Fig. 9, bottom) and occupies 4.6 mm^2, which is mainly determined by the need to position the Hall/coil sensors above the slots of the S-shaped current rail. The die is isolated from the lead frame by non-conductive glue (Fig. 9, top). The chip is powered by an analog supply (1.8 V) and a digital VDD (1.8 V). All other bias currents/voltages are implemented on-chip. The sensor draws 7.8 mA, of which 5 mA is used to bias the Hall plates. To mitigate high-frequency crosstalk, two grounded on-chip shields are employed: one above the metal coil in metal 6, while the other is placed between the coil sensor and the Hall plate.

As shown in Fig. 10, a daughterboard printed board circuit (PCB) is mounted over a motherboard PCB to measure the sensor sensitivity. The daughterboard PCB includes the S-shape lead frame and the chip, while the motherboard consists of voltage regulators, differential-to-single-ended amplifiers, and an external clock reference. The calibration setup is also provided off-chip on the motherboard. A network analyzer that sweeps over the frequency is connected to a waveform amplifier with high current capability. The output of the waveform amplifier delivers the current to the current rail. The sensor sensitivity can be determined at different frequencies by measuring the ratio between the sensor output voltage and the waveform amplifier current monitor output.

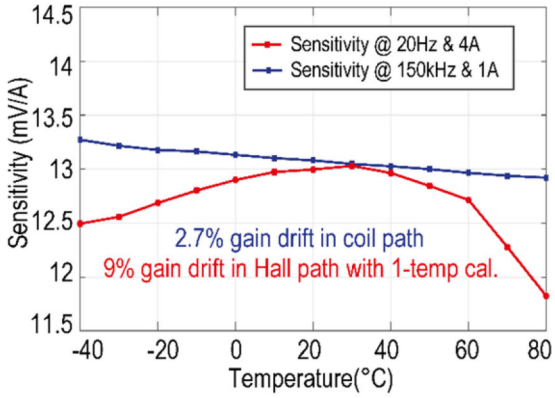

Fig. 11. Sensitivity versus temperature.

The sensitivities of the Hall and coil paths over temperature are shown in Fig. 11. The PTAT bias current effectively compensates for the linear component of the Hall plate's temperature dependency, resulting in a 9% gain drift in the Hall path. The 2.7% gain drift in the coil path is due to the expected residual TC of using different resistors.

After trimming at room temperature, the measured TF of the sensor is shown in Fig. 12. Its 3-dB bandwidth is limited to 5 MHz by eddy currents induced in the current rail. Around f_X (dc-to-100 kHz), the measured gain variation is less than $\pm 1.5\%$ (± 0.12 dB), which is about $6\times$ less than that reported in [18]. The spread above 200 kHz is caused by

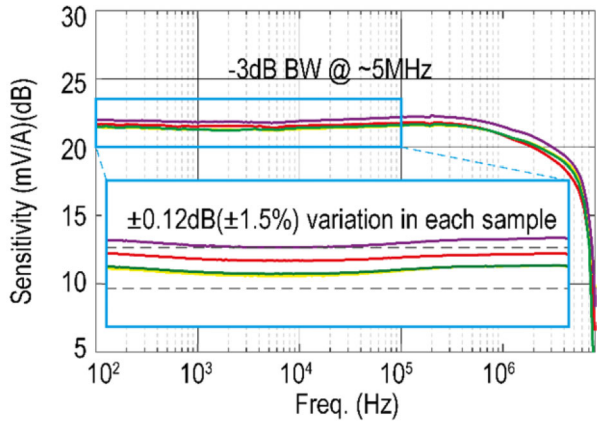

Fig. 12. Sensitivity versus frequency magnitude.

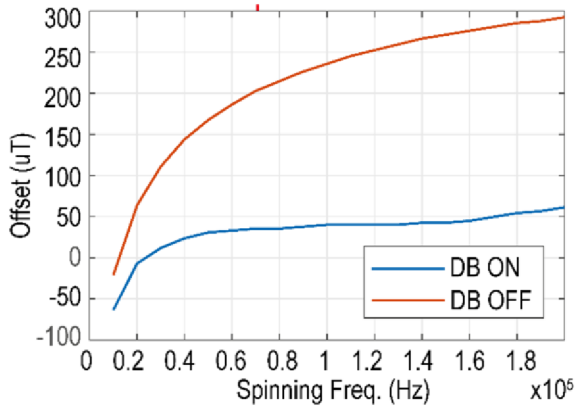

Fig. 13. Uncalibrated offset versus f_{sp} w/ deadbanding on/off.

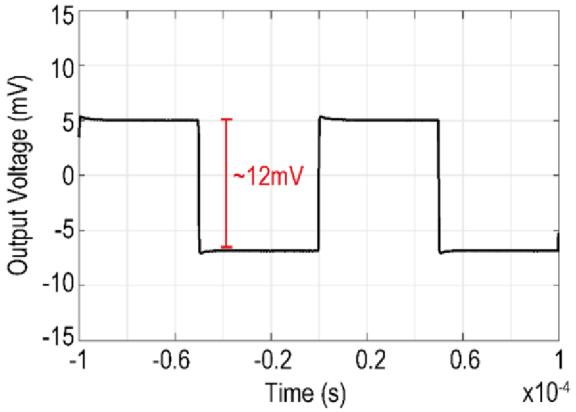

Fig. 14. Transient response for a 1-A_{p-p} square-wave@10 kHz (After 1024× averaging).

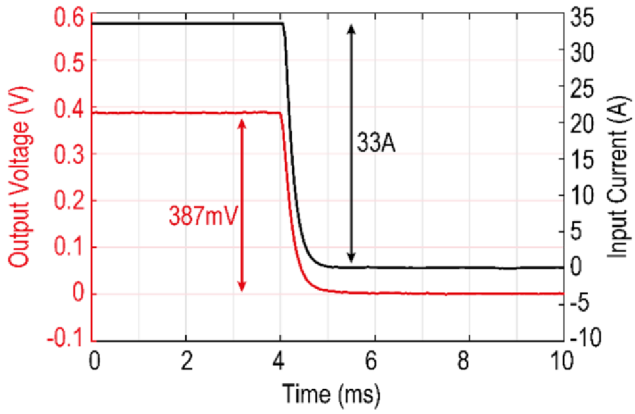

Fig. 15. 33-A step response.

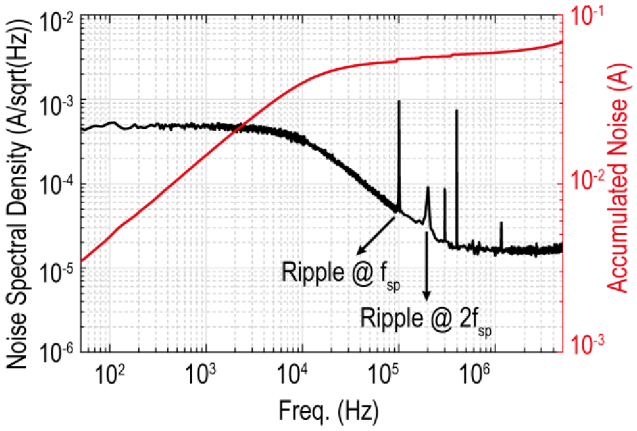

Fig. 16. Noise spectral density and accumulated noise referred to current rail.

the manual alignment of the chips with the slots in the current rail.

The DR of the sensor was determined experimentally. At dc, the self-heating of the current rail limits the maximum input current to ∼33 A. As the input frequency is increased above f_X, the induced coil voltage increases, causing the input stage of the coil path to eventually clip. By injecting a test current into the coil path, it was found to have a BW of ∼8 MHz, with the onset of clipping (THD = 3%) corresponding to 33 A_{rms}(46 Ap) at 300 kHz in the current rail. As shown in Fig. 13, the use of deadbanding makes the Hall plate offset relatively independent of f_{sp}. For a good tradeoff between offset and the filtering of residual spinning ripple, f_{sp} = 99 kHz was chosen. This results in the worst case offset of 57 μT (4 samples), which corresponds to 130 mA in the current rail. The sensor's response to small (1 A) and large (33 A) steps is shown in Figs. 14 and 15, respectively. In the case of the large step, the slow fall time is mainly due to the limitations of the 33-A current supply.

Fig. 16 shows the noise spectral density together with the accumulation noise. The MRRL suppresses the main spinning ripple (at f_{sp} and $3f_{sp}$) by more than 20 dB. The total input-referred ripple corresponds to 16 mA_{rms} (5 μT_{rms}), which is about 20% less than that reported in [17]. In a 5-MHz bandwidth, the sensor's accumulated noise corresponds to 69 mA_{rms} (20 μT_{rms}). It should be mentioned that the current resolution depends on the proximity of the current rail to the on-chip sensors. Thus, designs with on-chip current rails may have a higher current resolution at the expense of increased manufacturing cost and galvanic isolation. Finally, the residual ripple at f_{sp} only causes a 2-mA step in the total accumulated noise. The residual ripple is mainly due to the limited BW of the CCAs. As a result, the ripple components are not perfect square waves, and thus, they are not completely canceled by the RRLs. Switching transients also contribute to the residual ripple.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Source	**This work**	ISSCC'21 [16]	JSSC'17 [17]	JSSC'19 [15]	JSSC'22 [8]	APEC'19 [18]
Sensor Type	**Coil + Hall**	Coil + Hall	Coil + Hall	Hall	IFG	Coil + Hall
Technology (μm)	**0.18**	0.18	0.18	0.35	0.25	0.18
Supply (V)	**1.8**	1.8/3.3	5	3.3	1.8/5	1.8
Area (mm^2)	**4.6**	4.6	8.75	N/A	4+3.6	2.74
Resolution (mA_{rms})	**69**	64	480	480	11[c]	710
Input Range (A)	±**46**[a]	±25	±18[a]	±300	±53[c]	±60
Dynamic Range (dB)	**54**	52	17	56	74	39
BW (MHz)	**5**	1.8	3	1.7	0.125	15.3
Power Consumption (mW)	**14**	19.5	38.5	13.2	100[d]+13	63.5
Gain Flatness	±**1.5%**	±12%	N/A	N/A	N/A	±3.7%
Residual Ripple @f_{sp} (μT)	**6**	74	8	N/A	N/A	N/A
Residual Offset (μT)	**57**	75	40	262	N/A	N/A
FoM[b][fW/Hz]	**1.6**	17.7	2281	5	8.5	145
DR + 10log(BW/Power)	**139**	131	96	137	135	122

[a]Extrapolated [b]FoM = Power/(BW x (Range/Resolution)^2) [c]Conversion rate = 45μT/A [d]Full-range power

Table I summarizes the performance of the proposed hybrid current sensor and compares it with state-of-the-art magnetic current sensors. Compared to [18], the gain flatness and input-referred ripple are improved by 6× and 16×, respectively. This design also achieves the highest energy efficiency figure of merit (FoM) (3×) and the lowest power consumption (1.4×) of all hybrid sensors.

IV. CONCLUSION

In this work, a hybrid magnetic current sensor with wide BW (5 MHz) is proposed. A multiplexed RRL is employed to effectively deal with the Hall plate offset in different spinning phases. With this approach, the residual ripple at the spinning frequency is 4× below the total integrated noise. The offset of the coil path is blocked by large on-chip capacitors (1.5 nF each), which are implemented in an area-efficient manner by placing MOS capacitors below MIM capacitors. The drift in the sensitivity of the coil path over temperature is compensated with the help of silicided poly resistors, which have nearly the same TC as the metal coils, while the drift of the Hall path is compensated by biasing them with a PTAT current. The resulting temperature drift is limited to 9% from −40 °C to 80 °C, mainly due to the residual drift of the Hall path. A one-time room-temperature calibration scheme with on-chip calibration coils is utilized to equalize the sensitivity of the Hall and coil paths. The overall sensor achieves the state-of-the-art energy efficiency with an FoM of 1.6 fW/Hz.

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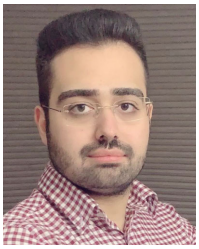

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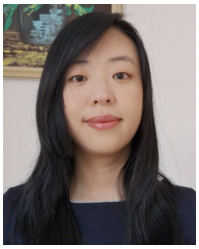

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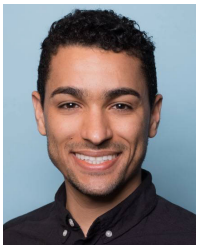

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