A Variable-Gain Low-Noise Transimpedance Amplifier for Miniature Ultrasound Probes

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A Variable-Gain Low-Noise Transimpedance Amplifier for Miniature Ultrasound Probes

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***Abstract*— This article presents a low-noise transimpedance amplifier (TIA) designed for miniature ultrasound probes. It provides continuously variable gain to compensate for the time-dependent attenuation of the received echo signal. This time-gain compensation (TGC) compresses the echo-signal dynamic range (DR) while avoiding imaging artifacts associated with discrete gain steps. Embedding the TGC function in the TIA reduces the output DR, saving power compared to prior solutions that apply TGC after the low-noise amplifier. The TIA employs a capacitive ladder feedback network and a current-steering circuit to obtain a linear-in-dB gain range of 37 dB. A variable-gain loop amplifier based on current-reuse stages maintains constant bandwidth in a power-efficient manner. The TIA has been integrated in a 64-channel ultrasound transceiver application-specific integrated circuit (ASIC) in a 180-nm BCDMOS process and occupies a die area of 0.12 mm^2. It achieves a gain error below ±1 dB and a 1.7 pA/$\sqrt{}$Hz noise floor and consumes 5.2 mW from a ±0.9 V supply. B-mode images of a tissue-mimicking phantom are presented that show the benefits of the TGC scheme.**

***Index Terms*— Continuous gain control, time-gain-compensation (TGC), transimpedance amplifier (TIA), ultrasound application-specific integrated circuit (ASIC), ultrasound imaging.**

I. Introduction

ULTRASOUND imaging is a safe and cost-effective tool for the diagnosis of medical conditions and the guidance of treatment. Size reduction of imaging devices has enabled ultrasound imaging from the tip of an mm-size catheter, for instance, for intracardiac echocardiography (ICE), as illustrated in Fig. 1(a) [1], [2]. Applications of ICE probes include guidance and monitoring of catheter ablation for the treatment of atrial fibrillation, guidance of closure of atrial septal defects, and guidance of transcatheter valve implantation [3], [4].

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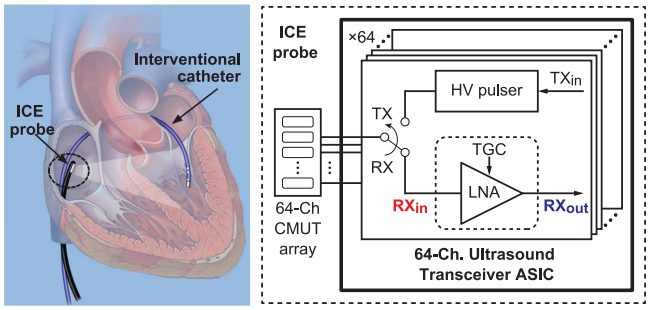

Fig. 1. (a) Application scenario of an ICE probe. (b) Block diagram of the transceiver ASIC with the proposed TIA.

ICE probes, and other miniature ultrasound probes alike, employ an array of ultrasound transducer elements to transmit ultrasonic pulses and record the resulting echo signals, from which an image is reconstructed using beamforming techniques [5]. In many probes, each transducer element is electrically connected via a cable to the external imaging system [5]–[7]. However, this approach limits the number of transducer elements due to the limited number of cables that can be accommodated and results in signal attenuation due to the fact that the cables load the elements. Increasingly, application-specific integrated circuits (ASICs) are integrated in the probe close to the transducer array to address these issues [8]–[13].

Fig. 1(b) shows a block diagram of the front end of such an in-probe ASIC. For each transducer element, it contains transmit (TX) and receive (RX) circuitry. The former tends to include a high-voltage (HV) pulser that drives the element to generate a pressure wave [8]–[11]. At the start of the RX signal path, a low-noise amplifier (LNA) amplifies the echo signal so that it can be further processed by the following circuitry, which may involve beamforming, multiplexing, and digitization [12], [13].

An important function in the RX signal path is time-gain compensation (TGC), which reduces the echo-signal dynamic range (DR) by compensating for the propagation attenuation experienced by the acoustic waves as they travel through the body [14]. Due to this attenuation, echo signals from deep tissue, which need to travel longer than echoes from nearby structures and, therefore, arrive later, are more attenuated.

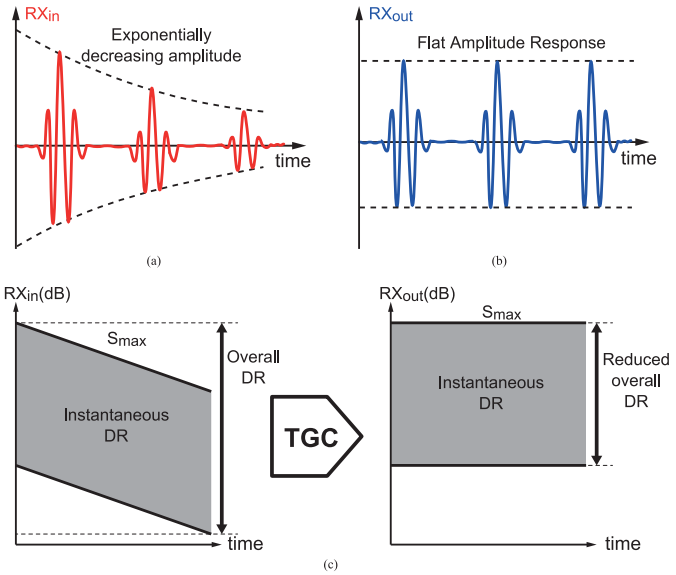

Fig. 2. (a) RX signal before TGC. (b) RX signal after TGC. (c) RX input and output signal range as a function of time with ideal TGC.

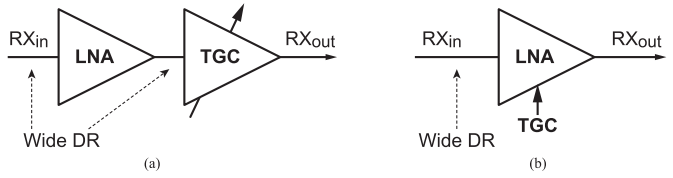

Fig. 3. (a) Block diagram of the conventional solution of an LNA followed by a TGC amplifier. (b) Block diagram of the proposed LNA with embedded TGC function.

This leads to an exponential decrease in echo amplitude with time, as illustrated in Fig. 2(a). Since propagation attenuation increases with frequency [14], this is particularly significant at the relatively high frequencies (>5 MHz) typically used in miniature probes. The attenuation may amount to 40 dB at the largest imaging depth. It can be compensated for by providing a gain that increases linearly in decibels as a function of time, thus providing a uniform echo amplitude across depth, as illustrated in Fig. 2(b).

The impact of the TGC on the signal DR is further illustrated in Fig. 2(c), which shows how the range of echo-signal levels (the instantaneous DR) varies as a function of time (or, equivalently, depth) before and after the TGC, demonstrating that the time-dependent attenuation is corrected for, thus reducing the overall DR to a level similar to the instantaneous DR. In conventional ultrasound systems, the TGC is typically performed after the LNA [15], as shown in Fig. 3(a), implying that a power-hungry LNA is required that is capable of handling the full DR of the echo signal at its output.

In this article, we present an LNA with a built-in continuous TGC function that mitigates this problem, as shown in Fig. 3(b) [16]. The LNA is a transimpedance amplifier (TIA) optimized to amplify the signal current of a capacitive micro-machined ultrasound transducer (CMUT). We demonstrate its integration into a 64-channel ASIC for a CMUT-based ICE probe, as shown in Fig. 1(b). While the

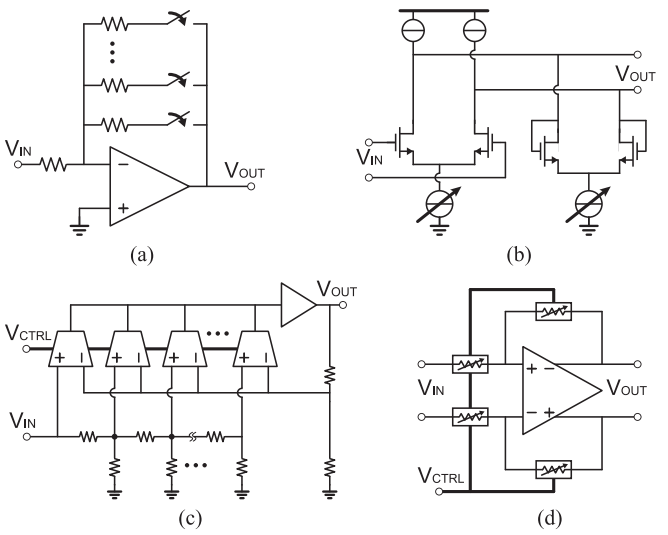

Fig. 4. Circuits to realize the TGC. (a) Amplifier with discrete gain steps [17]–[21]. (b) Amplifier with time-varying biasing [24]. (c) Amplifier that interpolates between the outputs of a resistive ladder attenuator [29]. (d) Amplifier using a feedback network with MOS variable resistors [23].

LNA has been designed for application in an ICE probe, the presented amplifier architecture is applicable to ultrasound front ends for miniature ultrasound probes in general.

This article is organized as follows. Section II reviews the existing approaches for the TGC. Section III describes the proposed TIA architecture. The circuit implementation details of the TIA are presented in Section IV. Electrical measurements and imaging experiments are presented in Section V. This article ends with a comparison with the state-of-the-art and conclusions.

II. Comparison of TGC Circuits

Various approaches have been taken to realize the amplifiers suitable for the TGC. They can globally be divided into two groups: amplifiers with discrete gain steps and amplifiers with continuous gain control.

Amplifiers with discrete gain steps approximate the ideal exponentially varying gain by a number of discrete gain steps that are sequentially applied. An important advantage of this approach is that the gain steps can be accurately defined by means of a digitally programmable resistive feedback network, as illustrated in Fig. 4(a) [17]–[21], a digitally programmable capacitive feedback network [12], [13], [22], or a digitally programmable current-steering feedback network [23]. Moreover, the gain steps can be divided among multiple amplifier stages, with course gain steps realized in the LNA at the input of the receive signal path, which enables the realization of highly power-efficient amplifiers [12], [19]. Switching from one discrete gain step to the next, however, is typically associated with a switching transient that can lead to artifacts in the ultrasound image at a depth that corresponds to the gain-switching moment. Such artifacts can be made negligible by making the gain steps small [20], but this requires a large number of gain steps to cover the gain range, leading to a complex circuit that requires substantial die area.

Amplifiers with continuous gain control are also referred to as variable-gain amplifiers (VGAs) and typically have a gain that can be set by an analog control input, typically a control voltage. The gain tends to depend (approximately) exponentially on the control voltage, giving a linear-in-dB gain control. By ramping the control voltage linearly as a function of time, the gain can be swept across a desired range to realize the TGC without the disadvantages associated with discrete gain steps. The many ways in which this can be realized can be roughly divided into two categories: amplifiers with an approximately exponential transfer function and amplifiers with interpolation between discrete gain steps.

Amplifiers with an approximately exponential transfer function typically exploit the non-linear characteristics of MOS or bipolar transistors to realize the variable gain. This can be done, for instance, by changing the operating point of a differential pair as a function of a gain-control voltage, leading to a variable transconductance. Combined with a load with an impedance that is also dependent on the control voltage, for instance, by changing the operating point of diode-connected transistors as a function of the same control voltage, an amplifier with a non-linear transfer function is obtained, as shown in Fig. 4(b) [24], [25]. However, this non-linear transfer function only approximates an exponential across a limited gain range and tends to be sensitive to process, supply voltage, and temperature (PVT) variations. Multiple stages can be cascaded to extend the range [26], [27].

Another approach to approximate an exponential transfer function is to use the exponentially increasing output voltage of a positive-feedback amplifier during a well-defined time window [28]. This approach, however, requires that the signal is sampled at the amplifier's input, allowing each successive sample to be amplified using the positive-feedback amplifier, and the gain to be varied from sample to sample by changing the positive-feedback time window.

A TGC amplifier topology with interpolation between discrete gain steps has been reported in [29] and [30]. As illustrated in Fig. 4(c), the input signal is attenuated by a resistive ladder network, each section of which provides a fixed attenuation step in decibels. These attenuated signals are fed to an amplifier with multiple input stages, the bias currents of which are controlled in order to gradually change from one step to the next. Another topology that employs multiple inputs stages with controlled biasing has been reported in [31], where the attenuating network is part of the feedback of the amplifier, and the input stages directly connect to the input in order to provide not only the variable gain but also simultaneously varying the input noise and signal swing.

Interpolation between discrete gain steps can also be achieved by smoothly changing the components values in a passive attenuator network by including MOS transistors that act as variable resistors, as illustrated in Fig. 4(d) [23], [32]. Special biasing circuits are needed in order to mitigate the PVT dependence.

The third approach to achieve interpolation between discrete gain steps is to use a differential pair as a current-steering device. In [33], a differential pair at the output of an amplifier directs a fraction of the output current back to the input and a fraction toward the output. Thus, the current gain of this amplifier can be continuously controlled through the voltage applied to the differential pair. In an amplifier with two parallel input stages, Onet *et al.* [34] used current steering to control how much of the output current of the current produced by these input stages is added to the output.

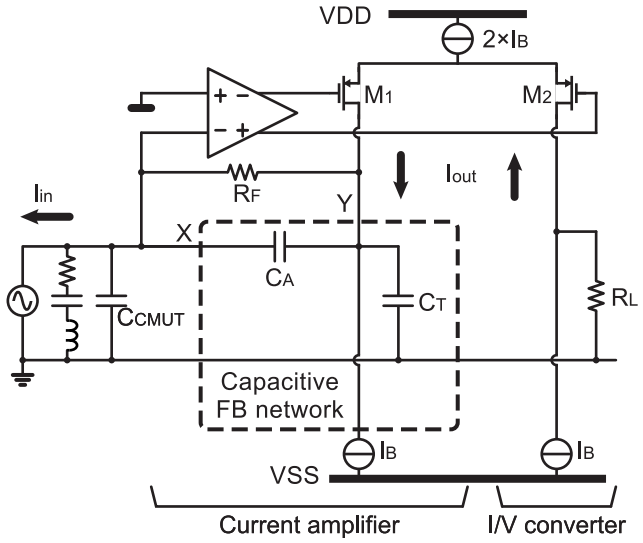

Fig. 5. Simplified circuit diagram of the proposed TIA with a fixed-gain capacitive feedback network.

Compared to the prior art, the amplifier proposed in this work has three appealing features. First, it provides continuous TGC, avoiding the switching artifacts associated with discrete gain steps. Second, as the TGC function is realized in the LNA, it does not rely on a preceding (fixed-gain) LNA to obtain a good noise figure and/or to obtain a suitable input impedance, like in, e.g., [23], [29], [30], and [35]. Such a fixed-gain LNA has an output DR that equals the large input DR, which tends to be associated with additional power consumption in the output stage to achieve acceptable distortion at the largest signal levels, or with additional power consumption to reduce the noise in the stage after the LNA if the LNA's gain is kept limited to avoid distortion. Third, as it relies on capacitor ratios to define the gain, it avoids the additional noise associated with a resistive feedback network and the PVT dependence of approaches that rely on non-linear device characteristics.

III. Architecture of the TIA With the TGC

A. Current Amplifier-Based TIA

As mentioned, the proposed TIA has been designed to interface with a CMUT transducer. Such a transducer consists of a flexible micro-machined membrane that forms one of the electrodes of a parallel-plate capacitor. In response to an incoming pressure wave, the membrane is moving, leading to a small change in the capacitance. When the CMUT is DC biased, this change can be detected as a signal current [36]. The CMUT can then be modeled as a signal-current source I_{in} shunted by a capacitance C_{CMUT} modeling the transducer's electrical capacitance and a resonator representing its mechanical resonance, as shown in Fig. 5. The transducer

used in this work is operated at 5 MHz and has a capacitance of 15 pF.

To detect the signal current, an LNA with low input impedance is needed, making a TIA is a suitable choice [37]. In this work, an input-referred noise level of 2 pA/$\sqrt{\text{Hz}}$ and a maximum signal current of 100 μA are targeted. A TIA with resistive feedback is commonly used [38] but does not readily support the widely variable gain needed for the TGC. Moreover, resistive feedback contributes additional noise.

Therefore, instead, we use a TIA based on a current amplifier with capacitive feedback as a starting point, based on [39]. As shown in Fig. 5, this TIA consists of a current amplifier with a gain defined by capacitors C_{A} and C_{T}, followed by a resistive load R_{L} that turns the amplified current into an output voltage. A high-ohmic feedback resistor R_{F} serves to set the dc operating point and plays a negligible role at the signal frequencies of interest. A loop amplifier senses the input voltage V_X so as to maintain a virtual ground at the input. As a result, the input current I_{in} is integrated on capacitor C_{A}, leading to a voltage V_Y across capacitor C_{T}, and an amplified output current

$$I_{\text{OUT}} = \left(1 + \frac{C_{\text{T}}}{C_{\text{A}}}\right) I_{\text{IN}} = \alpha I_{\text{IN}}. \tag{1}$$

Thus, the circuit provides a current gain of $\alpha = 1 + C_{\text{T}}/C_{\text{A}}$.

We use this current gain mechanism to implement the required 40 dB gain range, as will be discussed shortly.

Contrary to [39], in which a single-ended loop amplifier and a source follower with a resistive load are used, we employ a fully differential loop amplifier and a differential pair (M_1 and M_2) that provides equal currents of opposite polarity to the feedback network and to R_{L} to convert the amplified current to an output voltage. To avoid clipping, the bias current I_{B} should be larger than the maximum amplified current. The resulting overall transimpedance is $(1 + C_{\text{T}}/C_{\text{A}})R_{\text{L}}$. This differential topology helps to reduce the power-supply sensitivity and increases the output voltage headroom.

B. Capacitive Ladder Feedback Network

Although variable gain could be realized by adjusting $C_{\text{T}}/C_{\text{A}}$, this would require a large capacitor ratio to achieve a 40 dB range and dense gain steps to minimize the switching artifacts between the gain steps. This would be unattractive in terms of die size and complexity. Therefore, as shown in Fig. 6(a), we realize gain steps covering a wide range by means of a ladder structure and then interpolate between these steps by means of a current-steering network (CSN).

Ignoring the interpolation for now, let us assume that the feedback node Y is connected to one of the nodes of the ladder network X_n ($0 \le n \le 5$ in our design). The ladder capacitors C_{A}, C_{B}, and C_{T} are dimensioned such that the capacitance to ground at each node X_n equals C_{T}, which implies

$$C_{\text{B}} + \frac{C_{\text{A}}C_{\text{T}}}{C_{\text{A}} + C_{\text{T}}} = C_{\text{T}} \Rightarrow C_{\text{B}} = \frac{C_{\text{T}}^2}{C_{\text{A}} + C_{\text{T}}}. \tag{2}$$

We will now show that this choice causes every ladder section to contribute an additional gain factor $\alpha = 1 + C_{\text{T}}/C_{\text{A}}$.

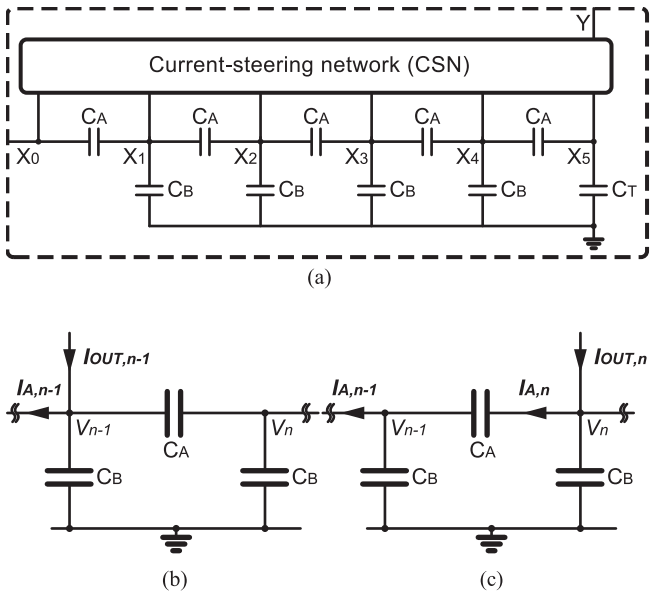

Fig. 6. (a) Capacitive ladder feedback network with CSN to realize the variable gain. Arbitrary section of the ladder network, with a feedback connection to (b) node $n-1$ and (c) node n.

If the feedback is connected to node X_0, the output current $I_{\text{OUT},0}$ equals I_{IN}, corresponding to a gain of 1 ($\alpha = \alpha^0$). The ladder network then merely forms an additional capacitive load at the input. If the feedback is connected to X_1, the topology is the same as in Fig. 5, and the output current equals $\alpha I_{\text{OUT},1} = I_{\text{IN}}$.

Now consider a feedback connection to an arbitrary node X_{n-1}, associated with an output current $I_{\text{OUT},n-1}$, as shown in Fig. 6(b), and a feedback connection to the next node X_n, with the output current $I_{\text{OUT},n}$, as shown in Fig. 6(c). Given that the feedback network is a linear passive network, the current $I_{\text{A},n-1}$ flowing back toward the input and the voltage V_{n-1} at node X_{n-1} must be equal, implying

$$I_{A,n-1} = I_{\text{OUT},n-1} - sC_{\text{T}}V_{n-1} = I_{A,n} - sC_{\text{B}}V_{n-1} \tag{3}$$

where $I_{A,n}$ is the current flowing in Fig. 6(c) through the capacitor C_{A} connecting node X_{n-1} to node X_n. This current can also be expressed in terms of $I_{\text{OUT},n}$:

$$I_{A,n} = \frac{C_{\text{A}}}{C_{\text{A}} + C_{\text{T}}} I_{\text{OUT},n} - s\frac{C_{\text{A}}C_{\text{T}}}{C_{\text{A}} + C_{\text{T}}} V_{n-1} \tag{4}$$

where the first term represents the fraction of $I_{\text{OUT},n}$ that would flow to node X_{n-1} if V_{n-1} would be zero, and the second term represents the current flowing from node X_{n-1} to node X_n if $I_{\text{OUT},n}$ would be zero. Substituting (2) and (4) into (3) gives

$$I_{\text{OUT},n} = \left(1 + \frac{C_{\text{T}}}{C_{\text{A}}}\right) I_{\text{OUT},n-1} = \alpha I_{\text{OUT},n-1} \tag{5}$$

which proves by induction that $I_{\text{OUT},n} = \alpha^n I_{\text{IN}}$.

Thus, by an appropriate choice of the capacitor values, exponential gain steps can be realized without requiring large capacitor ratios. In our implementation, we adopted a five-section ladder network with $\alpha = 2.5$ (i.e., gain steps of 8 dB covering 40 dB) realized using integer multiples of a unit capacitor C_{U}: $C_{\text{A}} = 10C_{\text{U}}$, $C_{\text{B}} = 9C_{\text{U}}$, and $C_{\text{T}} = 15C_{\text{U}}$.

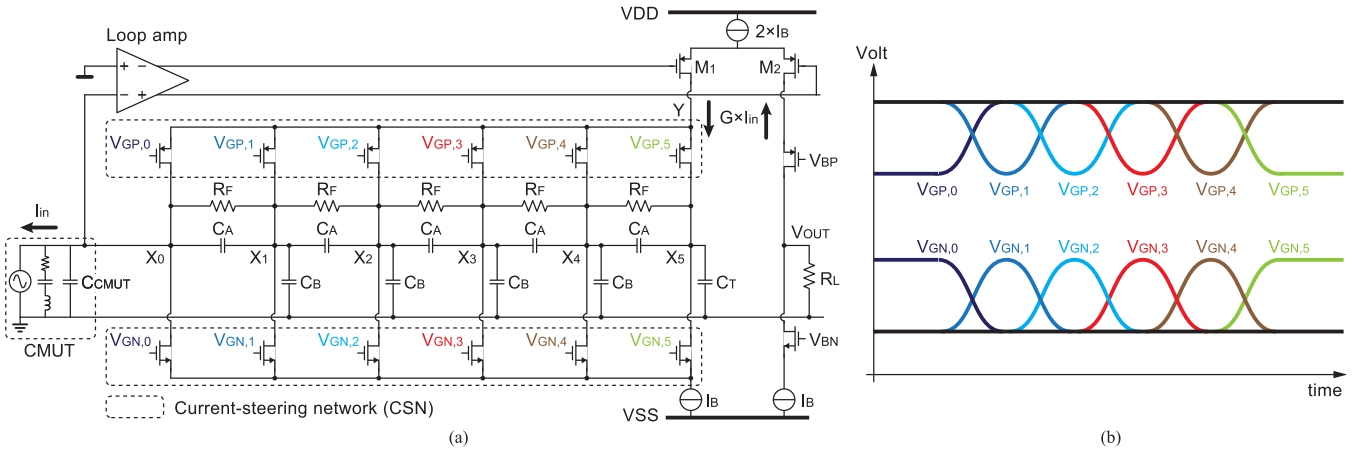

Fig. 7. (a) Circuit diagram of the proposed TIA. (b) Gate-control voltages for the CSNs for continuous gain control.

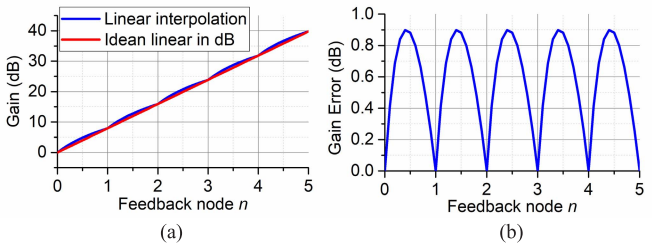

Fig. 8. (a) Gain as a function of the selected feedback node X_n for linear interpolation and for an ideal linear-in-dB curve. (b) Corresponding gain error relative to the linear-in-dB curve.

This allows for a compact and well-matched layout. The value of C_U should be sufficient to keep the voltage swing in the network limited and to make the impact of parasitic capacitance on the gain negligible. We use 0.3 pF to limit the swing to 360 mV at a maximum I_{IN} of 100 μA at 5 MHz.

C. Interpolation by means of Current Steering

To interpolate between the gain steps of the ladder network, we propose a CSN as shown in Fig. 7(a). A set of PMOS transistors directs the feedback current at node Y to the ladder nodes X_n. The feedback current is initially steered completely to the input node X_0, by providing a lower gate voltage $V_{GP,0}$ to the corresponding PMOS transistor, as shown in Fig. 7(b). The feedback current then gradually shifts from node to node, by alternately pulling down the gate voltages $V_{GP,n}$, effectively linearly interpolating between the exponential gain steps of the ladder network. Finally, the feedback current is steered entirely to the last tap, providing maximum gain. To bias the circuit, a complementary NMOS CSN, with similar complementary gate-drive voltages $V_{GN,n}$, steers a bias current I_B to the nodes of the feedback network. High-ohmic resistors R_F in the feedback network prevent charge accumulation due to small current differences between the CSNs, without affecting the in-band AC current gain.

The CSN provides an approximately linear interpolation between exponential gain steps. The resulting error with respect to an ideal linear-in-dB (exponential) gain curve is shown in Fig. 8. A ladder network consisting of five sections with a gain step of 8 dB each has been chosen to achieve a gain error less than 1 dB, in line with the requirements of the imaging application. This can be reduced by increasing the number of ladder sections. Note that the sharp dips in the gain-error curve in Fig. 8(b) are due to the ideal linear interpolation applied. The actual implementation using PMOS transistors and smoothly varying gate voltages as illustrated in Fig. 7(b) will lead to less sharp transitions in the gain-error curve.

D. Noise Analysis

To be able to detect the smallest echo signals at the highest gain, the TIA's noise contribution should not exceed that of the transducer. At the high end of the gain range, the noise contribution of the load resistor, the output differential pair, and the bias-current sources are negligible, because they are attenuated by the 40 dB current gain when referred to the input. The feedback network, due to its capacitive nature, does not contribute in-band noise. This leaves the loop amplifier as the dominant noise source. Its input-referred voltage noise appears at the virtual ground and leads to an equivalent input current noise due to the total impedance to ground at the input. This impedance is dominated in our design by the CMUT capacitance of about 15 pF and amounts to about 2 kΩ at 5 MHz. To achieve an equivalent input current noise below 1.5 pA/$\sqrt{\text{Hz}}$, the loop amplifier's input voltage noise should be below 3 nV/$\sqrt{\text{Hz}}$. Note that this noise level only needs to be achieved at the highest gain level. At lower gain levels, the input signal is bigger, and so proportionally larger noise can be accepted without loss of signal-to-noise ratio (SNR). Achieving this noise level in a power-efficient manner is one of the key design objectives for the loop amplifier implementation, as will be elaborated in Section IV.

IV. Circuit Implementation

A. Gain-Control Circuit

To generate the gate-control voltages $V_{GP,n}$ and $V_{GN,n}$ for the CSNs in Fig. 7(b), an external gain-control voltage V_{TGC}

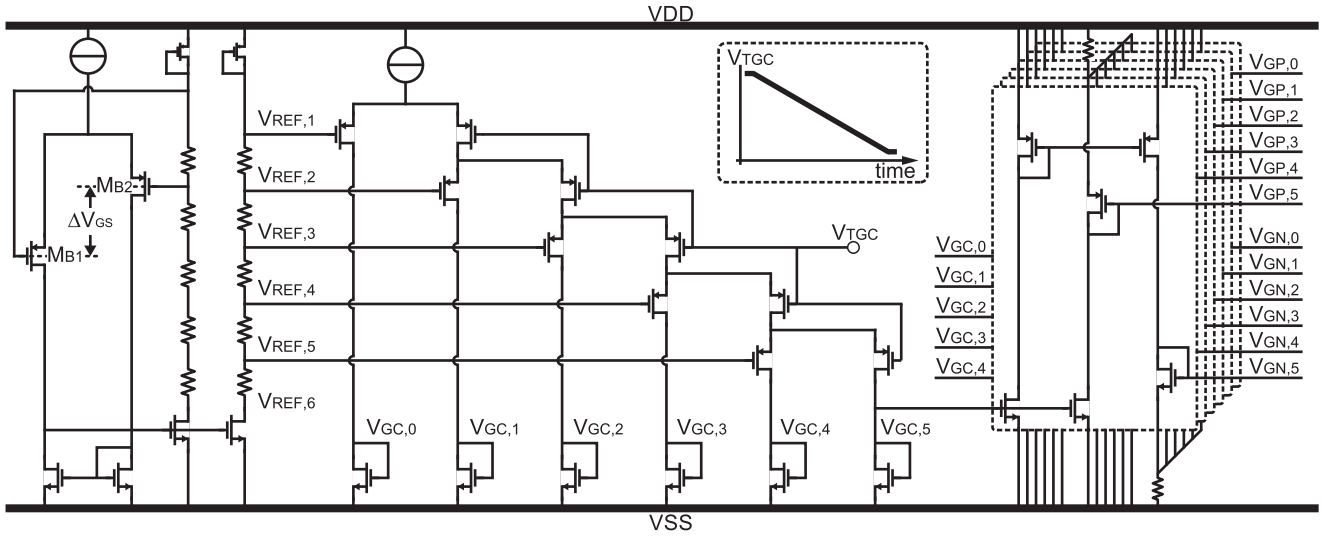

Fig. 9. Circuit diagram of the gain control circuit.

is compared to a set of reference voltages generated using a stack of cascaded PMOS differential pairs, as shown in Fig. 9. The reference voltages $V_{\mathrm{REF},i}$ are generated using a resistive divider. Thus, as V_{TGC} is swept, the tail current is steered from drain to drain. The drain currents are mirrored to diode-connected PMOS and NMOS transistors at appropriate common-mode levels to generate $V_{\mathrm{GP},n}$ and $V_{\mathrm{GN},n}$, respectively, resulting in the voltages shown in Fig. 7(b) when V_{TGC} is linearly ramped down.

In this circuit, all PMOS differential pairs have identical sizes and have bulk connections to the source to mitigate the body effect. The bias current of the gain-control circuit is chosen such that the bandwidth of the circuit is sufficient to track the required V_{TGC} transient, while avoiding excess bandwidth, as this would add undesired in-band noise to the signal path. The bias current for the resistive ladder is generated using the bias circuit shown in the left-hand side of Fig. 9. This bias circuit employs a feedback loop to generate a current proportional to the difference in gate–source voltage ΔV_{GS} of ratioed PMOS transistors M_{B1} and M_{B2}. The bias circuit employs a replica of the resistive ladder, so that the voltage steps between the reference voltages equal ΔV_{GS}, making the current division in the PMOS differential pairs as a function of V_{TGC} insensitive to process and supply variations.

B. Loop Amplifier Design

A key challenge in the design of the loop amplifier is to maintain sufficient loop gain in the presence of the widely varying current gain. We analyze the loop gain by breaking the feedback loop at the input of the loop amplifier. The resulting loop-gain $A_{\mathrm{LP}}(\omega)$ consists of the product of the loop amplifier's voltage gain $A_{\mathrm{amp}}(\omega)$ and the transfer function from the output of the loop amplifier back to the input

$$A_{\mathrm{LP}}(\omega) = A_{\mathrm{amp}}(\omega) \cdot \frac{g_{m,\mathrm{out}}\beta}{j\omega C_{\mathrm{IN}}} \tag{6}$$

where $g_{m,\mathrm{out}}$ is the transconductance of the differential pair $M_{1,2}$ (see Fig. 5), β is the fraction of that differential pair's

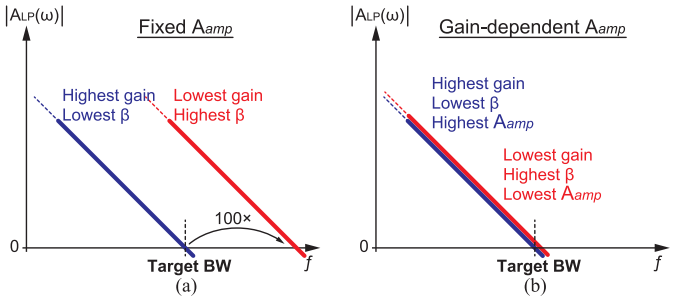

Fig. 10. Magnitude of the loop gain as a function of frequency, showing (a) strongly gain-dependent unity-gain frequency for a fixed-gain loop amplifier and (b) constant unity-gain frequency for a loop amplifier with variable gain.

output current that makes it back to the input, and C_{IN} is the total capacitance at the input, which is dominated by the CMUT capacitance C_{CMUT}. The fraction β is related to the closed-loop current gain, which in Section III-B has been shown to be α^n. Although the closed-loop current gain is independent of C_{IN}, because C_{IN} is at the virtual ground in the closed-loop configuration, C_{IN} does influence the fraction β. However, if $C_{\mathrm{IN}} \gg C_{\mathrm{T}}$, we can approximate the input as being shorted to ground by C_{IN}, and the factor β is then by good approximation, the inverse of the current gain α^n. If we assume that the loop amplifier has a constant gain and a wide bandwidth, i.e., that $A_{\mathrm{amp}}(\omega)$ is constant across the frequency range of interest, this implies that for a 40 dB variation in current gain, the unity-gain frequency of $A_{\mathrm{LP}}(\omega)$, which sets the closed-loop 3-dB bandwidth, would vary by a factor 100, as illustrated in Fig. 10(a). In order to achieve enough bandwidth at the highest current gain, which corresponds to the lowest β, we would obtain a bandwidth that is 100 times larger than needed at the lowest current gain, which corresponds to the highest β. To realize this, the loop amplifier would need to have an unrealistically wide bandwidth.

Therefore, instead, we employ a loop amplifier whose gain $A_{\mathrm{amp}}(\omega)$ is adjusted to compensate for the varying β.

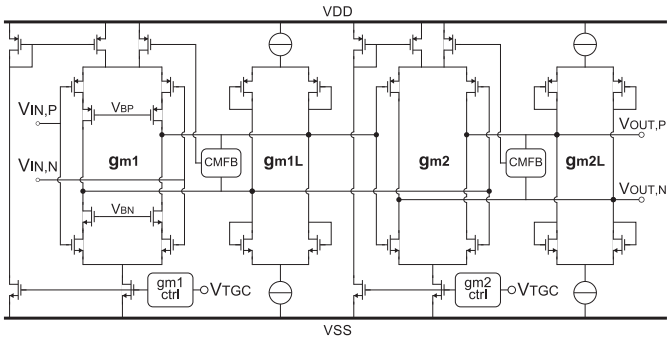

Fig. 11. Circuit diagram of the loop amplifier.

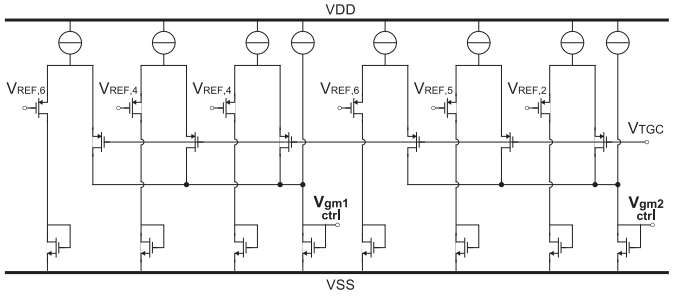

Fig. 12. Circuit diagram of the transconductance-control circuit.

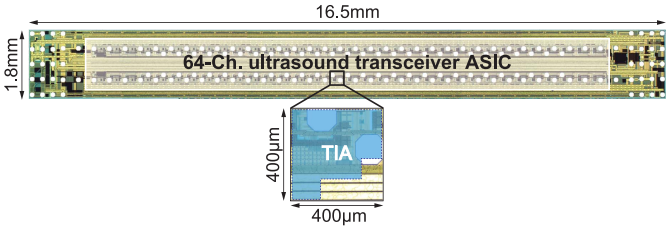

Fig. 13. Chip micrograph of the 64-channel transceiver ASIC, with inset showing the element-level TIA.

For the highest current gain (i.e., the lowest β), we make the dc gain of the loop amplifier roughly 100 times higher than for the lowest current gain (i.e., the highest β). This gives the loop an approximately constant unity-gain frequency, corresponding to an approximately constant closed-loop 3-dB bandwidth, as illustrated in Fig. 10(b). Any poles in the loop amplifier should be sufficiently above this frequency to maintain stability.

Since the required gain-bandwidth product of the loop amplifier is hard to realize with a single-stage amplifier, we use a cascade of two stages, as shown in Fig. 11. A fully differential amplifier structure is adopted. The first stage consists of a current-reuse input stage with diode-connected load transistors, resulting in a gain set by the transconductance ratio g_{m1}/g_{m1L}. The transconductance of the input stage g_{m1} is defined by the tail current, which is shared by the NMOS and PMOS pair to improve the power efficiency [40]. This tail current is varied as a function of the gain-control voltage V_{TGC} (details provided in Section IV-C) to obtain the required variable gain. Besides maintaining constant bandwidth, this scheme also saves power, by ensuring that the input stage is biased at the highest current level only at the high end of the gain range, where the lowest input noise is required, in line with the noise requirement discussed in Section III-D. For lower gain levels, at which a higher input noise is acceptable, the bias currents are reduced.

At the chosen bias point, the input transistors suffer from relatively low output impedance and large gate–drain capacitance, which degrades the gain and increases the input-referred noise. To mitigate these effects, cascade transistors are employed.

A similar second stage provides additional gain g_{m2}/g_{m2L}. In this case, the input is a current-reuse stage without cascoding for simplicity. Again, a tail current dependent on V_{TGC} is used to obtain the overall desired variable gain. Each stage has its own common-mode feedback circuit (CMFB) to maintain a proper dc biasing point.

C. Transconductance-Control Circuit

The circuit that generates the bias currents for the loop amplifier as a function of V_{TGC} is shown in Fig. 12. A current steering mechanism similar to that used in the gain-control circuit (Fig. 9) is employed, in which V_{TGC} is compared to reference voltages by means of differential pairs. For each stage of the loop amplifier, three PMOS differential pairs are used of which the tail currents add to the bias current when V_{TGC} drops below the respective reference voltage. The tail current levels and reference voltage levels (derived from the resistive divider shown in Fig. 9) have been chosen based on the simulation to obtain a near-constant closed-loop bandwidth and sufficient phase margin.

V. Experimental Results

A. Experimental Prototype

The ASIC has been fabricated in 0.18-μm HV BCDMOS process. The ASIC consists of 64 RX and TX channels, each of which interfaces with one element of a 64-element CMUT transducer array. Each RX channel consists of the proposed TIA and a cable driver [41] and is powered by a $\pm$0.9 V analog supply and a 1.8 V logic supply. Each TX channel has a programmable HV pulser to generate pulses with a maximum amplitude of $\pm$30 V and an HV transmit/receive (T/R) switch to protect the low-voltage RX circuits during pulse transmission. Details of the TX-channel circuitry have been reported in [42]. The channels are arranged in two rows with 32 blocks in each row. This arrangement enables direct pitch-matched connection to the 64-element CMUT transducer array. Fig. 13 shows a photograph of the chip. The proposed TIA occupies an area of 0.12 mm^2.

B. Electrical Characterization Results

To measure the TIA's transfer function, an input current was generated by applying a voltage signal to a 15-pF off-chip capacitor, which mimics the CMUT capacitance, connected to the TIA's input. Fig. 14(a) shows the measured transfer

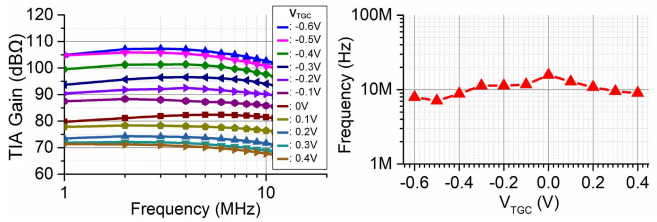

Fig. 14. (a) Measured transfer function and (b) corresponding −3-dB bandwidth as a function of V_{TGC}.

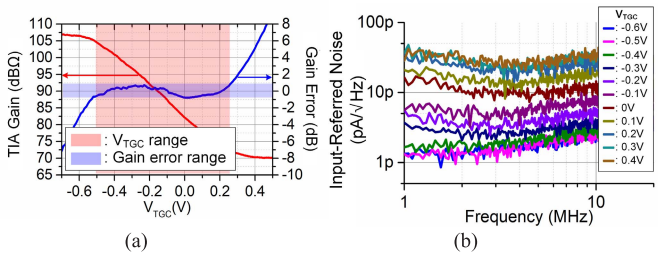

Fig. 15. (a) Measured gain at 5 MHz as a function of V_{TGC}, with the associated error compared to a linear-in-dB curve. (b) Input-referred noise spectrum.

function over the whole gain range. As shown in Fig. 14(b), the −3-dB bandwidth varies between 7.1 and 15.7 MHz across the gain range. Compared to the gain variation of almost 40 dB, the bandwidth is kept relatively constant, in good agreement with the designed adaptive gain operation of the loop amplifier.

Fig. 15(a) shows the TIA gain at 5 MHz as a function of the TGC control voltage (V_{TGC}). Note that, as expected, the gain decreases with increasing values of V_{TGC}, which in combination with a V_{TGC} that decreases with time leads to the desired gain that increases with time. The TIA gain can be varied continuously across a 37 dB range. The corresponding gain error with respect to an ideal linear-in-dB curve is less than ±1 dB across the middle 33 dB of the gain range.

The input-referred noise of the TIA was determined by connecting the same off-chip capacitor at the input of the TIA, measuring the output noise, and dividing it by the measured transfer function. The resulting input-referred noise spectra for different values of V_{TGC} are shown in Fig. 15(b). The noise floor is 1.7 pA/$\sqrt{}$Hz at 5 MHz at the highest gain, which is comparable to the CMUT noise floor. The measured spectra also demonstrate that the noise floor increases for lower TIA gains, as expected due to the adaptive biasing of the loop amplifier. At the lowest gain, the noise floor is about 30 pA/$\sqrt{}$Hz at 5 MHz. This increase of about 25 dB is less than the expected increase in the signal level of about 40 dB. Therefore, the SNR is not degraded by this gain-dependent noise floor.

This is confirmed by the DR measurement shown in Fig. 16(a), which shows the measured output SNR as a function of the input signal current for different values of V_{TGC}. The overall input DR, defined as the ratio between the input level at which 1-dB compression occurs at the lowest

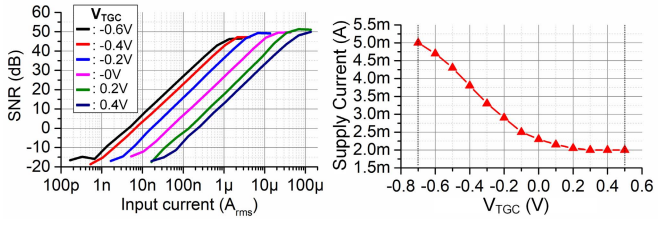

Fig. 16. (a) Measured SNR as a function of the signal amplitude for different values of V_{TGC}. (b) Measured supply current as a function of V_{TGC}.

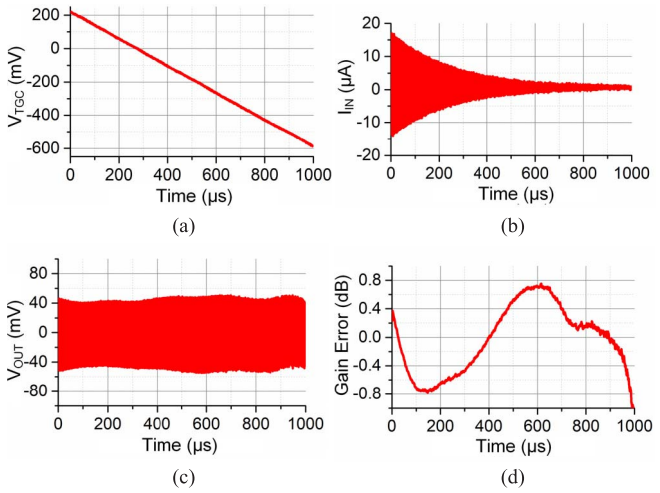

Fig. 17. Measured transient TGC operation. (a) Applied TGC control voltage. (b) Applied exponentially decreasing input signal. (c) Measured output signal. (d) Corresponding error with respect to a linear-in-dB gain curve.

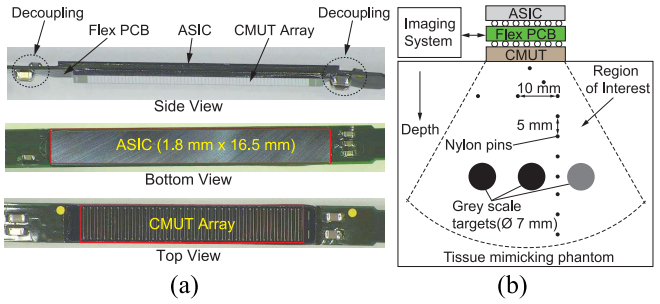

Fig. 18. (a) Implemented prototype. (b) Overview of the measurement setup used for acoustic characterization.

gain and the input level at which the SNR reaches zero at the highest gain, amounts to 82 dB. The variable gain reduces this to 46 dB at the output.

As expected due to the adaptive biasing, the TIA supply current also changes in a gain-dependent manner, as shown in Fig. 16(b). Assuming a linear variation of V_{TGC} as a function of time to cover the gain range, the variable supply current leads to an average power consumption of 5.2 mW.

Fig. 17 shows the measured transient behavior of the continuous TGC operation. A continuous sinusoidal input current with a frequency of 7 MHz and an exponentially decreasing amplitude, and a corresponding ramp signal are applied to

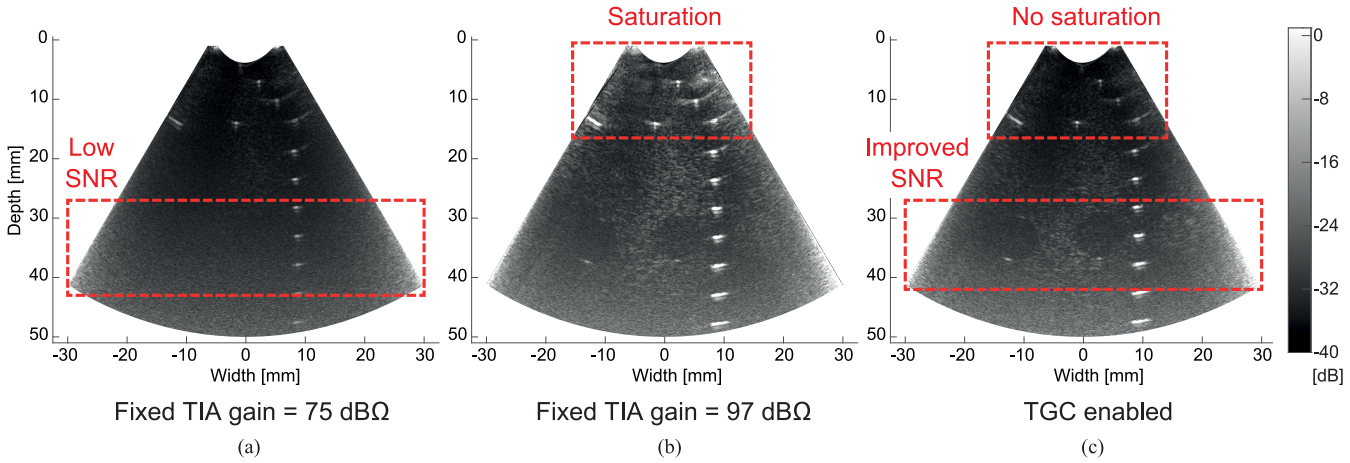

Fig. 19. Phased-array B-mode images with a ±45° opening angle, obtained with (a) fixed low gain, (b) fixed high gain, and (c) proposed continuous TGC operation.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This work	[42]	[44]	[45]	[46]	AD8332 [47]	VCA2617 [48]
Process	**0.18 µm HV BCDMOS**	0.18 µm HV BCDMOS	0.18 µm HV CMOS	0.35 um CMOS	BCD-SOI	-	-
BW	**7MHz**	16MHz	10MHz	40MHz	11MHz	100MHz	50MHz
LNA type	**TIA**	TIA	TIA	TIA	TIA	Voltage amp	Voltage amp
Max gain	**107dBΩ**	119dBΩ	116dBΩ	106dBΩ	78.4dBΩ	68.5dB	38dB
Full gain range	**37dB**	12dB	12dB	0dB	0dB	48dB	48dB
Gain error(1) (gain range)	**± 1dB (33dB)**	± 3dB(2) (12dB)	± 3dB(2) (12dB)	-	-	± 0.3dB (42dB)	± 0.9dB (37dB)
Gain control	**Continuous**	Discrete	Discrete	Fixed gain	Fixed gain	Continuous	Continuous
Transducer capacitance	**15pF**	0.7pF	2 pF	0.09pF	9.2pF	-	-
Input referred noise	**1.7pA/√Hz @5MHz**	2.0pA/√Hz @13MHz	0.41pA/√Hz @ 5MHz	0.31 pA/√Hz @ 20MHz	5.1pA/√Hz @10MHz	0.74 nV/√Hz @5MHz	4.1nV/√Hz @5MHz
Power consumption	**5.2mW**	0.42mW	1.4mW	0.8mW	1mW	138mW	52mW
NEF'(3) [mP·√(mW/Hz)]	**0.78(4)**	1.23(4)	2.7	-	0.55	-	-

(1) Maximum deviation from the ideal linear-in-dB curve across the mentioned gain range
(2) Estimated from the discrete gain step
(3) NEF' = $p_{n,in}\cdot\sqrt{Power_{tot}}$ [44] where $p_{n,in}$ is the input-referred acoustic pressure noise spectral density averaged inside the passband
(4) Calculated by referring the measured noise to an equivalent pressure noise using the estimated transducer sensitivity

the TIA's input and the gain-control port, respectively. The measured output has an approximately constant and smoothly compensated output swing. The gain error extracted from the output amplitude variation is less than ± 1 dB, demonstrating the intended continuous linear-in-dB TGC operation.

C. Acoustical Experiments

Fig. 18(a) shows a fabricated prototype in which the ASIC and CMUT have been flip-chip bonded on a flexible printed circuit board (flex PBC). Each TX/RX channel on the ASIC directly interfaces with a CMUT element. The TIA outputs, buffered by the cable drivers, go to a Verasonics imaging system (Verasonics Inc., Redmond, WA, USA) [43] to record the received echo signals. The flex PBC also connects the power supplies, with local decoupling capacitors, to the ASIC, as well as digital control signals, which are provided by a field-programmable gate array (FPGA).

The test bench for imaging experiments is shown in Fig. 18(b). The implemented prototype is placed at the surface of a tissue-mimicking phantom (GAMMEX SONO404) with an attenuation coefficient of 0.5 dB/cm/MHz. The phantom contains nylon wires acting as point reflectors and gray-scale targets to evaluate the SNR in the image.

Fig. 19 shows ±45° phased-array B-mode images of the phantom with 64-channel TX and RX operation. Fig. 19(a) is obtained using a fixed TIA gain of 75 dB·Ω. As this gain is optimized for the near field, the circular gray-scale targets at larger depth are hardly distinguishable. When the gain is fixed at a higher value of 97 dB·Ω to improve the SNR at larger depth [Fig. 19(b)], the RX signal at the shallow depths suffers from saturation, leading to a too bright image. With continuous TGC, these issues are mitigated, leading to a higher quality image in which no saturation occurs and the gray-scale targets can be clearly distinguished from the surrounding speckle pattern [Fig. 19(c)]. This imaging experiment successfully

demonstrates the continuous TGC capability of the prototype.

Table I compares the proposed TIA with the prior art. Compared to commercial LNAs with continuous TGC function [46], [47], $>10\times$ lower power consumption is achieved. While some of this difference may be attributed to the proposed circuit architecture, it should be noted that these parts have quite different noise and bandwidth specifications and are not intended for in-probe integration. Compared to prior in-probe TIAs, which employ discrete steps or fixed gain [42]–[45], comparable performance is obtained, but with much wider gain range and without the imaging artifacts associated with gain switching.

VI. Conclusion

This article has presented a low-noise TIA with continuous TGC for ultrasound imaging applications. The TIA employs a capacitive ladder feedback network and interpolation by means of current steering to provide linear-in-dB gain control. The proposed architecture combines LNA and TGC functionality in a single feedback loop, leading to better power efficiency than solutions that employ a fixed-gain LNA followed by a TGC stage, in which the LNA needs to be able to handle the full input DR at its output. In order to accommodate the large variation in the feedback factor, a current-reuse loop amplifier with adaptive biasing has been introduced, which provides approximately constant closed-loop bandwidth and saves power by allowing higher input noise at the lower part of the gain range.

Compared to prior in-probe TIAs, which employ discrete steps or fixed gain, competitive noise efficiency and a wider gain range are obtained without gain-switching transients. The presented electrical measurements demonstrate continuous gain control that is linear-in-dB to within ± 1 dB. The imaging results obtained in combination with a 64-element CMUT transducer show reduced imaging artifacts and highlight that the presented topology is a promising solution for future in-probe ultrasound ASICs.

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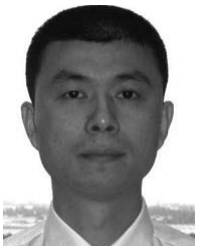

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