Integrated High-Side Current Sensors

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Integrated High-Side Current Sensors

Dissertation

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at Delft University of Technology

by the authority of the Rector Magnificus Prof.dr.ir. T.H.J.J. van der Hagen

Chair of the Board for Doctorates

to be defended publicly on

Tuesday 15, December 2020 at 12:30 o'clock

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LIST OF ABBREVIATIONS

AC	Alternating Current
ADC	Analog-to-Digital Converter
BCD	Bipolar-CMOS-DMOS
CCIA	Capacitively-Coupled Instrumentation Amplifier
CDS	Correlated Double Sampling
CHL	Low-Frequency Chopping
CM	Common-Mode
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common-Mode Rejection Ratio
DAC	Digital-to-Analog Converter
DC	Direct Current
DM	Differential-Mode
MOM	Metal-Oxide-Metal
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PSRR	Power Supply Rejection Ratio
PTAT	Proportional-to-Absolute-Temperature
RVG	Reference Voltage Generator
SFDR	Spurious-Free Dynamic Range
SNR	Signal-to-Noise Ratio
SNDR	Signal-to-Noise and Distortion Ratio
TCR	Temperature Coefficient of Resistance
TCS	Temperature Compensation Scheme
TS	Temperature Sensor
ΔΣ	Delta-Sigma

1. Introduction

1.1 Motivation and Objective

The internet of things (IoT) has greatly increased the use of sensors in today's world. A wide variety of sensors can be found in our smartphones, our homes and our working places. Current sensors are one of the most widely used types of sensors and will be the focus of this thesis. They measure the magnitude and the direction of a current flow, and can be found in a wide range of applications, such as:

- *Battery charge estimation in smartphones, tablets, laptops and other portable devices. This requires current sensors with high dynamic range. (Figure 1.1).*
- *Over-current protection due to fault operation and short circuits. This requires fast sensors with high-current capability.*
- *H-bridge motor control. This requires bidirectional current sensors with high-voltage and high-current capability.*

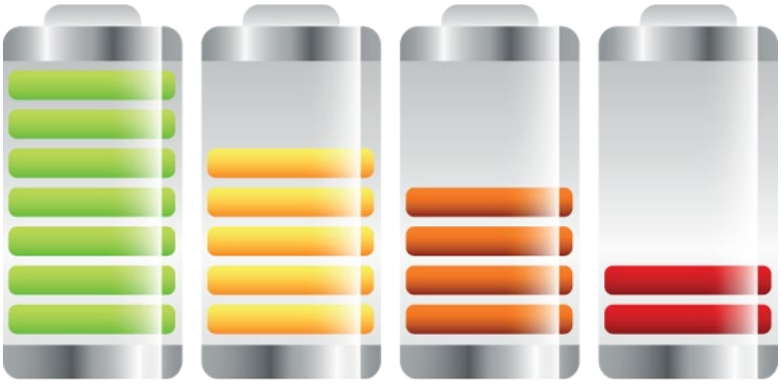


Figure 1.1. Battery charge estimation.

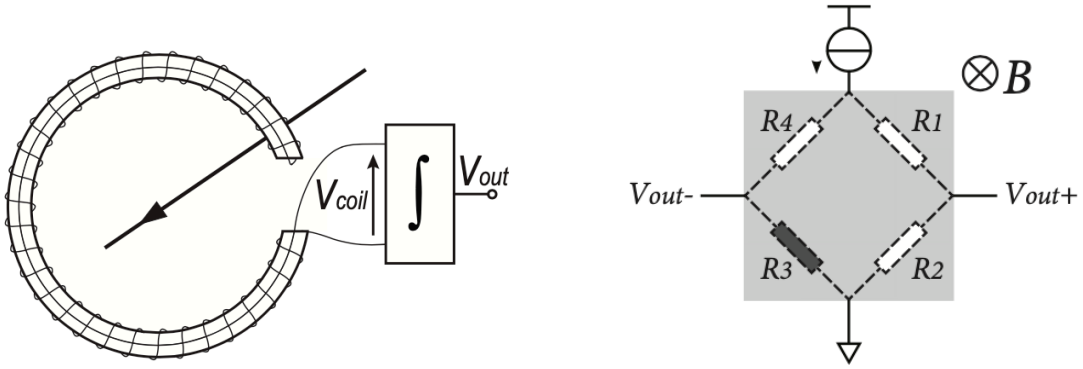
With more and more functions being integrated into our portable devices, the amount of PCB space allocated to each function (including current sensing) becomes increasingly limited. In addition, battery size is also limited. A good example of a space-constrained design is a wireless in-ear headphone, which must be small enough to fit into a human ear. Modern current sensors must therefore satisfy two main requirements. First, they should be compact and require no external components. Second, their power consumption should be as low as possible to avoid degrading battery life. This is especially important in portable electronic devices, in which current monitoring is an always-on requirement. The object of this thesis is then to develop fully integrated current sensors with low power consumption.

1.2 Background and Challenges

There are several different current sensing techniques. Each technique offers different current sensing ranges, and none are suitable for all applications. Depending on how the sensing element is connected to the monitored system, current sensing techniques can be classified into two categories: indirect and direct [1].

Most indirect current sensors use the fact that current flowing through a conductor will generate a magnetic field. Examples of such indirect sensing techniques include inductive sensors (e.g., using Rogowski coils) and magnetic field sensors (e.g. using Hall effect [2]). Inductive and magnetic sensors enable non-contact current measurements and are well suited for use in high common-mode (CM) voltage (>100V) and high current (>100A) applications. However, inductive sensors cannot sense DC currents, and both types of sensors are relatively complex and

expensive. Typically, they can achieve an 0.2%-5% sensing inaccuracy [1]. Another type of indirect current sensing can be found in some DC-DC converters [3]. In order to measure the large current (several tens Amps) of the output stage, it is first scaled down to a much smaller current by an active current mirror, and then converted to a voltage by a shunt resistor (Figure 1.3). In this way, the extra losses associated with directly inserting a shunt resistor in the high current path are avoided.



(a) (b)

Figure 1.2. Simplified diagrams of (a) a Rogowski coil and (b) a Hall effect sensor.

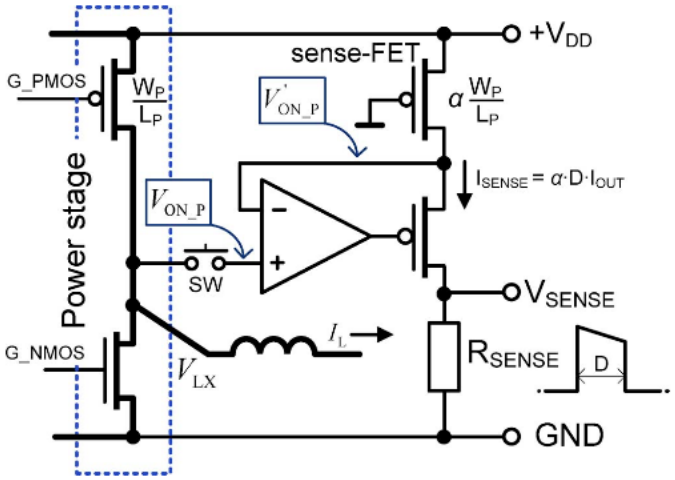


Figure 1.3. Simplified current sensing configuration in a DC-DC converter: from V. Michal [3].

Direct current sensing is based on Ohm's law of resistance. By placing a shunt resistor in series with a load, the current through the load can be determined by measuring the voltage drop across the shunt resistor (Figure 1.4). The shunt-based sensors can sense both AC and DC current with an inaccuracy of 0.1%-2% depending on what types of shunt resistors are used [1]. Although shunt resistors generate power loss and add circuit impedance, they are more widely used, mainly due to the following advantages:

- *Low cost*
- *Simple implementation*
- *High sensing resolution*

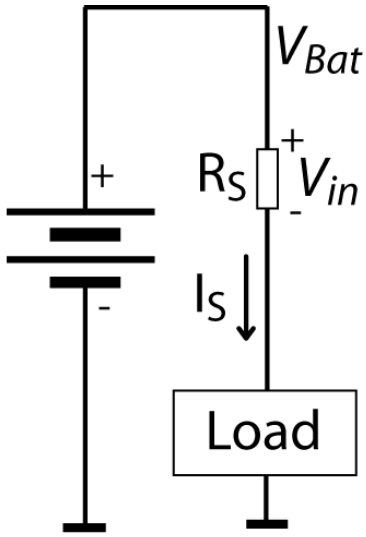


Figure 1.4. Shunt-based current sensing.

The focus of this thesis will be on the design of shunt-based current sensors. This involves meeting two main challenges.

The first relates to the input CM range (ICMR) of the current sensor's interface circuitry. Applications like over-current protection and motor

control require a wide ICMR (up to several tens of Volts). Since the shunt resistor is electrically connected to the monitored system, the interface circuitry of a current sensor must then be designed to safely handle large CM voltages [4-5]. The design of interface circuitry that can do this without consuming excessive power and silicon area is one of the challenges that will be addressed in this thesis. Previous solutions consume either high power (>9mW) [4] or large silicon area (>1.4mm^2 excluding ADC) [5].

The second is related to the co-integration of the interface circuitry and the shunt resistor. Most shunt-based current sensors consist of a discrete resistor with a low temperature coefficient of resistance (TCR) and a chip that houses the interface circuitry. This approach results in a large PCB area and, thus, high cost. To reduce this, shunt resistors can be integrated on the same chip or package with interface circuits. Either CMOS-compatible metal layers [7] or a lead-frame from a plastic package [8-10] can be used for this purpose.

One drawback of fully integrated resistors is their relatively large TCR (~0.3%/K). Some form of temperature compensation is then required to achieve decent inaccuracy over a wide temperature range, and in the presence of the significant Joule heating caused by large currents. The implementation of on-chip temperature compensation schemes with minimum power consumption and chip area is the second challenge that will be addressed in this thesis.

1.3 Performance Review of Commercial Current Sensors

Most work on shunt-based current sensors has been performed by industry. Major players in this field are Texas Instruments, Maxim Integrated and Analog Devices. Their early products consisted of a wide range of current sensing amplifiers [10-11], intended for use with off-chip shunt resistors. They generally offer low offset (<100μV), low gain error (<0.5%) and wide ICMR (0-100V) and high CMRR (>100dB) in order to accurately amplify small shunt voltages before further processing. To enable direct communication with a microcontroller, more recent products [12-13] also include an ADC to provide a digital output. Over the past few years, several products have been developed [14-15] that integrate shunt resistors and interface electronics into a single package to reduce PCB area. Table 1.1 summarizes the key performance specifications of these products. It can be seen that most modern current sensors provide the following two features:

- *Integration of an ADC to provide a digital output*
- *Co-integration of a shunt resistor*

However, integration of an ADC leads to greater supply currents (>100μA). In addition, products with integrated shunts typically exhibit more gain error than those using off-chip shunts. The main objective of this thesis is to design modern current sensors (with co-integrated ADCs and shunt resistors) that draw less supply current and have lower gain error. Some key target specifications are listed below:

1. Wide ICMR (>15V) to enable both low-side and high-side current sensing
2. Low offset (<100μV)
3. Low gain error (<1%)
4. Low supply current (<100μA)

Table 1.1 Performance summary of state-of-the-art current sensors

	INA210	MAX44284	MAX9611	ISSCC 2020	INA260	LTC2947
Shunt integration	No	No	No	No	Yes	Yes
ADC integration	No	No	Yes	Yes	Yes	Yes
Current sense range	N.A	N.A	N.A	N.A	±15A	±30A
ICMR	26V	36V	60V	60V	36V	15V
Gain error	1%	0.05%	0.5%	0.5%	0.5%	1%
Offset	35μV	2μV	500μV	5μV	10μV	4.5μV
Conversion time	N.A	N.A	2ms	N.A	8.2ms	100ms
Resolution	N.A	N.A	13μV	N.A	2.5 μV	0.9μV
Current	100μA	41.5μA	2.6mA	5-60μA	420μA	3.5mA

1.4 Organization of the Thesis

The remainder of this thesis is divided into four chapters.

Chapter 2 briefly compares the two main shunt-based current sensing configurations: high-side and low-side. This is followed by a brief review of various HV interface designs for high-side current sensing. In addition, several temperature compensation schemes are described, together with their pros and cons.

Chapter 3 introduces the beyond-the-rails ADC, which greatly simplifies the implementation of HV interface circuits for high-side current sensing. Based on this concept, two prototype ADCs [16-17] are presented with both circuits implementation details and measurement results.

Chapter 4 describes two novel temperature compensation schemes (TCS): analog TCS and hybrid (analog & digital) TCS. These schemes greatly simplify the system-level implementation of a current sensor and minimize overall power consumption. By combining these two schemes with a beyond-the-rails ADC, two fully integrated high-side current sensors have been realized [18-19]. Their circuit implementation is described, together with some experimental results.

Finally, chapter 5 concludes the thesis, and potential future work is presented at the end of the chapter.

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2. An Overview of Shunt-Based Current Sensors

In this chapter, the pros and cons of high-side and low side current sensing are discussed. The main challenge associated with high-side current sensing is the design of the interface circuits, which in contrast to low-side sensing, must be able to sense small differential voltages in the presence of large CM voltages. Thus, the chapter begins with an overview of the current state-of-the-art in HV interface design. This is followed by an overview of various types of shunt resistors and temperature compensation schemes.

2.1 High-Side Sensing versus Low-Side Sensing

Shunt-based current sensors can be used in both high-side and low-side configurations. Each of these has its own advantages and disadvantages.

As shown in Figure 2.1, a shunt resistor can be placed between the load and ground, or between the supply and the load. The former configuration is referred to as low-side current sensing, while the latter is referred to as high-side current sensing. High-side current sensing has two major advantages over low-side current sensing: First, it can detect load currents caused by accidental shorts to ground, and second, it does not increase the resistance in the ground path. However, the associated interface circuits must be able to handle large and dynamic CM voltages,

which makes their implementation more complex than for low-side current sensing. In the next section, several existing HV interface designs will be discussed.

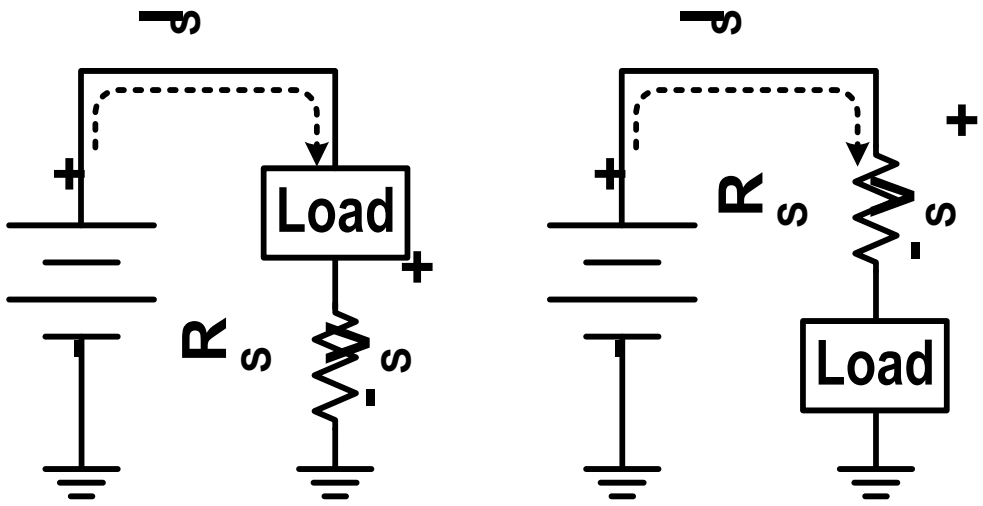

Figure 2.1. Low-side current sensing (left) and high-side current sensing (right).

2.2 An Overview of HV Interface Circuits for High-Side Current Sensing

Conventionally, interface circuits for high-side current sensing consist of a HV instrumentation amplifier (IA) with a wide ICMR. It shifts the small voltage drop across the shunt from a HV domain to a LV domain, in which it can be digitized by a conventional ADC (Figure 2.2). The HV IA thus isolates the ADC from large CM voltages, in addition, its gain relaxes the ADC's noise requirements.

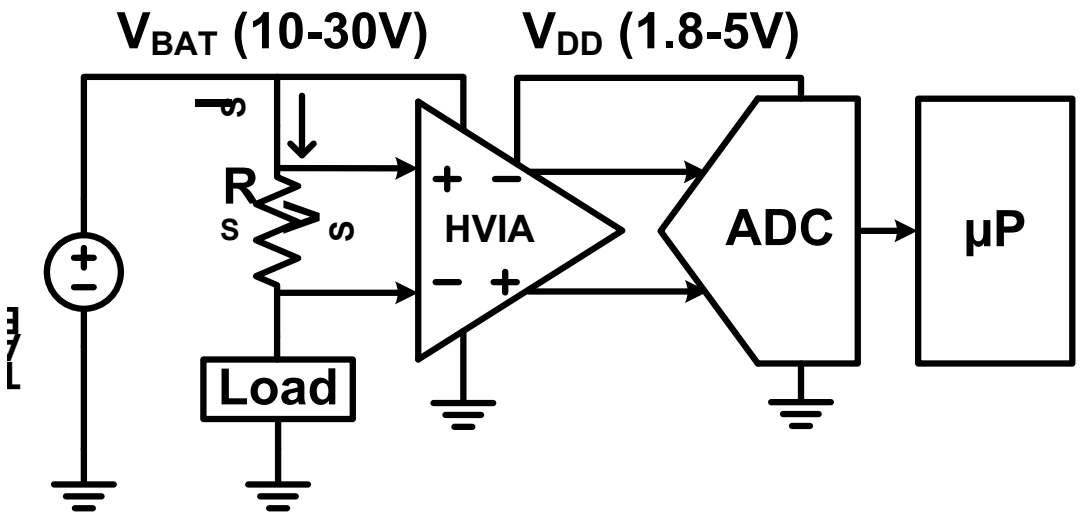

Figure 2.2. HV Interface circuits for high-side current sensing.

The most straightforward way of implementing a HV IA is as a resistive-feedback IA as shown in Figure 2.3. The resistive divider formed by resistors R_1 and R_3 attenuates the input CM, thus facilitating the use of a low-voltage opamp. However, its DC CMRR and gain inaccuracy are primarily limited by the matching of $R_{1\text{-}4}$. One of such designs [1] achieves 1% gain error and 100dB DC CMRR. In [2], the current-feedback topology is employed for high-side current sensing. (Figure 2.4). The input transconductor G3 and feedback transconductor G4 convert the input and feedback voltages into corresponding currents. Their difference is then nulled by the gain of Gm3. To handle large input CM voltages, its input transconductor Gm1 is powered from the HV domain, resulting in significant power consumption. It achieves a 30V ICMR while consuming 200µA from a 30V supply and another 650µA from a 5V supply. Also, it exhibits a 0.2% gain error and a 143dB DC CMRR.

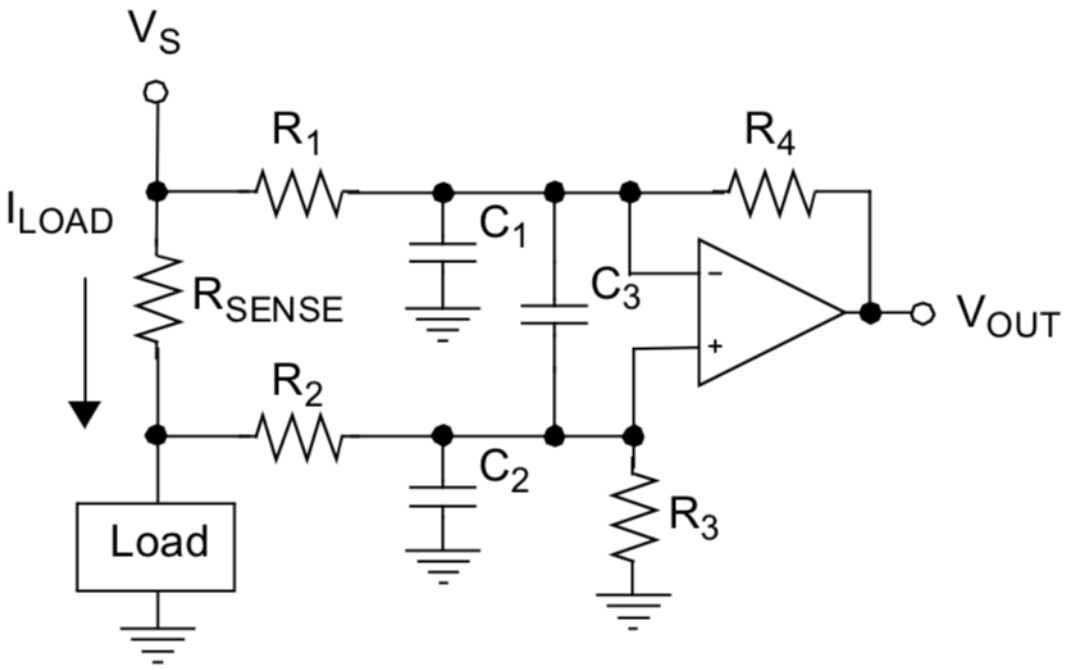

Figure 2.3. Resistive-feedback IA

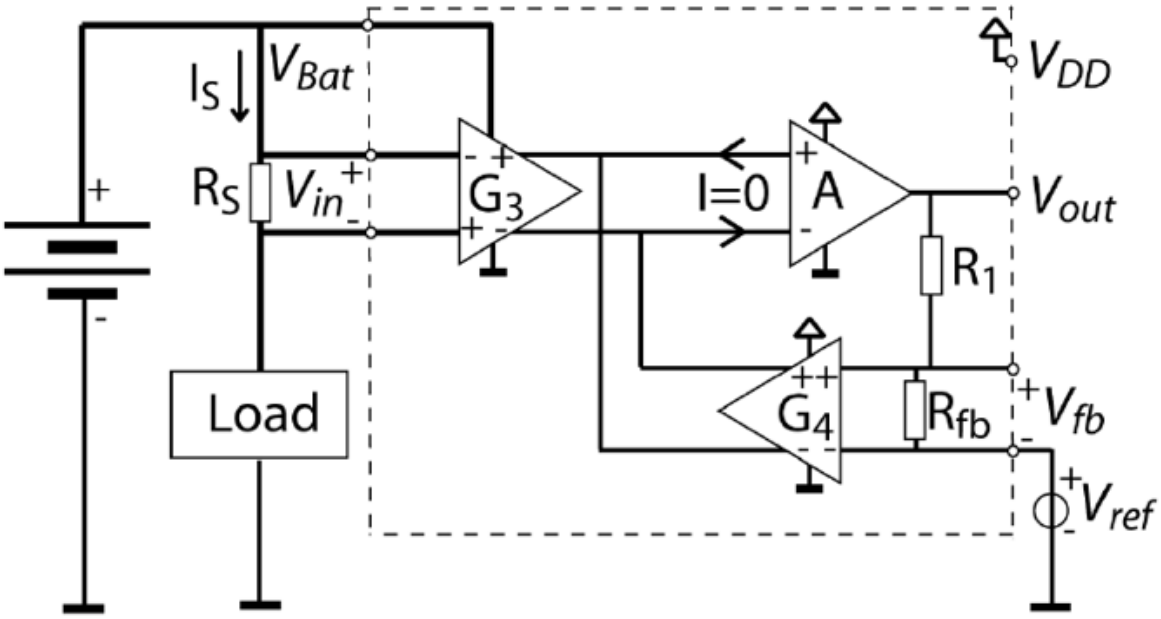

Figure 2.4. Current feedback IA.

The IAs developed in [3-4] are based on an inverting topology with capacitive feedback, combined with chopping technique (Figure 2.5). Originally developed for biomedical applications [5-7], this approach offers significant advantages in HV applications. The input capacitors block CM voltages, while the use of chopping allows the amplification of DC signals and simultaneously mitigates offset and 1/*f* noise. The metal-oxide-metal (MOM) capacitors available in most CMOS technologies provide effective HV-to-LV isolation, and can also be used to implement the capacitive feedback network. Therefore, a wide ICMR can be achieved without the need for an opamp with a HV input-stage. The design described in [4] achieve a ±30V ICMR while drawing only 78μA from a single 5V supply. Its gain error and DC CMRR are 0.13% and 160dB, respectively.

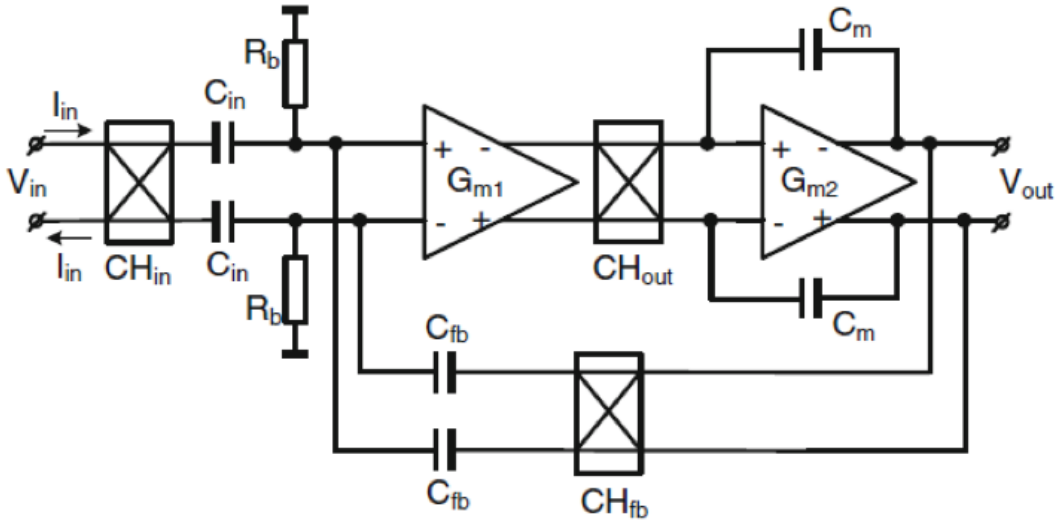

Figure 2.5. Capacitively-coupled IA.

In [10], a novel bootstrapped switch topology is proposed that enables a SAR ADC to handle both differential-mode (DM) signals and CM mode signals beyond its supply voltage. It achieves a 50V CM and DM range while consuming 1.3mA from a 3.3V supply. To accommodate large DM signals, HV DMOS transistors are used, which leads to increased chip area. Moreover, the large DM signal range leads to poor resolution in a small DM signal range which current sensing applications require.

2.3 An Overview of Shunt Resistors

In a shunt-based current sensing system, the shunt can be implemented with either off-chip or on-chip resistors. Bulk metal foil resistors, power metal strip resistors and thin-film resistors are the most commonly used off-chip resistors [11]. They have low (tens to hundreds of ppm/°C) temperature coefficients of resistance (TCR) and low tolerances (less than ±0.5%), but are relatively expensive and so are not suitable for low-cost applications. In [12], the use of a PCB copper trace is proposed as a low-cost alternative. However, the trace has a large TCR (~0.39%/°C), resulting in large errors due to the Joule heating associated with high current levels. Compensating for such errors is complicated by the difficulty in ensuring good thermal coupling between a PCB trace and an on-chip temperature sensor. Similarly, the metal layers of a CMOS chip [13-17], its bond wires [18-19], or its lead-frame [20-23] can be used to make low-ohmic (from sub-mΩ to 10mΩ) shunts. Compared to off-chip resistors, these have two main advantages: lower cost and smaller footprint (no external components). However, above mentioned on-chip resistors suffer from large TCR (>0.3%/°C), and so an efficient temperature compensation scheme is usually essential to achieve

reasonably low inaccuracy. A notable exception is the lead-frame shunt described in [23], which achieves low TCR by using a relatively expensive, non-copper lead-frame.

2.4 An Overview of Temperature Compensation Schemes

Temperature compensation of an on-chip shunt can be implemented either in the analog domain [17], [21] or in the digital domain [13-16]. In [17], the shunt's TCR is compensated by the ADC's reference buffer, which is a resistive-feedback amplifier. Two types of resistors are utilized in the feedback network to make the temperature dependency of the buffer match that of the shunt, thus cancelling the effect of self-heating errors at the ADC's output. Since the current sensor in [17] is embedded in a class-D amplifier, its current sensing performance is not discussed in the paper. Similarly, an amplifier with a temperature-dependent resistive-feedback network can be used to amplify the shunt voltage before it is digitized [21]. To compensate for the shunt's TCR, its gain is designed to have an equal-but-opposite temperature coefficient and the spread of the shunt resistance is also corrected by trimming the amplifier's gain. This approach achieves a 3% gain error over a ±15A range. Digital compensation schemes developed in [13-16] share the similar basic principle. As shown in Figure 2.6, the shunt's temperature is sensed by an on-chip temperature sensor and this information is used to correct the ADC's output with the help of a 2^{nd}-order polynomial engine. Two designs presented in [15] exhibit same 0.3% gain error over a ±5A range and a ±36A range, respectively.

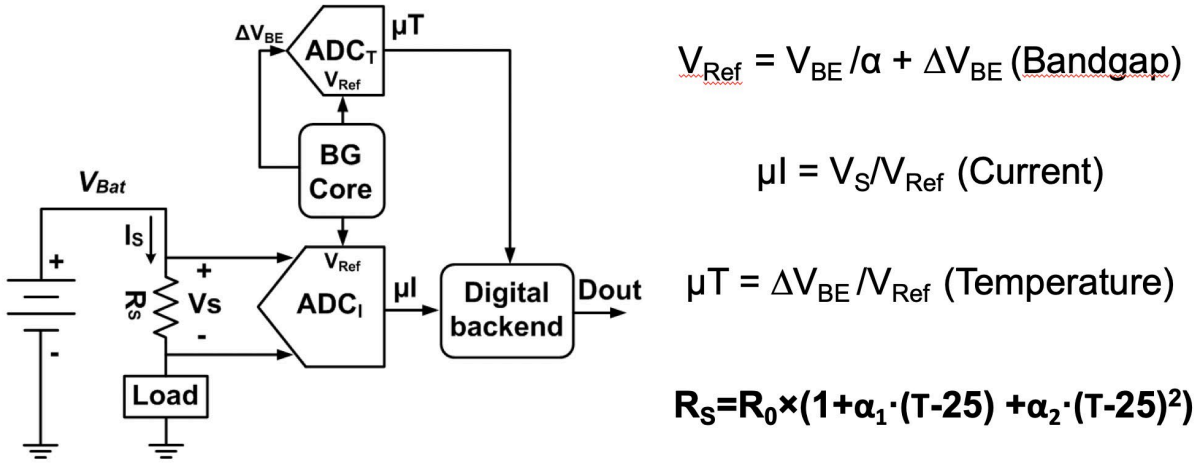

Figure 2.6. Digital temperature compensation scheme.

2.5 Conclusion

This chapter presents an overview of HV interface circuits and temperature compensation schemes. Both of them are core elements of a fully integrated current sensor, and largely determine the power, cost and area of the entire sensor system.

Although the power efficiency of HV IAs has been improved by using more advanced topologies [2-3], they still consume a significant amount of chip area. To eliminate the need for HV IAs, one of the main goals of this thesis is to develop a HV ADC which can directly digitize small differential signals in the presence of large CM voltages while operating with a low supply voltage (Figure 2.7). Since such ADCs can have an ICMR which is greater than the supply voltage or less than ground, it is called the beyond-the-rails ADC.

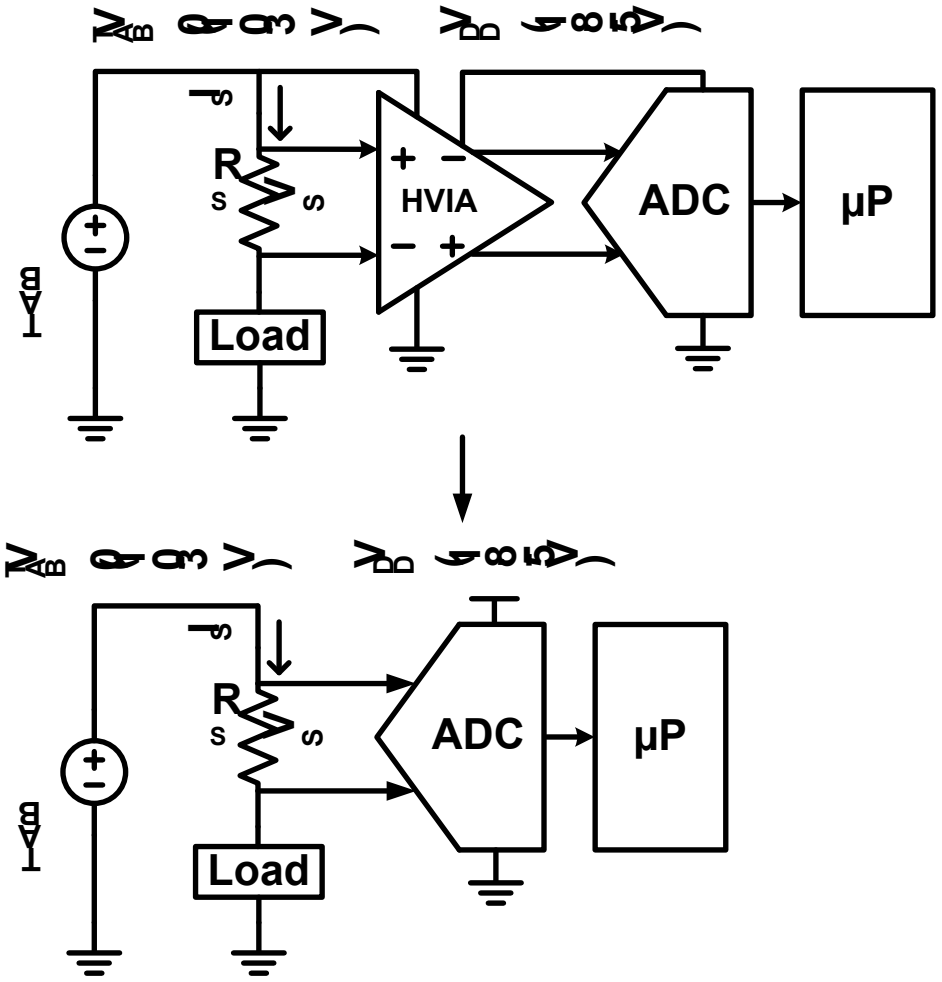

Figure 2.7. High-side current sensing interface design with beyond-the-rails ADC.

In terms of temperature sensor schemes, the implementation of analog compensation schemes is simpler than that of digital ones since there is no need for digital backend to post-processing the ADC output. However, extra resistive-feedback IAs are still needed in existing schemes [17], [21], which results in increased complexity and power consumption. Digital temperature schemes [13-16] achieve superior inaccuracy with the help of temperature sensors. Temperature sensing inaccuracy has a major impact on the current sensing inaccuracy. Dynamic offset cancellation techniques are required to achieve reasonably small temperature sensing inaccuracy. In order to further reduce their power

consumption and complexity, an improved analog scheme and a hybrid analog/digital schemes have been developed in the work described in this thesis.

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3. Beyond-the-Rails ADC for High-Side Current Sensing

In this chapter, the beyond-the-rails ADC concept is introduced, and the design of its key building block, a HV chopper, is described. Two prototype ADCs [1-2] are presented, both of which achieve a high resolution and a wide ICMR, while operating from a low supply voltage. This makes them suitable for high-side current sensing applications.

3.1 Basic Concept

A beyond-the-rails ADC is similar to a capacitively-coupled instrumentation amplifier (CCIA) in that capacitors are used to isolate a low-voltage front-end from large CM voltages. The front-end consists of a switched-capacitor (SC) integrator (Figure 3.1), which is an elementary building block of discrete-time ΔΣ ADCs. It employs the same front-end structure as a CCIA: an input chopper followed by a pair of capacitors. The input chopper CH_{IN} samples input signals in a cross-coupled fashion such that a charge proportional to the differential input signal is transferred to the integration capacitors $C_{I1,2}$, while the input CM voltage is blocked by the sampling capacitors $C_{S1,2}$. By using such integrators, a beyond-the-rails ΔΣ ADC can be realized, whose ICMR is mainly limited by the voltage rating of the capacitors used. Although this sampling scheme has been used to improve the SNR of ΔΣ ADCs by effectively doubling the signal amplitude across the input sampling capacitors $C_{S1,2}$ [3], its potential to extend the ADC's ICMR has not been previously explored.

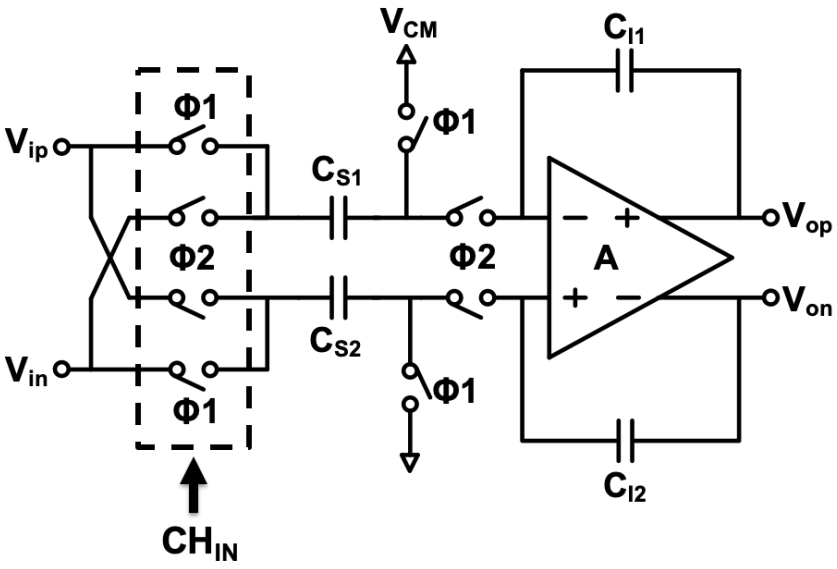

Figure 3.1. SC integrator with cross-coupled sampling scheme.

In a HV BCD technology, $C_{S1,2}$ can be implemented as HV fringe capacitors with large breakdown voltages (up to several tens of volts). However, the input chopper CH_{IN} must also be able to accurately and reliably handle small differential input signals in the presence of large CM voltages. The following section will describe the detailed implementation of CH_{IN}.

3.2 HV Input Chopper

The core of the HV input chopper is similar to the one developed for a HV CCIA [4]. A simplified schematic of the CH_{IN} is shown in Figure 3.2. It is driven by two non-overlapping clocks Φ1L and Φ2L, which are generated by LV (1.8V/5V) logic. They are capacitively-coupled to the gates of four sampling switches $M_{1\text{-}4}$ via a level shifter composed of two HV capacitors $C_{1\text{-}2}$ and a latch $M_{5\text{-}6}$. Due to the cross-coupled sampling scheme, $M_{1\text{-}4}$ can share one set of coupling capacitors. This leads to a more compact implementation than that proposed in [5], in which each switch needs a separate bootstrap capacitor.

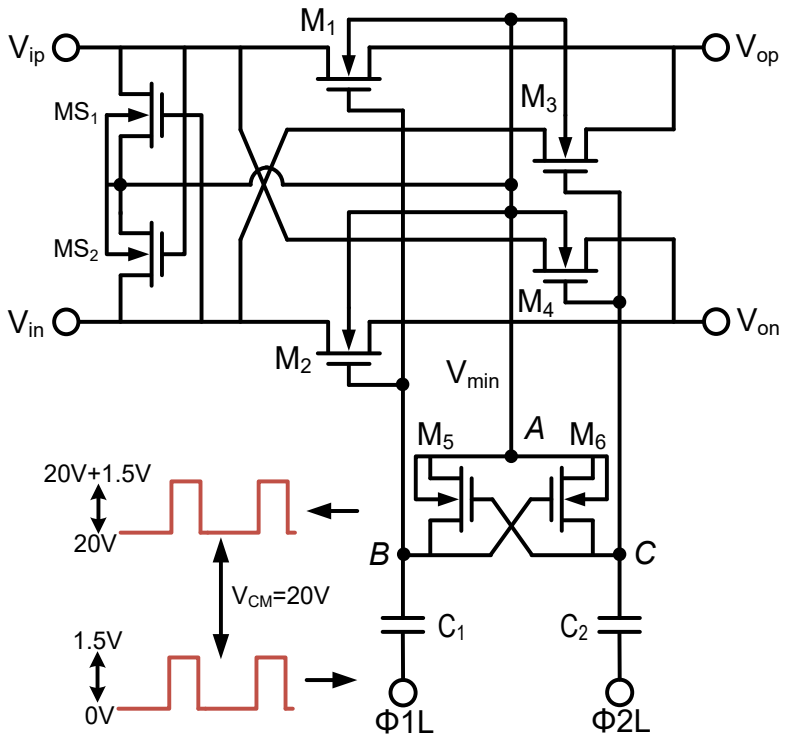

Figure 3.2. Simplified schematic of the HV input chopper CH_{IN}.

In [4], the reference node of the level shifter (the source terminals of $M_{5\text{-}6}$) is tied to one of the input terminals (e.g., V_{ip}) such that the coupled clock is always superimposed on V_{ip}. If V_{ip} is higher than V_{in}, the gate-source voltages (V_{GS}) of M_2 and M_4 will still be slightly positive ($\approx V_{ip}$-V_{in}) when they are supposed to be off. This results in a certain leakage current, especially at high temperatures. Moreover, the bodies of $M_{1\text{-}4}$ are tied to their sources, which in turn creates parasitic diodes between CH_{IN}'s input and output terminals and also contributes extra leakage current.

As discussed in [6], the leakage current of the chopper switches can degrade the inaccuracy of bidirectional current sensing. To prevent this, a minimum selector $M_{S1\text{-}2}$ is inserted between the input terminals V_{ip} and V_{in}, to select the lowest input voltage. Its output (node A) is tied to the reference of the clock level shifter such that the coupled clocks are always superimposed on V_{min} (the lower of V_{ip} and V_{in}). It ensures that

V_{GS} of $M_{1\text{-}4}$ will always be equal or less than zero when they are off. In addition, the body of each switch is also connected to node A which prevents forward biasing of their parasitic diodes.

To further reduce their channel leakage current, both the sampling switches $M_{1\text{-}4}$ and the latch $M_{5\text{-}6}$ are implemented with high-Vth NMOS devices, while the minimum selector $M_{S1\text{-}2}$ is made from low-Vth devices to extend its operational range. All of them are isolated by a semi-floating HV N-well (HVNW), which forms two back-to-back connected parasitic diodes D_{P1}, D_{P2} with the local P-well (LPW) and the P-substrate (PSUB), respectively (Figure 3.3). The LPW is connected to one of the input terminals via the minimum selector. If the input CM voltage rises, D_{P1} will ensure that the potential of the HVNW will follow. In this case, D_{P2} will be reverse-biased and so its breakdown voltage determines the upper limit of the ADC's ICMR. When the input CM voltage drops below ground, the HV PNP transistor connected to the HVNW will turn on and the potential of the HVNW will be clamped at V_{dd} (1.5-5V). This ensures that D_{P2} is always reverse-biased to prevent potential latch-up. Meantime, D_{P1} is reverse-biased and so its breakdown voltage sets the lower limit of ICMR. The breakdown voltages of D_{P1} and D_{P2} are determined by the chosen process (70V in a 180nm HV process). The leakage currents at both input nodes are almost identical because of the small differential input voltage (< ±100mV for current sensing applications), and it will appear as a common-mode disturbance.

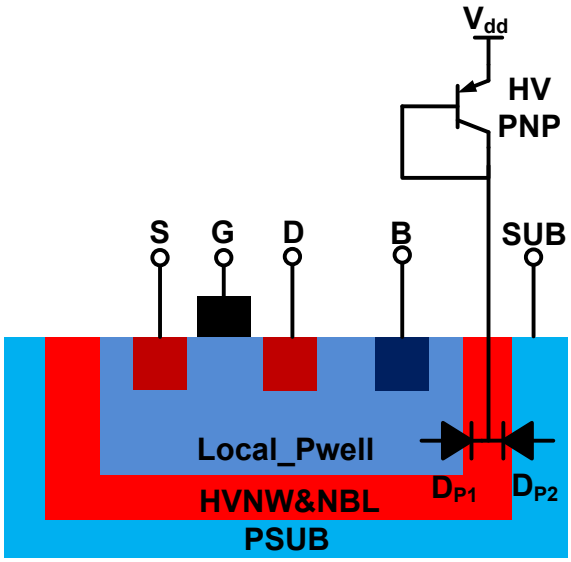

Figure 3.3. Cross section of the isolated NMOS transistor in CH_{IN}.

Figure 3.4 shows the schematic of CH_{IN} with extra protection circuits. Four diodes $D_{1\text{-}4}$ are added in parallel with $M_{1\text{-}4}$ to limit their drain-source voltages when a large input CM transient presents. In addition, a current mirror composed of $M_{7\text{-}9}$ and another coupling capacitor C_3 are added to protect the gates of $M_{1\text{-}4}$. When the input CM voltage (source voltage of $M_{1\text{-}4}$) drops rapidly, the voltage at node A (V_{min}) will follow via the minimum selector, which turns on the transistor M_8. Then the transistors M_7, M_9 will mirror the operation of M_8 and lower the voltages at nodes B and C (gate voltage) to limit the V_{GS} of $M_{1\text{-}4}$. When the input CM voltage rises, V_{min} also rises via the minimum selector, and the parasitic diodes D_{BD1}, D_{BD2} between $M_{5\text{-}6}$'s bodies and drains will limit the source-gate voltages (V_{SG}) less than the threshold voltage of these diodes.

This chopper scheme will be used in two protype ADCs presented in the following sections.

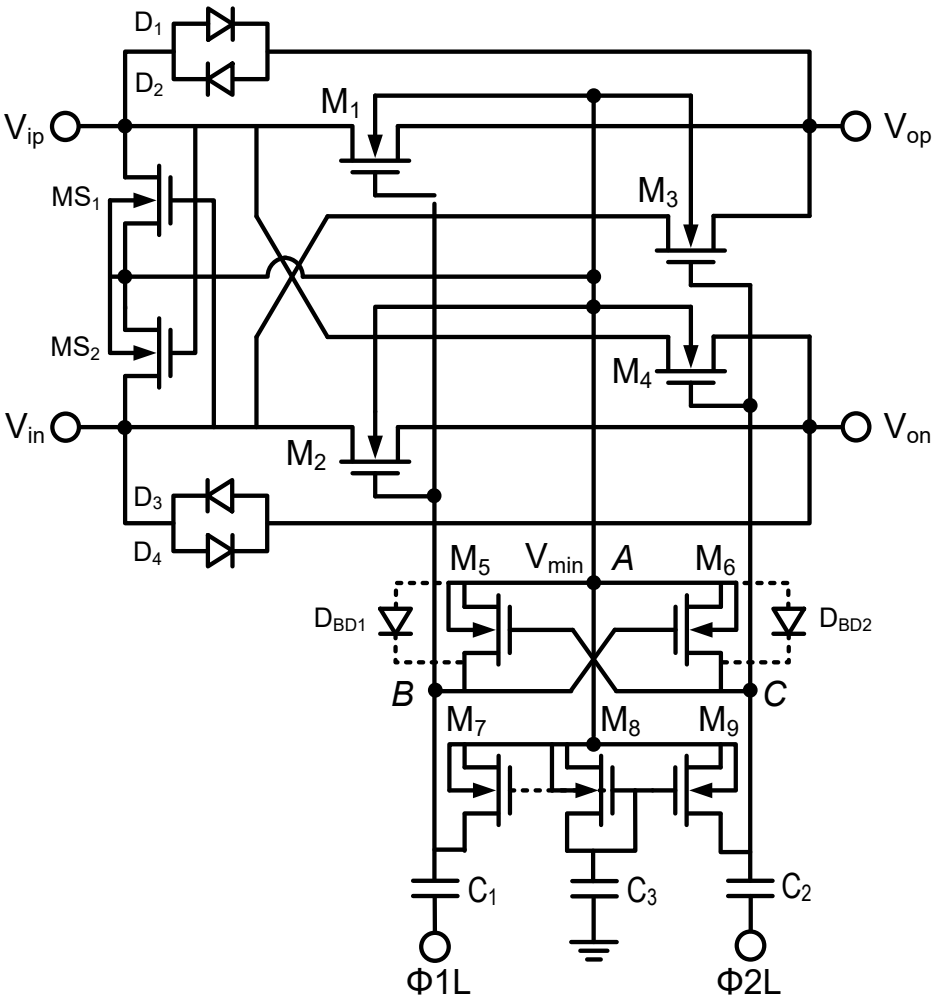

Figure 3.4. Schematic of CH_{IN} with extra protection circuits.

3.3 Prototype ADC I

This section presents the first prototype of a beyond-the-rails ADC [1]: ADC I. It is targeted for battery charge estimation (based on high-side current sensing) where high resolution and low offset are required. A wide ICMR is obtained by the HV chopper described in the previous section. Several dynamic offset cancellation techniques are used to achieve low offset and good CMRR.

3.3.1 Circuit Implementation

Figure 3.5 shows the block diagram of the ADC I. It consists of a single-loop single-bit SC ΔΣ ADC with a feed-forward architecture. ADC I samples at 150kHz and uses a 5pF sampling capacitor to achieve a 110dB SNR (thermal noise limited) over a 100Hz BW. A 3rd-order loop filter is chosen to ensure the quantization noise is well below the thermal noise. An inner set of HV choppers (CH_{in}), together with switches Φ1 and Φ2, implements a correlated double sampling (CDS) scheme that mitigates the effect of the 1st OTA's offset and 1/*f* noise. Further offset reduction is obtained with the help of an outer set of HV choppers (CH_{sys}), which together with a digital chopper at the modulator's output, implement a system-level chopping scheme. During Φ1, the input signal Vin and the OTA's offset are sampled on the input capacitors C_s. During Φ2, the HV chopper (CH_{in}) reverses the input and thus transfers a charge packet proportional to $2 \cdot C_s \cdot V_{in}$ to the integration capacitors C_{int}. The input capacitors are implemented as HV fringe capacitors with a breakdown voltage of 80V. The feedback capacitors are also implemented with the same type of capacitors, to ensure good matching and hence, low gain inaccuracy.

The 1st integrator is implemented around a folded-cascode gain-boosting OTA, which achieves 120dB DC gain and draws 40μA. Its unity-gain bandwidth is 2MHz to meet the settling requirement. The 2nd and 3rd integrators are scaled down to improve power efficiency. They are built around single-stage folded-cascode OTAs, each of them has a gain of 90 dB and draws only 5μA. The comparator is composed of a pre-amplifier and a dynamic latch. For flexibility, the decimation is performed by an off-chip 512-tap sinc^3 filter.

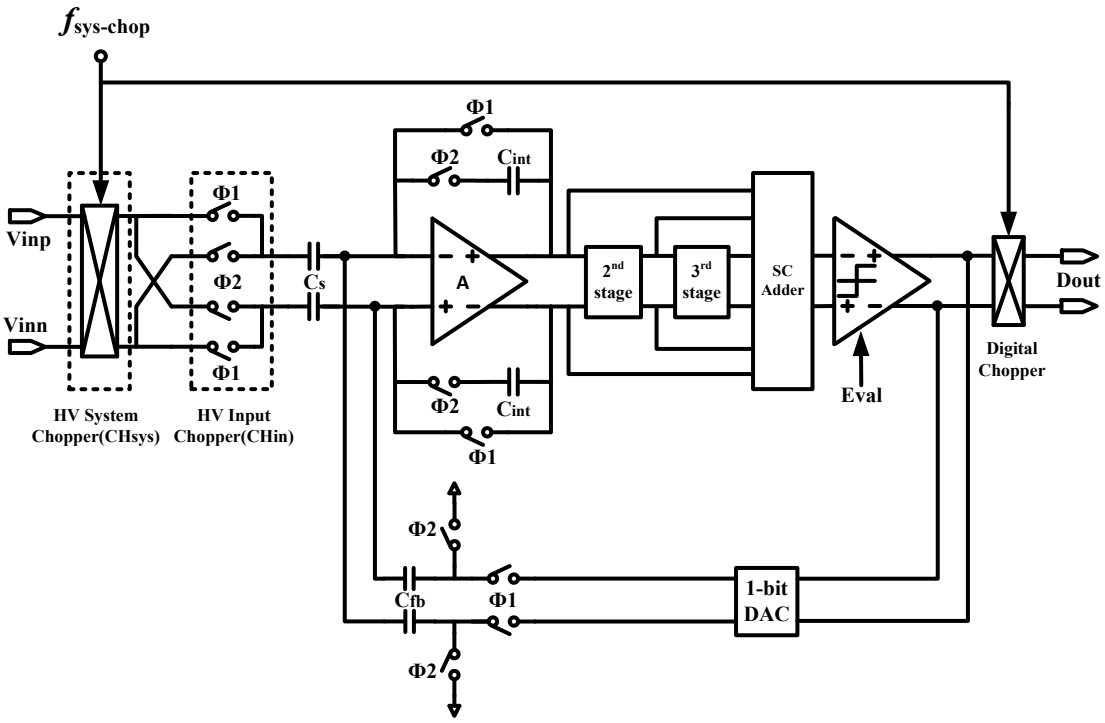

Figure 3.5. Block diagram of the ADC I.

3.3.2 Experimental Results

ADC I was realized in a HV 0.18μm CMOS process (Figure 3.6). It occupies an active area of 0.8mm^2 and draws 101 μA from a 5V supply. The sampling frequency is 150kHz and the signal bandwidth is 100Hz. Figure 3.7 gives the 2^{22}-point FFT output spectrum for a -6.2dB input signal (relative to the ADC's 2.8V reference) that is superimposed on a 25V CM voltage. Figure 3.8 shows the measured SNR/SNDR versus input amplitude. The peak SNR, SNDR and SFDR are 110.1dB, 100.6dB and 100.8dB respectively. The ADC's ICMR is limited to ±30V by the ESD diodes at input terminals. The peak SNDR only varies by 0.5dB over the ±30V ICMR, demonstrating the excellent linearity of the HV chopper over the full ICMR. Figure 3.9 depicts the ADC's low-frequency characteristics obtained from 15 samples. Its offset is less than 250μV with CDS alone, which improves to 8μV after system-level

chopping (at 0.5Hz), and, in both cases, changes by less than ±2μV over the full ICMR. The ADC's gain inaccuracy is lower than 0.6%, while its DC CMRR is always greater than 140dB. Although the CMRR rolls off with frequency, it is still greater than 110dB and 72dB at 0.5Hz and 50Hz, respectively (Figure 3.10). The ADC's performance is summarized in Table 3.1.

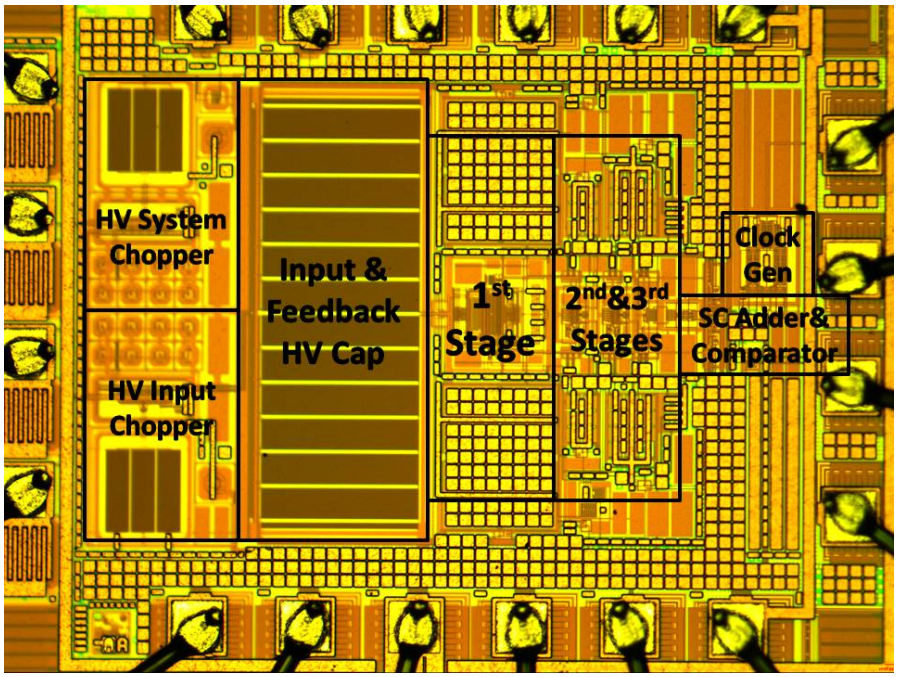

Figure 3.6. Chip micrograph.

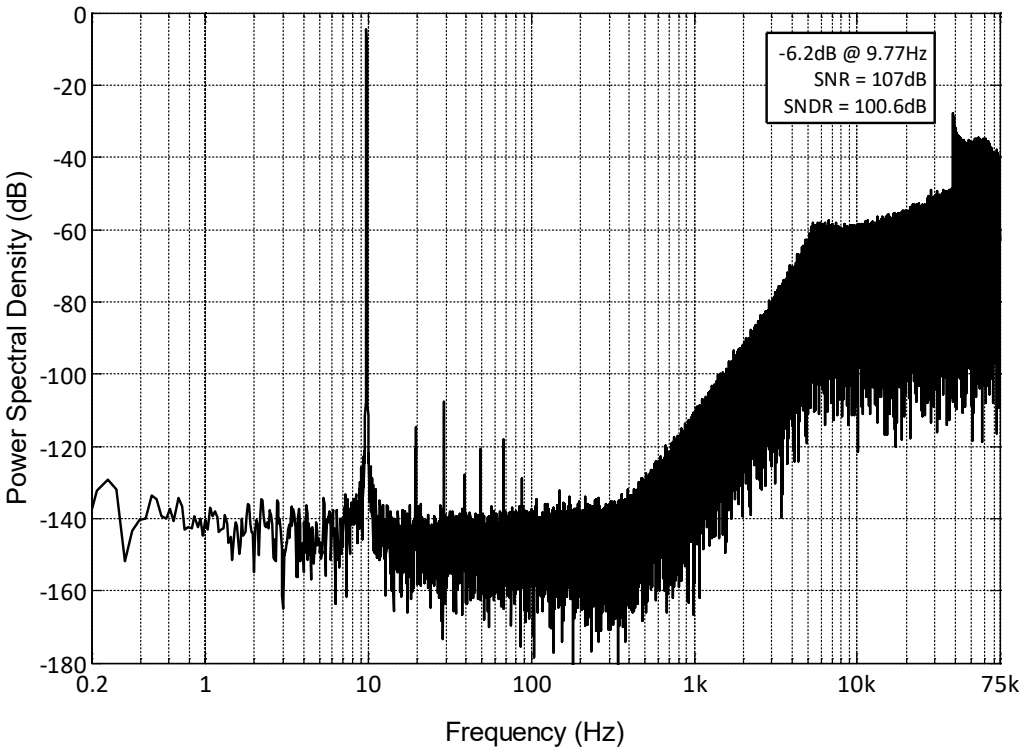

Figure 3.7. Measured 2^{22}-point FFT of the ΔΣ modulator's output (V_{CM}=25V).

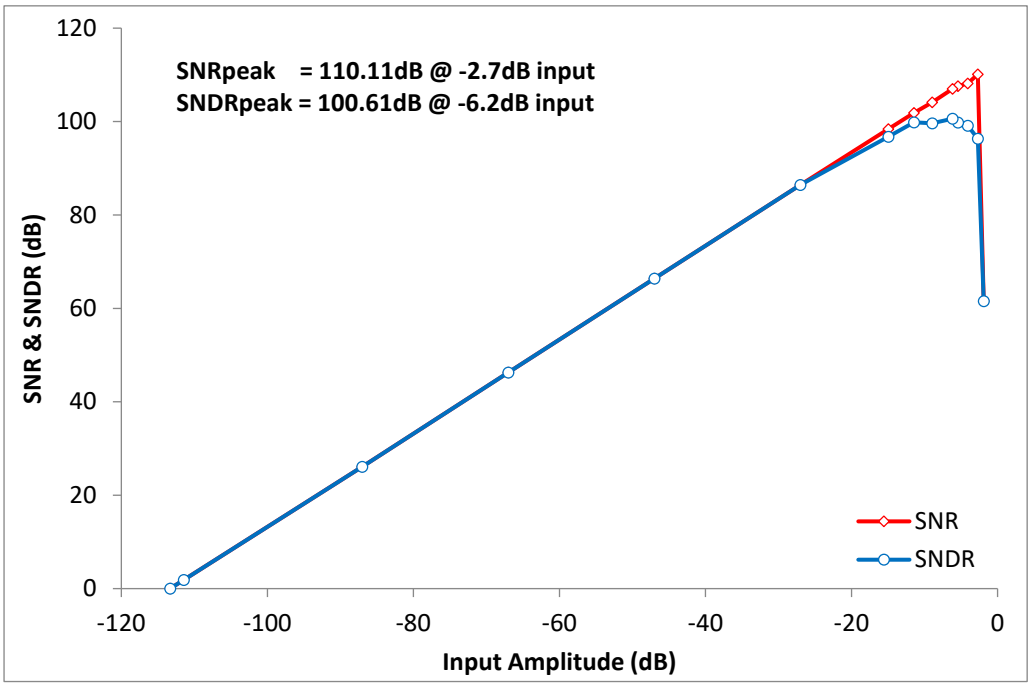

Figure 3.8. SNR and SNDR versus input amplitude.

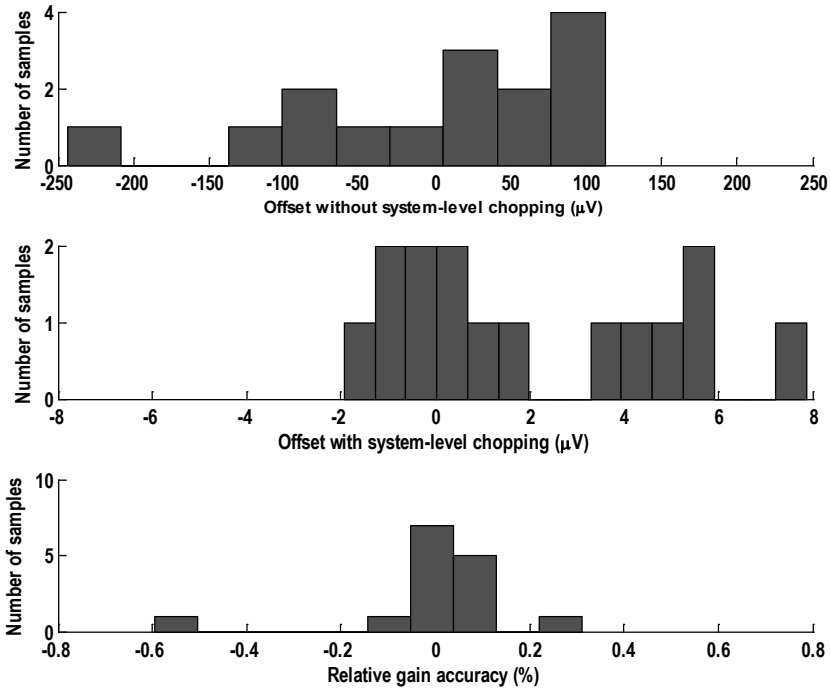

Figure 3.9. Histograms (15 samples) of the measured offset (with and without system-level chopping) and the relative gain error.

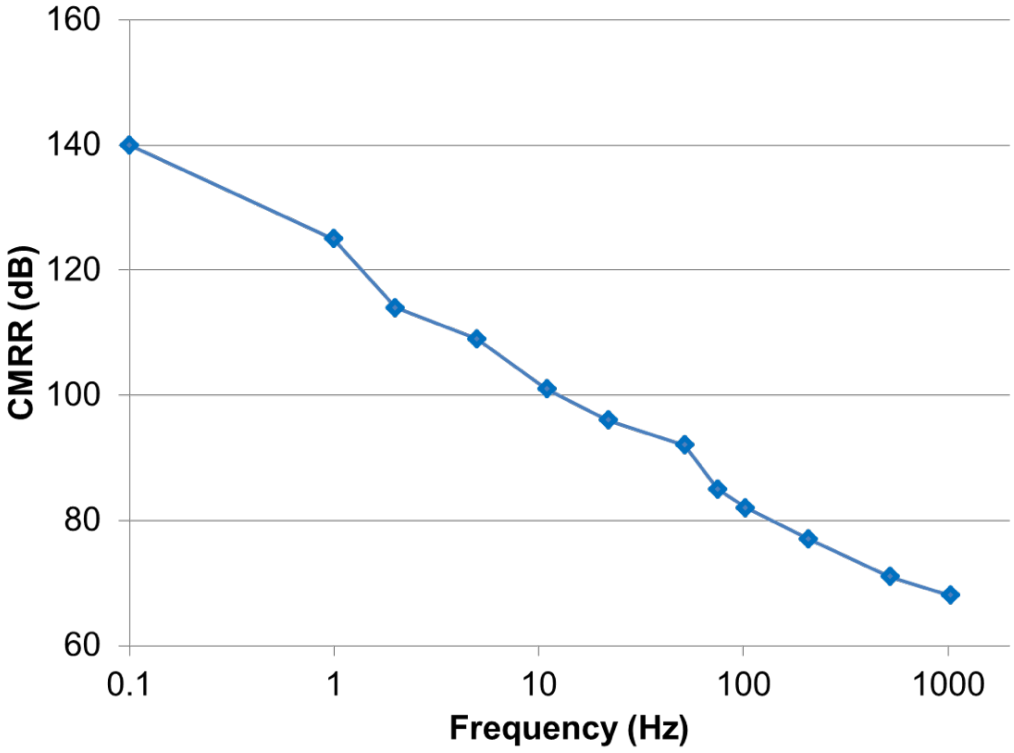

Figure 3.10. Measured CMRR over frequency.

Table 3.1. Performance summary

	ADC I [1]
Supply voltage	5V
Input CM range	±30V
Input DM range	$4.4V_{p\text{-}p}$
SNR	110.1dB
SNDR	100.6dB
SFDR	100.8dB
BW	100Hz
Offset	8μV
CMRR (@DC)	140dB
PSRR (@DC)	80dB
Chip area	$0.8mm^2$
Power	505μW

Note: SNR, SNDR and SFDR of the ADC I are measured with a 9.9Hz input signal.

3.4 Prototype ADC II

Although ADC I achieved the beyond-the-rails capability, it suffered from limited bandwidth and AC CMRR. A bandwidth of several kHz may be required to track fast current peaks. Moreover, in applications where large CM voltage transients may occur, e.g. in motor current monitoring, an ADC with a high AC CMRR is required. The second prototype ADC II addresses these two issues by operating the ADC at a higher sampling frequency and adopting a different chopping scheme.

3.4.1 Circuit implementation

Fig. 3.11 shows the block diagram of ADC II [2]. It employs the same topology as ADC I. However, ADC II samples at 5MHz (33x faster than ADC I) to increase its BW. The 2.5pF sampling capacitors result in a

95dB SNR (thermal noise limited) over a 10kHz BW. Two pairs of capacitors $C_{S1,2}$ and $C_{DAC1,2}$ are used for input sampling and DAC feedback respectively. This arrangement allows the ADC's input CM voltage to be different from that of the reference, as required for high-side current sensing. HV fringe capacitors are also used in this design to implement $C_{S1,2}$ and $C_{DAC1,2}$. Two diodes $D_{A,B}$ are placed after $C_{S1,2}$ to protect the rest of the ADC from large input CM transients.

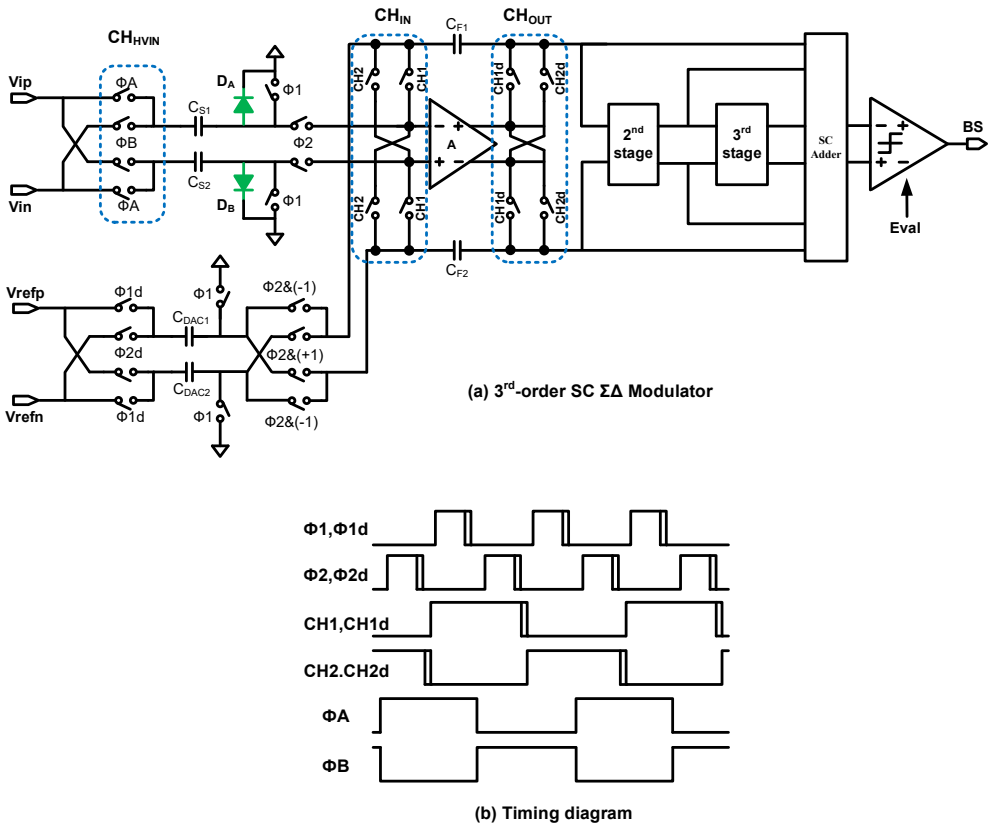

Figure 3.11. Block diagram of the ADC II.

All integrators are built around folded-cascode OTAs. The 1st integrator achieves 82dB DC gain and 30 MHz unity-gain bandwidth while drawing 230μA. The 2nd and 3rd integrators are scaled down by 8x to improve power efficiency. The comparator consists of a pre-amplifier and a dynamic latch. The outputs of three integrators are summed by a passive SC adder.

Unlike ADC I, the 1st integrator employs a chopping scheme to mitigate its 1/*f* noise and offset [7]. A pair of choppers (CH_{IN} and CH_{OUT}), controlled by chopping clocks CH1,2 and CH1d,2d, periodically swaps the position of the integration capacitors $C_{F1,2}$. As shown in Figure 3.11, the correct polarity of the input sampling branch is maintained by the clocks ΦA and ΦB that control the HV input chopper. The chopping frequency is thus at half the modulator's sampling frequency. To minimize intermodulation between the chopping clock and the modulator's quantization noise, the chopping transitions occur in the non-overlapping phase between Φ1 and Φ2. The delayed clock CH1d,2d ensures that CH_{IN} turns off slightly before CH_{OUT}. This ensures that signal-dependent charge from CH_{OUT} is not injected into the virtual ground. The clock network is extensively shielded and balanced to avoid noise coupling.

The advantage of this chopping scheme is that it swaps the position of the sampling capacitors, thus mitigating their mismatch and improving the ADC's high-frequency CMRR. The detailed operation of the 1st integrator is shown in Figure 3.12. In one integration cycle (CH1 is high), the input signal V_{ip} is sampled on C_{S1} (V_{in} is sampled on C_{S2}) during Φ1. During Φ2, the HV chopper CH_{HVIN} reverses the input and thus a positive charge packet $C_{S1}\cdot(V_{ip}-V_{in})$ is transferred from C_{S1} to the C_{F1} (a charge packet $C_{S2}\cdot(V_{in}-V_{ip})$ is transferred from C_{S2} to the C_{F2}). After 1st integration is done, the position of C_{F1} and C_{F2} is interchanged with the help of CH_{IN} and CH_{OUT}. In the next integration cycle (CH1 is low), the sampling network keeps cross-connected and V_{ip} is sampled on the C_{S2} (V_{in} is sampled on the C_{S1}). During Φ2, a positive charge packet $C_{S2}\cdot(V_{ip}-V_{in})$ is transferred to C_{F1} (a charge packet $C_{S1}\cdot(V_{in}-V_{ip})$ is transferred from C_{S2} to the C_{F2}). Assuming $C_{S1}= C_S+\Delta/2$ and $C_{S1}= C_S-\Delta/2$, the total

positive charge transferred to C_{F1} after two integration cycles will be $2 \cdot C_S \cdot (V_{ip}-V_{in})$. Consequently, the sampling capacitor mismatch is averaged out by chopping.

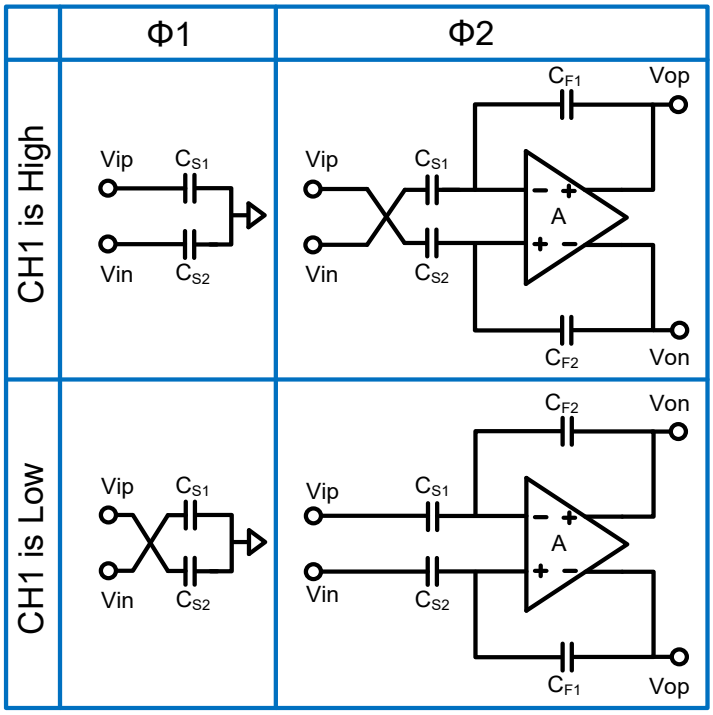

Figure 3.12. The detailed operation of the 1st integrator.

3.4.2 Experimental results

ADC II is fabricated in a different 0.18μm HV BCD CMOS process and occupies 0.53mm^2 (Figure 3.13). The chip draws 372 μA from a 1.8V supply: 290μA by the three integrators and the comparator, and 82μA by the clock generator.

Figure 3.14 shows the output spectrum with a 500mVp-p differential input signal (the ADC's reference voltage is 600mV) that is superimposed on a 10V CM voltage. When chopping is enabled, the 1/*f* noise and 2nd-order distortion are efficiently suppressed. Figure 3.15 (top)

shows the measured SNR/SNDR versus input amplitude with chopping on. The ADC achieves 93.7dB peak SNR and 89dB SNDR over 10kHz bandwidth at a sampling frequency Fs = 5MHz. For small DC inputs, and chopping on, small idle tones were observed due to residual cross-coupling between high-frequency quantization noise and chopping clocks at Fs/2. As shown in Figure 3.15 (bottom), the SNDR varies by only 0.3dB over the entire ICMR, demonstrating the excellent linearity of the HV chopper. The ADC's ICMR is limited to 0-29V by the ESD diodes at input terminals.

Measurements on 12 samples (Figure 3.16) show that chopping reduces the ADC's maximum offset from 2mV to 110μV. This relatively large residual offset is due to the relatively high chopping frequency (2.5MHz). The minimum CMRR at DC is 131dB with or without chopping. As shown in Figure 3.17, however, chopping improves the CMRR at high frequencies. At 10kHz, the CMRR improves from 97dB to 115dB. The ADC operates from a 1.5V to 2V supply, and its PSRR at DC and 50Hz are 95dB and 90dB respectively. In Table 3.2, the ADC II's performance is summarized. Compared to ADC I, ADC II achieves 100x wider BW and 60dB more AC CMRR while maintaining the beyond-the-rails capability. It's worth noting that current sensing for applications like motor control requires even higher BW [11-13]. Several magnetic-based current sensing analog front-ends [11-13] with several MHz BW have been developed and ADCs with similar BW are needed.

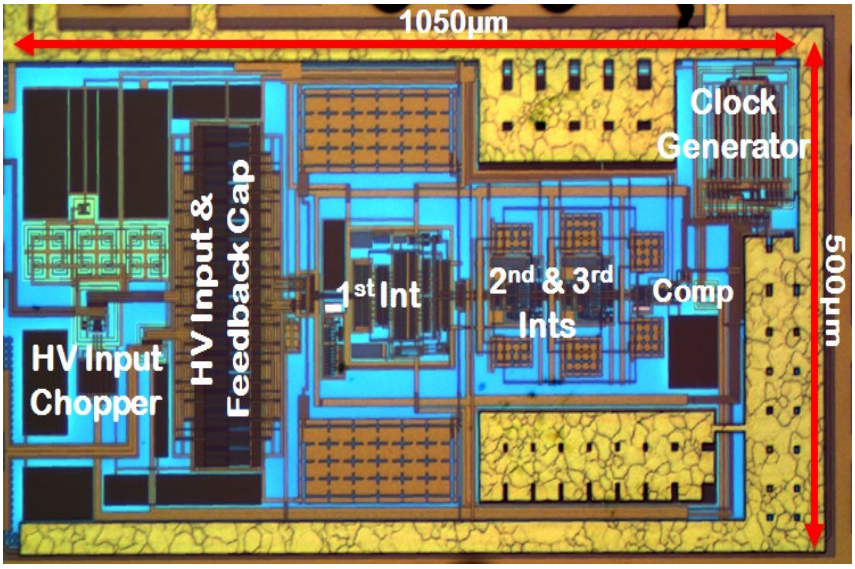

Figure 3.13. Chip micrograph.

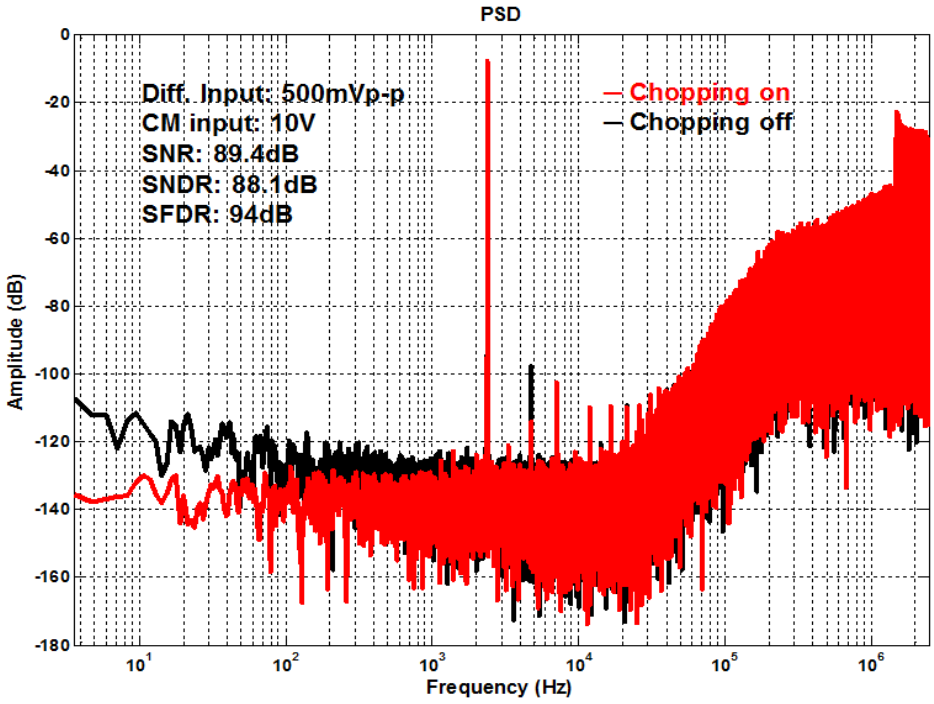

Figure 3.14. Measured output spectrum of the ΔΣ modulator under 10V input CM voltage.

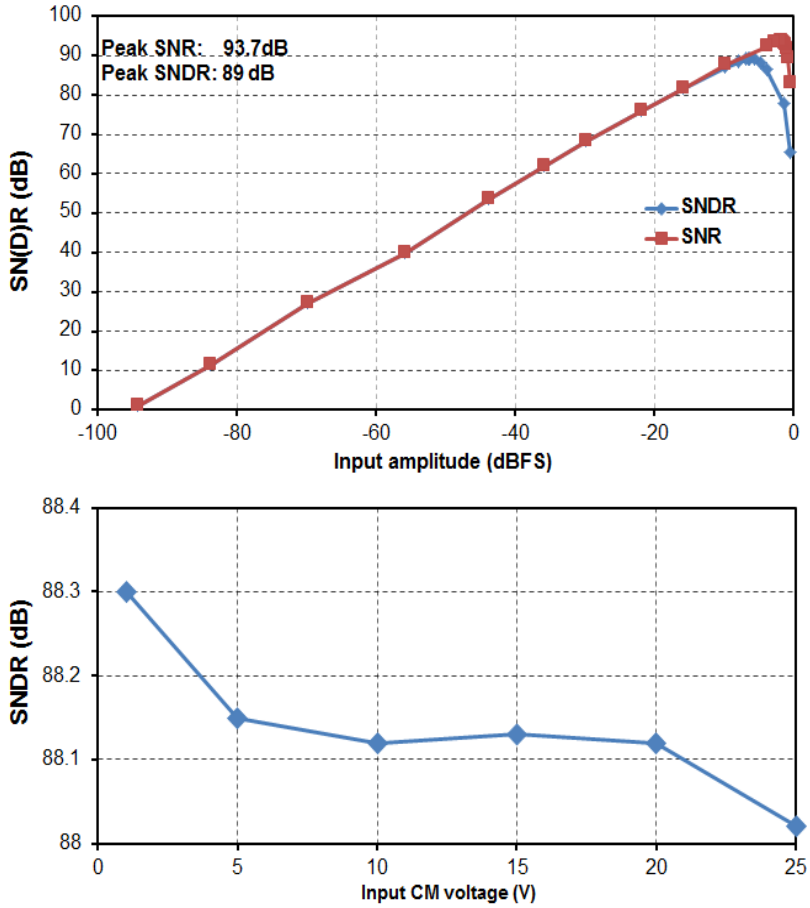

Figure 3.15. SNR & SNDR versus input amplitude (top) and SNDR over input CM range (bottom).

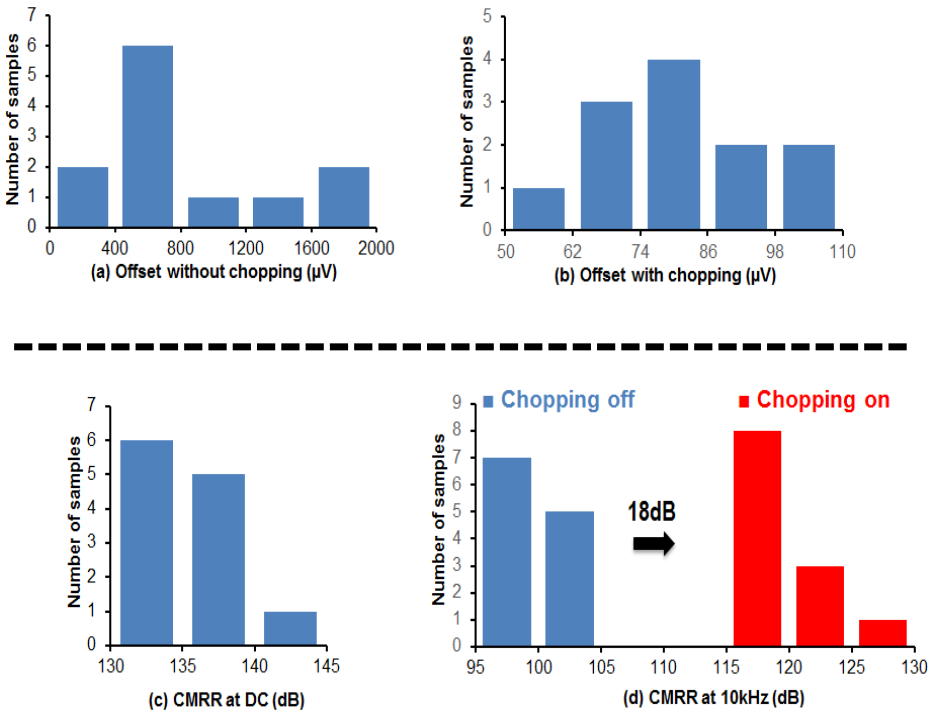

Figure 3.16. Histograms (12 samples) of the measured offset and the CMRR at DC & 10kHz.

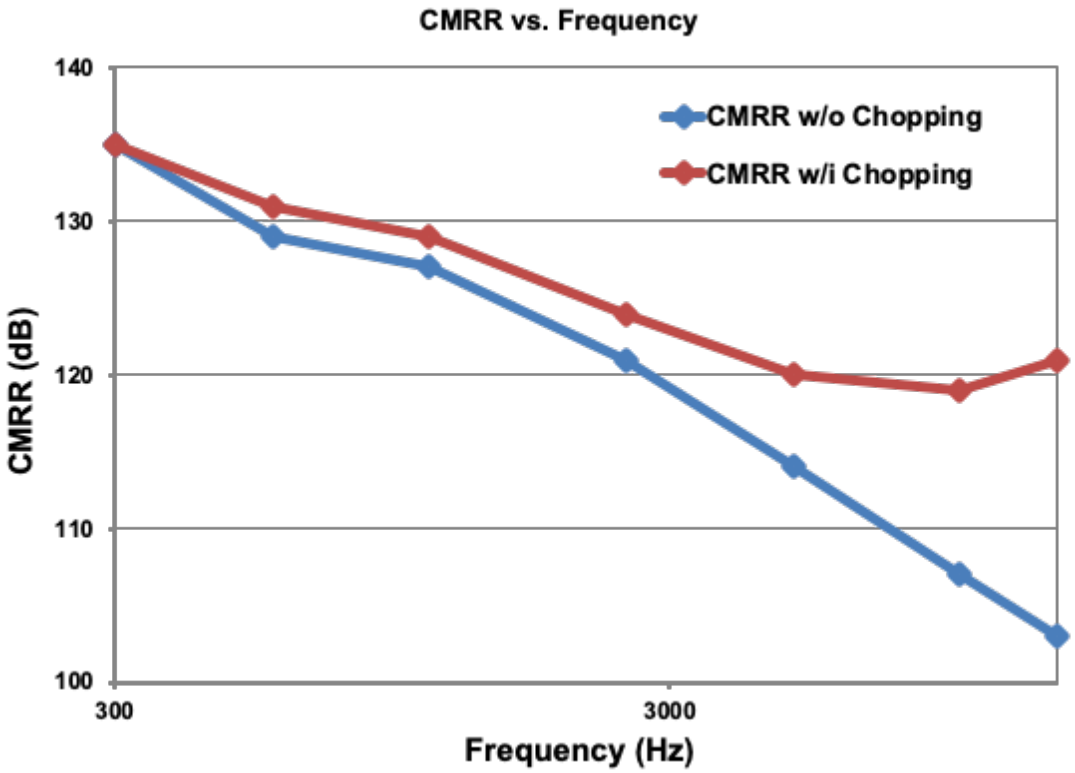

Figure 3.17. Measured CMRR versus input frequency ($20V_{p-p}$ sinewave is applied for CMRR measurement).

Table. 3.2 Performance summary.

	ADC I [1]	ADC II [2]
Supply voltage	5V	1.5-2V
Input CM range	±30V	29V
Input DM range	$4.4V_{p-p}$	$1V_{p-p}$
SNR	110.1dB	93.7dB
SNDR	100.6dB	89dB
SFDR	100.8dB	94dB
BW	100Hz	10kHz
Offset	8μV	110μV
CMRR (@DC)	140dB	131dB
CMRR (@10kHz)	<65dB	115dB
Chip area	$0.8mm^2$	$0.53\ mm^2$
Power	505μW	670μW

Note: SNR, SNDR and SFDR of the ADC II are measured with a 2.7kHz input signal.

3.5 Conclusion

Two beyond-the-rails ADCs have been presented in this chapter. The beyond-the-rails capability is enabled by a capacitively-coupled HV chopper. In addition, several dynamic offset cancellation techniques including chopping and CDS are utilized to reduce the offset and improve the CMRR.

Their performances are compared to other HV interfaces in Table 3.3. Both of them exhibit higher (>10dB) resolution and better power efficiency than another similar HV ADC [8] in a much smaller (50x) input DM range. Their power consumption is similar to a standalone IA [10], and much less than [9] which includes a separate IA and ADC. Most importantly, both ADCs achieve a wide ICMR (±30V and 29V) while operating from a low supply voltage (5V and 1.8V).

In summary, with the beyond-the-rails capability and precision DC performance, two proposed ADCs can be used as HV interface circuits for high-side current sensing without the need for a dedicated HV IA, thus reducing the overall power consumption and silicon area of the interface circuits. Their specific applications in current sensors will be discussed in the next chapter.

Table 3.3 Performance summary and comparison.

	ADC I [1]	ADC II [2]	[8]	MAX9611 [9]	INA210 [10]
Architecture	ADC	ADC	ADC	IA+ADC	IA
Supply voltage	5V	1.5-2V	3.3V	2.7V-5.5V	2.7V-26V
Input CM range	±30V	29V	0-50V	60V	26V
Input DM range	$4.4V_{p-p}$	$1V_{p-p}$	$50V_{p-p}$	$440mV_{p-p}$	$130mV_{p-p}$
SNR	110.1dB	93.7dB	81dB	73.98dB	--
BW	100Hz	10kHz	125kHz	500Hz	14kHz
Offset	8μV	110μV	--	500μV	35μV
CMRR (@DC)	140dB	131dB	--	120dB	131dB
Power	505μW	670μW	4.29mW	4.32mW	500μW**
FOM*	163dB	165.5dB	155.6dB	124.6dB	--

* $FOM = SNR + 10\log(\frac{BW}{Power})$

**with a 5V supply

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4. Design of Integrated High-Side Current Sensors and Temperature Compensation Schemes

In this chapter, two integrated high-side current sensors [1-2] are presented. The first design employs an analog temperature compensation scheme (TCS) in order to provide first-order compensation for the current sensing error caused by the metal shunt's large temperature coefficient of resistance (TCR), while maintaining low power consumption. This results in a residual gain error of 0.9% over the industrial temperature range. For improved inaccuracy (0.35%), the second design employs a hybrid analog/digital TCS to correct the residual errors of the analog TCS.

4.1 Current Sensor I Based on An Analog Temperature Compensation Scheme

4.1.1 System-level Architecture and Shunt Implementation

Figure 4.1 shows the system-level architecture of the current sensor I [1]. It consists of an on-chip metal shunt resistor, a beyond-the-rails ADC and a proportional-to-absolute-temperature (PTAT) reference voltage generator (RVG). The RVG generates a PTAT voltage V_{PTAT} that substantially compensates for the TCR of R_S, which, serendipitously, is itself almost exactly PTAT.

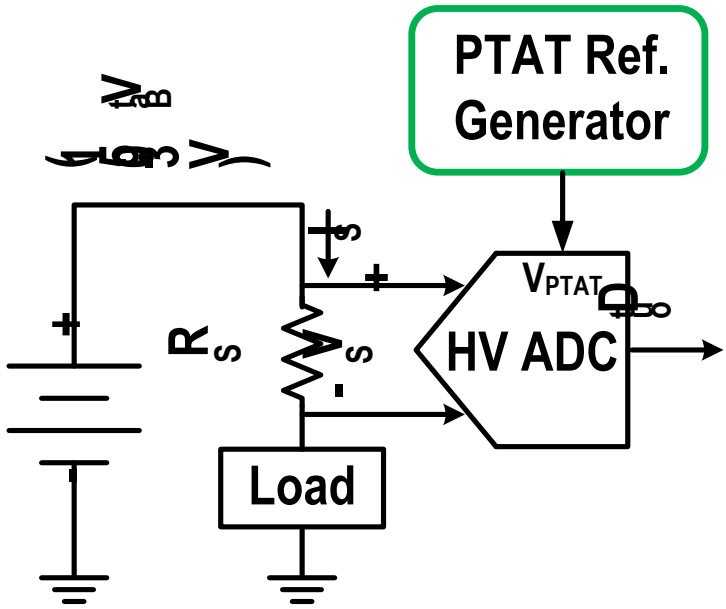


Figure 4.1. System-level architecture of the proposed current sensor I.

A. Shunt Implementation

Figure 4.2 shows the cross-section of the shunt R_S. It consists of four metal layers M2-M5 connected in parallel, and is similar to the ones described in [3-4]. The oxide separating the metal layers from the substrate provides galvanic isolation. To facilitate accurate temperature compensation, NPN transistors are located directly under the shunt to ensure good thermal coupling. Contacts to these transistors are made via the first metal layer (M1). The thermal coupling between the shunt and the NPNs is further enhanced by the use of thermal vias that connect the shunt to a dummy M1 layer that completely surrounds the NPNs.

As reported in [4], a metal shunt exhibited about 0.1% drift during a long-term (24 days) measurement at high current levels (±5A) and high ambient temperature (85 °C). This is caused by electromigration, and is a strong function of the current density through the shunt [5-6]. To reduce drift while maintaining the same resistance (10mΩ), the metal

shunt in this design (880μm×450μm) is 20% wider than the one in [4]. In addition, the maximum sensing current is limited by design to 4 A, which represents a further 20% reduction in current density compared to [4]. To minimize the parasitic resistance between the shunt and the outside world, and hence the on-chip power dissipation, the metal shunt is directly connected to the test PCB via 18 short (<1mm) bond wires (each bonding wire has a parasitic resistance of roughly 300mΩ).

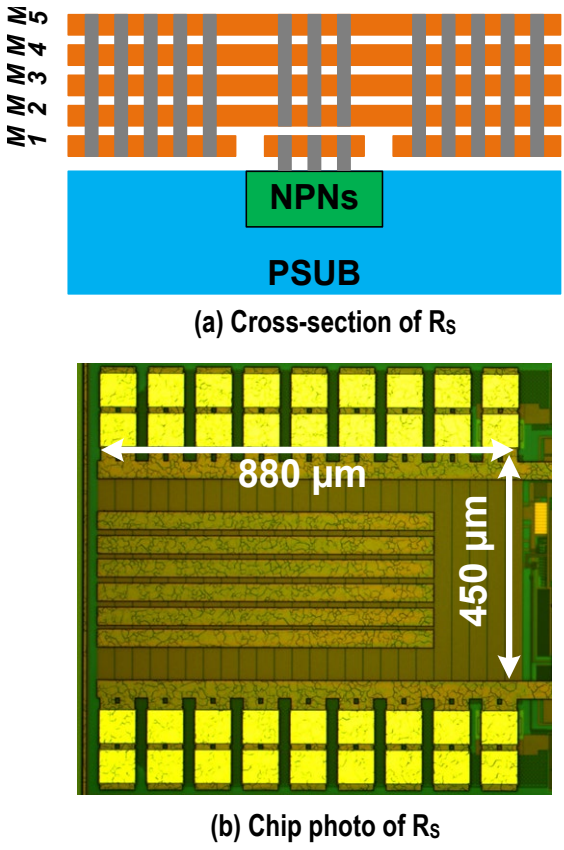
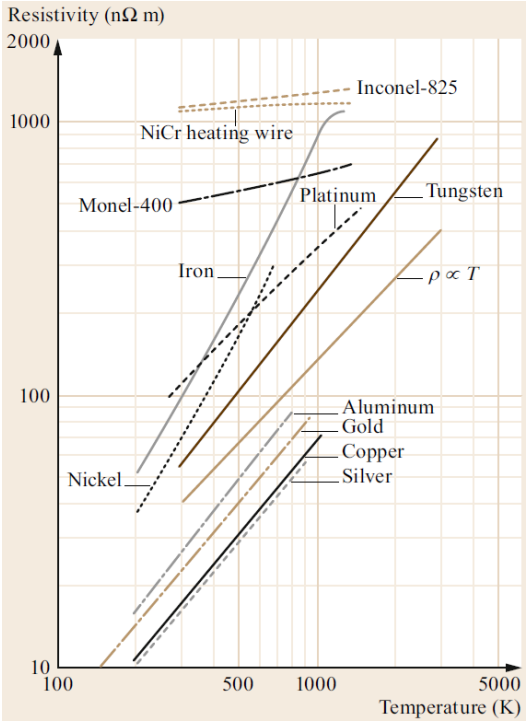


Figure 4.2. Cross section of the metal shunt R_S (top) and its chip photo (bottom).

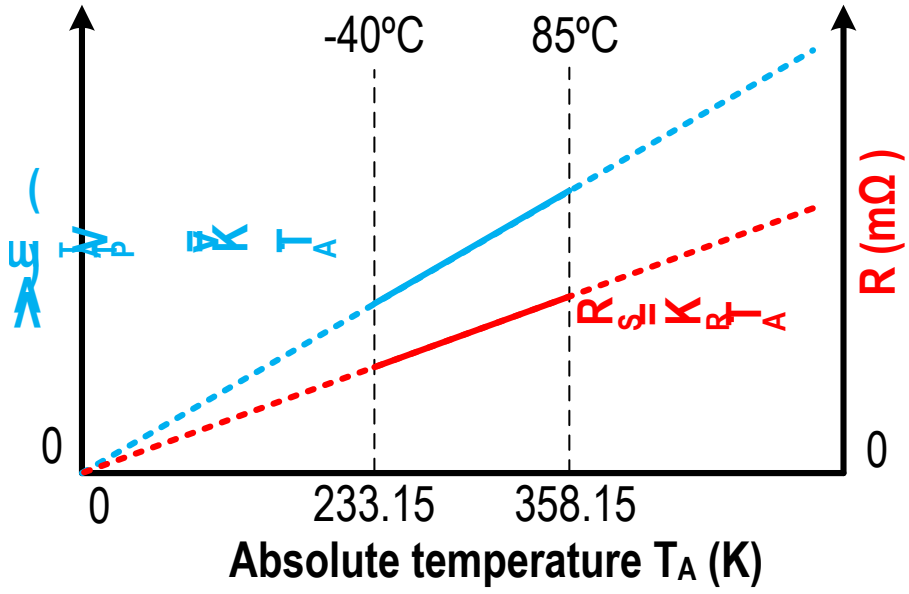
B. TCR of the Metal Shunt

As shown in Figure 4.3, the resistivities of most nonmagnetic pure metals increases with temperature [7]. The TCR's of the metals used in most CMOS technologies, i.e. aluminum and copper, are nearly PTAT over the industrial temperature range. In practice, however, the TCR of the metal layers used in CMOS process will be affected by geometrical

variation, the presence of impurities and other process-related factors, and so will not be perfectly PTAT [8].



(a)



(b)

Figure 4.3. (a) the resistivities of various metals: taken from [7], (b) behavior of a PTAT reference V_{PTAT} and the resistance of a metal shunt R_S over temperature.

C. Analog Temperature Compensation Scheme

As shown in Figure 4.3, instead of a bandgap voltage, a PTAT voltage V_{PTAT} ($=k_V \cdot T_A$) is employed as the ADC's reference. Since the metal shunt's temperature dependence is nearly PTAT ($R_S \approx k_R \cdot T_A$, T_A is absolute temperature) over the industrial temperature range, the shunt's 1st-order temperature dependency is corrected at the ADC's output D_{out} in a ratiometric manner:

$$D_{out} \approx \frac{I_S \cdot R_S}{V_{PTAT}} \approx \frac{I_S \cdot k_R \cdot T_A}{k_V \cdot T_A} \approx \frac{I_S \cdot k_R}{k_V} \qquad (4.1)$$

To verify the effectiveness of the analog TCS, D_{out} is simulated over the industrial temperature range with a fixed (1A) input current. As shown in Figure 4.4, D_{out} then varies by nearly ±20% when a bandgap voltage is used as the reference. This drops to ±0.5% when a PTAT reference is used. The residual error is mainly due to the non-linear components of the shunt's TCR.

To evaluate the effect of the thermal gradient between the shunt and the NPN transistors used to generate the PTAT reference, D_{out} is also simulated for the case when there is a 4 °C difference between them. As shown in Figure 4.5, the variation of D_{out} over temperature still remains within ±0.5%. This shows that the proposed TCS makes the sensor relatively insensitive to on-chip thermal gradients.

Compared to the digital TCS [4-5], the proposed analog TCS eliminates the need for an accurate temperature sensor, which in turn reduces the total calibration time since the characterization of the temperature sensor is not needed. According to the equation 4.1, the gain of the current sensor is mostly determined by the ratio between the shunt

resistance and the reference voltage, and their spread can be corrected simultaneously by a one-point trim.

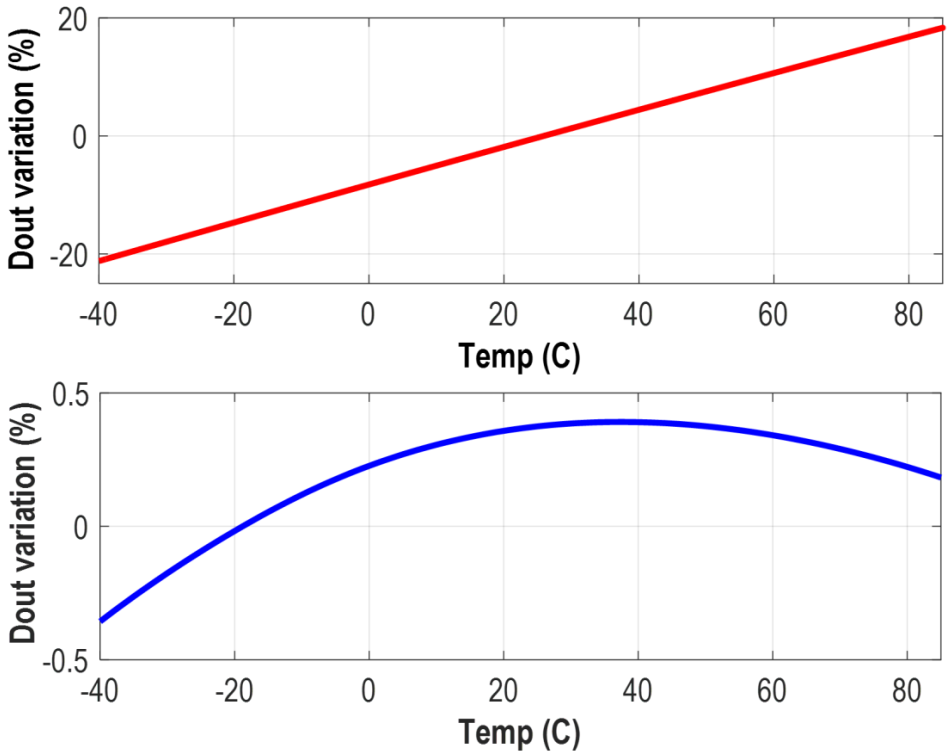


Figure 4.4. Simulated D_{out} variation over temperature when a bandgap reference (top) and a PTAT reference (bottom) are applied to the ADC.

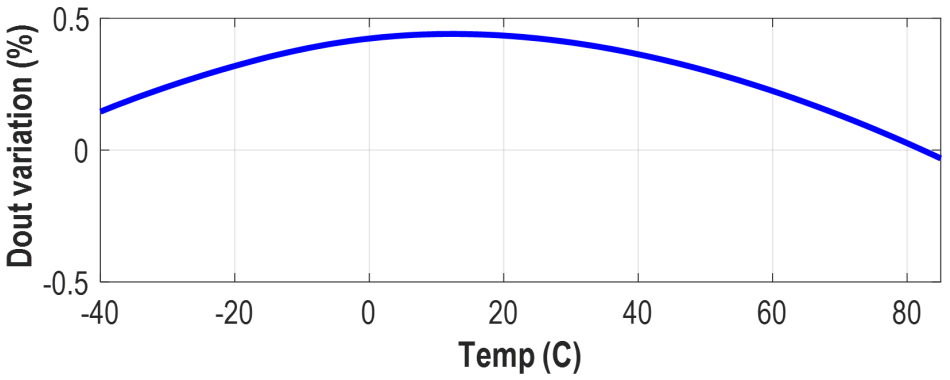


Figure 4.5. Simulated D_{out} variation over temperature with PTAT reference including 4 °C thermal difference.

4.1.2 Circuit implementation

A. ADC

As shown in Figure 4.6, the ADC architecture is similar to that used in ADC I (chapter 3). The order of the loop filter is reduced from three to two due to the relaxed quantization noise requirement. The ADC's full-scale input range is only ±40mV (±4A×10mΩ), which results in a very small voltage swing inside the loop filter. Hence, its integrators can be realized with energy-efficient current-reuse amplifiers [9], as shown in Figure 4.7. The amplifiers in both integrators have a minimum DC gain of 80 dB and 800 kHz unity-gain bandwidth while drawing 5μA in total.

The shunt voltage V_S (V_{ip}-V_{in}) is sampled onto input capacitors C_{S1} (2.5pF) by a HV input chopper CH_{HV}. In this way, the ADC's active blocks are isolated from input CM voltages, and so can be powered from a LV supply. In a similar manner, a reference voltage V_{PTAT} is sampled onto feedback capacitors C_{S2} (2.5pF) with the help of a LV chopper whose polarity is determined by the modulator's bitstream. To obtain wide ICMR and good matching, HV fringe capacitors with a breakdown voltage of 70V are employed to implement both C_{S1} and C_{S2}.

The implementation of low-frequency chopping (CHL) is also different from that used in ADC I. The required polarity inversion is achieved by placing an extra pair of choppers around the ADC in [3-4]: one ($CH_{SYS.IN}$) is at its analog input and the other ($CH_{SYS.OUT}$) at its bitstream output. Since the original ADC already has an input chopper (CH_{HV}), the function of two choppers $CH_{SYS.IN}$ and CH_{HV} can be emulated by swapping the clock signals Φ1, Φ2 applied to CH_{HV}, as shown in Figure 4.8. This chopping scheme does not cancel the residual offset due to the charge injection mismatch of CH_{HV}. However, with proper timing, this

mismatched charge will flow into the low-impedance shunt, and so causes negligible offset.

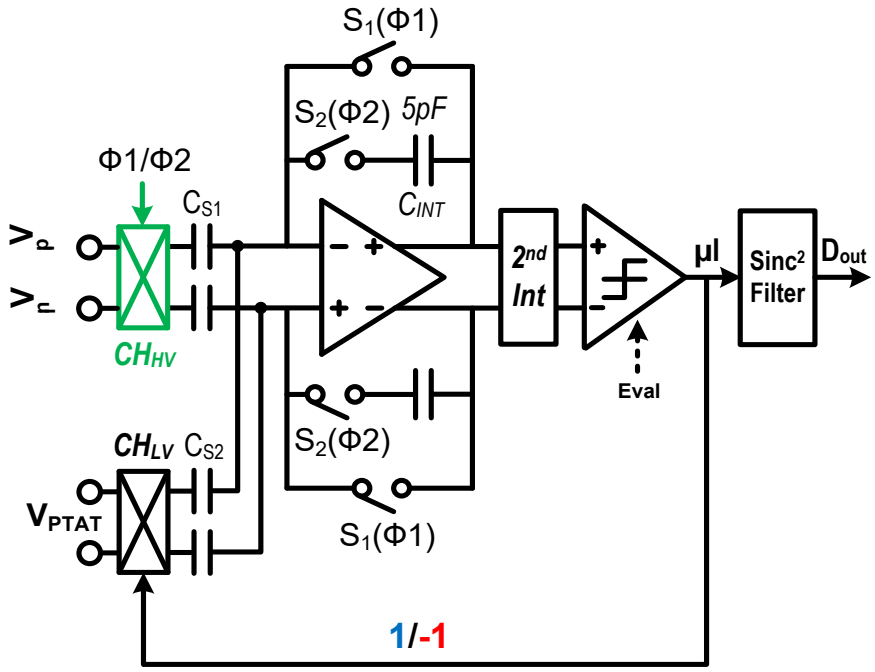


Figure 4.6. Schematic of the beyond-the-rails ADC.

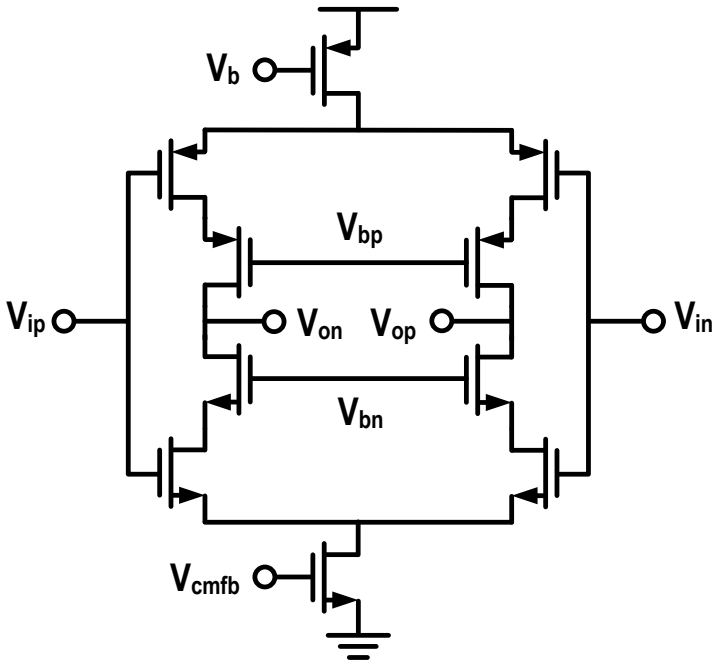


Figure 4.7. Schematic of the current reuse amplifier.

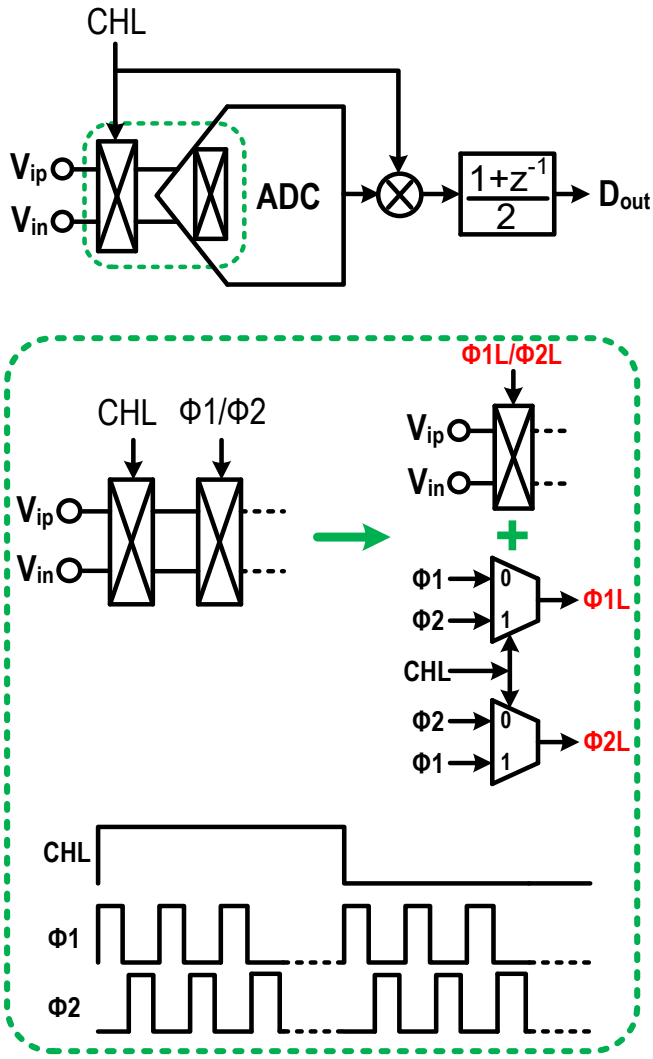


Figure 4.8. Low-frequency chopping implementation and its timing diagram.

B. PTAT generator

Figure 4.9 shows the schematic of the RVG. It consists of a bias circuit and a bipolar core. The bias circuit generates a PTAT current, which is then mirrored (1:4) to the bipolar core. Benefiting from the availability of vertical NPNs in the chosen process, the bias circuit is implemented without the extra low-offset amplifier required by PNP-based bias circuits [3-4]. Two NPN transistors in the bipolar core are biased at a current density ratio of 7, and so their base-emitter voltage difference $\Delta V_{BE} = (k/q)\cdot\ln(p)\cdot T_A$ is PTAT, and this is used as the ADC's reference V_{PTAT}.

Thanks to the analog TCS, a one-point trim will correct both spread in the shunt's resistance and the spread in the absolute value of ΔV_{BE} (due to the mismatch of NPNs). Hence, the NPNs do not require dynamic element matching, which represents a simplification over [3-4]. Furthermore, the output of the PTAT reference (~50mV at room temperature) is smaller than the bandgap reference (~ 100mV) used in [3-4], resulting in less swing in the loop filter, and thus relaxing its settling requirement.

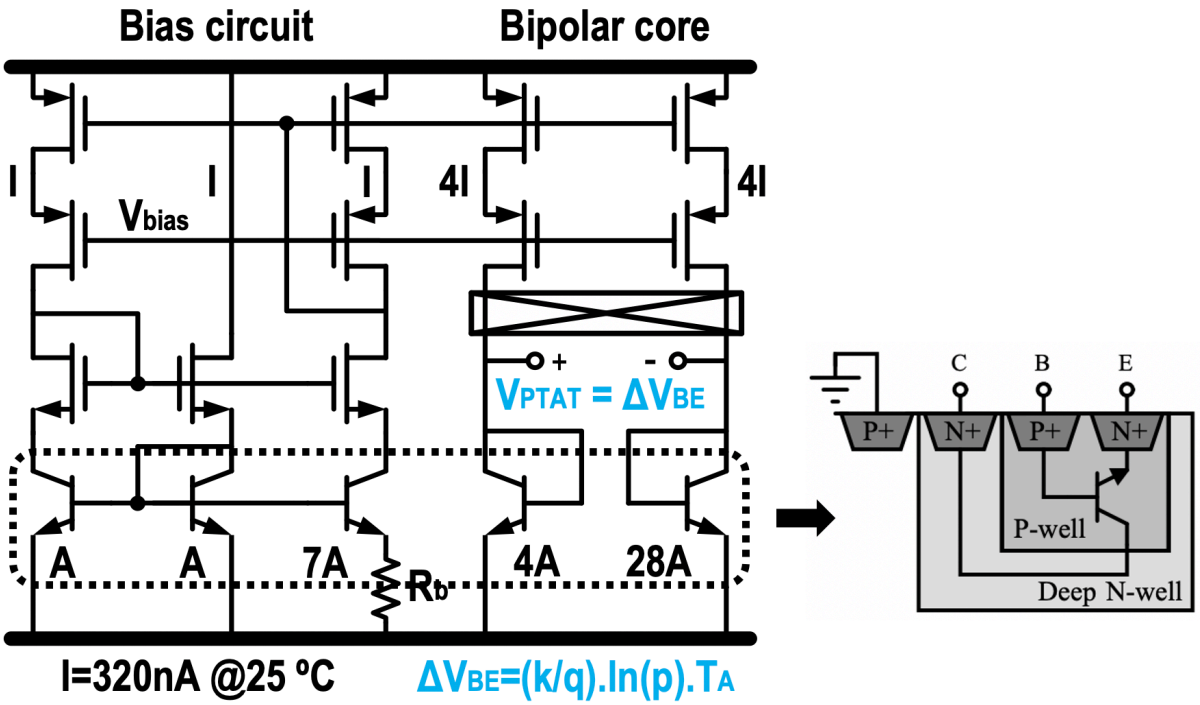


Figure 4.9. Schematic of the PTAT RVG and the cross section of the NPN transistor.

The two current sources in the bipolar core are chopped to suppress their 1/f noise. To avoid potential intermodulation between chopping ripple and the ADC's quantization noise, the chopping frequency is the same as the ADC's sampling frequency. Compared to the analog compensation scheme described in [10], which uses a bandgap voltage

followed by a reference buffer with a temperature-dependent gain, the proposed solution is much simpler and more power efficient.

4.1.3 Experimental results

The current sensor was implemented in a 0.18μm HV BCD CMOS technology and occupies 1.4mm^2 (Figure 4.10). It draws 10.9μA from a 1.5V supply at room temperature. The RVG, the ADC and the digital clock generator consume 4μA, 5.2μA and 1.7μA respectively. Figure 4.11 shows the 2^{20}-point FFT output spectrum of the free-running ΔΣ modulator under different input currents. It is thermal-noise limited in a 1-kHz BW and does not exhibit idle tones. At a sampling frequency of 250-kHz, the ADC achieves a output noise of 1.5μV_{rms} in a conversion time of 2ms (Figure 4.12), which translates into a current-sensing resolution of 150μA_{rms} based on Ohm's law $Isense_{rms}=Vnoise_{rms}/Rs$ where Rs=10mΩ.

Similar to the previous simulation shown in Figure 4.4, the sensor was also measured with a fixed 1A input. The ADC's output D_{out} then varies by 0.3% over the industrial temperature range (Figure 4.13), which agrees well with the results of simulation. To explore the effect of Joule heating in the shunt, ΔV_{BE} was measured at different input currents (Figure 4.14). It increases by 2.5mV when input current changes from 0A to 4A, which translates into a 15°C temperature rise. Figure 4.15 shows the transient measurement with a 4A current step input. It can be seen that the gain error of the D_{out} settles to 0.1% within 40ms (this latency is mainly caused by the limited slew rate of the Keithley 2400 SourceMeter used for the measurement). The slow thermal settling of die temperature (or equivalently ΔV_{BE}) is also shown.

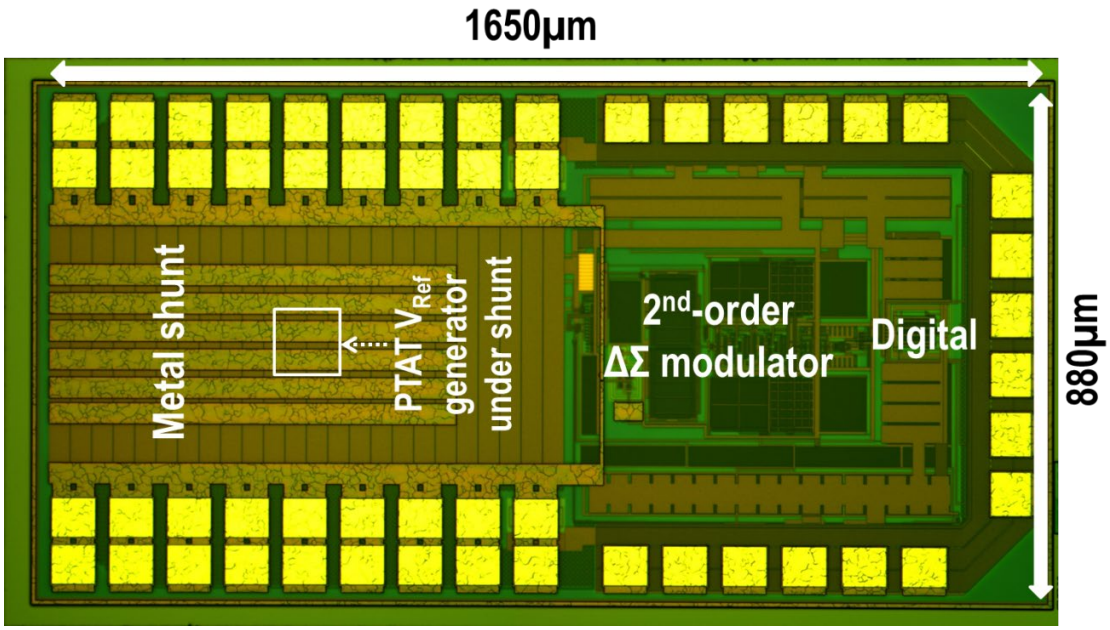


Figure 4.10. Chip photo of the current sensor I.

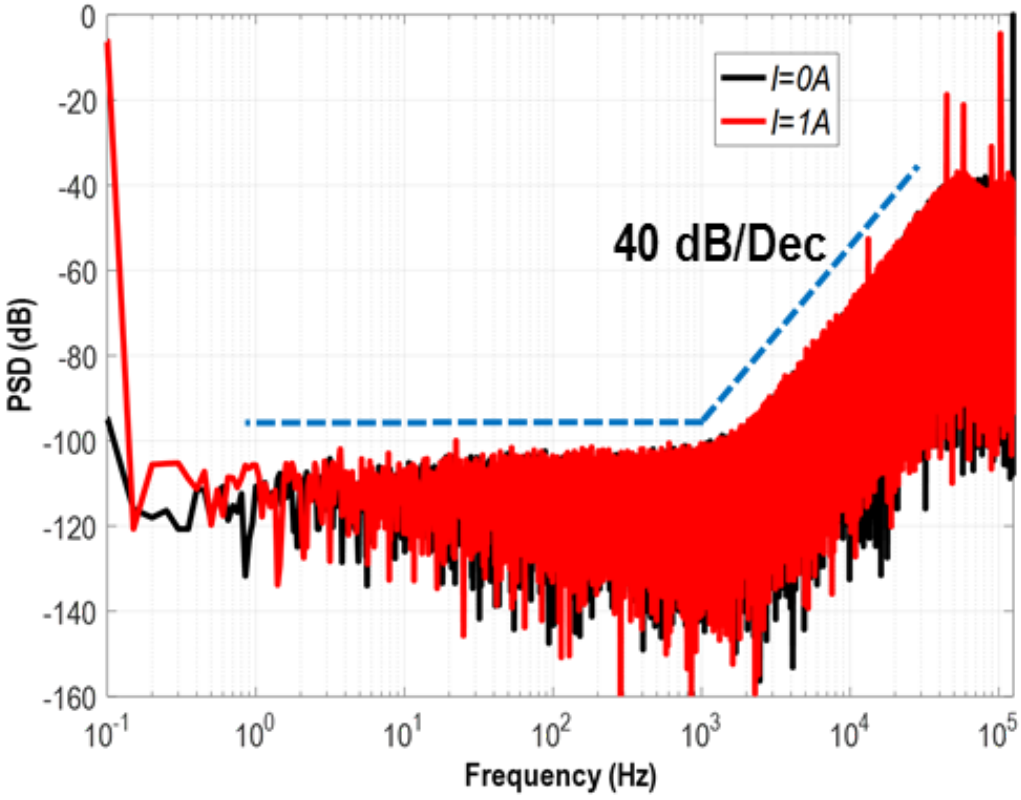


Figure 4.11. Measured output spectrum of the ΔΣ ADC (before decimation) with 0A&1A current input (2^{20}-point FFT).

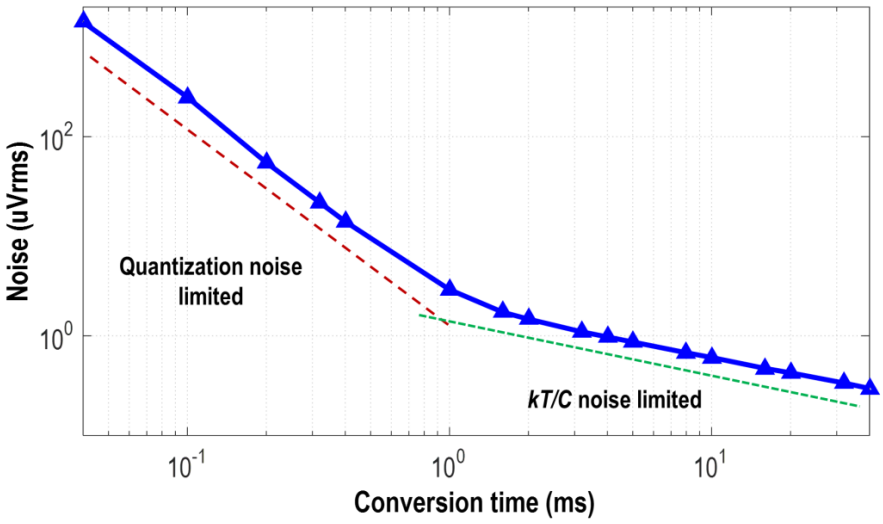


Figure 4.12. Measured output noise versus conversion time.

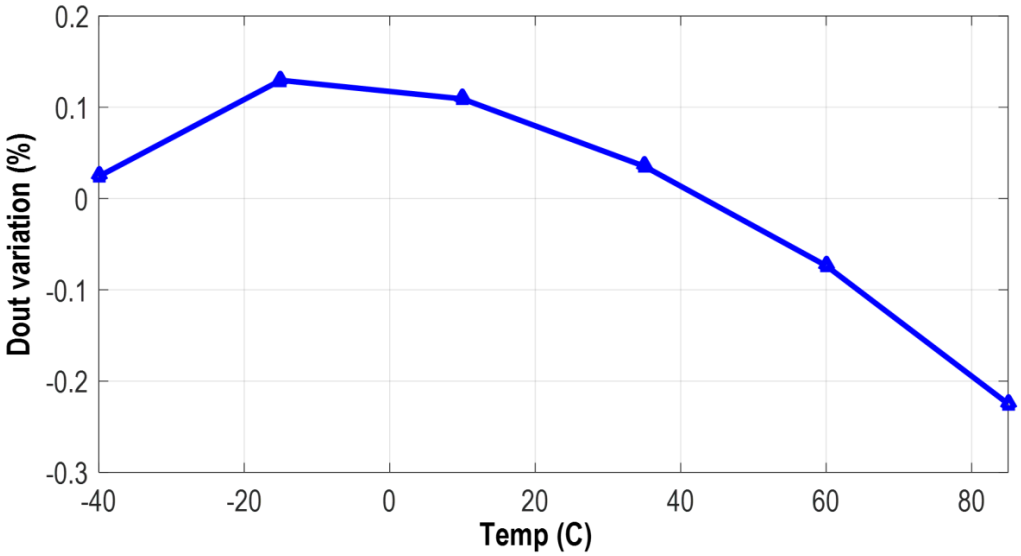


Figure 4.13. Measured D_{out} variation over temperature.

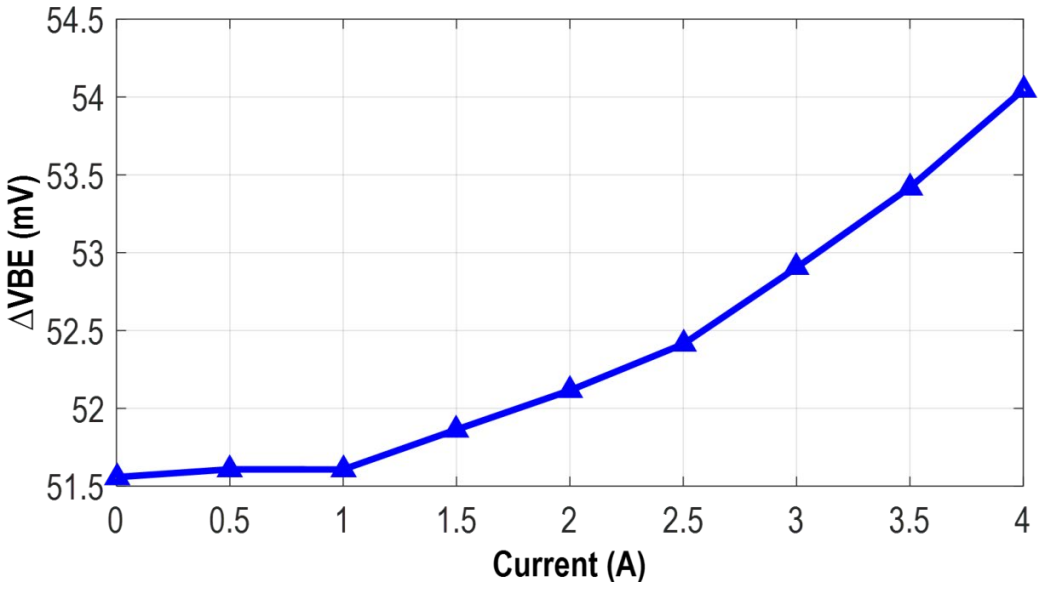


Figure 4.14. Measured ΔV_{BE} versus input current.

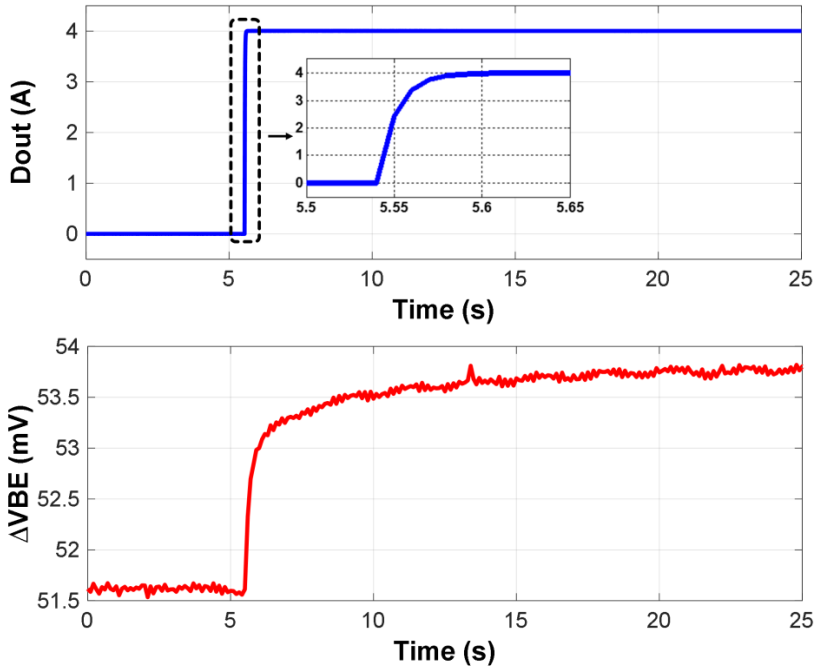


Figure 4.15. Transient measurement under a 4-A current step input.

Ten sensors were characterized over a ±4A range from -40°C to 85°C (Figure 4.16). After a one-point trim (at +3A and ~25°C), the sensor's gain error is only 0.05% at room temperature, increasing to 0.9% over the full temperature range. As discussed before, this large gain error over temperature is mainly caused by the higher-order coefficients of the

shunt's temperature dependence, which are not cancelled out by a linear PTAT reference. Over a 25V ICMR, the ADC's maximum offset is 6.4μV (640μA), dropping below 400nV (40μA) when CHL (a 250Hz square wave) is enabled (Figure 4.17). The offset varies by less than 700nV over the full ICMR, corresponding to a CMRR of 151dB, which improves to 158dB after CHL (Figure 4.18). Over a supply range from 1.5V to 2V, the ADC's offset varies by less than 1μV, which corresponds to a DC PSRR of 113dB. This improves to 125dB when CHL is enabled (Figure 4.19). The PSRR at high frequencies is measured when the ΔΣ ADC is in free-running mode (CHL is disabled) and a 100mV$_{p-p}$ sinusoid is added to the 1.5V supply. It remains above 95dB up to 1kHz (Figure 4.20).

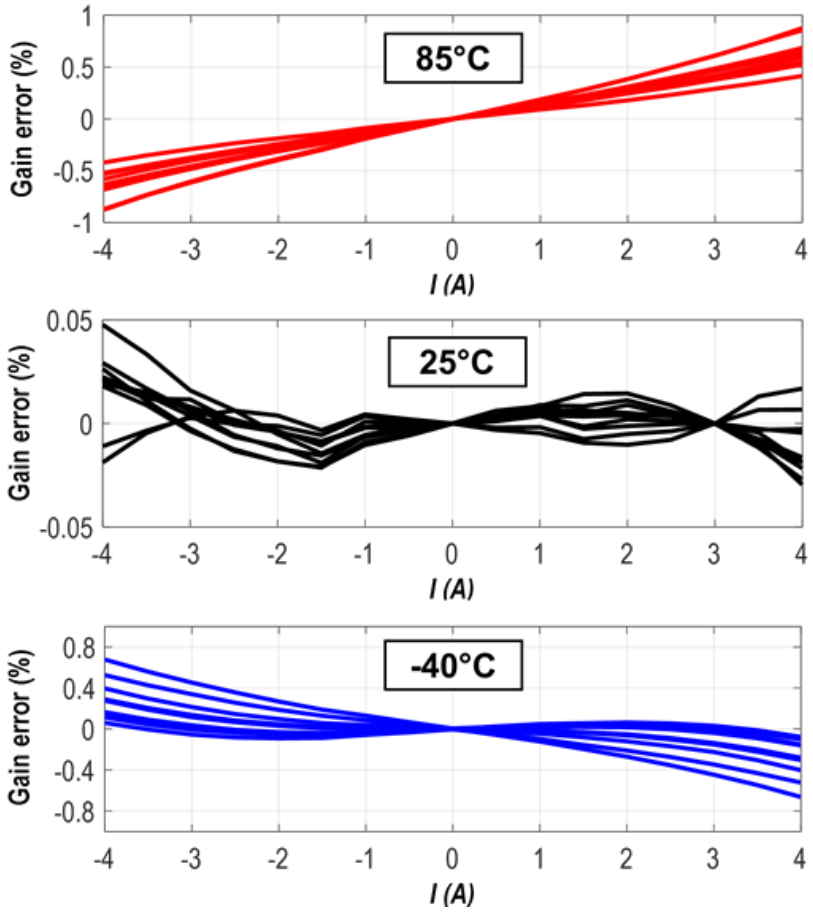


Figure 4.16. Measured current sensing gain error at different ambient temperature.

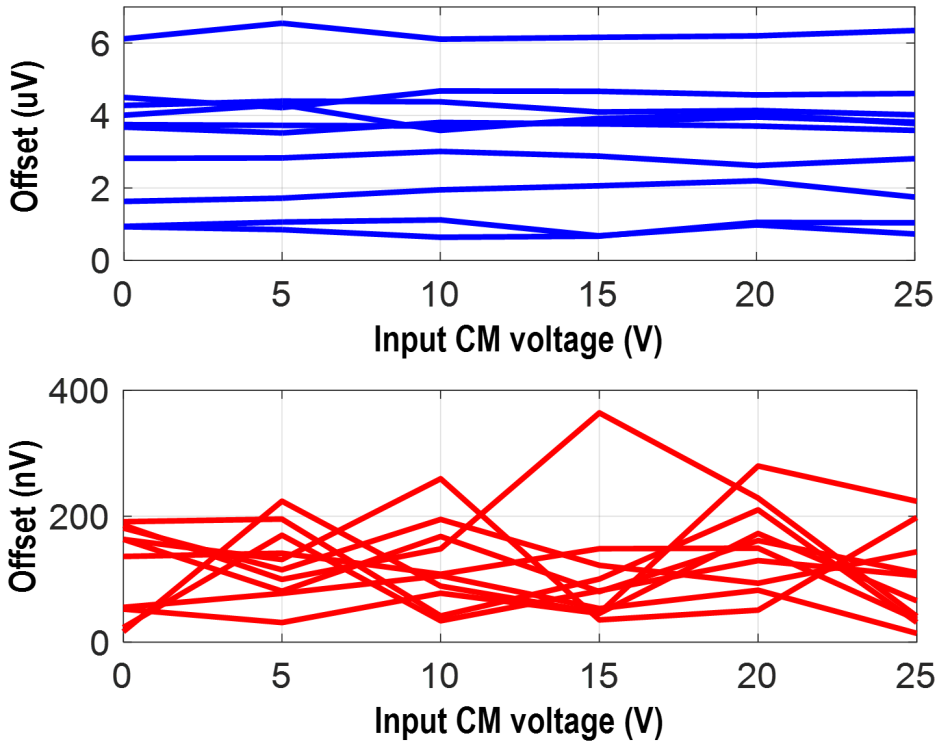


Figure 4.17. Measured offset over ICMR without CHL (top) and with CHL (bottom).

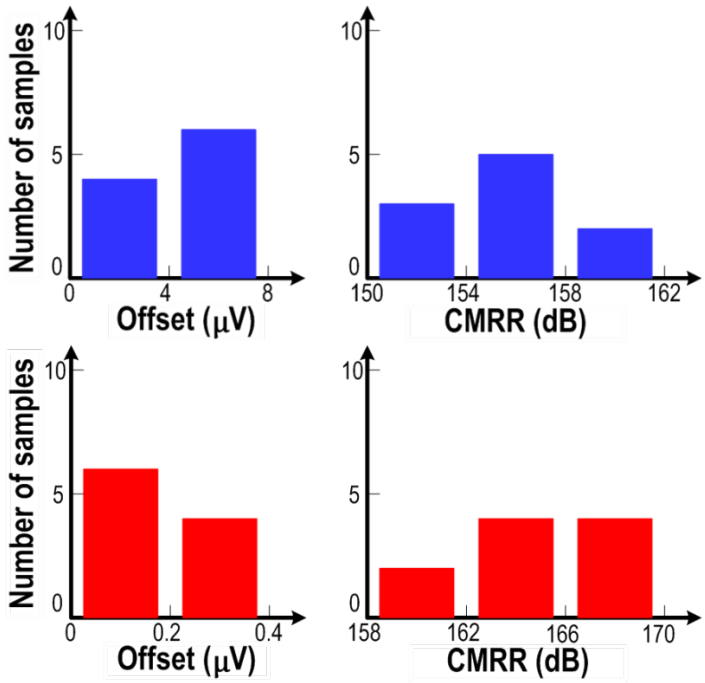


Figure 4.18. Measured histograms of offset and CMRR without CHL (top) and with CHL (bottom).

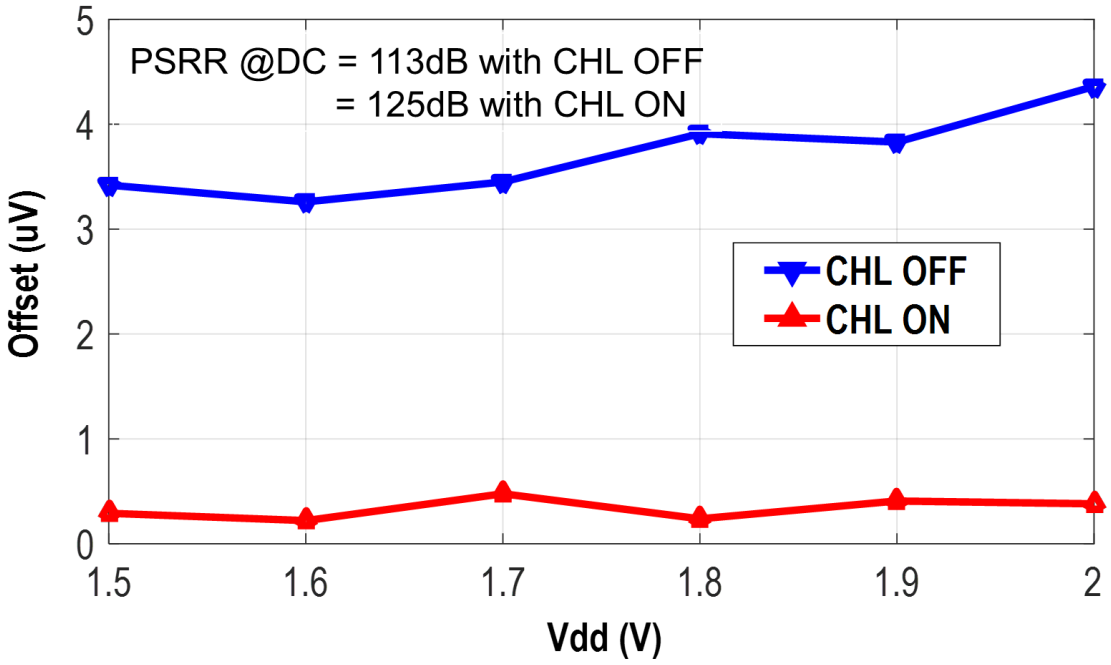


Figure 4.19. Measured PSRR at DC.

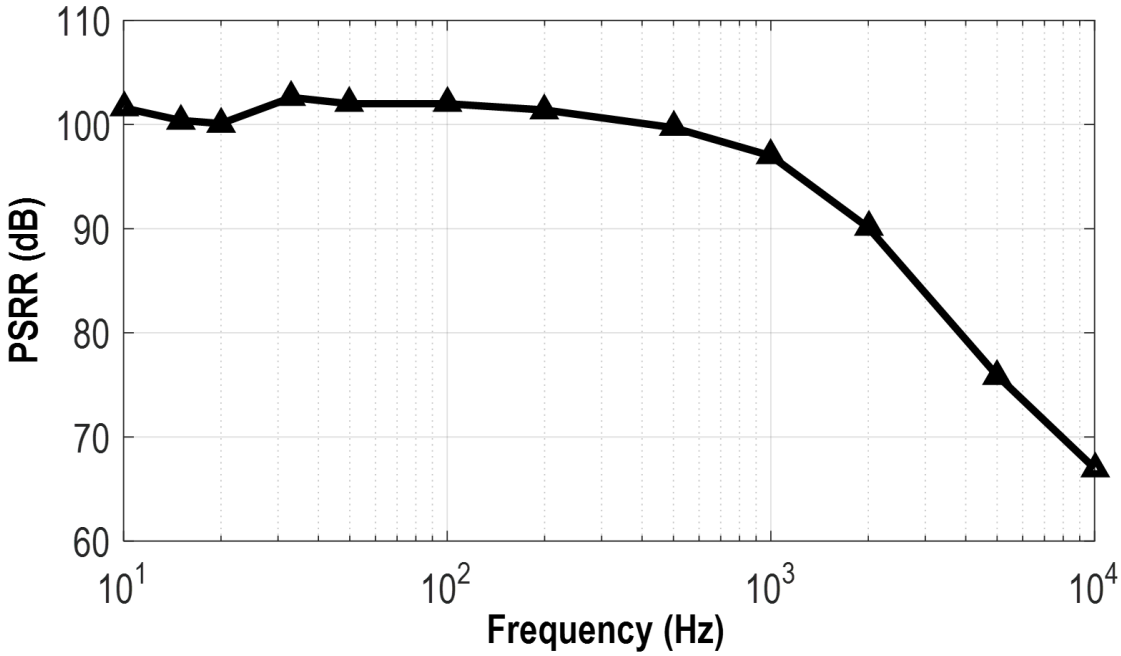


Figure 4.20. Measured PSRR over frequency.

The performance of the sensor is summarized in Table 4.1. Its energy efficiency, like that of a temperature sensor, can be expressed in terms of a resolution figure-of-merit (FOM) [11]. Compared to other fully integrated current sensors [4], [12-13], this design achieves 10x better energy efficiency, the lowest gain error at room temperature, and comparable gain error over the industrial temperature range.

Table 4.1 Performance summary.

	This work	JSSC 17 [4]	LT2947 [12]	INA260 [13]
I-range	**±4A**	±5A	±30A	±10A
Temperature range	**-40-85°C**	-55-85°C	-40-85°C	-40-125°C
Shunt	**10mΩ**	10mΩ	300μΩ	2mΩ***
Input CM range	**0-25V**	0-0.75V	0-15V	0-36V
Gain error (25°C)	**0.05%**	0.1%	0.75%	0.15%
Gain error (-40-85°C)	**0.9%**	0.3%	1%	0.5%
Offset	**40μA**	4μA	9mA	5mA
Resolution	**150μA**	200μA	3mA	1.25mA
Conversion time	**2ms**	10ms	100ms	8.2ms
Supply voltage	**1.5-2V**	1.3-1.7V	4.5-15V	2.7-5.5V
Supply current	**10.9μA**	13μA	9mA**	310μA
Polynomial Calibration	**No**	Yes	Yes	No
FOM*	**0.74fJ·A²**	**7.8fJ·A²**	--	--

* FOM = (Energy / Conversion) × Resolution²

** Includes the power of current-sense ADC, voltage-sense ADC, temp. sensor and digital circuitry

*** Uses a customized low-TC shunt

4.2 Current Sensor II Based on A Hybrid Temperature Compensation Scheme

4.2.1 System-Level Architecture and Shunt Implementation

Figure 4.21 shows the system architecture of the second design: current sensor II [2]. Compared to current sensor I, important differences are the use of a smaller shunt resistor R_S (~1mΩ) based on a copper PCB trace, and the implementation of an on-chip temperature sensor (TS).

A. Shunt implementation

For rapid prototyping, a PCB trace is used to emulate a lead-frame shunt [4]. Compared to the use of an on-chip metal shunt [1], this does not cost silicon area, and enables a larger (±12A) current sensing range, which is 3x wider than [4]. Good thermal coupling and galvanic isolation are achieved by directly bonding the chip to the trace with electrically isolating glue. The HV ADC digitizes the voltage drop across the shunt V_S via Kelvin contacts S1 & S2 (Figure 4.22) with respect to a voltage reference V_{PTAT} generated from the RVG. Meanwhile, the TS senses the shunt's temperature, and its output μT is then used to correct the digitized shunt voltage μI with the help of a single 2^{nd}-order polynomial.

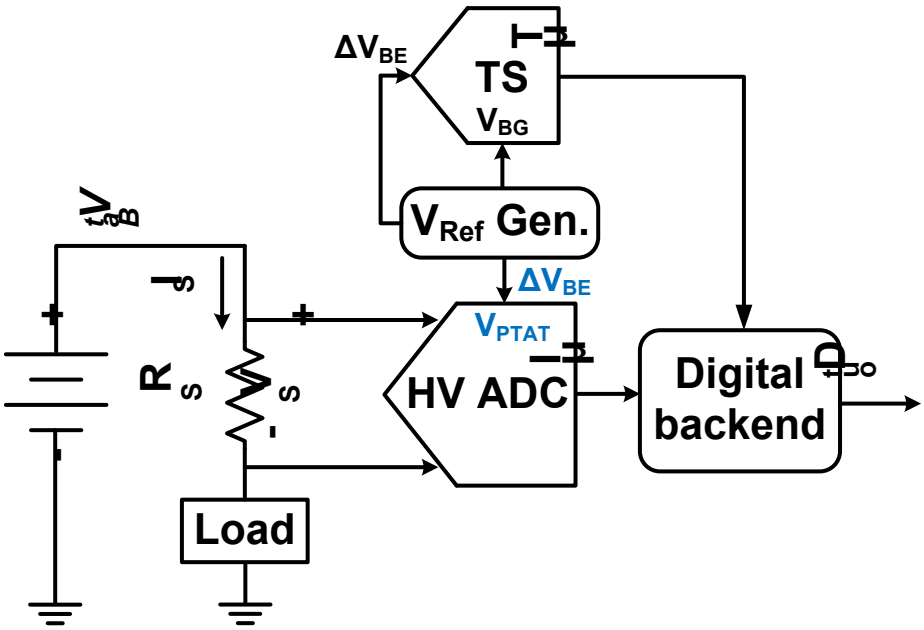


Figure 4.21. System architecture of the sensor.

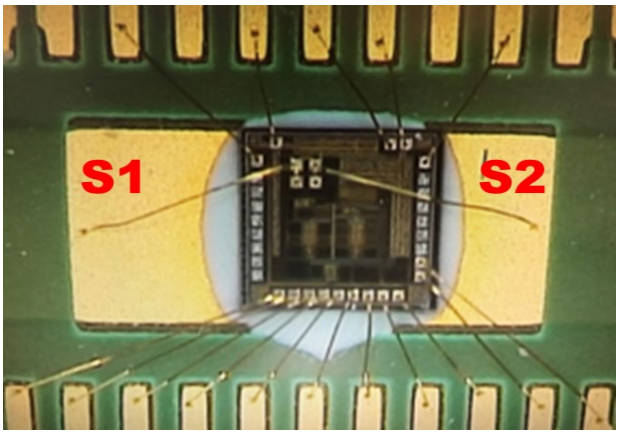


Figure 4.22. Bonding diagram of the chip.

B. Hybrid analog/digital temperature compensation scheme

In [3-4], the shunt voltage V_S is digitized by an ADC with respect to a nearly temperature-independent bandgap reference. An on-chip TS then senses the shunt's temperature such that its temperature dependency can be compensated in the digital domain. Since copper has a relatively large temperature coefficient of resistance (TCR ~ 0.38%/ºC), the TS has to achieve an inaccuracy of less than 0.5ºC in order not to become a dominant error source.

In this design, instead of a bandgap reference, a proportional-to-absolute-temperature (PTAT) voltage V_{PTAT} is employed as the ADC's reference [1]. Since the shunt resistance's temperature dependency is also roughly PTAT, it is effectively compensated by the TC of V_{PTAT}, thus realizing an analog TCS. However, since the shunt resistance's temperature dependency is not perfectly PTAT, there will still be some residual error. This can be modelled by a fixed 2nd-order polynomial and then digitally corrected with the help of the TS. Noting that the TC of this residual error is 8x less than that of copper, the inaccuracy of the TS can be relaxed for the same current sensing inaccuracy.

4.2.2 Circuit Implementation

A. ADC

The ADC used in this design is identical to the one used in current sensor I and so will not be described here.

B. RVG and TS

Figure 4.23 shows the schematic of the RVG and the TS. Two vertical NPN transistors are biased at a current density ratio of 7. The base-emitter voltage difference ΔV_{BE} of two NPN transistors is PTAT, and is used as the ADC's reference V_{PTAT}. Dynamic element matching of the NPNs and CHL for TS are eliminated in this design due to the relaxed requirement on the TS inaccuracy. The current sources are chopped to suppress their 1/*f* noise.

The TS digitizes the shunt's temperature by balancing ΔV_{BE} against $-V_{BE}/10$ [3]. When bsT is 0, C_{S3} (= 1pF) samples $+\Delta V_{BE}$ and when bsT is +1, C_{S4} (= 100fF) samples $-V_{BE}$. This results in an average value of bsT (μT) equal to $\Delta V_{BE} / (\Delta V_{BE}+V_{BE}/10)$ ($(\Delta V_{BE}+V_{BE}/10)$ generates a bandgap reference), which is a linear function of temperature.

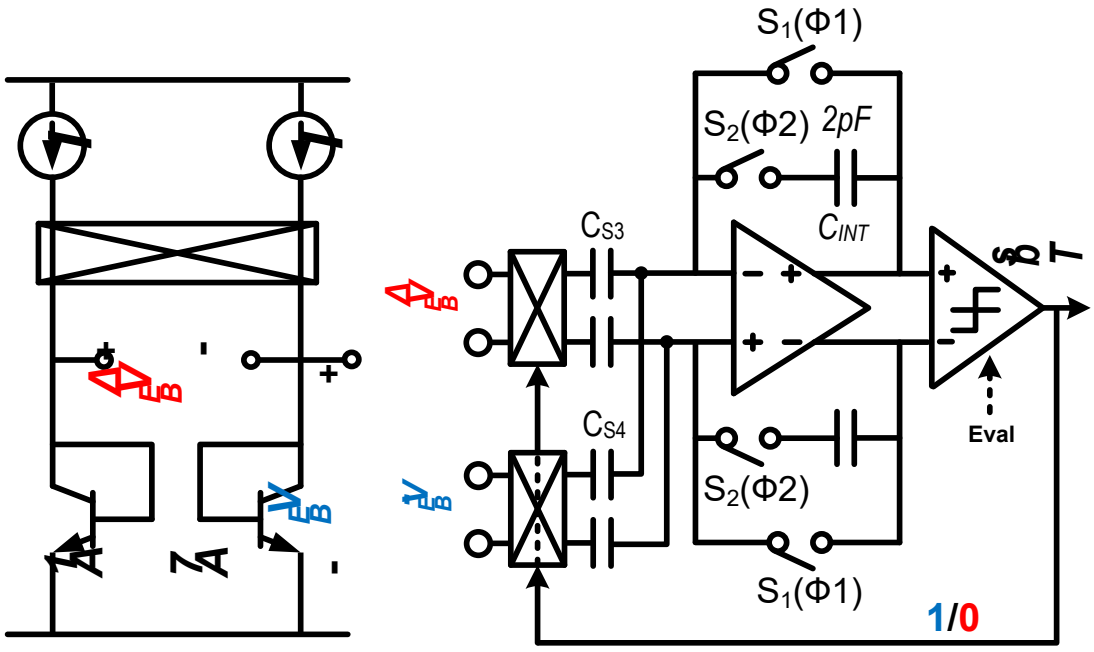


Figure 4.23. Schematic of the RVG (left) and the TS (right).

4.2.3 Experimental Results

The sensor was fabricated in a 0.18μm HV BCD CMOS technology with a core area of 1.4mm^2 (Figure 4.24). At room temperature, it draws 13.8μA from a 1.8V supply. At a 200-kHz sampling frequency and for a conversion time of 12.5ms, the ADC and TS achieve output noise of 1.1μV_{rms} and 10mK_{rms} respectively.

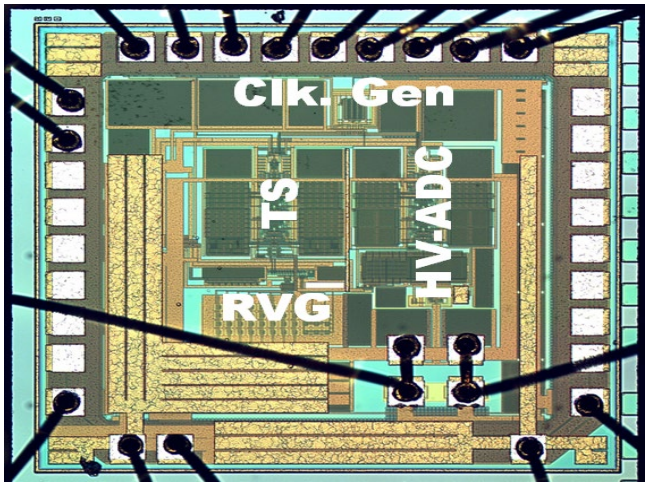


Figure 4.24. Chip photo.

Figure 4.25 shows the variation of the ADC's bit-stream average μI over temperature. For a constant input current (1A), μI varies by ±28% from -40°C to 85°C due to the large TCR of the copper shunt when the bandgap reference is used. This drops to ±3.5% when the PTAT reference V_{PTAT} is used. Without the TCS, the sensor only achieves a gain error of 30% (1 sample) from -40°C to 85°C (Figure 4.26). The use of a PTAT reference (analog TCS) reduces this to 3.8% (8 samples) (Figure 4.27), which is further reduced to 0.35% when the output of the ADC is digitally corrected (Figure 4.27). Each sensor is individually trimmed (at ~23°C and 4A) to correct the spread of the shunt's nominal resistance. From -40°C to 85°C and over a 25V input CM range (ICMR), the ADC exhibits a maximum offset of 24μV, which drops below 1μV after applying CHL (Figure 4.28). The measured inaccuracy of the TS is ±1.2°C without trimming (Figure 4.29), which is quite relaxed (2.5x worse) compared to the TS used in [4].

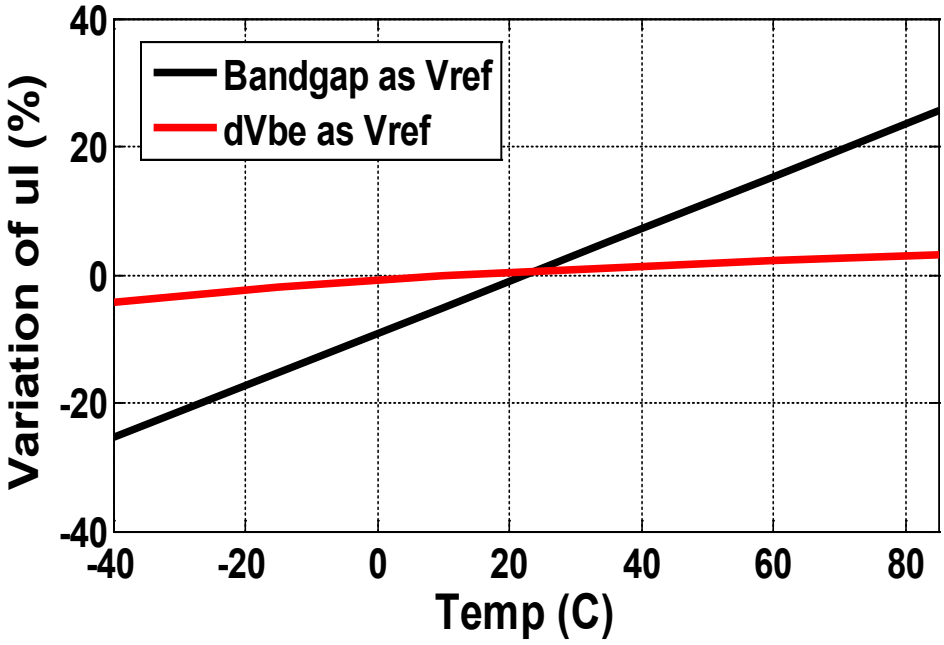


Figure 4.25. Variation of µI over temperature.

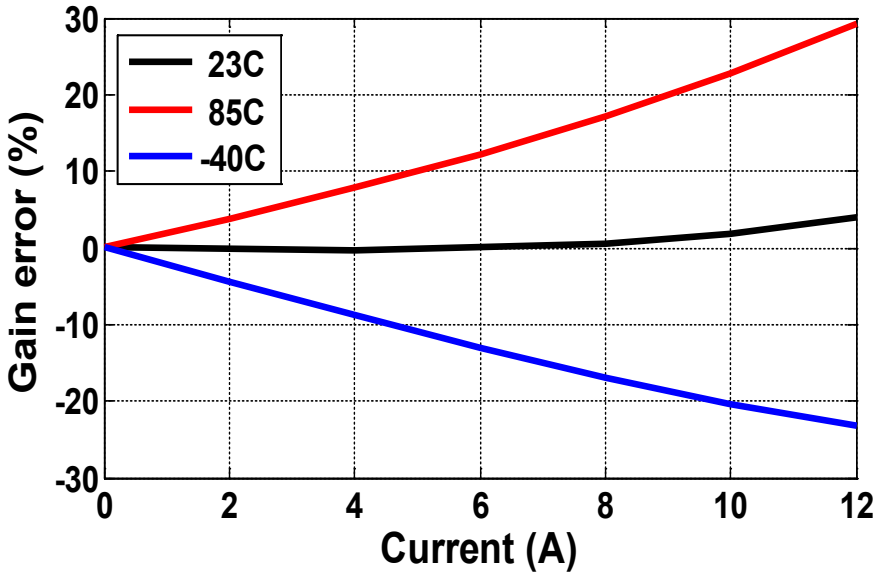


Figure 4.26. Current sensing gain error without TCS.

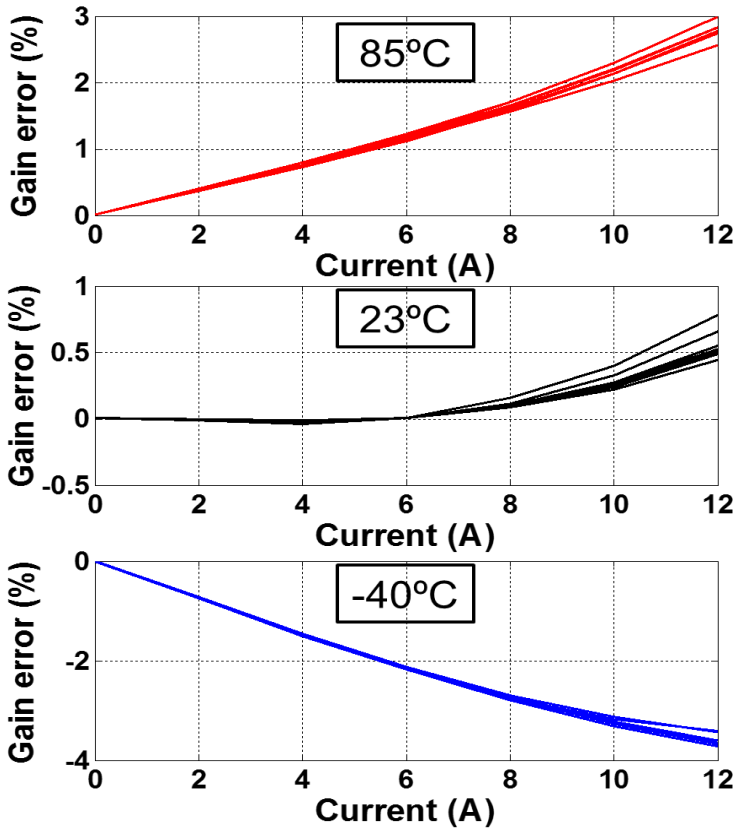


Figure 4.27. Current sensing gain error with only analog TCS.

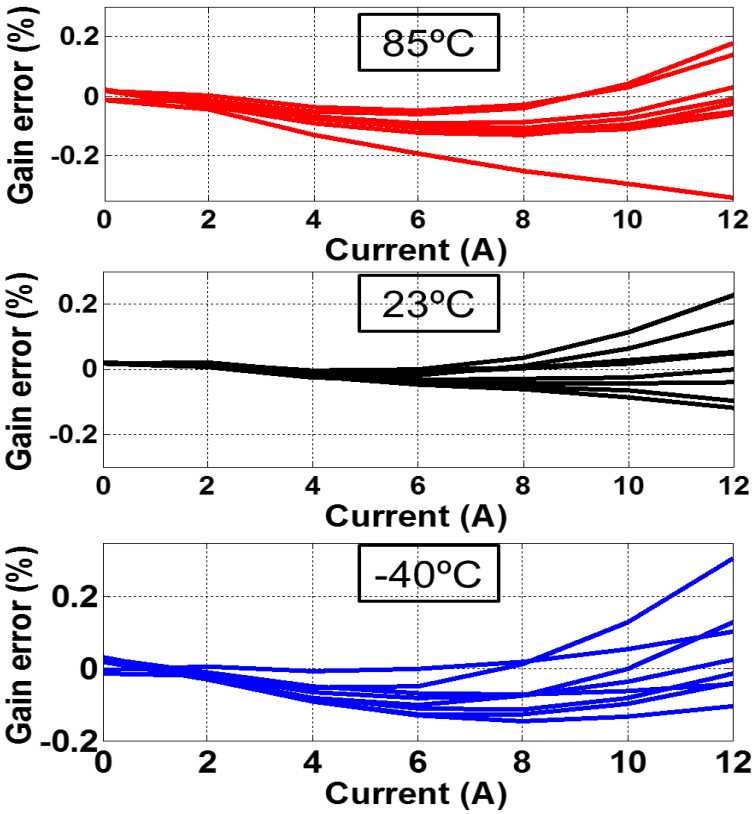


Figure 4.28. Current sensing gain error with hybrid TCS.

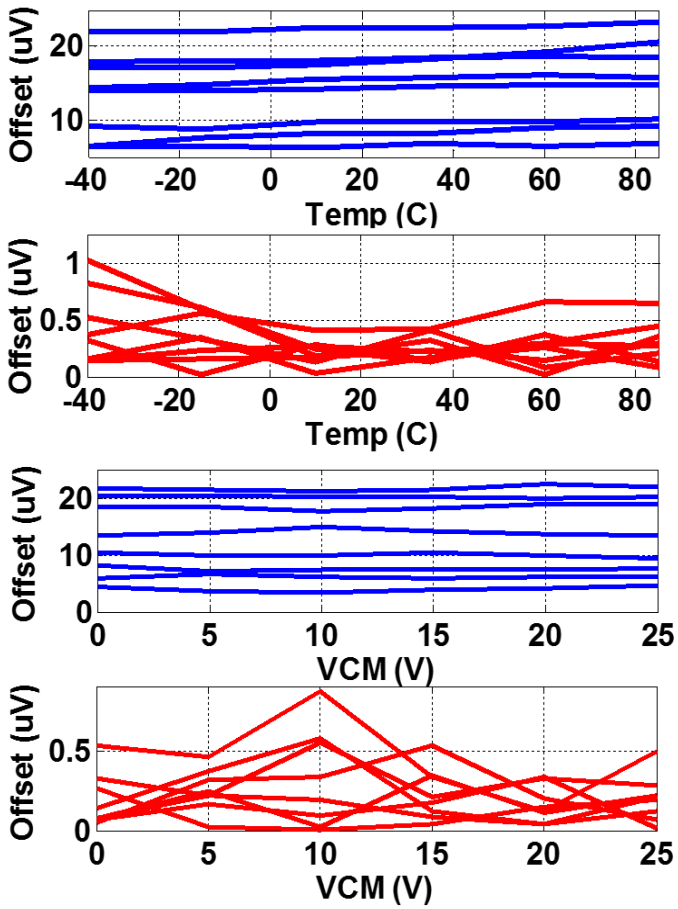


Figure 4.29. Offset before CHL (blue) and after CHL (red) over temperature and ICMR.

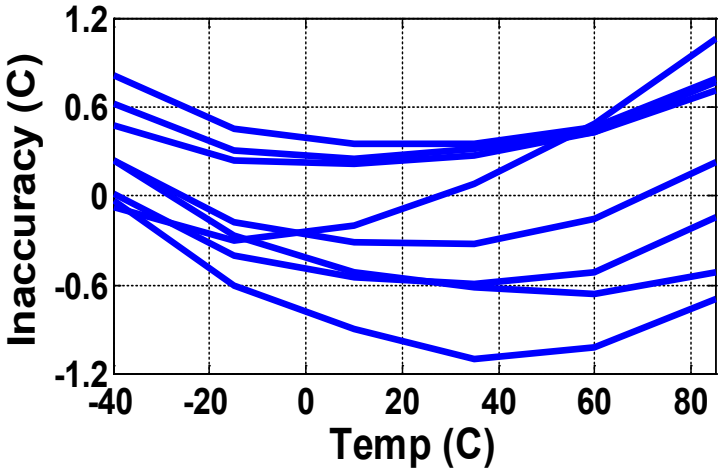


Figure 4.30. Temperature sensing error.

The performance of the sensor is summarized in Table 4.2. Among high-side current sensors [1], [12-13], this design achieves the lowest gain error. Compared to [4] it achieves similar inaccuracy and 30x wider ICMR, by using a beyond-the-rails ADC and a hybrid TCS.

Table 4.2. Performance summary.

	ICMR	I range	T_{Conv}	Resolution	Gain error	Supply current
This work	**25V**	**±12A**	**12.5ms**	**1.1mA$_{rms}$**	**0.35%**	**13.8**µA
[1]	25V	±4A	2.5ms	150µA$_{rms}$	0.9%	10.9µA
[4]	0.75V	±36A	18ms	200µA$_{rms}$	0.3%	13µA
[12]	15V	±30A	100ms	3mA$_{rms}$	1%	9mA**
[13]	36V	±10A	8.2ms	1.25mA$_{rms}$	0.5%*	310µA

* Uses a custom low-TC shunt
**Includes the power of current-sense ADC, voltage-sense ADC, temp. sensor and digital circuitry

4.3 Conclusion

This chapter presents two integrated high-side current sensors based on shunt resistors made from different materials, on-chip metal layers and PCB copper traces. Based on their different temperature characteristics, two TCSs (analog TCS and hybrid TCS) are developed. The analog scheme eliminates the need for a temperature sensor while maintaining a moderate inaccuracy. The hybrid scheme achieves state-of-the-art inaccuracy with a much simpler temperature sensor. In addition, the beyond-the-rails ADC enables the direct digitization of the shunt voltage in the presence of large CM voltage and obviates the use of HV IAs. As a result, the two sensors achieve state-of-the-art power efficiency, as well as low gain error over the industrial temperature range.

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5. Conclusions and Future Work

The main objective of the work described in this thesis is the realization of fully integrated high-side current sensors with low cost and low power consumption. There are two main challenges that stand in the way of achieving this objective. The first is the design of HV interface circuits for high-side current sensing. Previous solutions either consumed too much power or occupied too much chip area. In this work, a beyond-the-rails ADC has been developed to directly digitize small shunt voltages in the presence of large CM voltages. It greatly simplifies the design of HV interface circuits by eliminating the need for HV IAs, thus reducing power consumption and chip area. The other challenge is the design of TCS. Previous solutions required a relatively accurate temperature sensor, thus increasing system complexity and power consumption. In this work, two temperature compensation schemes have been developed to obviate the need for a temperature sensor, or significantly relax its inaccuracy requirements. As a result, they reduce system complexity and lead to a significant improvement in energy efficiency.

5.1 Original Contributions

The main contributions of this work are listed below:

- An improved HV capacitively-coupled chopper has been realized. Compared to previous work [1], it can handle a 14x wider DM signal range ($4.4V_{p\text{-}p}$ with a 5V supply for ADC I) while exhibiting lower leakage current. More protection circuits are also added to improve its robustness in the presence of large CM spikes.

- By using the improved chopper in their sampling front-ends, two beyond-the-rails ADCs were realized. Both achieve decent resolution (18-bit and 15-bit) while maintaining the beyond-the-rails capability (±30V and 29V).
- The similarity between the TC of a PTAT voltage ΔV_{BE} and the TCR of on-chip metal layers is exploited. Based on this, a simple analog temperature compensation scheme (TCS) is proposed to dramatically reduce the power consumption of the current sensor.
- By combining the analog TCS with the digital TCS, a hybrid TCS is created. It achieves similar inaccuracy (0.35%) as a fully digital TCS with a much simpler temperature sensor.

5.2 Future Work

The following issues would be interesting to explore in future work:

- Since the resolution of interface circuits is mainly limited by the *k*T/C noise of SC ΔΣ ADC, a continuous-time ΔΣ ADC [2-3] can be used as interface circuits to further improve the sensor's energy efficiency.
- As shown in chapter 4, the proposed analog TCS does not work well for copper-trace shunts or lead-frame shunts. Since they are usually made of copper alloys [4], their TCR will not be as ideally PTAT as that of pure copper [5]. For such shunts, the temperature dependency of the reference voltage can be adjusted by combining ΔV_{BE} with a scaled version of V_{BE}. In this way, a more generalized analog TCS can be implemented for shunt resistors that are made of both pure metals and alloys. However, since the temperature dependency of V_{BE} has more spread than ΔV_{BE}, its effect on current sensing inaccuracy still needs to be investigated.

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Summary

This thesis describes the design and implementation of integrated high-side current sensors for IoT applications. As explained in chapter 1, the main challenges are the need to achieve low power, low cost and low area while maintaining a reasonably low gain error. To meet them, the focus of this thesis is on (1) the design of precision HV interface circuitry that does not need a HV supply, and (2) the design of energy-efficient temperature compensation schemes that enable the integration of shunt resistors with CMOS circuitry. Several new techniques at both system-level and circuit-level have been proposed and their effectiveness is verified in two prototypes.

An integrated shunt-based current sensor consists of an interface circuit, a shunt resistor and a temperature compensation scheme. Chapter 2 gives an overview of these three elements. It first describes two sensing configurations: low-side sensing and high-side sensing, followed by a discussion of their pros and cons. High-side sensing is favored because of its ability to avoid the ground disturbance and detect the high load current caused by accidental shorts. However, it makes the design of the HV interface circuitry more challenging, as this must accurately and safely extract weak differential signals in the presence of large CM voltages. Several existing solutions are reviewed. However, these either consume too much power or occupy large silicon area. This observation leads to the first challenge addressed by this thesis: the design of power-efficient and compact HV circuitry for high-side current sensing.

In the two prototypes described in this thesis, low-cost shunt resistors based on the metal layers of a CMOS process, or the lead-frame of a standard plastic package were used. However, both of them suffer from a large temperature coefficient of resistance (TCR) (>0.3%/°C), and so a temperature compensation scheme is necessary to achieve reasonable low inaccuracy. Two types (analog and digital) of temperature compensation schemes are reviewed. Analog ones achieve poor (>1%) inaccuracy while digital ones need a dedicated temperature sensor and a rather complex calibration process. This leads to the second challenge that this thesis addresses: the design of temperature compensation schemes that are low power and easy to use, while still achieving reasonable low inaccuracy.

Chapter 3 discussed the design and implementation of two beyond-the-rails ADCs. In order to accurately sample differential signals in the presence of large CM voltages, an improved HV capacitively-coupled chopper was designed. Based on this design, two prototype ADCs were implemented in HV BCD technologies. Both designs achieve a wide ICMR (>25V), high resolution (>15bit) and low offset (<150μV) while operating from a low-voltage supply (≤5V). This beyond-the-rails capability together with high precision enables the direct digitization of small shunt voltages in a high-side sensing configuration, thus eliminating the need for additional HV IAs and reducing the power consumption of the HV interface circuits.

Chapter 4 describes two high-side current sensors based on two types of integrated shunt resistors: metal shunt and copper trace shunt. To match their respective TCRs, an analog temperature compensation scheme was developed for the metal shunt, while a hybrid temperature

compensation was developed for the copper trace shunt. These schemes achieve low inaccuracy (<1%) without using a temperature sensor (analog scheme), or using one with significantly relaxed inaccuracy requirements. In combination with the beyond-the-rails ADC described in the previous chapter, two integrated high-side current sensors were realized. They both achieve state-of-the-art power efficiency, as well as low (<1%) gain inaccuracy over the industrial temperature range.

Finally, chapter 5 lists the main findings of this thesis. Some recommendations for future work are presented. These include: (1) the need to develop versatile analog temperature compensation scheme to match the TCRs of a variety of shunt resistor; (2) the exploration of continuous-time readout circuits to further improve power efficiency.

Samenvatting

Dit proefschrift behandelt het ontwerp en de implementatie van geïntegreerde high-side stroomsensoren voor IoT toepassingen. Zoals beschreven in hoofdstuk 1 zijn de voornaamste uitdagingen het realiseren van laagvermogen, lage kosten en een laag oppervlak met behoud van een goede nauwkeurigheid. Om aan deze eisen te voldoen, ligt de focus van dit proefschrift op (1) het ontwerp van precisie HV-interfaceschakelingen die geen HV-voeding nodig hebben en (2) het ontwerp van energie-efficiënte temperatuurcompensatieschema's. Deze schema's zorgen voor de integratie van de shuntweerstanden met de CMOS-schakeling. Zowel op systeem- en circuitniveau zijn er enkele nieuwe technieken voorgesteld en de effectiviteit hiervan is geverifieerd met twee prototypes.

Een op shunt gebaseerde geïntegreerde stroomsensor bestaat uit een interfacecircuit, een shuntweerstand en een temperatuurcompensatieschema. Een overzicht van deze drie elementen is gegeven in hoofdstuk 2. Dit hoofdstuk beschrijft eerst twee detectieconfiguraties: detectie aan de low-side en aan de high-side, gevolgd door een discussie met de voor- en nadelen hiervan. Detectie aan de high-side heeft de voorkeur, vanwege het vermogen om verstoring van de grond te vermijden en de hoge belasting stroom die wordt veroorzaakt door onbedoelde kortsluitingen te detecteren. Echter maakt dit het ontwerp van de HV-interfaceschakeling uitdagender, doordat het in aanwezigheid van grote CM spanningen veilig en nauwkeurig zwakke signalen moet extraheren. Verschillende bestaande oplossingen worden beoordeeld, echter verbruiken deze te veel stroom

verbruiken of bezetten ze een te groot siliciumoppervlak. Daarom is de eerste uitdaging die in dit proefschrift is behandeld het ontwerpen van energiezuinige en compacte HV-circuits voor high-side stroomdetectie.

Er zijn twee verschillende prototypen beschreven, in de eerste is gebruik gemaakt van goedkope shuntweerstanden die gebaseerd zijn op de metaallagen van een CMOS-proces en in de tweede is het lead-frame van een standaard plastic verpakking gebruikt. Echter hebben beide een grote temperatuurweerstandscoëfficiënt (TCR) (> 0.3%/°C), waardoor een temperatuurcompensatieschema nodig is om een redelijke nauwkeurigheid te bereiken. Daarnaast zijn er twee soorten temperatuur compensatieschema's beoordeeld, namelijk een analoge en een digitale. Analoge schema’s hebben een slechte nauwkeurigheid (> 1%), terwijl digitale schema’s afhankelijk zijn van een goede temperatuursensor en een vrij complex kalibratieproces. Dit leidt tot de tweede uitdaging die is beschreven in dit proefschrift, namelijk het ontwerpen van temperatuurcompensatieschema's die een laag vermogen hebben en daarnaast gemakkelijk te gebruiken zijn, terwijl ze ook nog een redelijke nauwkeurigheid bereiken.

Hoofdstuk 3 beschrijft het ontwerp en de implementatie van twee beyond-the-rails ADC's. Om differentiële signalen nauwkeurig te bemonsteren in de aanwezigheid van grote CM-spanningen, is een verbeterde HV capacitief-gekoppelde chopper ontworpen. Op basis van dit ontwerp zijn er twee prototype ADC's geïmplementeerd in HV BCD technologieën. Beide ontwerpen bereiken een brede ICMR (> 25 V), een hoge resolutie (> 15 bit) en een lage offset (<150 µV), terwijl ze werken op een laagspanningsvoeding ($\leqslant$ 5 V). Dit beyond-the-rails vermogen in combinatie met de hoge precisie maakt de directe digitalisering van

kleine shuntspanningen in een high-side detectieconfiguratie mogelijk. Hierdoor wordt de noodzaak van aanvullende HV IA's geëlimineerd en is het energieverbruik van de HV-interfacecircuits verminderd.

Hoofdstuk 4 beschrijft twee high-side stroomsensoren met twee verschillende geïntegreerde shuntweerstanden: een metalen shunt en een koperen traceer shunt. Om de TCR's te evenaren, is er voor de metalen shunt een analoog temperatuurcompensatieschema ontwikkeld, terwijl er voor de koperen traceer shunt een hybride temperatuurcompensatie is ontwikkeld. Deze schema's bereiken een goede nauwkeurigheid (<1%) zonder gebruik te maken van een temperatuursensor (analoog schema), of gebruiken er een met aanzienlijk versoepelde nauwkeurigheidsvereisten. In combinatie met de beyond-the-rails ADC beschreven in het vorige hoofdstuk, zijn er twee geïntegreerde high-side stroomsensoren gerealiseerd. Ze bereiken allebei de modernste energie-efficiëntie en een lage (<1%) onnauwkeurigheid over het industriële temperatuurbereik.

Het laatste hoofdstuk beschrijft de belangrijkste bevindingen van dit proefschrift. Daarnaast zijn er enkele aanbevelingen voor toekomstig werk gepresenteerd zoals (1) de noodzaak om een veelzijdig analoog temperatuurcompensatieschema te ontwikkelen dat past bij de TCR's van verschillende shuntweerstanden; en (2) het onderzoeken van het gebruik van continue-tijd- uitleescircuits om de energie-efficiëntie verder te verbeteren.

Acknowledgments

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List of Publications

Journal papers:

[1] L. Xu, J. H. Huijsing, K. A. A. Makinwa, “A ±4-A High-Side Current Sensor With 0.9% Gain Error From− 40° C to 85° C Using an Analog Temperature Compensation Technique,” *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3368-3376, Oct. 2018.

[2] L. Xu, S. H. Shalmany, J. H. Huijsing, K. A. A. Makinwa, “A ±12-A High-Side Current Sensor With 25 V Input CM Range and 0.35% Gain Error From− 40° C to 85° C,” *IEEE Solid-State Circuits Lett.*, vol. 1, no. 4, pp. 94-97, Jul. 2018.

Conference papers:

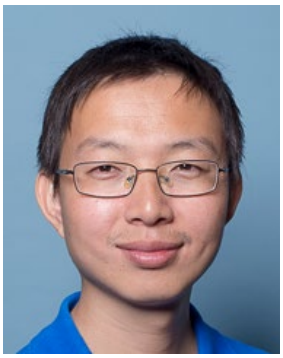
[1] L. Xu, J. H. Huijsing and K. A. A. Makinwa, "A ± 4A high-side current sensor with 25V input CM range and 0.9% gain error from −40°C to 85°C using an analog temperature compensation technique", *IEEE ISSCC Dig. Tech. Papers*, pp. 324-325, Feb. 2018.

[2] L. Xu, B. Gonen, Q. Fan, J. H. Huijsing and K. A. A. Makinwa, "A 100dB SNR ADC with ±30V input common-mode range and 8μV offset for current sensing applications ", *IEEE ISSCC Dig. Tech. Papers*, pp. 90-91, Feb. 2015.

[3] L. Xu, J. H. Huijsing and K. A. A. Makinwa, "A 10-kHz-BW 93.7dB-SNR chopped ΔΣ ADC with 30V input CM range and 115dB CMRR at 10kHz", *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, pp. 49-52, Nov. 2017.

[4] L. Xu, J. H. Huijsing and K. A. A. Makinwa, "A 12μW NPN-based temperature sensor with a 18.4pJ K^2 FOM in 0.18μm BCD CMOS", *in Proc. IEEE IWASI,* pp. 180−182, 2017.

About the Author



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