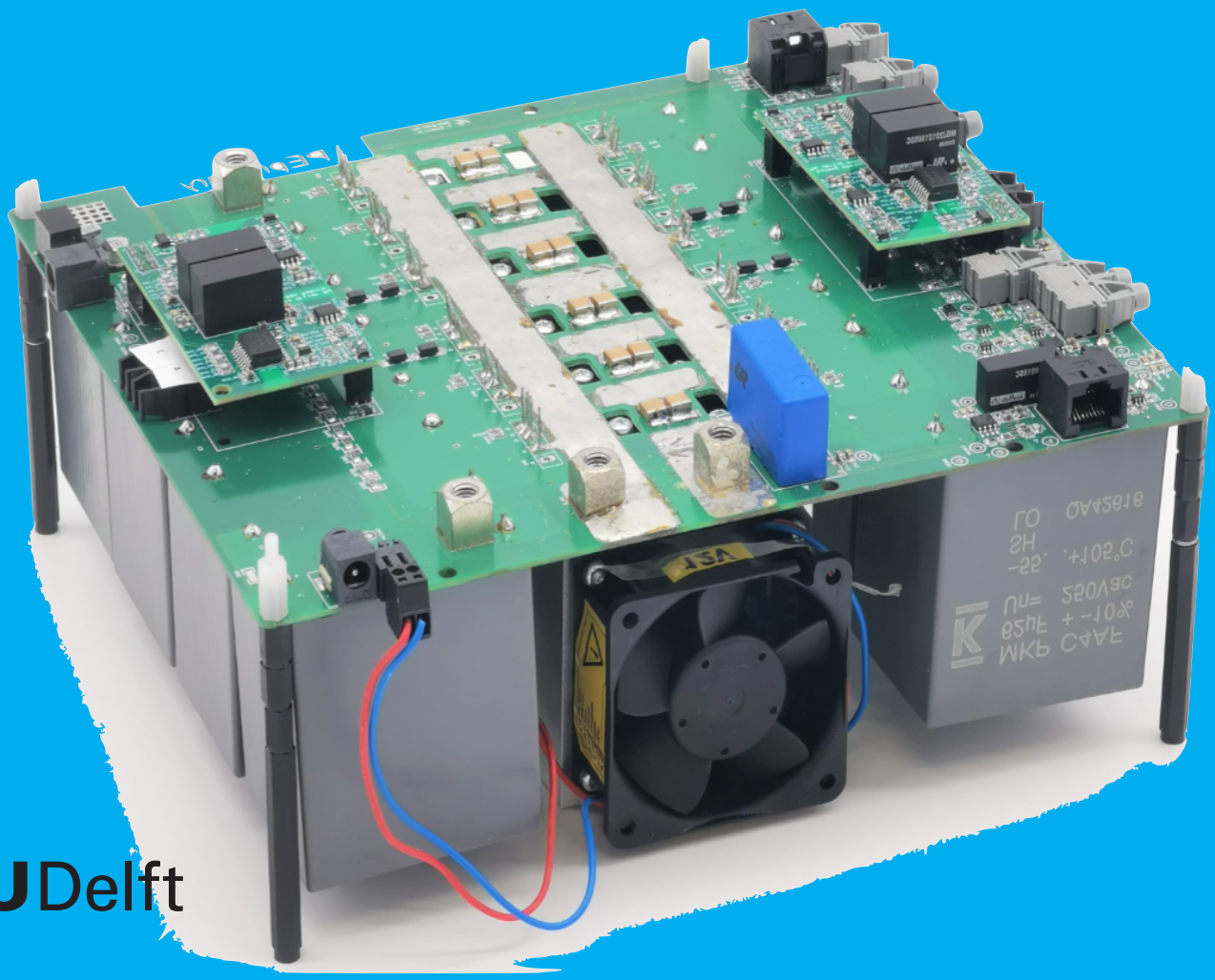
Thesis EE3L11

Design of an inverter in a dynamic inductive power transfer system

J.A. Treurniet
O. Wattenbergh



TU Delft

Thesis EE3L11

Design of an inverter in a dynamic inductive power transfer system

by

J.A. Treurniet
O. Wattenbergh

to obtain the degree of Bachelor of Science
at the Delft University of Technology,

Student numbers:	56238123	5081823
Project duration:	14 April, 2025 – 27 June, 2025	
Thesis committee:	Andrea Neto,	TU Delft, chair
	Wenli Shi,	TU Delft, supervisor
	Dennis van der Born,	TU Delft

TU Delft

Preface and Acknowledgments

0.1. Preface

This thesis presents the design, simulation, and implementation of an inverter and rectifier for a dynamic inductive power transfer (DIPT) system intended for wireless charging of electric vehicles. The work focuses on developing and validating a pulse-width modulation (PWM) strategy for high-frequency switching (85 kHz) to efficiently control both the inverter and the active rectifier.

The system aims to deliver reliable and efficient power transfer under realistic conditions, accounting for coil misalignment and dynamic operation. Key aspects include the implementation of Zero Voltage Switching (ZVS) to minimize switching losses, and the use of phase-shifted PWM signals generated by a TI F28379D LaunchPad. The chosen topology, an H-bridge inverter and active rectifier, was selected to achieve both high efficiency and precise control over the power flow.

Simulations in Simulink, combined with hardware testing, were used to verify design choices and validate performance against predefined system requirements. The results demonstrate that the proposed control strategies enable stable power delivery across a broad range of operating conditions.

This thesis forms part of a broader effort within the TU Delft BSc Electrical Engineering program to explore practical solutions for dynamic wireless EV charging, contributing to the development of sustainable transportation technologies.

0.2. Acknowledgments

We thank our project leader, Wenli Shi, and our supervisor, Hossein Haghnazari, for their supervision, help, and patience. We are also grateful to Bart Roodenburg for his incredible support. Special thanks to Julie Diender, Nathan van Himbergen, Stefan de Jong, and Stefan Kort, the members of the other subgroups of our project. Finally, we thank our partners, friends, and family for always supporting us.

J.A. Treurniet
O. Wattenbergh
Delft, 2025

Contents

1 Introduction

People have always had a desire to travel: nomadic tribes, pilgrimage, and oversees travels to discover the world. In the beginning this was done by horse, then by ship, train, and finally with commercial vehicles. The world has changed since then, the effects of carbon emissions are in full view: worsening health, extreme weather and a negative effect on the environment. To reduce emissions, fossil fuel is being swapped with electricity as a main source of power. More and more vehicles are being made electric instead of fossil-fueled. There is a problem that remains. Electric vehicles (EV) provide less travelling freedom than combustion engines.

In 2025, the rise of EVs is clearly visible, a quarter of the new cars being sold worldwide is electric [1]. This might be due to many governments that are encouraging the development of the EV market to reduce greenhouse gasses. Nevertheless, there are a few drawbacks compared to combustion engines: they are more expensive, heavier and take a long time to recharge [2]–[4]. There are several solutions that are being investigated such as: improving batteries, battery swapping stations and dynamic wireless charging of EVs [2].

A lot of research is being done on how to make batteries more efficient. The research into batteries is already quite mature [5], but a lightweight, power-efficient battery which is in direct competition with fossil fueled car has yet to be found. A second option would be a battery swapping station, however new limitations arise with this solution, batteries need to be interchangeable, the cost for a second battery is quite high and there are safety concerns with storing large amounts of batteries [6]. A different way to extend the driving range is by using a dynamic inductive power transfer system, enabling EVs to be charged while driving [7]–[9]. This allows the driving range to be extended while keeping the battery compact.

The ideal situation is a reliable, efficient and cost effective charging method to allow EVs to be the transportation method of the future.

1.1. Proposed system description

Such a DIPT system can be divided into three parts, as illustration is depicted in Fig. 1.1. Each part of the system is being researched by a different subgroup as part of the TU Delft Electrical Engineering Bachelor's End Project.

The first part is the controller [10]. Using feedback- or feedforward control, this controller ensures that the system delivers a smooth supply of power to the EV, by generating a reference voltage signal for the PWM controller of the inverter.

The inverter combined with the PWM controller and the rectifier constitutes the second part of the system, the converter. This part of the system converts a DC input voltage to an AC voltage for the coils on the transmitter (Tx) side, and rectifies the AC voltage to a DC voltage on the receiver (Rx) side.

The last part of the system is the magnetic coils, which allow the system to wirelessly transfer power from the Tx- to the Rx-coil [11]. In a dynamic inductive power transfer (DIPT) system, the Tx-coils are embedded in the road, and transfer power to the Rx-coils, which are in a moving object.

This thesis focuses on the converter part of the DIPT system.

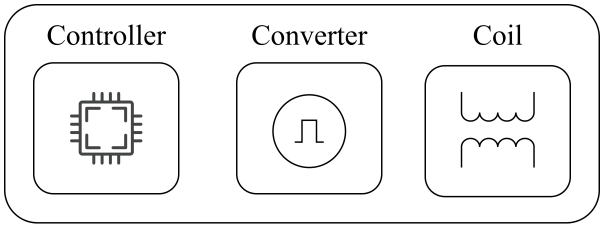


Figure 1.1: Overview of the 3 parts, and subgroups, for the proposed DIPT system

1.2. Thesis structure

This thesis has the following structure. In Chapter 2, the problem definition and program of requirements is discussed. Chapter 3 gives an operational overview of the entire system, including some components not further discussed in this thesis. In Chapter 4, the generation of PWM signals and strategies to do so are outlined. Chapter 5 gives a description of rectifier topologies. Chapter 6 describes the design and construction of the simulation used to verify design choices. The plan and results of testing are discussed in Chapter 7. A discussion about the mistakes can be found in Chapter 8. The conclusion of this thesis is discussed in Chapter 9. Recommendations on how to continue the work in this thesis is also discussed in this chapter.

In appendix A a list of used hardware, software, and written code can be found.

2

Problem definition

As mentioned in the previous chapter, this thesis consists of three subgroups. This report is focused on the signal generation used to drive the inverter and rectifier. This signal will be a PWM signal. This chapter gives a quick overview of the system and the program of requirements.

2.1. System overview

2.1.1. Inverter

The inverter will be located within the road, or near the road. It will convert a DC voltage into an AC voltage which will be used to drive the coils embedded within the road's surface. The signal used to drive the inverter will need to be modulated by the control system to ensure efficient power transfer between the stationary road coils and the moving vehicle's coils. This control system is out of the scope of this thesis.

2.1.2. Rectifier

The rectifier is located within the vehicle. It will convert the AC signal generated by the receiving coil into DC power, which will be used to charge the vehicle's battery. This rectification can be passive by using a diode bridge or active by using driven switches instead of diodes [12]–[15]. The benefit of active rectification is the additional control over the output power of the wireless energy transfer system. There are several rectifier topologies, this project will use the H-Bridge topology due to its high efficiency and energy-transfer capability, compared to for instance a half-bridge.

2.1.3. PWM control signal

A PWM control signal controls the inverter and possibly the active rectifier. To do this, a PWM strategy is implemented [16]–[23]. This strategy is optimized to transfer power as efficiently as possible. It therefore uses Zero Voltage Switching, which ensures the inverter switches on only when the voltage over the output capacitor of the MOSFET is zero, so there is no power loss.

2.2. Simulink Model

A model of the complete DIPT system will be constructed in simulink. This model will be used to generate simulations that will drive and verify design decisions. It is therefore necessary for this model to accurately represent the real world, while still being as simple as possible.

2.3. Program of requirements

In order to design our system, a Program of Requirements (PoR) was set up. The PoR consists of performance indicators including conditions applying to its development, production and implementation amongst others. We will use the PoR put forward in the following sections for assessment of the design and results throughout the thesis. The goal of this project is to design a script that generates a

PWM signal that controls the inverter. This signal and the system it is implemented in have to comply to some requirements. Those requirements are listed below.

2.3.1. Global system requirements

The global system requirements are shared between all three sub-groups of this BAP project. They consist of number of functional requirements, followed by specific performance requirements.

2.3.2. Functional requirements

1. The Tx- and Rx-side of the system must be separated without a physical link.
2. The complete system must be able to inductively transfer power to a moving vehicle (dynamic).
3. The complete system must be able to lower the amount of power ripple, compared to a non-controlled standard situation.
4. The system must operate on the specified, already established hardware in the ESP lab.
5. The system must be physically tested during the project scope.
6. The radiated power must not be harmful for humans.

2.3.3. Performance requirements

1. The system operates on a switching frequency of 85 kHz.
2. The system has a maximum input voltage of 30 V.
3. The system has a maximum input current of 1 A.
4. The system must be able to invert the voltage from a DC power supply.
5. The system must be able to rectify the outgoing current on the receiver side.

2.3.4. Specific requirements for the converter

1. A minimum power efficiency of 98%
   The inverter needs a high enough efficiency to be usable in real applications.
2. Implementing zero-voltage switching in PWM generation
   This technique is used to achieve the aforementioned efficiency requirement by reducing switching losses in the power switches of the inverter (3.0.3).
3. PWM strategy must be compatible with TI F28379D LaunchPad
   This is a specification of 2.3.2.4, because it is actually very relevant and important to this specific part of the project. The system uses this microcontroller development board 7.2.1, so it should be possible to implement the PWM strategy on this board.
4. Use of reference voltage to determine the conduction width of the output voltage, thus controlling the output power
   The controller that will be developed by another sub-group of this Bachelor End Project [10] outputs a reference voltage. The converter should make sure the output voltage of the inverter matches this reference voltage by using PWM.

3

Operation Overview

This system uses an inverter, controlled by a PWM signal, that creates a pulse wave. That PWM signal is created by a PWM generator. Because a pulse wave has a lot of unwanted harmonics, there is a compensation circuit added to the output of the inverter. This circuit makes sure a sine wave is sent through the coil at the output. The receiving coil also has a compensation circuit, which feeds into the rectifier. The output of the rectifier is fed into the battery to charge. This section will walk through the basic operation of the PWM generator, inverter, the compensation circuits and the rectifier.

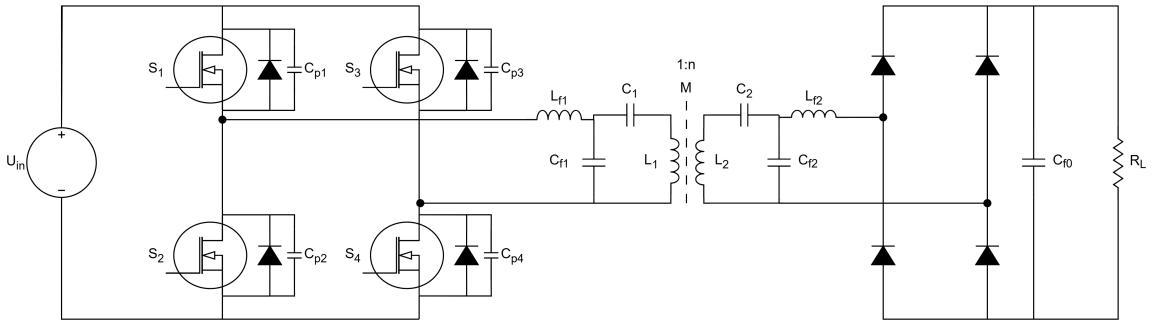


Figure 3.1: An inverter with full bridge topology and passive rectifier.

3.0.1. PWM generator

The PWM generator outputs the gate signals to drive the inverter's MOSFETs. The duty cycle of the PWM signal will be modulated based on a reference voltage from the controller [24]–[27]. By generating a PWM signal with a certain duty cycle, the power output of the inverter can be controlled. Both the controller and PWM generator are located on the TI F28379D LaunchPad 7.2.1.

There are multiple PWM strategies that can be used to drive the inverter. These strategies are discussed in section 4.

3.0.2. Inverter

The inverter uses a full bridge topology. This means it exists of two parrallel rows of two MOSFETs. Those two rows are connected to a DC voltage source. The MOSFETs are turned on in crosswise pairs by the PWM signal. If that PWM signal is perfectly square, with a duty cycle of 50%, it creates a square wave. In Figure 3.1, at one time, S_1 and S_4 are turned on or S_2 and S_3 are turned on. This creates the earlier mentioned square wave, with a maximum voltage of u_{in} and a minimum voltage of $-u_{in}$. This is illustrated in figure 3.2.

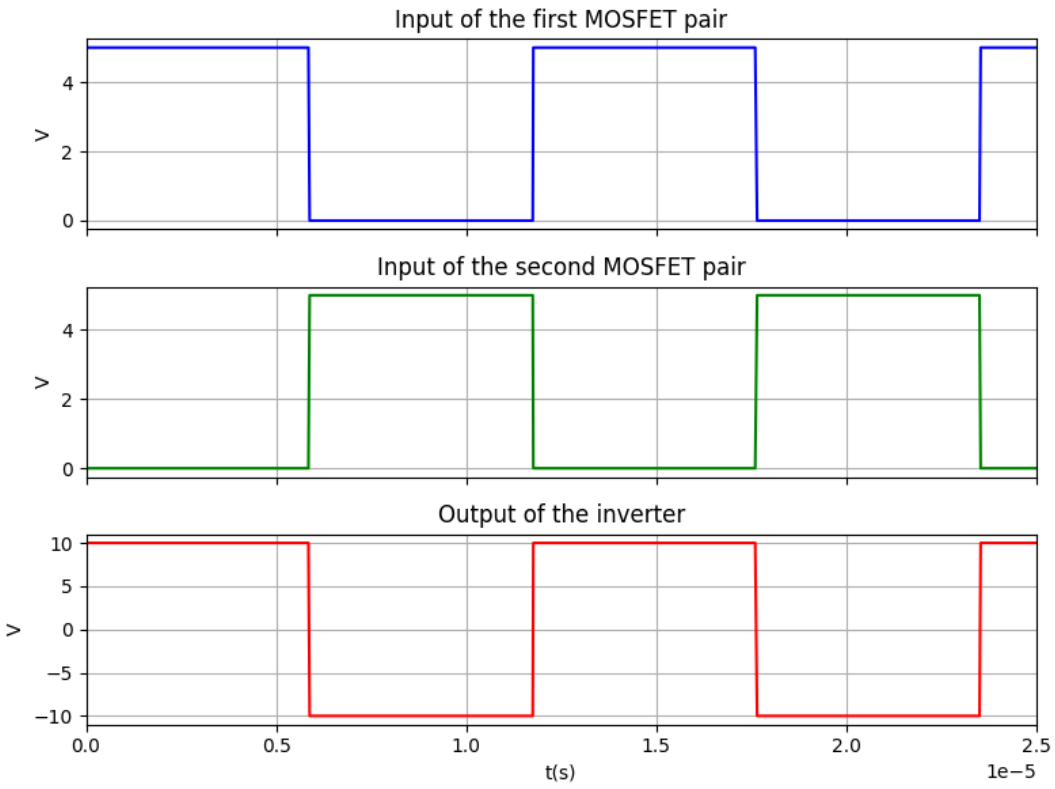


Figure 3.2: The signals of a full bridge inverter, using gate voltages of 5 V and and DC input voltage of 10 V

3.0.3. Zero Voltage Switching

In real-world inverters, non-ideal components cause switching losses due to the overlap of voltage and current (As can be seen in Figure 3.4) during MOSFET transitions. This is particularly significant when driving inductive loads, such as coils in power transfer systems, where current lags voltage. To minimize these losses, zero voltage switching (ZVS) is applied.

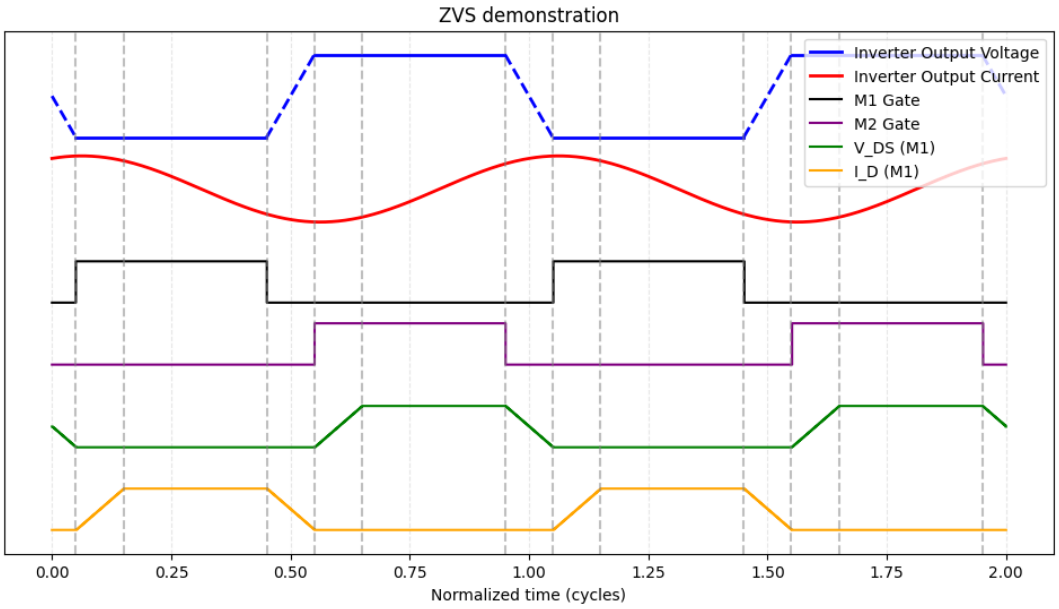


Figure 3.3: Demonstration of Zero Voltage Switching (ZVS) in an inverter

ZVS ensures MOSFETs switch when the drain-source voltage is zero, eliminating overlap between voltage and current. This is achieved by introducing a dead-time interval in the PWM signal [28]. This dead time is introduced to delay the gate signal of the MOSFET that is about to turn on, ensuring that the inductive load current flows through its body diode after the output capacitor (C_{oss}) is discharged. This process brings the drain-source voltage of the MOSFET close to zero before the gate driver applies the turn-on signal. As a result, the MOSFET switches on with nearly zero voltage across it, greatly reducing switching losses [29]. It should be noted that ZVS operation eliminates only turn ON losses; switching losses during turn OFF, both due to overlap and C_{oss} charging, will still be incurred, as can be seen in Figure 3.4.

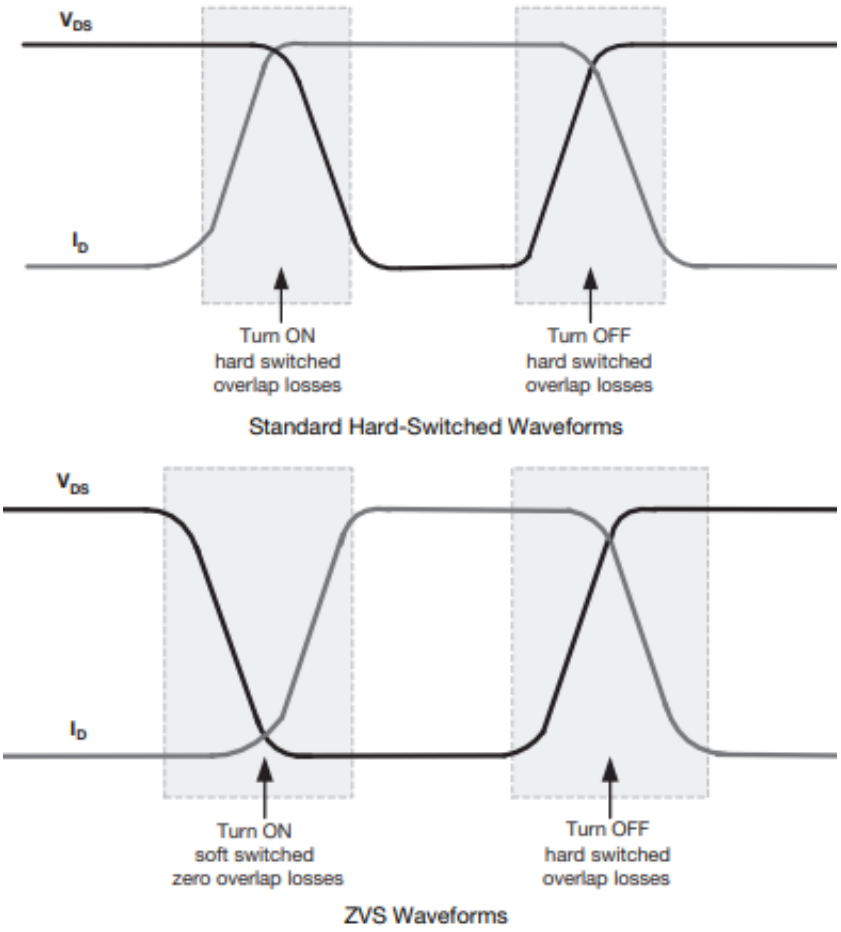


Figure 3.4: Comparison of MOSFET voltage and current waveforms under standard hard switching and Zero Voltage Switching (ZVS). Source: [30]

Fig. 3.4 compares the voltage and current waveforms of a MOSFET during standard hard switching and during Zero Voltage Switching (ZVS). In the hard-switched case (top), both voltage (V_{DS}) and current (I_D) overlap significantly during turn-on and turn-off transitions, leading to high switching losses. In the ZVS case (bottom), the voltage across the MOSFET is reduced to zero before turn-on, eliminating overlap losses during turn-on. Turn-off is still hard-switched, but overall switching losses are significantly reduced due to ZVS at turn-on.

3.0.4. Compensation

The output of the Full-bridge inverter is compensated by a DLCC compensation circuit [31]–[34] . That means it uses two capacitors and an inductor on both sides of the transformer to modulate the square to a sine wave. This form of compensation has a high tolerance for misalignment of the coils, meaning the compensation is still adequate when the coils are not aligned optimally, which often happens due

to the stochastic movements of a vehicle driving on a motorway.

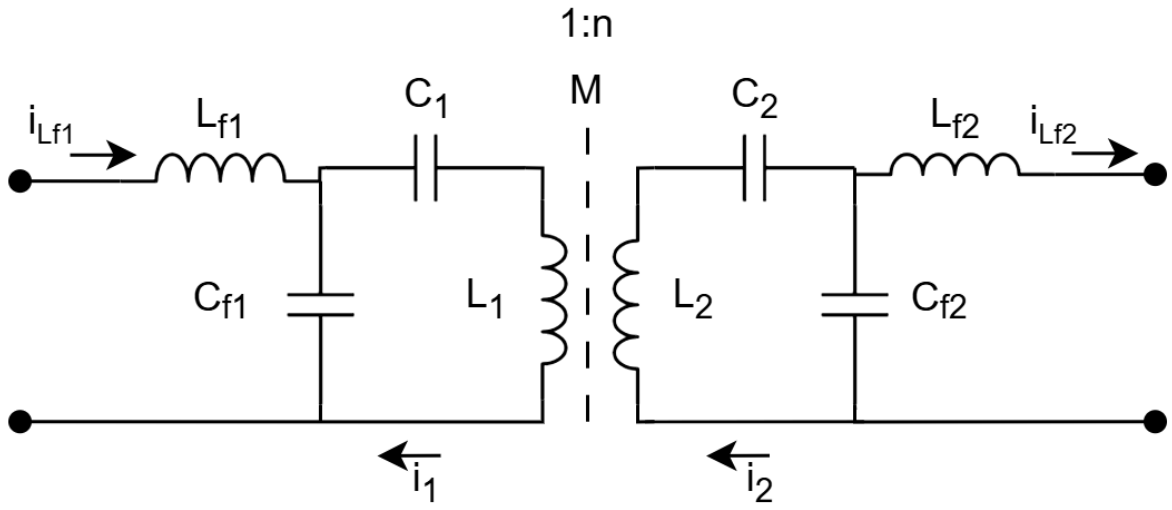


Figure 3.5: Both sides of the transmit and receive coils with LCC compensation.

In 3.5, the circuit for DLCC is shown. C_{f1}, C_1 and L_1 form a resonance tank. This means the current through the transmit coil is only dependent on the RMS value of the input voltage U_{in} and the value of L_{f1}. The formula for that current in phasor form is [35]:

$$I_1 = \frac{U_{in}}{j\omega_0 L_{f1}} \tag{3.1}$$

The receiver side of the circuit also has a resonance tank, which means the formula for the current through that coil is:

$$I_2 = \frac{U_{out}}{j\omega_0 L_{f2}} \tag{3.2}$$

Notice that in the first case, the mutual inductance M is no factor in the equation. This means the current is not dependent on the mutual inductance and this compensation circuit is therefore very useful for this system where misalignment causes great fluctuations in M. Using substitution, we see that the output current on the receiver side, $I_{L_{f2}}$ can be expressed as:

$$I_{L_{f2}} = \frac{k\sqrt{L_1 L_2}U_{in}}{j\omega_0 L_{f1} L_{f2}} \tag{3.3}$$

and since:

$$M = k\sqrt{L_1 L_2} \tag{3.4}$$

This equation can also be written as:

$$I_{L_{f2}} = \frac{MU_{in}}{j\omega_0 L_{f1} L_{f2}} \tag{3.5}$$

This means that for the goal of a constant output and a fluctuating M, the input voltage should be controlled in such a way that the fluctuations of M are cancelled out. This is exactly what the Control system is able to do (Which is outside of the scope of this report, but can be found in our sister report [10]). The mathematical derivation of the PWM signal can be found in Section 4.5.

3.0.5. Rectifier

The rectifying part of the system can be done in multiple ways. The most simple topology is a passive full bridge diode rectifier. This uses four diodes to rectify the incoming AC signal and a large capacitor to ”flatten” the output. This is a perfectly well working topology, but it does not offer any control over the output power.

The other option is active rectifying. This uses a very similar circuit to that of the inverter. It consists of four MOSFETs that are turned on and off in alternating pairs. This means there is some type of synchronization needed, but also gives control over the output power, since the control input for the MOSFETs can be regulated. Using this topology effectively creates a Dual Active Bridge [12]–[15] between the inverter and rectifier. Besides the additional control over output, active rectification also allows for more efficient conversion. The rectifier will need to be synchronized with the inverter. The topology of the rectifier and the synchronization that is required is further discussed in Chapter 5.

4

PWM strategies

There are several PWM strategies. First it must be decided whether Uni-polar or Bi-polar signals must be generated, afterwards a specific strategy can be selected.

If the duty cycle of the PWM signal is 50%, the output is a square wave. This wave carries the most power, but also has the problem of creating a lot of harmonics. There are other types of PWM signals. These signals carry less power, but contain less harmonics.

4.1. Bi-polar and Uni-polar PWM

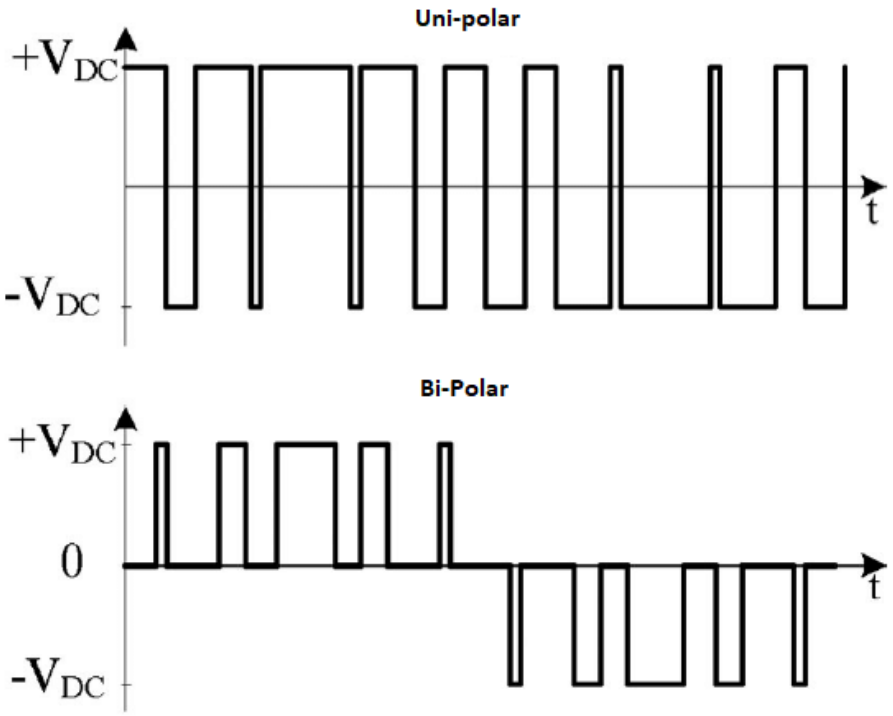


Figure 4.1: Uni- and Bi-Polar PWM. Source: [36]

In bi-polar PWM, the output voltage switches between the full positive and negative levels, $\pm V_{\mathrm{dc}}$, and 0V. [37]. Two carrier comparisons are used: one for the positive half-cycle and one for the negative half-cycle. During the positive half of the reference waveform, the output toggles between $+V_{\mathrm{dc}}$ and

$0\,\mathrm{V}$; during the negative half, it toggles between $-V_{\mathrm{dc}}$ and $0\,\mathrm{V}$. This results in lower harmonic distortion and improved spectral characteristics compared to bi-polar PWM [37].

In uni-polar PWM, the output switches between $0\,\mathrm{V}$ and either $+V_{\mathrm{dc}}$ or $-V_{\mathrm{dc}}$. This is achieved by comparing a reference waveform with a high-frequency triangular carrier signal. When the reference is greater than the carrier, the output is $+V_{\mathrm{dc}}$; when it is lower, the output is $-V_{\mathrm{dc}}$. This method results in a waveform that continuously toggles between positive and negative voltages, providing efficient switching and harmonic performance

These PWM strategies are used in low frequency applications; for instance, 50 Hz machine drives.

4.2. Carrier-based PWM strategies

In carrier-based PWM strategies, a carrier-wave is generated; for example a sawtooth or a triangle wave. The carrier signal is compared to a reference signal to generate the pulse train. The type of reference single determines the type of PWM that is generated. The main types of carrier-based PWM strategies are listed below.

4.2.1. Single-Pulse Width Modulation

Single-PWM is the simplest carrier-based PWM type. A reference signal is compared to a triangle carrier signal. This will create a single pulse per cycle, where the width is directly correlated to the voltage of the reference signal. This technique is a very simple one. The problem with this technique is related to the ”dead time” that occurs between the pulse for the first and second pair of MOSFETs. When all the MOSFETs are switched off, the diodes that are in parallel with the MOSFETs in reverse will form a diode bridge that will conduct the current that the inductive load will generate upon switching off the MOSFETs and therefore create an unwanted current spike in the signal. This can be seen in figure 4.2.

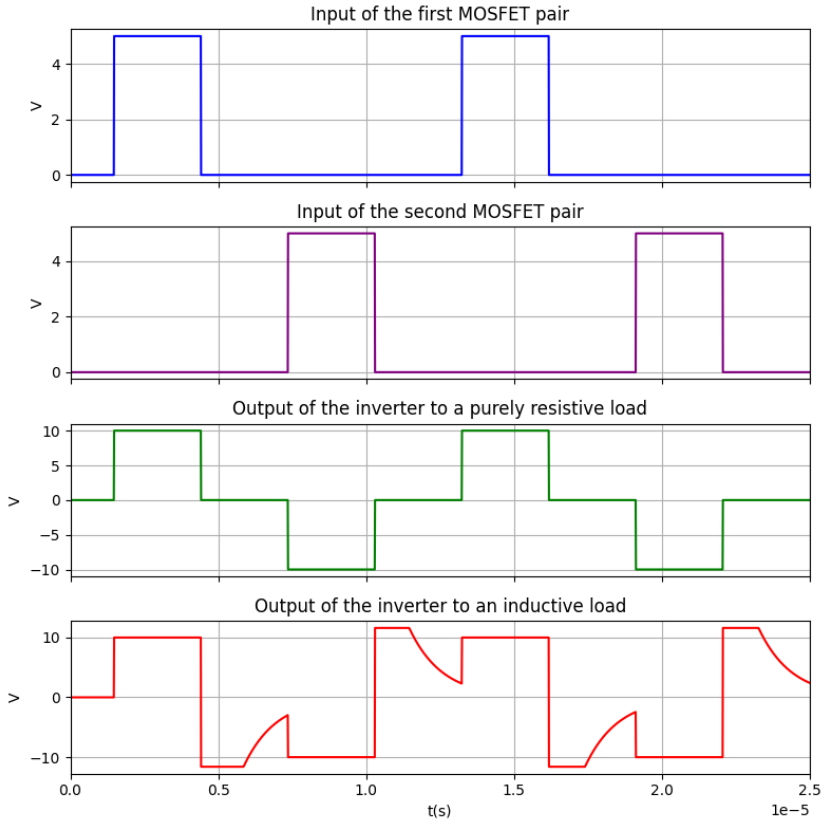


Figure 4.2: Input and output of Single-PWM with an inductive load, with gate voltages of 5 V and U_{in} of 10 V

4.2.2. Multiple-Pulse Width Modulation

Multiple-PWM is comparable to Single-PWM and is created in the same way. The defining difference is that in Multiple-PWM there are more pulses per cycle. The amount of pulses per cycle can be controlled by varying the carrier signal frequency compared to the output cycle frequency. The higher amount of pulses per cycle makes this method more accurate than single-PWM, but is slightly more complex to implement.

4.2.3. Sinusoidal Pulse Width Modulation (SPWM)

SPWM is a carrier-based PWM type where the Pulse train is generated by by comparing a sinusoidal reference signal with a triangle carrier signal. The width of pulses changes in accordance with the amplitude of the reference signal. The frequency of the reference signal determines the frequency of the output signal. The number of pulses in each output signal cycle is determined by the carrier frequency, meaning that a higher frequency carrier frequency increases the resolution of the PWM signal. This method of PWM signal generation is often used in industrial and commercial grade inverters operating at low frequencies [38].

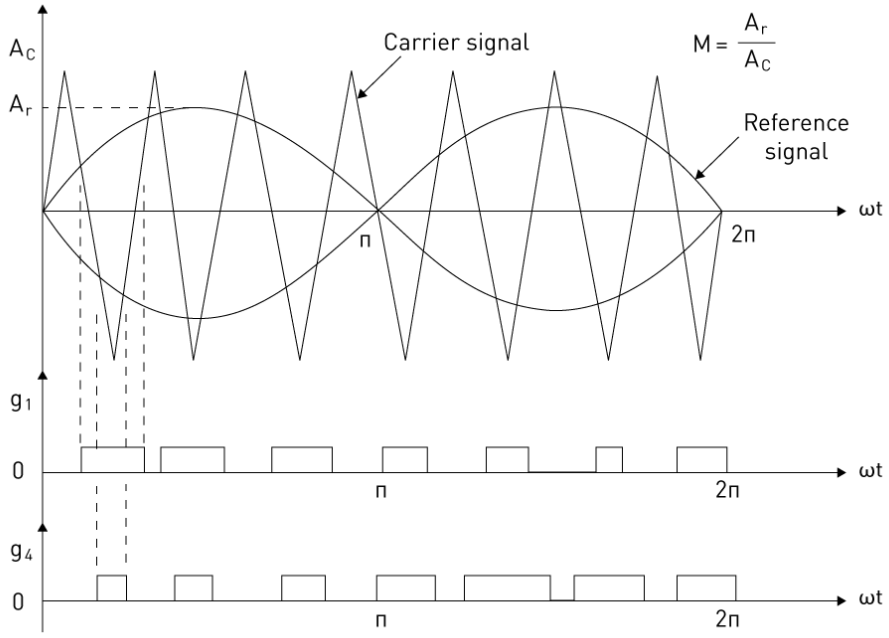


Figure 4.3: Gate Signal Generation in SPWM. Source: [39]

4.3. Selective Harmonic Elimination (SHE)

Selective Harmonic Elimination (SHE) is mainly used in grid-connected inverters to meet Total Harmonic Distortion (THD) standards. This method is typically applied to multilevel inverters. SHE eliminates higher order harmonics without the use of filters [40]. This method uses a lot of real-time computation and the advantage of Harmonic Elimination is severely decreased when used with a bi-level inverter. Furthermore, additional hardware is needed for implementing this strategy. For these reasons it will not be used in this thesis.

4.4. Phase Shifted PWM (PS-PWM)

Phase Shifted PWM (PS-PWM) is a PWM strategy that uses a phase shift between the two signals of the same pair, so S_1 and S_3 or S_2 and S_4 in this case [41]. By introducing this phase shift, ZVS can be guaranteed and the conduction width can be modulated without making the inverter a passive diode bridge. This means there are four distinct modes in which the system can be described. The first mode, mode 1, is when both S_2 and S_3 are on. At this point a negative voltage is the output of the inverter.

In the next mode, mode 2, S_2 is switched off and S_1 is switched on. This means there is 0 V over the output, since both S_1 and S_3 are conducting. In mode 3 S_3 is switched off and S_4 is switched on. This results in a positive voltage at the output. In the last mode, mode 4, S_1 is switched on and S_2 is switched off. Therefore, there is 0 V over the output, as both S_2 and S_4 are conducting. At this point, ZVS is not implemented. To implement this, there are 4 extra modes added. These ZVS commutation modes [42] leave room for the capacitors of the MOSFETs to discharge and charge. In practice, this results in a small time gap between the switching off of S_1 and the switching on of S_2 and vice versa and the same goes for S_3 and S_4. A table displaying the required modes for ZVS can be found in Section 6.3.1. This PWM strategy is used in high frequency applications, like the 85 kHz system used in this thesis.

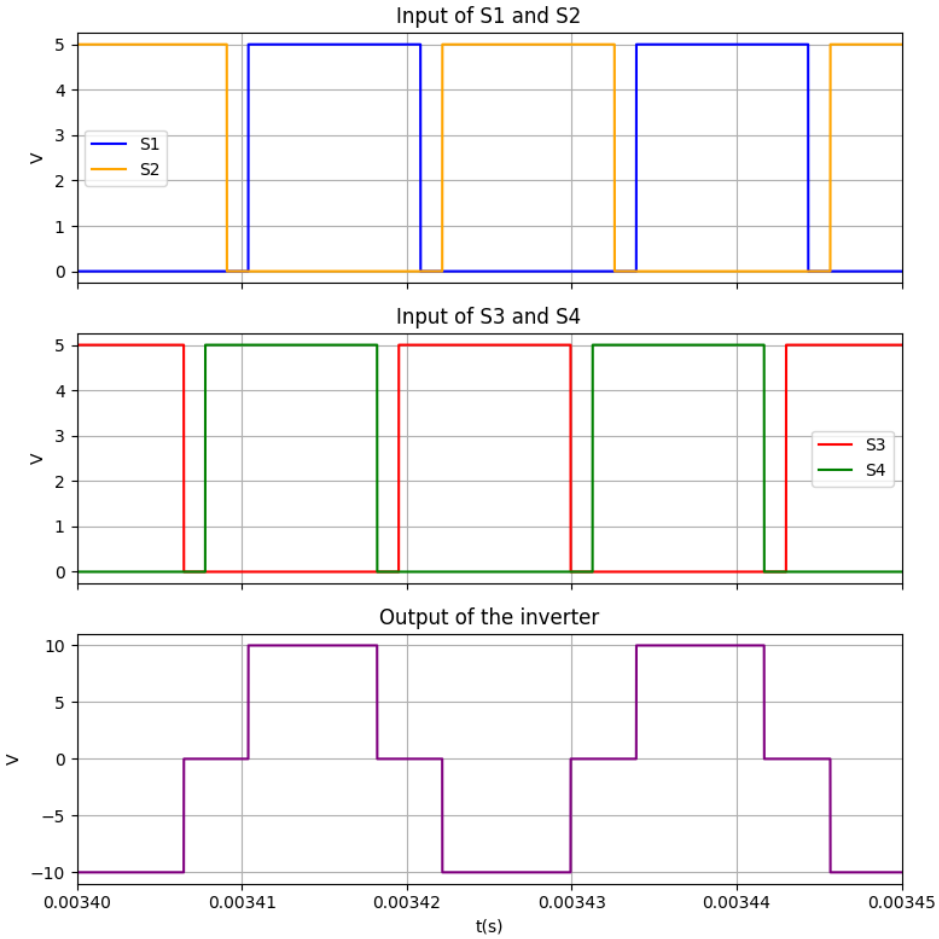


Figure 4.4: PS-PWM Gate Signals and resulting output of the inverter connected to a 50Ω load

4.5. Mathematical Derivation of the conduction width

As seen in section 3.0.4, the RMS output voltage of the inverter is the variable that has to be controlled with the PWM signal. To do this, it is necessary to know the way that RMS value is dependent on the conduction width D. The conduction width is the width of the pulse wave at the output of the inverter, so it is the duty cycle of the output voltage. For practicality, it will be called conduction width to make sure it is not confused with the duty cycle of the PWM signals. The relation between the RMS output voltage and the DC input voltage when the conduction width is 50%, so the maximum value, is [43]:

$$U_{out} = \frac{2\sqrt{2}}{\pi} V_{dc} \tag{4.1}$$

where U_{out} is the RMS value of the output voltage of the inverter and V_{dc} is the DC voltage that is the input for the inverter. Since the goal is to be able to change this voltage using the conduction width, the equation that derives that relation is needed. According to [44], this relation is:

$$U_{out} = \frac{2V_{dc}}{\pi}\sqrt{1 - cos(2\pi D)} \tag{4.2}$$

Where D is the controllable variable; the (normalized between 0-0.5) conduction width of the inverter output. This means the conduction width that is needed at the output of the inverter is:

$$D = \frac{1}{2\pi}\cos^{-1}\left[1 - \left(\frac{\pi U_{ref}}{2V_{dc}}\right)^2\right] \tag{4.3}$$

Where U_{ref} is the reference voltage coming from the controller. This formula is integrated in the PWM generating code, as can be seen in Appendix A.3.1.

4.6. Choice of strategy

For this project, the Phase Shift PWM strategy was chosen. This strategy is relatively simple to implement, while providing a broad ZVS range and stable operating frequency. It is therefore possible to achieve all the requirements Section2.3. The other PWM strategies are not as suitable, because they either can not achieve a broad ZVS range or operate in a single frequency or require a multilevel or multiphase topology of the inverter.

5

Inverter and Rectifier topology

5.1. Inverter

The inverter topology used in this design is an 'H-Bridge-', or 'Full-Bridge-', Inverter. The topology is practically identical to the topology used for the Active Rectifier (and identical to the Passive Rectifier, with diodes instead of MOSFETs) (For both see section 5.2.1).

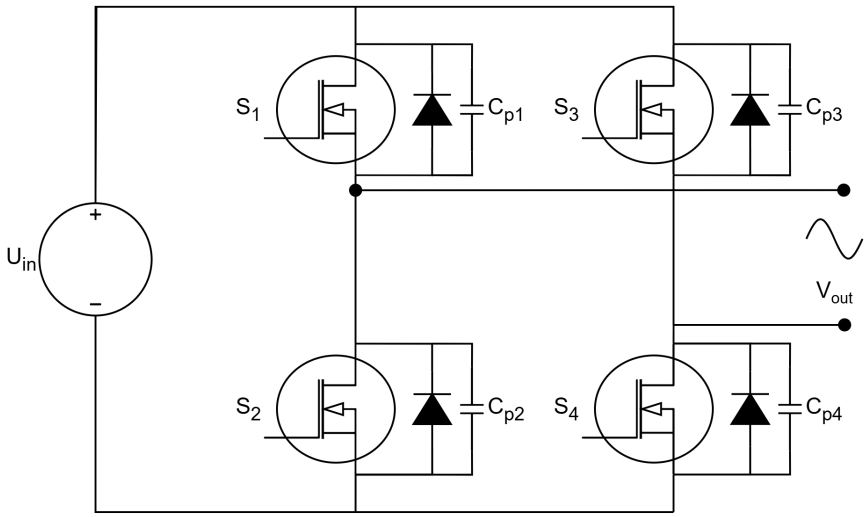


Figure 5.1: A full bridge Inverter

5.1.1. Selection of MOSFETs

For the selection of a suitable MOSFET to use in this system, there are four relevant parameters that need to be looked at. These are the voltage and current rating, output capacitance and on-resistance. The voltage rating should be 1.5 times the maximum voltage that it is expected to handle [45], so that would be 150 V. The current rating should also be 1.5 times the maximum it is expected to handle, so that would be 15 A. For both the output capacitance and the on-resistance, the lowest value should be selected. However, since the effect on the efficiency by the output capacitance will be counteracted by ZVS, but the effect of the on-resistance will not, the on-resistance should have priority over the output capacitance, when the criterium is efficiency. If the criterium is highest output power, the output capacitance should be prioritized, since that means the maximum duty cycle of the PWM signal while maintaining ZVS can be larger, which means higher power output. The output capacitance should

however not become too high, because then it will significantly impact the output power capabilities of the system. Therefore, the maximum output capacitance will be set at 300 pF.
For example, the Infineon BSC220N20NSFD [46] has a on-resistance of 22 $m\Omega$, but a output capacitance of 279 pF, while the Infineon IMZ120R030M1H [47], which is used in the inverter that is used in this system, has a larger on-resistance of 30 $m\Omega$, but a lower output capacitance at 116 pF. In this case the former would be the more efficient, while the latter has a higher maximum output power. The selected MOSFETs can be used in both the Inverter and in the Active Rectifier Sect. 5.2.1.

5.2. Rectifier

5.2.1. Active and passive topologies

The rectifier can be passive or active. With a passive rectifier, the rectification from AC to DC is very efficient, but there is no control over the output power. It also is a very simple design. This means a passive rectifier is less prone to errors or defects. By using an active rectifier, the output power can be controlled by a PWM signal. An active rectifier also needs smaller capacitors, which decreases the weight of the system [45], which is important in aviation applications, but also for EV's.

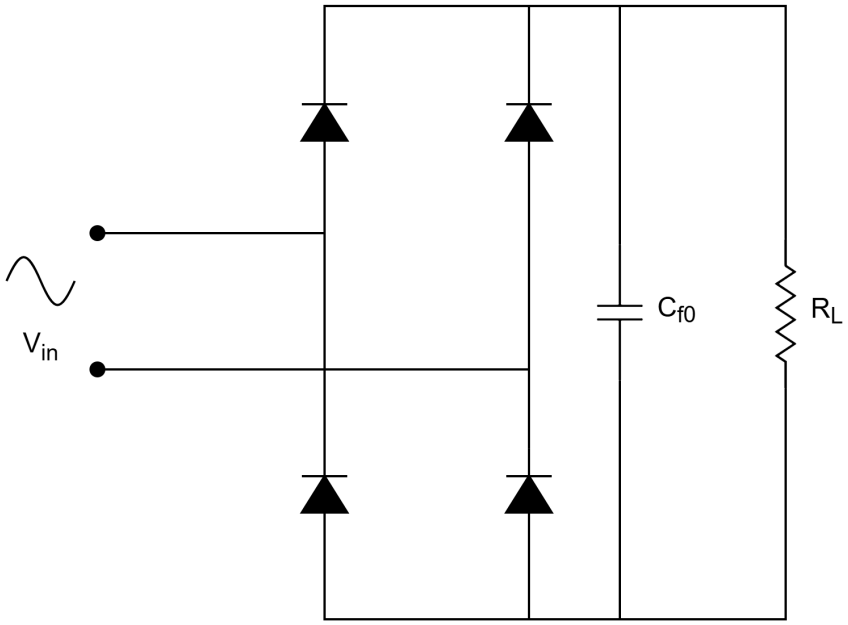


Figure 5.2: A full bridge passive rectifier

Since charging batteries effectively and efficiently is quite complicated, active control over the input of the battery is desirable [48]. An active rectifier can make sure it first uses Constant Current and later Constant Voltage, which can be used to charge the battery of the vehicle. By controlling on the receiver side, this information does not have to be transmitted to the transmitter side.
Using active rectification, impedance matching can be implemented [49], [50]. This allows for higher efficiency.
An active rectifier can also be more efficient than a passive rectifier, when using synchronous rectification. Unfortunately, this makes impedance matching impossible, but that problem can be solved by adding a DC/DC converter after the rectifier [51].
By using control for the power output due to misalignment and changing mutual inductance on the primary side, the different coils in the road can be used together and the computational load lies at the side where there is enough space and weight of the system is not an issue. The battery characteristics

and load matching can then be done in the vehicle, because it is complicated to send this information to the primary side.

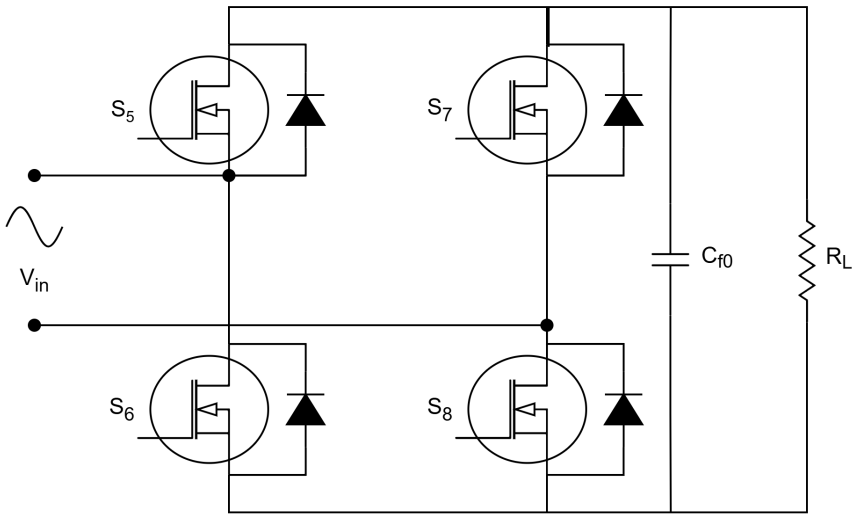


Figure 5.3: A full bridge active rectifier

5.2.2. Synchronization

If an active rectifier is used, there should be some kind of synchronization between transmitter and receiver, to ensure the rectifier operates correctly and the H-bridge is 'turned on' at the right moments to optimize the efficiency. Furthermore, the rectifier mostly uses a phase shifted version of the PWM signal of the inverter, because there is a phase difference between the primary and secondary side. By introducing a phase shift between the two control signals of the inverter and rectifier, the maximum efficiency is achieved. There are multiple ways to implement this phase shift [12].
The synchronization of the rectifier with the inverter is very complex, since there is no wired connection between the two. A wireless communication is very complicated to incorporate. A single microcontroller on the inverter's side that also sends a signal to the rectifier is therefore not feasible. The rectifier side will have to detect the waveform and generate its own signal based on that measurement.
[52] explains how this can be achieved. The zero crossings of the current of the secondary coil are sensed by adding a current sensor. This is fed into an opamp with hysteresis, which means its output switches between high and low with every zero crossing. This signal is fed into a microcontroller. This microcontroller uses this signal to synchronize a PWM signal that it generates for the rectifier.

6

Simulation

6.1. Overview

This section introduces the purpose of the simulations, the motivation for constructing two separate simulation environments, and how they relate to each other and to the overall project.

6.2. Simulation Objectives and Strategy

The primary objective of these simulations is to generate and validate the PWM signals that control the wireless power transfer system. Both models include an inverter stage to observe the resulting output waveforms corresponding to the generated PWM signals. Two simulation models were developed, each serving a distinct purpose and level of abstraction:

- **Simulation 1: Defined Output Model** - This model allows explicit definition of the desired inverter output waveform and computes the PWM signals required to produce it.
- **Simulation 2: Firmware-Based Model** - This model implements the actual phase-shift PWM control logic as used in the embedded firmware.

These simulations enable us to:

- Verify the inverter switching behavior and the controller's ability to generate the correct PWM signals and output waveforms.
- Compare the PWM signals and inverter outputs from both models to validate control logic consistency.
- Provide reference waveforms for code verification and hardware-in-the-loop testing.

6.3. Simulation 1: Defined Output Model

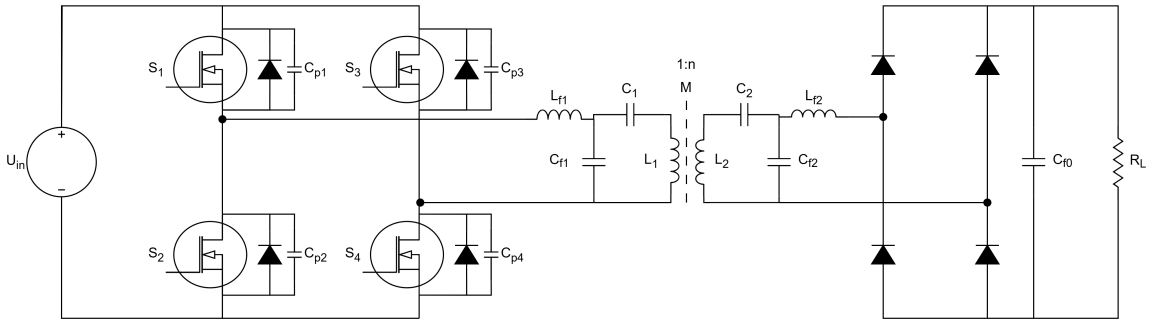


Figure 6.1: A model of the complete system.

6.3.1. Inverse PWM Signal Derivation

The critical component of this simulation is the generation of realistic gate-level switching signals (S1-S4) for the inverter MOSFETs. Instead of immediately generating PWM signals, we adopt a reverse-engineering approach: we start with the desired inverter output waveform, use it to determine predefined stage timings, and then compute the PWM gate signals necessary to reproduce that output. This allows us to verify whether the real-time control strategy Section 6.4 produces an output waveform that matches the intended behavior.

The 8-Stage PWM Structure The inverter operates using a fixed 8-stage switching cycle, derived from a phase-shifted square wave driving the full-bridge topology. Each stage defines a unique configuration of the four MOSFETs (S1-S4). The 8 stages form a full $85\,\mathrm{kHz}$ period (with mirrored symmetry around the midpoint), and their durations directly define the inverter's output waveform.

The following table shows the MOSFET logic states for each stage:

Table 6.1: MOSFET logic states (1 = ON, 0 = OFF) across one full switching cycle. Only stages 1 and 5 represent active conduction, others are transition (switching) states.

Stage	S1	S2	S3	S4	Type
1	1	0	1	0	Positive Conduction
2	1	0	0	0	Switching
3	1	1	0	0	Switching
4	0	1	0	0	Switching
5	0	1	0	1	Negative Conduction
6	0	0	0	1	Switching
7	0	0	1	1	Switching
8	0	0	1	0	Switching

Each of these stages corresponds to a distinct state of the H-bridge. The duration of each stage determines the effective average output voltage over one PWM cycle, and implements ZVS.

Complementary Signal Structure with Dead Time The gate-level signals for the MOSFETs can be grouped into complementary pairs: (S1, S4) and (S2, S3). Each pair is responsible for driving one half of the H-bridge. Within each pair, only one device is allowed to conduct at a time, and to ensure safe transitions and enable ZVS, dead times are inserted between switching. For the S1/S4 pair, dead time is implemented during stages 4 and 8, while for S2/S3, dead time occurs during stages 2 and 6 Fig. 6.2. As a result, the signals are not perfect logical inverses, but time-shifted complements with inserted off intervals.

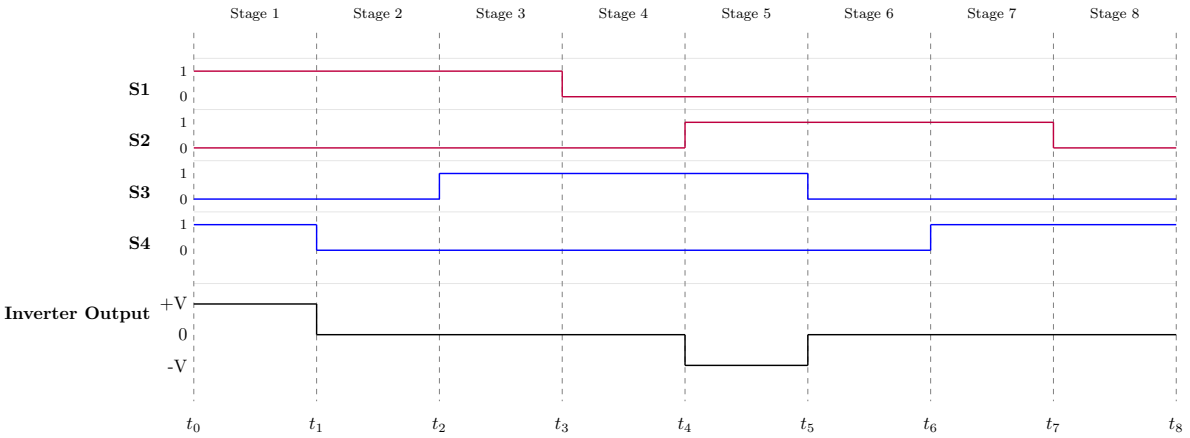


Figure 6.2: Timing diagram of the H-bridge switching signals and resulting inverter output.

Predefining Stage Timings Instead of computing switching points dynamically, we precompute the duration of each stage based on the desired inverter output voltage V_{ref}. This provides a clean ground truth for validation. The total PWM cycle is subdivided into:

- 2 conduction intervals (stage 1 and stage 5), which define the polarity and amplitude of the output voltage. Their width directly scales with V_{ref}, as seen in the conduction regions in Figure 6.2.
- 6 switching transitions (stages 2, 3, 4, 6, 7, 8), which symmetrically link the conduction intervals. Their durations are weighted and clamped to enforce soft switching (ZVS) and insert sufficient dead time. In Figure 6.2, these are the 6 (3, mirror symmetrical) intervals between the conduction phases.

Stage Timing Allocation With the total period T derived from the time-base clock (TBCLK) and switching frequency:

$$T = 2 \cdot \left\lfloor \frac{f_{\text{TBCLK}}}{f_{\text{PWM}}} \right\rfloor,$$

we define:

$$T_{\text{cond}} = d \cdot T, \quad T_{\text{sw}} = T - T_{\text{cond}}, \quad t_i = w_i \cdot T_{\text{sw}},$$

where w_i are normalized weights (e.g., $[1/3, 1/3, 1/3]$ by default) allocating the remaining switching time among the transition stages. These stage durations t_i are annotated in Figure 6.2, with clear boundaries between each switching event.

The conduction time T_{cond} is equally split between stages 1 and 5 and visualized as the wide high or low output regions in the graph. The switching time T_{sw} (shown as the gaps surrounding these conduction phases) is clamped by minimum dead time to guarantee safe operation and ZVS. Once the conduction time is fixed by V_{ref}, the remaining time is allocated to the transition stages using the chosen w_i weights.

This allocation creates a full 'stage schedule' over one PWM period, with durations that can be directly compared to the gate-level timing waveforms in Figure 6.2, enabling straightforward visual and algorithmic validation.

MOSFET Signal Generation Each simulation timestep queries the current system time t, converted to ticks:

$$\text{count} = \lfloor t \cdot f_{\text{TBCLK}} \rfloor \bmod T.$$

This value is compared against a cumulative list of stage boundaries to determine the active stage. The corresponding logic row from Table 6.1 then defines the gate signals for S1-S4 at that instant, which are shown in Figure 6.2.

Verification Strategy This reverse PWM process creates a reference signal that serves as a benchmark. Once the real-time control algorithm is introduced (see Section 6.4), its output waveform can be directly compared to this reverse-generated output. If both methods produce identical inverter outputs for the same V_{ref}, we confirm that our control logic and event sequencing work as intended.

Summary of Benefits This reverse-PWM approach:

- Allows direct control over inverter output shape and symmetry.
- Enables inverter control using arbitrary PWM waveforms, independent of the generation method.
- Simplifies debugging by isolating control logic from the power model.
- Enables waveform comparison for real-time control verification.

The code used to generate these signals can be found in Section A.3.1.

6.3.2. H-Bridge/Inverter Modeling

The inverter is modeled with 4 MOSFETs in an H-bridge configuration. The gate PWM signal is generated with code Section A.3. The output of the H-Bridge is connected to a Low-pass filter in parallel with the transmission coil with its compensation capacitor, making the DLCC circuit 3.0.4. But that is outside of the scope of this report Chapter 8.

6.3.3. Simulation Results and Analysis

The first key result is the generation of the MOSFET switching signals (S1-S4) across the full range of conduction widths, from 0 to 1. Figure 6.3 shows the signals generated at a conduction width of 50%. These waveforms clearly demonstrate the correct timing and complementary behavior of the MOSFETs, with the expected dead-time intervals visible between switching transitions.

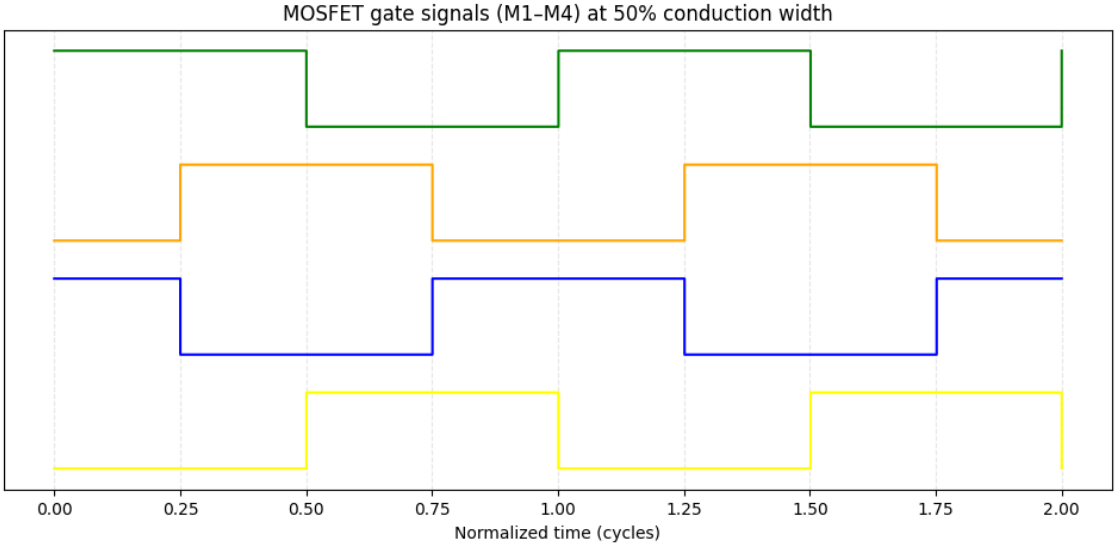


Figure 6.3: Simulation: MOSFET gate signals (M1–M4) at 50% conduction width, with no deadtime

This confirms that our code effectively controls the entire expected conduction width range, allowing precise tuning of the inverter output voltage. It is important to note that we use the term *conduction width* rather than duty cycle, as duty cycle traditionally refers to the PWM signal itself, whereas conduction width here describes the relative duration of the conduction stages in the switching cycle. Although the conduction width could be viewed as a form of duty cycle, we maintain this distinction to avoid confusion, since the inverter output waveform is not a simple PWM signal.

The second key result from the simulation is the relationship between the RMS voltage measured at the inverter output and the conduction width, shown in Figure 6.4. The measured RMS voltage closely follows the mathematically derived relationship:

$$V_{rms} = V_{in}\sqrt{d}$$

where $V_{in} = 100\,\mathrm{V}$ is the inverter input voltage and d is the normalized conduction width.

This agreement confirms the accuracy of our PWM signal generation code, which produces the switching signals for MOSFETs S1-S4. The inverter model used in the simulation includes detailed MOSFET characteristics, switching delays, and parasitic elements, ensuring a realistic representation of the inverter's electrical behavior.

The smooth square-root dependence of the output RMS voltage on conduction width demonstrates that the stage timing allocation and switching control logic effectively replicate the expected theoretical output. This validates both the signal generation method and the inverter model's accuracy.

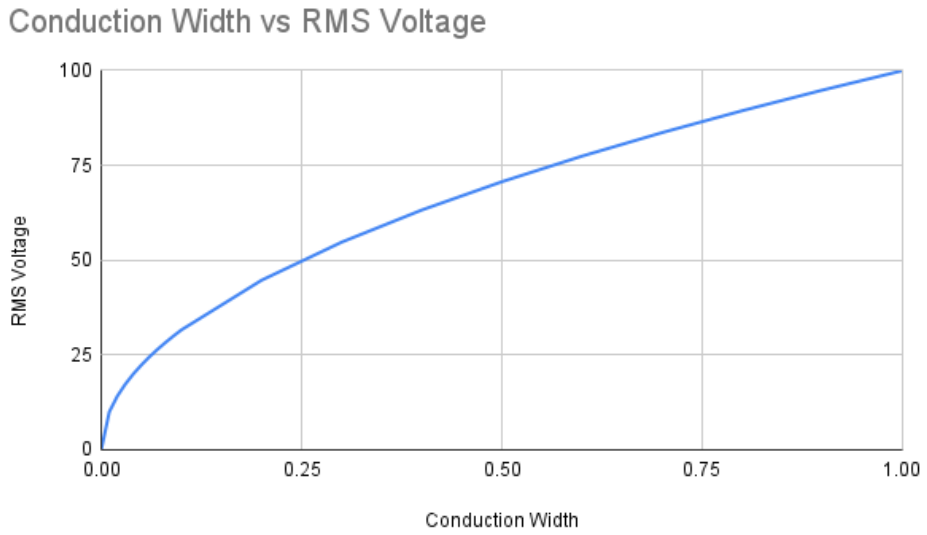


Figure 6.4: Simulation: RMS voltage measured at inverter output vs Conduction Width

6.4. Simulation 2: Firmware-Based Model

In an ideal implementation, the gate signals (S1–S4 from the first simulation) would be generated directly from the LaunchPad and sent to the MOSFET gate drivers. However, due to the complexity and computational demands of the full Simulink model used in Simulation 1, running this code in real-time on the LaunchPad is not feasible. This necessitated the creation of a second, simplified simulation model tailored for embedded execution (although a precomputed look-up table was also considered).

This firmware-oriented model implements the core switching logic using a phase-shift control approach, designed to be compatible with the LaunchPad's hardware constraints. Crucially, this model does not output gate signals directly. Instead, it configures and controls the LaunchPad's onboard ePWM (enhanced PWM) modules, which are responsible for generating the actual PWM waveforms. The model interacts with the ePWM hardware registers to define timing, phase shifts, and duty cycles in real-time.

To ensure that the phase-shift control was implemented correctly, we compared the output gate signals produced by the ePWM modules (simulated in Simulink) with the ideal waveforms from Simulation 1. This verification confirmed that the simplified firmware model accurately reproduces the intended switching behavior and can be deployed to the LaunchPad for real-world testing.

6.4.1. PWM Generation via Phase-Shift Control

Unlike Simulation 1, which outputs idealized S1–S4 gate signals directly, the firmware-based model implements the switching behavior by configuring the TI F28379D LaunchPad's ePWM modules. In-

stead of manually generating gate signal waveforms in code, the model programs hardware parameters such as counter modes, compare registers, phase offsets, and dead-time insertion. These parameters govern the internal PWM waveform generation autonomously.

Two ePWM modules are used—one per inverter leg—operating in up-down count mode to produce complementary PWM outputs. The key control input is the phase offset between these modules, set via the TBPHS (Time-Base Phase) register. Adjusting this phase shift controls the power flow by modulating conduction overlap, effectively reproducing the switching behavior targeted in Simulation 1.

By offloading waveform generation to the LaunchPad's dedicated ePWM peripherals, the model reflects real embedded constraints and allows direct deployment to hardware. The firmware interacts with these modules through register-level commands generated by Simulink's Embedded Coder, bridging simulation and embedded implementation.

This architecture shifts the responsibility for waveform generation from the simulation code to the LaunchPad's embedded peripherals, aligning the model more closely with how the real system operates and making it deployable to hardware.

The following subsection details the functionality of the TI F28379D LaunchPad's ePWM module relevant to this control strategy, providing insight into how hardware PWM generation is leveraged in the firmware model.

6.4.2. TI F28379D LaunchPad's EPWM module

The TI F28379D LaunchPad features multiple enhanced PWM (ePWM) modules designed for flexible and precise waveform generation, critical for power electronics applications like inverter control. Each ePWM module operates largely independently, with dedicated hardware for timing, output generation, and dead-time insertion.

At a high level, the ePWM module uses a time-base counter that can count up, down, or both (up-down mode, used in this implementation). This counter sets the fundamental timing for the PWM waveform. The module compares the counter value against programmable compare registers (CMPA and CMPB), which determine when the output toggles, thus controlling the PWM duty cycle, as can be seen in Fig. 6.5.

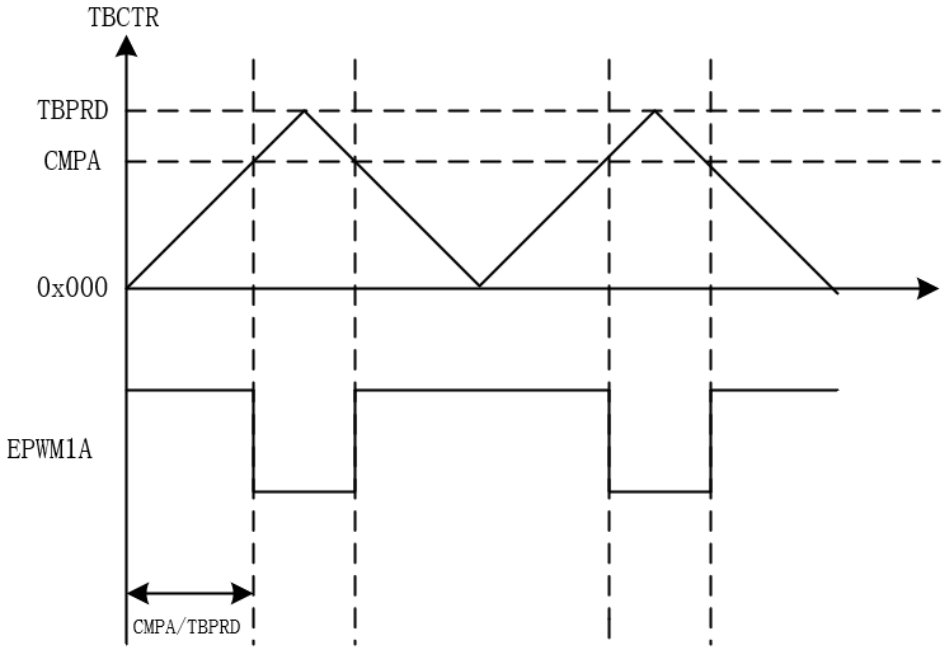


Figure 6.5: PWM generation in ePWM module in up-down mode

Key to our implementation is the phase-shift capability. The TBPHS (Time-Base Phase) register

introduces a phase offset to the counter start of a given ePWM module relative to others. By adjusting TBPHS values between modules, the system can create precise phase-shifted PWM signals, which is central to controlling power flow in the inverter.

Additionally, the ePWM module provides hardware-managed dead-band insertion to prevent shoot-through by delaying switching between high-side and low-side MOSFETs. This relieves the firmware from managing critical timing at nanosecond scales and improves reliability.

Outputs from the ePWM module are complementary pairs, with configurable polarity and synchronization options. This hardware-level control enables efficient, low-latency generation of the complex switching patterns required.

Overall, the ePWM module's combination of flexible timing control, phase shift, and dead-time insertion forms the backbone of the firmware-based PWM generation approach, allowing us to implement phase-shift control efficiently on the LaunchPad hardware.

6.4.3. Simulink/Embedded Code Integration

In this firmware-based model, the input reference voltage V_{ref} is used solely to derive the phase shift between the inverter legs. The duty cycle is ideally fixed at 50%, but the actual effective duty cycle is slightly reduced due to the preset dead-time configured separately to ensure safe switching transitions.

The Simulink model computes the **phase offset** from V_{ref}, which controls the relative timing between the two ePWM modules and thus the power transfer by adjusting conduction overlap.

This phase offset is written to the LaunchPad's ePWM TBPHS (Time-Base Phase) register to dynamically update the switching phase. The duty cycle remains fixed within the ePWM modules, and dead-time insertion is managed by hardware using a constant, predefined value.

The embedded code generated by Simulink's Embedded Coder integrates these calculations and register writes, enabling real-time updates of phase shifts based on changing V_{ref}, while the dead-time setting remains unchanged during operation.

The code used to generate these results, which was the firmware running on the launchpad can be found in Section A.3.2.

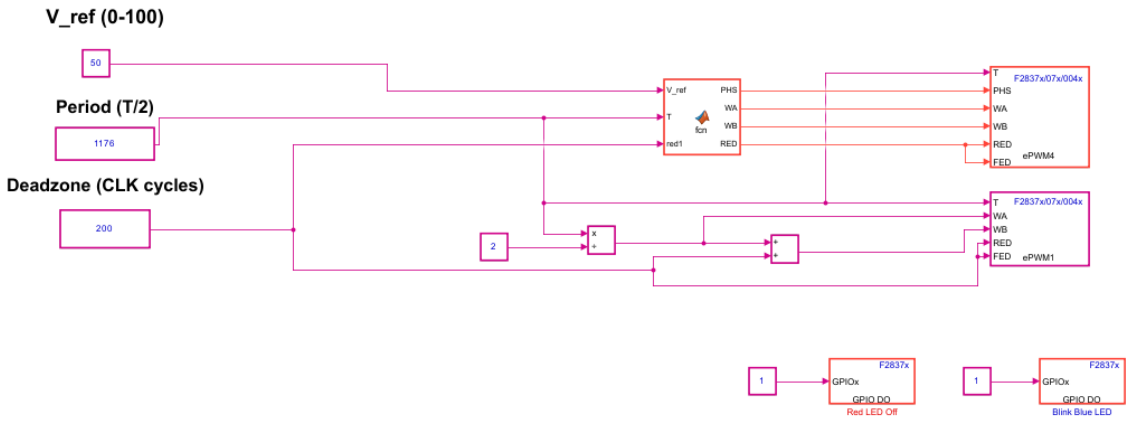


Figure 6.6: Simulink model configured for deployment on the TI F28379D LaunchPad.

6.4.4. Comparison to Simulation 1

The goal is to compare the S1–S4 gate signals generated by Simulation 2's ePWM blocks with the idealized gate signals from Simulation 1. Simulation 1 produced explicit, idealized gate signals (S1–S4) via direct logic, enabling rapid testing of phase-shift control concepts without hardware constraints. Simulation 2, however, generates these signals indirectly by configuring the LaunchPad's ePWM modules to produce phase-shifted PWM outputs in hardware.

To validate the firmware model, S1–S4 waveforms from both simulations were compared under matching conditions—phase shift, switching frequency, and dead-time. The alignment of pulse timing, widths, and phase confirmed that the ePWM-based signal generation accurately replicates the ideal logic outputs from Simulation 1.

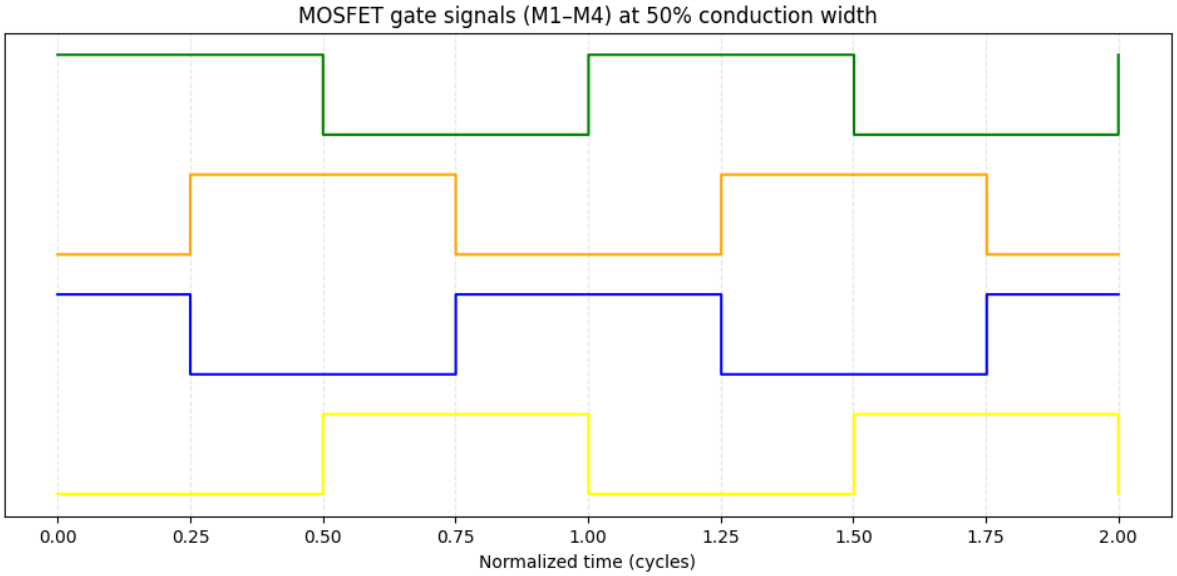


Figure 6.7: PWM signal generated by Simulation 1 with a Conduction Width of 0.5 and a deadtime of 20 ticks

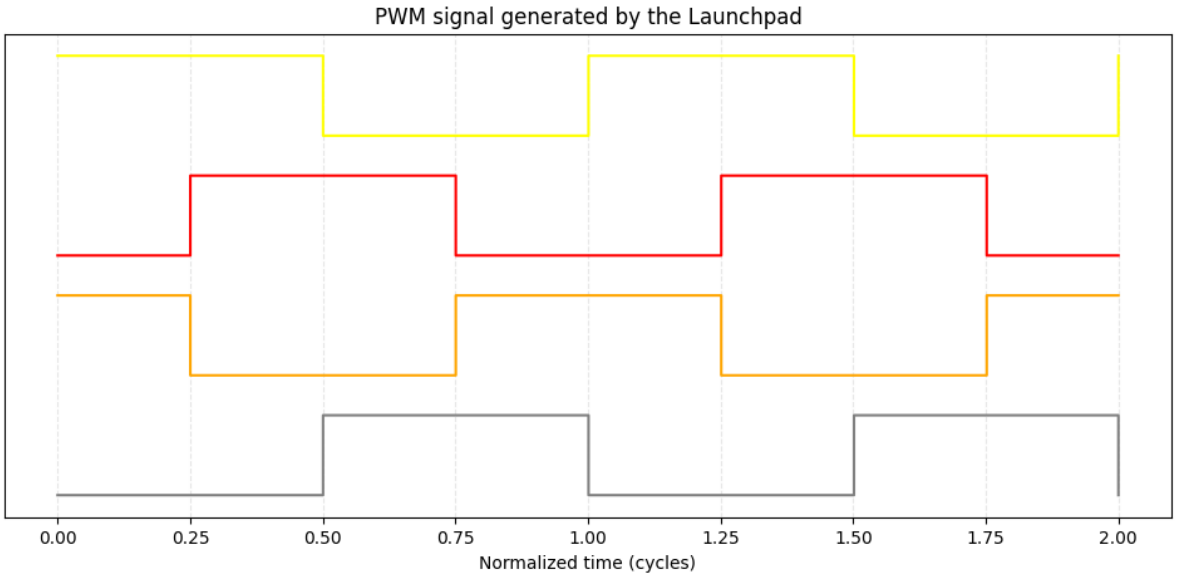


Figure 6.8: PWM signal generated by the Launchpad running Simulation 2's software

Visually, the two figures demonstrate a perfect match in timing and waveform structure. Figure 6.7 shows the ideal gate signals generated in Simulation 1, while Figure 6.8 presents the signals measured from the LaunchPad running Simulation 2's ePWM-based control. Both sets of waveforms clearly exhibit identical pulse widths, dead-times, and relative phase shifts, confirming that the hardware output mirrors the simulated logic. This visual agreement is further supported by numerical comparisons under different test conditions—such as varying conduction widths and phase shifts—which also showed consistent alignment between the two simulations.

This close agreement validates the embedded model's correctness, justifying its deployment to real hardware and confirming that the core phase-shift control logic was preserved despite transitioning from logic-based simulation to hardware-timed PWM generation.

7

Testing

To verify the theoretical and simulated results, two tests will be performed. The test will investigate within which output range of the conduction width the converter can be controlled and the output power of the inverter. In this chapter, the test plan and test setup will be explained. The results of the testing will be presented at the end of this chapter.

7.1. Testplan

The goal of the test is to validate the ability to generate a desired PWM signal based on a given reference voltage. This will be achieved by measuring the output signal of the inverter for several predetermined reference voltages. These signals will be analysed afterwards to confirm correct signal generation. This would confirm the converter sub-group's ability to integrate with the control sub-group [10], allowing them to continue testing within the lab with the converter group's sub-component, which would also give the converter's group 'real world' test data. The following measurements will be done:

- Control over full range of the output voltage.
- Current over the full range of the output.

7.2. Equipment used

7.2.1. The system

Microcontroller The TI F28379D LaunchPad is a microcontroller development board based on the TMS320F28379D, a dual-core Delfino series digital signal controller (DSC) from Texas Instruments. It is specifically designed for high-performance real-time control applications such as motor control, power conversion, and industrial automation [53]. In this system, the LaunchPad is used to generate the PWM signals that control the inverter. Its high-resolution PWM (HRPWM) modules allow for precise signal control, which is essential for accurate power transfer and implementing advanced PWM strategies and functions such as ZVS. Its fast computation capabilities make it ideal for closed-loop control and implementing future extensions such as coil alignment adjustment.

Inverter A heavy duty inverter Figure 7.1 will be used outside and in the ESP lab. This inverter is capable of delivering 20 kW to a load, but it will be tested in much lower power conditions.

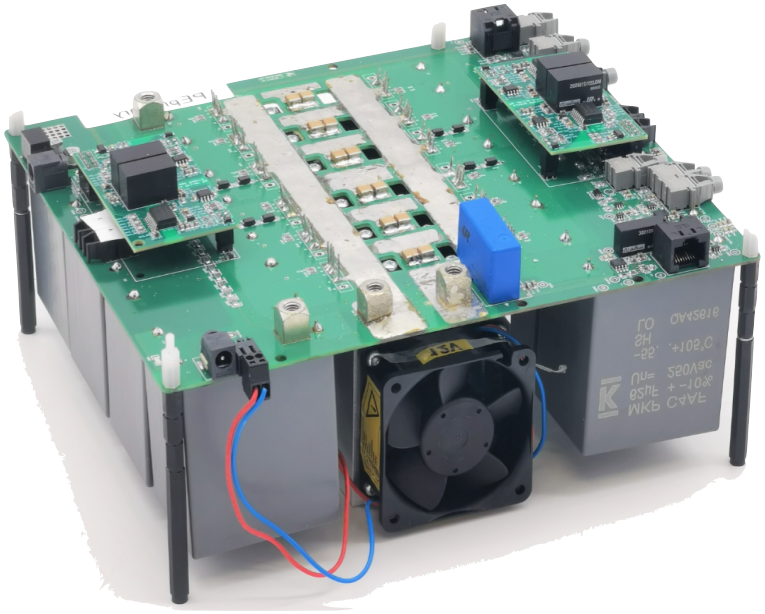


Figure 7.1: The high power inverter used for testing

Load A resistive load of 22.8 Ω will be used to test if the output is correct. In the ESP lab the load is the complete system, with compensation circuits, transmit and receiver coils, rectifier and a resistive load. That load is 50 Ω.

Power supply A simple, low power, power supply is used outside the ESP lab. This will provide a DC voltage of 30 V, which is enough to test the working of the inverter. In the ESP lab a larger power supply is used, but it is still tested at 30 V.

7.2.2. Measuring instruments

Oscilloscope A four channel oscilloscope is used to visualize the output signal, both voltage and current, of the inverter and the voltages over the MOSFETs.

Logic analyzer For plotting the PWM signals, a logic analyzer can be used. This device can measured up to 8 digital signals simultaneously, which makes it perfect for checking if the PWM signals are correct.

7.3. Test setup

In the first tests, the output pins of the microcontroller will be connected directly to the logic analyzer. In this way, it is possible to visualize the signals to test if the output is what is expected. When this is confirmed, the output of the inverter will be connected to a resitive load. The output will be measured with the oscilloscope. This way, it is possible to check if the form and conduction width of the output are in accordance with the expected values. Also, by plotting both the voltage and the current, the output power can be determined. In the ESP lab, the complete system will be connected to the inverter to check if there are no unexpected results, but the main measurements are done over the resistive load.

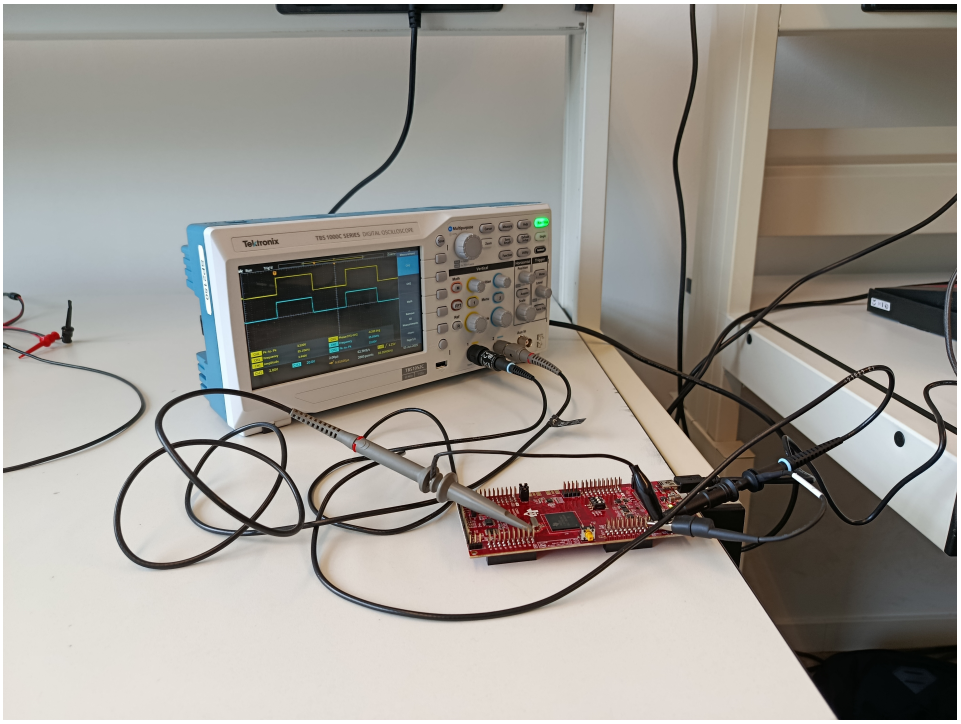


Figure 7.2: The test setup for testing the PWM output signals

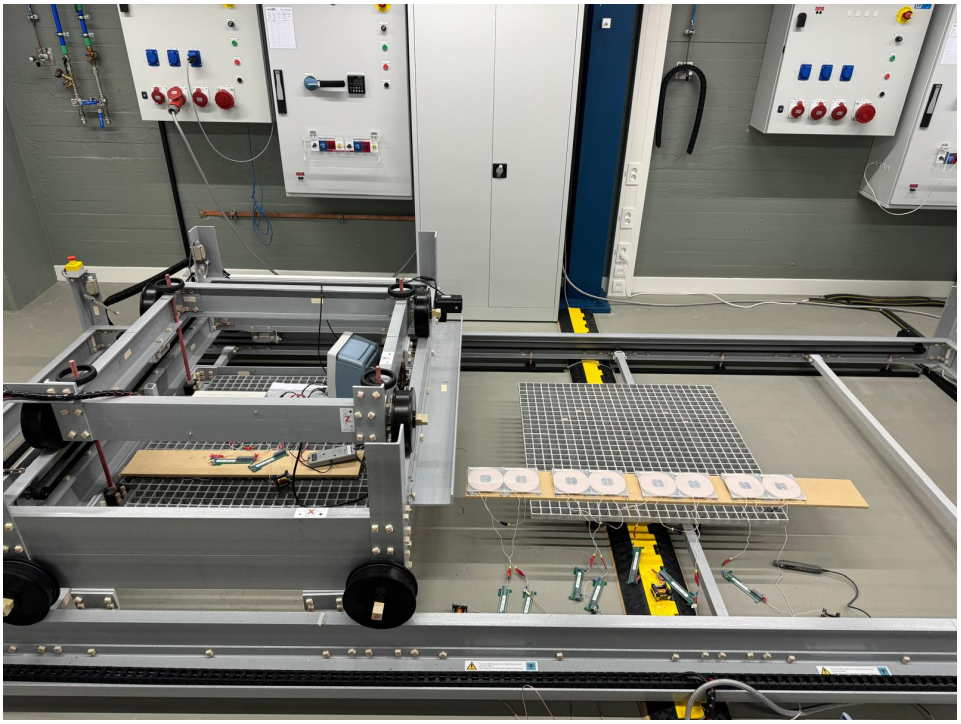


Figure 7.3: The complete system on the gantry with compensation circuits, coils and rectifier

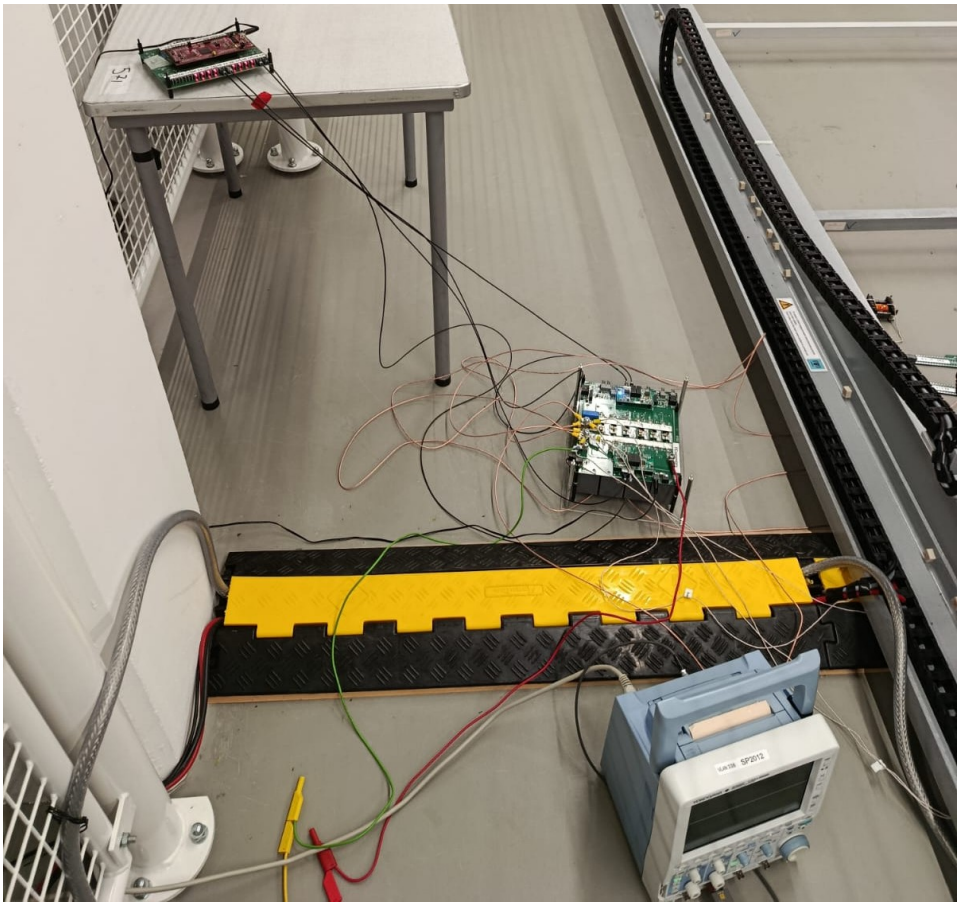


Figure 7.4: The launchpad and inverter, connected to the system in figure 7.3

7.4. Results

7.4.1. Control over full range of the output

As can be seen in figure 7.5, the output of the inverter can be controlled over a range between 8% and 92% of the maximum Conduction Width. The reason it was not possible to control a broader range, is that the gate signals for the MOSFETs had a very long turn on delay. It took around 450 ns from the time the gate signal was applied until the signal was at its maximum Fig. 7.8. Although the MOSFETs of course conduct when the gate voltage is around 4.5 V [47], it is important to establish a safety margin to ensure that the inverter is not shorted. This is around 4% of the total period, so for two switches per period, this means 8% of the time is not usable, because the MOSFETs are in the process of being switched on and off.

In Fig. 7.6, it can be seen that the output RMS voltage is very close to the theoretical value calculated in equation 4.2. That means the output RMS value of the voltage can indeed be accurately predicted by using that equation, which means the voltage can be controlled precisely.

In Fig. 7.7 the output voltage and transmit coil current are plotted when the complete system is connected and at maximum output power. The voltage and current are out of phase, as is expected, and the current is sinusoidal due to the compensation circuit. It was not the goal to measure the current through the transmit coil, but the current probe was connected incorrectly, so that is what was measured in the end.

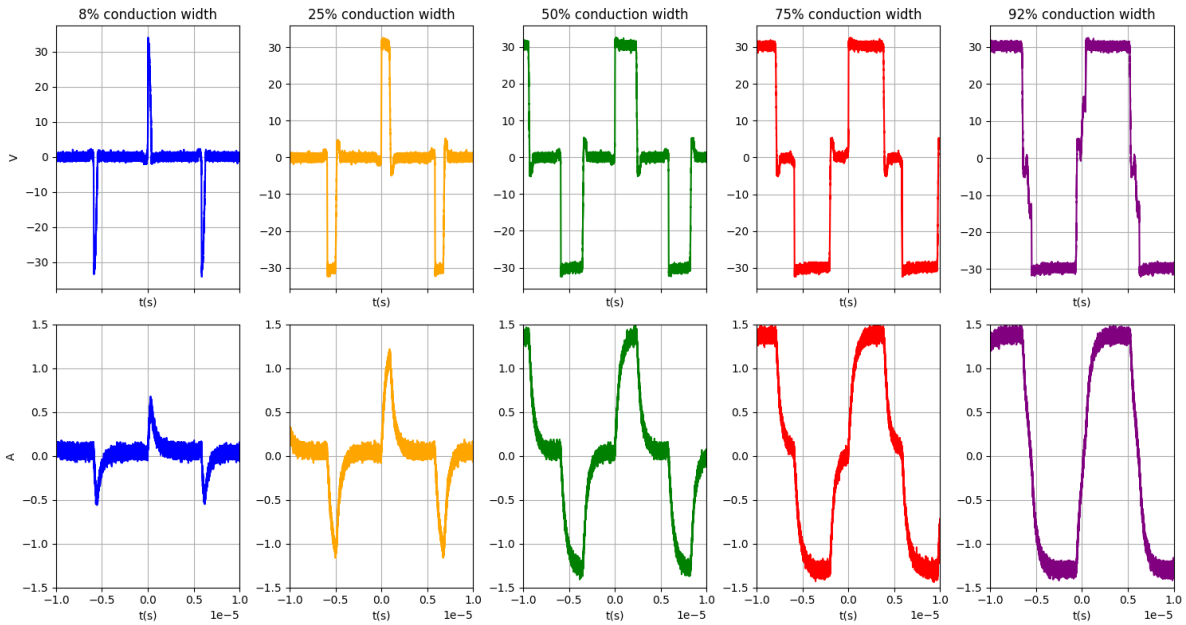


Figure 7.5: The output of the inverter over a resistive load for different conduction widths

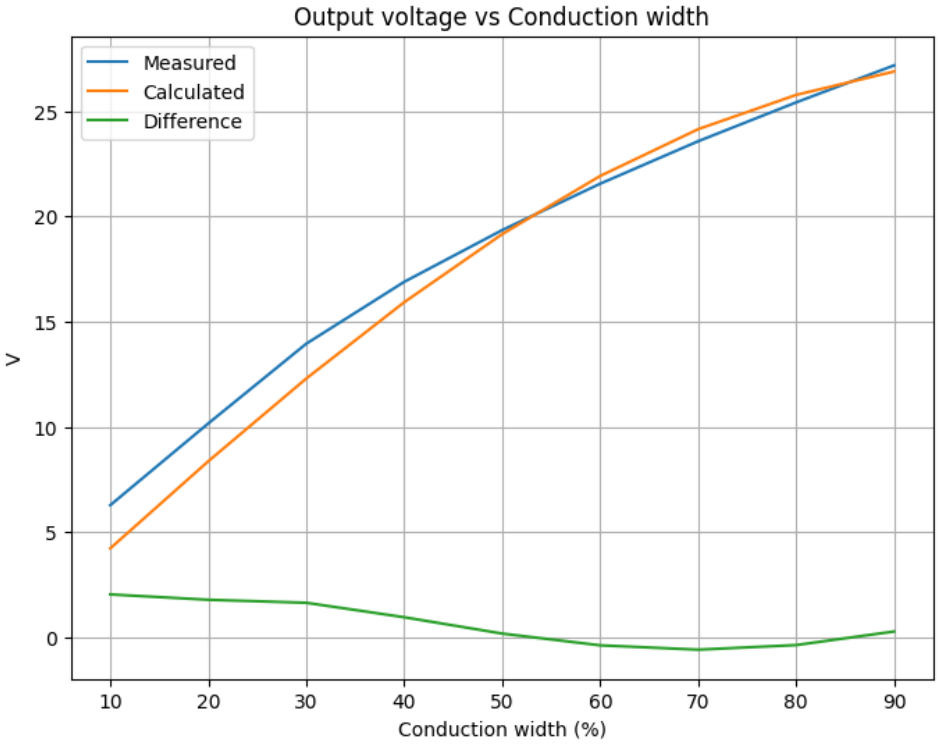


Figure 7.6: The output RMS voltages for different conduction widths compared to the calculated value

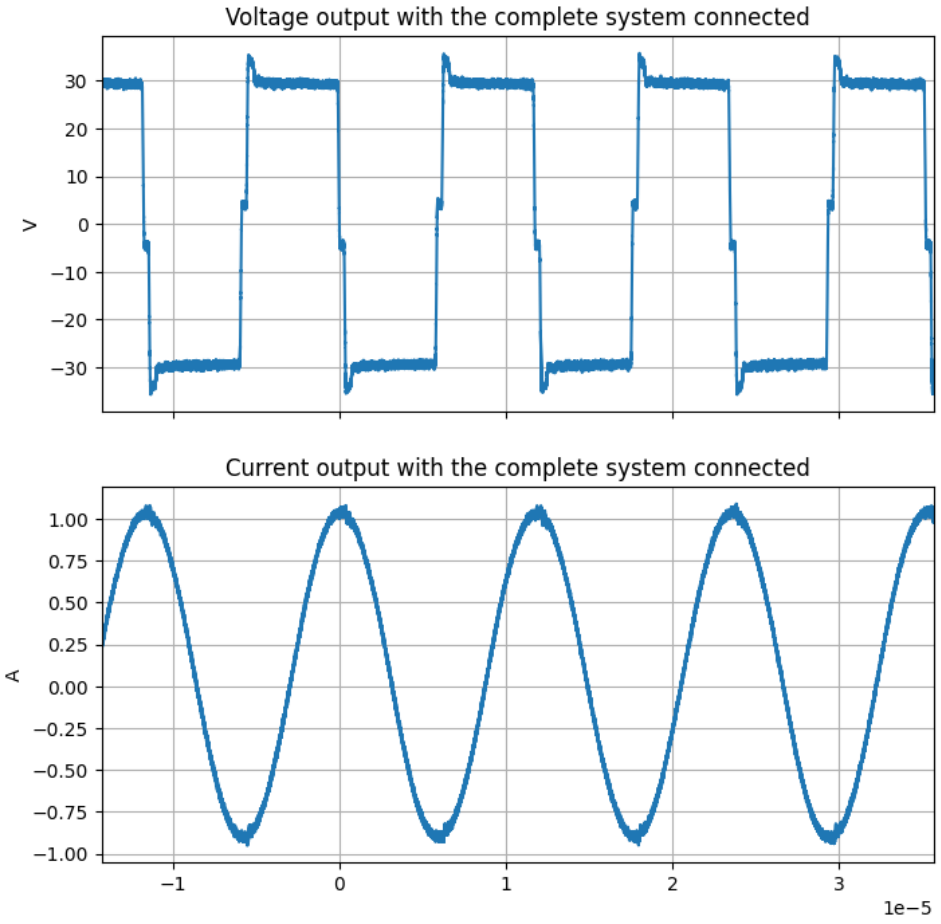


Figure 7.7: The output voltage and current with the complete system connected

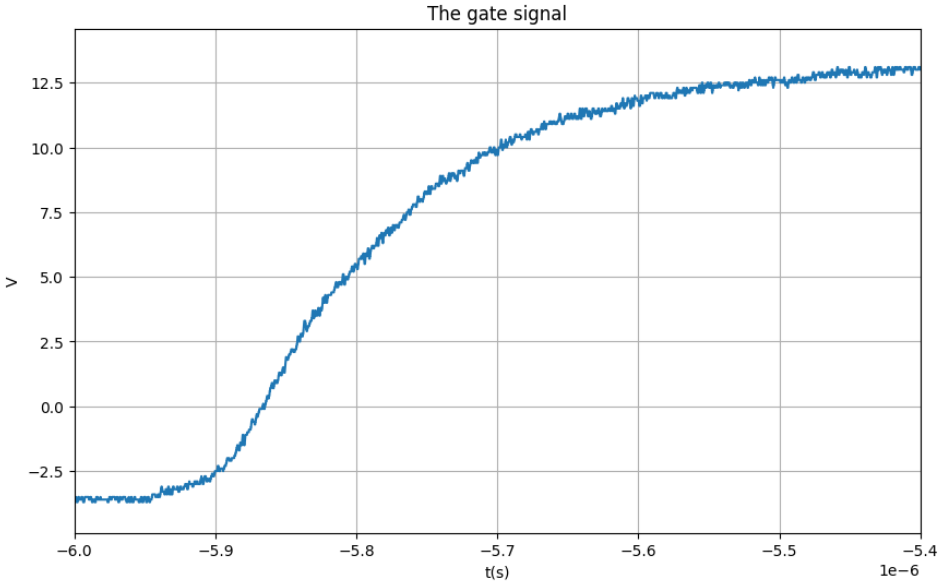


Figure 7.8: The gate signal takes around 450 ns to reach its maximum

7.4.2. The power output of the inverter

In figure 7.9, the power is plotted against the conduction width. It is clear that there is a linear relation between the output power and the conduction width. This is desired, because it makes control over the output power easier.

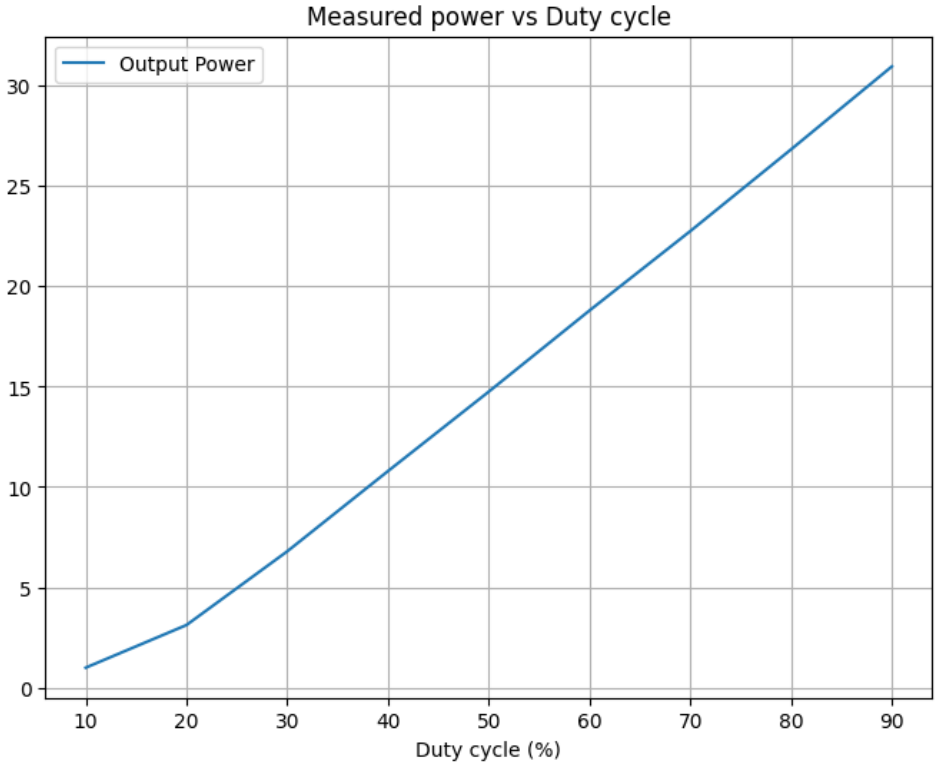


Figure 7.9: The input and output power in relation to the conduction width

It is not possible to say anything about the power output with the complete system connected, since the current that was measured is not the inverter output current.

8

Discussion

8.1. Mistakes

8.1.1. Unnecessary Simulation Beyond the Inverter Output

Initially, our subgroup operated under the assumption that the reference voltage V_{ref} to be obtained was measured downstream of the coils and the DLCC circuit. This led us to extend the simulation beyond the inverter output, including the full coil and resonant circuit models. However, it later became clear that V_{ref} was defined as the RMS voltage directly at the inverter output. Consequently, the additional simulation beyond the inverter was not required for the scope of this report.

While the extended simulations provided a useful sanity check and insight into the overall system behavior, they added unnecessary complexity and computational load and was thus not included in the final simulations or report. For more insight into this part of the system, see the sister reports of the Control and Coil subgroups [10], [11].

8.1.2. Phase Control Limitations in ePWM Module Code

A second limitation encountered was related to the control code driving the ePWM modules (see Appendix A.3.2 for the full code). We experienced difficulties achieving continuous phase control over the two complementary PWM signals. Specifically, the phase shift appeared to saturate at 180°, meaning that increasing the phase register (TBPHS) beyond half its maximum value had no further effect. The root cause of this behavior remains unclear.

To work around this issue, a hybrid control method was implemented:

- For phase shifts up to 180°, the intended code was used as designed.
- For phase shifts beyond 180°, the phase was clamped at 180°, and additional phase shift was achieved by adjusting the CMPA and CMPB compare values, accompanied by added deadtime to compensate for the altered timing effects caused by these changes.

This workaround allowed us to approximate full 360° phase control in practice, but it complicated the control logic. The implementation of this workaround can be found in Section A.3.2. Further investigation into the ePWM hardware or firmware behavior is recommended.

8.1.3. Input Power Measurement Uncertainty

During testing, the output power was measured directly and confidently. However, the input power was estimated using the voltage and current readings provided by the voltage source instrument. It later became apparent that these readings were flawed, as they indicated a scenario where the calculated input power was less than the measured output power; an inconsistency that suggests measurement error.

Because of this discrepancy, the input power data currently cannot be fully trusted for efficiency calculations and we are thus unable to provide a valid efficiency calculation at this time.

Another power measurement, the power of the output of the inverter with the complete system connected, failed because the current that was measured was not the correct one. This can be done better in future by checking if the connection of the probes is correct.

9 Conclusion

Despite our errors and mistakes, the system works as intended. It can handle 100 V, 10 A and uses 85 kHz as operating frequency. It uses zero voltage switching in its generation of the PWM signals, which are done on the launchpad, which uses a reference voltage to determine the duty cycle of the output signal. The efficiency can not be measured with certainty, but it is stable over the whole range.

9.1. Global system requirements

The global system requirements have all been achieved by using the test setup that was already built in the ESP lab.
The functional requirements were that the system should operate at 85 kHz and should be able to handle 100 V and 10 A and that a DC voltage should be converted to AC and rectified at the end Section 2.3. This has all been achieved.
The handling of 100 V and 10 A is achieved by the right selection of components for the inverter that is used and especially the MOSFETs used for the switching. This has been done in theory Section 5.1.1 and in practice, the inverter used for testing is rated for 50 kW, which is quite enough.
The operating frequency of 85 kHz has been achieved by programming the microcontroller to output control signals at that frequency.
The inversion and rectifying of the DC and AC voltages has been successfully achieved, which will be discussed in the next sections.

9.2. Generation of the signal

The signal had three requirements. These were implementation of Zero Voltage Switching, compatibility with the TI Launchpad and use of a reference voltage to control the inverter Section 2.3. This has also all been achieved.
The implementation of Zero Voltage Switching is done by using a phase shift PWM strategy. In that way, the output capacitance of all the MOSFETs can be discharged while never switching all MOSFETs off or shorting the inverter, while still having control over the duty cycle of the output wave.
Compatibility with the TI launchpad was guaranteed by testing and implementing everything on said device. By testing the output signals of the Launchpad and finding them satisfactory, it has been established the generation algorithm for the PWM signals is compatible with the TI Launchpad.
The use of a reference voltage to generate control the output of the inverter is has also been implemented by using the phase shift PWM strategy. By calculating the phase shift from the reference voltage, the PWM signals are controlled by the reference voltage that is fed to the algorithm.

9.3. Efficiency

The efficiency of the inverter should be 98% Section 2.3. It is not possible to confirm if this requirement is met from the measurements that have been performed. In hindsight is would not even be possible to confirm this even if the measurements had been done correctly. The measurement error that is

unavoidable is something in the range of 1-3%. Such an uncertainty could of course never confirm an efficiency of 98%, since the measurements would have to show 101% efficiency, which is impossible.

The efficiency was taken into account primarily in two parts of the design. Firstly selecting MOSFETs with a low on-resistance, the efficiency can be made as high as possible, especially in combination with the second part of the design, Zero Voltage Switching. By making sure the voltage is zero when switching the MOSFET on or off, the the switching losses are reduced significantly.
Unfortunately, the input power of the inverter was not measured accurately, so it can not be compared with the output power to calculate the efficiency. For the discussion about this aspect, see Section 8.1.3.

9.4. Future work

To expand on this project, more research could be done into implementing an active rectifier. By developing a way to synchronize that to the transmitter side the system as a whole could become more efficient with a lower power ripple, since there is control on both sides.

Another possible continuation of this work is to research if different MOSFETs or a different control scheme can improve the maximum and minimum output power. This way, the system will be more viable to use in a real world scenario.

A

Appendix

A.1. Hardware

- TI F28379D LaunchPad
- Logic analyzer (Sparkfun 24MHz/8-Channel)
- Custom TUDelft build Inverter

A.2. Software

- MATLAB
- SIMULINK
- Logic 2.0 (Saleae)

A.3. Code

A.3.1. Simulation 1: Defined Output Model

```
function [stage, M1, M2, M3, M4] = get_stage_and_mosfets(t, Vref)
%#codegen

    % ========== CONSTANTS ==========
    TBCLK_freq = 200e6;
    PWM_freq = 85e3;
    T = floor(TBCLK_freq / PWM_freq);  % Up-down count
    VDC = 100; % Supply voltage
    min_switch_frac = 0.1;  % Min switch duration as fraction of full
        period (0.1 = 10%)
    zvs_bias = [0.33 0.33 0.34]; % Equal bias for all stages, gets
        normalized later

    % ========== Compute Duty Cycle ==========
    arg = 1 - (pi * Vref) / (2 * VDC);
    arg = min(max(arg, -1), 1);  % Clamp acos domain
    d = (2/pi) * acos(arg);
    VREF_scaled = min(max(d * 100, 0), 100);  % Clamp output to 0-100%

    % ========== Calculate Tick Allocations ==========
    min_switch_ticks = round(min_switch_frac * T);
    zvs_bias = zvs_bias(:)' / sum(zvs_bias);  % Normalize bias
```

```
conduction_total_ticks = round((VREF_scaled / 100) * T);
conduction_each_ticks = floor(conduction_total_ticks / 2);

min_switch_total_ticks = 6 * min_switch_ticks;
leftover_switch_ticks = max(0, T - conduction_total_ticks -
   min_switch_total_ticks);

extra_switch_A_ticks = round(leftover_switch_ticks * zvs_bias);
extra_switch_B_ticks = fliplr(extra_switch_A_ticks);

p_ticks = zeros(1, 8);
p_ticks(1) = conduction_each_ticks;
p_ticks(5) = conduction_each_ticks;
p_ticks(2:4) = min_switch_ticks + extra_switch_A_ticks;
p_ticks(6:8) = min_switch_ticks + extra_switch_B_ticks;

% Fix rounding to exactly fill T ticks
total_assigned = sum(p_ticks);
diff = T - total_assigned;
if diff > 0
    % Add leftover ticks to the largest switching stage
    [~, idx] = max(p_ticks(2:4) + p_ticks(6:8));
    % idx in 2:4 corresponds to indices 2,3,4, if idx > 3 means 6:8
    % Adjust index accordingly:
    if idx <= 3
        p_ticks(idx + 1) = p_ticks(idx + 1) + diff;
    else
        p_ticks(3 + idx) = p_ticks(3 + idx) + diff; % idx>3 means
           index 6 or above
    end
elseif diff < 0
    % Remove excess ticks from conduction stages first
    to_remove = abs(diff);
    removable_1 = min(p_ticks(1), to_remove);
    p_ticks(1) = p_ticks(1) - removable_1;
    to_remove = to_remove - removable_1;

    removable_5 = min(p_ticks(5), to_remove);
    p_ticks(5) = p_ticks(5) - removable_5;
    to_remove = to_remove - removable_5;

    % If still negative, remove from smallest switching stages
    switch_indices = [2 3 4 6 7 8];
    while to_remove > 0
        [~, idx_min] = min(p_ticks(switch_indices));
        dec = min(p_ticks(switch_indices(idx_min)), to_remove);
        p_ticks(switch_indices(idx_min)) = p_ticks(switch_indices(
           idx_min)) - dec;
       to_remove = to_remove - dec;
    end
end

% ========== Compute Tick Edges ==========
tick_edges = zeros(1, 9);
for i = 2:9
    tick_edges(i) = tick_edges(i-1) + p_ticks(i-1);
```

```
    end

    % ========== Determine Current Stage ==========
    count = mod(floor(t * TBCLK_freq), T);
    stage = int8(8);
    for i = 1:8
        if count >= tick_edges(i) && count < tick_edges(i+1)
            stage = int8(i);
            break;
        end
    end

    % ========== MOSFET STATES ==========
    states = [
        1 1 1 0 0 0 0 0;
        0 0 1 1 1 0 0 0;
        1 0 0 0 0 0 1 1;
        0 0 0 0 1 1 1 0
    ];
    M1 = states(1, stage);
    M2 = states(2, stage);
    M3 = states(3, stage);
    M4 = states(4, stage);

end
```

A.3.2. Simulation 2: Firmware-Based Model

```
function [PHS, WA,WB,RED] = fcn(V_ref,  T, red1)
if V_ref == 50
    V_ref2 = 100 - V_ref

    V_ref_clamped = max(0, min(100,V_ref2));
    V_ref_scaled = V_ref_clamped;
    PHS2 = T*V_ref_scaled/100;

    PHS = max(1, min(T-1,PHS2+1));
    WA = T/2;
    WB = mod((WA + red1),T);
    RED = double(0+red1);
elseif V_ref > 50
    V_ref2 = 100 - V_ref

    V_ref_clamped = max(0, min(100,V_ref2));
    V_ref_scaled = V_ref_clamped;
    PHS2 = T*V_ref_scaled/100;

    PHS = max(1, min(T-1,PHS2));
    WA = T/2;
    WB = mod((WA + red1),T);
    RED = double(0+red1);
else
    PHS = uint16(T-1);
    V_ref2 = V_ref;

    V_ref_clamped = max(0, min(100,V_ref2));
```

```
    V_ref_scaled = V_ref_clamped;

    temp = T*V_ref_scaled/100;
    WA = uint16(mod((T/2 + temp),T));
    WB = uint16(mod((WA + red1),T));
    RED = double(mod(0 + 2 * temp + red1,T));
end
```

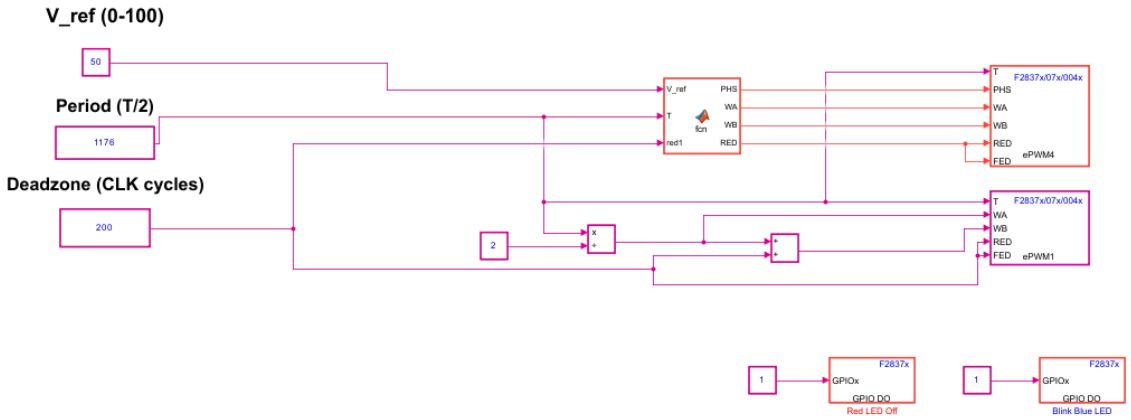


Figure A.1: Simulink model configured for deployment on the TI F28379D LaunchPad.

A.3.3. H-Bridge Simulator

```
function Vout = hbridge_sim(PWM1, PWM2, PWM3, PWM4)
    % Combine legs
    legA = PWM1 || PWM3;
    legB = PWM2 || PWM4;

    % Output voltage normalized to +1, 0 or -1
    % First 2 cases are non-physical, but are usefull for visually
       determining which of the 8 states the Inverter is in.
    % Set Vout = 0; for those 2 cases if you dont wish to use that
    if PWM1 && PWM3
        Vout = 0.1;
    elseif PWM2 && PWM4
        Vout = -0.1
    elseif legA && ~legB
        Vout = 1;
    elseif legB && ~legA
        Vout = -1;
    else
        Vout = 0; % both on or both off
    end
end
```

Bibliography

[1] J. Leijten, "Cijfer van de dag: 20 miljoen autos," *NRC*, May 2025. [Online]. Available: https://www.nrc.nl/nieuws/2025/05/14/cijfer-van-de-dag-20-miljoen-autos-a4893167.

[2] K. Li, J. Chen, X. Sun, G. Lei, Y. Cai, and L. Chen, "Application of wireless energy transmission technology in electric vehicles," *Renewable and Sustainable Energy Reviews*, vol. 184, p. 113 569, 2023. DOI: 10.1016/j.rser.2023.113569. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S1364032123004264.

[3] A. A. S. Mohamed, A. A. Shaier, H. Metwally, and S. I. Selem, "An overview of dynamic inductive charging for electric vehicles," *Energies*, vol. 15, no. 15, p. 5613, 2022. DOI: 10.3390/en15155613. [Online]. Available: https://doi.org/10.3390/en15155613.

[4] C. Panchal, S. Stegen, and J. Lu, "Review of static and dynamic wireless electric vehicle charging system," *Eng. Sci. Technol. Int. J.*, vol. 21, no. 5, pp. 922–937, Jun. 2018. DOI: 10.1016/j.jestch.2018.06.015. [Online]. Available: https://doi.org/10.1016/j.jestch.2018.06.015.

[5] C. Yang, "Running battery electric vehicles with extended range: Coupling cost and energy analysis," *Appl. Energy*, vol. 306, p. 118 116, Nov. 2021. DOI: 10.1016/j.apenergy.2021.118116. [Online]. Available: https://doi.org/10.1016/j.apenergy.2021.118116.

[6] J. Li, F. Wang, and Y. He, "Electric vehicle routing problem with battery swapping considering energy consumption and carbon emissions," *Sustainability*, vol. 12, no. 24, p. 10 537, 2020. DOI: 10.3390/su122410537. [Online]. Available: https://www.mdpi.com/2071-1050/12/24/10537.

[7] R. Bosshard, "Multi-objective optimization of inductive power transfer systems for ev charging," Ph.D. dissertation, ETH Zürich, 2015. DOI: 10.3929/ethz-a-010664107. [Online]. Available: https://www.research-collection.ethz.ch/handle/20.500.11850/117204.

[8] V. Cirimele, "Design and integration of a dynamic ipt system for automotive applications," Master's thesis, Politecnico di Torino, 2017.

[9] W. Shi, "Dynamic wireless charging of electric vehicles," *resolver.tudelft.nl*, 2023. DOI: 10.4233/c469a4fa-92bc-4ddf-9790-bd9f7a248815. [Online]. Available: https://doi.org/10.4233/c469a4fa-92bc-4ddf-9790-bd9f7a248815.

[10] N. W. v. Himbergen and S. Kort, *Control of dynamic wireless power transfer systems*, 2025.

[11] J. Diender and S. d. Jong, *Coil placement in dynamic wireless charging*, 2025.

[12] N. Hou and Y. W. Li, "Overview and comparison of modulation and control strategies for a nonresonant single-phase dual-active-bridge dc–dc converter," *IEEE Transactions on Power Electronics*, vol. 35, no. 3, pp. 3148–3172, Mar. 2020. DOI: 10.1109/tpel.2019.2927930.

[13] M. H. Malek, H. Kakigano, and K. Takaba, "Dual active bridge dc-dc converter with tunable dual pulse-width modulation for complete zero voltage switching operation," *IEEJ Journal of Industry Applications*, vol. 8, no. 1, pp. 98–107, Jan. 2019. DOI: 10.1541/ieejjia.8.98.

[14] J. Li, Q. Luo, D. Mou, Y. Wei, P. Sun, and X. Du, "A hybrid five-variable modulation scheme for dual-active-bridge converter with minimal rms current," *IEEE Transactions on Industrial Electronics*, vol. 69, no. 1, pp. 336–346, Jan. 2022. DOI: 10.1109/tie.2020.3048278.

[15] A. Mohan and A. Thosar, "Comparison of pwm based modulation techniques for dual active bridges," *2024 1st International Conference on Innovative Sustainable Technologies for Energy, Mechatronics, and Smart Systems (ISTEMS)*, pp. 1–6, Apr. 2024. DOI: 10.1109/istems60181.2024.10560207.

[16] E. C. d. Santos Jr and E. R. C. d. Silva, *Advanced Power Electronics Converters: PWM converters processing AC voltages*. John Wiley and Sons Inc, 2015.

[17] J. Everts, F. Krismer, J. Van den Keybus, J. Driesen, and J. W. Kolar, "Optimal zvs modulation of single-phase single-stage bidirectional dab ac–dc converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 3954–3970, Aug. 2014. DOI: 10.1109/tpel.2013.2292026.

[18] S. Guo, J. Su, J. Lai, and X. Yu, "Analysis and design of a wide-range soft-switching high-efficiency high-frequency-link inverter with dual-phase-shift modulation," *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 7805–7820, Sep. 2018. DOI: 10.1109/tpel.2017.2771765.

[19] J. Kan, S. Xie, Y. Wu, Y. Tang, Z. Yao, and R. Chen, "High-frequency-link inverter using combined synchronous rectifiers," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 12, pp. 6769–6777, Dec. 2014. DOI: 10.1109/tie.2014.2320233.

[20] J. Leon, R. Portillo, S. Vazquez, J. Padilla, L. Franquelo, and J. Carrasco, "Simple unified approach to develop a time-domain modulation strategy for single-phase multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 9, pp. 3239–3248, Sep. 2008. DOI: 10.1109/tie.2008.928141.

[21] J. Leon, S. Vazquez, A. Watson, L. Franquelo, P. Wheeler, and J. Carrasco, "Feed-forward space vector modulation for single-phase multilevel cascaded converters with any dc voltage ratio," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 2, pp. 315–325, Feb. 2009. DOI: 10.1109/tie.2008.926777.

[22] E. Monmasson, *Power Electronic Converters: PWM strategies and current Control Techniques*. Wiley, 2013.

[23] Z. Zeng, Z. Li, and S. M. Goetz, "A high performance interleaved discontinuous pwm strategy for two paralleled three-phase inverter," *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13 042–13 052, Dec. 2020. DOI: 10.1109/tpel.2020.2996903.

[24] W. Shi, J. Dong, T. B. Soeiro, J. Deng, C. Riekerk, and P. Bauer, "Continuous reduced-order dynamic model based on energy balancing for inductive power transfer systems," *IEEE Transactions on Power Electronics*, vol. 37, no. 8, pp. 9959–9971, Aug. 2022. DOI: 10.1109/tpel.2022.3153846.

[25] G. Zhu, J. Dong, W. Shi, T. B. Soeiro, J. Xu, and P. Bauer, "A mode-switching-based phase shift control for optimized efficiency and wide zvs operations in wireless power transfer systems," *IEEE Transactions on Power Electronics*, vol. 38, no. 4, pp. 5561–5575, Apr. 2023. DOI: 10.1109/tpel.2022.3231451.

[26] Y. Li, J. Hu, F. Chen, Z. Li, Z. He, and R. Mai, "Dual-phase-shift control scheme with current-stress and efficiency optimization for wireless power transfer systems," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 9, pp. 3110–3121, Sep. 2018. DOI: 10.1109/tcsi.2018.2817254.

[27] H. Li, J. Xu, F. Gao, Y. Zhang, X. Yang, and H. Tang, "Duty cycle control strategy for dual-side lcc resonant converter in wireless power transfer systems," *IEEE Transactions on Transportation Electrification*, vol. 8, no. 2, pp. 1944–1955, Jun. 2022. DOI: 10.1109/tte.2021.3123340.

[28] J. Jiang, S. Pan, J. Gong, F. Liu, X. Zha, and Y. Zhuang, "A leakage current eliminated and power oscillation suppressed single-phase single-stage nonisolated photovoltaic grid-tied inverter and its improved control strategy," *IEEE Transactions on Power Electronics*, vol. 36, no. 6, pp. 6738–6749, 2021. DOI: 10.1109/TPEL.2020.3035033.

[29] M. Chen, Z. Ye, Y. Chen, and D. Xu, "Zero-voltage-switching single-phase full-bridge inverter with active power decoupling," *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 571–582, 2021. DOI: 10.1109/TPEL.2020.2998640.

[30] P. Zuk and S. Havanur, *Zero-voltage switching full-bridge converter: Operation, fom, and guidelines for mosfet selection*, https://www.vishay.com/docs/90936/an847.pdf, Vishay Siliconix, Application Note AN847, Revision: 15-Dec-14, Document Number: 90936, 2014.

[31] Q. Zhu, L. Wang, Y. Guo, C. Liao, and F. Li, “Applying lcc compensation network to dynamic wireless ev charging system,” *IEEE Transactions on Industrial Electronics*, vol. 63, no. 10, pp. 6557–6567, Oct. 2016. DOI: 10.1109/tie.2016.2529561.

[32] X. Zhang, J. Li, and X. Tong, “A unique design approach of double-sided lcc compensated ipt system for misalignment-tolerant characteristic,” *IEEE Transactions on Power Electronics*, vol. 38, no. 1, pp. 1288–1300, Jan. 2023. DOI: 10.1109/tpel.2022.3200719.

[33] S. Cetin and V. Yenil, “Performance evaluation of constant current and constant voltage charge control modes of an inductive power transfer circuit with double-sided inductor-capacitor-capacitor and inductor-capacitor/series compensations for electrical vehicle battery charge applications,” *Transactions of the Institute of Measurement and Control*, vol. 43, no. 8, pp. 1710–1721, Jun. 2020. DOI: 10.1177/0142331220932438.

[34] S. Li, W. Li, J. Deng, T. D. Nguyen, and C. C. Mi, “A double-sided lcc compensation network and its tuning method for wireless power transfer,” *IEEE Transactions on Vehicular Technology*, vol. 64, no. 6, pp. 2261–2273, 2015. DOI: 10.1109/TVT.2014.2347006.

[35] S. Li, W. Li, J. Deng, T. D. Nguyen, and C. Mi, “A double-sided lcc compensation network and its tuning method for wireless power transfer,” *IEEE Transactions on Vehicular Technology*, vol. 64, pp. 2261–2273, Jun. 2015. DOI: 10.1109/TVT.2014.2347006.

[36] A. Abrishamifar, A. A. Ahmad, and M. Mohamadian, “Fixed switching frequency sliding mode control for single-phase unipolar inverters,” *IEEE Transactions on Power Electronics*, vol. 27, no. 5, pp. 2507–2514, May 2012. DOI: 10.1109/TPEL.2011.2175249.

[37] A. Namboodiri and H. S. Wani, “Unipolar and bipolar pwm inverter,” *International Journal for Innovative Research in Science and Technology (IJIRST)*, Dec. 2014, ISSN: 2349-6010.

[38] A. Sinha, K. Chandra Jana, and M. Kumar Das, “An inclusive review on different multi-level inverter topologies, their modulation and control strategies for a grid connected photo-voltaic system,” *Solar Energy*, vol. 170, pp. 633–657, 2018, ISSN: 0038-092X. DOI: https://doi.org/10.1016/j.solener.2018.06.001. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0038092X18305413.

[39] Monolithic Power Systems, Inc., *Pulse-width modulation techniques*, https://www.monolithicpower.com/en/learning/mpscholar/power-electronics/dc-ac-converters/pulse-width-modulation-techniques, Accessed: June 16, 2025.

[40] S. Urgun and H. Yigit, “Selective harmonic eliminated pulse width modulation (she-pwm) method using genetic algorithm in single-phase multilevel inverters,” *International Journal on Electrical Engineering and Informatics*, Mar. 2021, ISSN: 2085-6830.

[41] I.-O. Lee and G.-W. Moon, “Phase-shifted pwm converter with a wide zvs range and reduced circulating current,” *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 908–919, 2013. DOI: 10.1109/TPEL.2012.2205408.

[42] T. Mishima, C. Takami, and M. Nakaoka, “A new zvs phase-shifted high-frequency resonant inverter incorporating asymmetrical pwm-based unit control for induction heating,” in *IECON 2012-38th Annual Conference on IEEE Industrial Electronics Society*, IEEE, 2012, pp. 3256–3261. DOI: 10.1109/IECON.2012.6389377.

[43] J. Yang, X. Zhang, X. Yang, Q. Liu, and Y. Sun, “A hybrid compensation topology for battery charging system based on ipt technology,” *Energies*, vol. 12, no. 20, p. 3818, Oct. 2019. DOI: 10.3390/en12203818.

[44] Y. Chen, H. Zhang, N. Jin, *et al.*, “A unipolar-duty-cycle hybrid control strategy of series–series compensated ipt system for constant-current output and efficiency optimization,” *IEEE Transactions on Power Electronics*, vol. 37, no. 11, pp. 13 884–13 901, 2022. DOI: 10.1109/TPEL.2022.3173041.

[45] W. Santiago and A. Birchenough, “Single phase passive rectification versus active rectification applied to high power stirling engines,” in *3rd International Energy Conversion Engineering Conference*, 2006, p. 5687.

[46] *Mosfet optimostm3power-transistor,200v*, BSC220N20NSFD, Rev. 2.0, Infineon, 2018. [Online]. Available: https://4donline.ihs.com/images/VipMasterIC/IC/INFN/INFN-S-A0008943926/INFN-S-A0008943926-1.pdf?hkey=52A5661711E402568146F3353EA87419.

[47] *Coolsic™ 1200v sic trench mosfet silicon carbide mosfet*, IMZ120R030M1H, Rev. 2.2, Infineon, 2019. [Online]. Available: https://www.infineon.com/dgdl/Infineon-IMZ120R030M1H-DataSheet-v02_02-EN.pdf?fileId=5546d46269e1c019016a92fdcc776696.

[48] Y. Dou, Y. Liu, X. Huang, Z. Ouyang, and M. A. E. Andersen, "An active-rectification based communication free inductive power transfer for battery charging system with soft-switching capability," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 1627–1633. DOI: 10.1109/APEC39645.2020.9124058.

[49] F. Corti, A. Reatti, A. Nepote, *et al.*, "A secondary-side controlled electric vehicle wireless charger," *Energies*, vol. 13, no. 24, p. 6527, 2020. DOI: 10.3390/en13246527.

[50] A. Berger, M. Agostinelli, S. Vesti, J. A. Oliver, J. A. Cobos, and M. Huemer, "A wireless charging system applying phase-shift and amplitude control to maximize efficiency and extractable power," *IEEE Transactions on Power Electronics*, vol. 30, no. 11, pp. 6338–6348, 2015. DOI: 10.1109/TPEL.2015.2410216.

[51] D. Pehrman, Y. Liu, C. Cui, and X. Huang, "Loss reduction by synchronous rectification in a 50 kw sic-based inductive power transfer system," in *IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society*, 2020, pp. 3907–3912. DOI: 10.1109/IECON43393.2020.9254316.

[52] H. Dialani, J. Dong, G. Zhu, P. Bauera, and M. G. Niasar, "Highly efficient dual-side wireless power transfer: Implementation of synchronization and wireless communication," M.S. thesis, Delft University of Technology, 2023.

[53] T. Instruments, "Digital control of high-frequency switched-mode power converters using tms320c2000 real-time mcus," Texas Instruments, Tech. Rep. SPRACN0F, Mar. 2022. [Online]. Available: https://www.ti.com/lit/an/spracn0f/spracn0f.pdf.