Transactions Briefs

A Generalized Class of Dynamic Translinear Circuits

J. Mulder, W. A. Serdijn, A. C. van der Woerd, and A. H. M. van Roermund

***Abstract*—This brief proposes a generalization of the class of "dynamic translinear," or "exponential state-space," circuits. As an illustration of the proposed general class of dynamic translinear circuits, the brief describes the design of a second-order translinear filter that does not fit into the existing classification of exponential state-space filters. The externally linear behavior of the designed filter is demonstrated by means of simulations.**

***Index Terms*—Companding filters, translinear circuits.**

I. Introduction

In the area of analog continuous-time filters, the design of dynamic translinear (DTL) and log-domain circuits has become a definite (academic) trend [1]–[17]. Translinear (TL) filters were originally introduced by Adams in 1979 [1] and independently by Seevinck in 1990 [2]. The log-domain filters presented by Adams and Seevinck were first-order. The interest in TL filters really started to increase from 1993, when Frey published a synthesis method enabling the design of higher order log-domain filters. Furthermore, Frey recognized that log-domain filters only constitute a subset of a more general class of "exponential state-space" (ESS) filters [18], [19]. In particular, Frey described the subsets of tanh and sinh filters.

The aim of this brief is to show that the "general" class of ESS or DTL filters proposed in [18], [19] can be generalized even further. As an illustration, the brief describes the design of a second-order TL filter that does not fit into the framework suggested in [18], [19].

Section II first provides a short review of the static translinear (STL) and dynamic translinear principles. Next, Section III treats the generalization of the class of DTL and ESS circuits. The generalization is addressed both in terms of currents and in terms of voltages, as both the current-mode and the voltage-mode approach are used in the literature. A circuit design example is described in Section IV. Finally, Section V presents the conclusions.

II. Translinear Principles

Translinear circuits can be divided into two major groups: STL and DTL circuits. Static TL circuits realize static transfer functions, both linear and nonlinear; DTL circuits realize frequency-dependent (transfer) functions, i.e., differential equations (DEs). The underlying principles of STL and DTL circuits are reviewed in this section.

Manuscript received April 1998; revised April 2001. This paper was recommended by Associate Editor M. Banu.

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Publisher Item Identifier S 1057-7130(01)07781-3.

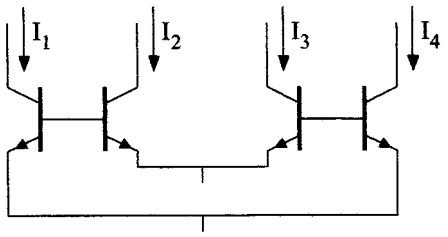

Fig. 1. A four-transistor translinear loop.

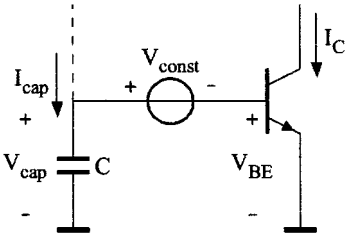

Fig. 2. Principle of dynamic translinear circuits.

A. Static Translinear Principle

Translinear circuits are based on the exponential relation between voltage and current, characteristic for the bipolar transistor and the MOS transistor in the weak inversion region. The STL principle applies to loops of semiconductor junctions. A TL loop is characterized by an even number of junctions [20], [21]. The number of devices with a clockwise orientation equals the number of counterclockwise-oriented devices. An example of a four-transistor TL loop is shown in Fig. 1. It is assumed that the transistors are somehow biased at the collector currents I_1 through I_4. When all devices operate at the same temperature, this yields the familiar representation of TL loops in terms of products of currents

$$I_1 I_3 = I_2 I_4. \tag{1}$$

This generic TL loop equation is the basis for a wide variety of static electronic functions, which are theoretically temperature and process independent.

B. Dynamic Translinear Principle

The DTL principle can be explained with reference to the subcircuit shown in Fig. 2. Using the current-mode approach, this circuit is characterized by the relation between the collector current $I_{\rm C}$ and the capacitance current $I_{\rm cap}$ flowing through the capacitance C. Note that the dc voltage source $V_{\rm const}$ does not affect $I_{\rm cap}$. The expression for $I_{\rm cap}$ is easily found to be given by [21], [22]

$$I_{\rm cap} = C U_T \frac{\dot{I}_{\rm C}}{I_{\rm C}} \tag{2}$$

where U_T is the thermal voltage and the dot represents differentiation with respect to time.

Equation (2) shows that $I_{\rm cap}$ is a nonlinear function of $I_{\rm C}$ and its time derivative $\dot{I}_{\rm C}$. A better understanding of (2) is obtained by slightly rewriting it as

$$C U_T \dot{I}_{\rm C} = I_{\rm cap} I_{\rm C}. \tag{3}$$

Equation (3) directly states the DTL principle: *A time derivative of a current can be mapped onto a product of currents*. Now, the product of currents on the right-hand side of (3) can be realized very elegantly by means of the STL principle. In other words, the implementation of (part of) a DE becomes equivalent to the implementation of a product of currents.

III. Generalization

The specific characteristics of each subset within the class of ESS filters (e.g., $\log$-domain, $\tanh$ and $\sinh$ filters) can be described either in terms of voltages [19] or in terms of currents [10], [23].

Using the voltage-mode approach, the capacitance *voltages* V_{C_i} are chosen to represent the memory of a filter circuit, where $i \in [1, \ldots, n]$, and n denotes the order of the filter. In DTL circuits, the capacitance voltages are *nonlinearly* related to the linear state variables x_i. For the class of ESS filters, the relations between the variables x_i and V_{C_i} are given by [19]

$$x_i = f_i\left(V_{C_i}\right) \tag{4}$$

where the functions f_i are transcendental and have to be strictly monotonic. Different subclasses of ESS filters result from different choices for the functions f_i. The functions proposed in literature are $\exp$, $\tanh$, and $\sinh$ [19]. The transcendental nature of these functions reveals the internally nonlinear behavior of ESS filters.

Alternatively, using the current-mode approach, the *currents* I_{x_i} are chosen to represent the state of a TL filter [10], [23]. The currents I_{x_i} are *linearly* related to the state variables x_i. The internally nonlinear behavior of DTL circuits is now revealed by the equations for the capacitance currents I_{C_i}. The current-mode equivalent of (4) is given by

$$I_{C_i} = g_i\left(I_{x_i}, \dot{I}_{x_i}\right). \tag{5}$$

Different choices for the nonlinear functions g_i result either in $\log$-domain, $\tanh$ or $\sinh$ filters. For example, note that (2) is a special case of (5). Obviously, there exists a very tight correspondence between the functions f_i and g_i.

In (5), each capacitance current I_{C_i} is a function of only *one* state current I_{x_i} and its first-order derivative. This restriction to a dependence on one state current only is not fundamental. Equation (5) can be generalized by allowing each capacitance current I_{C_i} to be a function of *all* state variables and their first-order derivatives, which are represented by the vectors $\vec{I}_x$ and $\dot{\vec{I}}_x$, respectively. This yields

$$I_{C_i} = g_i\left(\vec{I}_x, \dot{\vec{I}}_x\right). \tag{6}$$

Equation (6) constitutes a class of DTL circuits more general than the class of ESS filters proposed in [18], [19]. The voltage-mode equivalent of (6) is given by

$$x_i = f_i\left(\vec{V}_C\right) \tag{7}$$

where $\vec{V}_C$ is the vector of capacitance voltages V_{C_i}.

As an example, consider the definitions of two capacitance currents I_{C_1} and I_{C_2}, given by

$$I_{C_1} = CU_T\left(\frac{\dot{I}_x}{I_x} + \frac{\dot{I}_{\text{out}}}{I_{\text{out}}}\right) \tag{8}$$

$$I_{C_2} = CU_T\left(\frac{\dot{I}_x}{I_x} - \frac{\dot{I}_{\text{out}}}{I_{\text{out}}}\right) \tag{9}$$

where the currents I_x and I_{out} are (strictly positive) linear state variables. It is easily seen that (8) and (9) do not fit into the framework suggested by (5), as both I_{C_1} and I_{C_2} are functions of both state currents I_x and I_{out}.

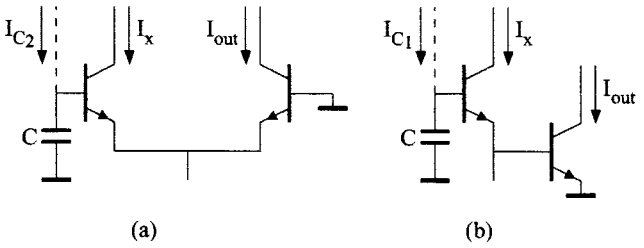

Fig. 3. Two capacitance current definitions.

The voltage-mode equivalents of (8) and (9) are given by

$$V_{C_1} = U_T \ln \frac{I_x I_{\text{out}}}{I_{\text{s}}^2} \tag{10}$$

$$V_{C_2} = U_T \ln \frac{I_x}{I_{\text{out}}} \tag{11}$$

where I_{s} is the saturation current of the bipolar transistor. Note that (10) and (11) do not fit into the general ESS framework of (4).

A possible implementation of (8) and (9) is depicted in Fig. 3(b) and (a), respectively. It is assumed that the transistors are somehow properly biased at the currents I_x and I_{out}. These subcircuits can be used as parts of a complete TL filter implementation.

IV. Design Example

As an illustration of the proposed generalization, we now describe the design of a second-order TL filter, based on (8) and (9). Starting with a suitable DE, the current-mode synthesis path of DTL circuits comprises the following design steps: definition of capacitance currents, translinear decomposition and hardware implementation [23].

A possible state-space description of a second-order Butterworth low-pass filter is given by

$$2CU_T\dot{I}_{\text{out}} = I_{\text{o}}(I_x - 2I_{\text{out}}) \tag{12a}$$

$$CU_T\dot{I}_x = I_{\text{o}}(I_{\text{in}} - I_{\text{out}}) \tag{12b}$$

where I_{o} is a dc current, I_{in} is the input current and I_{out} is the output current. The (linear) state variables are I_x and I_{out}. The filter cutoff frequency ω_c equals $I_{\text{o}}/(\sqrt{2}CU_T)$.

A. Definition of Capacitance Currents

The first step toward the TL implementation of (12a) and (12b) is the definition of two capacitance currents. These capacitance currents are used to implement the derivatives $\dot{I}_{\text{out}}$ and $\dot{I}_x$. We use (8) and (9) to obtain a circuit that is not a member of the class of ESS filters. These definitions are valid if I_x and I_{out} are class-A biased, i.e., if they are strictly positive. Assume that I_{in} contains a dc component $I_{\text{in,dc}}$. Then, as a result, I_{out} and I_x contain dc components equal to $I_{\text{in,dc}}$ and $2I_{\text{in,dc}}$, respectively. Consequently, for a sufficiently "small" ac signal swing ΔI_{in} of I_{in} (i.e., $|\Delta I_{\text{in}}| < I_{\text{in,dc}}$), I_{out} and I_x are strictly positive and can be implemented by collector currents (see Fig. 3).

Solving (8) and (9) for $\dot{I}_{\text{out}}$ and $\dot{I}_x$ and substitution in (12a) and (12b) yields two current-mode polynomials

$$I_{\text{out}}(I_{C_1} - I_{C_2}) = I_{\text{o}}(I_x - 2I_{\text{out}}) \tag{13a}$$

$$I_x(I_{C_1} + I_{C_2}) = 2I_{\text{o}}(I_{\text{in}} - I_{\text{out}}). \tag{13b}$$

B. Translinear Decomposition

To implement (13a) and (13b) using STL circuit techniques, suitable TL decompositions have to be derived, resulting in TL loop [21], [23]. In principle, many TL decompositions exist for (13a) and (13b). The

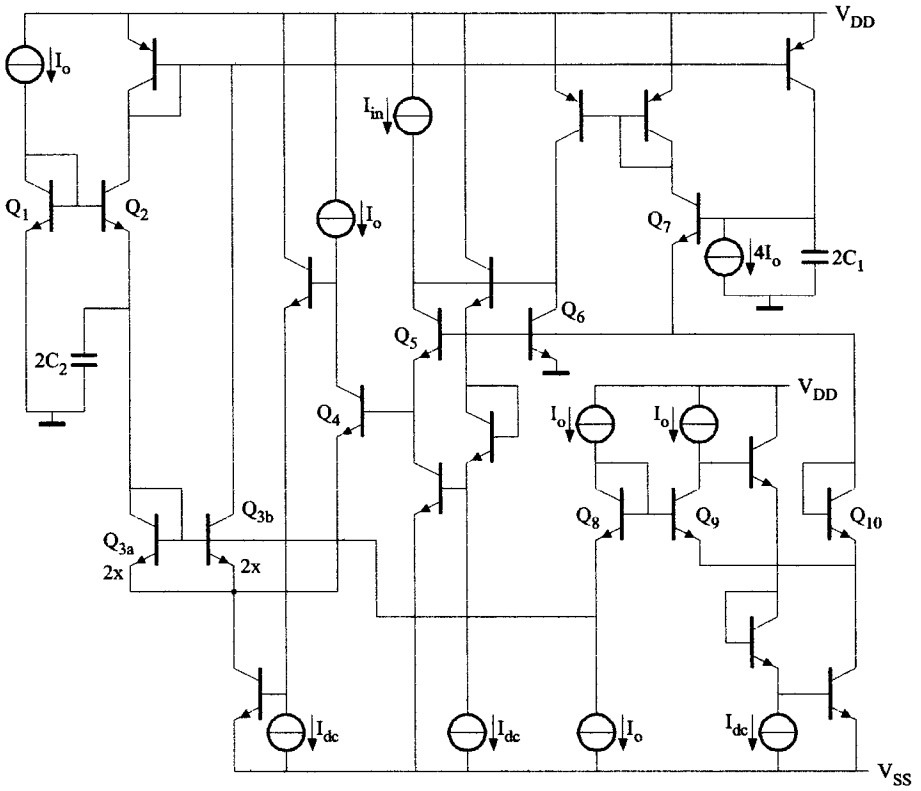

Fig. 4. A Butterworth second-order low-pass filter.

solution described below is only one of many possibilities and not necessarily the best or most simple one.

First, we derive a TL decomposition for (13a). Addition of a redundant term $2I_{\rm o}I_{\rm out}$ to both sides of (13a) directly yields a valid TL loop equation

$$I_{\rm out}(2I_{\rm o}+I_{C_1}-I_{C_2})=I_{\rm o}I_x. \tag{14a}$$

Note that all linear factors in (14a) are strictly positive. Hence, they can be mapped directly onto collector currents; compare Fig. 1 and (1).

A second TL decomposition, for (13b), can be derived by adding a term $2I_{\rm o}I_x$ to both sides of (13b). This yields

$$I_x(2I_{\rm o}+I_{C_1}+I_{C_2})=2I_{\rm o}(I_{\rm in}-I_{\rm out}+I_x). \tag{14b}$$

All factors in (14b) are again strictly positive making (14b) a valid TL loop equation.

C. Hardware Implementation

Next, (14a) and (14b) have to be mapped on TL loops and a proper biasing scheme has to be designed. This step requires quite a bit of heuristics and the implementation depicted in Fig. 4 is again only one of many possible implementations. The only aim here is to demonstrate the existence of a more general class of DTL circuits.

Equation (8) for I_{C_1} is implemented by Q_6, Q_7, and C_1. The collector currents of these two transistors are the state variables, i.e., $I_{{\rm C},Q_6}=I_{\rm out}$ and $I_{{\rm C},Q_7}=I_x$. Note that the loop Q_6–Q_7–C_1 is identical to the subcircuit shown in Fig. 3(b).

The second capacitance current is implemented in a different way. Combining (9) and (14a), an alternative expression for I_{C_2} is obtained

$$I_{C_2}=CU_T\frac{\dot I_{C_1}-\dot I_{C_2}}{2I_{\rm o}+I_{C_1}-I_{C_2}}. \tag{15}$$

Equation (15) is implemented by the loop Q_1–Q_2–C_2, where the collector current of Q_2 equals $I_{{\rm C},Q_2}=2I_{\rm o}+I_{C_1}-I_{C_2}$. Note that the dc bias current of Q_1, $I_{{\rm C},Q_1}=I_{\rm o}$, does not affect I_{C_2}; compare $V_{\rm const}$ shown in Fig. 2.

Translinear loop (14a) is implemented by transistors Q_6–Q_{10}–Q_9–Q_8–Q_2–Q_1, where $I_{{\rm C},Q_8}=I_{\rm o}$, $I_{{\rm C},Q_9}=I_{\rm o}$, and $I_{{\rm C},Q_{10}}=I_x$. The second TL loop, (14b), is not implemented directly. Instead, combining (14a) and (14b) results in an alternative second TL loop equation, given by

$$I_{\rm out}(2I_{\rm o}+I_{C_1}-I_{C_2})(2I_{\rm o}+I_{C_1}+I_{C_2})=2I_{\rm o}^2(I_{\rm in}-I_{\rm out}+I_x). \tag{16}$$

This third-order loop is implemented by transistors Q_1–Q_2–Q_3–Q_4–Q_5–Q_6, where $I_{{\rm C},Q_3}=2I_{\rm o}+I_{C_1}+I_{C_2}$, $I_{{\rm C},Q_4}=I_{\rm o}$, and $I_{{\rm C},Q_5}=I_{\rm in}-I_{\rm out}+I_x$. The factor 2 at the right-hand side of (16) is realized by the scale factor of Q_3. All unnumbered n-p-n transistors (and also Q_8 and Q_9) constitute simple level shifts and nullor implementations, required for biasing purposes. The p-n-p transistors implement a current mirror, which is also used for biasing the TL loops. Note that the subtraction of $I_{{\rm C},Q_2}$ and $I_{{\rm C},Q_{3a}}$ equals $2I_{C_2}$, and the addition of $I_{{\rm C},Q_2}$ and $I_{{\rm C},Q_{3b}}$, implemented by the p-n-p mirror, equals $2(2I_{\rm o}+I_{C_1})$.

The output current $I_{\rm out}$ of the filter is the collector current of Q_6. A copy of $I_{\rm out}$ can be obtained by connecting an additional n-p-n transistor in parallel with Q_6.

D. Simulation Results

Correct operation of the circuit was verified by means of simulations, using realistic transistor models. In the simulations, the dc current $I_{\rm dc}$ equals 0.5 μA. The supply voltages are $+2/-1.3$ V. Fig. 5 shows a transient simulation at 40 kHz. The amplitude of the input signal is 90% of $I_{{\rm in,dc}}$, which equals 1 μA. With $C=C_1=C_2=100$ pF, $U_T=26$ mV and $I_{\rm o}=1$ μA, ω_c equals 43.3 kHz.

Fig. 5 clearly shows that the relation between $I_{\rm in}$ and $I_{\rm out}$ is linear. Hence, the circuit is externally linear [24]. However, internally, the filter is strongly nonlinear, which is evidenced by the wave forms of

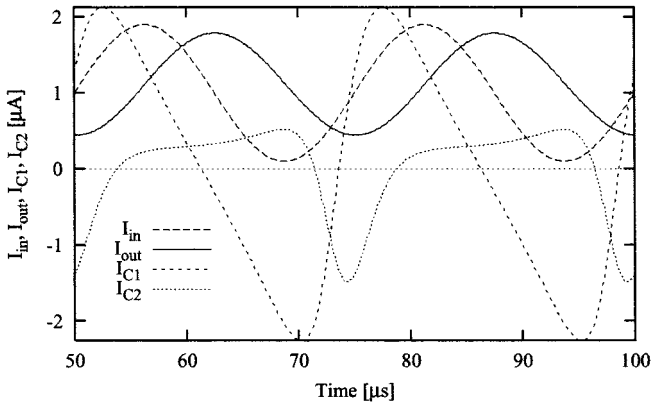

Fig. 5. Transient simulation of the Butterworth filter.

I_{C_1} and I_{C_2}. Internally nonlinear behavior is a general characteristic of companding filters [24].

V. Conclusion

This brief has described a class of dynamic translinear circuits, or exponential state-space circuits, that is more general than the existing classification found in literature. The proposed generalization has been articulated both in terms of voltages and in terms of currents. As an example, a second-order translinear filter has been designed, that fits only into the generalized class of dynamic translinear circuits.

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Active-R Design Using CFOA-Poles: New Resonators, Filters, and Oscillators

Abdhesh K. Singh and Raj Senani

***Abstract*—Recently, the active-R circuits utilizing the current feedback op–amps (CFOA)-pole have been shown to be superior alternatives to the active-R circuits designed using the compensation–poles of the traditional voltage-mode op-amps. The object of this brief, is to present some new CFOA-pole-based active-R circuits which employ a very small number of active and passive components, and yet, offer features which have not been attained simultaneously from any of the previously known active-R circuits using CFOA-poles such as, noninteracting controls of parameters, and the availability of the intended properties, in spite of the presence and consideration of all the parasitics (even other than those forming CFOA-pole). The workability of the proposed circuits has been confirmed by PSPICE simulations and hardware implementations based on AD844 type CFOAs.**

***Index Terms*—Active filters, active-R circuits, current feedback op-amps, gyrators, resonators, sinusoidal oscillators.**

I. Introduction

The transimpedance op–amps, popularly known as current feedback op–amps (CFOAs), are receiving growing attention as alternative building blocks for analog circuit design, because they offer several advantages over the traditional voltage–mode op–amps (VOAs). These advantages include, wider bandwidth (relatively independent of the closed loop gain), very high slew rates, and ease of realizing

Manuscript received December 1999; revised April 2001. This paper was recommended by Associate Editor M. Helfenstein.

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Publisher Item Identifier S 1057-7130(01)06234-6.