CMOS magnetic field sensor using a pick-up loop

for measuring electric currents

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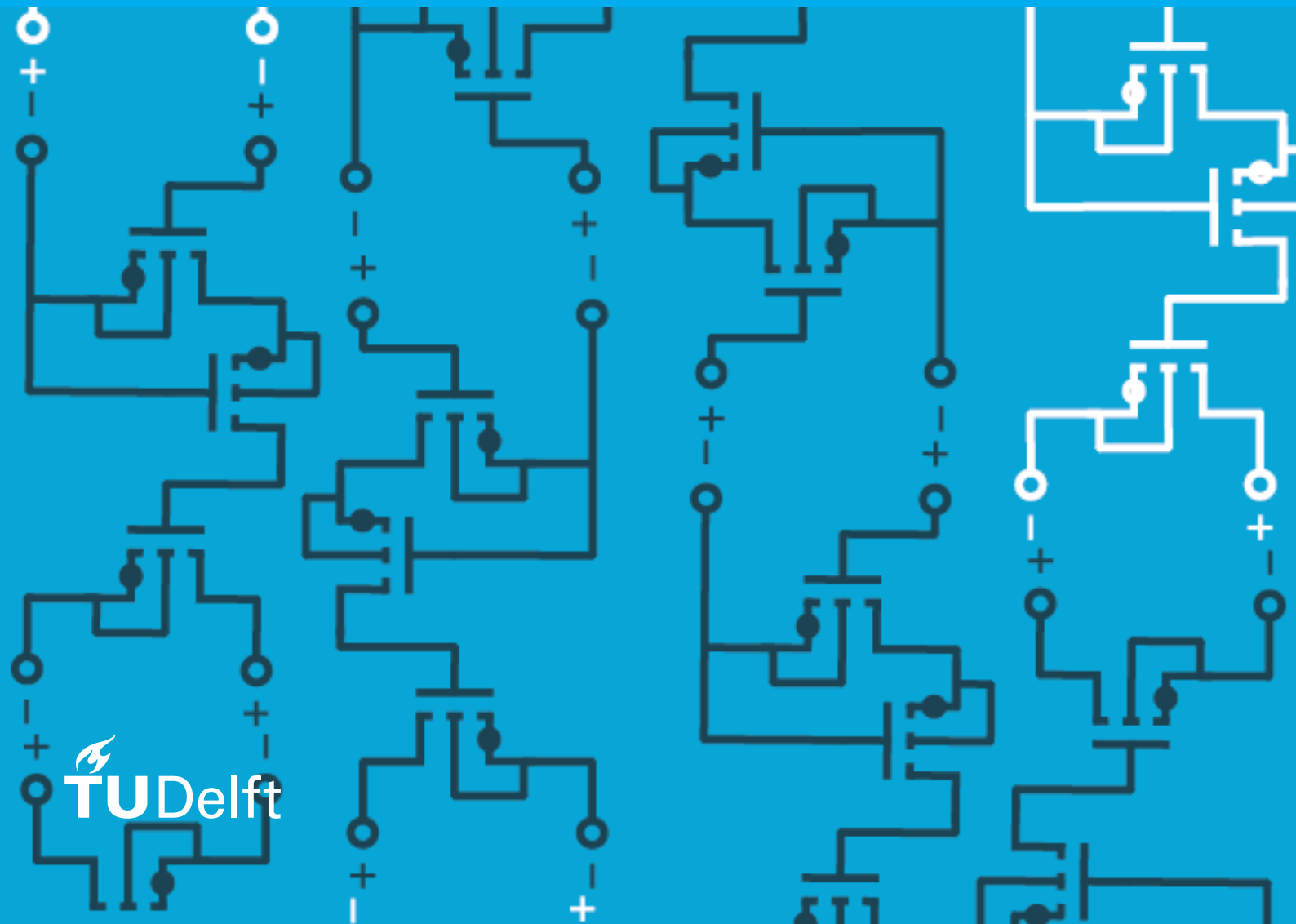

CMOS magnetic field sensor using a pick-up loop

for measuring electric currents

by

J. Boele

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This thesis is confidential and cannot be made public until January, 2023.

TU Delft

Preface

"Make all aproximations you can, as soon as you can, justified or not.
Leave behind you a wake of assumptions and approximations.
All you've to do is go back and check them later.
You can't lose by trying."
[R. Middlebrook, Methods of design-oriented analysis: Low Entrophy Expressions, 1992]

J. Boele
Dordrecht, January 29, 2022

Contents

1 Introduction

As a result of our urgent desire to electrify (personal) transportation, there is a large demand for compact, low cost current sensors. These sensors have numerous applications in transportation but also in power conversion and industry. They can be used for example to monitor the charge and discharge currents of large battery packs, or to accurately measure current flow in an electric drivetrain. Recent trends show completely integrated current sensing systems, where both sensor and readout electronics are made on a single die. The magnetic field as a result of the current, flowing through an external bus-bar, is measured using a magnetic field sensor. Typically a Hall element [1–6] is used as sensor, but some exotic variants exist using magnetoresistive (MR) elements [7, 8] or a fluxgate [9]. The bus bar can be a trace on a printed circuit board (PCB) or part of the leadframe used for packaging the chip. These two examples are shown in 1.1. A less preferred option is the use of bond wires as bus-bar [10].

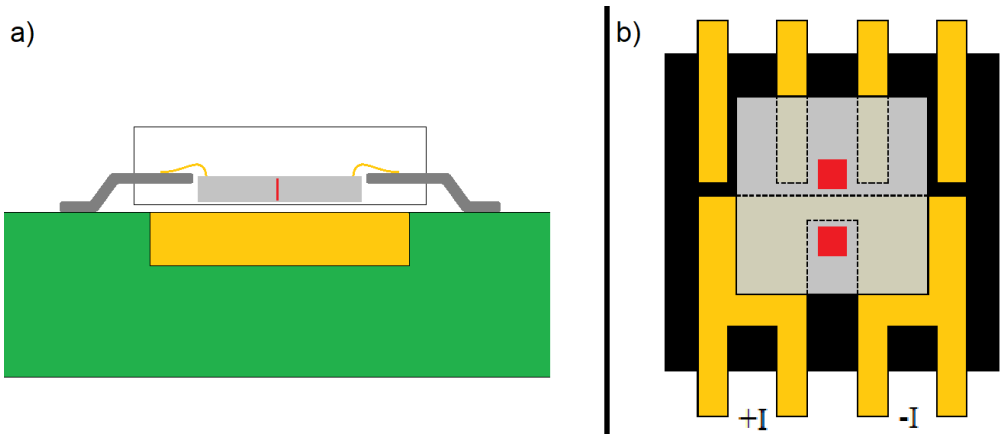


Figure 1.1: a): Cross section of current sensor IC measuring the magnetic field as a result of current flowing through a PCB trace. Red indicates the Sensor location. b). Top view of the layout of a current sensor IC measuring the magnetic field as a result of current flowing through a section of leadframe. Red indicates the Sensor locations considering differential readout. For single ended readout, one of the sensors can be omitted. (Drawings based on [1, 5])

Hall elements are preferred, as they can be made using conventional CMOS technology. This greatly facilitates the integration of the whole system on a single substrate, as this technology is commonly used for manufacturing the readout circuits. In figure 1.2 the block diagram of a typical wideband magnetic field sensor using Hall plates is shown. It consists of two paths one for high frequency (HF) signals and one for low frequency (LF) signals. An output amplifier is used to provide sufficient load drive capabilities. The low frequency path makes use of current spinning in combination with orthogonal connected plates [11] to reduce the large offset component in the Hall plate output voltage. In the high frequency path, the offset is eliminated by use of AC coupling. Such a system is severely limited in bandwidth, as the noise power of a Hall plate increases with bandwidth. The noise resulting from a Hall plate is inversely proportional to the bias current. Therefore, a wideband low noise sensor system using this topology has high power consumption.

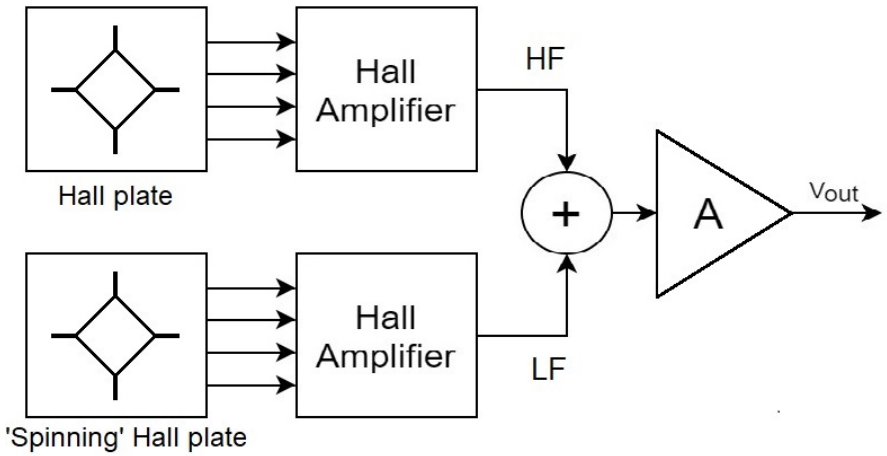


Figure 1.2: Hall Block schematic of a wide band magnetic field sensor using a spinning Hall plate for DC and LF and non spinning Hall plate for HF.

1.1. Motivation and objective

An alternative sensor type is needed to improve the performance of the sensor system, without a large increase in cost. The use of alternative materials for making a Hall element would result in additional (post-) processing steps, increasing the cost. Ferromagnetic sensor materials limit the functionality of the system, as their properties are altered by strong external (common mode) fields. Therefore the use of these materials is to be avoided.

This thesis describes the design of a wideband magnetic field sensors system for electric current sensing in standard CMOS technology. The report describes two phases; a research and a design phase. The research part focuses on exploring different sensor types for improving the bandwidth and power consumption of CMOS magnetic sensing system based on conventional Hall sensors. In the design part, a system using these different sensor is designed and verified on performance.

1.2. Scope

For this thesis, the scope is limited to sensor types that can be made using standard CMOS technology. The intended market for this sensor system is automotive and industry, therefore the system must be capable of operating under harsh conditions (vibrations, large temperature variations). Also the sensor must be capable of enduring magnetic fields much larger than the intended input range. When this strong field is applied, the sensor should remain operational, without any changes to its sensitivity. The design of the bus-bar will not be part of this thesis. However, the effect of fast and large voltage spikes on the bus-bar will be taken into account during the design.

1.3. Organization

The second chapter of this thesis describes the research of Hall plates and alternative magnetic field sensors. Their operation principle and performance is introduced in these sections. The most promising alternative is chosen and motivated. The third chapter describes the design of a system concept using the alternative sensor. Two concepts are presented in this chapter, considering voltage or current as information carrying quantity, but no decision is made yet. This is described in the fourth chapter, where a pick-up loop is designed and a topology for the amplifier was chosen. In the fifth chapter, the amplifier topology is further worked out and verified using simulations. In the sixth chapter a conclusion is presented.

2

Magnetic field sensors

2.1. Introduction

A magnetic field sensor is a transducer that converts a magnetic field quantity into a different physical quantity. From a practical point of view, the output quantity should be electric, thus rendering the solution presented in figure 2.1 useless.

The goal of this chapter is to find alternative sensor types for the commonly used Hall plate. This alternative sensor should be capable of resolving fields up to 10 mT accurately. It must provide a large bandwidth (>1 MHz), large SNR (>40 dB) and have low power consumption (<50 mW). The sensor must remain operational if a strong external field of 1 T is present. Therefore sensors using ferromagnetic materials or MEMS technology are no valid candidates. A sensor using ferromagnetic material becomes magnetized after experiencing a strong field. A MEMS sensor has a high susceptibility of sticking to the substrate (van der Waals-bond) for large deflections caused by strong fields [12]. The application field for the sensor will be automotive and/or industrial, therefore the sensor must be able to work properly in the presence of vibrations, over a wide temperature range and be capable of sustaining large transient voltage steps (i.e. large dV/dt) on the bus-bar.

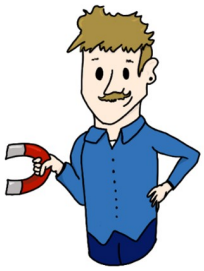


Figure 2.1: A primitive magnetic field 'sensor'.

During the research phase of this project, eight alternative sensor types were considered. In the end only two sensor types, the pick-up loop and the vacuum magnetic sensors were compatible with conventional CMOS technology. These two sensor types are discussed in this chapter. The remaining six sensor types are described in appendix A. For each of these alternatives, the physical working principle, the fundamental performance properties and some state of the art examples will be described. If there is a strong indication that a solution is not feasible for an integrated-on-chip sensor system the research ends.

The focus in this chapter lies on identifying the parameters: noise, bandwidth and maximum signal level. These three parameters were considered as they constitute to the channel capacity (Shannon). For each sensor type, multiple publications of state-of-the-art designs will be discussed. As introduced in the previous chapter, the investigation of sensor principles will be limited to concepts that can be integrated-on-chip using conventional CMOS technology.

In the second section the Hall plate is investigated. In the third section, two alternatives for Hall plates are considered. The fourth part will consist of a conclusion where the most promising sensor(s) are indicated.

2.2. Hall effect sensors

The most commonly used magnetic field sensor is the Hall plate [11, 13]. It is named after E. Hall who first discovered the effect in 1879 using gold leaf clamped on a glass surface [14].

2.2.1. Sensor principle

The operation of a Hall plate sensor relies on a externally supplied constant current flow [11]. This constant bias current I_b is flowing through a flat plate of conductive material. A magnetic field is oriented perpendicular to the plate. Due to this field, charge carriers experience the Lorentz force F_L and are redistributed in the conductor. This results in an electric field gradient perpendicular to the current and magnetic field. A voltage V_H can be measured across the width of the Hall plate due to the redistribution of charge carriers. The voltage is proportional to the magnetic field and to the current flowing through the plate. Figure 2.2 shows the Hall plate with the physical quantities indicated. The figure assumes a bias current, but a bias voltage can also be used [15]. A charge carrier e, moving with velocity v, in magnetic field B and electric field E experiences Lorentz force found as [11]:

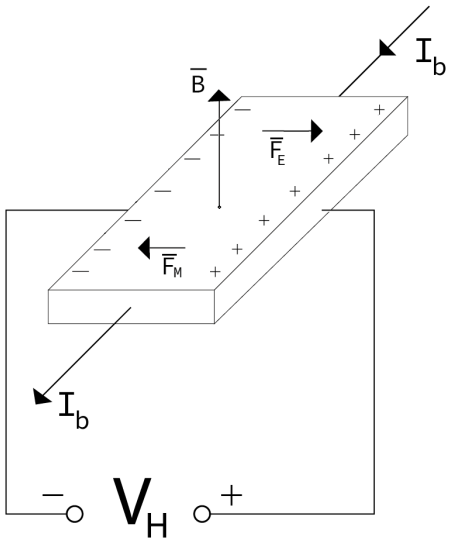


Figure 2.2: The Hall effect demonstrated in a planar conductor.

$$\boldsymbol{F} = e \cdot \boldsymbol{E} + e(\boldsymbol{v} \times \boldsymbol{B}) \tag{2.1}$$

where e is the charge of the particle, E the electric field, v the velocity of the particle and B the magnetic field. The bold faced symbols represent vectors. The Hall voltage as a result of the redistribution of charge carriers under influence of electric field E_H, is found by integrating the electric field along the width w [11]:

$$V_H = E_H w \tag{2.2}$$

where E_H is the electric field resulting from the redistribution of charge carriers and w is the width of the Hall plate. The width is assumed much larger than the thickness of the Hall plate for this expresssion to be valid. A practical relation of the Hall voltage and magnetic field is found as [11]:

$$V_H = G\frac{R_H}{t} I_b B \tag{2.3}$$

where G is a geometrical correction factor (for symmetric hall plates it is ≈ 1), R_H is the Hall scattering coefficient, B the magnetic field perpendicular to the Hall plate surface, t the thickness of the Hall plate and I_b the bias current, assuming a current biased Hall plate. The voltage sensitivity S_{Hv} of a heavily doped semiconductor Hall plate using voltage bias is found to be [16]:

$$S_{Hv} = GR_H \frac{w}{l} \mu_n \tag{2.4}$$

where w the width of the Hall plate, l the length of the Hall plate, μ_n the electron mobility and R_H the Hall scattering coefficient. The model indicates a relation between mobility and sensitivity: high mobility yields high sensitivity. Using the model for a current biased Hall plate, the mobility drops out of the sensitivity equation [11]:

$$S_H = G\frac{R_H}{t} \tag{2.5}$$

Considering this sensitivity expression, typical Hall based sensor systems use current bias. This eliminates the effect of temperature variations on the sensitivity.

2.2.2. Fundamental performance properties

A Hall plate has non-zero resistance therefore it adds thermal noise to the signal. The bandwidth of a Hall plate is large: it is only limited by the parasitic capacitance. Typically the switching frequency used for offset cancellation or the electronics for readout impose an upper limit to the bandwidth at a lower frequency as the cut-off frequency of the Hall plate. The upper limit to the bias voltage or current is set by the material and construction method. Typical sensitivity of a silicon Hall plate is 50 mV/VT [17, 18].

2.2.3. Integrated Hall plate

Hall plates can be made on a silicon substrate [19, 20] using conventional CMOS techniques. Typically it is laid out as a square plate to mitigate offsets related to material anisotropy. The Hall plate is made in a N-well with with four contact pads located at the corners as demonstrated in figure 2.3. One diagonally opposing pair of contacts (for example 1 and 3) is used to apply the Hall bias current I_b. The remaining pair of contacts (2 and 4) is used to measure the Hall voltage. As this Hall plate construction is diagonally symmetric, the contacts used for biasing and sensing can be interchanged. This allows for mitigation of offset, by periodically switching the pairs of contacts between forcing and sensing (i.e. spinning or rotating). Summing the Hall voltage from these two phases cancels the offsets, resulting in a more accurate magnetic field measurement. In this example the Hall plate is operated in two phases of equal duration, but methods using more phases (and contacts) can be used to mitigate the offset [21].

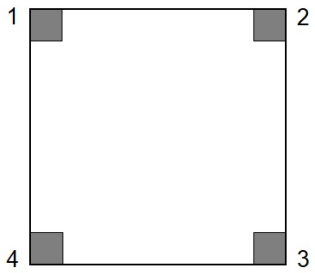


Figure 2.3: Top view of a symmetrical Hall plate layout. The gray squares resemble contact pads.

2.2.4. Materials

A major drawback of a silicon (Si) Hall plate is its low sensitivity. Using high mobility materials for fabricating Hall plates overcomes this problem [22]. Indium-antimony (InSb) is a commonly adopted substrate material having a larger charge carrier mobility as silicon, thus yielding larger sensitivity. The mayor drawback of InSb is the temperature dependency. Other commonly used materials are indium-arsenic (InAs), gallium-nitrate (GaN) Aluminum-gallium-nitrate (AlGaN) and gallium-arsenic (GaAs), all being group III-V elements [23]. These elements have high electron mobility, thus allowing high sensitivity, and can be vacuum deposited using thin film technologies. A second drawback of a Si Hall plate is the high sensitivity for mechanical stress [24, 25]. This makes an accurate measurement difficult, as its sensitivity for stress is similar to the sensitivity for magnetic fields. Finally over a long period of time, the sensitivity of a Hall plate decreases. According to [11], the sensitivity of a current biased Hall plate is decreasing by a rate of:

$$\frac{\Delta S_I}{S_I} = \frac{10^{-4}}{year} \tag{2.6}$$

where S_I is the sensitivity and ΔS_I the difference in sensitivity of a current biased hall plate.

sensor

2.3. Alternative sensor Principles

This section introduces a number of sensor principles, each having their own subsection. The sensor subsections are limited to describing the sensor and do not consider a complete sensor system.

All sensors listed can be used in a feedback configuration (or closed loop) for improved linearity of the transfer [11, 26, 27]. This is done by locally compensating the external field, with another field of opposite sign. This keeps the sensor most of the time in zero-field operating region, thus minimizing the effects of saturation at large signal excursions (i.e. for strong fields)[43]. When the external field changes, the local compensating field no longer is an exact sign-reversed copy of the external field. During this small period of time the feedback loop evaluates the new value of the compensating field, until the difference after summation is zero. The strength of the external magnetic field can be found by measuring the current required for generating the compensating field (assuming a coil as compensating field source)[26]. This feedback method is commonly referred to as a null-detector. The concept is illustrated in figure 2.4.

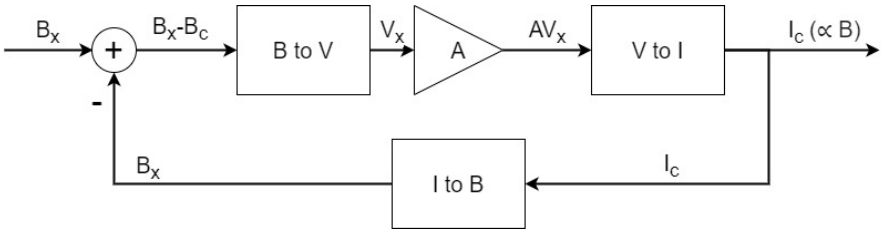


Figure 2.4: A closed loop magnetic field sensing circuit. Block 1 resembles the magnetic field sensor. Block 2 is the controller and amplifies the error signal V_x with a factor A. Block 3 translates this voltage into a current and block 4 uses this current I_c to generate the compensating field B_c. The information about the field strength is embedded in the drive current I_c, as $I_c \propto B_x$ when the loop has settled.

The input signal is magnetic field B_x. The signal is summed with a compensating field $-B_c$, yielding the signal $B_x - B_c$, which should be regulated to zero by the loop. A method for generating the compensating field is forcing current to a coil. The magnetic field generated by a long coil is related to the drive current and is found as:

$$B = \mu_0 \frac{n}{l} I \tag{2.7}$$

where μ_0 is the vacuum permeability, n the turn count, l the length and I the current through the solenoid. Considering fields of 1 T (the upper limit of the input range), a large number of turns per length or (and) a high current is required to generate the desired field. The first option is limited by the large inductance resulting from a high turn count, introducing a bandwidth limit. The second option costs power, assuming $n = 1,800$ kA·m^{-1} is required to generate a field of 1 T. The high current requirement is a serious drawback of a feedback system. Also the current carrying capability of the interconnect wire, and the inter-wire distance should be considered, both will cost chip area. A second disadvantage with this method is that the field produced by the coil will not be a homogeneous magnetic field (assuming a planar coil fabricated using conventional CMOS technology) [27]. This introduces a gain error to the transfer of the overall system. A third disadvantage, of using a compensating magnetic field is that it locally distorts the external magnetic field.

2.3.1. Pick-up loop

A pick-up loop converts a varying magnetic flux into a voltage according to Faraday's law of induction [28]. Usually it is made by using multiple loops of conducting wire are to form a coil. A pick-up loop requires no external power for operation, unlike all other principles investigated.

Transducer principle

Operation of the pick-up loop as magnetic field sensor can be explained using Faraday law of induction. The induced voltage as a result of a varying magnetic flux is found as [11]:

$$V_i = -n\frac{d\phi(t)}{dt} = -n\frac{d(nA(t)\mu_0\mu_r(t)H(t))}{dt} \tag{2.8}$$

where n is the turn count, A the area of a single loop, μ_0 and μ_r the relative and vacuum permeability, $H(t)$ the magnetic field and $\phi(t)$ the magnetic flux. The flux must vary in time to obtain a non-zero induced voltage. It is not capable of detecting constant or static (i.e. 'DC') magnetic fields. A time varying flux can be realized by varying the area, the permeability or the external magnetic field. Air coils make use of air as core material, equivalently $\mu_r = 1$, therefore the induced voltage is a linear function of frequency and field strength. Assuming a stationary air coil (thus constant area A) and a sinusoidal source of magnetic field, the induced output voltage is found as [11, 13]:

$$V_i = -nA\mu_0 \frac{dH(t)}{dt} = -nA\frac{dB(t)}{dt} \tag{2.9}$$

A pick-up loop is direction dependent; if the plane of the loops is oriented perpendicular to the magnetic field the induced voltage is maximal and for parallel orientation it is zero (assuming a stationary source of sinusoidal field). The sensitivity of a pick-up loop can be increased using a ferromagnetic core at the cost of introducing non-linearity to the transfer due to hysteresis (especially for large fields). A ferromagnetic core increases the sensitivity by a factor μ_r. For small fields, the induced voltage of a pick-up loop with a ferromagnetic core is found as [11]:

$$V_i = -nA\mu_r \frac{dB(t)}{dt} \tag{2.10}$$

This is a linear transfer function. In large field demagnetization effects can no longer be neglected. The voltage-field relation is found as [11]:

$$V_i = -nA\frac{\mu_r}{1+D(\mu_r-1)}\frac{dB(t)}{dt} = -nA\mu_a\frac{dB(t)}{dt} \tag{2.11}$$

where D is the demagnetization factor, and μ_a the apparent relative permeability. As previously mentioned, a core would introduced a non-linear component to the transfer. This is because of saturation and hysteresis properties of ferromagnetic material. The core permeability changes with time, temperature, DC magnetization and when subjected to mechanical stress. A strong magnetic field causes the core to saturate, resulting in a different in sensor sensitivity. Using a feedback coil wrapped around the same core, saturation can be avoided at the cost of an increased power consumption. Therefore the use a ferromagnetic materials is not preferred and should be avoided.

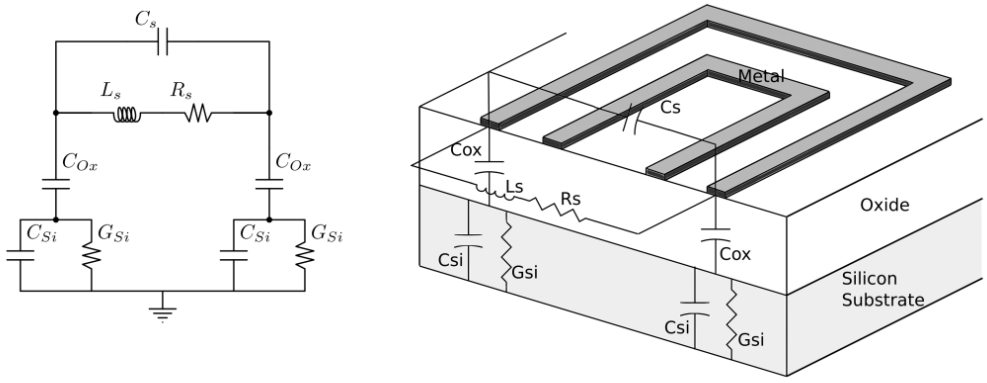
Fundamental performance properties

In the previous section it became clear that the pick-up loop is incapable of detecting static magnetic fields. A hybrid sensor system, as for example seen in a DC current probe [29], obtains large bandwidth including DC. This system type uses a different type of sensor for the DC and low-frequency part of the bandwidth, and a pick-up loop for the high frequency part of the bandwidth. A pick up loop requires no power for operation, therefore a reduction in power consumption can be obtained compared to a wide band Hall sensor system.

The pick-up loop is fabricated using the aluminum or copper interconnect layer(s). Therefore, it will have non-zero series resistance introducing thermal noise. The thermal noise will determine the minimum frequency where the pick-up loop provides a useful SNR (i.e. SNR»1). The upper limit of the bandwidth results from the parasitic capacitance to substrate combined with the inductance and series resistance of the pick-up loop. These three circuit components form a second order low-pass filter. The effect of the substrate capacitance can be eliminated by using the short circuit current as information carrying quantity, thereby increasing the bandwidth of the sensor. The amplitude of the induced voltage (i.e. pick-up loop output signal) is frequency dependent, increasing with a rate of 20 dB per decade. Therefore the spot SNR is frequency dependent, as well as the dynamic range, both increase with frequency. The amplitude can also be manipulated by the turn count and loop area. Considering a pick-up loop with air core, the maximum magnetic field strength will be set by the breakdown voltage of the isolation material in between traces.

In figure 2.5a model for an integrated coil is presented [30]. Typically planar constructions are opted, figure 2.5b shows an section of a so called pancake-style coil. Figure 2.5a shows a model of an on-chip flat coil. A number of parasitic components are considered. As with any practical implementation of an inductor, the wire has non-zero resistance resulting in series resistance R_s. The inter-winding or distributed capacitance is modeled in parallel to the inductance L_s as capacitor C_s . The model also includes a capacitance to model the coupling between pick-up loop and substrate using capacitor C_{ox}. The series resistance and oxide capacitance are the most important elements after the inductance. The model forms a 2nd order low-pass

filter. Parasitic capacitance C_{ox} can be eliminated by using the short-circuit current as information carrying quantity. This increases the effective bandwidth of the pick-up loop.



(a) Equivalent circuit for integrated coil working at RF frequencies

(b) Cross section of integrated coil operating at RF frequency

Figure 2.5: Equivalent Model of an integrated coil (a) and a cross section of the coil on a Si substrate (b). [30]

State-of-the-art

In [31] a design for an integrated inductor for magnetic field measurements is shown. The substrate below the coil is removed. The conductivity of the Si substrate causes eddy currents to flow decreasing the sensitivity. The problem is prominent for high frequency fields (>10 MHz), but for lower frequencies the effect can be neglected. For a high pick-up loop sensitivity, a large turn count is needed. A coil having low effective area but high turn count is proposed in [32] by using a flip-chip integration method. A model is presented for the proposed inductor construction. Unfortunately no actual chip-inductors using the proposed method where made and tested.

As mentioned, a pick-up loop is not capable of resolving DC fields. A second sensor of a different type is needed to obtain a large bandwidth including DC, resulting in a hybrid system. In [3, 4] a hybrid magnetic field sensor system utilizing a pick-up loop and a Hall plate is demonstrated. The design measures the magnetic field resulting from a current carrying conductor differentially by using a pair of sensor of each type on each side of the conductor. The coils uses about 1/3th of the total chip area as a result of a single layer planar layout. A pair of Hall plates provides the low frequency transfer and two pick-up loops are used for high frequencies, providing a total system bandwidth of DC up to 3 MHz. The output signals of the two paths are combined using an analog filter. This requires a careful design of the crossover behavior in order to obtain a flat transfer. In both systems, the crossover frequency is set to 2 kHz, close to the point where the SNR of the coil equals the SNR of the Hall plate. The advantages found compared to a single Hall plate is an improved noise performance.

In [7, 8, 33] hybrid current sensors are introduced using the HOKA principle. The designs make use of pick-up loops for high-frequency magnetic field component and are implemented on PCB-scale. They provide extensive insight in the methods used for combining the signal paths. The first paper mentioning the HOKA principle [33] considers a Hall plate for the DC and low frequency magnetic field component. [7, 8] make use of a tunneling-magneto-resistive, respectively giant-magneto-resistive element for resolving DC and low frequency magnetic fields. [34] presents a desing using Hall plates and a Rogowski coil as pick-up loop. The special layout of this pick-up loop allows a system bandwidth up to 75MHz.

2.3.2. Vacuum magnetic sensor

For well over 150 years, magnetic fields are known to deflect electron beams. In 1880, multiple devices were developed using electron beams deflected by magnets, known as cathode ray tubes. Around the same time A. Schuster, J.J. Thomson and J. Perrin made use of cathode ray tubes to evaluate the mass and charge of an electron [35]. Permanent magnets were used to center the electron beam on an external target. The target is held at a high positive voltage to attract electrons. A similar cathode ray tube was developed by F. Braun around 1897, with the addition of a fluorescent screen inside the tube as commonly seen in more recent cathode ray tubes. The screen emits visible light when bombarded with electrons. In 1899, J. Zenneck in cooperation with F. Braun, improved the cathode ray tube further by the addition of electromagnets for accurately controlling the beam position on the screen. This enabled Zenneck and Braun for the first time in history to visualize an electric signal [35]. The use of electromagnets for deflecting electron beams would become essential in the late 1930s for the development (and at a later point for the miniaturization) of commercial television sets.

Transducer principle

In a cathode ray tube, an electron beam is deflected by a magnetic field perpendicular to the beam (electric fields could also be used to deflect the beam). The deflection can be accurately controlled by feeding current trough coils wrapped around the middle of the cathode ray tube. Similarly, if the external field is unknown, but all other properties of the electron beam and path length are known, the principle could be used to measure a magnetic field. Measuring the deflection as a result of the unknown magnetic field contains information about the field strength. An electron moving in a homogeneous magnetic field experiences a force found as:

$$\boldsymbol{F} = e(\boldsymbol{v} \times \boldsymbol{B}) \tag{2.12}$$

where e is the charge of the particle, v the velocity and B the magnetic field. This expression is derived from expression for the Lorentz force introduced in (2.1), assuming $E = 0$. The force is perpendicular to the velocity and magnetic field. The particle will move in a circular trajectory if the magnetic field and velocity are perpendicular. The radius of the circular trajectory is:

$$r = \frac{mv}{eB} \tag{2.13}$$

where m is the mass of the particle and r the radius of the circular path. This relation indicates the radius being inversely proportional to the magnetic field strength.

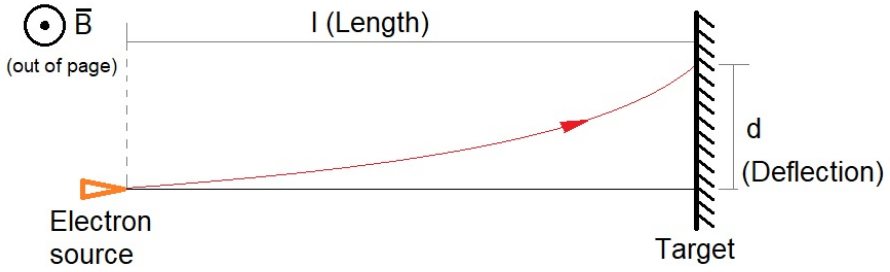


Figure 2.6: Deflection of an electron beam (red) due to the influence of a magnetic field (pointing out of the page).

In figure 2.6 the deflection of an electron beam as result of a magnetic field is illustrated. The deflection measured on a target plane perpendicular to the zero-field propagation direction is:

$$d = r(1 - \cos(\phi)) \tag{2.14}$$

where d is the distance of deflection, r the radius and ϕ the angle of rotation. For small deflections the model can be simplified to:

$$d = B\frac{el^2}{2mv} \tag{2.15}$$

where l is the path length. The electron velocity can be found by manipulating the relation $\frac{1}{2}mv_e^2 = eV$ into:

$$v_e = \sqrt{\frac{2eV}{m}} \tag{2.16}$$

where v_e the velocity and V the potential in volts. For an acceleration potential of 100 V, the velocity will be about $5.9 \cdot 10^6$ m/s or 5900 km/s. The deflection, assuming an electrode distance of 1μm is:

$$d = B\frac{el^2}{2mv} = 1.49 \cdot 10^{-8} B \tag{2.17}$$

Thus for a channel length of 1 μm and a potential of 100 V the resulting deflection is about 15 nm/T. Increasing the electrode distance to 10 μm results in 10^2 more deflection, or 1.5 μm/T. From these simple calculations it becomes clear that the sensitivity is related to the cathode anode distance, where a larger distance yields a higher sensitivity. The cathode to anode distance can't be made arbitrary large, as the electric field strength decreases with distance (assuming a fixed potential across the anode-cathode spacing). The use of an accelerator electrode can mitigate this problem. Typically a field strength of $> 10^7$ V/cm is required to obtain 'cold' emission. The shape of the cathode influences the minimum potential required for emission: sharp, conical-shaped structures provide the best results.

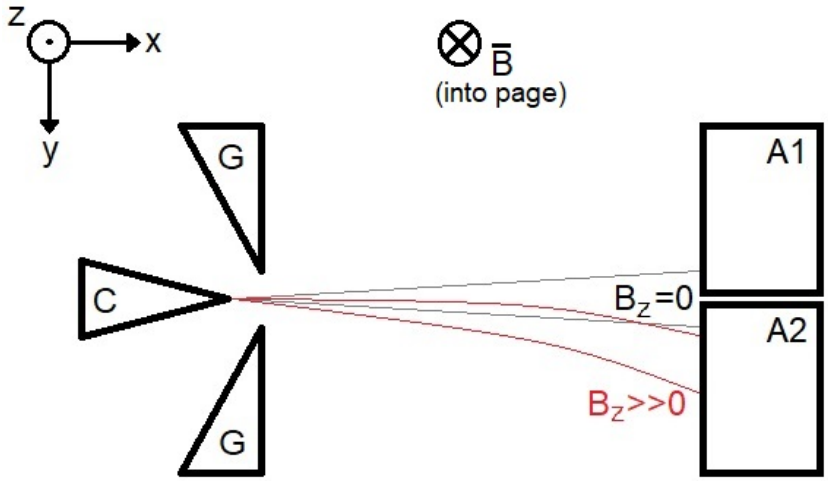


Figure 2.7: Simplified construction of a CMOS vacuum magnetic field sensor. The magnetic field is applied in the -Z direction, pointing into the page.

The deflection is measured using two isolated targets as anode (i.e. split-anode) biased at the same potential [36, 37]. Figure 2.7 shows a simplified vacuum magnetic sensor, consisting of cathode C in the form of a tip-shaped field emitter, gate structures G and the pair of anodes A_1 and A_2. The layout and dimensions of the gate and cathode influence the angular divergence of the electron beam. The gate voltage is used to control the beam current. For zero field, the beam is positioned such that half of the beam current impinges on each anode, indicated in figure 2.7 as the black beam. When a perpendicular magnetic field (in the negative Z-direction, pointing into the page) is present the beam current is no longer split equally per anode. The difference in anode current is proportional to the field strength. At some point, after increasing the field strength, the beam only hits one anode, the situation is exaggerated in figure 2.7, indicated by the red beam. Stronger fields cannot be detected using this method, as the difference in the 2 anode currents ca not become larger. An advantage of a two-anode construction is that the beam intensity is eliminated from the transfer: the information is embedded in the relative difference in anode current and not in the absolute anode current, as is the case for a single anode device.

Fundamental performance properties

In vacuum magnetic field sensors, vacuum is used as a transport medium. In comparison with semiconductors, the vacuum does not impose a speed limit. Therefore the bandwidth of a vacuum sensor is expected to be large. A second advantage of the vacuum is that the mobility of charge carriers is not depending on temperature. The vacuum is expected to provide lower 1/f-noise, as there are no charge traps, like seen in a semiconductor interface. The maximum field intensity is limited by the device dimensions, a small anode to

cathode distance would enable very large fields to be detected, but sacrifices the low end of the input range. The input range is limited to about one decade, but it can be increased with the application of (magnetic) feedback. Drawbacks of vacuum magnetic sensors are the high voltage required for field emission, the relative large device size ($> 10x10$ mm) and the required high vacuum. This vacuum must be better than 0.13 mPa ($1.3 \cdot 10^{-6}$ mBar) to obtain a long lifespan of the emitter. It requires a hermetically sealed package for maintaining the vacuum.

State-of-the-art

In [37–39] a CMOS planar magnetic field sensoris described utilizing a field array emitter and a two-anode target. The anode to cathode distance is 10μm, and the device needs to be in a vacuum lower than 0.13 mPa ($1.3 \cdot 10^{-6}$ mBar) in order to avoid damage to the field emitter. The sensitivity of the sensor is defined as a percentage of half the beam current and is found to be 4000%/T, for a field strength range of 0...1 mT. The use of conventional CMOS technology limits the layout of a vacuum magnetic sensor to planar structures, where the electron beam is in plane with the substrate. In [40] a sensor is described using additional manufacturing process to obtain a sensor with an electron beam propagating in the Z-direction. The gate, focus and cathode electrodes where made using conventional CMOS technology, but the anode consists of a separate structure placed 5mm from the cathode. The device uses a two anode detector structure and has an additional focusing electrode to obtain a collimated beam. This was done to obtain a higher sensitivity in the X and Y direction, but reduced sensitivity in the z-direction In [41] another vacuum magnetic field sensor is described using a field emission array with an additional pair of deflection electrodes. These electrodes are biased at $+V/2$ and $-V/2$ respectively. They provide a perpendicular electric field to compensate the magnetic deflection, thus increasing the upper limit of field strength to be measured. The device is capable of detecting magnetic fields up to 0.1 T. The device could be used in a null-detector system, using the electric field to compensate the deflection of the magnetic field. The strength of the electric field required to return the beam to zero-field position on the anode would then provide information about the magnetic field strength.

2.4. Conclusion

This chapter starts with the description of Hall plate magnetic field sensors. In this remaining sections of this chapter, two alternative magnetic field sensor principles were described that could replace the commonly used Hall plate. Pick-up loops and vacuum magnetic sensors were considered as they are fully compatible with conventional CMOS technology and require no ferromagnetic materials or MEMS technology. The pick-up loop seems to be the most promising solution. It is a simple to construct sensor type and offers unprecedented dynamic range, but it is not capable of detecting DC fields. This could be solved using a combination of sensors as demonstrated in [4, 7, 8, 29, 33, 34]. Therefore the remaining chapters of this thesis will focus on a hybrid magnetic field sensor system using a pick-up loop for HF signals and Hall plates for LF signals.

3

System concept design

3.1. Introduction

This chapter describes the concept design of a hybrid current sensor. The term hybrid indicates the use of multiple sensors in parallel combined to a single output node. A Hall plate is chosen for resolving the DC and LF signals and a pick-up loop for the HF signals as demonstrated in [4, 7, 8, 29, 33, 34, 42]. This solution provides a lower noise contribution compared to a Hall-based wide band sensor. Special care is needed when designing the crossover behavior between the two transducers. The amplitude, phase and crossover frequencies of the two sensor paths must be exactly equal to obtain a flat magnitude and phase transfer without a transition zone. Figure 3.1 shows a top level block diagram of the hybrid sensor system consisting a pick-up loop and Hall plate path. Each path contains a sensor (or multiple sensors) and a dedicated amplifier. Their output signals are combined into one signal. And finally there is an output amplifier providing the required output drive capabilities.

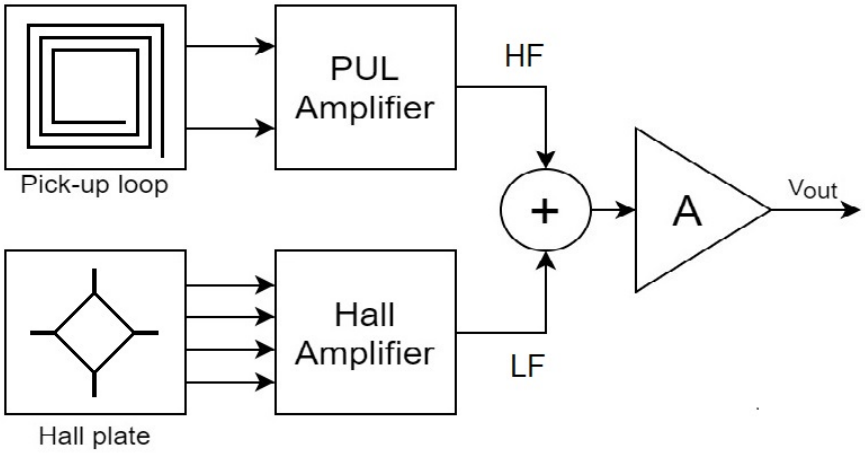


Figure 3.1: Top level block diagram of a hybrid sensor system consisting of a pick-up loop and a Hall plate path.

3.2. System requirements

This section introduces the system level requirements, as requested by the client (i.e. the company SystematIC design BV). The section is subdivided into four subsections: functional requirements, signal processing requirements, environmental requirements and cost factors.

3.2.1. Functional specification:

Table 3.1: Functional specifications

functionality	description	Comments/notes
1	Amplification	Increasing the available power of the signal
2	Conversion	Change Magnetic field (or current) signal into a proportional voltage signal at the output
3	Combination	Sum two signal paths to one output path

3.2.2. Signal processing

Table 3.2: Performance requirements, system level

Req	description	value	unit	verification method	Comments/notes
1	Noise	<60	μT	Spectrum analyzer	RMS integrated noise, source referred
2	Bandwidth (-3dB)	>5	MHz	phase-gain analyzer or oscilloscope, compare result with mid-band gain	
3	Sensitivity	500	V/T	Apply known B-field and measure output signal. Compare result with calc.	max output swing / max input signal (Req9/Req4)
4	Signal (max)	8	mT	Oscilloscope (with FFT) or spectrum analyzer	System must no clip / saturate at given input level
5	Offset	<10	μT	Measure output voltage with zero current (or field)	differential
6	Full scale error	<1	%	Measure maximum output voltage and compare with calculated maximum signal	use sensitivity and max. signal (Req3 + Req4)
7	Sensitivity error drift	<1	%	Measure maximum output voltage and compare with calculated maximum signal	Over whole Lifetime $T_a = 25°C$
8	Chopping spurs	<1.5	mV(RMS)	Measured using Spectrum analyzer at output of system	including folded back components
9	Maximum output level	4	V	voltmeter	0.8VDD(min) used for evaluating sensitivity (Req3)

3.2.3. Environmental requirements

Table 3.3: Environmental requirements

Req	description	value	unit	verification method	Comments/notes
1	Maximum temperature	150	°C	Climate chamber temperature setting	Better to design for 0 TC
2	Minimum temperature	-55	°C	Climate chamber temperature setting	Better to design for 0 TC
3	Common mode Transient immunity	>25	kV/μs	HV probe + oscilloscope	Voltage step op bus-bar
4	ESD discharge	2000	V	ESD-gun, 2 kV on each pad	IEC 61000-4-2 level 1: 2 kV HBM
5	Isolation Voltage	1000	V	Between bus-bar and sensor system	1 minute

3.2.4. Cost factors

Table 3.4: Cost factors

Req	description	value	unit	verification method	Comments/notes
1	Minimum supply voltage	3	V	Power supply setting during test	typical supply is 5V
2	Maximum supply voltage	5.5	V	Power supply setting during test	Technology dependent
3	Maximum current consumption	10	mA	Measure current consumption	multiple methods possible
4	Chip Area	T.B.D.	mm^2	proved by design	Layout editor (?? T.B.D.)

3.3. Sensor models

This section describes models for the pick-up loop and Hall plate magnetic field sensors. At this point, no specifications of the two sensors are known. Therefore this section focuses on the derivation of universal source models for the pick-up loop and Hall plate.

3.3.1. Pick-up loop

A pick-up loop has a linear frequency dependent magnetic field to voltage relation. This is the result of the induced voltage being proportional to the derivative of the magnetic flux. Thus the voltage is increasing in magnitude proportional to the frequency.

According to the Farady's law of induction, the induced voltage as a function of magnetic field $b(t)$ is found as [11, 13]:

$$v_i(t) = -n\frac{d\phi(t)}{dt} = -nA\frac{db(t)}{dt} \tag{3.1}$$

where ϕ is the magnetic flux, b is the magnetic field confined by a single loop with area A and n is the number of turns. The minus sign in the equation is a result of the induced voltage opposing the magnetic flux. It can be removed from the transfer by interchanging the two terminals of the pick-up loop. Transforming this relation to the frequency domain results in:

$$V_i = -snAB \tag{3.2}$$

where s represents the Laplace operator. Using $S_H = nA$ as sensitivity of the pick-up loop, this expression reduces to:

$$V_i = -sS_{PUL}B \tag{3.3}$$

Inductive circuit model

The pick-up loop will have inductance, as it is a coil of highly conductive material (Cu or Al traces on the interconnect layer). Neglecting the wire resistivity for now, a simple circuit model for the pick up loop would be a voltage source with value V_i and a series inductance with value L_s. The model is shown in figure 3.2

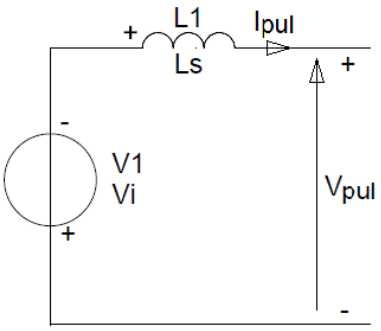


Figure 3.2: Simple pick-up loop model.

The output quantity can be either voltage or current. The output voltage, or open-circuit voltage is found as:

$$V_{PUL} = -V_i = sS_{PUL}B \tag{3.4}$$

and the short-circuit current:

$$I_{PUL} = -V_i \cdot \frac{1}{sL_s} = \frac{S_{PUL}B}{L_s} \tag{3.5}$$

Pick-up loop circuit model with parasitic elements

In reality, the traces of the pick-up loop will have non-zero resistivity, introducing series resistance to the model. Next to the series resistance, the pick-up loop also has parasitic capacitance to substrate (C_p) and distributed capacitance (C_d) between consecutive turns. Expanding the model to include these parasitic components results in the lumped circuit shown in figure 3.3:

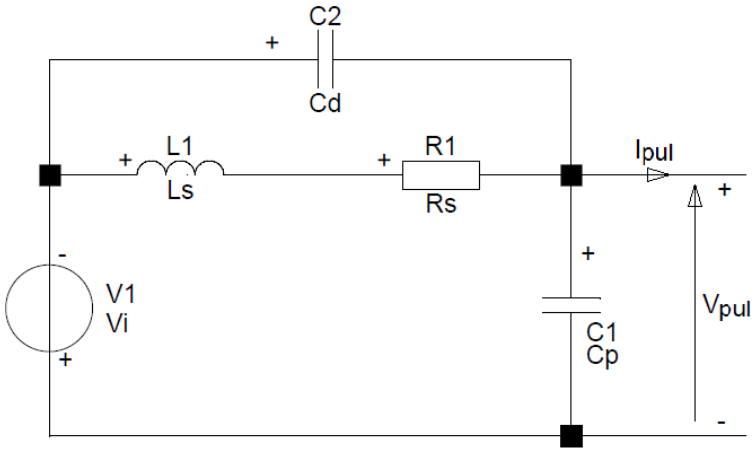


Figure 3.3: Pick-up loop model including parasitic elements.

The output quantity can be either voltage or current. The output voltage, or open-circuit voltage is found as:

$$V_{PUL} = -V_i \cdot \frac{s^2 L_s C_d + sR_s C_d + 1}{s^2 L_s (C_p + C_d) + sR_s (C_p + C_d) + 1} = \frac{sS_{PUL} B(s^2 L_s C_d + sR_s C_d + 1)}{s^2 L_s (C_p + C_d) + sR_s (C_p + C_d) + 1} \tag{3.6}$$

and the short-circuit current:

$$I_{PUL} = -V_i \cdot \frac{R_s + sL_s}{s^2 L_s C_d + sC_d R_s + 1} = \frac{sS_{PUL} B(sL_s + R_s)}{s^2 L_s C_d + sC_d R_s + 1} \tag{3.7}$$

Simplified pick-up loop circuit model

Figure 3.4 shows the simplified circuit for modeling the mid-band transfer of the pick-up loop. This model is used for designing the in-band transfer of the amplifier. For the design of the high frequency roll-of of this amplifier the complete model including parasitic components is used. The simplified circuit does include the series resistance. Inductance L_s, substrate capacitance C_p and distributed capacitance C_d are expected to only influence the transfer at high (out-of-band) signals. At a later point in the design of the pick-up loop it became clear that the impedance presented by its inductance is much smaller compared to the series resistance considering the bandwidth requirement. Therefore the pick-up loop can be modeled as a magnetic-field sensitive resistance when considering in-band signals.

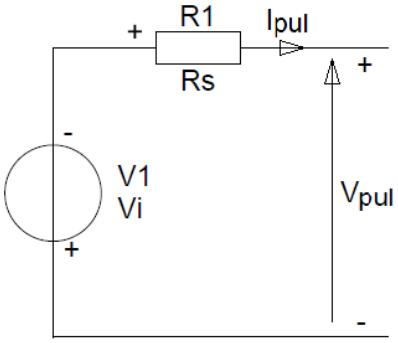


Figure 3.4: Pick-up loop model including parasitic elements.

The output quantity can be either voltage or current. The output voltage, or open-circuit voltage is found as:

$$V_{PUL} = -V_i = sS_{PUL}B \tag{3.8}$$

and the short-circuit current:

$$I_{PUL} = -V_i \cdot \frac{1}{R_s} = \frac{sS_{PUL}B}{R_s} \tag{3.9}$$

Pick-up loop noise model

The series resistance of the pick-up loop introduces thermal noise. Assuming the simplified sensor model the spectral density of this noise source in V^2/Hz is:

$$S_{v,n_{PUL}} = 4kTR_s \tag{3.10}$$

In figure 3.5 the signal magnitude and noise are plotted as a function of frequency. This figure clearly shows a increasing signal to noise ratio as a function of frequency. This can be used to lower the total integrated source referred noise of a wideband magnetic field sensor system.

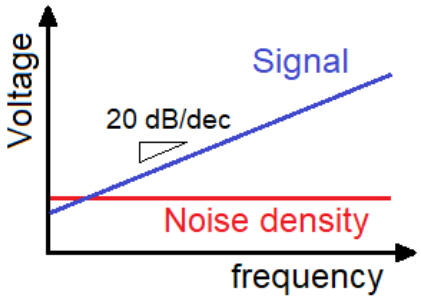


Figure 3.5: Noise and signal voltage as a function of frequency resulting from the Pick-up loop.

3.3.2. Hall plate

In section 2.2.1 the Hall plate was introduced as magnetic field sensor. Equations relating the magnetic field to the hall voltage V_H were described. For a current biased Hall plate the Hall voltage as a result of the magnetic field is:

$$V_H = S_H B \tag{3.11}$$

where S_H is the magnetic field sensitivity of a current biased Hall plate, introduced in 2.2.1 as:

$$S_H = G\frac{R_H}{t} \tag{3.12}$$

Resistive Hall plate circuit model

The Hall plate is made in a silicon substrate having non-zero resistivity. A circuit model of the Hall plate is shown in 3.6, were the non-zero resistivity is modeled as a series resistor with value R_h (note: R_H and R_h are not the same!).

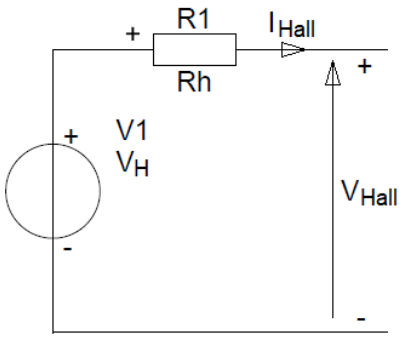


Figure 3.6: Hall plate circuit model with series resistance.

The output voltage, or open-circuit voltage is found as:

$$V_{Hall} = V_H = S_H B \tag{3.13}$$

Hall plate circuit model with parasitic components

The Hall plate model introduced in 3.3.2 model has infinite bandwidth. In reality, the bandwidth of a Hall plate is finite as a result of parasitic capacitance. This can be modeled using a capacitor C_h, demonstrated in figure 3.7.

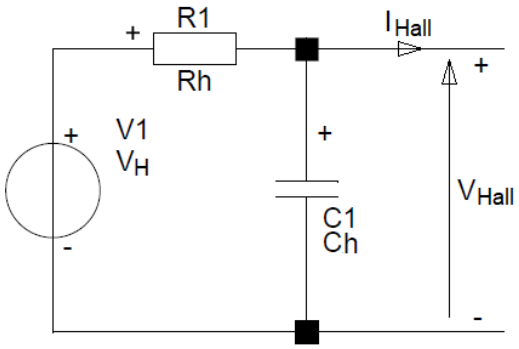


Figure 3.7: Hall plate circuit model with series resistance and parasitic capacitance.

The output voltage, or open-circuit voltage is found as:

$$V_{Hall} = V_H \cdot \frac{1}{1+sC_hR_h} = \frac{S_H B}{1+sC_hR_h} \tag{3.14}$$

The low-pass corner frequency f_H of the circuit is $1/(2\pi\tau_H)$ were time constant $\tau_H = R_h C_h$. The model has a bandwidth from DC to f_H. The magnetic field sensor system will use a Hall plate for the low frequency magnetic field information. The bandwidth of the Hall plate path will be limited to the crossover frequency. This frequency will be much lower than the low-pass hall corner frequency f_H, equivalently $f_H >> f_{cross}$. Therefore, the design of the system will consider the resistive circuit model.

Hall plate noise model

The series resistance of the Hall plate introduces thermal noise. Assuming the simplified sensor model the spectral density of this noise source in V^2/Hz is:

$$S_{v,n_H} = 4kTR_h \tag{3.15}$$

In figure 3.8 the signal magnitude and noise are plotted as a function of frequency. This figure clearly shows a constant signal to noise ratio as a function of frequency.

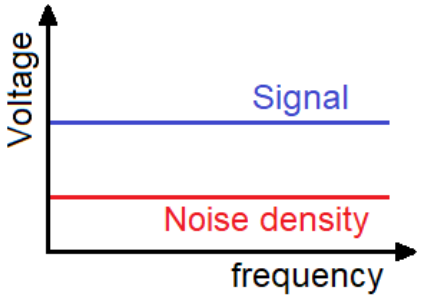


Figure 3.8: Noise and signal voltage as a function of frequency resulting from the Hall plate model.

Hall plate offset

The Hall voltage V_H contains a component proportional to the magnetic field and an offset component. The offset component is of larger magnitude as the signal. Using the current spinning technique [11, 17], these offsets can be mitigated. This method 'rotates' the sense and force terminals of the hall plate over 4 phases. The resulting Hall voltage readings are averaged, thereby reducing the (orientation dependent) offsets. The switching takes place at a frequency higher than the Hall-path bandwidth. As a result of the switching, a residual offset component is up-modulated and appears as noise in the pick-up loop path bandwidth. The design of the Hall-path will not be part of this thesis, as there is already a design available within the company. This design Hall-path design is part of a hybrid Hall plate magnetic field sensor, consisting of a low and high frequency Hall path.

The pick-up loop does not produce offset. The signal processing electronics will however contribute some offset to the signal. By using AC-coupling at the output of the pick-up loop path, the offset is eliminated. This can be implemented in the high-pass filter at the end of the pick-up loop path.

3.4. Hybrid current sensor concepts

A pick-up loop does not provide DC-transfer. Therefore a two channel hybrid sensor topology is chosen, using a Hall plate for the DC transfer, as demonstrated in [4, 7, 8, 29, 33, 34, 42]. The Signal to noise ratio of a pick-up loop is increasing with frequency. A Hall plate has a constant signal to noise ratio versus frequency.

3.4.1. Concept 1: pick-up loop voltage readout

The first system concept is shown in figure 3.9, using simple source models introduced in the previous sections. In the first concept assumed the corner frequency of the Hall plate as crossover point. Considering the relative high frequency of this pole, it will probably not yield best signal to noise ratio for the complete system and difficulties with matching the pole locations will be unavoidable. A second concept is therefore derived, where the crossover frequency can be arbitrarily set using one filter section.

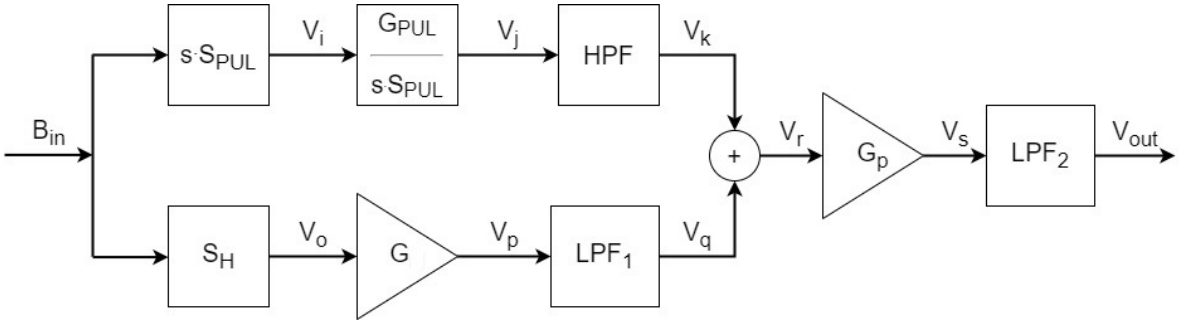


Figure 3.9: Concept 1: A hybrid Hall+pick-up loop sensor system.

On the left side magnetic field B_{in} is applied to the system. The signal is converted in to voltage by the two sensors. The sensor sensitivities are represented by S_{PUL} and S_H for the pick-up loop and Hall plate respectively. Considering the pick-up loop path, the voltage at this point is:

$$V_i = s \cdot S_{PUL} B_{in} \tag{3.16}$$

This signal is proportional to frequency. A flat transfer is obtained in the following block that consists of an integrator operation and a gain factor G_{PUL}. After this block the signal is:

$$V_j = G_{PUL} B_{in} \tag{3.17}$$

Now the signal must be filtered to introduce the crossover corner frequency (i.e. high pass corner) with time constant τ_{cross} using the HPF block. The HPF block has transfer:

$$H_{HPF} = \frac{s\tau_{cross}}{s\tau_{cross}+1} \tag{3.18}$$

The output signal after passing through the filter is:

$$V_k = G_{PUL} B_{in} \frac{s\tau_{cross}}{s\tau_{cross}+1} \tag{3.19}$$

This signal is fed into a summing block where it is added to the Hall path signal V_q. Considering the Hall path, after the sensor has converted the magnetic field to a voltage, the signal is:

$$V_o = S_H B_{in} \tag{3.20}$$

The signal is expected to be very small as typical Si-Hall elements have a sensitivity of 50 mV/V/T [17]. An amplifier with gain $G = G_{PUL}/S_H$ is used to increase the signal amplitude to the same level as the signal resulting from the pick-up loop path V_k. After this amplifier the signal is:

$$V_p = G_{PUL} B_{in} \tag{3.21}$$

This signal is filtered using a low-pass filter to introduce the desired crossover corner frequency using block LPF_1 with transfer function:

$$H_{LPF_1} = \frac{1}{s\tau_{cross}+1} \tag{3.22}$$

The output signal after passing through the filter is:

$$V_q = G_{PUL} B_{in} \frac{1}{s\tau_{cross}+1} \tag{3.23}$$

Both input signals of the summing block are now described. The resulting signal after summing is:

$$V_r = V_k + V_q = B_{in} G_{PUL} \tag{3.24}$$

This signal is increased by the output amplifier with a gain of G_p. Finally, the system bandwidth is limited using a second low-pass filter LPF_2 with transfer function:

$$H_{LPF_2} = \frac{1}{s\tau_h + 1} \tag{3.25}$$

where τ_h represents the time constant of the filter. The filter LPF_2 and output amplifier can be combined to one circuit block. Similarly, the summing block, LPF_1 and HPF_1 can be merged into one circuit block. The source to load transfer H_{C1} of the system is:

$$H_{C1} = \frac{V_{out}}{B_{in}} = \frac{G_p G_{PUL}}{s\tau_h + 1} \tag{3.26}$$

The system sensitivity is $S_s = G_p G_{PUL}$.

Noise

This paragraph presents the noise model of concept 1. In figure 3.10, the model is shown including equivalent noise sources for the two sensors. Thermal noise resulting from non-zero series resistances of the transducers are considered in the noise model. The remaining signal processing blocks are considered noiseless in this stage of the design. The resulting expressions therefore represent the best noise result obtainable, and can only be approximated in a real implementation.

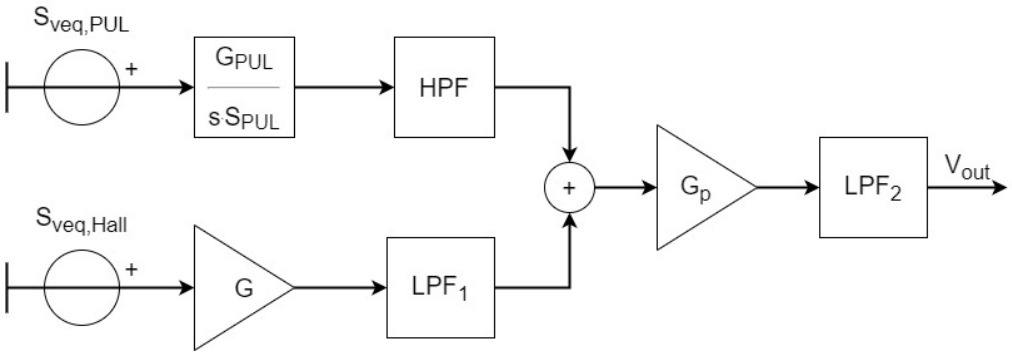


Figure 3.10: Noise Model of concept 1

The noise power spectral density in V^2/Hz resulting from the pick-up loop is:

$$S_{veq,PUL} = 4kTR_s \tag{3.27}$$

The noise power spectral density (voltage) in V^2/Hz resulting from the Hall plate is:

$$S_{veq,Hall} = 4kTR_h \tag{3.28}$$

The noise power spectral density in V^2/Hz at the output of the system is:

$$S_{n,out} = \left[S_{veq,PUL} \left(\frac{2\pi f \tau_{cross}}{2\pi f \tau_{cross} + 1} \frac{1}{S_{PUL}} \right)^2 + S_{veq,Hall} \left(\frac{1}{S_H} \frac{1}{2\pi f \tau_{cross} + 1} \right)^2 \right] \frac{G_{PUL}^2 G_p^2}{1 + 4\pi^2 f^2 \tau_h^2} \tag{3.29}$$

Referred back to the input of the system, using system sensitivity S_s, the noise power spectral density in T^2/Hz:

$$S_{n,out} = \left[S_{veq,PUL} \left(\frac{2\pi f \tau_{cross}}{2\pi f \tau_{cross} + 1} \frac{1}{S_{PUL}} \right)^2 + S_{veq,Hall} \left(\frac{1}{S_H} \frac{1}{2\pi f \tau_{cross} + 1} \right)^2 \right] \frac{1}{1 + 4\pi^2 f^2 \tau_h^2} \tag{3.30}$$

3.4.2. Concept 2: pick-up loop current readout

The second concept uses the short circuit current of the coil as information carrying quantity. For simplicity, it was assumed that the output of the pick-up loop amplifier uses voltage as information carrying quantity. If a current output amplifier type is preferred at a later point in the design, this may be changed. A current to voltage converter block is in this case needed before summation with the Hall path.

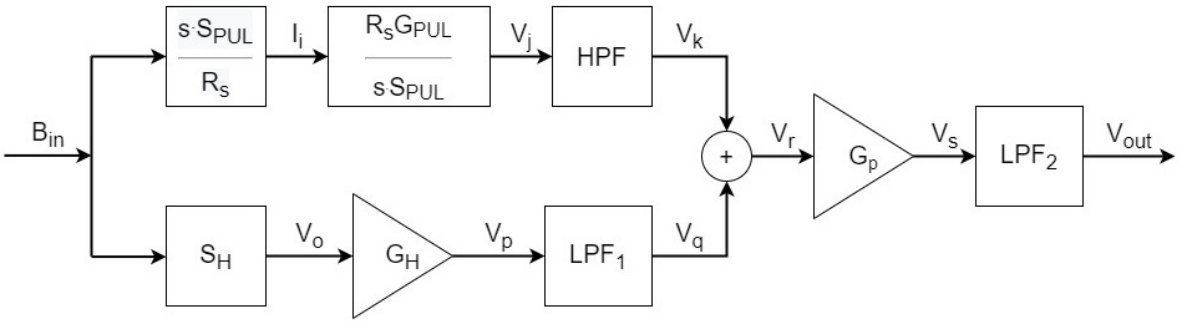


Figure 3.11: Concept 2: A hybrid Hall+pick-up loop sensor system.

On the left side magnetic field $B_i n$ is applied to the system. The signal is converted in to voltage by the two sensors. The sensor sensitivities are represented by S_{PUL} and S_H for the pick-up loop and Hall plate respectively. Considering the pick-up loop path, the voltage after conversion is (assuming the simple pick-up loop circuit model):

$$I_i = s \cdot \frac{S_{PUL} B}{R_s} \tag{3.31}$$

This signal is proportional to frequency. A flat transfer is obtained in the following block that consists of an integrator operation and a gain factor G_{PUL}. After this block the signal is:

$$V_j = G_{PUL} B_{in} \tag{3.32}$$

Now the signal must be filtered to introduce the crossover corner frequency (i.e. high pass corner) with time constant τ_{cross} using the HPF block. The HPF block has transfer:

$$H_{HPF} = \frac{s\tau_{cross}}{s\tau_{cross} + 1} \tag{3.33}$$

The output signal after passing through this filter is:

$$V_k = G_{PUL} B_{in} \frac{s\tau_{cross}}{s\tau_{cross} + 1} \tag{3.34}$$

This signal is fed into a summing block where it is added to the Hall path signal V_q. The Hall path is the same as was described in concept 1. The signal after summing is:

$$V_r = V_k + V_q = B_{in} G_{PUL} \tag{3.35}$$

This signal amplitude is enlarged by the output amplifier with a gain of G_p. Finally, the system bandwidth is limited using a second low-pass filter LPF_2 with transfer function:

$$H_{LPF_2} = \frac{1}{s\tau_h + 1} \tag{3.36}$$

where τ_h represents the time constant of the filter. The filter LPF_2 and output amplifier can be combined to one circuit block. Similarly, the summing block, LPF_1 and HPF_1 can be merged into one circuit block. The source to load transfer H_{C1} of the system is:

$$H_{C1} = \frac{V_{out}}{B_{in}} = \frac{G_p G_{PUL}}{s\tau_h + 1} \tag{3.37}$$

Noise model

Thermal noise resulting from non-zero series resistances of the transducers are considered in the noise model. The remaining signal processing blocks are considered noiseless in this stage of the design. The resulting expressions therefore represent the best noise result obtainable, and can only be approximated in a real implementation.

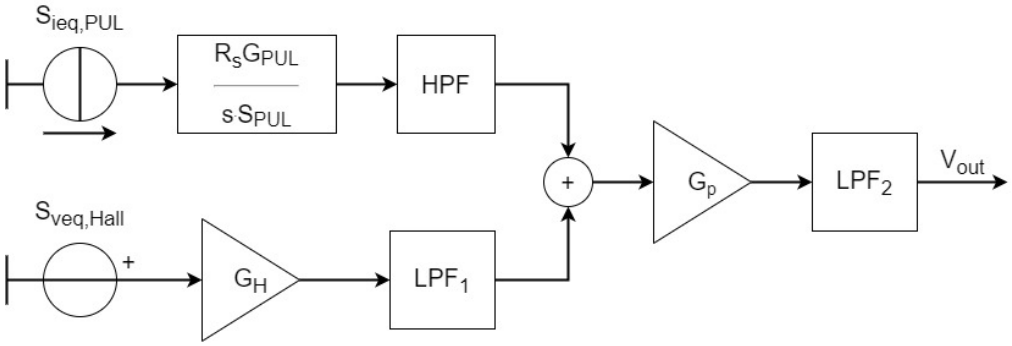


Figure 3.12: Noise Model of concept 2

The noise power spectral density in I^2/Hz resulting from the pick-up loop is:

$$S_{ieq,PUL} = \frac{4kT}{R_s} \tag{3.38}$$

The noise power spectral density (voltage) in V^2/Hz resulting from the Hall plate is:

$$S_{veq,Hall} = 4kTR_h \tag{3.39}$$

The noise power spectral density in V^2/Hz at the output of the system is:

$$S_{n,out} = \left[S_{ieq,PUL} \left(\frac{2\pi f \tau_{cross}}{2\pi f \tau_{cross} + 1} \frac{R_s}{S_{PUL}} \right)^2 + S_{veq,Hall} \left(\frac{1}{S_H} \frac{1}{2\pi f \tau_{cross} + 1} \right)^2 \right] \frac{G_{PUL}^2 G_p^2}{1 + 4\pi^2 f^2 \tau_h^2} \tag{3.40}$$

Referred back to the input of the system, using system sensitivity S_s, the noise power spectral density in T^2/Hz:

$$S_{n,out} = \left[S_{ieq,PUL} \left(\frac{2\pi f \tau_{cross}}{2\pi f \tau_{cross} + 1} \frac{R_s}{S_{PUL}} \right)^2 + S_{veq,Hall} \left(\frac{1}{S_H} \frac{1}{2\pi f \tau_{cross} + 1} \right)^2 \right] \frac{1}{1 + 4\pi^2 f^2 \tau_h^2} \tag{3.41}$$

3.5. Transfer errors

This section describes general transfer errors on system level. These result from errors in the crossover behavior due to small variations in corner frequencies or because of additional poles close to the crossover frequency.

3.5.1. Corner frequency mismatch related gain error

The peak gain error in dB resulting from a mismatch in the time constants of the two sensor paths is found as:

$$\epsilon_{cross}(dB) = 20\log\left(\frac{1}{1 + 2\pi f \tau_{cross} x} + \frac{2\pi f \tau_{cross}}{1 + 2\pi f \tau_{cross}} \right) \approx 20\log\left(\frac{2}{1 + x} \right) \tag{3.42}$$

where x is a constant representing the deviation between the desired τ_{cross} and realized corner frequency of the low-pass filter:

$$x = \frac{\tau_{cross}}{\tau_{LP,realized}} \tag{3.43}$$

This equation can also be used for modeling the impact of an error introduced in the high-pass filter. The error factor x should be substituted by:

$$x = \frac{1}{y} \tag{3.44}$$

where y is a constant represents the deviation in the realized and desired corner frequency of the high-pass filter:

$$y = \frac{\tau_{cross}}{\tau_{HP,realized}} \tag{3.45}$$

The result of the mismatch is a peak (if corner frequencies $f_{PUL} < f_{Hall}$) or dip (if corner frequencies $f_{PUL} > f_{Hall}$) in the magnitude response of the system. The location where this occurs is the average of the realized corner frequencies of the two signal paths.

3.5.2. Additional pole in Hall path

The system transfer shows a gain error if the low pass path introduces a second pole (for example due to finite gain-bandwidth product of the controller). The error is found as:

$$\epsilon_{2ndpole}(dB) = 20\log\left(\frac{1}{(1+2\pi f\tau_{cross})(1+2\pi f\tau_2)} + \frac{2\pi f\tau_{cross}}{1+2\pi f\tau_{cross}}\right) \approx 20\log\left(\frac{\tau_{cross}}{\tau_{cross}+\tau_2}\right) \tag{3.46}$$

where τ_{cross} is the time constant of the crossover network and τ_2 the time constant associated with the undesired second pole(for example introduced by the finite bandwidth of controller in the Hall plate path). Assuming the pole frequency to be greater than the crossover frequency, the resulting transfer will show a dip in magnitude between the target crossover frequency and the frequency of the second pole.

3.5.3. Additional pole in pick-up loop path

Similar to the additional pole mentioned in the previous section, a second pole (and zero) introduced in the pick-up loop path results in a dip in the magnitude transfer (assuming the pole frequency to be lower than the crossover frequency). The error as a result of this additional pole is:

$$\epsilon_{2ndpole\&zero}(dB) \approx 20\log\left(1 - \frac{\tau_{cross}}{\tau_{cross}+\tau_2}\right) \tag{3.47}$$

where τ_2 represents the time constant associated with the second pole. Assuming the pole frequency to be below the crossover frequency, the resulting transfer will show a dip in magnitude between the additional pole frequency and the desired crossover frequency. For example, an additional pole is introduced as a result of finite DC controller gain of the pick-up loop amplifier. The location of this pole is:

$$f_{p2} \approx \frac{S_{PUL-path}}{2\pi S_{PUL} A_v} \tag{3.48}$$

were $S_{PUL-path}$ is the pick-up loop path sensitivity (i.e. the pick-up loop and its amplifier) in V/T and S_{PUL} the sensitivity of the pick-up loop in V/T. To introduce an error <1%, the pole frequency must be a factor 100 below the crossover frequency.

3.6. Pick-up loop path requirements

This section describes a set of derived requirements considering only the pick-up loop path. Equivalently, the design of the pick-up loop and pick-up loop amplifier has the following requirements. In the remaining chapters of this thesis, the design of the pick-up loop path (i.e. the innovative part of the system) will be further worked out. As there is sufficient knowledge of Hall plate systems within the company SystematIC design BV, the Hall plate path will not be worked out further in this thesis.

3.6.1. Functional requirements

Table 3.5: Functional specifications

functionality	description	Comments/notes
1	Amplification	Increasing the available power of the signal
2	Conversion	Change Magnetic field (or current) signal into a proportional voltage signal at the output

3.6.2. Signal processing

Table 3.6: Performance requirements, system level

Req	description	value	unit	verification method	Comments/notes
1	Noise	<33	μT	Spectrum analyzer	RMS, Source referred [1]
2	Bandwidth (-3dB)	>5	MHz	phase-gain analyzer or oscilloscope, compare result with mid-band gain	
3	Sensitivity	100	V/T	Apply known B-field and measure output signal. Compare result with calc.	max output swing / max input signal (Req9/Req4)
4	Signal (max)	8	mT	Oscilloscope (with FFT) or spectrum analyzer	System must no clip / saturate at given input level
5	Offset(T.B.D.)	<10	μT	Measure output voltage with zero current (or field)	differential
6	Full scale error	<1	%	Measure maximum output voltage and compare with calculated maximum signal	use sensitivity and max. signal (Req3 + Req4)
7	Sensitivity error drift	<1	%	Measure maximum output voltage and compare with calculated maximum signal	Over whole Lifetime $T_a = 25°C$
8	Maximum output level	800	mV	voltmeter	$0.2 \cdot 0.8 \cdot VDD(min)$ used for evaluating sensitivity (Req3)

Note 1: This provides the hall path with a noise budget of 50 μT_{RMS}. *Note 2*: The same environmental requirements hold for the pick-up loop path.

3.6.3. Environmental requirements

Table 3.7: Environmental requirements

Req	description	value	unit	verification method	Comments/notes
1	Maximum temperature	150	°C	Climate chamber temperature setting	Better to design for 0 TC
2	Minimum temperature	-55	°C	Climate chamber temperature setting	Better to design for 0 TC
3	Common mode Transient immunity	>25	kV/μs	HV probe + oscilloscope	Voltage step op bus-bar

3.6.4. Cost factors

Table 3.8: Cost factors

Req	description	value	unit	verification method	Comments/notes
1	Minimum supply voltage	3	V	Power supply setting during test	typical supply is 5V
2	Maximum supply voltage	5.5	V	Power supply setting during test	Technology dependent
3	Maximum current consumption	2.0	mA		≈1/5th of total budget.

3.7. Conclusion

A table with requirements as requested by the client is presented in section two. In section three of this chapter, a number of source models were introduced for a pick-up loop and a Hall plate. For both sensors, simplified models and models considering parasitic components were described. The simplified models will be used for designing the in-band frequency response and includes only a series resistance. The models including parasitic components are used for evaluating the stability of the system.

The signal to noise ratio of the pick-up loop is proportional to frequency. The total system noise can be reduced using a pick up loop in the high frequency path by exploiting the increased signal to noise ratio at high frequencies. Two system concepts were introduced in section four and five of this chapter. These two concepts only differ in the information carrying quantity used for the pick-up loop path (current or voltage).

At this point no decision is made whether to use voltage or current in the pick-up loop path. This decision will be made in the next chapter. The remaining chapters of this thesis focuses on designing the pick-up loop path. A set of requirements is derived for this signal path and shown in the sixth subsection. These requirements were derived from the system level requirements provided by the company.

4

Topology design of the pick-up loop Path

4.1. Introduction

This chapter describes the concept design of the pick-up loop signal path. It consists of a pick-up loop and an amplifier for processing the signal. In the first section the pick-up loop modeling and optimization is described. In the remaining sections of this chapter, the concept design of the pick-up loop amplifier is described.

4.2. Pick-up loop design

This section describes the modeling and optimization of the pick-up loop transducer. First, a method for filling the pick-up loop area with wire yielding the highest signal to noise (SNR) ratio is described. Next, a method for determining the inductance and parasitic capacitance of the pick-up loop are introduced. Finally, a circuit model of the pick-up loop is introduced.

The pick-up loop will be constructed as a square planar coil, demonstrated in figure 4.1. The area of the pick-up loop is chosen to be equal to the area occupied by the Hall plate array ($300\mu m \times 300\mu m$). It's expected that a high turn count is beneficial for obtaining a large induced voltage. This would requires thin wire, resulting in a large series resistance and thus a large thermal noise contribution. On the other hand, a low turn count using thick wire would have low series resistance. Therefore it will have low thermal noise contribution, at the cost of a small induced voltage. It is expected that there will be an optimum wire width and turn count. This section describes a method for finding this optimum, where the signal to noise ratio is maximal.

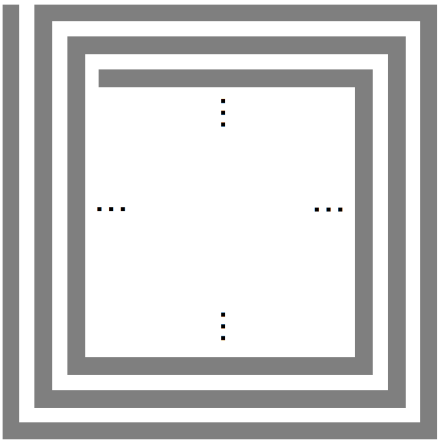


Figure 4.1: Spiraling layout model of the planar pick-up loop

4.2.1. Signal-to-noise ratio optimization

First, a mathematical model is needed, relating the coil layout (wire dimensions, turn count) to the corresponding electric parameters. To simplify the analysis of the pick-up loop layout model, each loop is assumed to be a closed square loop or mesh, demonstrated in figure 4.2. This model will be referred to as the mesh-model. Considering the wire width to be relatively small compared to the side length of the loop, the error introduced by the use of the simplified model is expected to be negligible over a broad range of wire width. For very wide wire, the assumption may introduce a large error. Thus a more accurate model is required if it becomes clear that thick wire is beneficial for the signal-to-noise ratio of the pick-up loop.

The most outer turn is considered to be the first turn. Each consecutive turn is confined within the previous turn, therefore the area enclosed by the consecutive turn is smaller as the area confined by its predecessor. The wire length of the n-th loop considering the mesh-model is found as:

$$l_n = 4\,(d - [(n-1)2(s+w) + w]) \tag{4.1}$$

where n is the turn count, d the side length of the pick-up loop in meters, w the wire width in meters ($w \geq 0.44\mu$m [17]) and s the inter winding distance in meters ($s \geq 0.46\mu$m [17]).

The total wire length of an n-turn pick-up loop is found by summing the length of each individual loop:

$$l_t = \sum_{n=1}^{N} 4\,(d - [(n-1)2(s+w) + w]) \tag{4.2}$$

where N is the maximum turn count to fit within the area. The maximum turn count is found as:

$$N = \frac{d+s}{2(w+s)} \tag{4.3}$$

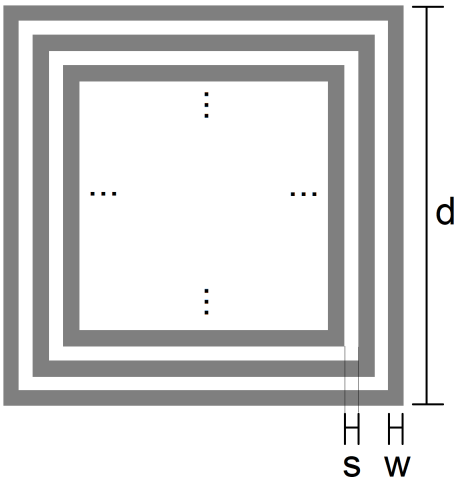


Figure 4.2: The mesh-model: a simplified layout model of the pick-up loop assuming closed loops.

By applying the closed form formula for this type of finite interval summation:

$$\sum_{i=1}^{I} n = \frac{I(I+1)}{2} \tag{4.4}$$

the summation term can be removed from the total wire length expression, resulting in:

$$l_t = 4N\left[(d+2s+w) - (s+w)\,(N+1)\right] \tag{4.5}$$

Similarly, considering the mesh-model again, the area enclosed by the n-th loop is found as:

$$A_n = (d - ((n-1)2(s+w)+w))^2 \tag{4.6}$$

The total area of an n-turn pick-up loop is found by summing the area of each individual loop:

$$A_t = \sum_{n=1}^{N} (d - (2n(s+w)+w))^2 \tag{4.7}$$

It is important to note that A_t represents the product of total area and turn count, thus the total enclosed area. Equivalently, S_{PUL}, the sensitivity of the pick-up loop equals A_t.

By using the closed form formula for this type of finite interval summation:

$$\sum_{i=1}^{I} i^2 = \frac{I(2I+1)(I+1)}{6} \tag{4.8}$$

the summation term can be removed from the total area expression, resulting in:

$$A_t = N\left[(d+2s+w)^2 - 2(N+1)(s+w)\left([d+2s+w] - \frac{1}{3}[s+w][2N+1]\right)\right] \tag{4.9}$$

The spot SNR of the pick-up loop as a function of wire width and turn count is found as:

$$SNR_{PUL} = \frac{V_i^2}{4kTR_{PUL}} \tag{4.10}$$

The series resistance R_{PUL} is found as:

$$R_{PUL} = \left(\frac{R_\square}{w}\right) \cdot l_t \tag{4.11}$$

where $R_\square$ is the square-resistance of the metal interconnect layer ($45m\Omega$ per square [17]).

The induced voltage of the pick up loop can be found using the expression for the total area enclosed by the pick-up loop. Substituting $n \cdot A$ in the induced voltage expression, introduced in chapter 3 (3.1), with expression A_t (4.9) results in an expression for the induced voltage of an N-turn pick-up loop. This expression is found as:

$$V_i = 2\pi f A_t B \tag{4.12}$$

Up to this point it is assumed the pick-up loop area to be fully filled with turns. The most inner turns contribute less to the induced voltage compared to the outer turns. On the other hand, the inner turns do contribute significantly to the total series resistance. This means that the SNR is increasing with turn count up to some point and after this point the SNR decreases. To find the optimum turn count for a given wire width and thus the optimum SNR, the derivative of the symbolic SNR expression 4.10 as a function of turn count is calculated an set equal to zero. This provides the optimum turn count for a given wire width. Next using the optimum turn count, the optimum SNR for a given wire width is calculated using eq. 4.10. The resulting optimal SNR is plotted as a function of the wire width and shown in figure 4.3 as well as the seires resistance, induced voltage and turn count of the pick-up loop model.

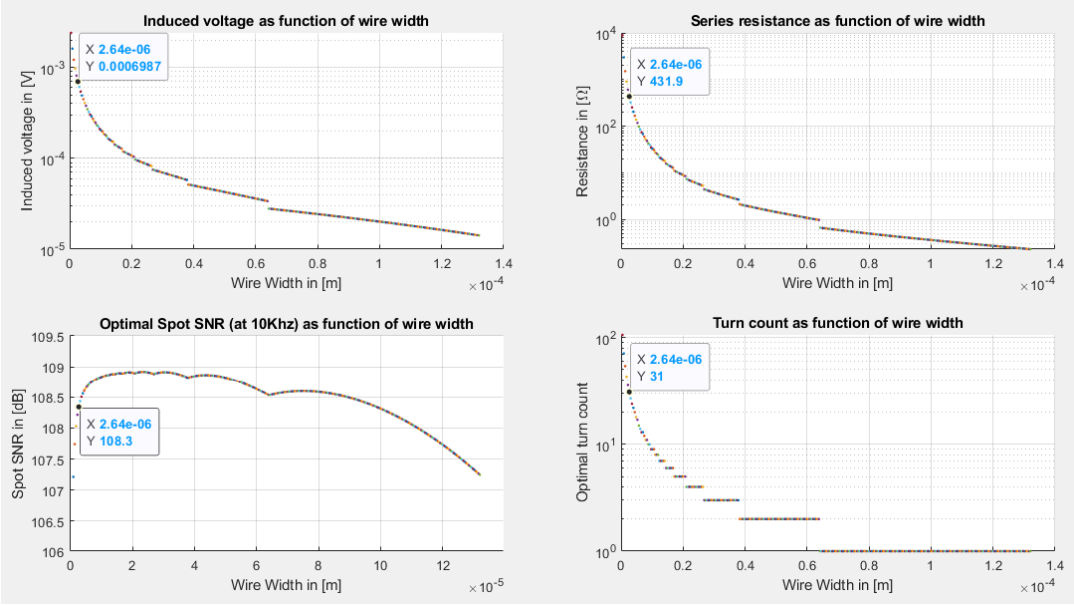


Figure 4.3: The induced voltage, series resistance, spot SNR and turn count as a function of the wire width of the pick-up loop for B = 8 mT.

The upper two sub-graphs in figure 4.3 show the induced voltage and series resistance as a function of the wire width. The bottom sub-graphs show the spot SNR and the maximum turn count as function of wire width. The spot SNR shows a relative weak dependency on the wire width. For 2 μm<w<120 μm the ΔSNR_{spot} is within 1.5 dB. This introduces a degree of freedom to the design of the pick-up loop, as the wire width can be any value within this range, without introducing a large SNR penalty. Therefore the SNR does not introduce motivation for the wire width of the pick-up loop. Next, the bandwidth is considered for motivating the pick-up loop design. This will be done in the next sections, where expressions for the inductance and parasitic capacitance are introduced.

Inductance and parasitic capacitance

In the previous section, the mesh-model for the pick-up loop was introduced. Parametric equations for the induced voltage, series resistance and spot SNR as a function of wire width were derived. The resulting expressions for the SNR did not provide motivation for the wire width (and thus turn count) of the pick-up loop design. In this section expressions for the inductance and parasitic capacitance are derived. These will provide information over the bandwidth of the pick-up loop and might provide motivation for the design. Applying the Wheeler inductance calculations for planar coils, the inductance of the pick-up loop is found as [43]:

$$L = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho} \tag{4.13}$$

where $K_1 = 2.34$, $K_2 = 2.75$ are constants, d_{avg} is the average distance or side length of a single loop and ρ the fill factor.

By using the optimum turn count, the average distance of a single mesh of the pick up loop is now no longer half the outer distance. The average distance, considering the optimum turn count, is found as [43]:

$$d_{avg} = d - d_{in} \tag{4.14}$$

where d (introduced in section 4.2.1, 300 μm) is the outer side length of the first loop and d_{in} the side length of the final (most inner) loop.

The fill factor ρ is found as [43]:

$$\rho = \frac{d_{avg}}{d + d_{in}} \tag{4.15}$$

The loop-to-substrate capacitance C_p (parallel capacitance) is modeled as a parallel plate capacitor, its value is found as:

$$C_p = \frac{\epsilon_a l_t w}{t_{ox}} \tag{4.16}$$

were t_{ox} is the oxide thickness and $\epsilon_a = \epsilon_0 \epsilon_r$ (SiO2) the oxide permeability.

The inter-winding capacitance, or distributed capacitance, C_d is approximated as [44]:

$$C_d = \sum_{n=1}^{N} \frac{1}{4} C_{mm} l_n [a(n+1) - a(n-1)]^2 \tag{4.17}$$

were l_n is the length of the n-th turn, $a(n) \equiv \frac{l_1 + l_2 + ... + l_{n-1} + l_n}{l_t}$ and C_{mm} is the inter winding capacitance per unit length. Its value is found as:

$$C_{mm} = \frac{\epsilon_a h}{s} \tag{4.18}$$

were h is the height of the metal layer used for the pick-up loop.

At this point, expressions for the pick up loop series resistance, series inductance, distributed capacitance and parallel capacitance are described. In the next section, these parameters are used to obtain a circuit model resembling the dynamic behavior of a pick-up loop. From this model, the expected bandwidth of the pick-up loop can be derived.

4.2.2. Circuit model of the loop

In the previous sections expressions for the pick up loop series resistance, series inductance, distributed capacitance and parallel capacitance were introduced. In this section these parameters will be used to derive a equivalent circuit model. This model will provide information about the maximum bandwidth obtainable. A circuit model closely approximating the pick-up loop would be a distributed network, consisting of a voltage source, a series inductance and resistance as well as two parasitic capacitance's (inter-winding and substrate) for each individual turn, indicated in figure 4.4.

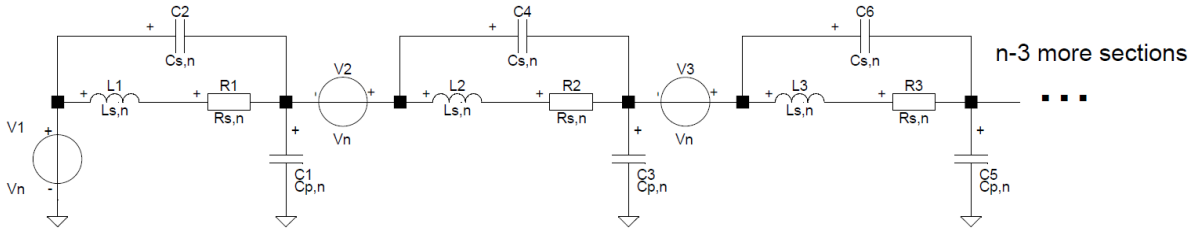


Figure 4.4: Distributed circuit model of the pick-up loop

This model would be very impractical for (hand) calculations. A more practical alternative is to use a lumped model, where all the individual elements are confined to a single voltage source, series inductance, series resistance, series capacitance, and parallel capacitance, indicated in figure 4.5.

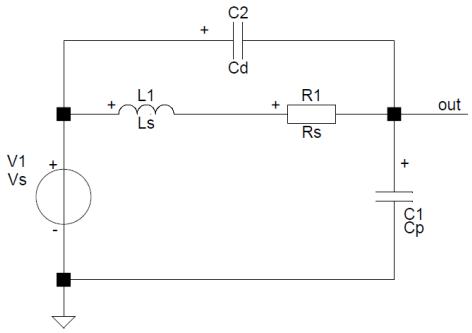


Figure 4.5: Lumped circuit model of the pick-up loop

To verify the accuracy of this model, the lumped model and the distributed model must be compared. This will be discussed at a later point in this chapter, after a decision is made on the wire width. For now, it is assumed that the lumped model is sufficiently accurate. The bandwidth is therefore verified using the worst-case parameter set, assuming the highest turn count (thus large resistance, inductance and capacitance). The resulting circuit model and frequency response are shown in figure 4.6. The -3 dB bandwidth obtained is 28 MHz, compared to a requirement of 5 MHz.

The bandwidth of a pick-up loop is found to be sufficiently large when considering the the thinnest wire available. The use of thicker wire will provide a lower series resistance, series inductance, series capacitance and parallel capacitance, and thus a larger bandwidth. Therefore the bandwidth of the pick up loop, as a result of wire width and turn count does not provide motivation for a specific wire width. Next, the power consumption of the controller will be considered for motivating the design. First a suitable feedback amplifier concept is needed to provide more details about this amplifier. This is described in the following sections. After this, the power consumption is considered for motivating the design of the pick-up loop in section 4.3.6.

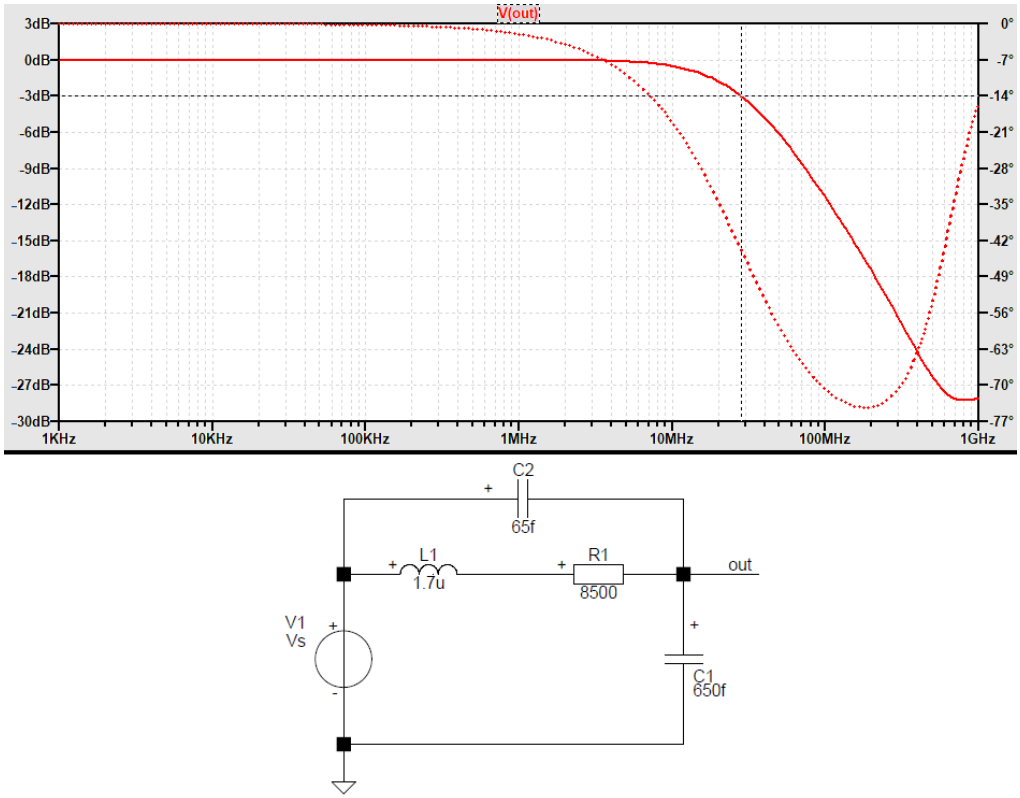


Figure 4.6: Top: frequency and phase response of the lumped pick-up loop model assuming the worst case parameter set. The corner frequency is located at 28 MHz Bottom: circuit model used for verifying the bandwidth.

4.3. Pick-up loop amplifier topology design

This section describes the concept design of the pick-up loop amplifier. The pick-up loop amplifier performs two main tasks:

- It integrates the frequency dependent input signal resulting in a flat frequency response
- It provides gain to obtain an increase in available power of the signal

4.3.1. Ideal source-to-load transfer of pick-up loop amplifier

This section describes the ideal transfer of the pick up loop amplifier. The magnetic field-to-voltage transfer of the pick-up loop is found as:

$$H_{PUL}(s) = \frac{V_s}{B} = sS_{PUL} \tag{4.19}$$

where S_{PUL} represents the pick-up loop sensitivity, found in section 4.2.1 as:

$$S_{PUL} = A_t \tag{4.20}$$

where A_t represents the product of the pick-up loop area in square meters and the pick-up loop turn count. The amplitude of the induced voltage is thus depending on the amplitude and frequency of the magnetic field. A flat frequency response is required at the output of the pick-up loop pick-up loop amplifier. The required transfer of the pick-up loop amplifier to obtain a flat frequency response at the output is found by taking the inverse of the magnetic field to induced voltage expression H_{PUL}. This transfer is found as:

$$H_{amplifier}(s) = \frac{V_s}{B} = \frac{1}{sS_{PUL}} \tag{4.21}$$

From this expression it follows that an amplifier having an integrating transfer is required. The integration operation is preferred to be executed as early as possible in the pick-up loop path, in order to limit the

signal swing for high frequencies. At this point, both input and output information carrying quantity (current and/or voltage) are undetermined. Therefore a set of four possible solutions exist: voltage-to-voltage, voltage-to-current, current-to-voltage and current-to-current. In the next subsections, concepts for all these four possible combinations are introduced. Each amplifier type is analyzed and tested for 'show-stoppers' [45]. In the end, one concept was considered feasible for the application. This concept will be elaborated in more detail.

4.3.2. Pick-up loop amplifier concept 1: V-to-I

The pick-up loop amplifier can be implemented as a transconductance feedback amplifier with an inductor as feedback element, demonstrated in figure 4.7. This results in a inverting voltage to current integrator.

The transfer function of this feedback amplifier concept is found as:

$$H(s) = \frac{I_{out}}{V_s} = -\frac{1}{sL_{fb}} \tag{4.22}$$

The magnetic field to current transfer function of the pick-up loop and amplifier is found as:

$$H(s) = \frac{I_{out}}{B} = -\frac{A_t}{L_{fb}} \tag{4.23}$$

This is a constant (flat) transfer function versus frequency. This concept does not require any pre- or post-filtering, minimizing the complexity and chip area of this concept.

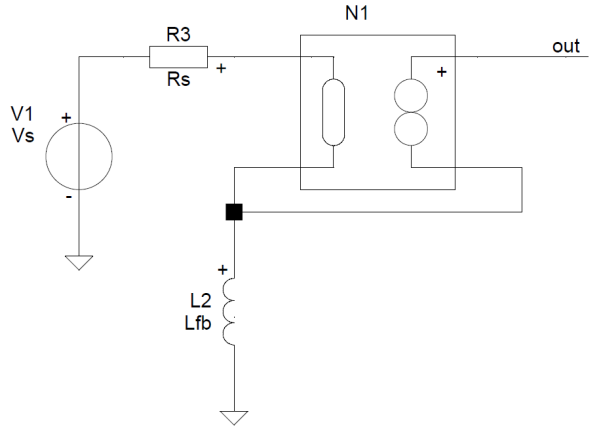


Figure 4.7: Integrating voltage-to-current amplifier pick-up loop amplifier

Considering actual on-chip inductors, it is difficult to obtain a low series resistance compared to the inductance (i.e. high quality factor). The transfer function including series resistance is found as:

$$H(s) = \frac{I_{out}}{B} = -\frac{sA_t}{sL_{fb} + R} \tag{4.24}$$

Figure 4.8 illustrates the effect on the transfer of the pick-up loop and amplifier considering a series resistance of the feedback inductor. For high frequencies, where $R >> 2\pi f L_{fb}$, the amplifier behaves as an integrator, thus providing a flat frequency transfer at the output.

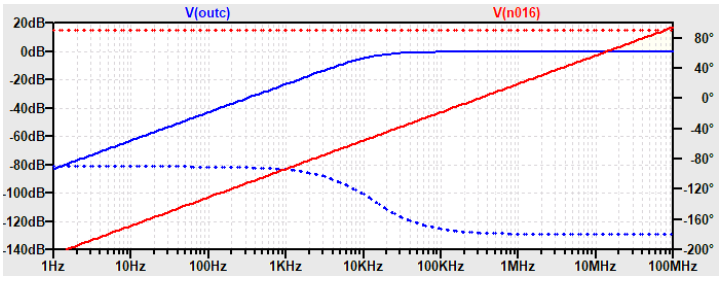


Figure 4.8: Resulting frequency response of the pick-up loop amplifier and the pick up loop, assuming a series resistance of only 1 mΩ and 15 nH inductance. The resulting source-to-load frequency response (blue) of the amplifier and the frequency response of the source (red).

Conclusion

This concept is not feasible given the poor quality (i.e. large series resistance compared to inductance) of on-chip inductors.

4.3.3. Pick-up loop amplifier concept 2: I-to-I

The pick-up loop amplifier can be implemented as a current-to-current amplifier with a frequency dependent feedback network, demonstrated in figure 4.9. The resulting circuit concept behaves as an integrator for low frequencies (where $1 >> 2\pi f C_1 R_1$). The transfer function is found as:

The current to current transfer function of this feedback amplifier concept is found as:

$$H(s) = \frac{I_{out}}{I_s} = 1 + \frac{1}{sC_1R_1} = \frac{sC_1R_1 + 1}{sC_1R_1} \tag{4.25}$$

At high frequency (where $1 << 2\pi f C_1 R_1$), the gain becomes unity, due to an unwanted zero in the transfer function.

This can be solved by placing a pole at the zero location, using an input filter. Placing a capacitor at the input to implement a filter using the series resistance of the pick-up loop is not effective due to the feedback configuration (The voltage at the input port is forced to 0). A filter at the output is also not preferred, as this would require the amplifier a very large signal at high frequencies.

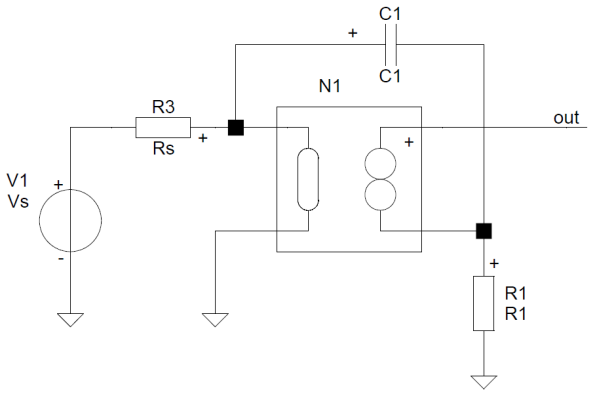


Figure 4.9: Current-to-current amplifier pick-up loop amplifier

Conclusion

This concept is not feasible due to the difficulties with implementing a filter to cancel the zero introduced in the feedback network.

4.3.4. Pick-up loop amplifier concept 3: I-to-V

The pick-up loop amplifier can be implemented as a transimpedance amplifier with a capacitor as feedback element, demonstrated in figure 4.10. This results in a inverting current to voltage integrator.

The current to voltage transfer-function of this feedback amplifier concept is found as:

$$H(s) = \frac{V_{out}}{I_s} = -\frac{1}{sC_{fb}} \tag{4.26}$$

The source current as a result of source voltage V_s is found as:

$$I_s = \frac{V_s}{R_s} \tag{4.27}$$

Substituting this equation into the amplifier transfer-function, the total magnetic field to voltage transfer-function of the system is found as:

$$H(s) = \frac{V_{out}}{B} = -\frac{A_t}{C_{fb}R_s} \tag{4.28}$$

This is a frequency independent transfer. This does not require any pre- or post-filtering, reducing the complexity and area consumption of this concept.

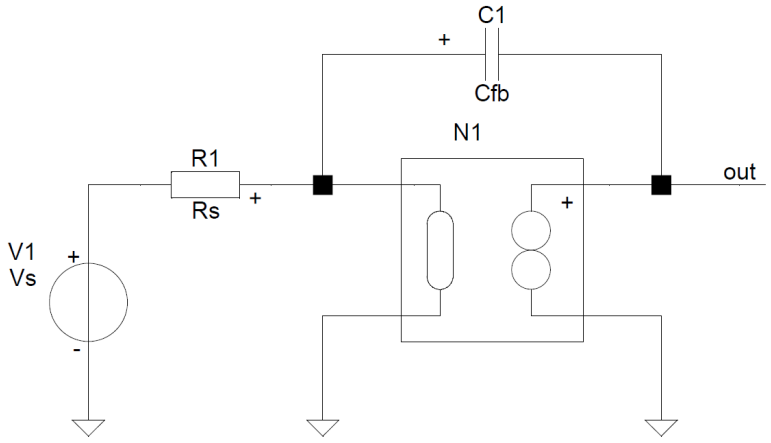


Figure 4.10: Current-to-voltage amplifier pick-up loop amplifier

Differential circuit

The pick-up loop path will be implemented as a differential circuit. This is done to provide rejection of (unwanted) common mode signals, injected into the source circuit by capacitive coupling between the magnetic field source and pick-up loop. A differential version of the amplifier concept is demonstrated in figure 4.11 with the common mode-signal source and coupling included. A common mode signal presented at the input of the amplifier couples via the feedback impedance's directly to the output. Equivalently, the common mode gain equals one. In order to reduce the common mode transfer, attenuation of the common mode signal is used. This can be done both at the input or output of the amplifier. Attenuation at the output node seems beneficial as this will provide less deterioration of the signal to noise ratio. The attenuation is realized using capacitors C_3 and C_4 having a value of C_{cm}. The coupling between the magnetic field source and pick-up loop is expected to be about 1 fF [17], figure 4.11 demonstrates the common mode source (V2) and coupling (C6 and C5). The voltage step is expected to have an amplitude of 1kV and a rise time of 40ns. For 100 dB attenuation of the common mode step, C_{cm} needs to be 100 pF. This large capacitor would require a large chip area and increases the output drive requirement of the controller.

Conclusion

This amplifier concept provides the desired integrating transfer. But realizing the relative large output capacitors for attenuation of the common mode-input step makes it a costly (area and power) solution.

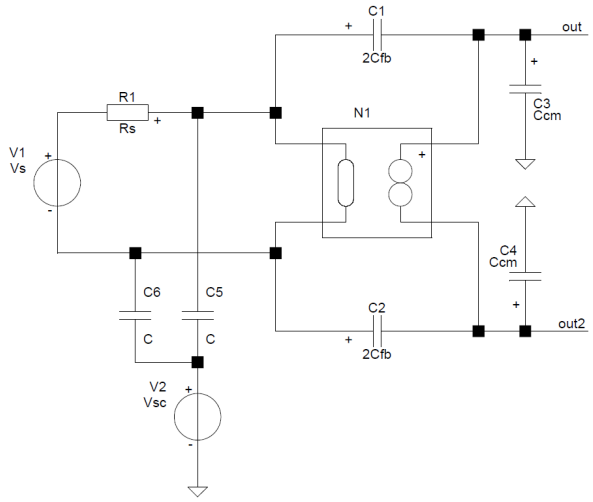


Figure 4.11: Differential current to voltage integrator concept with the common mode source and coupling modeled using voltage source V2, capacitor C6 and C5

4.3.5. Pick-up loop amplifier concept 4: V-to-V

The pick-up loop amplifier can be implemented as a non-inverting integrator, derived from the voltage-to-voltage feedback amplifier.

The transfer function of this feedback amplifier concept is found as:

$$H(s) = \frac{V_{out}}{V_s} = \left(\frac{1}{s(C_f + C_p)R_s + 1}\right)\left(1 + \frac{1}{sC_1R_1}\right) = \left(\frac{sC_1R_1 + 1}{s(C_f + C_p)R_s + 1}\right)\left(\frac{1}{sC_1R_1}\right) \tag{4.29}$$

where C_p is the oxide capacitance (or parallel capacitance) of the pick-up loop, C_f the added filter capacitance. From a matching point of view, the capacitor in the feedback network is set to the same value as the filter capacitance in parallel to the pick-up loop. By substituting $(C_f + C_p) = C_1$ and $Rs = R1$ the expression reduces to:

$$H(s) = \frac{1}{sC_1R_1} \tag{4.30}$$

The total magnetic field to voltage transfer-function of the pick-up loop and amplifier is found as:

$$H(s) = \frac{V_{out}}{B} = \frac{A_t}{C_1R_1} \tag{4.31}$$

This is a constant (flat) transfer over frequency.

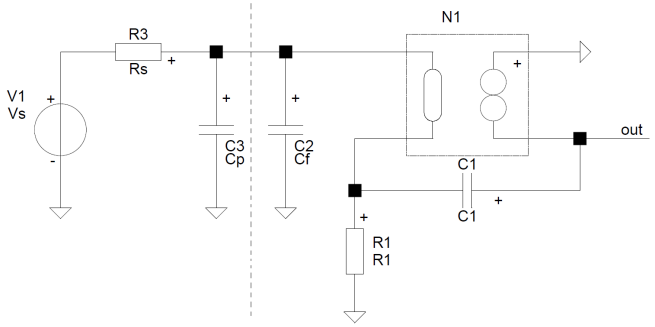


Figure 4.12: Voltage-to-voltage amplifier pick-up loop amplifier

Differential circuit

Figure 4.13 shows the differential version of the pick-up loop amplifier concept. The differential mode (voltage) source-to-load transfer is the same as the single ended circuit discussed before. If the circuit is perfectly balanced, thus being constructed of perfectly matched components, there is no transfer of differential mode to common mode signals. If there is some unbalance in the circuit, the differential-to-common mode source-to-load transfer is non-zero. Also this circuit has no direct path to the output via the feedback network. As a result it has a high common-mode rejection ratio.

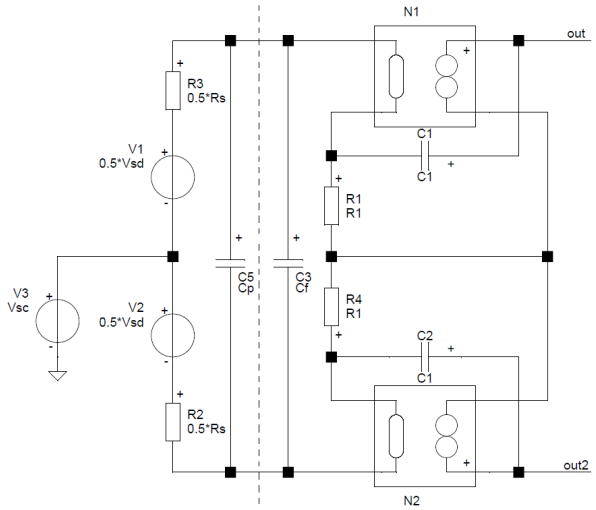


Figure 4.13: Differential Voltage-input concept 3

Conclusion

This concept provides the desired integrating transfer. The differential version of this circuit concept has good common mode immunity without the need of additional circuits, as seen with the current-to-voltage integrator. Therefore it seems the most promising pick-up loop amplifier concept.

4.3.6. Power consumption considerations

The total noise budget for the pick-up loop signal path was introduced in section 3.6.1. The noise budget for the pick-up path was set to 33 μT_{RMS} source referred. This provides the Hall plate path with a remaining budget of $50\mu T_{RMS}$.The pick-up loop path will contain 3 main noise sources: the signal source, the feedback network and the controller, demonstrated in figure 4.14. The total source referred noise in V/T is approximated as:

$$S_{tot} \approx \left(\frac{1}{2\pi f S_{PUL}}\right)^2 \left(4kTR_s + 4kTR_1 + S_{eq}\right) \tag{4.32}$$

where S_{eq} resembles the total noise contribution of the controller. The noise contribution of the source results from the series resistance R_s of the pick-up loop. Making the series resistance low would thus result in a low noise contribution. The same holds for the resistor in the feedback network: a low resistor value will yield a low noise contribution. Reducing the feedback resistance has a major drawback: a low feedback-network impedance will require more power to be supplied by the output stage. This also requires large area, as the feedback capacitor needs to be big. Alternatively: low power requires a high feedback resistor value. Another disadvantage of a pick-up loop with low resistance is the low induced voltage, thus large gain requirement.

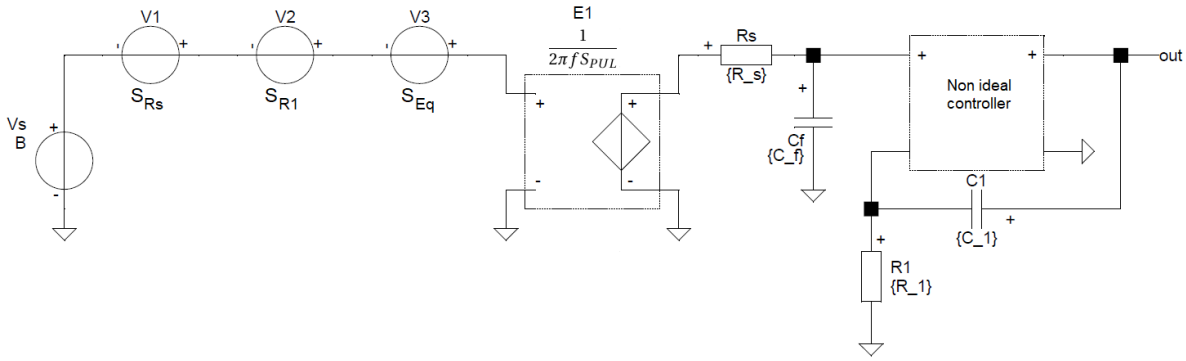


Figure 4.14: Simple noise model of the feedback amplifier, assuming a non ideal controller with noise. All noise contributions are referred to the magnetic field source V_s.

First, lets consider the chosen amplifier type with the largest source resistance. For $R_s = 8500\Omega$, the total thermal noise contribution resulting from the 2 resistors (assuming $R_1 = R_s$) will be 27 μT_{RMS} source referred. This would leave a relatively small noise budget for a controller design ($19\mu T_{RMS}$). A low-noise controller design requires large transistors (area) and large quiescent current (power) resulting in high cost. Thus it seems beneficial to assign the largest part of the noise budget to the controller, and make the feedback network and source have a minimal (close to negligible) contribution, without making them arbitrary low as this would require a larger drive current to be supplied by the output stage. It is expected that $R_1 = R_s$ will approximate the optimum ratio for obtaining low power.

Noise source S_{eq} results predominantly from the controller. It will be a multi stage design with a common source input stage. The drain current noise of this input stage can be approximated as:

$$S_{I_d} = 4kTn\Gamma g_m \left(1 + \frac{f_l}{f}\right) \tag{4.33}$$

This noise contribution can be transformed to the source using the T1 parameters of a CS stage:

$$B = \frac{-j\omega}{\omega_T} \text{ and } D = \frac{-1}{gm} \tag{4.34}$$

The resulting noise expression is the so called 'gate induced' noise. Assuming $R_1 = R_s$, the total source referred noise power spectral density (voltage) is found as:

$$S_{v_{in}} = 4kT\left[2R_s + n\Gamma g_m \left(\frac{1}{g_m^2} + \frac{f^2}{f_T^2}\right)\left(1 - \frac{f_l}{f}\right)\right] \tag{4.35}$$

The signal band of interest is assumed to be well below the f_T ($f << f_T$) of the MOSFET, the expression reduces to:

$$S_{v_{in}} \approx 4kT\left[2R_s + \frac{n\Gamma}{g_m}\left(1 - \frac{f_l}{f}\right)\right] \tag{4.36}$$

By assuming the signal bandwidth to be above the $1/f$-corner frequency f_l, this expression is reduced to:

$$S_{v_{in}} \approx 4kT\left(2R_s + \frac{n\Gamma}{g_m}\right) \tag{4.37}$$

$$S_{v_{in,MOS}} \approx \frac{4kTn\Gamma}{g_m} \tag{4.38}$$

Where Γ represents the noise parameter, n the substrate factor and g_m the transconductance of the MOS-device. Assuming short-channel devices, $n\Gamma \approx 2$.

By solving $S_{v_{in,MOS}} = S_{v_{loop}}$, thus fixing the thermal noise component of the MOSFET to be equal to the noise resulting from the source model, a first approximation of the required transconductance is found:

$$g_m \approx \frac{1}{R_s} \tag{4.39}$$

For a low thermal noise contribution, a short transistor operating in moderate inversion is required [46]. In this operating region, the gm-efficiency ($\eta_{g_m} = \frac{g_m}{I_D}$) is high, the intrinsic voltage gain is high and the gate-referred thermal noise voltage is low. Assuming operation in moderate inversion provides an estimated quiescent drain current of:

$$I_D \approx \frac{1}{\eta_{g_m} R_s} \tag{4.40}$$

Analyzing this expression indicates that a large source resistance seems beneficial for a low current consumption of the pick-up loop amplifier input stage.

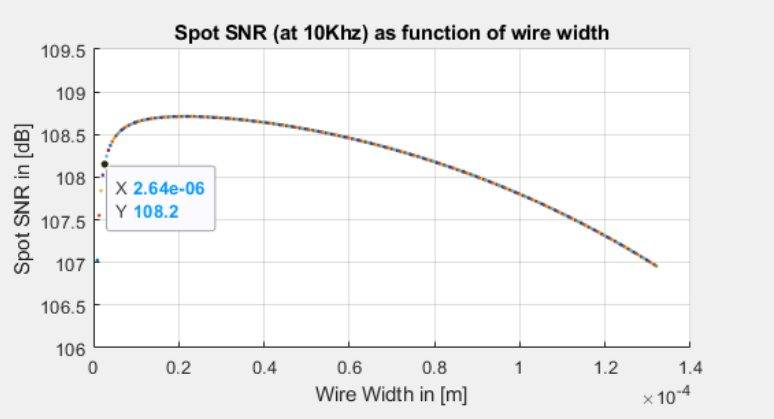


Figure 4.15: SNR as a function of the wire width

By choosing the wire width just left to where the optimum SNR occurs in figure 4.15, a low noise contribution of the source and feedback resistor is obtained. At the same time this provides a large noise budget for the controller, thus low power consumption. The wire width is chosen to be $2.6\mu m$ and the series resistance of the pick-up loop assuming this wire width is 440Ω.

The resulting subdivision of the noise budgets is demonstrated in table 4.1

Table 4.1

source	value	unit
Controller	32	$\mu T(RMS)$
Source	4.4	$\mu T(RMS)$
Feedback network	4.4	$\mu T(RMS)$

4.3.7. Pick-up loop parameters

In the previous section a decision was made about the wire width resulting in a parameter set for the pick-up loop design. From the wire width, all other pick-up loop parameters can be found. In figure 4.16 the resulting graphs for the inductance, wire length, SNR_{PUL} compared to SNR_{Hall}, filled pick-up loop area, enclosed area A_t and parasitic capacitance as a function of the turn count are shown. In table 4.2 a complete overview of all pick-up loop parameters is presented.

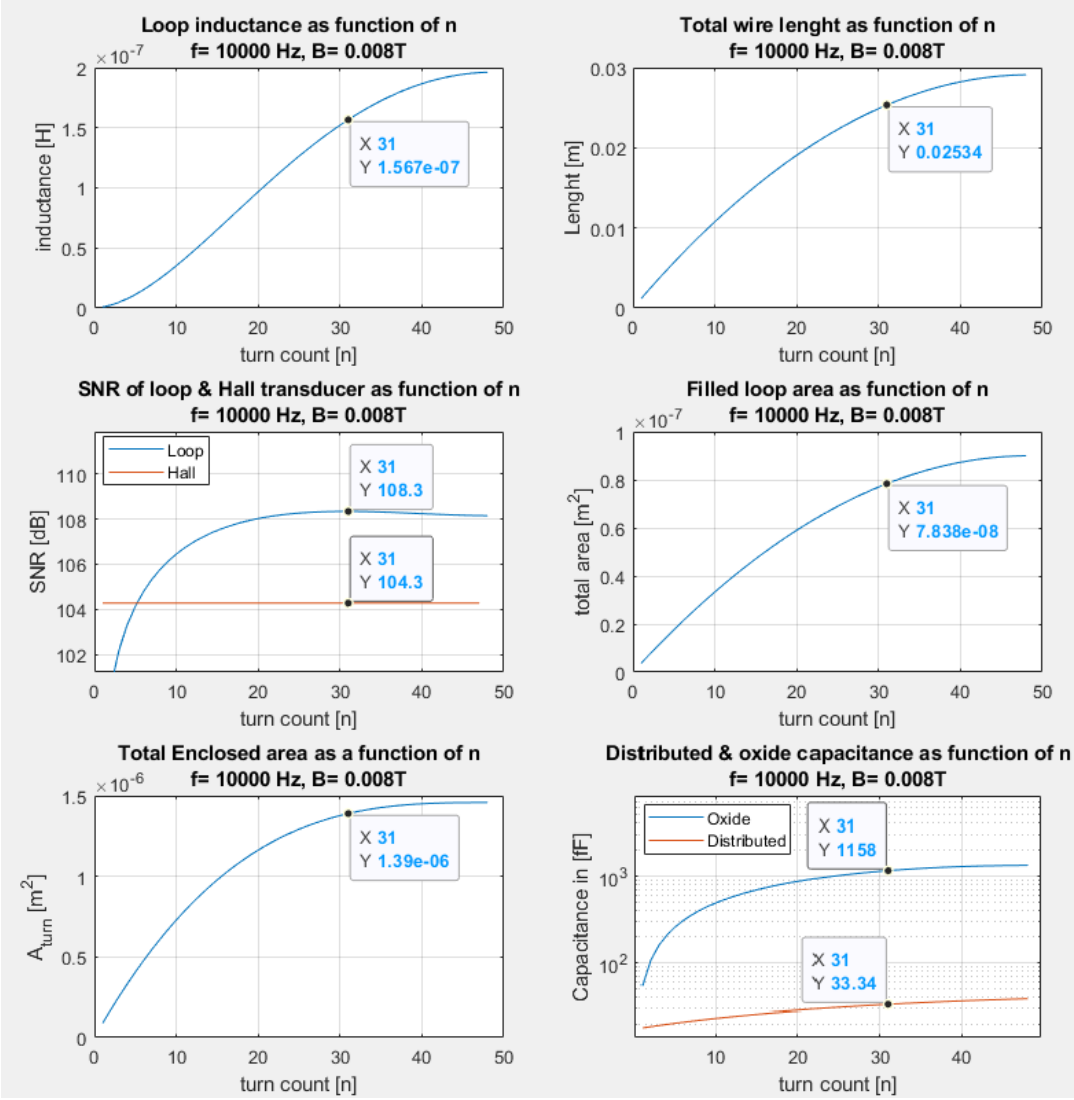


Figure 4.16: Coil parameters as a function of the turn count

The resulting turn count is 31. In all the previous pick-up loop parameter graphs (4.3, **??** and 4.16) this point, for a turn count of 31 or a wire width of 2.64μm, is indicated with a cursor.

Table 4.2: Pick-up loop parameters

Parameter	**Value**	**Unit**	**Notes**
Outer dimensions	300 × 300	μm ×μm	Matlab sim.
Wire width	2.64	μm	[17]
Wire thickness	0.52	μm	[17]
Wire spacing	0.46	μm	[17]
Oxide thickness	2	μm	[17]
Turn count	31	-	Matlab sim.
Sensitivity	$8.73 \cdot f$	uV·Hz·T^{-1}	Matlab sim.
Self inductance	157	nH	Matlab sim. [43]
Series resistance	440	Ω	Matlab sim.
Open square area	108 × 108	μm × μm	Matlab sim. [43]
Capacitance to substrate	1550	fF	Matlab sim. (Approximation)
Parallel capacitance	33	fF	Matlab sim. (Approximation)

4.3.8. Pick-up loop amplifier parameters

After the design of the pick-up loop, the components of the feedback network can be determined. The resulting values are shown in table 4.3

Table 4.3: Back-of-the-envelope calculation results

	Value	Unit	Note
C1	31.59	pF	
R1	440	Ω	
Cf	30.395	pF	Forms parallel circuit with C_p for total of 31.59pF
DC controller gain	210k	V:V	To meet LF-corner freq. req.
Source-to-load transfer	$\frac{1}{sR_1C_1}$	$\frac{V_{out}}{V_s}$	

4.3.9. Circuit model verification

As indicated in section 4.2.2, the lumped and distributed circuit model of the pick up loop must be compared to validate the model accuracy within the band of interest. The two models were compared in a circuit simulator using the parameters listed in the previous section. The resulting models show similar behavior up to 100Mhz, indicated in figure 4.17.

After this point, the lumped model shows some deviation from the distributed model. Luckily, this is well above the band (high-pass corner will be derived in next section up to 5 Mhz) of interest. Therefore the lumped model provides sufficient accuracy for designing the system, as well as for signals (i.e. disturbances) just above the band of interest. For design of the in-band signal transfer of the system, the model can be simplified further, resulting in the model shown in figure 4.18. Here all network elements, except the series resistance and voltage source, are left out. For analyzing the stability of the amplifier, the lumped source model is used.

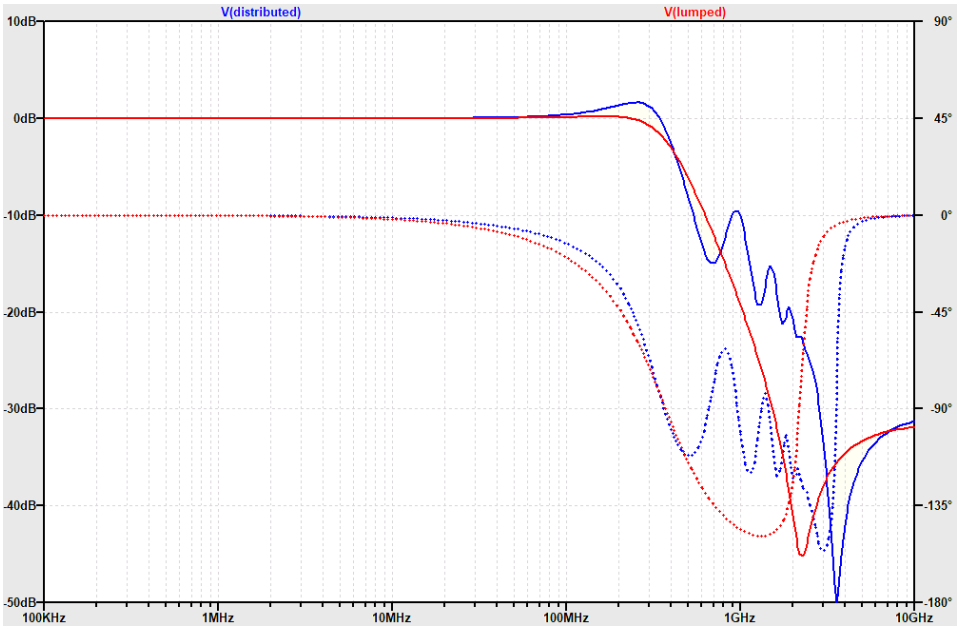


Figure 4.17: Lumped (red line) model compared to a distributed (blue line) coil model

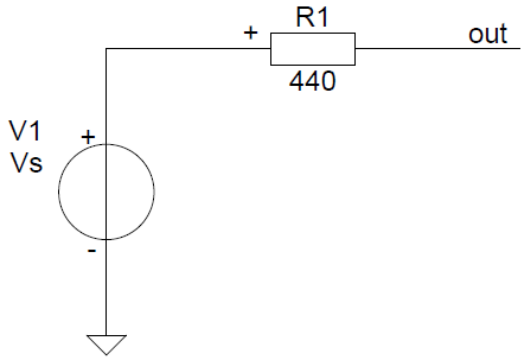


Figure 4.18: Simplified source model

4.4. Crossover frequency

This section describes the load circuit of the amplifier. After the pick-up loop amplifier a circuit for combining the signals resulting from the pick-up loop and Hall plates must be combined (i.e. integrated). This circuit will therefore load the output of the pick-up loop amplifier. The integration of the two signal paths to one can be done using an analog RC-filter. This is the most obvious solution for now, it might not be the most area or power efficient solution, but optimization of this block may be done at a later time. The same holds for the decision to use voltage as information carrying quantity in this filter section. For now it is chosen without direct motivation, but the most optimal solution will need to be investigated at a later point in time. The high-frequency path will be coupled using capacitor and the low frequency path using a resistor to a single summing node. First the optimal crossover frequency is determined. Next an implementation for the filter is described. The optimal crossover frequency is found using the spot signal-to-noise ratio expressions of the the two sensors, introduced in section 3.3.

The optimal crossover frequency is found by solving $SNR_{Hall} = SNR_{Loop}$ for the frequency f_{cross}:

$$f_{cross} \geq \frac{S_H}{2\pi A_t} \cdot \sqrt{\frac{R_L}{R_H}} \tag{4.41}$$

this provides the minimum frequency to obtain an improved SNR compared to a Hall plate system. Figure 4.19 shows a plot with the optimal crossover frequency as a function of the wire width.

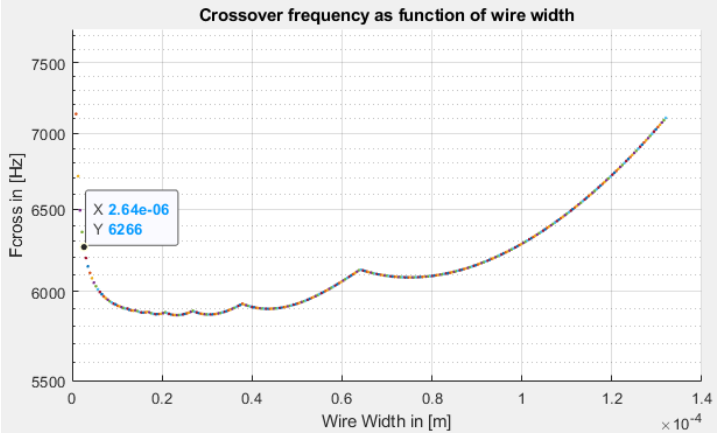


Figure 4.19: Optimal crossover frequency as a function of wire width

From this figure, the optimal crossover frequency is found to be greater or equal to $6300Hz$. This corresponds to a maximum time constant of:

$$\tau_{cross} = \frac{1}{2\pi f_{cross}} = 25.26\mu s \tag{4.42}$$

The CMOS process provides square resistance and capacitance as [17]:

$$\begin{aligned} R_{\square} &= 400\frac{\Omega}{\mu m^2} \\ C_{\square} &= 1\frac{fF}{\mu m^2} \end{aligned} \tag{4.43}$$

For a minimum area filter, the area consumption of the resistor will equal the area of the capacitor. By multiplying the square resistance and capacitance, the time constant of a unit RC filter is found as:

$$\tau_{\square} = R_{\square}C_{\square} = 0.4ps \tag{4.44}$$

The minimum number of unit-size squares, denoted as $N_{\square}$ required for realizing the capacitor or resistor is found as:

$$N_{\square} = \sqrt{\frac{\tau_{cross}}{\tau_{\square}}} = 7947 \tag{4.45}$$

Equivalently, both capacitor and resistor each have an area of 7947 μm^2. The minimum area of the filter is $15894\mu m^2$. In table 4.4 the accompanying values of the resistor and capacitor are listed.

Table 4.4: Crossover-filter parameters

	Value	**Unit**	**Area** (μm^2)	**notes**
f_{cross}	6.3	kHz	-	6266 Hz calculated
R_{load}	3.18	MΩ	7950	3178800Ω calculated
C_{load}	7.95	pF	7947	

4.5. Conclusion

This chapter describes the design of the pick-up loop and the choice for an dedicated amplifier topology. The pick-up loop model shows that the spot SNR of the pick-up loop is weakly dependent on wire width over a broad range of widths. Therefore, the bandwidth of the pick-up loop was considered. Again, no direct motivation for making a design choice was found. Finally, the power consumption of the amplifier was considered for motivating the pick-up loop design. Here it became clear that a relative high source resistance is beneficial for the total power consumption of the amplifier. But picking the highest possible value would not leave much room in the noise budget for the controller circuit. Therefore a moderately high value was chosen, providing almost negligible noise contribution by the source and enabling a low-power controller design. In the sections 4.3 concepts for the pick-up loop feedback amplifier were compared. In the end the most promising concept is a non-inverting integrator. Finally the design of the optimal crossover frequency was described. A preliminary circuit for integrating the signal paths was described, implementing the desired crossover frequency. This resembles also the load circuit of the amplifier.

5

Pick-up loop amplifier design

5.1. Introduction

This chapter describes the design of the pick-up loop amplifier. In the previous chapter the design of the pick-up loop was finalized and a topology for the pick-up loop amplifier was chosen. Also the design of a (provisionally) crossover circuit was described, as this will resemble the load of the amplifier. In this chapter this amplifier topology will be further elaborated.

The design described in this chapter will be a single ended design. This reduces the design complexity. In the near future a differential version will be designed, but this is outside the scope of this project. For a differential circuit two controllers will be used. The controller design will need no major modification. The biasing for the differential amplifier is different, and must be partly redone.

In the first section the design of the amplifier topology chosen in the previous chapter is worked out in more detail. The second section describes the design of an input stage to meet the noise requirement. The design of a dedicated output stage design to fulfill the load drive requirements is described in the third section. This is followed by a section describing the design of the mid-band accuracy. After these steps the design was tested for stability. The circuit model showed unstable behavior thus frequency compensation is required. This will be described in two separate sections.The second to last section describes the design of the biasing concept and its implementation. Finally the results obtained from simulating the amplifier design are described in the last section.

5.2. Amplifier topology

In the previous chapter the decision was made to use a non-inverting integrator, derived from the voltage-to-voltage type of amplifier. This amplifier can be subdivided into a feedback network, an input filter and an ideal controller: the nullor. The input filter and feedback network were designed to obtain the desired transfer. In figure 5.1 a complete overview of the topology of the pick-up loop signal path is demonstrated. Here the nullor is replaced with a finite gain (V-to-V) controller.

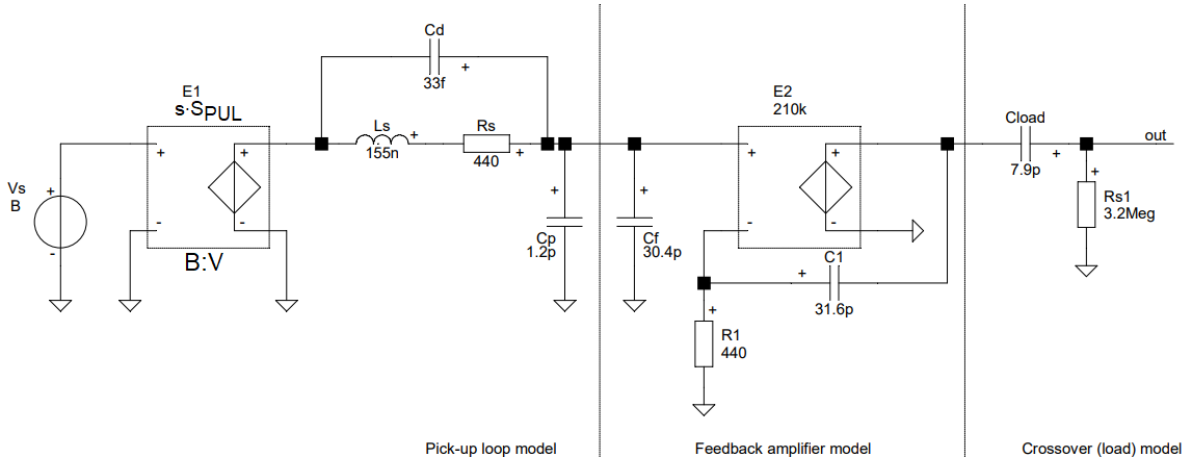


Figure 5.1: Complete model of the pick-up loop path including the crossover filter network. The controller is modeled using a finite gain voltage controlled voltage source.

The model shown in 5.1 was simulated with SLiCAP to verify the transfer. The resulting Bode plot is shown in figure 5.2.

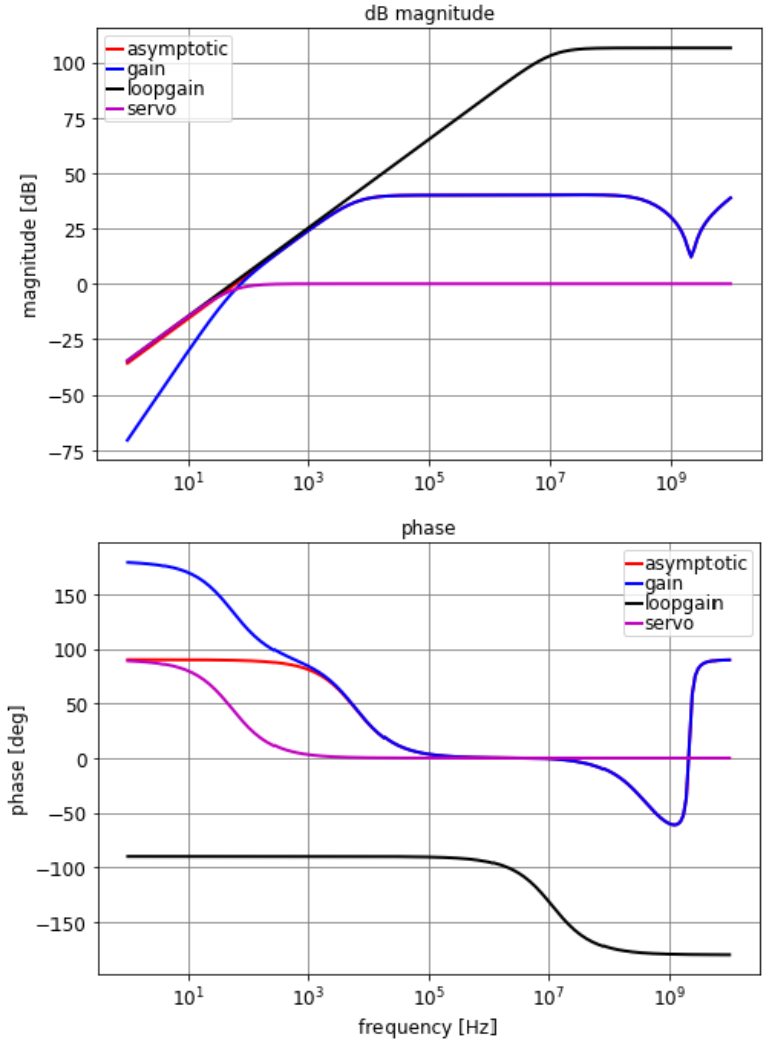


Figure 5.2: Bode plot (magnitude & phase) of the feedback amplifier concept using a finite-gain controller. Note: the magnitude curve of the asymptotic gain lies for a large part on top of the gain curve.

The source model is only valid for frequencies ≪100 MHz. A distributed model is required for verifying the stability at higher frequencies. This step is included in the verification section of the design 5.9. In table 5.1 the poles and zeros of the loop gain (transfer) are listed.

Table 5.1: The poles and zeros of the loop gain of the feedback amplifier model using a finite gain-controller

P or Z	Calculated	Motivation	Simulated (SLiCAP)	Note
p_1	11.45 MHz	$\frac{1}{2\pi C_1 R_1}$	11.45 MHz	feedback network pole
z_1	0 Hz	C_1 is 'open' circuit for $f = 0$	0 Hz	

The source-to-load transfer has 3 more poles, indicated in table 5.2: a low frequency pole $p1$ resulting from the finite gain of the controller, a slightly higher low frequency pole $p2$ resulting from the crossover filter and a high frequency pole $p4$ resulting from the pick-up loop model.

Table 5.2: The poles of source-to-load transfer of the amplifier model using a finite gain-controller

Poles	Calculated	Motivation	Simulated (SLiCAP)	Note
p_1	54.5	$\approx \frac{S_{PUL-path}}{2\pi S_{PUL} A_v}$	54.5 Hz	S_{PUL}: pick-up loop sensitivity [V/T], $S_{PUL-path}$: pick-up loop path sensitivity [V/T]
p_2	6296 Hz	$\approx \frac{1}{2\pi R_{load} C_{load}}$	6217 Hz	output filter pole
p_3	11.45 MHz	$\approx \frac{1}{2\pi(C_p+C_f)R_1}$	11.45 MHz	input filter pole, canceled by zero
p_4	439.8 MHz	$\approx \frac{1}{4\pi}\left(-\frac{R}{L} - \sqrt{\left(\frac{R}{L}\right)^2 - \frac{4}{LC}}\right)$	440.1 MHz	

In the design of the mid-band transfer, $p1$, $p2$ and $p4$ will be omitted as their location will not be influenced by the loop gain. This will be done by using a simplified model, where some of the components are omitted, indicated in figure 5.3. Later in the verification of the amplifier stability, these components will be reintroduced to the model to verify if this assumption was justified.

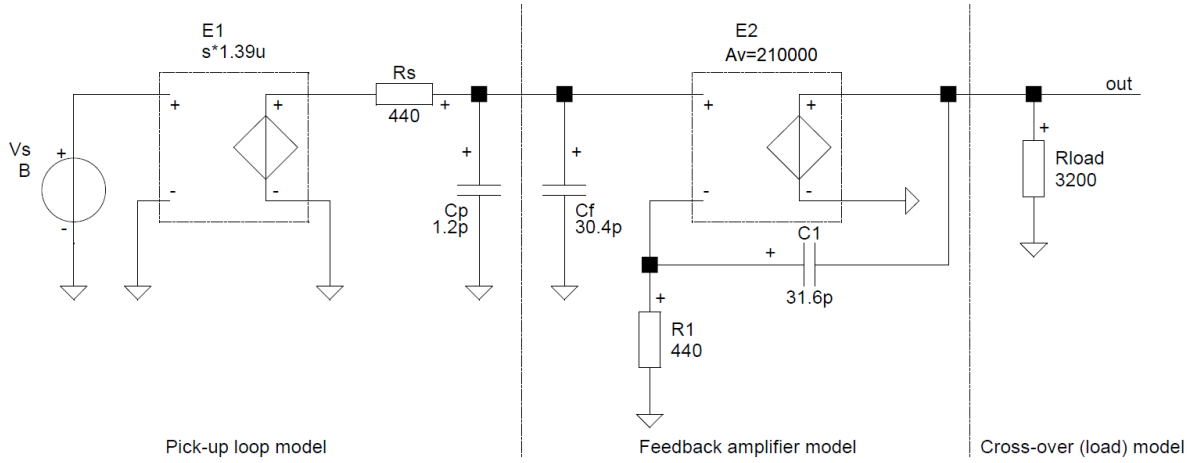


Figure 5.3: Complete model of the pick-up loop path including the crossover filter network. The controller is modeled using a finite gain voltage controlled voltage source.

5.3. Noise design

This section describes the design of the input transistor in a 500 nm 5 V CMOS process. The preferred input stage is a common source stage, as it is the best available approximation of the nullor.

In section 4.3.6 an estimation of the transconductance required in the first stage was made assuming zero flicker noise and gate current. The result was a transconductance of 2.27 mS, assuming zero flicker-noise and zero gate current. Simulations using device dimensions based on these assumptions showed much higher noise: the flicker-noise component was much larger than expected. Thus a better model including flicker-noise was needed. The improved model is:

$$S_{V_N} = \frac{4kTn\Gamma}{g_m}\left(1+\frac{f_l}{f}\right) \tag{5.1}$$

This model provided sufficient accuracy to design a input stage with sufficient low noise. The flicker-noise corner frequency f_l was estimated from previous simulation results. The transistor is operating in moderate inversion and in saturation. The inversion coefficient I.C. corresponding to the desired operating region is ≈1 [46]. Considering the g_m-efficiency in this region provides a quiescent current requirement of approximately 200 μA.

The device dimensions obtained using the noise expression (5.1) were verified in the simulator (T-spice) using the transistor models supplied by the foundry. The test-bench model used for verification of the transistor is demonstrated in figure 5.4. For completeness the filter and complete source model (with C_{Load}, C_d and L_s) was included, but compared to hand calculations without these elements their influence on the noise is negligible.

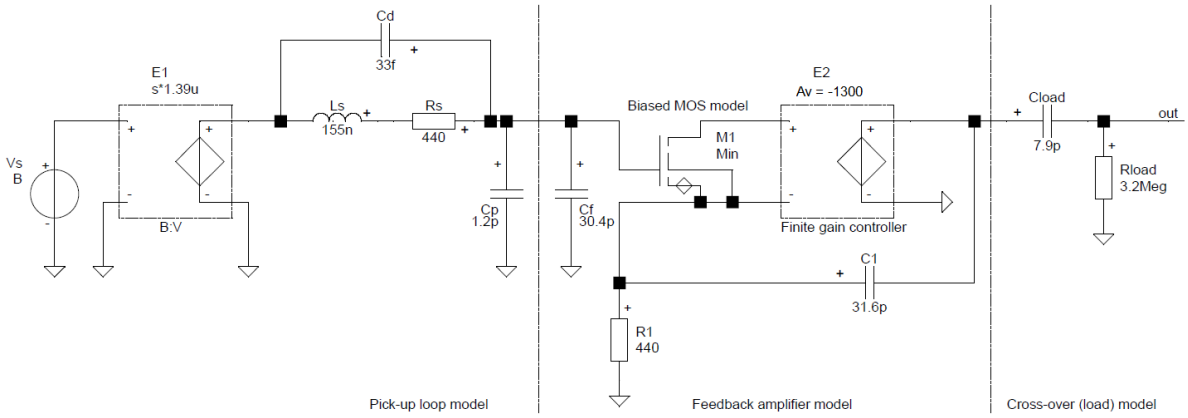


Figure 5.4: Test bench for verifying the noise contribution of the input stage.

The results of the simulation of this design is indicated in table 5.3. Included in the table are also some important small-signal parameters used in a later stage of the design and the inversion coefficient.

Table 5.3: Parameters of the input transistor M_{in} for each design iteration.

parameter	value	unit	note
W	600	μm	
L	800	nm	
V_{ds}	1	V	
I_d	200	μA	
g_m	3.45	mS	simulated
I.C.	1.16	-	calculated
Source referred noise	29.1	μ T_{RMS}	including external circuits, simulated
C_{gs}	530	fF	calculated
C_{gd}	214	fF	calculated

5.4. Design of the drive capability

This section describes the design of the drive capabilities of the controller. First a single stage designed is considered. In the remaining part of this section the design of a dedicated output stage is described.

5.4.1. Single stage solution

Minimizing the number of stages in a controller is beneficial for obtaining low power consumption and minimal area. A controller using a single stage is therefore considered. This controller would require a high drain output impedance r_o (assuming g_m to remain fixed) to provide sufficient voltage gain. Assuming the g_m found in the previous section, the output impedance of the single stage controller must be at least 19 MΩ to provide sufficient DC controller gain. The problem with this controller topology is that the load impedance must be $\ll$ 19MΩ to not reduce the voltage gain of the stage. This would result in an unfeasible large resistance to implement on chip. Therefore a dedicated output stage is preferred, resulting a multi-stage topology.

5.4.2. Output stage

This sub-section describes the design of an output stage fulfilling the load drive requirement. The output stage must provide a voltage swing of 800mV$_{pp}$. The maximum swing available from a single ended class A stage using a MOSFET is $V_{DD} - V_{DS(sat)}$. Considering the minimum supply voltage, the specified swing is feasible. The output stage is required to work in class A, such that the current drawn from the supply is constant independent of the output signal. The preferred type of stage is a common source stage. The peak load current provided by this stage is equal to the quiescent current. The required load drive current is found by dividing the peak output voltage (400 mV$_p$) by the worst case load impedance. Neglecting the contribution of the crossover network (as $Z_{cross} >> Z_{fb}$), the load impedance can be approximated as:

$$Z_{load} = \sqrt{R_1^2 + \left(\frac{1}{j2\pi f C_1}\right)^2} \tag{5.2}$$

The worst case loading appears at the upper end of the bandwidth (f_h = 5 MHz). The resulting load impedance at this frequency is $Z_{load,min}$ ≈1.1 kΩ. The peak load current is I_{out} = 363μA and will also be the minimum quiescent current for the output stage. It is increased to 400 μA to provide some headroom. The output transistor is operating in strong inversion and in saturation. This was chosen as it provides large transconductance using minimal area. The overlap capacitance $C_o\upsilon$ in this operating region is small. The gate drain capacitance can be approximated as C_{ov} and is small compared to the gate source capacitance. The stage is thus approximating unilateral behavior. At the same time the $V_{DS(sat)}$ is low, thus enabling a large output voltage swing. A relative small device is used, having a length of 500 nm and a width of 50 μm. This device was simulated in T-spice. Its small-signal parameters are listed in table 5.4.

Table 5.4: Parameters of the output transistor M_{out}

parameter	value	unit	note
W	50	μm	
L	500	nm	
V_{ds}	1.5	V	half of $V_{DD}(min)$
I_d	400	μA	
g_m	3	mS	simulated
I.C.	17.4	-	calculated
C_{gs}	45	fF	calculated
C_{gd}	18	fF	calculated

5.5. Design of the mid-band accuracy

In the previous two sections the design of the input and output stage were described. A cascade of these two stages would result in a DC controller voltage gain of about 9700 (80 dB) compared to a requirement of 210000 (106 dB). The DC controller gain must be increased by a factor 21.6 (or 27dB) to meet the requirement. A third intermediate common source stage could be added, but obtaining a stable response from this 3-stage controller is expected to be difficult.

A more promising option is to increase the (voltage) gain of one of the two stages. This can be accomplished by replacing one of the common source stages with a cascode stage (cascade of common source and common base). Placing a common gate stage after the output stage is ineffective, for the same reason as seen with the single stage controller in 5.4.1. Therefore the input stage is used for increasing the voltage gain of the controller.

The device dimensions of the common gate stage are set to obtain a similar set of small-signal parameters as the input transistor. This will provide a sufficient increase of the DC controller gain. The noise contribution of the cascode stage can be considered negligible due to the large transconductance provided by the input transistor, therefore the length was set to L_{min}. The total DC voltage gain of the controller is 325000 (110 dB), providing headroom compared to the requirement found in 4.3. Table 5.5 lists the resulting device dimensions, operating point and some small-signal parameters.

Table 5.5: Parameters of the cascode transistor M_{casc}

parameter	value	unit	note
W	600	μm	
L	500	nm	
V_{ds}	1	V	
I_d	200	μA	
g_m	3	mS	simulated
I.C.	3.1	-	calculated
C_{gs}	538	fF	calculated
C_{gd}	230	fF	calculated

5.6. Interconnection of the stages

So far, an input and output stage where designed. The input stage is a cascode stage and the output stage a common source stage. Directly cascading these two stages results in an improper interconnection [45]. The resulting circuit is shown in figure 5.5, the return path of the stages must flow through the external circuit (thus the feedback network). The result of this improper interconnection is that the gain does not equal the ideal gain, if one of the stages is replaced with a nullor. Alternatively, replacing one of the stages by a nullor does not result in a controller with nullor-like behavior. By choosing an input stage with a high $g_m r_o$-product (i.e. cascode), the effect of the improper interconnection is expected to be small [45].

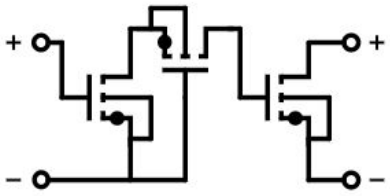


Figure 5.5: Interconnections of the stages.

5.7. Design of the frequency response

The simplified small-signal circuit model of the amplifier is shown in figure 5.6. Each transistor is modeled as a voltage controlled current source with transconductance g_m, an equivalent output resistance r_o and an gate source capacitance C_{gs}. The simplified source and load model, without C_d, L_s and C_{Load} is considered in the first part of the design of the bandwidth. Leaving these components out removes poles from the source to load transfer that do not appear in the loop gain. At a later point, the justification of these simplifications is verified.

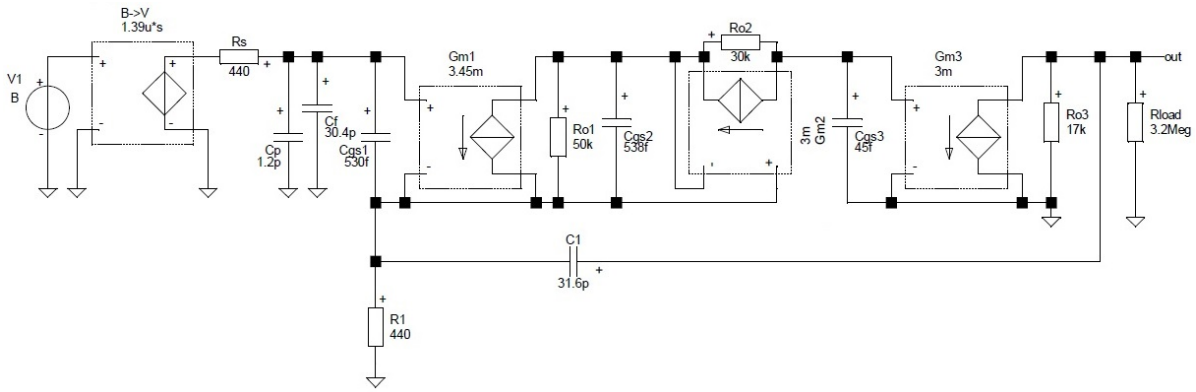


Figure 5.6: implified small-signal model used for hand calculations.

The stability of the amplifier is evaluated by analyzing the root locus plot of the servo function. First the loop gain reference variable must be selected. A proper selection of the loop gain reference variable yields an asymptotic gain that equals the ideal gain, for a controller gain $A \rightarrow \infty$ [45]. This situation occurs if the transconductance of the input stage is selected as loop gain reference variable. The root-locus as a function of the transconductance of the input stage is demonstrated in figure 5.7. The transconductance g_{m1} is stepped over a range of 1nS (sufficiently small: zero as start point would introduce a division by zero) to 3.5 mS. For $g_{m1} \rightarrow 0$, all poles have zero imaginary part and lie in the left half-plane. When increasing g_{m1}, two poles will obtain a non-zero imaginary part (i.e. they become a complex conjugated pole-pair). Increasing the transconductance further moves these two poles toward the imaginary axis and eventually, for even higher g_m, into the right half plane.

Next the poles & zeros, mid-band loop gain and system order are determined. This is done using a simplified small-signal model, allowing the use of hand-calculations. It is shown in figure 5.8. The output transistor M_{out} is operating in strong inversion and in saturation, thus including only the gate source capacitance in the model is sufficiently accurate. This does not hold for the transistors in the input stage, as these are operating in moderate inversion and saturation, were the gate drain capacitance is much larger compared to the gate source capacitance. Omitting one of these two or both capacitors results in a significantly different roll-off behavior. But a model including these gate-drain capacitances is difficult to analyze. Therefore a model without the gate-drain capacitances is used for hand calculations, to gain insight in the pole locations. The results from these hand calculations will not provide the absolute values of the pole locations and are thus not representative. They do on the other hand provide information about their relative locations and more importantly identify the components that contribute to the pole locations. After analyzing this simplified model, the small-signal including the gate-drain capacitances, is used in the design of the frequency compensation.

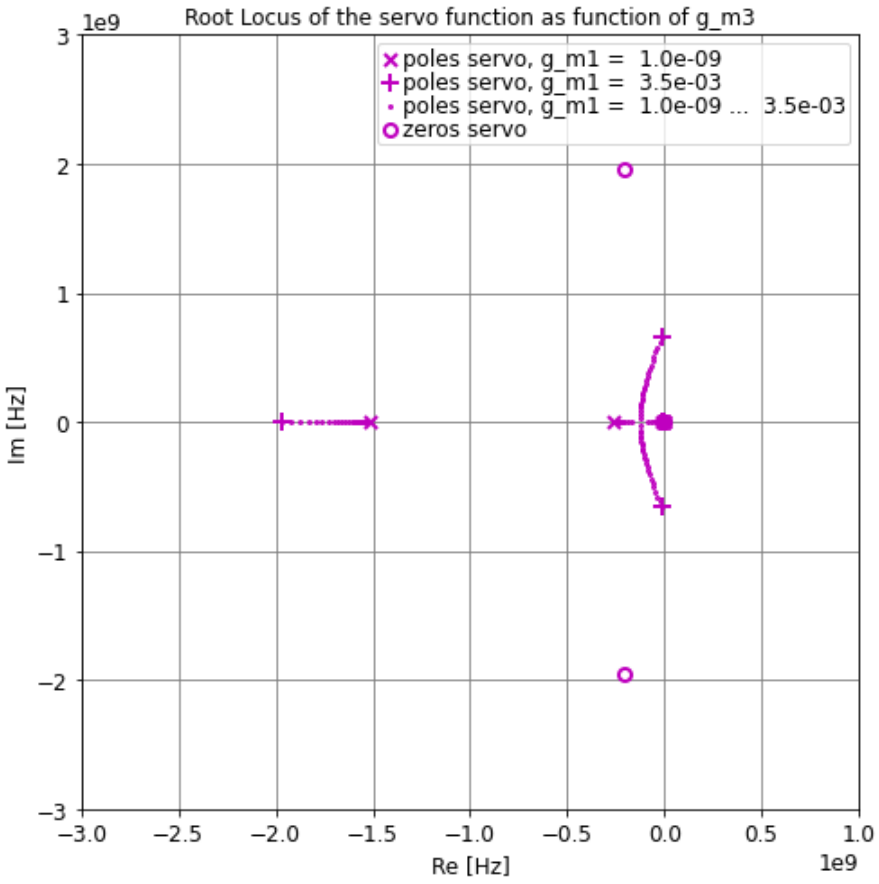


Figure 5.7: Root locus plot as function of g_{m1} of the non-compensated amplifier.

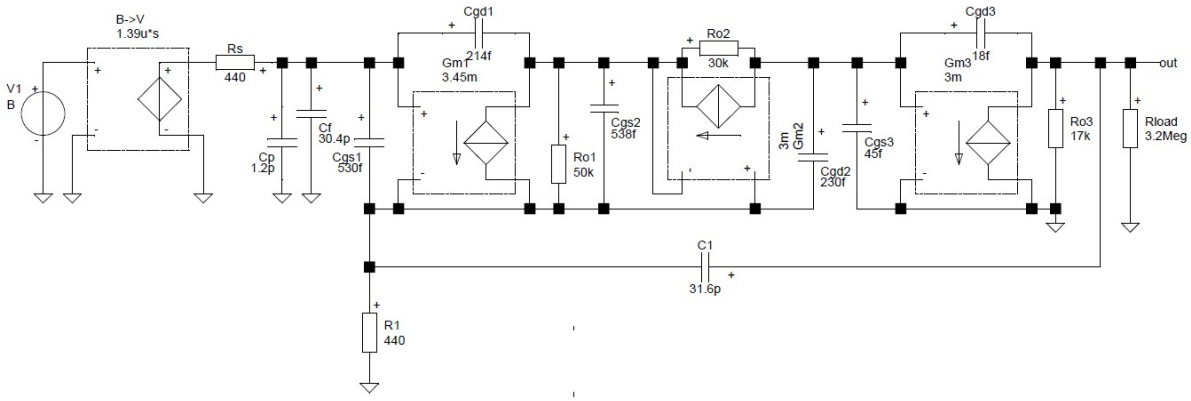


Figure 5.8: Small-signal model used for evaluating the amplifier stability with all gate drain capacitances included.

5.7.1. Poles and zeros of the loop gain

In the previous section a LG-reference was selected. In figure 5.9 the simplified small-signal model for the analysis of the loop gain is shown. The model is a alternatively drawn version of figure 5.8, with only the relevant contributors to the loop gain included.

The equivalent input small-signal resistance seen at the inverting input, or source of the input transistor M_{in}, is found as:

$$r_{in1} \approx \frac{1}{g_{m1}} \tag{5.3}$$

Similarly, the input resistance of the cascode transistor M_{casc} is found as:

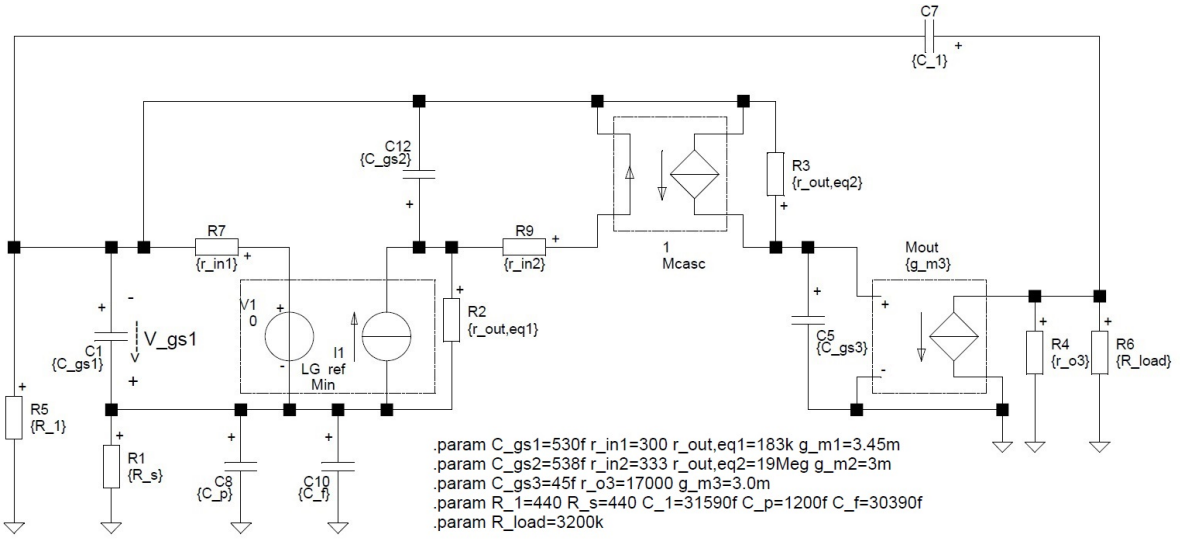


Figure 5.9: Circuit model for deriving the loop gain transfer of the amplifier.

$$r_{in2} \approx \frac{1}{g_{m2}} \tag{5.4}$$

and its effective output resistance:

$$r_{out,eq2} \approx \left[(r_{fb} + r_{in1})(1 + g_{m1} r_{o1})\right](1 + g_{m2} r_{o2}) + r_{o2} \tag{5.5}$$

Using this model, symbolic expressions for approximating the poles and zeros of the loop gain transfer were derived. The resulting pole and zero locations are indicated in table 5.6. The approximations where verified using a pole-zero analysis on the simplified small-signal model (figure 5.8).

Table 5.6: pole zero analysis results (C_{Load}, L_s and C_d omitted)

P or Z	calculated	motivation	simulated (SLiCAP)	note
p1	186 kHz	$\approx \frac{1}{2\pi R_{out,casc} C_{gs3}}$	115 kHz	moves to z1
p2	306 kHz	$\approx \frac{1}{2\pi C_1 [(R_1 \| r_{in1}) + (r_{o3} \| R_{load})]}$	1.5 MHz	factor 5 error in calc.
p3	11.5 MHz	$\approx \frac{1}{2\pi (C_p + C_f) R_s}$	11.26 MHz	moves to z2
p4	896 MHz	$\approx \frac{g_{m2}}{2\pi C_{gs2}}$	913 MHz*	* p4 & p5 conjugated pole pair
p5	1001 MHz	$\approx \frac{1}{2\pi C_{gs1} [(R_1 + R_s) \| r_{in1}]}$	913 MHz*	* p4 & p5 conjugated pole pair
z1	0 Hz	C_1 appears 'open' at $f \to 0$	0 Hz	
z2			11.45 MHz	
z3			10.6 GHz	

With the symbolic pole expressions a compensation strategy is derived. This will be discussed in the next sections. In table 5.7 the poles and zeros of the small signal model with all gate-drain capacitance included are listed. The number of poles is the same as the simplified model but their locations are different. Especially p1 and p4 show large deviations. Also one additional zero z4 is found, constituting to a complex zero-pair with zero z3. In the next section the maximum bandwidth and system order is derived using these pole locations.

The loop gain of the amplifier has a zero in the origin, resulting in a band-pass transfer. Therefore the maximum value of the loop gain is not located at f=0 Hz. By analyzing the pole-zero locations in table 5.6 and the sketch of the magnitude response 5.10, the location of the maximum loop gain is found. For clarity the pole located at $f \approx$11.5 MHz is omitted from this drawing as there is a zero on top (thus their effect is not visible in the magnitude response).

The maximum is located in between poles p1 and p2. The mid-band loop gain at this point can be approximated as:

Table 5.7: simulated poles and zeros of the loop gain derived using the small-signal model with all gate-drain capacitances included

P or Z	simulated (SLiCAP)	note
p1	24 kHz	moves to z1
p2	1.19 MHz	
p3	11 MHz	moves to z2
p4	280 MHz	
p5	1.51 GHz	
z1	0 Hz	
z2	11.45 MHz	
z3	1.92 GHz*	*z3 & z4 conjugated zero pair
z4	1.92 GHz*	*z3 & z4 conjugated zero pair

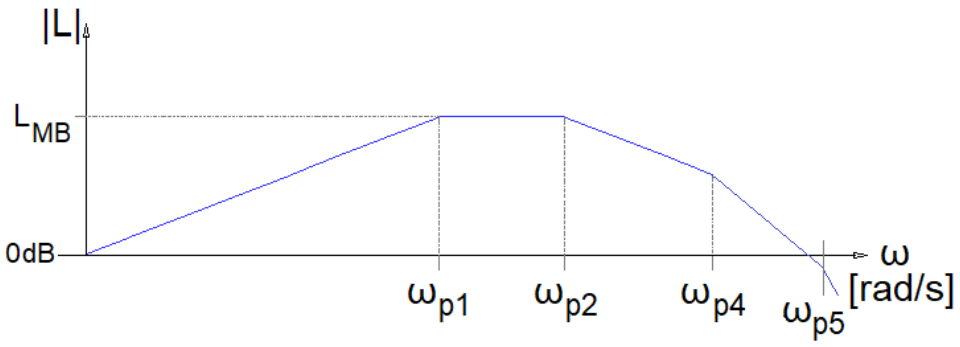


Figure 5.10: Sketch of the magnitude transfer of the loop gain

$$L_{MB} \approx g_{m1} \cdot R_{out,casc} \| Z_{C_{gs3}} \cdot -g_{m3}(r_{o3} \| R_{load}) \frac{R1}{Z_{C_1} + R_1} \frac{r_{in1}}{R_1 + r_{in1}} \tag{5.6}$$

Filling in the values provides a mid-band loop gain of -2500 (≈68 dB, inverting). Compared to simulation data obtained with SLiCAP and T-spice this value is sufficiently accurate. The amplifier needs to have a loop gain of at least 40 dB to meet the mid-band accuracy requirement, but some headroom (≥10 dB) is desired considering temperature and process variations.

5.7.2. System order and bandwidth

The order of the system (equivalently, the number of dominant poles of the system) can be found using [45]:

$$\omega_n = \sqrt[n]{\left| (1 - L_{MB}) \prod_{i=1}^{n} p_i \right|} \tag{5.7}$$

The first pole p1 (i.e. pole with lowest frequency in table 5.6) moves toward the zero z1 in the origin when the loop gain reference variable approximates infinity. Thus it does not contribute to the high frequency behavior of the amplifier and are not included in determination of the LP-product. The same can be concluded about pole p3 and zero z2 as they lie on top of each other.

Table 5.8: Table for finding order of the system with Cgd's

ω_n	value	unit
ω_1	18.7	G rad/s
ω_2	5.73	G rad/s
ω_2	6.78	G rad/s

The order of the system is provided by the lowest ω_n, indicated in green. The high frequency roll-off can thus be modeled as a system with order two. The maximum bandwidth obtainable from this circuit is ≈0.9 GHz. By analyzing the expressions in table 5.6, it becomes clear that the pole location of p_2 (and p_1) can be

manipulated by changing the parameters of the output transistor, thereby reducing the loop gain and system order. This will be further elaborated in the next section.

5.7.3. Frequency compensation

In the previous section, it became clear that the amplifier is unstable. This section describes a method for compensating the amplifier resulting in a stable response. The bandwidth will be limited in the power amplifier after the crossover network. The design of the power amplifier is outside the scope of this project. In figure 5.11 the desired loop gain magnitude response after compensation is shown in red.

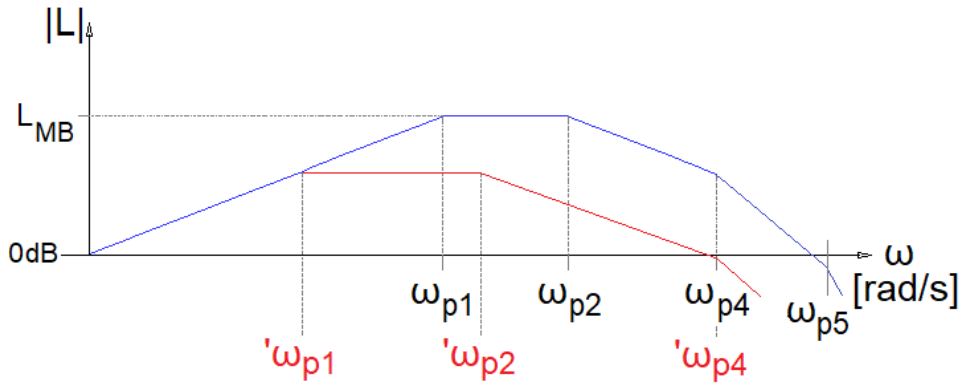


Figure 5.11: Sketch of the magnitude transfer of the loop gain of the uncompensated amplifier (blue) and a proposed magnitude transfer of the compensated amplifier (red).

The idea is to reduce the pole frequencies of p1 and p2, thus effectively reducing reducing the loop gain and thus the number of dominant poles. The result would be a first order roll-off of the loop gain. This could also be obtained by manipulating pole p4. But p4 can not be manipulated, as it depends on the components of the feedback network (fixed by the design of the ideal transfer) and the small signal parameters of the input transistor (fixed by the noise design). The frequencies of p1 and p2 are depending on the small signal parameters of output transistor M_{out}. These can be altered without introducing a large penalty.

Phantom zero compensation

Implementation of a phantom zero is not possible. The source appears capacitive (due to filter capacitor) around the frequencies where the zero should be implemented. A phantom zero can not be implemented here. In the feedback or load circuit, a phantom zero can be implemented using a inductor. But implementing an inductor with high-Q on chip is not possible. Therefore phantom zero compensation is not an option.

Reducing pole frequencies of output stage

In section 5.7.2 the dominant poles of the loop gain were approximated resulting in design equations relating the pole locations to the model parameters. Both p1 and p2 are dependent on the parameters of transistor M_{out}. By manipulating the transistor dimensions, the pole location can be changed. The penalty for doing this is a reduction of the mid-band loop gain. This is acceptable, as the loop gain is higher than the minimum to meet the mid-band accuracy. Reduction of the pole frequencies can be accomplished by increasing the transistor size or by placing a capacitor in parallel with C_{gs3}. Increasing the length of the output transistor provides larger gate source capacitance C_{gs3} and output resistance r_{o3} while C_{gd3} remains constant. The penalty is a reduced g_m3, but this is acceptable as r_o3 increases much faster, thus the effective voltage gain or μ of the stage is increased. Obtaining a stable response just by increasing the length would result in a very long transistor. Therefore the transistor length was only increased by a factor 4 and a small capacitor C_c is placed in parallel to C_gs3. This provides a stable amplifier, using minimal area for the frequency compensation. In table 5.9 the old and new device parameters of M_{out} are listed.

Table 5.9: Resizing of the output transistor M_{out}

parameter	old value	new value	unit	note
W	50	50	μm	
L	500	2000	nm	
r_{o3}	17	291	kΩ	
g_{m3}	2.9	1.4	mS	simulated
I.C.	17.4	70	-	calculated
C_{gs3}	45	188	fF	calculated
C_{gd3}	18	18	fF	calculated

The effectiveness of this method was verified using the small signal model (figure **??**) in SLiCAP. The compensation capacitor in parallel to gate source capacitance has a strong effect on the pole locations, as can be seen from the root locus plot of the servo function 5.12. The black crosses in this figure indicate the pole locations of the high-frequency poles before increasing the length of M_{out}.

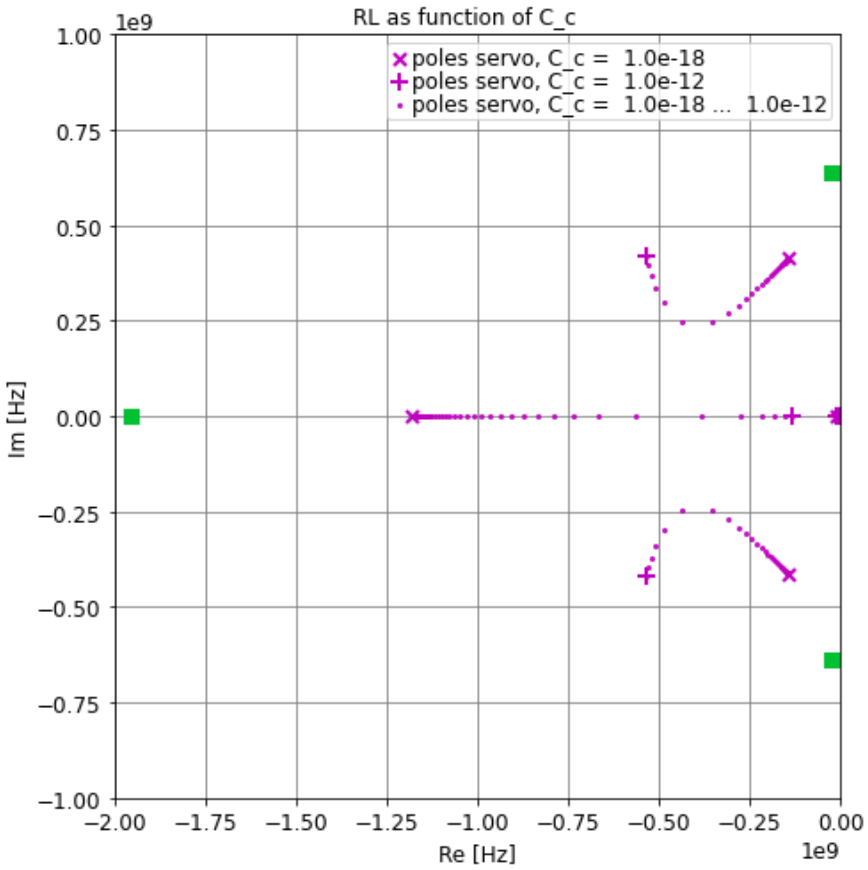


Figure 5.12: Root locus plot as function of C_c of the amplifier. The green squares represent the pole locations of the dominant poles before increasing the length of M_{out}.

The complex conjugated pole pair moves into the right half plane, increasing the stability of the circuit. For $C_{gs3} > 800$ fF a stable frequency response is obtained. A value of 1 pF was chosen. The resulting pole locations are not in Butterworth, but this is not required; a stable response without peaking is sufficient. The Bode plot after frequency compensation is shown in figure 5.13.

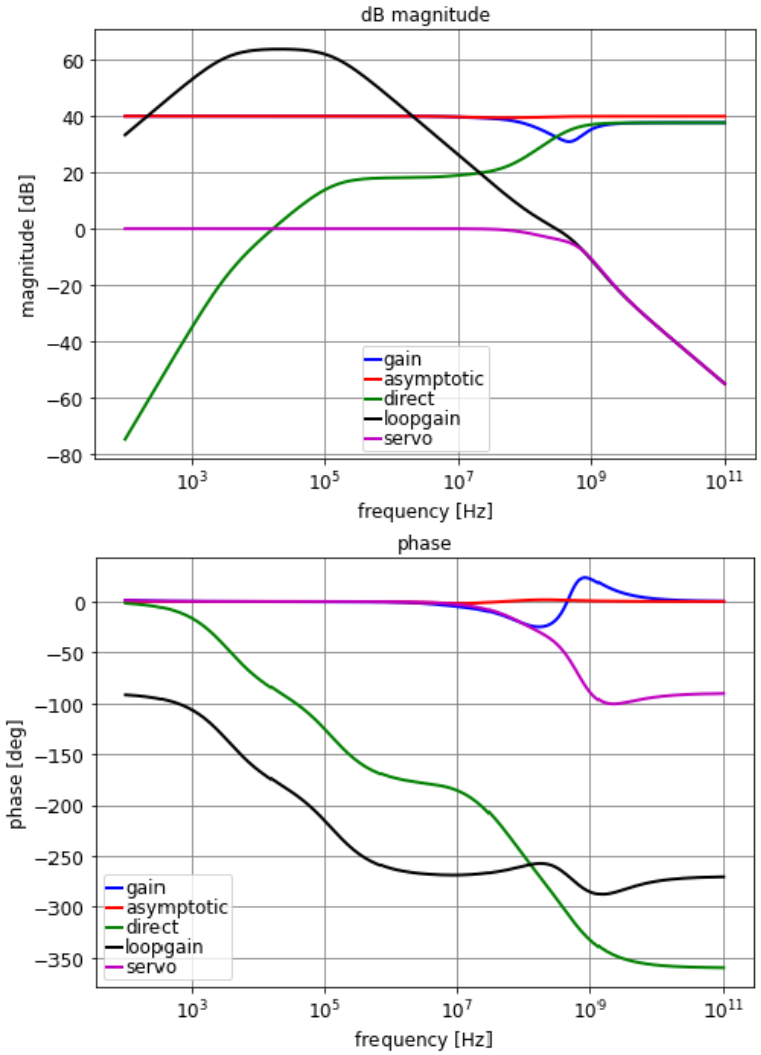


Figure 5.13: Bode plot of the amplifier circuit after compensation.

The peaking is effectively eliminated from the servo function and the gain of the amplifier. The bandwidth of the source-to-load transfer is ≈150 MHz.

After designing the bandwidth of the amplifier using the small-signal model without C_d, L_s and C_{Load}, the validity is checked by introducing the omitted elements to the model. As expected, the effect of C_d, L_s and C_{Load} is only visible in the gain and asymptotic gain 5.14 and at very high frequencies ($f >> 1$ GHz).

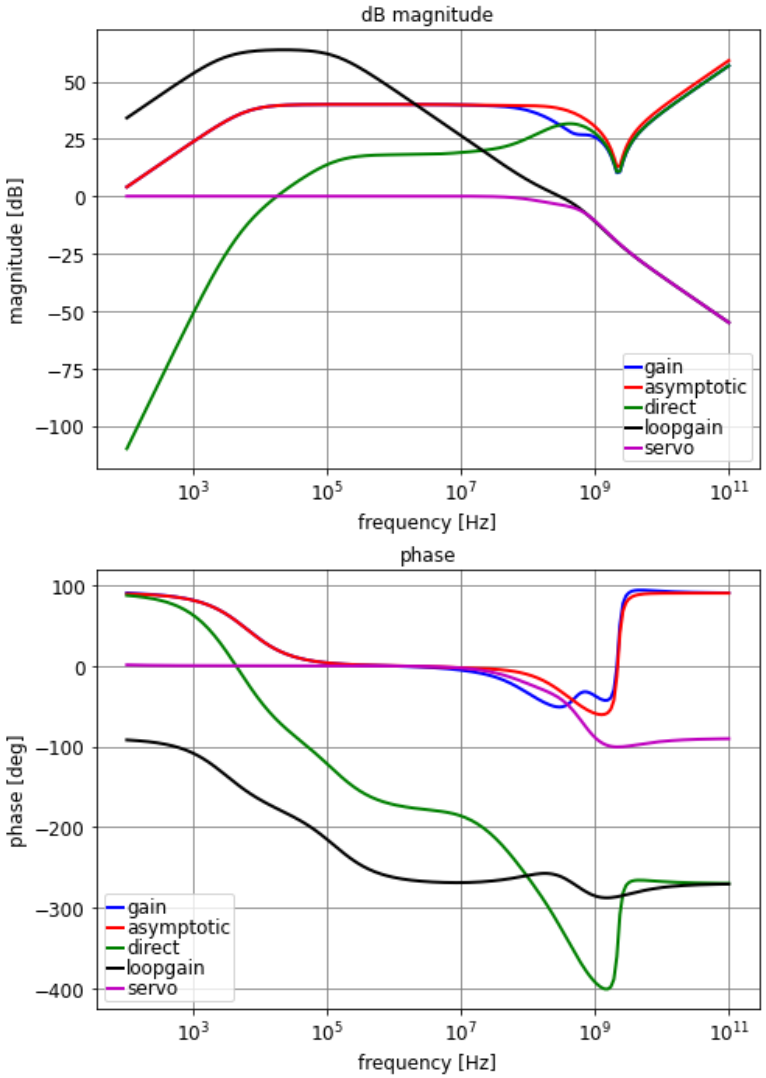


Figure 5.14: Bode plot after introduction of all gate-drain capacitances, C_{Load}, L_s and C_d to the model.

5.8. Controller biasing

This section describes the biasing of the amplifier.

5.8.1. Biasing concept

This section describes the design of the biasing of the amplifier using ideal sources. First the number of floating sources is reduced. Next a bias loop is described. Figure 5.15 shows the starting point for deriving the biasing circuit. In this circuit, each transistor has 4 ideal bias sources. The feedback capacitor is omitted from the model because only DC voltages and currents are considered. The goal here is to reduce the number of (floating) sources.

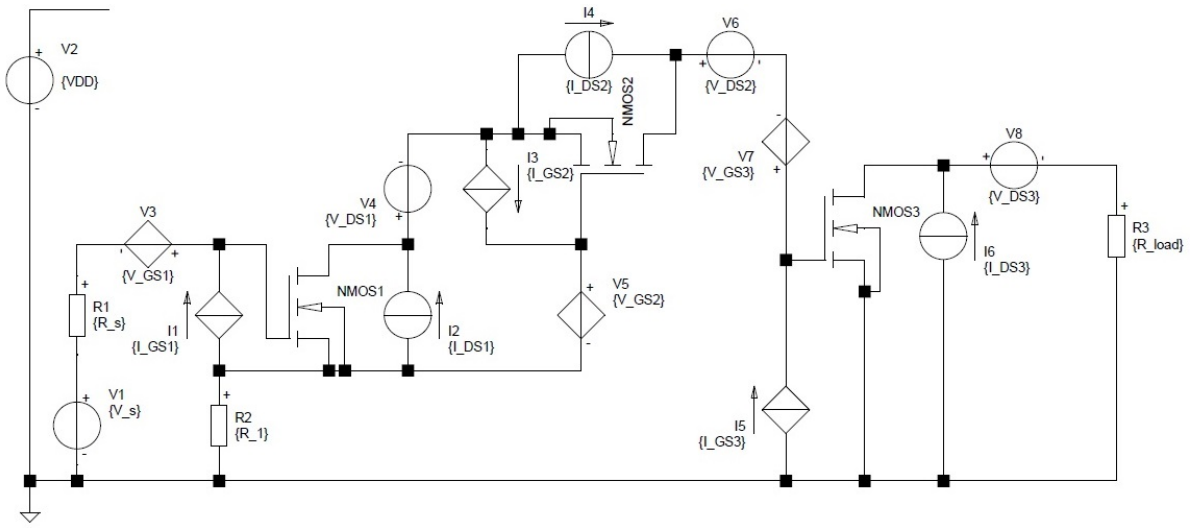


Figure 5.15: Circuit with four bias sources per transistor.

At this point, all transistors are implemented using NMOS devices. The controller model including the ideal bias sources is connected to a single supply source. This is done by redirecting currents over ground or the supply line and by moving voltage sources through nodes into different branches (Blakesley voltage shift & current redirect, Norton & Thévenin equivalent networks). The step also reduces the number of floating sources. The result after execution of the first bias steps is shown in figure 5.16.

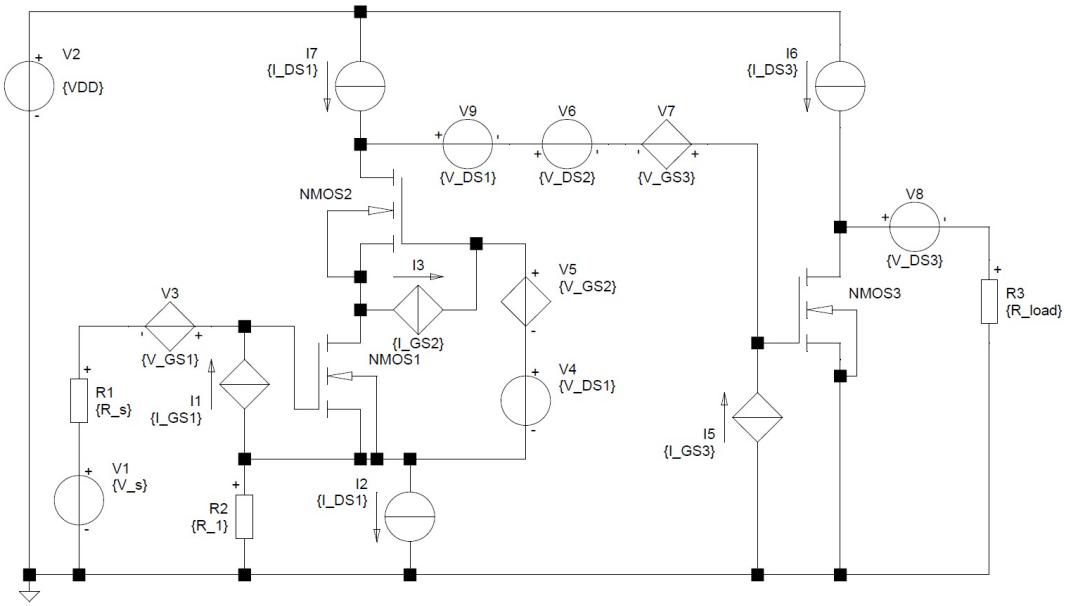


Figure 5.16: Bias circuit after the first source manipulation

This circuit has two floating voltage sources (each consisting of the sum of a number of bias sources). Sources V6, V7 and V9 can be shifted through the output transistor and ground node resulting in the circuit shown in figure 5.17. In this figure, source V6 and V9 are combined into one independent voltage source.

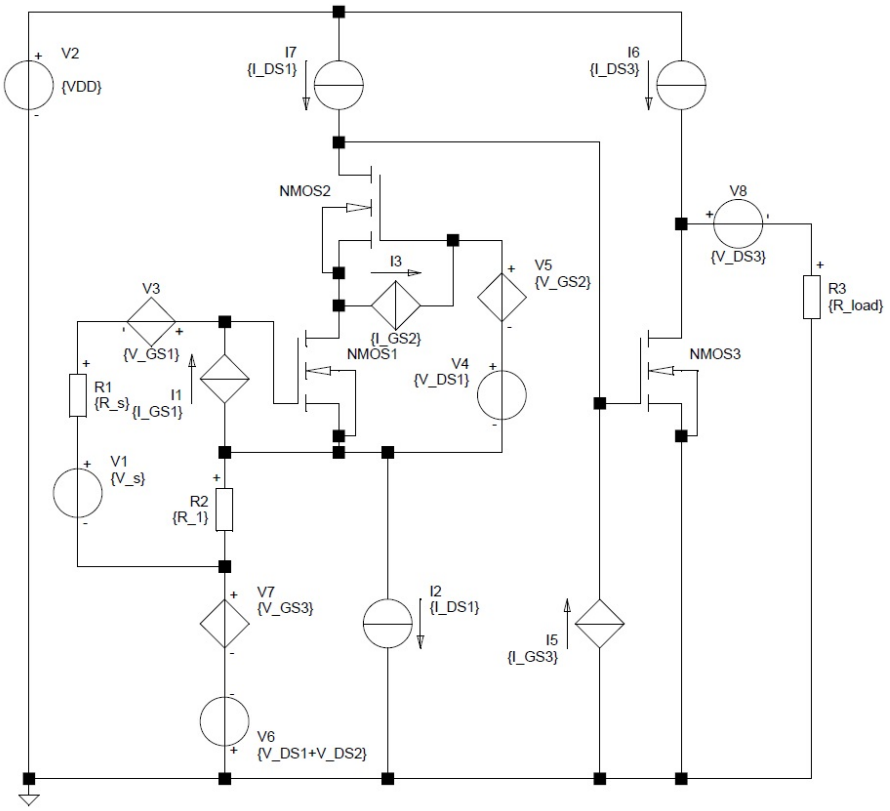


Figure 5.17: Bias circuit after manipulating the location of V6 V7 and V9.

The two drain source voltages (M_{in} and M_{casc}) and the bias voltage sources (V6 and V7) in series leave little supply voltage for implementing current source I7 considering the minimum supply voltage of 3V. A solution is to change the device type of the cascode transistor to a PMOS. This introduces an extra current path, thus increasing the power consumption of the circuit. This is an acceptable penalty, as the power consumption of the amplifier is well below the requirement. Switching the device type of the cascode transistor does not directly reduce the number of floating sources, as can be seen in figure 5.18.

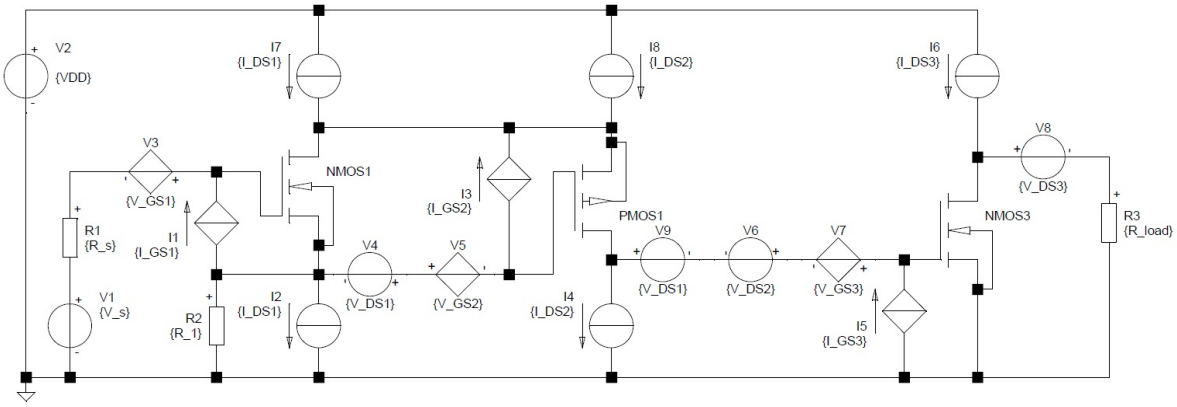


Figure 5.18: Reduced biasing circuit. For clarity voltage sources in series are not combined to a single source. The same holds for current sources in parallel.

A floating source is required in between the input and cascode transistor (V4 and V5) and in between

the cascode stage and output stage (V6, V7 and V9). The first of the two (V4 and V5) can be eliminated by choosing the drain source voltage of the first stage such that:

$$V_{DS1} - V_{GS2} \approx 0 \tag{5.8}$$

This does not significantly influence the small-signal parameters of the input stage. The second floating source (V6, V7 and V9) can be shifted through the output transistor and ground node to be in series with the source and feedback resistor as shown in figure 5.19. This figure also shows the over-all biasing loop. It was decided to only control the gate source voltage of the first stage. Omitting the control of V5 and V7 introduces an acceptable bias error. In the end this will be reduced by the over-all bias loop. The amplifier is AC-coupled to the consecutive circuitry, thus a relative large output offset is acceptable. The drain source bias voltage source (V8) of the output stage can be omitted because of the AC-coupling.

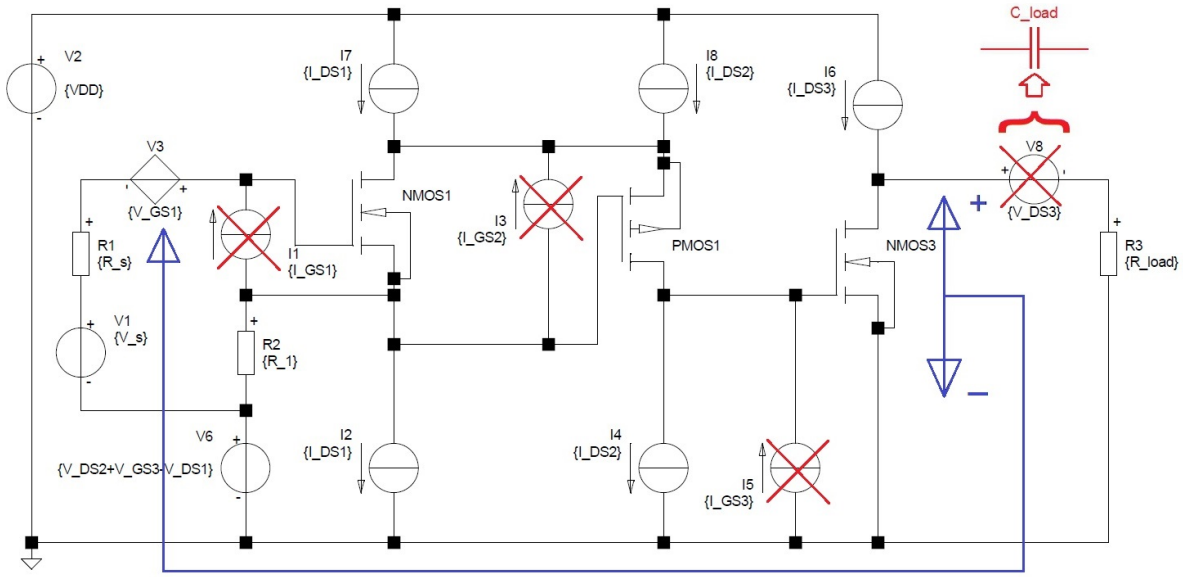


Figure 5.19: Final biasing concept. The overall biasing loop is indicated in blue: the output voltage is measured and is used to control the gate-source voltage of the input transistor. The gate bias current sources can be omitted introducing negligible error. Source V8 can be omitted due to the AC-coupling.

The ideal gate current sources are crossed out as they can be omitted. The other circuitry connected to the gates will provide the small gate bias currents introducing negligible error. The result is a circuit with four independent bias current sources, one independent bias voltage source (one side connected to ground) and a floating dependent voltage source. In the next section the implementation of the ideal bias sources is described.

5.8.2. Biasing implementation

In this section the implementation of the ideal bias sources is described.

Current sources

The bias current sources do appear in parallel with other impedance's in the small-signal model, thus influencing (reducing) the loop gain. Therefore the node impedance connected to each current source is determined. Table 5.10 lists the impedance seen by each current source.

Table 5.10: Bias current sources

Source	symbolic value	I_q	node impedance	realized r_{out}
I_{7+8}	$I_{DS1} + I_{DS2}$	400 μA	$\approx$ 50kΩ	91 kΩ
I_2	I_{DS1}	200 μA	$\approx$44 kΩ	1.04 MΩ
I_4	I_{DS2}	200 μA	$\approx$25 MΩ	1.45 MΩ
I_6	I_{DS3}	400 μA	$\approx$200 kΩ	501 kΩ

The most problematic source here is I_4 as it requires a very high impedance. In the end it was decided to introduce a too small impedance here, as there is sufficient headroom in the loop gain. By doing so, all current sources can be implemented using a single transistor current source (thus avoiding cascode current sources). The resulting circuit is shown in figure 5.21. Each PMOS transistor has a length of 10 μm and each NMOS a length of 20 μm. Using the width the current is scaled to the appropriate value for each branch. The output stage current source (I_6) uses a separate transistor to produce the gate-source voltage for the current source transistor. This allows to use a wider transistor as used in current source I_{7+8}, thus providing a lower $V_{DS,sat}$ and thus sufficiently large output swing.

Voltage sources

Using the same procedure as described in 5.8.2 requirements for the sources in the single ended design were found.

Table 5.11: Bias voltage source requirements

Source	symbolic value	V	r_{out}	note
V3	V_{GS1}	709 mV	<440Ω	To obtain a negligible noise contribution
V6	$V_{GS3} + V_{DS1} + V_{DS2}$	1.01 V	<4.4Ω	Introduces error in asymptotic gain

Source V3 can be realized by injecting a current into the pick-up loop. The series resistance will as a result of this current have the bias voltage across its terminals. Source V6 can be derived from the main reference source on the chip.

The bias voltage sources were not implemented but some preliminary analysis was done to locate the design problems that might arise in a differential design. Figure 5.20 shows the biasing circuit for the differential amplifier. Comparing this circuit to the single ended version, the location of the bias voltage sources have changed. The gate-source bias voltage sources cancel each other as they appear in anti-series. As a result of executing Blakesley voltage shift on one of these gate source voltages, a second gate-source bias voltage source appears in the branch connecting it to ground. This circuit compensates the differential mode and common mode error by feeding signals into the input of the circuit. This was chosen as it was the most obvious implementation for now, but optimization of the bias loops may be done at later point in time.

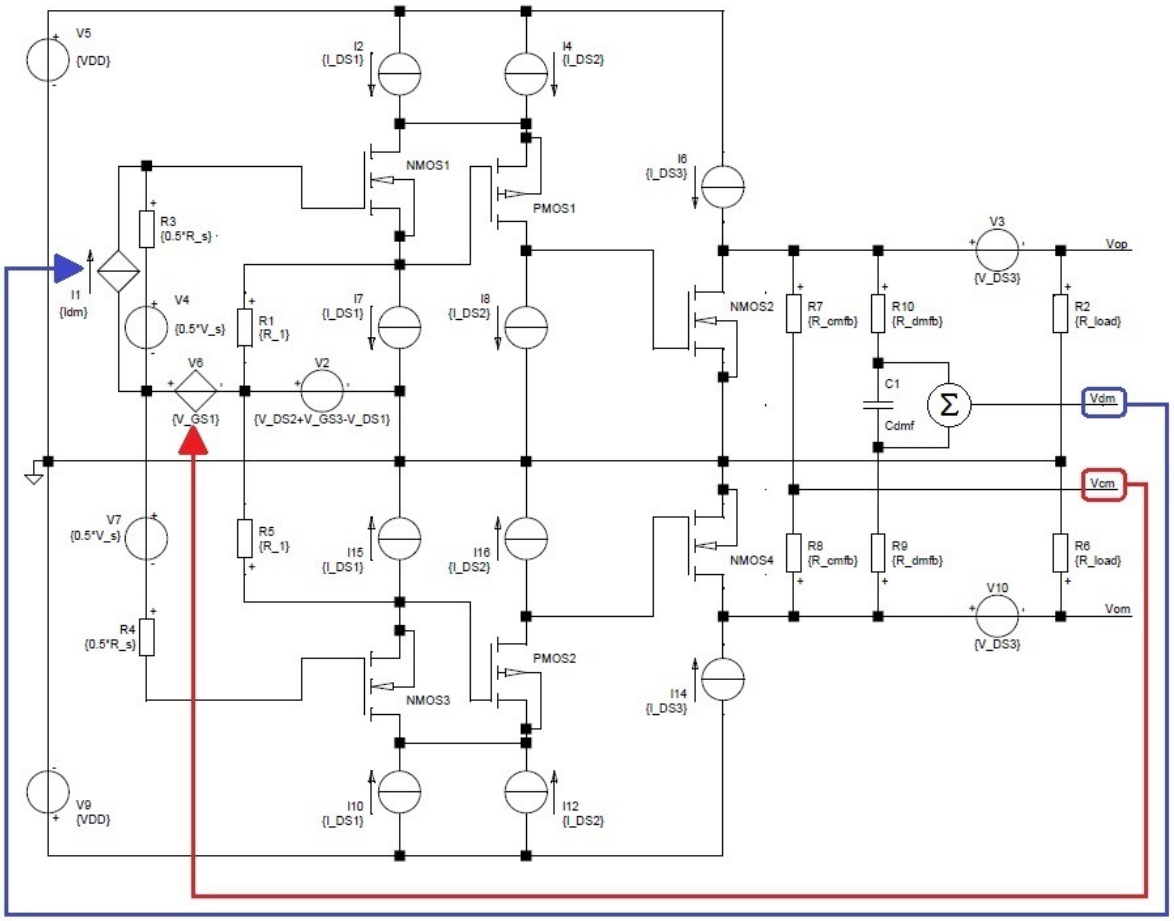


Figure 5.20: A possible differential biasing circuit using ideal sources. The CM biasing loop is indicated in red: the output common mode bias voltage is measured using resistors R_{cmfb}, and is used to control the gate-source voltage of the input transistors. The DM loop is indicated in Blue: the output differential mode bias voltage is measured using a filter (resistors R_{dmfb} and capacitor C_{dmf}, and is used to control the gate source voltage of one of the input transistors.

Bias loop

The bias loop is used to reduce biasing errors introduced by omitting the control of all sources. If the control loop is omitted, the output biasing error is $\epsilon_{out} \approx 810$ V (calculated) or 3.72 mV source referred. This error must be reduced to <500 mV at the output of the amplifier. This means a bias error reduction factor of ≈2000x (rounded-up from 1620 to provide headroom). The bias loop measures the quiescent output voltage and compares this to a reference. The result of the comparison is an error signal. It is processed and fed back into the input of the amplifier to correct for the output offset. The bias loop requires the separation of offset and information carrying signals which are both voltages. The signals can be separated in the frequency domain, as the bias loop will operate at low frequencies, while the signal is contained in a bandwidth several decades higher in frequency.

A method of implementing the bias loop is adding a resistor in parallel to C_{fb}. The difficulty with this method is that it also moves a high-pass pole. The location of this pole must be at least to decades below the high pass corner frequency of the pick-up loop path bandwidth to avoid introducing a gain error larger than 1%. The loop gain at DC is found as:

$$L_{DC} \approx (-g_{m1}) \cdot r_{out,eq2} \| r_{out,I4} \cdot (-g_{m3}) \cdot r_{o3} \| r_{out,I6} = 218 \cdot 10^3. \tag{5.9}$$

or equivalently, 107 dB. To obtain an error reduction of 2000x, the resistor value is found to be 48 kΩ. This would move the high-pass corner to 107 kHz and thus results in insufficient bandwidth. The bias error attenuation factor and pole location can be decoupled by using a bias loop consisting of a filter (the bias filter) and an amplifier (or attenuator as a gain less than 1 is expected). The required gain of the bias amplifier is 0.01 and is found by considering the DC loop gain again. In order not to influence the high-pass roll-of of the signal bandwidth, the bias loop bandwidth must be set sufficiently low. The signal bandwidth crosses 0 dB at 63 Hz. The time constant of the bias filter should be 2000x larger than the 0 dB frequency (16 ms), resulting in a time constant requirement of 32 s. This is too large to implement using passive on-chip components. In the simulator the time constant is implemented using R = 100 MΩ and C = 320 nF to verify the design. The differential version of the circuit (figure 5.20) uses common mode and differential mode signals combined with a filter (with a smaller time constant) for the separation of the signal and bias information. The offset in the differential circuit can be split in a common mode offset component (as a result of biasing errors) and a differential mode offset component (due to device mismatch in the circuit). The common mode bias loop does not require filtering. Its error is of similar magnitude as the bias error of the single ended amplifier. The differential mode bias loop requires filtering. Its error is expected to be ≈ 1.6V (considering 2·2% mismatch in drain currents) and requires a smaller error reduction factor. As a result of the lower reduction factor, the filter pole frequency is increased with a smaller factor, thus the time constant required will be smaller.

5.9. Simulation results

This section describes the simulation results obtained from the design obtained in this chapter. First the small signal behavior (AC simualtion) of the design is verified. Next the noise is considered. The order follows directly from the simulation method of t-spice: first it calculates the AC transfer(s) and then it calculates the noise using these transfers. Finally the drive capabilities (large signal sine wave response) and stability (step response) of the design where tested using transient simulations.

For each simulation type (noise, AC or transient) a dedicated simulation test circuit was used. The controller in these test circuits is a reusable sub-circuit and is shown in figure 5.21.

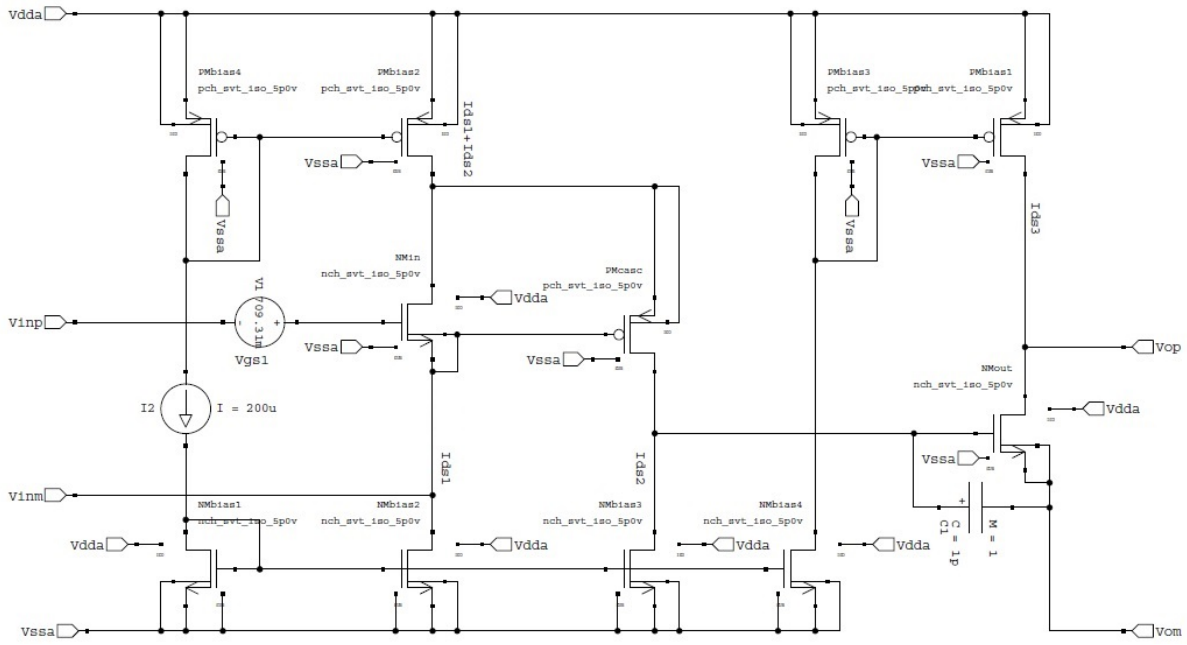


Figure 5.21: The controller sub-circuit.

5.9.1. Small-signal analysis

In figure 5.22 the test circuit for simulating the small-signal behavior is shown. First the circuit is simulated over a large bandwidth to verify the high frequency and low-frequency roll-off using the lumped source model. The Bode plot is shown in figure 5.23 the bandwidth (-3dB) is 6.3 kHz to 120 MHz. The peaking before the low-pass corner is < 1 dB and considered acceptable. After 100 MHz, the lumped model is no longer approximating the behavior of a pick-up loop. Therefore the upwards slope in the magnitude response at high frequencies (>1GHz) is neglected when evaluating stability.

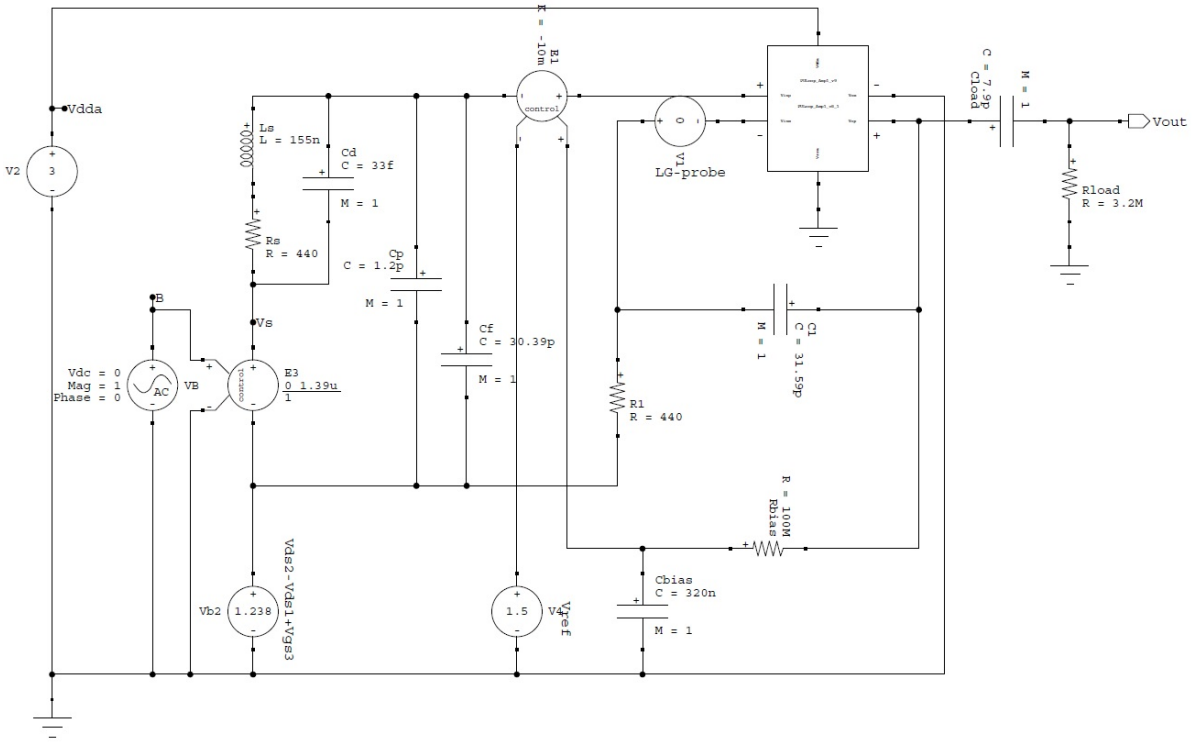


Figure 5.22: Test bench for validating the small signal behavior. The same test bench is used for determining the source referred noise.

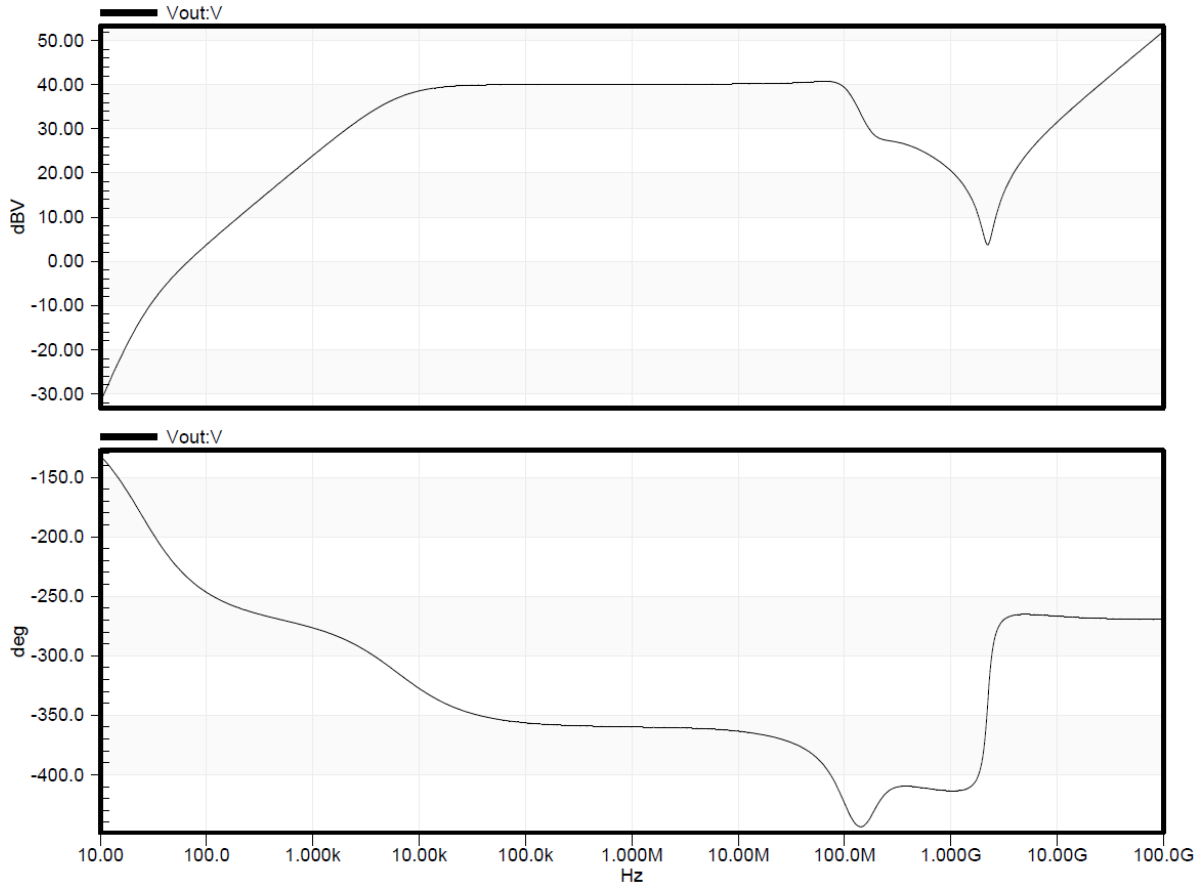


Figure 5.23: Bode plot (magnitude & phase) using the lumped source model.

In figure 5.24 a bode plot of the loop gain is shown. The mid-band loop-gain has a magnitude of 51 dB (at 60 kHz)

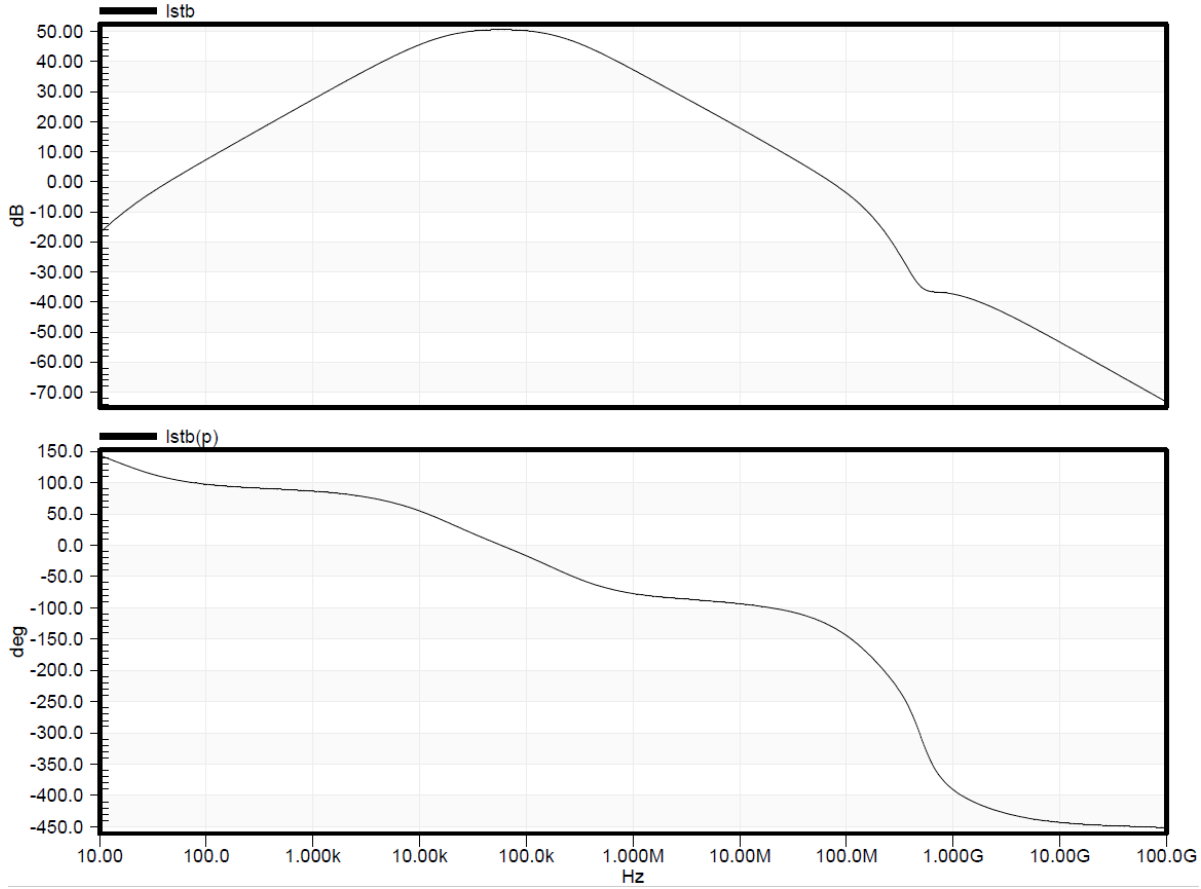


Figure 5.24: Loop gain Bode plot (magnitude & phase) of the pick-up loop amplifier.

After this, the small-signal behavior using the distributed source model is verified. In 5.25 the result is shown. The -3 dB bandwidth is the same as with the lumped model.

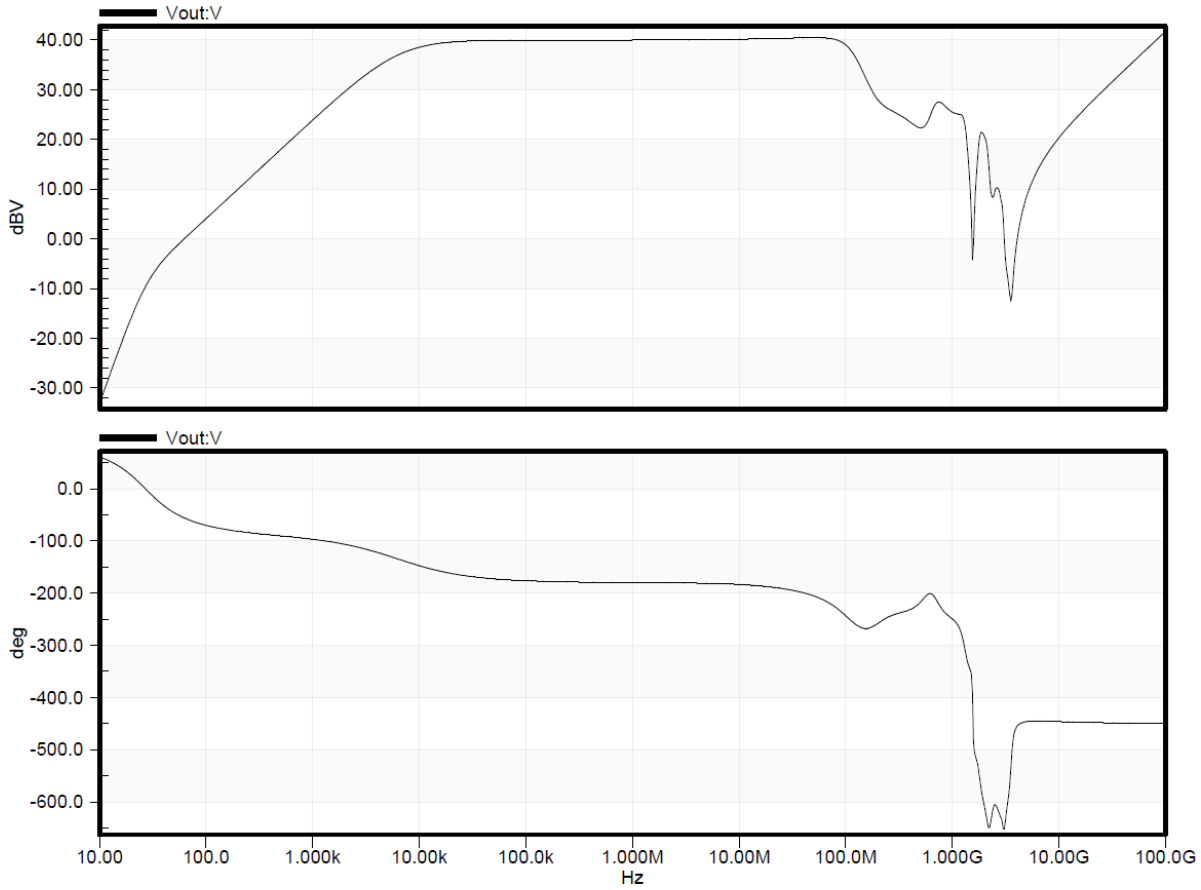


Figure 5.25: Bode plot (magnitude & phase) using the distributed source model.

Table 5.12: Small-signal results

	T-spice sim.	SliCAP sim.	spec.	unit	note
f_l	6.3	6.3	6.3*	kHz	*calculated in section 4.4
f_h	120*	150	5	MHz	*limited in output amplifier
mid-band accuracy	0.37	0.03	1	%	

5.9.2. Noise analysis

For verifying the noise result, the same test bench was used as demonstrated in 5.22. In figure 5.26 the source referred noise voltage spectral density (this represents the source referred magnetic field noise in $T/\sqrt{Hz}$) and the total source referred integrated (RMS) noise voltage (representing T_{RMS}). The top sub-figure indicates that the largest noise contribution appears to result from the first decade of the bandwidth. After 100 kHz the total integrated noise approximates a constant value. This is because the noise density drops below a negligible small value. In table 5.13 an overview of the dominant contributors to the total source referred noise are shown.

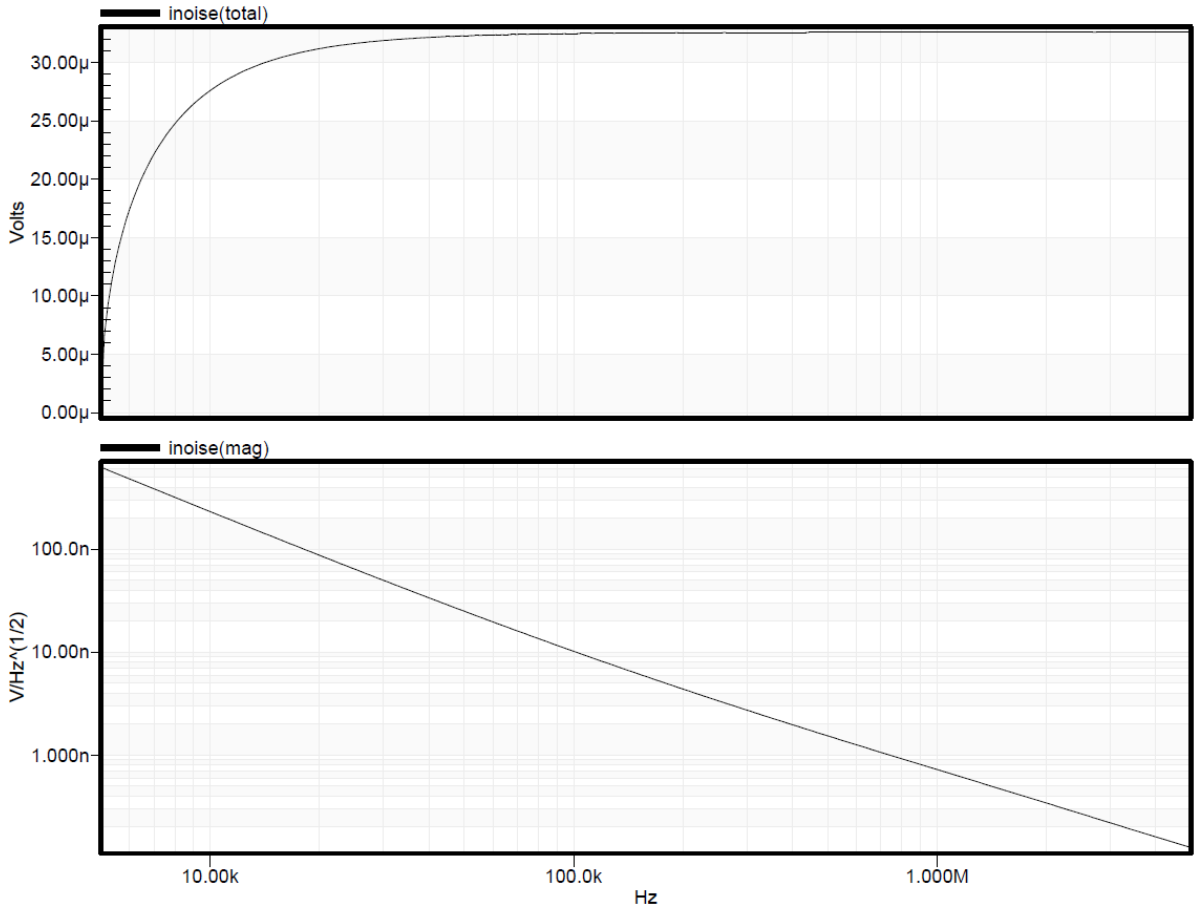


Figure 5.26: Total integrated input referred noise (inoise(total), top plot plane) and source referred voltage noise density (inoise(mag), bottom plot plane).

Table 5.13: Noise result for a bandwidth of 6.3 kHz to 5 MHz

	T-spice sim.	spec.	unit	note
input mosfet M_{in}	30.1	< 32	μT_{RMS}	
source resistance R_s	3.9	4	μT_{RMS}	
feedback resistor R_1	3.9	4	μT_{RMS}	
total source noise	31.62	33	μT_{RMS}	

5.9.3. Transient analysis

The transient behavior of the amplifier was tested using the test bench demonstrated in figure 5.27. The frequency dependent input signal was generated by measuring the short circuit current trough a capacitor. This current is used to control a current controlled voltage source. The output signal of this circuit is proportional to frequency, and thus has an upward slope of 20 dB/decade. First the response of the amplifier using a sinusoidal input signal is described. Second the step response of the amplifier is described.

Figure 5.27: Test bench for validating the drive capabilities and step response.

The steady state sine wave response is shown in figure 5.28. For a full-scale sinusoidal magnetic field input of 8 mT_{PP} with frequency 5 MHz (this is modeled as a voltage with the same magnitude i.e. 8 mV_{PP}), the swing at the gate of M_{in} is ≈ 350 mV_{PP}. The output swing as a result of this signal is 800 mV_{PP}. The output signal is not centered around zero volts. This is because the output filter has not fully settled to its steady state.

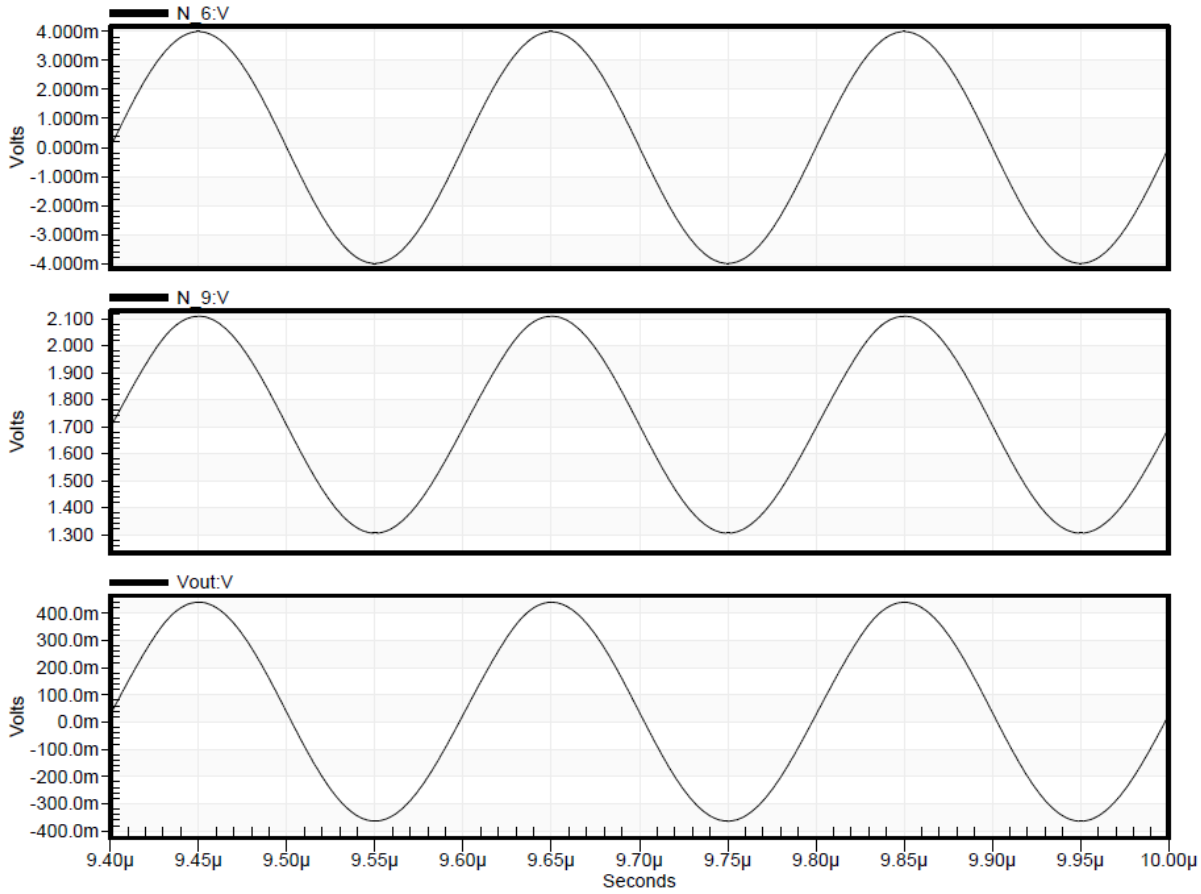


Figure 5.28: Steady state transient response as a result of a 5 MHz sinusoidal input signal with an amplitude of 8mT_{PP}. Top: the input signal representing a sinusoidal magnetic field. Middle: output signal at the drain of M_{out}. Bottom: output signal after the crossover filter.

Figure 5.29 shows the output signal (voltage) after the crossover filter as a result of a square wave input signal (i.e. step response with multiple steps). Again a voltage is used to model the magnetic field input signal. The rise time of the input signal is set to 100 ns. This is done because of the differentiating source to model the conversion of magnetic field to voltage: a very fast changing signal (i.e. large dV/dt) would translate in a very large voltage at the input of the amplifier.

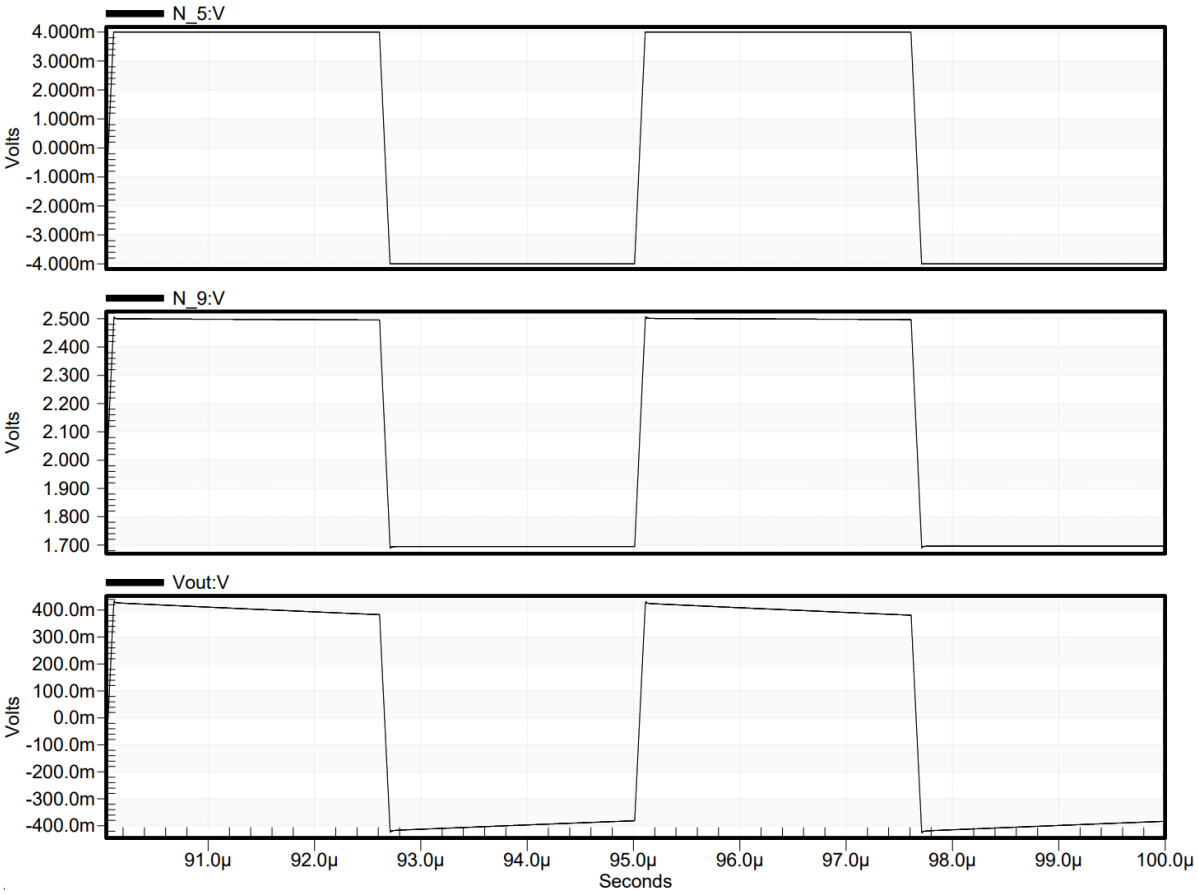


Figure 5.29: Step response using a square wave input signal with an amplitude of 8mT$_{PP}$. Top: Input signal. Middle: signal at the drain of M_{out}. Bottom: the output signal after the cross-over filter.

In figure 5.30 a rising edges is shown, in figure 5.31 a falling edge. The signal at the output follows the input signal. The corners of the pulse shows a minimal amount of overshoot, but the signal settles quickly to its final value.

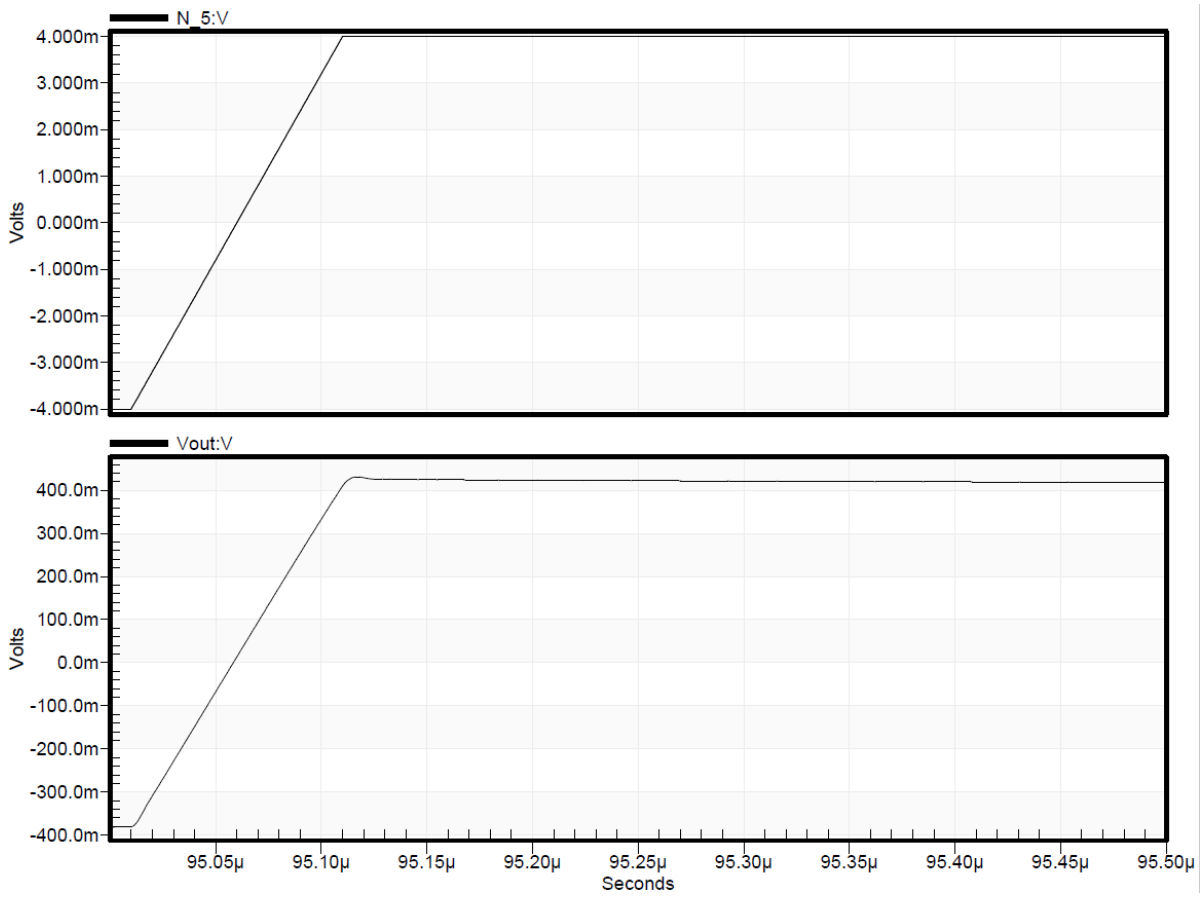


Figure 5.30: Close up of one single rising edge of the signal. Top: Input signal. Bottom: output signal after the cross-over filter.

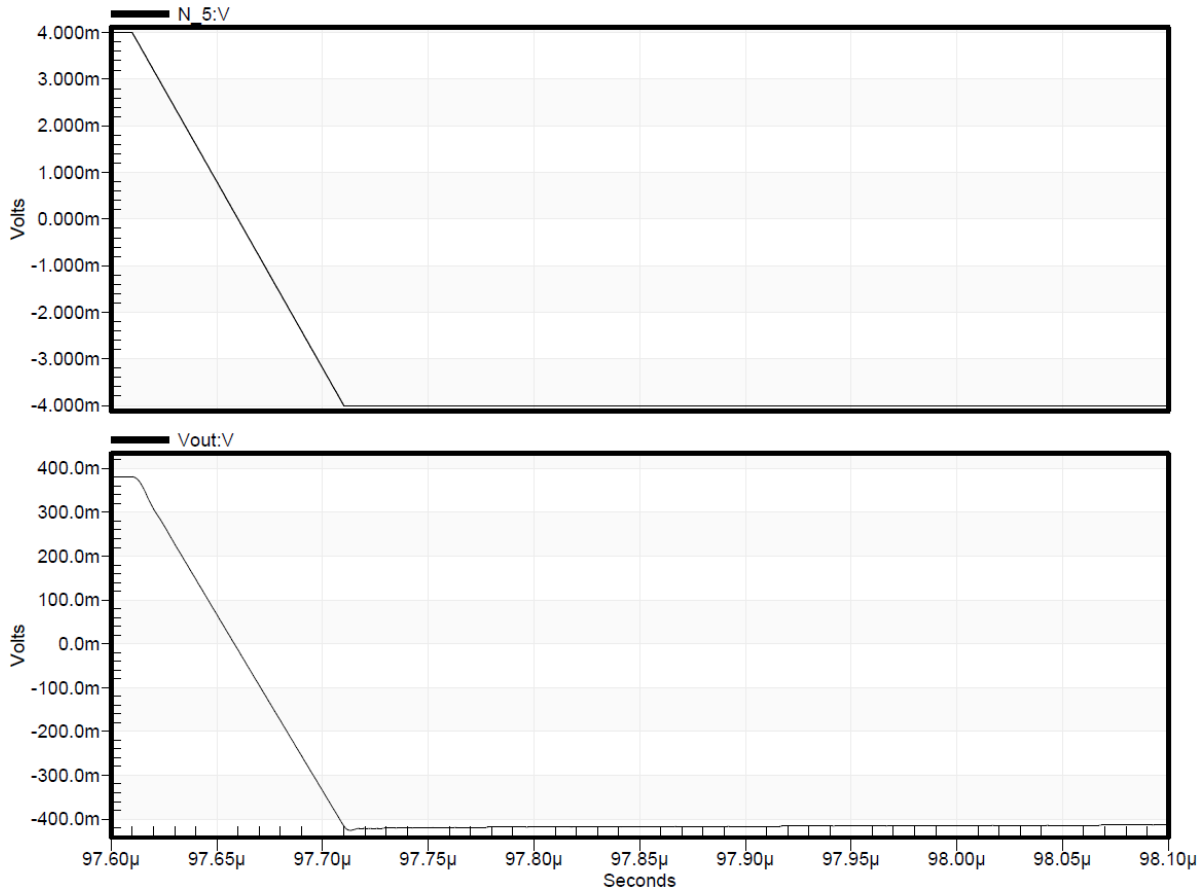


Figure 5.31: Close up of one single falling edge of the signal. Top: Input signal. Bottom: output signal after the cross-over filter.

5.9.4. Cost factors

Finally, the cost factors are considered. A budget for the current consumption was introduced in section 3.6.1. For the area, no requirement was set, except that it must be feasible (thus A $\ll$1mm^2). The results are listed in table 5.14

Table 5.14: Cost factors

	simulation	specification	unit	note
Current consumption	1.2	2	mA_{RMS}	Excluding bias voltage sources and bias loop
Area	195255	$\ll$1000000	$\mu m \times \mu m$	Estimate, excluding bias voltage sources and bias loop

6

Conclusion

In this thesis the design of a pick-up loop amplifier for use in a wide band magnetic field sensor system is described. The system consists of two paths, a low-frequency path using Hall elements and a high-frequency path using a pick-up loop. Compared to a system using Hall elements for both high-frequency and low-frequency information, the use of a pick-up loop in the high-frequency path shows a great improvement in power consumption (or noise, when considering similar power consumption as a Hall based system). This thesis project is limited to the design of the pick-up loop and pick-up loop signal path.

In the third chapter, sensor circuit models and 2 system concepts were described. Simple sensor models, considering a series resistance were described for design of the in-band frequency response. For evaluating the stability, models assuming parasitic components were described. Next two system concepts were introduced. These two concepts only differ in the information carrying quantity used for reading out the pick-up loop. At this point no decision was made on the readout method.

In the fourth chapter, a pick-up loop was designed. The SNR as a function of the wire width and turn count did not provide motivation for design of the pick-up loop, as it is relatively constant over a large range of wire widths. The bandwidth of the pick-up loop is sufficiently large, considering the worst case design parameters and did not provide motivation for the pick-up loop design. In the end its design was motivated by considering the power consumption of the pick-up loop amplifier. Next a dedicated topology for the pick-up loop amplifier was chosen. It was decided to use a non-inverting integrator (V-to-V), as this topology has good common mode immunity when considering a differential amplifier. This decision also fixed the information carrying quantity of the pick-up loop.

In the fifth chapter, a controller design for this amplifier topology is described. In this chapter the focus lies on deriving a single ended amplifier, as the differential circuit requires two of these controllers. The controller circuit is a two stage design, using a cascode input stage and a common source output stage. The biasing of the circuit was not fully completed, as the differential version requires a different bias circuit. The current consumption of the single ended circuit is 1.2 mA (assuming a 5 V supply the power consumption is 6 mW), the total source referred noise is 31.6 μT and the bandwidth obtained is 6.3 kHz to 120 MHz. An overview is listed in table 6.1.

Compared to similar magnetic field sensor systems developed by SystematIC design BV and competitors, a large reduction in power consumption and an increase in bandwidth can be obtained using a hybrid system with a pick-up loop. The total source referred noise is equal to previous sensor systems.

Table 6.1: Results obtained with the pick-up loop path design

parameter	**requirement**	**result**	**unit**	**note**
Bandwidth (-3dB)	5	120 *	MHz	*BW will be limited in output amplifier
Input level	-4...+4	-4...+4	mT	Full-scale
Output swing at V_K	-400...+400	-400...+400	mV	Full-scale, for VDD=5V
Noise	33	31.6	µT	
Power consumption	2	1.2	mA	Biasing: 400 µA, Amplifer: 800 µA
Sensitivity error	<1%	0.37 %	-	
Area	$<<1\cdot10^6$	195255	µm x µm	

Acknowledgments

This project would not have been possible without the help and support of ir. Chris van den Bos, who provided daily guidance during the whole thesis project. I gained a lot of knowledge and confidence from him during the last half year, and I am very grateful for this. Also would I like to thank all staff members of Systematic Design for their help and support. Secondly I would like to thank my supervisors Dr. Ir. Chris Verhoeven and Ir. Anton Montagne for their feedback, support and thrust during the execution of the project. The project was executed in cooperation with Systematic Design BV. The company provided the initial thesis project assignment and a comfortable work environment. Finally I would like to thank my girlfriend Britt van Dijk for helping me with making figures and making the cover design.

A

Apendix A: Magnetic field sensors

A.1. introduction

In this Appendix, six more sensor types are described. The sensors included in this appendix were considered not feasible as an alternative for Hall plates. Each section shortly describes the working principle of these sensors. Motivation is provided why each of these sensor types is considered not feasible. The sensors included in this appendix are: magnetoresistive, SQUID, megneto-optical, nuclear resonant, fluxgate and MEMS magnetic field sensors.

A.1.1. Magnetoresistive

Magnetoresistive (MR) magnetic field sensors vary in resistance when exposed to an externally applied magnetic field [13]. The effect was first discovered in 1857 by William Thomson, later Lord Kelvin [11], and takes place in all metals. He found that the resistivity of some metals reduces if a magnetic field in parallel to a current flowing through the metal was applied. By doing so he was able to reduce the resistance of some metals by a few percent. In the last four decades, new research led to improved sensors types like anisotropic magnetoresistance(AMR), giant magnetoresistance (GMR) and tunnelling magnetoresistance (TMR), with much larger variation of resistance.

Sensors principle

The change in resistance is proportional to the magnetic field strength and field orientation relative to the direction of the current. The resistivity is large for parallel and small for perpendicular magnetic fields. The variations in resistance can be translated into an electric signal by measuring the voltage drop across a MR structure as a result of a forced current. Using the reciprocity theorem, the voltage can also be fixed. In this case, the current flowing through the device contains the information about the magnetic field. The output signal of MR sensors are weakly dependent on temperature variations and have low offset drift. Recent developments use multi-layer structures of ferromagnetic layers separated by conductive (GMR) and even isolating (TMR) materials to increase the MR effect [11, 13, 47, 48]. These ferromagnetic materials are high susceptible to magnetization after application of a strong magnetic field. Their performance changes after application of a strong magnetic field due to hysteresis properties of the material. Therefore MR structures must be (periodically) flipped, to become demagnetized. This reduces their bandwidth and increases the system power consumption. Therefore they are not a valid alternative to Hall plates.

A.1.2. SQUID (Superconducting QUantum Interference Devices)

A SQUID magnetometer combines multiple principles of physic to measure small variations in magnetic flux [11]. A SQUID measures the flux, thus the magnetic field B multiplied by the area of the SQUID loop, rather than the absolute value of the field strength at a single point in space.

Sensors principle

A SQUID magnetic field sensor makes use of superconducting materials, by means of the Meissner effect [11]. A material is said to be superconducting if it is cooled below a certain temperature, known as the transition temperature T_c. Considering a ring of super conducting material, magnetic flux lines will penetrate the material for temperatures above the transition temperature, demonstrated in figure A.1a. If the temperature is lower than the transition temperature, the magnetic flux lines are expelled from the material, demonstrated in figure A.1b. This can be explained using maxwell's laws: a magnetic field gradient cannot exist inside a superconductor. After removing the external field, a induced current I circulates inside the ring, keeping the flux confined constant. This situation is demonstrated in figure A.1c.

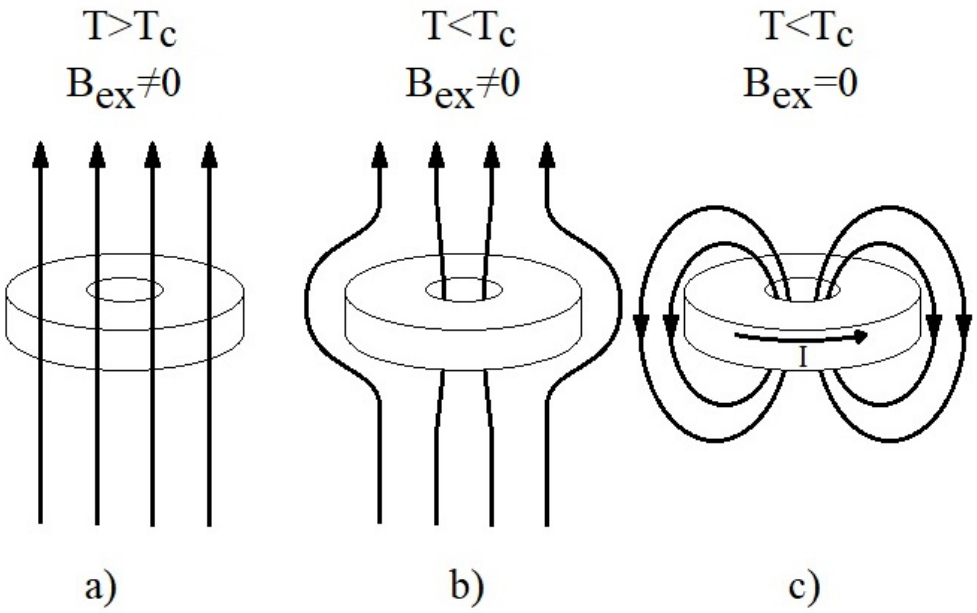


Figure A.1: Meissner effect in a ring of conductive material.

The flux level inside the ring cannot take on any arbitrary value. It appears quantized, in integer steps of flux quanta's $\Phi_0 = \frac{h}{2e}$. The induced current flows for eternity, as the ring has zero resistance. If the ring would be cut open on one side and a piece of 'normal' resistive material is introduced in the gap, a deviation from classical physics is found. It is expected, from classical physics point of view, that the resistive material would introduce a voltage drop, and thus the current trapped inside the loop would quickly decay to zero. Using modern physics, thus assuming a wave like property of electrons, the piece of resistive material can be seen as a finite potential barrier. Below a certain current (critical current I_c) and for a path length less than the penetration depth of the incident wave, electrons tunnel through the barrier of resistive material, with zero voltage drop. Therefore the current will continue to flow like in a normal superconducting ring. The resistive barrier is called a Josephson junction and the effect of electrons penetrating the barrier is called the Josephson Effect. Above the critical current a voltage drop across the junctions will appear, resulting in a decay of the current. By measuring the voltage drop, the external magnetic field strength is found.

Similar to the critical temperature the superconducting state also is influenced by the external magnetic field strength. Below this field the superconducting state occurs and above the critical field the resistance of the conductor is non-zero. In figure A.2, the shaded area represents the temperature and magnetic field region where the superconducting state occurs. The critical field is found to be related to the temperature via the following parabolic relation:

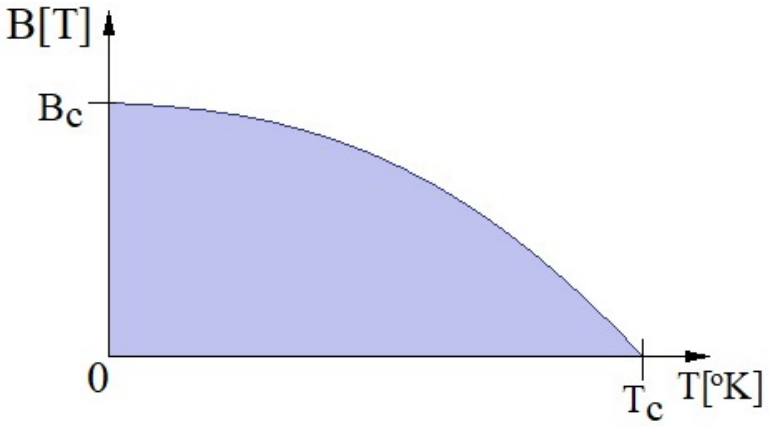


Figure A.2: The critical temperature and magnetic field strength. The purple area indicates where the conductor is superconducting.

$$B_c(T) \approx B_0 \left[1 - \left(\frac{T}{T_c} \right)^2 \right] \tag{A.1}$$

where T is the temperature, T_c is the critical temperature, B_0 is the critical field intensity at absolute zero temperature and H_c the resulting critical field intensity. This field strength dependency of the superconducting state limits the SQUID in the maximum detectable magnetic field strength. If the external field is larger than the critical field strength, the loop becomes resistive, resulting in a quick decay of the current inside the loop: the flux is now no longer trapped inside the loop. The highest critical field intensities reported are 80 mT for Lead and 190 mT for Niobium, well below the 1T requirement [**?**]. This means that a SQUID is not a feasible solution to replace a Hall plate.

A.1.3. Magneto-optical

Based on the faraday effect, the polarization of monochromatic light is rotated if traveling through a magneto-optic medium placed inside a magnetic field, demonstrated in figure A.3 [11]. The rotation takes place if the magnetic field is in parallel to the propagation direction of the light. The rotation of the polarization plane of a light wave is called Faraday rotation.

Sensors Principle

For para- and diamagnetic materials the angle of rotation is proportional to the external magnetic field H and the length of the magneto-optical material. The relation between field intensity and rotation is:

$$\theta = HVd \tag{A.2}$$

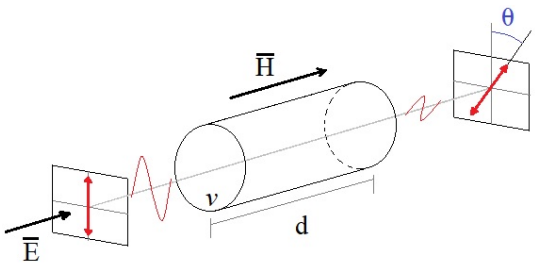


Figure A.3: A demonstration of the faraday effect; light is rotated when passing through an magneto-optic medium exposed to a magnetic field in parallel to the propagation direction.

where d is the length of the magneto-optic material, V is the Verdet constant of the material, B the magnetic field strength and θ the resulting Faraday rotation. Assuming a coil with N loops of optic material surrounding a conductor carrying current i_c, the equation can be rewritten to [49]:

$$\theta = VNi_c \tag{A.3}$$

The angle of rotation can be measured by passing the light through an analyzer (45° polarizer) and measuring the intensity using a photoreceiver. The output light intensity I_d is given by:

$$I_d = \frac{I_0}{2(1+\sin 2\theta)} \tag{A.4}$$

The sine function can be approximated by a linear function for small rotation angles θ. I_0 in this equation represents the light intensity of the input light wave. The value of I_0 must be accurate, as it is directly influencing the output signal. A solution of this problem , assuming small rotations, is to split the light beam into two equal parts with a 45° difference in polarization using a Wollaston prism [49].

$$S = \frac{I_1 - I_2}{i_1 + i_2} = \sin 2\theta \approx 2VNi_c \tag{A.5}$$

where I_1 and I_2 are the two output light intensities. Using this method, the input light intensity is no longer appearing in the output signal. As mentioned above, this relation is only valid for limited values of θ, as it approximates the sine function with a linear expression. For large values of θ, the nonlinear behavior of the sine function becomes too large to use this approximation. Another option to mitigate the influence of the light source intensity is to use a light source with a spectrum of wavelengths, equivalently a chromatic light source [11]. The infrared content of the light beam will not be influenced by the polarizer and will therefore not be influenced by the magnetic field. This part of the light spectrum will therefore serve as a reference signal. The most promising results are obtained using optic materials with ferromagnetic content. These materials have Verdet constants in the order of 100...1000 rad·T^{-1}·m^{-1} for light with 635 nm wavelength [50]. This allows optic path lengths below 10 mm. As the faraday effect is a nonreciprocal property of the material, bouncing the light once back and forward in the material would translate in twice the rotation, thus reducing the physical size of the magneto-optic material. However, due to the non-linearity of the sine function, the detectable rotation is limited, $\theta << 90°$. The Verdet constant is wavelength depended and reduces the rotation angle for larger wavelengths. The drawback of using ferromagnetic materials is that the simple relation

between the magnetic field intensity and rotation no longer holds. The angle of rotation for small field intensities is still found using the simple relation. But for strong fields, perming effects occur, the rotation is set by the magnetization state of the material, where the sign of rotation is determined by the direction of magnetization. Paramagnetic and ferromagnetic materials are very temperature dependent when considering the polarization rotation. Diamagnetic materials on the other hand are characterized with minimal temperature dependence ($10^{-4}\%K^{-1}$), but have much lower Verdet constants thus requiring much longer optical path lengths. Therefore a practical magnetic transducer based on the faraday effect is limited in the minimal size. Another issue imposed by the optic material is linear birefringence. This causes the light intensity at the detector to drop. The birefringence should therefore be low and constant over temperature to make accurate measurements of the magnetic field. Practical magneto-optical sensors make use of optic fiber wrapped around a conductor [51]. The fiber is made of non-ferromagnetic glass, owing a low but relative temperature insensitive Verdet constant. Therefore the length of the optic path must be made long to yield a useful amount of faraday rotation. Using this method makes an integrated on-chip solution unfeasible.

A.1.4. Nuclear resonant magnetometer

Nuclear resonant magnetometers make use of the resonant behavior of atoms/molecules when subjected to an magnetic field [11]. The method is mostly limited to measuring weak magnetic fields and can detect DC magnetic fields.

Sensors principle

The most common resonant magnetometer is the proton precession magnetometer [52]. A sample of hydrogen rich fluid is exposed to a strong homogeneous magnetic field. Hydrogen is favored, as it has a high proton to electron count. Large numbers of electrons would 'shield' the protons from external fields. Other hydrogen rich fluids can be used, like hydrocarbons. Part of the protons in the fluid sample align with the external magnetic field. After the external magnetic field is switched off, the protons rotate back into their original orientation, aligned with the external magnetic field. The rotation back to this initial state is at a frequency directly proportional to the external magnetic field, the process is called Larmor precession. The process generates a small magnetic field. The relation between the external field and the frequency is found to be [52]:

$$f_p = \frac{\gamma_p}{2\pi} B_0 \tag{A.6}$$

where f_p is the precess frequency, γ_p (the gyromagnetic ratio) a material dependent constant and B_0 represents the external field. The field generated by the rotation back to the initial state is detected (using a coil for example) and by measuring the frequency, the magnetic field intensity can be resolved. The result only gives information about the magnitude of the field, but not the orientation. An improved version of the proton precession magnetometer makes use of the Overhauser effect, and uses a mixture of hydrogen rich fluid and free radicals [53]. This type of magnetometer is using a HF field to align the electron spin of the radicals, and via the Overhauser effect, these will couple the alignment to the protons. A great reduction in energy consumption is made by using a HF field to replace the DC field. The hydrogen rich fluid required for this transducer to operate severely limits the possibility for integration on a silicon substrate. For example water, is a highly corrosive material that is preferably kept away from a Si substrate [25, 54]. If the water could be contained in a hermetically sealed container, but miniaturization of the sensor is difficult. Therefore nuclear resonant sensors are not a valid candidate to replace the Hall plate.

A.1.5. Fluxgate

Fluxgate sensors offer low noise measurement of the intensity and direction of a magnetic field over a wide temperature range [55]. They are capable of measuring static and LF magnetic fields.

Sensor principle

A basic fluxgate, shown in figure A.4 [11], consists of a pair of coils wound on a rod of high permeability ($\mu_c >> 1000 \cdot \mu_0$) core material. It operates by modulating the DC flux associated with the measured magnetic field by changing the core permeability. The core is periodically saturated, resulting in a change of the permeability. One winding (excitation) is used for saturating the core, using an excitation current I_{ex}. The second winding (sensing) is used for measuring the external field. The excitation coil induces voltage V_s into the sensing coil. The voltage is modulated by the net flux inside the core. The information about the field intensity is embedded in the second and higher even harmonics of the sensing coil voltage. Like a pick-up loop the number of (secondary) turns influences the output voltage directly.

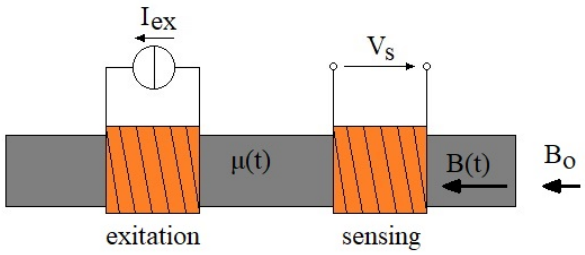


Figure A.4: Basic fluxgate.

Fundamental performance properties

Fluxgate sensors can be made on chip and can operate over a wide temperature range [55]. Like the pick-up loop, thermal noise is introduced due to the parasitic resistance of the winding's. A second noise source is found in the core material quality, especially for vacuum deposited thin-film core types. The bandwidth ranges from DC and is limited by the resonant frequency (parasitic capacitance of Ls introduces a resonant circuit). If a lower frequency is used to drive the excitation coil, the bandwidth will be limited by this lower frequency. The maximum detectable field intensity is limited by the strength of the magnetic flux generated by the excitation coil to saturate the core. Typical thin film core's deposited on-chip are made of Permalloy and have a saturation flux density of 0.8 T. The linear operating range of a fluxgate using a Permalloy core would be even smaller than its saturation level. This introduces a upper limit to fields of several 100 mT on the dynamic range of the fluxgate. This could be mitigated by using the fluxgate in a feedback system as null-detector. The drawback is the increased power consumption caused by the drive current. Therefore the fluxgate is not a valid solution to replace a Hall plate.

A.1.6. MEMS (Mechanical Electric Micro Systems)

Mechanical Electric Micro Systems offer a vast number of new possibilities for magnetic field sensors. Two common types where selected for review, but many other MEMS type magnetic field sensors exist [56–59]. The first type uses the Lorentz force to make a structure move. The second type makes use of a small permanent magnet, that under influence of an external magnetic field experiences a rotational force, or equivalently torque. Again the force is used to move or deform (i.e. applying stress) a structure. Typically these structures are made to resonate at their resonant frequency, referred to as normal mode. This greatly increases sensitivity, and mitigates the influences of external vibration sources. Above the normal mode frequency, parasitic resonance may occur. Preferably the frequency of the parasitic modes is much higher than the normal mode frequency.

Sensor principle: Lorentz force

Figure A.5 shows a possible construction for a MEMS magnetic field transducer based on the Lorentz force acting on a moving charge. A current carrying conductor placed inside a magnetic field experiences a force perpendicular to the magnetic field direction [60]. The transducer consist of a U-shaped cantilever structure with a conductor on top, anchored rigid into the substrate on one side. In general the Lorentz force acting on the conductor is found as:

$$\boldsymbol{F_L} = \boldsymbol{I}\, l \times \boldsymbol{B_0} \tag{A.7}$$

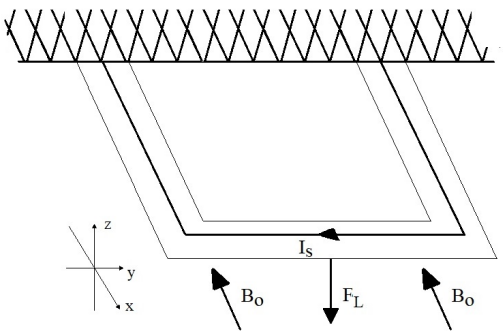


Figure A.5: MEMS magnetic field sensor based in the Lorentz force acting on a current carrying beam.

where I is the current vector, l the length of the current path in the y direction, B_0 the magnetic field vector and F_L the magnetic force vector. The magnitude of the force perpendicular to the magnetic field is found as:

$$F_L = IlB\sin\theta \tag{A.8}$$

where θ is the angle between the magnetic field and the current. The force can be used to move the cantilever structure and using for example optical, capacitive or piezo-electric structures, the movement can be translated into an electric signal.

Sensor principle: Permanent magnet

Figure A.6 shows a MEMS based magnetic field transducer based on the rotational force experienced by a permanent magnet contained in an external magnetic field B [61]. It consists of a very thin cantilever bar, anchored to the substrate on one side. A small piece of permanent magnetic material is deposited on the end of the cantilever bar, where M is the magnetic moment of the permanent magnet (the square labeled PM). An external magnetic field applies torque onto the permanent magnet, as it wants to rotate to align its magnetic moment with the external field. The relation between torque and field strength is found as:

$$\boldsymbol{\tau} = \boldsymbol{M} \times \boldsymbol{B} \tag{A.9}$$

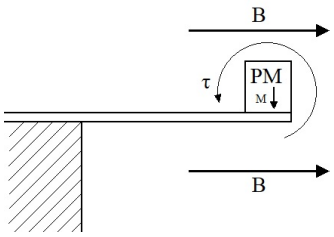


Figure A.6: MEMS magnetic field transducer using a permanent magnet.

where τ is the resulting torque, M the magnetic moment and B the magnetic field. The torque applies stress (resuting in deflection) on the cantilever, resulting in a change of the resonant frequency. By measuring the frequency change, the magnetic field intensity can be resolved.

Fundamental performance properties

The bandwidth of resonant sensors is limited by their resonance frequency. Using a low Q-factor, the bandwidth can be increased at the cost of a lower sensitivity. When subjected to strong magnetic fields the cantilever structure can be bend sufficiently far to make it touch the Si substrate. In this situation there is a high chance the beam will stick to the substrate due to atomic bonding. Therefore MEMS based magnetic field sensors are not an alternative for Hall plates.

A.1.7. Discussion

From this research a number of valid competitors for the Hall plate emerged. In the table below an overview of these sensor types is shown. It ranks them using +, − and 0 using the first 5 columns. A question mark is used if no data was available. The last column indicates the use of ferromagnetic materials.

	Noise	Max-Signal	BW	power	Size	Ferromagnetic
	+ = low noise	+ = large signal	+ = large BW	+ = low power	+ = small area	
Hall plate	-	-	+	0	+	No
Pick-up loop	+	+	+	+	-	No
Magnetoresistive	-	+	+	0	+	Yes
SQUID	+	+	+	-	-	No
Magneto-optical	?	0	+	0	-	Optional
Nuclear resonant	?	0	?	-	-	No
Fluxgate	+	+	+	-	-	Yes
MEMS	+	+	-	-	0	Optional
Vacuum magnetic	0	0	+	0	-	No

In Figure A.7 the input range of all investigated magnetic field sensors is shown.

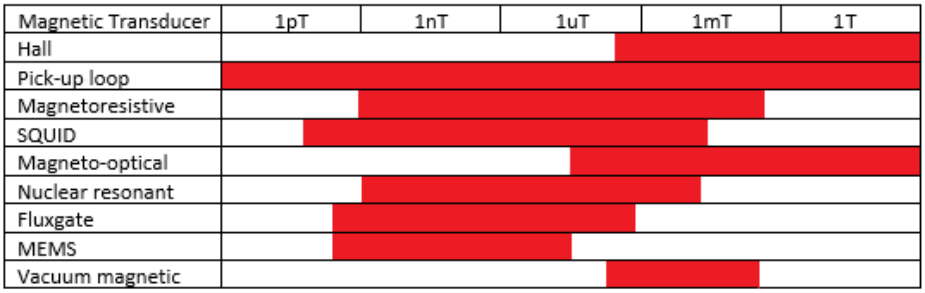


Figure A.7: Comparison of the input field range of several transducer (sensor) types [13]

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