The systematic design of a spectrum shaping analog front end for neural signal acquisition

by

M. K. Elboushi

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Thesis committee:	Prof. dr. ir. W. A. Serdijn,	TU Delft, supervisor
	Dr. ir. M.A.P. Pertijs,	TU Delft
	Dr. D. G. Muratore,	TU Delft
Date:	OCT 2025	

TU Delft

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Abstract

Neural signals exhibit a $1/f^n$ spectrum, spanning low-frequency local field potentials (LFPs) and higher-frequency action potentials (APs), which imposes tight constraints on noise, power, area, and tolerance to electrode DC offsets. This thesis presents a second-order Δ–ΔΣ analog front end (AFE) that performs spectrum equalization for direct digitization of neural signals. A state-space methodology separates the design into transfer-function specification, topology selection, and circuit implementation; an orthonormal ladder representation provides intrinsic state scaling and maximizes dynamic range. At the circuit level, a dynamic translinear (log-domain) equalization loop removes the need for a multi-bit DAC, reducing digital overhead.

Implemented in TSMC 180 nm BCD technology, the AFE occupies an estimated $0.00505\,\text{mm}^2$ per channel and consumes $41.12\,\mu$W in total ($7.11\,\mu$W in the G_m–C integrators, with the remainder in the quantizer, DACs, and DTL block). The measured input-referred noise is $3.45\,\mu\text{V}_{\text{rms}}$ in the AP band (300–10 kHz) and $14.08\,\mu\text{V}_{\text{rms}}$ in the LFP band (0.5–1 kHz), with a peak SNDR ≈ 69.8 dB for a $20\,\text{mV}_{\text{pp}}$ input.These results validate that spectrum-equalized Δ–ΔΣ AFEs, when designed with structured state-space methods and g_m/I_D-guided sizing, offer an efficient and scalable solution for large-scale neural recording systems.

Contents

1 Introduction

CMOS high-density neural recording probes have become indispensable tools in neuroscience research, enabling massive recordings of single-cell neural activity across different brain regions [1]–[3]. Over the past decade, there has been tremendous progress in the engineering of tools designed to interact with the nervous system, from signal detection and processing to restoration and functional enhancement [4]. While conventional extracellular probes provide excellent spatial and temporal resolution, they are limited to recordings from only a few dozen neurons per shank [4]. In contrast, CMOS neural probes allow large-scale recordings at single-cell resolution across multiple brain regions, establishing a new standard in electrophysiology [5].

The high spatial resolution of these probes also drives the development of implantable brain–computer interfaces (BCIs), which enable direct communication between the brain and external devices. Beyond unidirectional control, bidirectional BCIs open opportunities for closed-loop neuromodulation [6], potentially transforming the way neural disorders are studied and treated [7].

Despite these advances, developing readout circuitry to interface with high-density neural probes introduces several challenges [8]. These include area and power efficiency, signal characteristics, noise management, input impedance and biasing, connectivity, data handling, biocompatibility, and non-idealities. Achieving higher channel density requires minimizing per-channel area. In addition to the total power density, while maintaining low-noise performance. Neural signals are inherently weak, ranging from tens of microvolts to millivolts [4], which demands low-noise amplification while rejecting large and drifting electrode DC offsets (EDOs).

EDOs arise from the electrode–tissue interface, where electrochemical reactions generate a DC potential difference. At the microscopic level, each electrode in contact with the ionic medium of brain tissue develops a half-cell potential, which is necessary to enable the conversion between ionic and electronic currents [4], [8]. Since the recording and reference electrodes are typically fabricated from different materials and exhibit variations in geometry, surface properties, and local ionic concentrations, their half-cell potentials do not cancel each other out. The difference between them manifests as the electrode DC offset. These offsets can reach tens of millivolts, which poses a significant challenge to low-dynamic-range analog front-ends. Moreover, EDOs are not constant but drift over time due to slow electrochemical processes at the electrode–electrolyte boundary, further complicating stable signal acquisition [4].

Noise from intrinsic device sources, digital coupling, and the electrode-tissue interface can further degrade recording quality. In addition, the high impedance of small electrodes necessitates careful input bias network design to avoid signal attenuation while maintaining stability. Thus, a robust readout architecture must simultaneously tolerate large, drifting EDOs and preserve sensitivity to the microvolt-scale neural signals. Moreover, power consumption must remain strictly limited to prevent excessive heat dissipation into the surrounding tissue, as even small temperature increases (typically constrained to less than $1^{\circ}C$) can cause irreversible neuronal damage [9].

This chapter is organized as follows. Section 1.1 introduces the concept of systematic design methodologies and explains how they can be applied at both the system and circuit levels. The state-space approach for $\Delta\Sigma$ converter design is presented in Section 1.1.1, illustrating how the design problem can be separated into transfer function, topology, and circuit phases. Section 1.1.2 introduces the g_m/I_D design methodology for circuit design, which provides a structured means of transistor sizing and biasing. Section 1.2 outlines the overall organization of the thesis, and Section 1.3 concludes the chapter by summarizing the motivation and stating the research question.

1.1. Systematic Design Methodology

The previous section highlighted that designing Analog Front Ends (AFEs) for neural signal acquisition is challenging due to the difficulty in balancing power, area, EDO, and noise. This work suggests that using systematic design methods at different levels of abstraction can lead to designs that are easier to replicate, adapt to different technology nodes, and achieve high performance with fewer design iterations. To support this, two systematic approaches will be introduced, one at the system level [10], [11], and one at the circuit level [12].

1.1.1. State Space Approach for Optimal Design of $\Delta\Sigma$ Converters

As previously stated, the power and noise specifications pose a major design challenge. Hence, it is interesting to investigate if further system-level optimizations could be performed to yield better specifications.Past work [13] [10] suggest that a state space-based approach could be used to design an AFE with arbitrary transfer characteristics.

The state space approach reported in [10] (based on [11]) relies on separating the design problem into three phases:

1. the filter transfer function design phase,
2. the filter topology design phase
3. the filter circuit design phase.

During the first design phase, a set of requirements is used to derive a transfer function whose Laplace transform can be expressed in a proper rational function of low order. In the second phase, the transfer function will be mapped to a specific topology, or an optimal one could be mathematically derived [11]. Finally, low-level implementation of the filter's blocks on the transistor level is carried out.

Applying this separation to the design of an AFE for cardiac signal monitoring, Rout [13] demonstrated the effectiveness of the three-phase methodology introduced in [11]. By systematically deriving the transfer function and mapping it to an orthonormal high-pass $\Sigma\Delta$ topology, the design showed significant improvements compared to canonical forms, including reduced sensitivity to coefficient variations, improved dynamic range, and a better overall figure of merit. These results illustrate how the methodology can translate a complex analog design problem into structured phases, a principle that will be extended in this thesis to the neural signal acquisition domain.

With regards to the second design phase, multiple different state space representations can be used to realize the loop filter. Common options include the observer canonical form, the bi-quad form, and the orthonormal-ladder filter form. Among these, the orthonormal ladder filter topology [14] provides distinct advantages, as also emphasized in [11]. A key property of this representation is that it is inherently state-scaled: each state variable is normalized such that its maximum amplitude is bounded, leading to optimal use of the available signal range in the circuit implementation. In other words, the available dynamic range is distributed evenly across all states. This intrinsic scaling not only improves the achievable dynamic range, but also ensures that no single state dominates the internal node voltages or currents, thereby enhancing robustness. Furthermore, the orthonormal representation exhibits reduced sensitivity to coefficient variations, making it less susceptible to process and mismatch-induced errors, and it allows for straightforward implementation of high-order, arbitrary filter transfer functions. When this form was compared to the observer canonical form in the design of a third-order high-pass

ΣΔ modulator [10], it demonstrated superior performance, particularly in terms of noise reduction. For these reasons, the orthonormal ladder filter topology described in [10] is of particular interest for adoption in the design of an AFE for neural signal acquisition.

1.1.2. The g_m/I_D Design Methodology for Circuit Design

Analog front ends are typically constructed from common building blocks such as amplifiers, filters, and analog-to-digital converters. The components used to build these blocks are mostly transistors, resistors, and capacitors. Achieving state-of-the-art specifications requires proper sizing and biasing of the transistors within these blocks, which in turn demands a design methodology that can systematically manage the trade-offs between noise, power, and area. While many designers rely on intuition and iterative refinement, such approaches do not guarantee optimality. A structured methodology is therefore necessary.

Historically, transistor sizing relied on the square-law model, which offered simple analytical relations but became increasingly inaccurate with modern CMOS technologies. As scaling progressed, second-order effects such as velocity saturation, mobility degradation, and drain-induced barrier lowering introduced large errors in strong inversion, while moderate and weak inversion were not captured at all [12], [15]. This led to a situation where design points derived from the square-law model frequently failed to meet specifications, requiring extensive iterative tuning in simulation [12], [16]. Although such an approach can succeed when guided by experience, it is unstructured, difficult to port across technologies, and exposes too many design knobs simultaneously [17].

A more systematic alternative is the g_m/I_D methodology, first proposed in [18] and further refined in [12]. The key idea is to characterize device behavior using precomputed lookup tables (LUTs) obtained from simulation sweeps. These tables map normalized small-signal parameters and figures of merit to the transconductance efficiency g_m/I_D, which serves as the primary design variable. Unlike overdrive-based sizing, this approach is valid across all inversion regions and directly reflects modern device models. The LUTs also provide normalized current density (I_D/W), intrinsic gain, and output resistance, enabling straightforward calculation of transistor width and bias conditions once the inversion level and channel length are chosen. In practice, this reduces the analog design problem to selecting three main knobs: inversion level (g_m/I_D), channel length (L), and current budget (or a derived figure of merit).

In this thesis, the g_m/I_D methodology will be used in Chapter 4 to design the key circuit blocks of the neural AFE. By providing a structured link between high-level performance requirements and transistor-level implementation, it ensures that the architectures derived in Chapter 3 can be systematically realized while minimizing design iterations and maintaining portability across technology nodes.

1.2. Conclusion

This chapter introduced the motivation for designing analog front ends for neural recording and highlighted the main challenges associated with such designs, including power, area, noise, and electrode DC offset tolerance. To address these challenges, this work adopts a systematic methodology at both the system and circuit levels. At the system level, the state-space approach provides a structured means of deriving transfer functions and mapping them to optimal topologies. At the circuit level, the g_m/I_D methodology enables systematic transistor sizing and biasing to realize the required building blocks while maintaining consistency across technology nodes.

Based on this context, the central research question of this thesis is formulated as follows:

> How can systematic design approaches be applied to develop a spectrum-shaping analog front end for neural signal acquisition at the transfer function, topology, and circuit levels?

The remainder of this thesis builds on this question by first reviewing the state of the art, then applying the chosen methodologies to high-level modeling, circuit design, and implementation.

1.3. Thesis Organization

This thesis is structured as follows. Chapter 2 presents a literature review on analog front ends (AFEs) for neural recording systems. Chapter 3 develops a high-level model of a direct-digitization analog front end based on a $\Delta - \Delta\Sigma$ topology, including architectural considerations, state-space design, and modeling. Chapter 4 details the transistor-level implementation of the key circuit blocks using the g_m/I_D design methodology and precomputed lookup tables. Finally, Chapter 5 reports the simulation results and evaluates the performance of the proposed design against state-of-the-art requirements, and Chapter 6 concludes the thesis, highlighting the main contributions and recommendations.

2

Literature Survey

2.1. Introduction

This chapter reviews state-of-the-art analog front ends (AFEs) for neural signal acquisition. While CMOS neural probes have enabled large-scale, high-resolution recordings, the readout circuitry must address stringent constraints on area, power, and noise. In addition, AFEs must tolerate large electrode DC offsets (EDOs), handle both local field potentials (LFPs, 0.5–100 Hz) and action potentials (APs, 0.3–10 kHz), and provide sufficient dynamic range to accommodate artifacts from stimulation or movement [4], [8].

To meet these requirements, several AFE architectures have been proposed. The conventional approach [1] combines an AC coupled instrumentation amplifier (IA) with a low-resolution successive approximation register ADC (IA+ADC). The IA+ADC approach relies on analog-intensive techniques to implement the front-end IA and, in some cases, the bandpass filter to separate LFP and AP bands, which makes their scalability with technology difficult [8].More recent approaches employ direct digitization utilizing moderate-resolution ADCs (8-11 bits) to directly digitize raw neural signals [19], [20].). The large EDOs can be either compensated through mixed-signal DC-Servo loops (DSLs) or filtered by conventional AC-coupling.

This chapter highlights these architectures, discusses input coupling strategies (AC vs. DC), and compares recent designs in terms of noise, power, and area efficiency. The goal is to derive state-of-the-art requirements that motivate the design methodology explored in the following chapters.

2.2. State of the art AFE for Neural signal Acquisition

With the rapid scaling of neural probes discussed in Chapter 1, there is a growing demand for analog front-ends (AFEs) that balance noise, power, and area efficiency. A widely adopted solution in the literature is the IA+ADC architecture, where a high-gain instrumentation amplifier (IA) drives a low-resolution, power-efficient ADC [3], [21]–[26]. The IA ensures that neural signals in the μV range are boosted before further processing, so that downstream ADCs and filters don't need to meet extreme noise requirements[1].

However, this benefit comes with significant drawbacks. First, the IA is highly susceptible to saturation from electrode DC offsets (EDOs) and stimulation artifacts, which degrades the overall signal-to-noise-and-distortion ratio (SNDR). While DC servo loops [21] and AC coupling [24] have been proposed to mitigate this issue, they add complexity and overhead. Second, the IA's limited input impedance (Z_{in}) interacts with the high electrode impedance, leading to signal attenuation [4]. Finally, the reliance on complex analog circuitry limits scalability, making it increasingly difficult to meet area and power budgets as the number of channels grows.

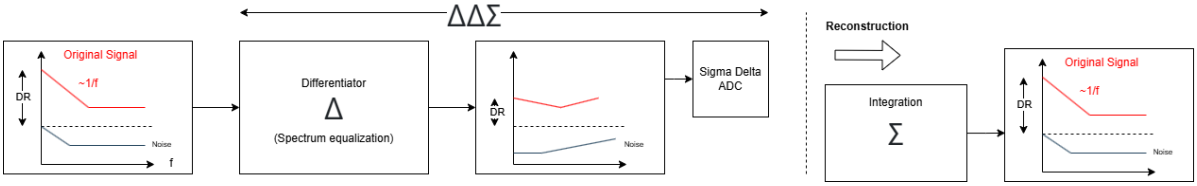


Figure 2.1: Spectrum equalization scheme used in $\Delta^2\Sigma$ AFEs

To address the short comings of the IA+ADC architecture, direct digitization architectures were proposed in literature [27] [19] [20] [28] [6] [29] [30] [31]. These architectures typically utilize a $\Delta\Sigma$ or $\Delta\Sigma$-like modulators to exploit the oversampling nature of $\Delta\Sigma$-like modulators and noise shaping techniques to achieve good noise performance. By eliminating the IA from the design, impressive area gains could be achieved. However, due to the absence of a gain stage, the ADC would require a high dynamic range specification to process the μV range neural signals. The high dynamic range (DR) specification requires a lower noise budget, which can only be reduced by increasing power consumption. Hence, designing a power-efficient AFE is highly dependent on the ability to reduce the input signal's DR [28].

Thus, recent literature [27][20][19] has proposed the so-called $\Delta - \Delta\Sigma$ ($\Delta^2\Sigma$) architecture for spectrum equalization. These architectures take advantage of the fact that neural signals possess a $1/f^n$ spectrum (where $n = 1-2$) at low frequencies. By taking the temporal difference of samples (differentiation), the spectrum is equalized; this process also serves as high-pass filtering of the signal, which effectively eliminates EDOs and relaxes the DR specification for the ADC. This, in turn, leads to the relaxation of the resolution requirement of the ADC. Figure 2.1 shows the process of spectrum equalization; as aforementioned, the original signal is first differentiated and then used as the input for a $\Delta\Sigma$ modulator. Hence, the output of the AFE is the derivative of the signal. Then, by integrating the signal in the digital domain, the original signal could be reconstructed while minimizing the DR of the ADC itself [27].

A critical design choice for neural AFEs is the method of input coupling. Many designs favor AC coupling [19], [20], [23], [25], [27], [31], where a coupling capacitor provides rail-to-rail electrode DC offset (EDO) rejection. To avoid low-frequency signal loss, the 3-dB corner of the resulting high-pass filter must be below 1 Hz, requiring capacitors in the order of 10 pF. The area penalty can be mitigated in processes with dense MIM capacitors, since capacitors can be stacked above active circuitry [27].

However, AC coupling introduces other challenges. First, setting the DC bias requires ultra-high-value resistors, typically implemented as pseudo-resistors. These elements suffer from strong non-linearity under large-signal artifacts (e.g., stimulation) [30], [32]. Alternatives such as duty-cycled resistors [8], [33] improve robustness, but their effectiveness is limited by parasitic capacitance, which limits the maximum achievable resistance while still requiring high-value AC-coupling capacitors. Second, AC coupling is incompatible with flicker-noise reduction by chopping, as for AC coupling, chopping results in noise multiplication and degradation of the input impedance [32].

An alternative to AC coupling is DC coupling, where no coupling capacitor is used and, instead, DSLs are used to eliminate the effect of EDOs. For example, $\Delta^2\Sigma$ modulation Designs utilizing DC coupling [21] [28] [20] [29] [30] show impressive power consumption specification. For instance, [28] reports less than $1\mu W$ per channel while utilizing DC-coupling. Additionally, DC coupling allows the use of chopping for flicker noise mitigation[20].

Recognizing the multitude of design choices associated with AFE design for neural signals, the remainder of this section will be dedicated to comparing state-of-the-art designs. This will be done with the goal of deriving state-of-the-art matching requirements for future design. Table 2.1 shows the aforementioned comparison. It should be noted that $\Delta^2\Sigma$ based designs show impressive Area/Ch specifications with [19] especially reporting impressive channel area. Moreover, this topology could offer sub-1 μW power consumption.

Table 2.1: Comparison of State-of-the-Art Direct Digitization AFEs for Neural Signal Acquisition

Metric	**[19]**	**[20]**	**[27]**	**[31]**	**[28]**	**[26]**	**[6]**	**[30]**
Application	AP+LFP	AP+LFP	AP+LFP	AP+LFP	Closed Loop Stimulation (LFP)	AP+LFP	Closed-Loop Neurostimulator	Closed-Loop Neurostimulator
Tech [nm]	22	55	180	110	130	40	130	130
Supply [V]	0.8	1.2	0.5/1.0	1	0.6/1.2/3.3	1.2	1.2/2.5	1.2
Area/Ch [mm^2]	0.0045	0.0077	0.058	0.078	0.011	0.113	0.013	0.023
AP Noise [µVrms] LFP Noise [µVrms]	7.71± 0.36 11.9±1.13	5.53 ±0.36 2.88± 0.18	3.32	9.5	2.6 (LFP)	6.35 1.8	1.13	1.13 (LFP)
Power per Channel [μW]	6.02	61.2	3.05	6.50	0.99	7.30	0.630	1.70
BW Low [Hz]	0.1	0.5	0.5	1	1	1	0.1	1
BW High [kHz]	10	10	10.9	10	0.5	5	0.5	0.5
BW [kHz]	10	10	10.9	10	0.499	5	0.4999	0.499
Power/BW [nW/Hz]	0.602	6.12	0.280	0.650	1.98	1.46	1.26	3.41
Zin [Ω]	Inf @ DC	663M@ 10Hz	inf @ DC	inf @ DC	2960M	1520M	0.99-1.02M	1456M
AC Input Range [mVpp]	43	148	-	300	-	200	-	-
EDO Tolerance [mVpp]	Rail-to-Rail	±70	Rail-to-Rail	±70	±1500	±100	Rail-to-Rail	±500
Topology	AC Coupled 1^{st} order $\Delta^2\Sigma$	DC Coupled 2^{snd} order $\Delta^2\Sigma$	IA+1^{st} order $\Delta^2\Sigma$	DC Coupled 2^{nd} order $\Delta\Sigma$	DC Coupled OpAmp-less Δ modulated	CCIA+$\Delta\Sigma$	AC coupled $\Delta-\Delta\Sigma$	Track and Zoom $\Delta\Sigma$

2.3. Conclusion

In conclusion, analog front ends (AFEs) for neural signal acquisition have evolved to address various trade-offs in power, area, and noise performance. The IA+ADC architecture, while popular for its simplicity and efficient power consumption, faces limitations in area. Direct digitization architectures, particularly those utilizing $\Delta\Sigma$ modulators, offer an alternative by eliminating the need for high-gain amplifiers, though they require ADCs with high dynamic range.

Recent advancements, such as the $\Delta^2\Sigma$ architecture, provide promising solutions by leveraging spectral equalization and noise shaping to manage the unique low-frequency spectrum of neural signals, ultimately relaxing ADC requirements and improving overall performance. Table 2.1 presented in this chapter provides a comparative analysis of state-of-the-art AFE designs, highlighting the different topologies developed to balance performance specifications for diverse neural recording applications.

3

Modeling

3.1. Introduction

This chapter presents the high-level design of an AFE for neural signal processing applications. The design aims to address the area and power consumption demands of AFEs while efficiently digitizing both LFPs and APs. Moreover, as previously mentioned in Chapter 2 of this work, AFEs designed for neural signal processing need to address a few key challenges, including: electrode-DC offset, wide input range, low noise requirements [19][27][20][8].

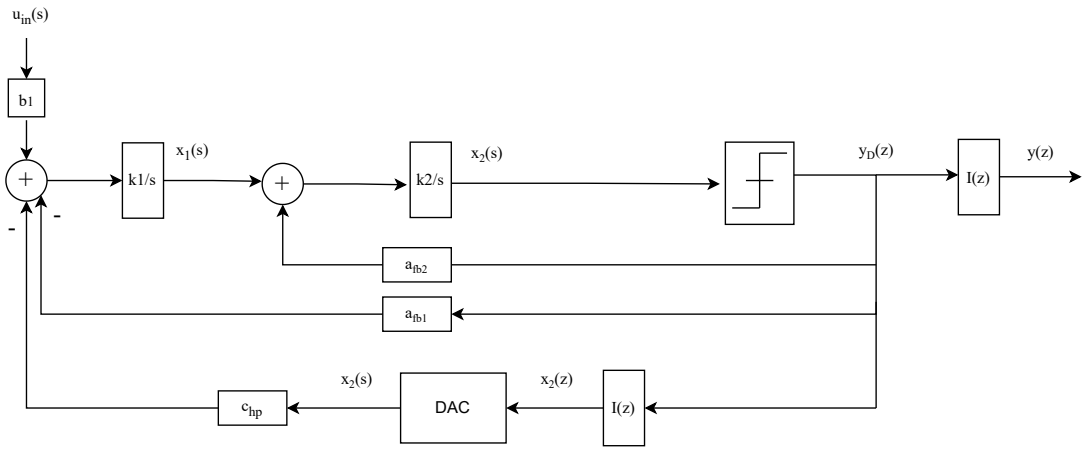
To address these challenges, this thesis chapter presents a high-level model of an AFE based on a Δ-ΔΣ topology. This design is based on approaches such as those proposed by [27], [3], and [19]. It was noted that the $\Delta - \Delta\Sigma$ topology has key similarities with the work of [10], which presents an orthonormal High-pass ΣΔ (HPΣΔ) front end for cardiac signal acquisition. This similarity is rooted in the shared introduction of an extra feedback loop with an integrator of the ΣΔ modulator, effectively setting a high-pass pole. This enables the design to specifically address crucial challenges like input DC offset (EDO) and unwanted low-frequency components, such as baseline wandering, which are prevalent in biopotential recordings across similar bandwidths (e.g., 0.5-200 Hz for ECG [10]). The key difference between the two approaches is that in the $\Delta - \Delta\Sigma$ proposed in [20], the core ΣΔ loop employs an observer-canonical structure (as shown in Figure 3.1a), while in [10] an orthonormal topology (as shown in figure 3.1b) was utilized. The orthonormal topology will be favored in this work, as previously mentioned in Chapter 2, [10] shows that the use of an orthonormal topology yields superior performance. Another key difference between the AFEs is the implementation of the state x_3 integrator. where [10] implements a low-frequency high-pass pole with a continuous time integrator, while the AFE reported in [20] introduces a frequency equalization loop utilizing a digital integrator, which requires conversion back to the continuous time domain.

This chapter is organized as follows. Section 3.2 discusses the architectural considerations and motivates a direct-digitization, DC-coupled topology for the AFE. Section 3.3 outlines the state-space approach for $\Delta - \Delta\Sigma$ ADC design, specifying the STF/NTF requirements and mapping them to an orthonormal ladder representation. Section 3.4 presents the modeling and simulation flow: a discrete-time MATLAB model, its validation, and an impulse-invariant transformation to an equivalent continuous-time Verilog-A implementation, followed by spectral comparisons. Section 3.5 concludes the chapter.

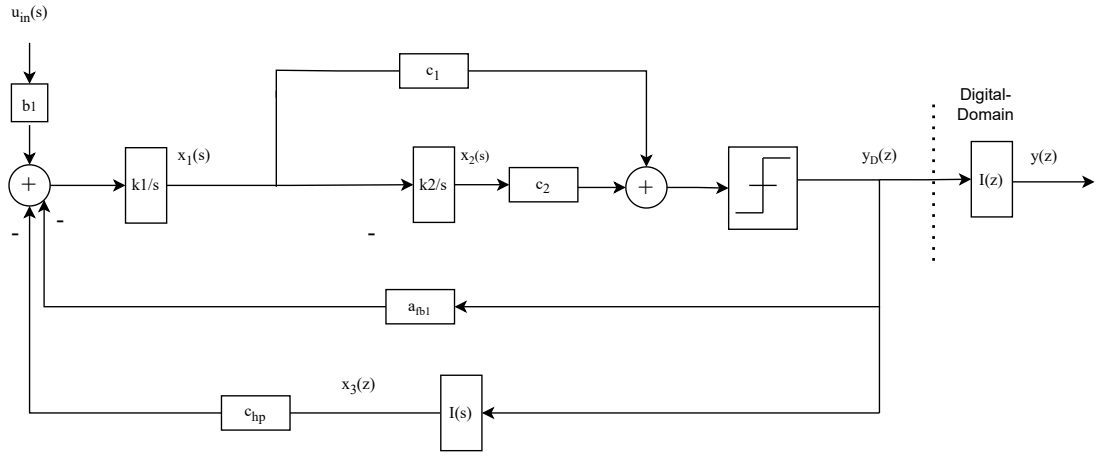
3.2. Architectural Considerations

The first design choice with regard to topology is the AFE architecture. As previously stated in Chapter 2, the two main architectures utilized in literature are IA+ADC and direct digitization. In this design, a direct-digitization topology will be favored, as these architectures are particularly advantageous for their ability to significantly reduce readout area [19].

The second design choice is the input coupling type. As stated in Chapter 2, there are two main design choices, which are, AC coupling and DC coupling. AC coupling presents several advantages.



(a)



(b)

Figure 3.1: Two state-space representations of the Δ-ΔΣ AFE:(a) observer-canonical representation [20]. $I(z) = \frac{1}{z-1}$ (b) orthonormal representation [10] with the addition of a reconstruction integrator in the digital domain;

One of the most important advantages is rail-to-rail EDO cancellation. This is typically achieved using a high-pass filter at the input stage, composed of capacitors and pseudo-resistors. By filtering out large DC components early in the chain, the circuit avoids saturating subsequent stages and allows the modulator to solely digitize the desired AC signal components [8], [19]. Another key advantage of AC coupling is the decoupling of circuit design from electrode performance. Because the input is capacitively coupled, the system can accommodate a variety of electrode types without imposing tight constraints on input impedance or biasing.

However, AC coupling comes with notable limitations. To set low-frequency cutoff points (e.g., sub-Hz for LFPs) using small on-chip capacitors (in the pF range), extremely high resistances (on the order of tera-ohms) are required. This is usually achieved with pseudo-resistors, which are compact but suffer from strong process variation, nonlinearity, and sensitivity to light and leakage currents [8].

However, DC coupling, when combined with DC-servo loops (DSLs), offers an alternative approach for handling EDO. Mixed-signal DSLs, in particular, offer the advantage of improved area efficiency by eliminating the requirement for large analog time constants [8], [19], [20]. Hence, by employing DSLs. The literature shows that area efficiency improvements could be achieved. Hence, a DC-coupled direct digitization topology will be favored in this design.

3.3. State-Space Approach for ΣΔ ADC Design

This section is primarily based on the structured design methodology presented in [11], where the state space approach separates the design process into three distinct phases: transfer function specification, topology selection, and circuit-level implementation. In the context of this work (as is also the case in [10]), the topology is predetermined to be an orthonormal ladder structure reflected in Figure 3.1b. This choice is motivated by the advantages discussed in the previous chapter and reported in [10]. The remainder of this chapter is therefore devoted to the transfer function design phase and its mapping onto the orthonormal ladder structure.

3.3.1. Transfer function design phase

The desired transfer function of the modulator must have the following characteristics for the signal transfer function (STF) and noise transfer function (NTF).

- For STF: inclusion of an extra pole which performs $\Delta - \Delta\Sigma$ spectrum equalization.
- For NTF: Noise transfer function (NTF): a high-pass filter characteristic with all real zeros at the origin, leading to a 40 dB/dec slope in the signal band (second order $\Delta\Sigma$ noise shaping).

In [10] it was shown that the orthonormal state space representation shown in Figure 3.1b satisfies these requirements. The STF and NTF of the said topology are expressed as

$$STF(s) = \frac{k_1\, b_1\, k_q\, c_1\, s^2 + k_1\, b_1\, k_q\, k_2\, c_2\, s}{s^3 + k_q\, k_1\, c_1\, a_{fb}\, s^2 + k_q\, k_1\big(k_2\, c_2\, a_{fb} + b_1\, k_3\, c_{hp}\, c_1\big)\, s + b_1\, k_q\, k_1\, k_2\, k_3\, c_2\, c_{hp}} \tag{3.1}$$

$$NTF(s) = \frac{s^3}{s^3 + k_q\, k_1\, c_1\, a_{fb}\, s^2 + k_q\, k_1\big(k_2\, c_2\, a_{fb} + b_1\, k_3\, c_{hp}\, c_1\big)\, s + b_1\, k_q\, k_1\, k_2\, k_3\, c_2\, c_{hp}}. \tag{3.2}$$

where k_q is the gain of the quantizer, and k_i is the gain of the integrator corresponding to the i^{th} state. Moreover, from the STF and for a low frequency approximation ($f << f_s$), the characteristic equation can be approximated as a first-order polynomial [10] where:

$$k_q k_1 [s(k_2 c_2 a_{fb}) + k_2 k_3 c_2 c_{hp}] = 0 \tag{3.3}$$

assuming $c_{hp} k_3$ is small, the high-pass pole can be approximated as equation 3.4.

$$s \approx \frac{-c_{hp} k_3}{a_{fb}}. \tag{3.4}$$

3.4. Modeling and Simulation

3.4.1. DT Modeling

The modeling of the modulator is carried out in two sequential phases. In the first phase, a DT model is developed to enable design space exploration in MATLAB. In the second phase, the validated DT model is converted into an equivalent CT representation and implemented in Verilog-A. The resulting Verilog-A model then serves as the starting point for the subsequent low-level hardware design and verification.

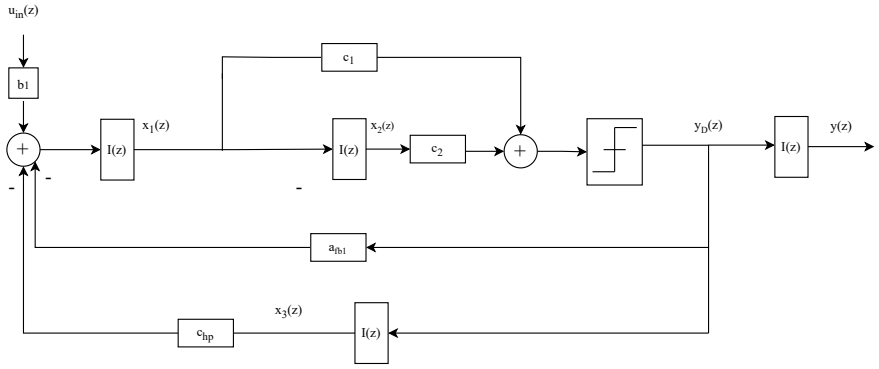


Figure 3.2: DT-AFE model used for Numerical simulations in MATLAB

From the block diagram of Fig. 3.1b the discrete-time state equations for $x_1(z)$, $x_2(z)$ and $x_3(z)$ read

$$x_3(z) = k_3 * y_d(z) + x_3(z-1), \tag{3.5}$$

$$x_1(z) = k_1\big[b_1\big(u_{in}(z)\big) - a_{\text{fb}}\, y_d(z) - c_{\text{hp}}\, x_3(z)\big] + x_1(z-1), \tag{3.6}$$

$$x_2(z) = k_2\, x_1(z) + x_2(z-1). \tag{3.7}$$

The summer and 1-bit quantizer generating the output $y_d(z)$ are described by

$$w(z) = c_1\, x_1(z) + c_2\, x_2(z), \tag{3.8}$$

$$y_d(z) = Q\big[w(z)\big] = \operatorname{sgn}\big[w(z)\big] = 2\,[\,w(z) \geq 0\,] - 1. \tag{3.9}$$

where $w(z)$ is the quantizer input while $y_d(z)$ is the quntizer output.

Equations (3.5)–(3.9) constitute the complete set of difference relations that model the orthonormal ΣΔ modulator of Fig. 3.1b. For small-signal analysis, the hard sign non-linearity in (3.9) is commonly replaced by an additive white quantization-noise source, i.e. $y(z) = w(z) + e_q(z)$ with $e_q(z)$ assumed uncorrelated with the state variables [34]. However, in behavioral transient time simulations, the exact form of (3.9) is retained to capture the modulator's large signal dynamics.

The loop constants were chosen such that the frequency-equalization loop pole defined in equation 3.4 is placed at $f_p = 15.9$ kHz, to ensure the full signal full signal bandwidth($10kHz$) is covered. This resulted in a value of $c_{hp} = 0.0098$ for $k3 = 1$, and $a_{fb} = 1$. The integrator gains, k_1 and k_2, and a_{fb}, were chosen to ensure modulator stability via transient time parametric sweeps over the DT model in MATLAB, while relying on state scaling (applied in later design steps) to further optimize their values.

Additionally, Figure 3.3 confirms the second transfer function design requirement outlined in Subsection 3.3.1, as it demonstrates a noise-shaping response with a slope of approximately $40\ \mathrm{dB/decade}$. To verify the first design requirement, Figure 3.4 presents the SQNR of the Δ–ΔΣ modulator before and after reconstruction. The figure clearly shows the presence of f^2 spectrum equalization, indicating that the shaping requirement in the low-frequency region has been satisfied.

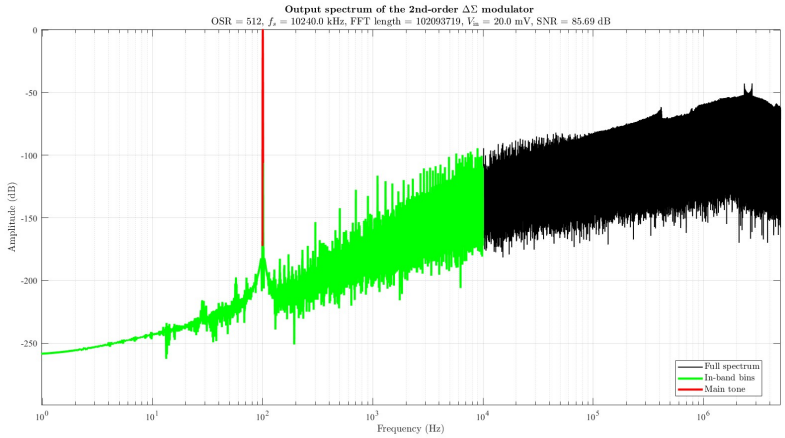


Figure 3.3: Normalized output spectrum of the second-order ΔΣ modulator with oversampling ratio $\mathrm{OSR} = 512$, sampling frequency $f_s = 10.24$ MHz, and FFT length $N = 102{,}000$. The input signal has amplitude $V_{\mathrm{in}} = 21.5$ mV and frequency $f_{\mathrm{in}} = 100.3$ Hz. The main tone and in-band noise bins are highlighted.

Table 3.1: Loop filter coefficients used in the discrete-time simulation model.

Parameter	Value
k_1	0.5
k_2	0.5
c_{hp}	0.0098
c_1	1
c_2	1
a_{fb}	1
b_1	1

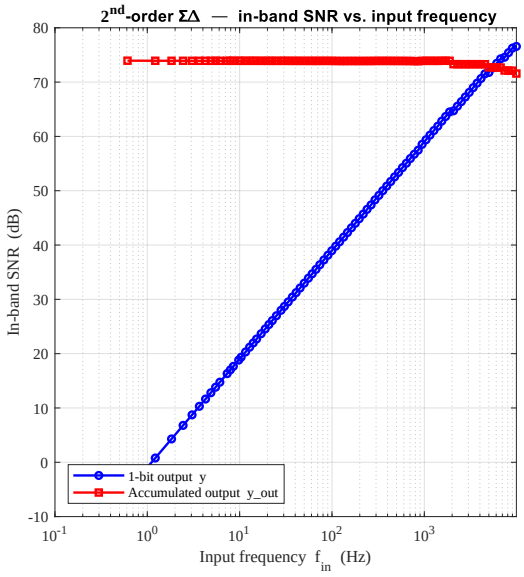


Figure 3.4: Coherent log–spaced SNR sweep of the orthonormal second-order Δ – ΔΣ modulator. Each tone ($0.1\ \mathrm{Hz} \le f_{\mathrm{in}} \le 9.93\ \mathrm{kHz}$) is simulated for $N_{\mathrm{FFT}} = 2^{24}$ samples and evaluated with a rectangular window.$f_s = 10.24\ \mathrm{MHz}$,and $\mathrm{OSR} = 512$. Signal power is taken from the ± 7 FFT bins around the coherent main-tone.The blue trace shows the in-band SNR of the raw 1-bit output $y[n]$, whereas the red trace corresponds to the reconstructed output $y_{\mathrm{out}}[n]$.

3.4.2. DT-to-CT Transformation

An additional step required to map the DT model to CT implementation involves applying the transformation proposed in [34]. As a first step, the continuous-time model is abstracted as shown in Fig-

ure 3.1b. To insure that both the DT model in Figure 3.2 and the CT implementation exhibit equivalent behavior, they must produce identical noise shaping and output bitstreams at the sampling instants [34].To insure this, [34] proposes an Impulse-Invariant Transformation (IIT), where the input to both the DT quantizer, $u_{in}(n)$, and the CT quantizer, $u_{in}(t)$, is the same at the sampling instants. This implies that the output bitstreams of both modulators, and therefore their noise performance, will be identical.

However, it should be noted that in the CT modulator, the digital-to-analog converter in the feedback loop acts as a discrete-to-continuous converter. Its input is a DT sample, $y(n)$, but its output is a continuous waveform, $y(t)$, whose shape depends on the DAC transfer function, $r_{DAC}(s)$. expressed mathematically, the condition for loop filter equivalence is expressed in the time domain as a convolution, where the impulse response of the DT loop filter $h(n)$ is equal to the sampled convolution of the DAC impulse response $r_{DAC}(t)$ and the CT loop filter $h(t)$: $h(n) = [r_{DAC}(\tau) * h(t-\tau)]|_{t=nT_S}$.
Assuming a Non-Return-to-Zero DAC, [34] proposes a set of partial transformations shown in Table 3.2. These transformations, when applied to the DT loop gain $L(z)$, yield a CT loop gain $L(s)$ that satisfies the condition for loop filter equivalence.

From the structure shown in Figure 3.1b, the loop gain expression in (3.10a) is derived. Given that for a DT system $I(z) \equiv \frac{z^{-1}}{1-z^{-1}}$, and using the substitutions provided in Table 3.2, the resulting CT loop gain $L(s)$ is expressed in (3.10b).

$$L(z) = -\left(a_{\mathrm{fb1}} + c_{\mathrm{hp}} \cdot I(z)\right) \cdot \left(c_1 k_1 I(z) + c_2 k_1 k_2 I(z)^2\right) \tag{3.10a}$$

$$L(s) = -\left(a_{\mathrm{fb1}} + c_{\mathrm{hp}} \cdot \frac{f_s}{s}\right) \cdot \left(\frac{f_s}{s}\left(c_1 k_1 + \frac{c_2 k_1 k_2}{2}\right) + \frac{f_s^2}{s^2} \cdot c_2 k_1 k_2\right) \tag{3.10b}$$

Table 3.2: Mapping between DT and CT transfer function elements [34].

Discrete-Time (DT)	Continuous-Time (CT) Equivalent
$\frac{1}{z-1}$	$\frac{f_s}{s}$
$\frac{1}{(z-1)^2}$	$\frac{\frac{1}{2}f_s s + f_s^2}{s^2}$

Similarly, the CT loop gain $L(s)$ was derived from Figure 3.1b and is shown in equation 3.11.

$$L(s) = -\left(a_{\mathrm{fb}} + I(s) \cdot c_{\mathrm{hp}}\right) \cdot \left(K_{C1\_s} \cdot I(s) + K_{C2\_s} \cdot I(s)^2\right) \tag{3.11}$$

Moreover, by substituting $I(s) = \frac{k_{s_i} f_s}{s}$ results in Equation 3.12.

$$L(s) = -(a_{\mathrm{fb}} + k_{s_3}\frac{f_s}{s} \cdot c_{\mathrm{hp}}) \cdot (k_{s_1} c_{1_s} \cdot \frac{f_s}{s} + k_{s_1} k_{s_2} c_{2_s} \cdot (\frac{f_s}{s})^2) \tag{3.12}$$

3.4.3. CT-Model

The CT Δ–ΔΣ modulator in Fig. 3.5 consists of two ideal $G_m - C$ integrators (G_{m1}, C_1) and (G_{m2}, C_2). where the transfer function $I(s)$ is defined as $I(s) = \frac{G_m}{SC}$ and k_i is set by the ratio between G_m and C. Hence, for the first integrator V_{x1} corresponding to the state $x1$ is defined as $V_{x1} = \frac{Gm_1 V_{in} - I_{fb}}{SC_1}$. while the second state variable is generated by the second integrator as $V_{x2} = \frac{Gm_2 V_{x1}}{SC_2}$. These states are summed according to Eq. (3.8) inside a 1-bit comparator that performs the quantization process. The feedback factor a_{fb1} is provided by current-mode DAC1, while DAC2 together with a current-mode integrator (CMI) realises the inner Δ path, and produces V_{x3}.

All CT constants follow the impulse-invariant rules of Section 3.4.2, so that the CT loop gain $L(s)$ matches the discrete-time prototype $L(z)$ at every sampling instant. The continuous-time modulator was implemented with behavioral Verilog-A blocks and simulated in Cadence Spectre. To validate the impulse-invariant design, its 1-bit output spectrum was compared with that of the discrete-time model. the two spectra are shown in Fig. 3.6. The two models demonstrate close alignment in mapping, exhibiting the expected behavior in terms of tone and noise-shaping order. However, the higher noise observed in the CT FFT remains unclear and may require further investigation to identify the underlying cause.

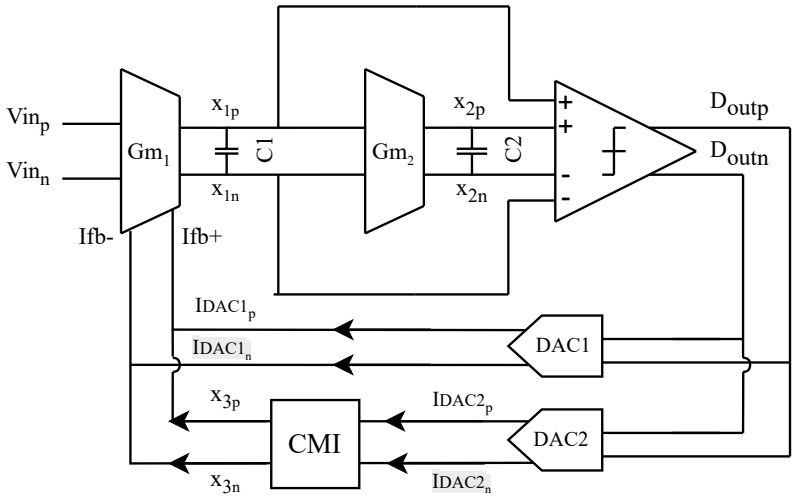


Figure 3.5: Behavioral CT Δ–ΔΣ modulator used in the simulations using the loop constants listed in Table 3.3.

3.5. Conclusion

This chapter presented the high-level design of a neural-signal analog front end based on a second-orderΔ–ΔΣ architecture. A direct-digitisation, DC-coupled topology was selected to meet the area, power, and offset requirements identified in earlier chapters.

A discrete-time orthonormal model was first derived and simulated in MATLAB. The results confirmed the required 40 dB per decade noise-shaping slope and the intended f^2 spectrum equalization across the entire neural band from 0.5hz to 10 kHz. Using impulse-invariant mapping, the discrete-time loop gain was translated into an equivalent continuous-time implementation.

The continuous-time modulator was realized in Verilog-A with ideal $Gm - C$ integrators, two current-mode DACs, a one-bit quantizer, and a current-mode integrator. The modulator was then simulated in Cadence Spectre. A Point-by-point FFT comparison showed agreement between the continuous-time and discrete-time spectra. These results validate the transfer function and topology design phases (as categorized in [11]) and provide a behavioral baseline for the next design phase, where ideal blocks will be replaced by transistor-level circuits while preserving verified loop dynamics.

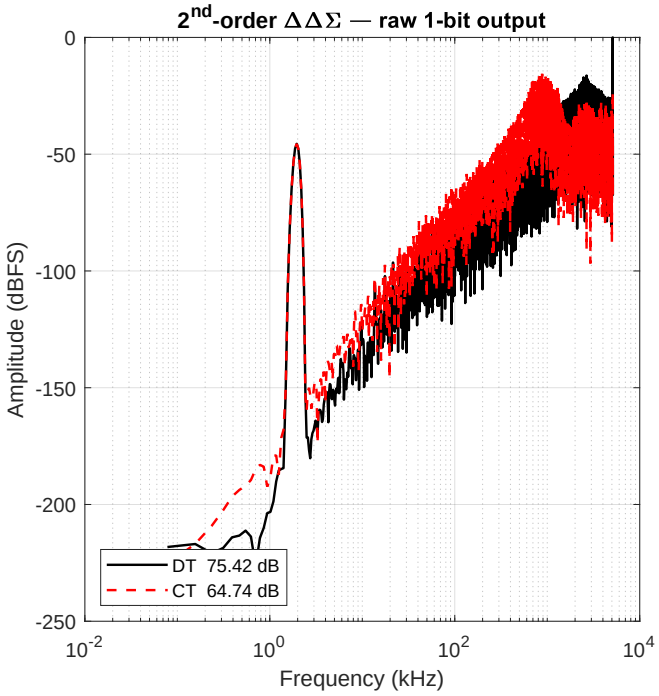


Figure 3.6: Raw 1-bit output spectra of the 2nd-order Δ–ΔΣ modulator. The discrete-time (solid black) and continuous-time (dashed red) models are analysed with a $N_{\mathrm{FFT}} = 131\,072$-point Kaiser window. Input tone: $f_{\mathrm{in}} = 1.953\,\mathrm{kHz}$, and the sampling frequency $f_{\mathrm{s}} = 10.24\,\mathrm{MHz}$ (OSR = 512).

Table 3.3: Simulation constants for the DT prototype and the CT Verilog-A model used in Fig. 3.6.

Global simulation settings	
Sampling frequency f_{s}	$10.24\,\mathrm{MHz}$
Signal bandwidth f_{b}	$10\,\mathrm{kHz}$
Oversampling ratio OSR	512
FFT length N_{FFT}	$131\,072$ (2^{17})
Discrete-time coefficients	
Feed-forward zero b_1	1
Integrator gains $k_1 = k_2$	0.5
Third integrator gain k_3	1
Summer weights $c_1 = c_2$	1
Global feedback a_{fb}	1
HP cancellation c_{hp}	0.01
Continuous-time parameters	
Capacitors $C_1 = C_2$	1 pF
Scaling C_{1s}	1.25
Scaling C_{2s}	1.00
Transconductances $G_{m1} = G_{m2}$	$0.5\,C_1 f_{\mathrm{s}}$

4

Circuit Design

4.1. Introduction

This chapter presents the third and final design phase of the AFE, where all functional blocks are implemented at the transistor level. The design procedure is based on pre-generated device lookup tables (LUTs) following the gm/ID design methodology [12].
The AFE employs gm–C integrators. In general, four types of integrators can be distinguished [11]:

(a) conductance–capacitance integrators,

(b) conductance–transcapacitance integrators,

(c) transconductance–capacitance (Gm–C) integrators, and

(d) transconductance–transcapacitance integrators.

Types (b) and (c) are commonly used in filter transfer function implementations. Type (a) cannot realize complex poles as it consists of two passive components, while type (d) requires two active components (a transconductance and a transcapacitance element). In this design, type (c) was chosen over type (b). The reason is that with type (c), parasitic capacitances appear in parallel with the signal path, allowing operation at higher frequencies, albeit with a reduced input dynamic range [11]. Furthermore, the feedback signal is processed in the current domain, which simplifies the implementation since current summation is more straightforward than voltage summation. Hence, current steering DACs will be utilized for the main feedback path and the Δ-path.

For the summer and quantizer, a multi-input strongARM latch [10] will be utilized as the StrongARM [35] latch combines low static power consumption, rail-to-rail outputs, and high sensitivity in a compact topology, However, its operation introduces kickback noise, and supply transients, while offset, kT/C noise, and metastability limit accuracy for small input signals. These trade-offs require careful sizing and often the addition of buffers or latches to ensure reliable system-level performance.

In recent Δ–ΔΣ AFEs reported in literature [19], [20], [36], the frequency equalization loop is often implemented in the digital domain using a digital counter, then converting the output back to the analog domain using a multibit DAC to generate the feedback quantity.In these implementations, the maximum input amplitude the loop can encode without saturation is set by the DAC full-scale. Following [20], the effective input full-scale is

$$V_{\mathrm{FS}} = 2^{N_{\mathrm{DAC}}}\, LSB_{in} \tag{4.1}$$

where N_{DAC} is the DAC resolution, LSB_{in} is the input-referred least significant bit defined as $\frac{I_{lsb2}}{Gm_1}$. This full-scale defines the numerator $P_{\mathrm{signal,max}}$ in the SQNR ratio,

$$\mathrm{SQNR} = 10\log_{10}\left(\frac{P_{\mathrm{signal,max}}}{P_{\mathrm{q,noise}}}\right), \tag{4.2}$$

Hence, for fixed loop order and OSR (which sets $P_{\mathrm{q,noise}}$), increasing V_{FS} raises the maximum achievable SQNR. However, larger LSB_{in} that boost V_{FS} also inflate the number of bits needed for the DAC. Consequently, requiring higher power consumption and area [20]. This work works around this trade-off by implementing the frequency equation loop using a dynamic translinear integrator.

This chapter is organized as follows. Section 4.2 presents the design of the two gm–C integrators based on the flipped-voltage-follower topology. Section 4.4 describes the implementation of the one-bit current-steering DAC cells. Section 4.5 covers the synthesis and design of the dynamic translinear integrator, including its fully differential extension. Finally, Section 4.6 details the design of the StrongARM comparator used as the quantizer.

4.2. First Gm–C integrator

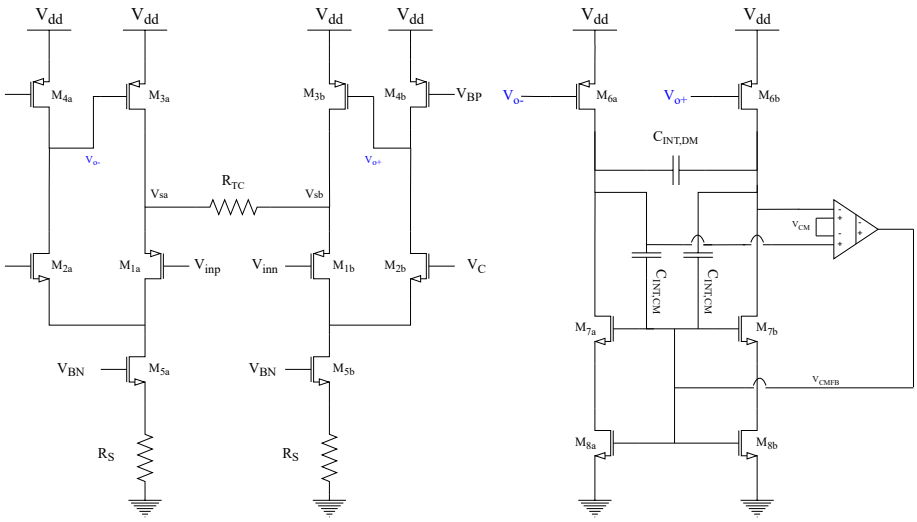


Figure 4.1: FVF based gm–C integrator presented in [19]

The first transconductance stage adopts the flipped-voltage-follower (FVF) [37] $G_m - C$ integrator reported in [19]. In Fig. 4.1, the input differential pair $M1$ senses the voltages V_{INP} and V_{INN}, while their sources are driven by the feedback transistor $M3$, which enforces the flipped-voltage follower action. The drain of transistor $M2$ drives the gate of $M3$ and acts as a cascode device, thus increasing the loop gain. The tail device $M5$ defines the bias current and is series-degenerated by R_s to suppress flicker noise. A small auxiliary bias current (about $I_{\mathrm{bias}}/10$) is provided by $M4$ for the second branch, while $M6$ steers the signal current into the integrating capacitor $C_{INT,DM}$.

The ideal transfer of the G_m stage from V_{IN} to $Vs_{a,b}$ is approximately $1/R_{TC}$. The loop gain of transistors M_{1-3} can be expressed as

$$LG \approx g_{m1} r_{o1}\, g_{m2} r_{o2}\, g_{m3} R_{TC}. \tag{4.3}$$

To first order, the open-loop ($\frac{V_{Sa,b}}{V_{IN}}$) gain is therefore

$$A_{OL} \approx g_{m1} r_{o1}\, g_{m2} r_{o2}\, g_{m3} R_{TC}, \tag{4.4}$$

and the closed-loop voltage gain approaches unity. From this, it follows that the output impedance at node Vs remains low due to the high loop gain, which leads to the voltage fluctuations at the drain of M_1 being small. Moreover, the effective transconductance of the stage can be approximated as

$$G_m \approx \frac{1}{R_{TC}}, \tag{4.5}$$

with a small error introduced by the finite output resistance of M_3.

The sensing resistor R_{TC} thus sees the exact differential input voltage, producing the signal current; the low output impedance allows for the subtraction of the feedback currents from the total current flowing through R_{TC}, where $V_{in}/R_{TC} - I_{fb}$. And the value was R_{TC} was chosen as $\frac{1}{R_{TC}} = G_m = k_1 * C_{INT,DM} * Fs$, where K is the integrator gain as in Table 3.3.
On the output side, unity current mirrors $M6 : M3$ steer I_{IN} into the integrating capacitor $C_{INT,DM}$. With finite output resistance $R_{out,Gm} \approx \frac{1}{gds_6} + \frac{1}{gds_{7,6}}$. and the transfer function is

$$\frac{V_o(s)}{V_{id}(s)} = \frac{G_m^{\text{eff}}}{C_{INT,DM}} \cdot \frac{1}{s + \frac{1}{R_{out,Gm} C_{INT,DM}}}. \tag{4.6}$$

while the finite $R_{\text{out,GM}}$ and capacitance at the output node introduce a secondary pole at

$$f_p = \frac{1}{2\pi R_{\text{out,GM}} C_{\text{out,tot}}} \tag{4.7}$$

A further non-dominant pole arises at the drain of $M4$ due to its parasitics, constraining stability.
From a noise perspective, flicker noise remains the dominant limitation [19], [20]. Tail degeneration (R_s in series with $M5$) suppresses flicker noise from the bias source but introduces additional thermal noise $4kT/R_s$. This leads to the following design trade-off: The tail path ($M5 + R_s$) balances flicker suppression against $4kT/R_s$; R_s must be chosen using gm/ID and noise targets rather than minimized arbitrarily.
At the device level, gm/ID analysis suggests:

- $M1$ should be biased in weak inversion, as its noise contribution directly adds to the input-referred noise.
- Current-source devices such as M_4, M_5, and $M_{3,6}$ were biased in moderate inversion. This choice was made to reduce their flicker-noise contribution, which requires relatively large device areas as flicker noise scales with device area. device LUTs showed that, for a fixed area WL, increasing the channel length L improves the output resistance r_0. However, to further suppress flicker noise, the minimum channel width was avoided for these devices, which required biasing these devices in moderate inversion, as it provided a balance between flicker noise reduction while maintaining sufficiently high r_0, whereas biasing deeper into weak inversion would have severely degraded r_0, and for strong inversion, the flicker noise would increase. .

The feedback currents I_{fb+} and I_{fb-} are injected into V_{Sa} and V_{Sb}, respectively. The peak feedback current sets the minimum bias current through $M5$ via $|I_{fb}| < I_{D_5} - I_{D_4}$.

Using the previously generated LUTs, the bias point of each transistor was set under the following constraints. The low-frequency pole is placed below $f_{\text{BW}}/\sqrt{3}$ as suggested in [19]. The unity-gain frequency is kept above 0.5 MHz. To account for the feedback currents, the minimum bias current of $M5$ was set to $I_{D5} = 0.5\,\mu$A. While the transconductance $Gm_1 = 0.5 \times C_1 F_s$ Is as in Chapter 3.

The dimensions that meet these conditions are reported in Table 4.1. The corresponding AC analysis is shown in Fig. 4.2, with $C_{INT,DM} = 200$ fF, giving $f_{pole} = 5.8$ kHz and $f_{UGF} = 500$ kHz.

4.3. Second Gm–C integrator

The second integrator reuses the same FVF G_m–C topology as in Section 4.2 (Fig. 4.1), with identical device roles and sizing. No architectural changes are introduced. The only difference is the tail bias current of $M5$, which is set to one quarter of the first integrator's bias to reduce static power:

$$I_{D5} = \frac{I_{D5,\text{GM–C1}}}{4} = \frac{0.5\,\mu\text{A}}{4} = 0.125\,\mu\text{A}.$$

All other parameters, including R_{TC} and $C_{INT,DM}$, are kept the same as in the first stage. Consequently, the small-signal relations for I_{IN}, the effective transconductance $G_m \approx 1/R_{TC}$, the transfer function, and

Table 4.1: First integrator sizing.

Device	Type	W [μm]	L [μm]	A_{gate} [μm^2]
M1	pch	100.000	1.800	180.0000
M3	pch	5.000	5.000	25.0000
M6	pch	5.000	5.000	25.0000
M7	nch	5.000	5.000	25.0000
M4	pch	5.000	5.000	25.0000
M5	nch	5.000	5.000	25.0000
M2	nch	0.220	0.180	0.0396
M8	nch	5.000	5.000	25.0000

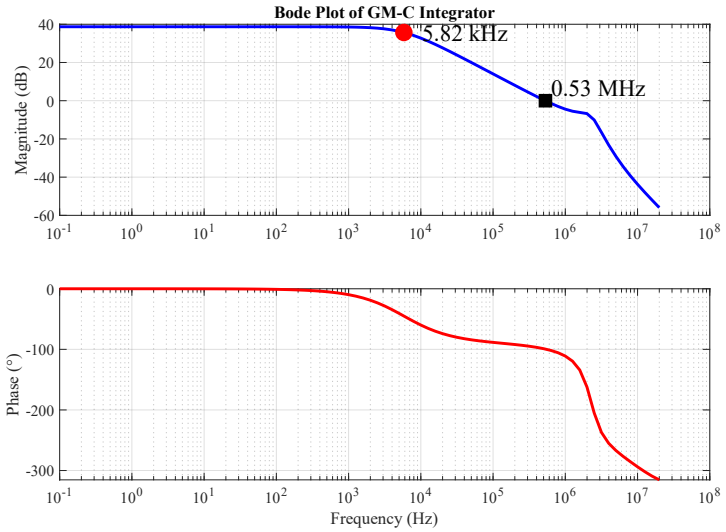


Figure 4.2: AC response of the first gm–C integrator (f_{pole} = 5.8 kHz, f_{UGF} = 0.5 MHz).

the unity-gain frequency

$$f_{UGF} \approx \frac{1}{2\pi R_{TC} C_{INT,DM}}$$

Given in Section 4.2 apply unchanged to this integrator as well.

4.4. DAC Cell

The AFE requires two one-bit current-domain DACs. The current-steering topology in Fig. 4.3 employs M_{tail} to set the unit current I_{lsb}, while M_0 and M_1 steer the current to the outputs. Cascode devices M_2 and M_3 are added to enhance the output impedance. The DAC cells were sized with a relatively long channel length of $L = 2$ μm while maintaining the minimum width to ensure strong inversion, thereby reducing noise and improving device matching.

Fig. 4.4 shows the simulated total current noise of a pMOS device as a function of channel length, obtained using precomputed gm/ID lookup tables. As expected, longer channel lengths significantly reduce device noise, justifying the chosen sizing strategy for the DAC cells in this design.

4.5. Dynamic trans-linear log-domain integrator

4.5.1. Trans-linear principles

As previously stated, the frequency equalization loop is implemented in the analog domain using a dynamic translinear integrator. To motivate this class of circuits, the static and dynamic translinear principles [38] are reviewed in the context of weak-inversion MOS devices.

Consider first the static translinear (STL) principle. In weak inversion, the drain current of a MOS

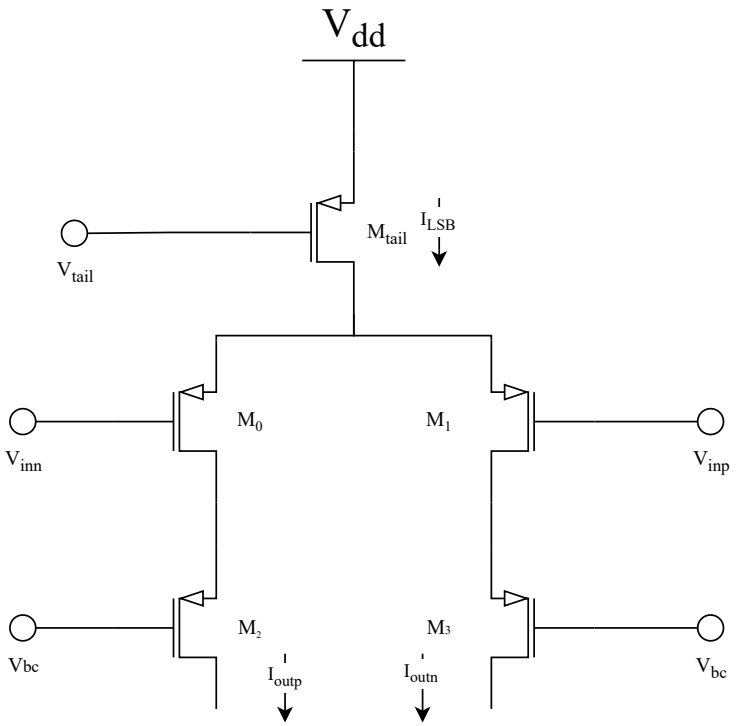


Figure 4.3: One-bit current-steering DAC cell. M_{tail} defines the unit current, M_0–M_1 act as switches, and M_2–M_3 provide cascoding.

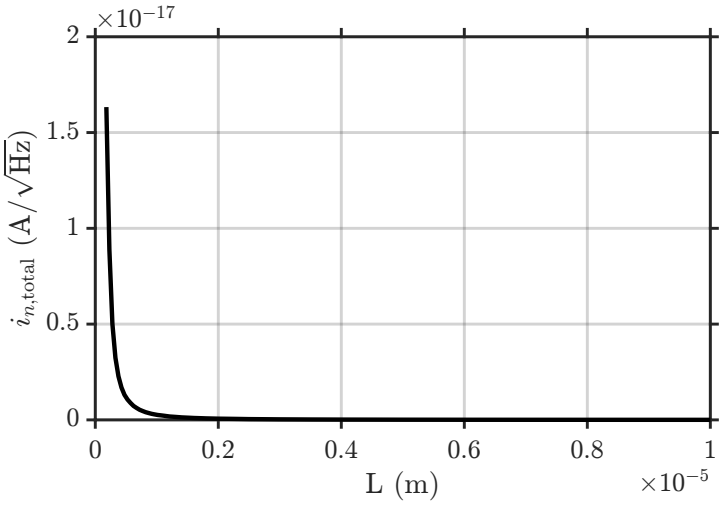


Figure 4.4: Total current noise of a pMOS device versus channel length, extracted from precomputed gm/ID lookup tables (TSMC 180 nm BCD) at a constant $\frac{gm}{ID}$

transistor is given by

$$i_D = I_0 \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right), \tag{4.8}$$

where n is the slope factor and V_T is the thermal voltage. In a closed four-transistor loop, shown in Fig. 4.5a, application of KVL around the loop yields

$$V_{GS1} + V_{GS3} = V_{GS2} + V_{GS4}. \tag{4.9}$$

Substituting (4.8) into (4.9) leads to the product-of-currents identity

$$I_1 I_3 = I_2 I_4. \tag{4.10}$$

This result illustrates the static translinear principle: the product of device currents in the clockwise direction is equal to that of devices in the counterclockwise direction. Such a relation enables direct implementation of algebraic functions, e.g., multiplication, division, and square rooting, in the current domain.

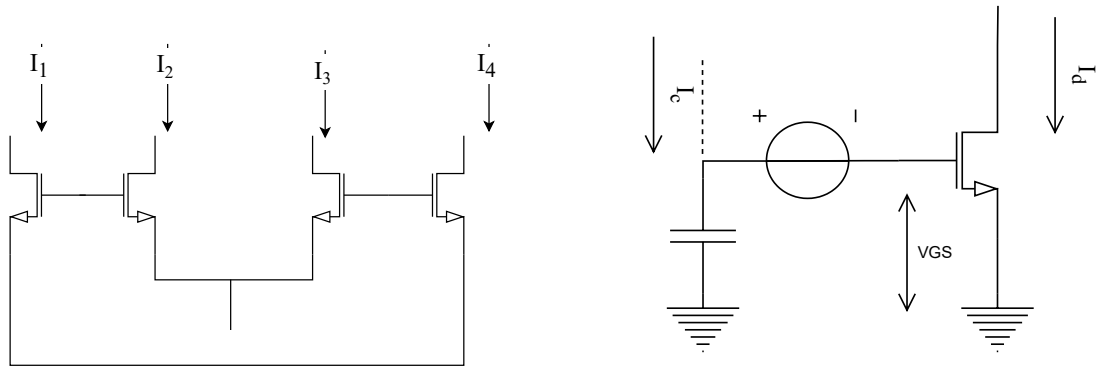
The dynamic translinear (DTL) principle extends this concept by including capacitors in the loop to add time dependence. The circuit shown in Fig. 4.5b demonstrates this principle, as in the current domain this circuit is described in terms of the drain current I_d and the capacitance current I_C. It should be noted that the DC-voltage source does not affect I_C. I_C could be derived from the derivative of the drain current as [38]:

$$I_c = CnV_T \frac{dI_d}{dt}. \tag{4.11}$$

Equation 4.11 shows that I_C is a non-linear function of I_d and its time derivative. A better understanding of equation 4.11 is obtained by rewriting it as equation 4.12.

$$I_d I_c = CnV_T \frac{dI_d}{dt}. \tag{4.12}$$

Equation (4.11) shows that time derivatives of currents are mapped into current products, which allows direct realization of differential equations in the current domain. This provides the basis for log-domain integrators and filters, as illustrated in Fig. 4.5b.



(a) (b)

Figure 4.5: Translinear principles in weak inversion: (a) static translinear loop for demonstrating the static transistor principle $I_1 I_3 = I_2 I_4$., (b) dynamic extension with a capacitor. A capacitor with voltage $v_c = nV_T \ln(i_d/I_0)$ produces current $i_c = C dv_c/dt$, leading to $i_d i_c = CnV_T\, di_d/dt$.

4.5.2. Dynamic translinear integrator synthesis

The synthesis of a dynamic translinear integrator follows a sequence of steps based on the STL and DTL principles [38], illustrated in Fig. 4.6.

The process begins with the dimensionless polynomial differential equation

$$\dot{y} = x, \tag{4.13}$$

where $\dot{y} = dy/d\tau$ is defined with respect to mathematical time τ. To relate this to real time, the derivative is scaled as

$$\frac{d}{d\tau} = \frac{CV_T}{I_0}\frac{d}{dt}, \tag{4.14}$$

and the variables are expressed in terms of normalized currents,

$$x = \frac{I_{in}}{I_0}, \qquad y = \frac{I_{out}}{I_0}. \tag{4.15}$$

Substitution into (4.13) gives

$$\dot{I}_{out}\frac{CV_T}{I_0^2} = \frac{I_{in}}{I_0} \quad \Rightarrow \quad \dot{I}_{out} = I_{in}\frac{I_0}{CV_T}. \tag{4.16}$$

In order to express this relation in a form suitable for current-mode implementation, the capacitor current is introduced as

$$I_{cap} = CV_T\frac{\dot{I}_{out}}{I_{out} + I_0}, \tag{4.17}$$

where I_0 is added to the output current to ensure that the capacitor current is unipolar. This leads to

$$(I_{out} + I_0)I_{cap} = I_{in}I_0. \tag{4.18}$$

Defining $I'_{out} = I_{out} + I_0$, the required behavior can then be realized with two translinear loops. The static loop implements

$$I'_{out}I_{cap} = I_{in}I_0, \tag{4.19}$$

while the dynamic loop provides

$$I'_{out}I_c = CV_T\frac{dI'_{out}}{dt}. \tag{4.20}$$

Finally, the equations in (4.19) and (4.20) can be mapped directly into the log-domain prototype circuit of Fig. 4.7, completing the synthesis procedure summarized in Fig. 4.6.

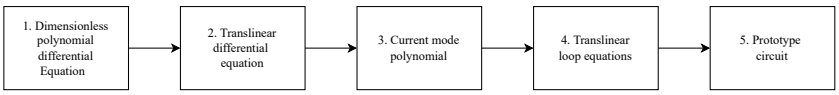


Figure 4.6: Synthesis procedure of a dynamic translinear integrator: (1) dimensionless equation, (2) translinear differential equation, (3) current-mode polynomial, (4) translinear loop equations, and (5) prototype circuit.

For use in the AFE the integrator must operate in fully differential manner. This is achieved by employing two copies of the prototype integrator, providing the positive and negative signal paths, together with a current-mode common-mode feedback (CMFB) circuit to regulate the output common-mode level. This is shown in Fig. 4.8.

4.6. Comparator

The StrongARM comparator [35] shown in Figure 4.9 is composed of two main parts: the pre-amplifier made up of the split differential pair M_{1-4} and the cross-coupled devices M_{5-8}, while devices M_{9-12} act as reset switches for all internal nodes. The circuit operation can be divided into a pre-charge phase (CLK = 0) and an amplification phase (CLK = VDD) [39]. During the pre-charge phase, the reset switches pull all internal nodes to VDD, thus eliminating any stored capacitor voltages and consequently suppressing dynamic offsets. In addition, the pre-charge switches keep the cross-coupled devices initially off, which reduces their offset contribution. When the clock rises and the circuit enters the amplification phase, the tail transistor M_{tail} turns on, establishing a discharge path for the capacitances at the drains of the input devices. In this split-input configuration, transistors M_1/M_3 and M_2/M_4 form two parallel input branches, and the discharge currents through each branch are modulated by

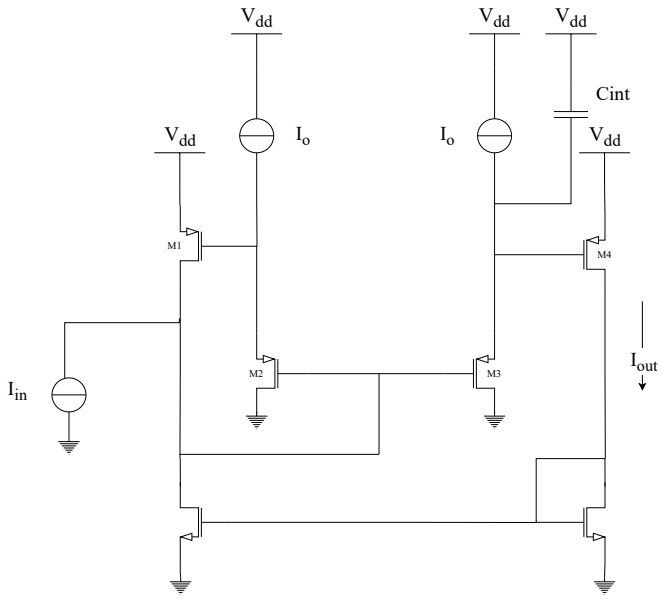


Figure 4.7: Prototype dynamic translinear integrator circuit.

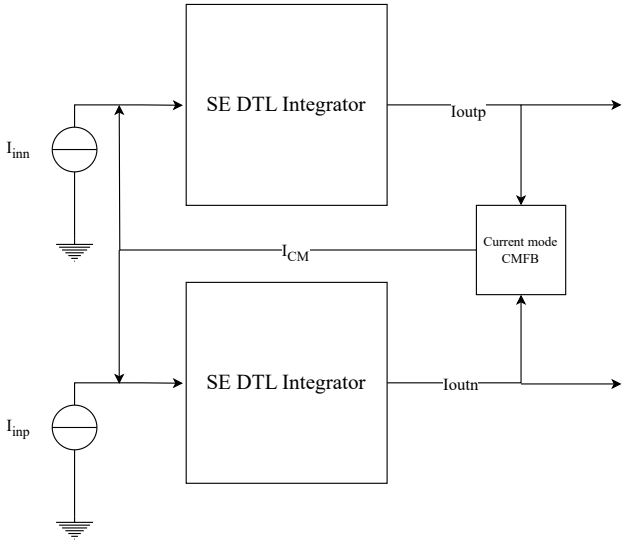


Figure 4.8: Fully differential dynamic translinear integrator with current-mode CMFB.

the applied differential input voltages V_{in1} and V_{in2}. Even a small difference between the inputs results in unequal discharge rates at the internal nodes, causing their voltages to diverge. As these voltages fall toward $V_{DD} - V_{THN}$, the cross-coupled NMOS pair (M_6 and M_8) begins to turn on, providing positive feedback and further amplifying the voltage difference. This regeneration continues until one side is pulled strongly low, while the opposite side is reinforced toward VDD. Finally, the PMOS pair (M_5 and M_7) restores the high output level, ensuring rail-to-rail logic levels at the outputs.

The main practical limitation of this topology is the kickback noise that arises at the input nodes due to rapid switching of internal nodes [39]. A common mitigation technique is to boost the width of the tail current transistor, which reduces the relative impact of kickback at the expense of higher power consumption.

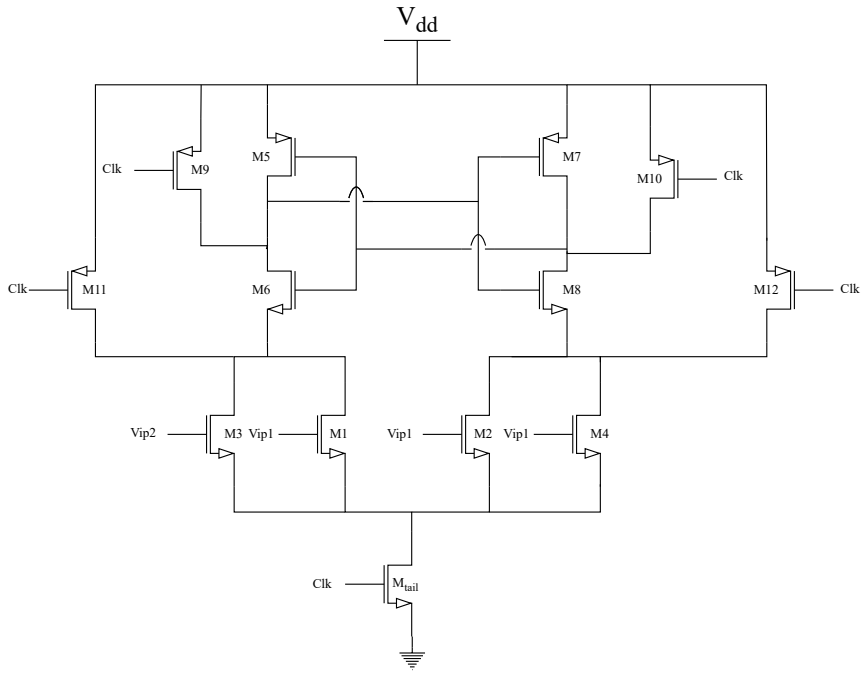


Figure 4.9: Two input dynamic StrongARM comparator

4.7. Conclusion

This chapter has detailed the transistor-level design of the AFE functional blocks using the gm/ID methodology and precomputed LUTs for the TSMC 180 nm BCD process. Two gm–C integrators based on the flipped-voltage-follower topology were implemented, with the first stage dimensioned to accommodate feedback current swings and the second optimized for low-power operation. The one-bit current-steering DACs were designed with cascoded devices to suppress INL errors, while device noise considerations led to the adoption of long-channel devices for the current source.

To realize the frequency equalization loop, a dynamic translinear log-domain integrator was synthesized and extended to a fully differential implementation with current-mode CMFB for compatibility with the AFE architecture. Finally, a StrongARM comparator was selected as the quantizer due to its low static power and high sensitivity, despite kickback noise trade-offs.

Together, these design choices ensure that the AFE achieves its required bandwidth, noise, and linearity specifications while maintaining compact area and low power consumption. The next chapter will tackle optimization and evaluate the performance of the complete system

5

Results

5.1. Introduction

This chapter presents the simulation results and performance evaluation of the proposed orthonormal $\Delta-\Delta\Sigma$ AFE. The aim is to demonstrate how architectural choices such as state scaling, and the use of a DTL integrator contribute to improvements in power efficiency, dynamic range, and noise performance compared to state-of-the-art designs.

First, the effect of state scaling optimization on the internal integrator states is examined, showing its role in maximizing the dynamic range without affecting the signal transfer. Next, the loop constants derived from post-scaling are summarized. Finally, detailed transistor-level simulation results are presented, including area, power, input-referred noise, and spectral performance, followed by a benchmark comparison against other direct digitization AFEs reported in the literature.

5.2. State scaling optimization

State scaling was applied to the orthonormal $\Sigma\Delta$ modulator to maximize its dynamic range. In this context, state scaling refers to adjusting the output amplitude of the internal integrator states such that they fully utilize the available output range M without clipping [10], [11], By scaling the dominant integrator outputs x_1 and x_2, the effective output swing is increased. This directly improves SNDR, as the useful signal power is maximized relative to the noise floor. The third state x_3 is multiplied by a small constant and therefore has a negligible effect on the dynamic range. In the implemented design, this scaling strategy resulted in a peak SNDR of $70\,\mathrm{dB}$, compared to $52\,\mathrm{dB}$ before state scaling.

Recalling the topology shown in Figure 3.5, the following loop constants were used after state scaling of x_1 and x_2. It should be noted that C_{1s} and C_{2s} represent the internal scaling factors of the quantizer (Figure 4.9) corresponding to states x_1 and x_2, respectively, while C_{int3} denotes the integration capacitor DTL integrator shown in Figure 4.7.

Table 5.1: Loop Constants After State Scaling

Symbol	Description	Value
C_{1s}	scaling factor for state x_1	0.9851
C_{2s}	scaling factor for state x_2	0.3292
$C_1 = C_2$	Integration capacitors	200 fF
C_{int3}	Third integrator capacitor	500 fF
I_{LSB2}	LSB current of DAC2	50 nA
I_{LSB1}	LSB current of DAC1	0.3072 µA
G_{m1}	Transconductance (First integrator)	1.949 µS
G_{m2}	Transconductance (Second integrator)	0.8 µS

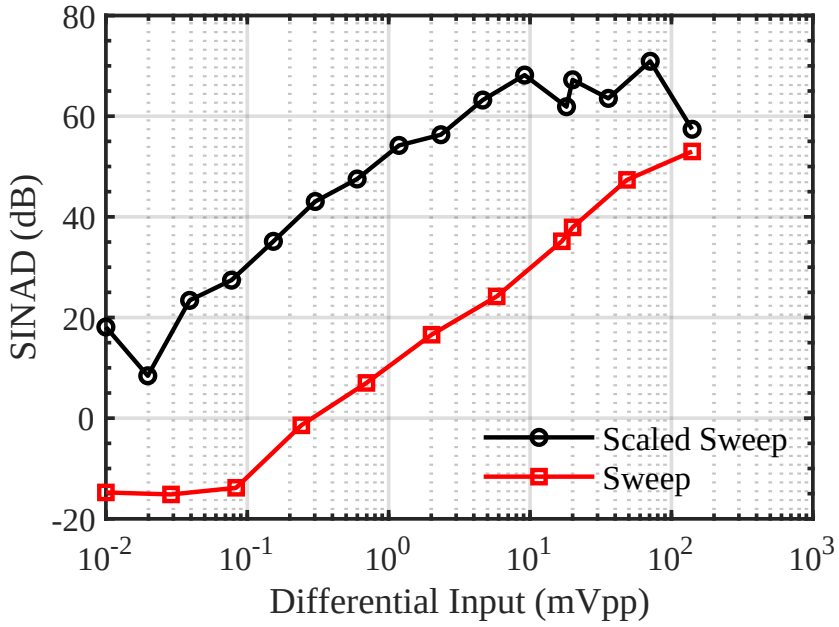


Figure 5.1: Measured SINAD versus differential input amplitude for the orthonormal ΣΔ modulator, over an input dynamic range from 10μV to 140, mV. The state-scaled design achieves the full input range, whereas the non–state-scaled design falls short, with the minimum recoverable input for SINAD > 0 dB occurring at approximately 0.3mV.

5.3. Results

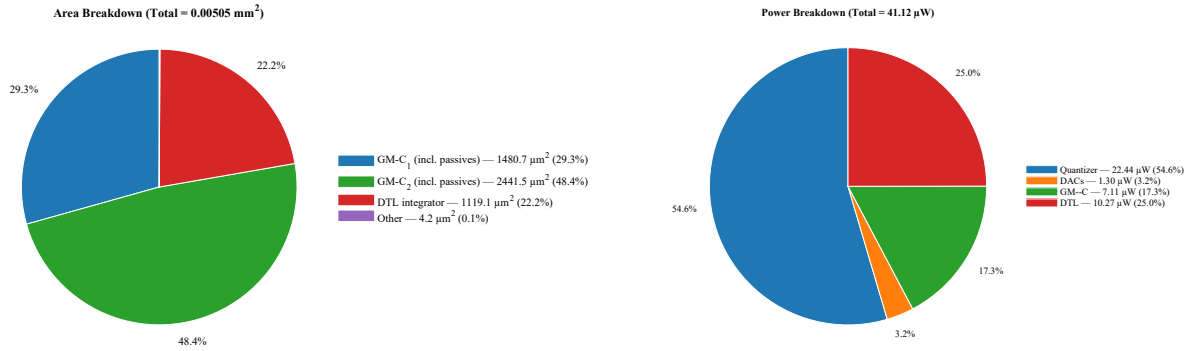
All results in this section are obtained from transistor-level simulations in a TSMC 180 nm BCD process. The channel area is $0.005\,05\,\mathrm{mm}^2$, with the distribution shown in Fig. 5.2a. The two GM-C integrators (including their associated passives) dominate the silicon cost, while the Quantizer, DACs, and comparator contribute a small fraction.

At $1.8\,\mathrm{V}$ supply, the simulated total power is $41.12\,\mu\mathrm{W}$, broken down as $22.44\,\mu\mathrm{W}$ (Quantizer), $1.30\,\mu\mathrm{W}$ (DACs), $7.11\,\mu\mathrm{W}$ (GM–C), and $10.27\,\mu\mathrm{W}$ (DTL), as summarized in Fig. 5.2b. The power consumption is dominated by the quantizer (54.6% of the total) this is due the strongARM topology being more susceptible to higher dynamic power consumption due to the charging and discharging of parasitic capacitance. However,the optimization of the quantizer design was left as an avenue for future work.

Fig.5.3 shows the power spectral density (PSD) for both the output bit stream post-quantization. The input referred noise spectrum was calculated as follows: First, the output was reconstructed using an ideal digital integrator. Then, the digital integrator output was referred to the input. The input referred noise in the AP band (300–10 kHz) and in the LFP band (0.5–1 kHz) was calculated as, $3.45V$ in the AP band (300–10 kHz) and $14.08V$ in the LFP band (0.5–1 kHz). Additionally, for a $20\,\mathrm{mV_{pp}}$ differential input, the modulator achieves a peak SNDR of $69.8\,\mathrm{dB}$ (ENOB = 11.3), and total harmonic distortion $= 0.001428\%@20mV_{pk-pk}, f_{in} = 122Hz$.

The noise analysis performed shows that flicker noise is the main noise contribution. Moreover, the EDO tolerance range was tested by a small sinusoidal input with the worst case amplitude of $20mV_{pp}$, while sweeping the DC-offset [20], and it was found to be $\pm 1.23\,\mathrm{V}$, while the input impedance is infinite at DC.

The comparison in Table 5.2 highlights several trade-offs between this work and prior state-of-the-art AFEs. Although the reported channel area of $0.005\,05\,\mathrm{mm}^2$ is an estimate derived from device area rather than a finalized layout, it is still competitive, with designs utilizing first-order noise shaping (i.e, [19]) presenting lower area AFEs. While, the utilization of the orthonormal topology and state-scale



(a) (b)

Figure 5.2: (a) Simulated power breakdown at $V_{\mathrm{DD}} = 1.8\,\mathrm{V}$. Total power = $41.12\,\mu\mathrm{W}$. (b) Estimated area breakdown of the proposed AFE. Total area = $0.005\,05\,\mathrm{mm}^2$.

optimization lead to a lower power consumption for the analog integrators ($7.11\mu W$) than what was reported in [20] ($17\mu W$) In terms of noise, the proposed AFE achieves an LFP noise of $14.08\,\mu\mathrm{V}_{\mathrm{rms}}$, which is in line with the first order AC coupled $\Delta - \Delta\Sigma$ reported in [19], where degradation resistors were used to mitigate flicker noise, similar to the approach adopted in this work. However, it remains higher than the $2.88\,\mu\mathrm{V}_{\mathrm{rms}}$ reported by [20], which benefits from chopping. The absence of chopping in this design avoids the associated penalty of reduced effective input impedance and EDO tolerance. As a result, this work demonstrates both high input impedance (infinite at DC) and a wide EDO tolerance of $\pm 1.23\,\mathrm{V}$. While the EDO range is not rail-to-rail, this is a direct consequence of avoiding an input high-pass filter. Importantly, not employing such a filter eliminates the need for pseudo-resistors, which often suffer from leakage currents and nonlinearity, thereby improving system linearity while also eliminating the need for large-value high-pass capacitors (such as the capacitors used in [19]).

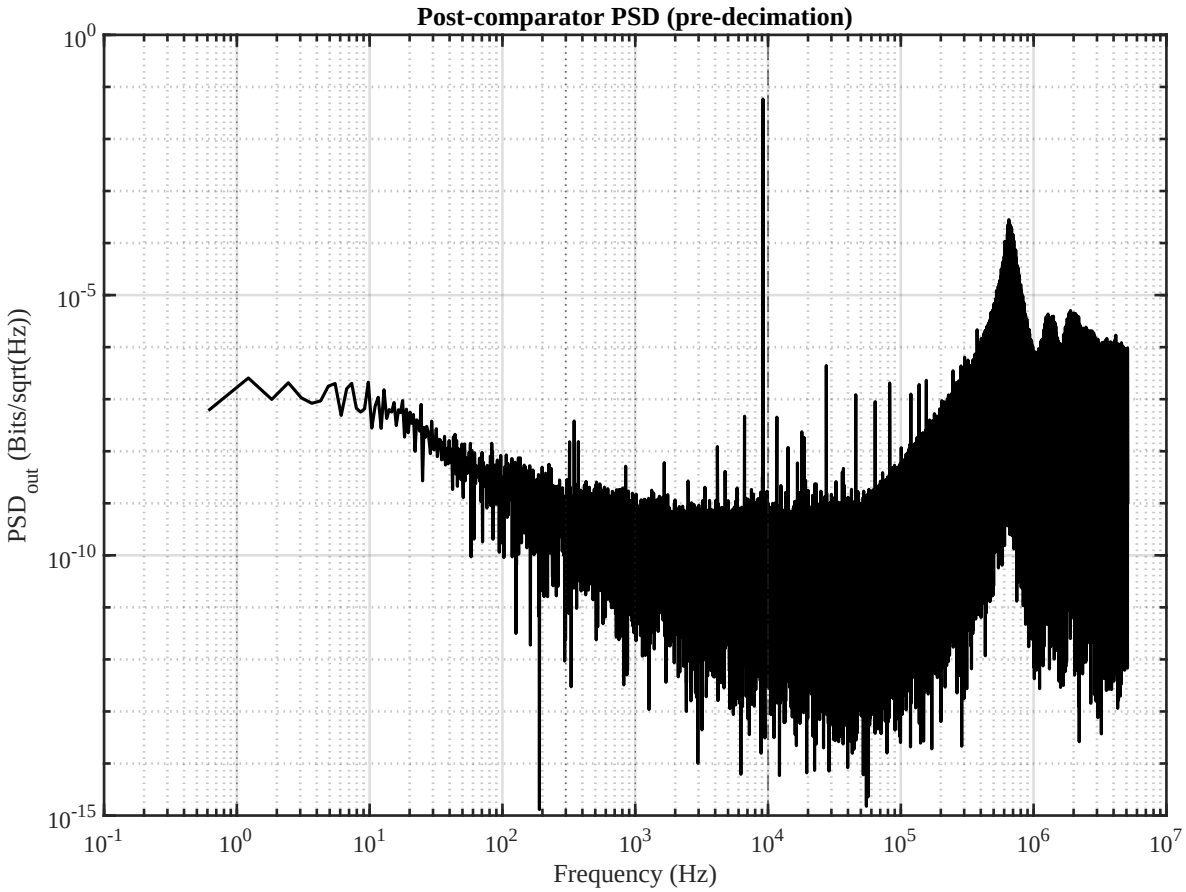


Figure 5.3: Post-quantization (output) PSD in $\mathrm{bit}/\sqrt{\mathrm{Hz}}$. Results shown for a coherent tone at $f_{\mathrm{in}} = 9155.273438\ \mathrm{Hz}$ with input amplitude $V_{\mathrm{pk}} = 20\ \mathrm{mV}$.

Table 5.2: Comparison of State-of-the-Art Direct Digitization AFEs for Neural Signal Acquisition

Metric	**[19]**	**[20]**	**[27]**	**[31]**	**[28]**	**[6]**	**This Work**
Application	AP+LFP	AP+LFP	AP+LFP	AP+LFP	Closed Loop Stimulation (LFP)	Closed-Loop Neurostimulator	AP+LFP
Tech [nm]	22	55	180	110	130	130	180
Supply [V]	0.8	1.2	0.5/1.0	1	0.6/1.2/3.3	1.2/2.5	1.8
Area/Ch [mm^2]	0.0045	0.0077	0.058	0.078	0.011	0.013	0.00505 (estimate)
AP Noise [µVrms] LFP Noise [µVrms]	7.71 11.9	5.53 2.88	3.32	9.5	2.6 (LFP)	1.13	3.45 14.08
Power per Channel [μ W]	6.02	61.2	3.05	6.50	0.99	0.630	41.12
BW Low [Hz]	0.1	0.5	0.5	1	1	0.1	0.5
BW High [kHz]	10	10	10.9	10	0.5	0.5	10
BW [kHz]	10	10	10.9	10	0.499	0.499	10
Power/BW [nW/Hz]	0.602	6.12	0.280	0.650	1.98	1.26	4.12
Zin [Ω]	Inf @ DC	663M@ 10Hz	inf @ DC	inf @ DC	2960M	0.99-1.02M	inf @ DC
AC Input Range [mVpp]	43	148	-	300	-	-	140
EDO Tolerance [mVpp]	Rail-to-Rail	±70	Rail-to-Rail	±70	Rail-to-Rail	Rail-to-Rail	±1230
Topology	AC Coupled 1st order $\Delta^2\Sigma$	DC Coupled 2nd order $\Delta^2\Sigma$	IA+1st order $\Delta^2\Sigma$	DC Coupled 2nd order $\Delta\Sigma$	DC Coupled OpAmp-less Δ modulated	$\Delta^2\Sigma$	$\Delta^2\Sigma$

5.4. Conclusion

This chapter has demonstrated the effectiveness of systematic design approaches in developing a spectrum-shaping $\Delta^2\Sigma$ AFE for neural signal acquisition. State scaling optimization successfully expanded the dynamic range, improving the peak SNDR from $52\,\mathrm{dB}$ to $70\,\mathrm{dB}$, and enabling robust recording across both AP and LFP bands. Transistor-level simulations in a TSMC 180,nm BCD process confirmed the feasibility of the proposed design, achieving a total estimated area of only $0.005\,05\,\mathrm{mm}^2$, low analog power consumption of $7.11\,\mu\mathrm{W}$, and noise performance of $3.45\,\mu\mathrm{V_{rms}}$ (AP) and $14.08\,\mu\mathrm{V_{rms}}$ (LFP).

A benchmark comparison against recent AFE designs highlighted the design's advantages in area efficiency, input impedance, and extended EDO tolerance, while also revealing trade-offs in LFP noise performance compared to chopping-based implementations. Crucially, the avoidance of input HPFs and pseudo-resistors eliminates leakage and non-linearity issues, ensuring long-term signal stability.

Overall, the results validate the central research question: systematic methodologies—including state-space representation at the transfer function level, orthonormal topology, DTL integrator synthesis, and G_m/ID-based transistor design—can be effectively combined to realize a power-efficient, spectrum-shaping AFE suitable for neural signal acquisition.

6

Conclusion

6.1. Conclusion

The proposed orthonormal-ladder Δ–ΔΣ AFE demonstrates promising performance, particularly in terms of power efficiency, when compared to similar state-of-the-art designs. For example, while the analog integrators in the second-order DC-coupled Δ–ΔΣ AFE reported in [20] consume 17 μW, the integrators in this work require only 7.11 μW. The total power consumption is 41.1 μW, dominated by the quantizer, yet the design maintains comparable noise performance. A key enabler is the use of a dynamic translinear integrator to implement the frequency-equalization Δ loop, which eliminates the need for complex digital circuits employed in prior works and thereby reduces both area and power consumption. In addition, state-scaling techniques expand the available dynamic range, enabling robust acquisition of low-amplitude, low-frequency LFP signals alongside higher-frequency AP signals. The design was developed using systematic methodologies at multiple abstraction levels: the state-space approach at the transfer-function level, dynamic translinear synthesis and the g_m/I_D methodology at the circuit level, and an orthonormal-ladder representation at the topology level. In doing so, this thesis directly addresses its central research question: how systematic design approaches can be applied to realize a spectrum-shaping analog front end for neural signal acquisition.

6.2. Contributions

This work contributes to the design of spectrum-shaping analog front ends for neural signal acquisition by applying a systematic methodology that divides the design process into transfer function design, topology selection, and circuit-level implementation. Within this framework, the following contributions were made:

- At the topology selection stage, the orthonormal ladder topology was adopted for the Δ–ΔΣ AFE. This choice ensured intrinsic state scaling, leading to optimal use of dynamic range and robust operation across both low-amplitude LFPs and higher-frequency APs.
- At the circuit level, the frequency equalization loop was realized in the analog domain using a dynamic translinear integrator. By synthesizing this block systematically, the design eliminated the need for a conventional multi-bit DAC in the feedback path, avoiding the overhead of large digital decoders and DWA circuits. This led to improvements in both power and area efficiency.

This work demonstrates how systematic approaches can translate high-level performance requirements into practical architectures and transistor-level implementations for neural AFEs.

6.3. Recommendations

Future work recommendations include carrying out the physical layout and post-layout extraction to obtain more accurate performance estimates, as well as implementing a decimation filter to complete the

system-level design. Porting the architecture to a down-scaled technology node could further reduce power consumption and area. In addition, optimization of the quantizer implementation is needed to improve energy efficiency. Another point for future improvement is the correction of the conversion error identified between the DT and CT models. Finally, while the loop constants for the DT model in this work were based on an initial design point to insure stablity, further optimization of these parameters could enhance overall modulator performance.

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