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An Analytical Turn-on Power Loss Model for 650-V GaN eHEMTs

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***Abstract*— This paper proposes an improved analytical turn-on power loss model for 650-V GaN eHEMTs. The static characteristics, i.e., the parasitic capacitances and transconductance, are firstly modeled. Then the turn-on process is divided into multiple stages and analyzed in detail; as results, the time-domain solutions to the drain-source voltage and drain current are obtained. Finally, double-pulse tests are conducted to verify the proposed power loss model. This analytical model enables an accurate and fast switching behavior characterization and power loss prediction.**

***Keywords*— GaN eHEMTs; turn-on; power loss model**

I. INTRODUCTION

Gallium nitride (GaN) power transistors, e.g., eHEMTs, are attracting increasing research interests due to their capability of high-performance power conversion, i.e., higher switching frequency, higher efficiency and higher power density than their silicon counterparts [1]-[2]. The parasitic capacitances of GaN transistors, i.e., the input capacitance C_{iss}, reverse capacitance C_{rss} and output capacitance C_{oss}, are much (3-10 times) smaller than Si devices with the same voltage rating and on-state resistance. Therefore, the switching speed is fast (e.g., ≈ 10 ns) and the switching energy loss can be low (e.g., tens of micro-joules for 650-V GaN eHEMTs) [3]-[4]. Nevertheless, the switching power loss can still be high when the switching frequency is increased to above hundreds of kilohertz or even megahertz. Hence, fast and accurate switching loss calculation is still important for circuit designers to predict power conversion efficiency and also the junction temperature.

For GaN transistors, the parasitic gate-source and gate-drain capacitances are small and the output capacitance C_{oss} still shows high nonlinearity, i.e., C_{oss} decreases when drain-source voltage increases. Thus, during the turn-off transition, it is potentially more possible to fast discharge the gate capacitances and cut off the channel before the drain-source voltage starts to rise. As a result, the turn-off energy loss is almost equal to the energy stored in the output capacitance, i.e., E_{oss} [3]-[6]. Then the main challenge for switching loss calculation of GaN transistors lies in the turn-on switching characterization.

The most simple method of calculating the switching losses is the piecewise linear model, as introduced by [7]-[9]. However, the parasitic inductance, the nonlinearity of the parasitic capacitances of transistors, and the reverse recovery effect and output capacitance of the synchronous transistor are not taken into account; therefore there may be a significant disagreement between the measurements and calculations. Based on detailed equivalent circuit, [10]-[12] proposed analytical switching loss models for MOSFETs; in these models, the current overshoot during turn-on is estimated by using only the reverse recovery characteristics of diode and the impact of the parasitic capacitance of diode is not taken into account. However, this approach does not hold for GaN transistors; first of all, there is no reverse recovery for GaN transistors; secondly, the voltage falling slope dv_{ds}/dt is steep (e.g., a few tens of volts per nanosecond), causing a large displacement current flowing through the parasitic capacitances of the synchronous transistor as well as the channel of the main transistor.

Recently, some switching loss models for GaN transistors have been proposed [13]-[17]. In [13], an accurate analytical loss model is presented for high-voltage GaN HEMT in a cascaded configuration, which is different from the enhancement mode GaN HEMT. In [14], Jones *et al* examine the temperature-dependent turn-on loss for GaN HEMTs, but do not take into account the parasitic inductance. In [15], a simple and accurate switching model is developed based the parameters extracted from the static I-V and C-V characteristics; however, this model can only be solved with a numerical approach, i.e., implemented with PSpice in [15]. Wang *et al* [16] presented an analytical switching model based on the detailed parasitic parameters; but this model is not for high-voltage GaN eHEMTs. By considering the nonlinearity of parasitic capacitances, Wang *et al* developed a turn-on loss model for high-voltage GaN eHEMTs in [17] where the numerical calculation must be used, which is relatively complicated and needs more time effort in practice.

This paper develops a simple analytical turn-on model for 650-V GaN eHEMTs. The normalized parameters (e.g., parasitic capacitances and transconductance) are extracted from the static C-V and transfer characteristics and they are further linearized. Then the turn-on process is divided into multiple stages and an equivalent-circuit based piecewise analytical model is built. Finally, measurements from double-pulse tests verify the developed turn-on loss model.

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II. Parameter Characterization of GaN eHEMTs

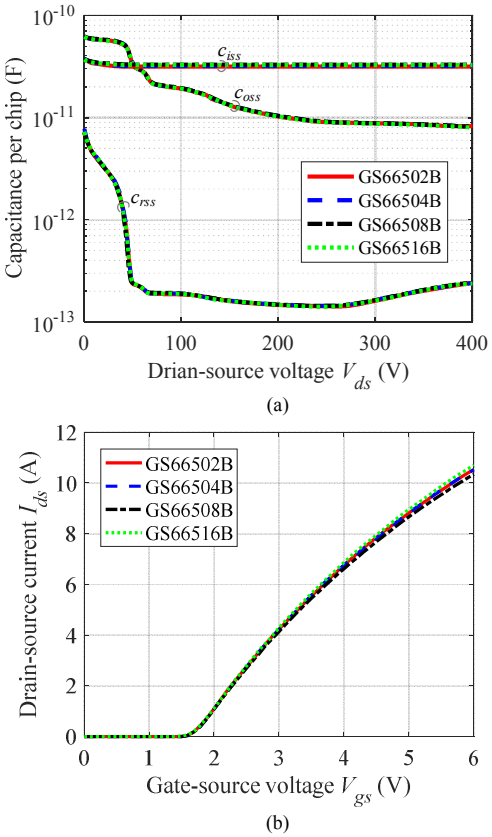

Fig. 1. Normalized GaN eHEMTs characteristics: (a) capacitances and (b) transconductance from datasheet.

The switching process in GaN eHEMTs is directly related to the parasitic capacitances and transfer characteristics, which can be obtained from the datasheet. For a series of GaN eHEMTs with the same voltage rating, the high current rating is achieved by increasing the number of chips in parallel inside the device. Divided by the number of chips in parallel, N, the normalized static parameters, e.g., the parasitic capacitances and transfer characteristics can be obtained from the datasheet, as shown in Fig. 1. It can be seen that the normalized parameters show the same trend and they are nonlinear.

In order to simplify the switching behavior characterization, a piecewise linear curve fitting is conducted, as depicted in Fig. 2. For the transfer characteristics, it can be fitted as $i_{ds} = g_{fs}(V_{gs} - V_{th})$ where g_{fs} is the transconductance and V_{th} is the threshold voltage. For the normalized output capacitance c_{oss} and reverse (gate-drain) capacitance c_{rss}, both of them are piecewise constant: when the drain-source voltage V_{ds} is lower than the knee point voltage V_{kn}, $c_{oss} = C_{ossH}$ and $c_{rss} = C_{rssH}$; when the drain-source voltage V_{ds} is higher than the knee point voltage V_{kn}, $c_{oss} = C_{ossL}$ and $c_{rss} = C_{rssL}$. Thus, the whole turn-on process can be described by linear differential equations, which makes an analytical turn-on model possible.

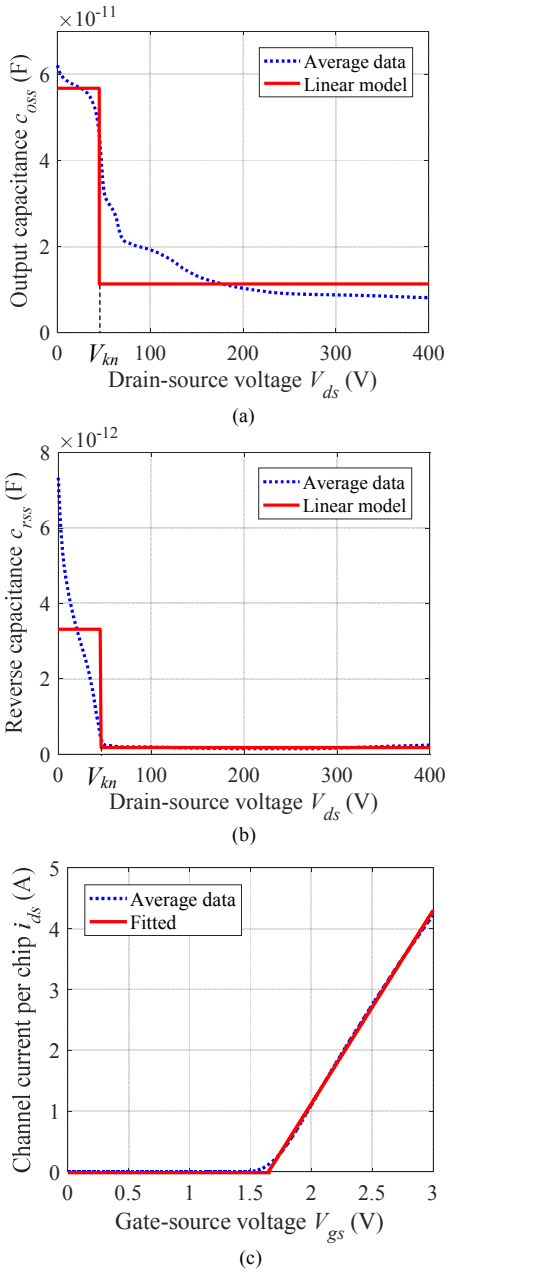

Fig. 2. Curve fitting for the (a) output capacitance, (b) reverse capacitance and (c) transconductance.

III. Switching Process of GaN eHEMTs

A half-bridge composed of two GaN transistors and parasitic inductances is shown in Fig. 3(a). The parasitic inductance can be obtained from datasheet or Q3D simulation in ANSYS, and they can be lumped together. In addition, during the turn-on transition, the upper switch S_1 can be regarded as a diode with an output capacitance. Thus, the simplified schematic can be derived, as shown in Fig. 3(b). The key turn-on waveforms of S is depicted in Fig. 3(c). As can be observed, four main stages can be identified, but only stages II and III involve energy loss and are considered in this study.

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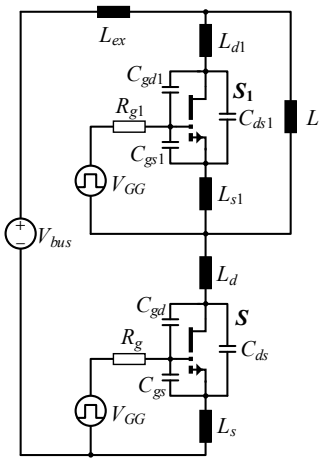
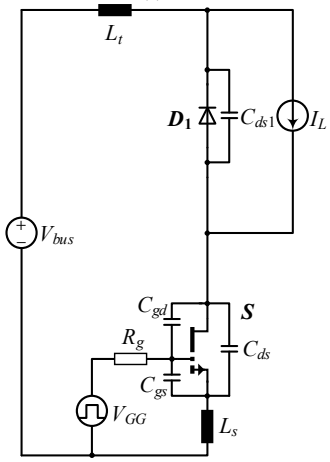


(a)



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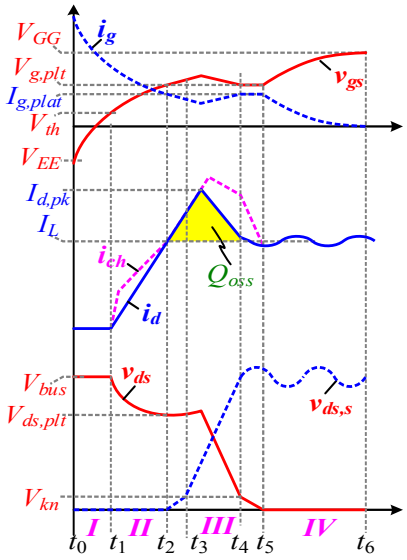

(c)

Fig. 3 (a) Half-bridge composed of two GaN eHEMTs; (b) Simplified structure for the turn-on process analysis; (c) operation waveforms during the turn-on period.

Stage I (t_0-t_1): Turn-on Delay Stage

At t_0, the gate signal V_{GG} is applied and the input capacitance C_{iss} ($C_{iss} = C_{gd} + C_{gs}$) is charged through the gate resistor R_g. Thus, the gate charge v_{gs} is increased as

$$v_{gs}(t) = V_{GG} - (V_{GG} - V_{EE})\exp\left(-\frac{t - t_0}{\tau_{iss}}\right) \tag{1}$$

where V_{GG} and V_{EE} are the positive and negative gate driver voltages, respectively; $\tau_{iss} = R_g(C_{gs} + C_{gd})$. The channel of switch S is kept off before the gate voltage v_{gs} reaches the threshold voltage V_{th}. No power loss occurs during this stage.

Stage II (t_1-t_2): Current Rising Stage

At t_1, the gate voltage v_{gs} rises to the threshold voltage V_{th} and the channel of S begins to conduct the current. In this stage, the channel operates as a voltage-controlled current source, i.e., $i_{ch}(t) = g_{fs}[v_{gs}(t) - V_{th}]$. The drain current i_d rises as the gate voltage goes up, but it is still smaller than the load current I_L. Therefore, the rest of load current, i.e., I_L - i_d, is freewheeling through the diode D_1. Thus, we have

$$\begin{cases} i_d(t) = g_{fs}[v_{gs}(t) - V_{th}] + C_{oss}\dfrac{dv_{ds}(t)}{dt} \\ R_g i_g(t) = V_{GG} - v_{gs}(t) - L_s\dfrac{di_d(t)}{dt} \\ i_g(t) = C_{iss}\dfrac{dv_{gs}(t)}{dt} - C_{gd}\dfrac{dv_{ds}(t)}{dt} \\ v_{ds}(t) = V_{bus} - L_{loop}\dfrac{di_d(t)}{dt} \end{cases} \tag{2}$$

Performing Laplace transformation to (2) yields

$$i_d(s) = \frac{n_2 / s}{1 + c_2 s + b_2 s^2 + a_2 s^3} \tag{3}$$

where $a_2 = C_{iss}C_{oss}R_gL_{loop}$, $b_2 = L_{loop}(C_{gd}g_{fs}R_g + C_{oss})$, $c_2 = R_gC_{iss} + g_{fs}L_s$, $n_2 = g_{fs}(V_{GG} - V_{th})$.

Then we can obtain the time-domain solution to the drain current $i_d(t)$

$$i_d(t) = \frac{n_2}{a_2}\left(\frac{e^{x_0 t}}{x_0(x_0 - x_1)(x_0 - x_2)} + \frac{e^{x_1 t}}{x_1(x_1 - x_2)(x_1 - x_0)} + \frac{e^{x_2 t}}{x_2(x_2 - x_1)(x_2 - x_0)} - \frac{1}{x_0 x_1 x_2}\right) \tag{4}$$

$$x_k = -\frac{1}{3a_2}\left(b_2 - r^k K_2 - \frac{\alpha_2}{r^k K_2}\right), k = 0, 1, 2 \tag{5}$$

where $\alpha_2 = b_2^2 - 3a_2c_2$, $\beta_2 = 2b_2^3 - 9a_2b_2c_2 + 27a_2^2$, $r = (i\sqrt{3} - 1)/2$, and $K_2 = [(\sqrt{\beta_2^2 - 4\alpha_2^3} - \beta_2)/2]^{1/3}$.

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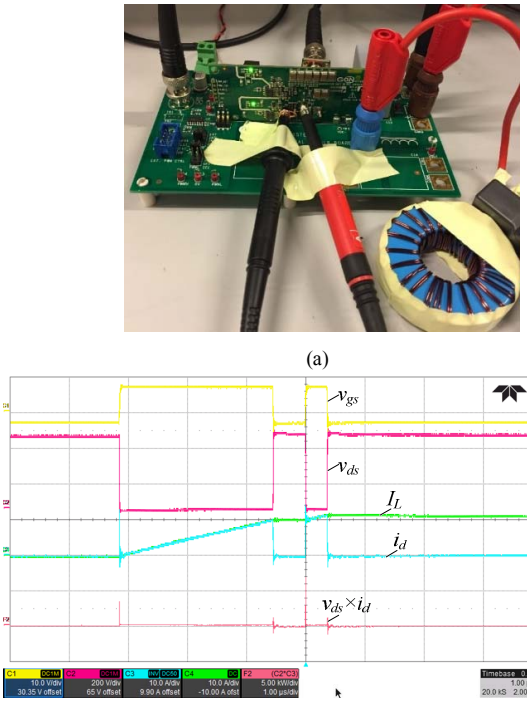

Fig. 4. (a) Double-pulse test setup; (b) Experimental waveforms.

By substituting (4) to (2), we can obtain the analytical solution to the drain-source voltage $v_{ds}(t)$.

Stage III (t_2-t_3): Voltage Fall Stage

At t_2, the drain current i_d rises to the load current I_L. Thus, the synchronous diode D_1 is turned off without reverse recovery and the parasitic capacitance C_{osst} begins to be charged. As results, there is a current overshoot at $i_d(t)$. During this stage, the drain-source voltage v_{ds} falls due to the discharging of C_{oss}. Then we have

$$\begin{cases} i_d(t) = g_{fs}[v_{gs}(t) - V_{th}] + C_{oss}\dfrac{dv_{ds}(t)}{dt} \\ R_g i_g(t) = V_{GG} - v_{gs}(t) - L_s\dfrac{di_d(t)}{dt} \\ i_g(t) = C_{iss}\dfrac{dv_{gs}(t)}{dt} - C_{gd}\dfrac{dv_{ds}(t)}{dt} \\ v_{ds}(t) = V_{bus} - L_{loop}\dfrac{di_d(t)}{dt} - v_{dst}(t) \\ i_d(t) = I_L + C_{osst}\dfrac{dv_{dst}(t)}{dt} \end{cases} \quad (6)$$

Performing Laplace transformation to (6) yields

$$v_{dst}(s) = \frac{m_3 + n_3 / s + p_3 / s^2 + u_3 s + w_3 s^2}{d_3 + c_3 s + b_3 s^2 + a_3 s^3} \quad (7)$$

where $a_3 = C_{iss}C_{oss}C_{osst}R_g L_{loop}$,

$b_3 = C_{osst}L_{loop}(C_{gd}g_{fs}R_g + C_{oss})$,

$c_3 = C_{osst}g_{fs}L_s + R_g C_{iss}(C_{osst} + C_{oss})$,

$d_3 = C_{gd}g_{fs}R_g + C_{osst} + C_{oss}$,

$m_3 = C_{iss}C_{oss}R_g(V_{bus} - V_{dsp}) + C_{osst}V_{dstp}(g_{fs}L_s + C_{iss}R_g) + (I_{dp} - I_L)(C_{oss} + C_{gd}g_{fs}R_g)L_{loop}$,

$n_3 = g_{fs}L_s(I_{dp} - I_L) + (C_{oss} + C_{gd}g_{fs}R_g)(V_{bus} - V_{dsp}) + R_g C_{iss}[g_{fs}(V_{gsp} - V_{th}) - I_L] + C_{osst}V_{dstp}$,

$u_3 = V_{dstp}L_{loop}C_{osst}(C_{oss} + C_{gd}g_{fs}R_g) + C_{iss}C_{oss}L_{loop}R_g(I_{dp} - I_L)$,

$w_3 = C_{iss}C_{oss}C_{osst}L_{loop}R_g V_{dstp}$.

By performing inverse Laplace transformation to (7), we can obtain the time-domain solution $v_{dst}(t)$

$$\begin{aligned} v_{dst}(t) = {} & \frac{y_0\{y_0[m_3 + y_0(y_0 w_3 + u_3)] + n_3\} + p_3}{y_0^2(y_0 - y_1)(y_0 - y_2)} e^{y_0 t} \\ & + \frac{y_1\{y_1[m_3 + y_1(y_1 w_3 + u_3)] + n_3\} + p_3}{y_1^2(y_1 - y_2)(y_1 - y_0)} e^{y_1 t} \\ & + \frac{y_2\{y_2[m_3 + y_2(y_2 w_3 + u_3)] + n_3\} + p_3}{y_2^2(y_2 - y_1)(y_2 - y_0)} e^{y_2 t} \\ & - \frac{n_3 y_1 y_2 y_0 + p_3(y_1 y_2 + y_1 y_0 + y_2 y_0)}{(y_1 y_2 y_0)^2} - \frac{p_3 t}{y_1 y_2 y_0} \end{aligned} \quad (8)$$

$$y_k = -\frac{1}{3a_3}\left(b_3 - r^k K_3 - \frac{\alpha_3}{r^k K_3}\right), k = 0,1,2 \quad (9)$$

where $\alpha_3 = b_3^2 - 3a_3 c_3$, $\beta_3 = 2b_3^3 - 9a_3 b_3 c_3 + 27a_2^2 d_3$, $K_3 = \left(\dfrac{-\beta_3 + \sqrt{\beta_3^2 - 4\alpha_3^3}}{2}\right)^{1/3}$. Substituting (8) into (6) yields the full solution.

Stage IV (t_3-t_4): On-State Operation

At t_3, the drain-source voltage v_{ds} reaches $V_{ds(on)}$; and the output capacitance C_{osst} begins to resonate with the loop inductance L_{loop}. The power loss in this stage is small and therefore it is not considered.

IV. Experimental Verifications

A double-pulse test setup has been built for GS66504B, as shown in Fig. 4(a). The double-pulse test waveforms are shown in Fig. 4 where the bus voltage V_{bus} is equal to 400 V, the gate driver voltage is between -3V and 6 V, the external gate resistor is 13 Ω and the high-frequency loop inductance is about 17.1 nH. A high bandwidth (500 MHz) oscilloscope is used and a 2-GHz coaxial current shunt (SDN-414-10, 0.1Ω) from T&M Research is installed for switching current measurement.

In order to verify the developed power loss model, a comparison of switching waveforms between the experiment and calculation is shown in Fig. 5(a) and (b). As can be

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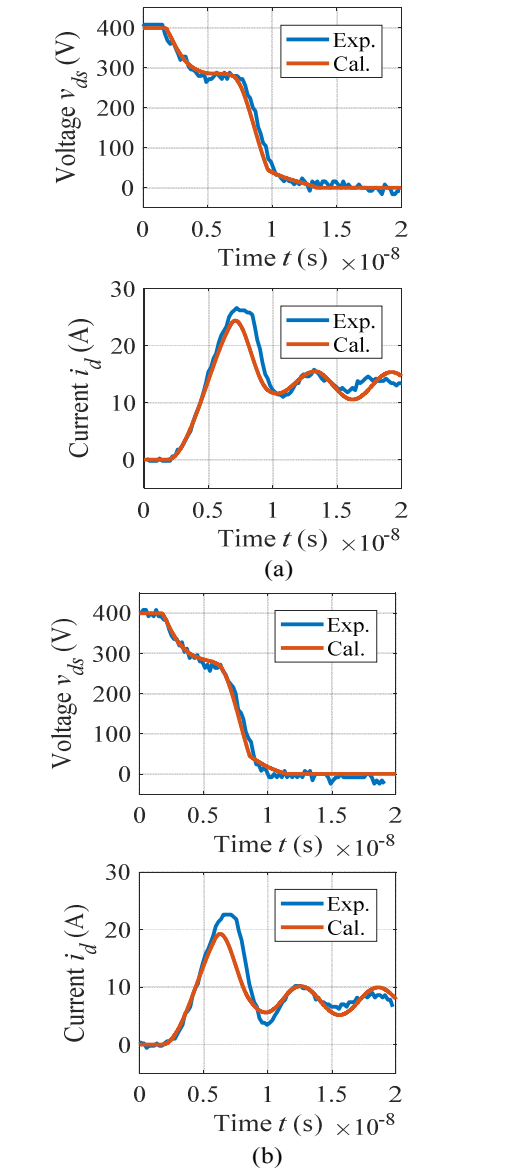

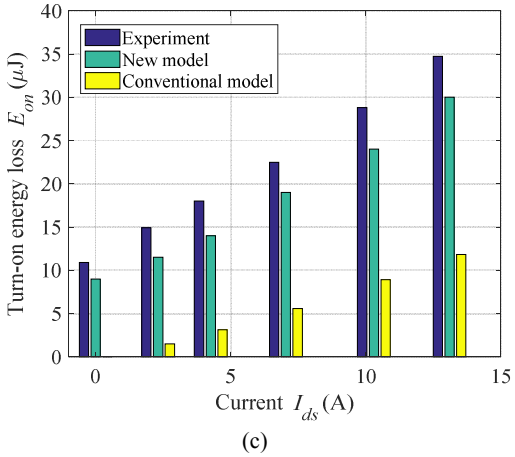

Fig. 5. Comparison between the measurements and calculations: (a) turn-on waveforms at I_L = 13 A; (b) turn-on waveforms at I_L = 7.5 A; (c) turn-on energy losses.

observed, a good agreement is achieved for both the drain-source voltage v_{ds} and drain current i_d. The measured and calculated turn-on energy losses are presented in Fig. 5(c). Compared with the conventional piecewise linear model, the developed analytical model can predict the turn-on loss with smaller error.

V. Conclusions

This paper developed an accurate turn-on power loss model for 650-V GaN eHEMTs. A double-pulse test setup for GS66504B was built for model validation. Compared with the conventional piecewise linear model, the developed model can predict the turn-on energy loss with much smaller error. In addition, the proposed model takes much less time effort to characterize the switching behavior.

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