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# A Desaturation-based Short Circuit Protection Technique for Quasi-Two-Level Converters

Anand Krishnamurthy Iyer [1], Henk Polinder [2], Thiago Batista Soeiro [1]

[1] Power Electronics Group, University of Twente, The Netherlands
[2] Department of Maritime and Transport Technology, Delft University of Technology, The Netherlands

Corresponding author: Anand Krishnamurthy Iyer, a.k.iyer@utwente.nl
Speaker: Anand Krishnamurthy Iyer, a.k.iyer@utwente.nl

## Abstract

This paper presents a desaturation-based technique for short-circuit protection in quasi-two-level converters. The proposed design enables a cost-effective implementation of this protection scheme in a flying capacitor multilevel converter operating as a quasi-two-level converter, requiring only two detection circuits for $n$ series-connected switches. Detailed design guidelines for the protection circuit are provided, along with simulations that illustrate its operational boundaries and experimental verification of the proposed scheme.

## 1 Introduction

Two-level converters are widely used in industry due to their robustness, simple control, and cost-effectiveness. Advances in semiconductor technologies have significantly enhanced their performance. With the increasing electrification of various industries, particularly in transportation, it is crucial to explore the potential of utilizing mature semiconductor technologies in applications requiring higher voltages and power levels.

One such approach is the Quasi-Two-Level (Q2L) converter, which leverages existing multilevel topologies while modulating them to operate as a two-level converter. This technique enables the series connection of low-voltage blocking semiconductor devices, which typically offer superior performance and cost advantages compared to a conventional two-level converter with similar capabilities [1], [2], [3]. In this case, the flying-capacitor multilevel (FCML) converter operated as a Q2L converter is considered, as it offers several advantages. Compared to NPC converters, it requires fewer switches, utilizes small flying capacitors ($<$1 µF), and closely resembles a conventional two-level converter in its Q2L operation. The Q2L FCML-based converter under consideration is shown in Fig. 1.

The Q2L bridge can also replace half-bridges in traditional topologies, offering similar performance benefits [4], [5]. For the Q2L converter to be a viable alternative in the aforementioned applications, auxiliary circuits play a crucial role in cost and reliability, making their design considerations essential for widespread adoption. A significant cost factor in such scalable concepts is the gate driver and associated auxiliary components, including protection circuitry, which also scales with the number of semiconductor devices used.

This paper introduces a desaturation (DESAT)-based protection architecture for Q2L converters, utilizing only one DESAT detection circuit per switch ($S_1$ and $S_2$). This approach reduces costs by enabling the use of simple gate drivers for all switches while employing discrete protection circuitry, effectively safeguarding the bridge against short circuits as opposed to protecting the individual devices using their own DESAT detection circuits. The Q2L converter with the proposed DESAT detection architecture is shown in Fig. 1.

The paper begins with the Q2L converter design in section 2, followed by the proposed DESAT-based protection scheme and its specific considerations for Q2L converters in section 3. Short-circuit scenario simulations and related discussions are presented in section 4, with experimental verification using a hardware prototype detailed in section 5.

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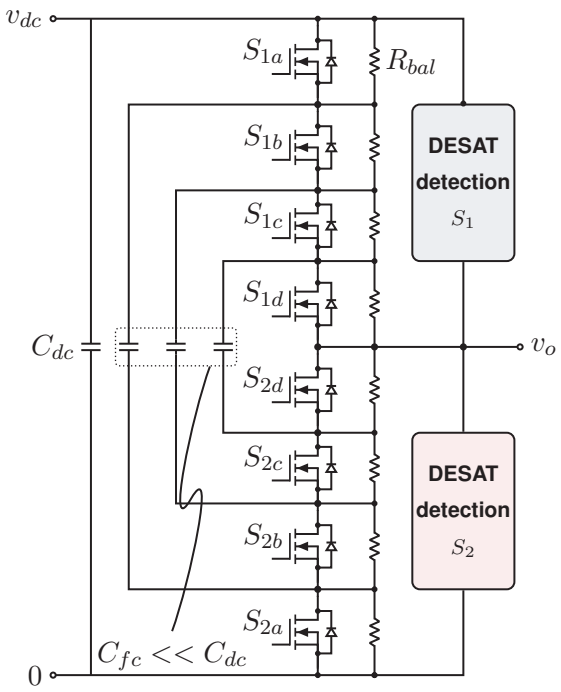


**Fig. 1:** A five-level FCML converter operated as a Quasi-two-level converter with balancing resistors along with the proposed DESAT detection in the outer switches. All $S_1$ and $S_2$ switches are commanded (synchronously) with the same PWM signal respectively. Over-current detection in any of the shown DESAT shuts down the whole circuit.

## 2 Q2L converter design

Designing a Q2L converter involves additional considerations compared to a conventional two-level converter. One significant advantage of the Q2L approach is the ability to use lower-voltage-rated semiconductor devices, which typically offer superior performance compared to their higher-voltage-rated counterparts [2], [3].

Another crucial aspect is the flying capacitor, as it influences both the converter's size and the blocking voltage applied across individual switches. The control strategy for the bridge switches directly impacts the design of the flying capacitor and its voltage balancing capability. This section first discusses the switching sequences, followed by an analysis of their implications on flying capacitor voltage balancing.

### 2.1 Switching sequence

The flying capacitors are sized to minimize voltage ripple, which in turn influences the voltage ripple across individual switches. The peak voltage ripple across the flying capacitors can be determined using Eq. (1):

$$\Delta v_{fc,pk-pk} = \frac{2 \cdot t_{del} \cdot I_{pk}}{C_{fc}} \tag{1}$$

where $t_{del}$ is the time delay between two individual switches turning on, $I_{pk}$ is the peak load current and $C_{fc}$ is the capacitance of the flying capacitor. Based on Eq. (1), the Q2L converter can be operated in two modes:

1. Synchronous switching: In this mode, a single PWM signal is given to all the gate drivers of the inner switches corresponding to $S_1$ and $S_2$ respectively. Thus, all the switches are expected to turn-on synchronously, and the flying capacitors will act only to clamp transient delays between the inner switches. This allows very small sizing of the flying capacitors, such as 100 nF, since for a maximum propagation mismatch of 10 ns, and a peak current of 20 A, the peak voltage ripple is only 4 V.

2. Staggered switching: In this mode, the PWM signals of the individual switches, such as $S_{1_{n-1}}$ and $S_{1_n}$, are phase-shifted by a small, controlled delay in the order of hundreds of nanoseconds. This technique provides more precise control over the turn-on times of individual switches and enables optimization of the harmonic performance of the converter's output voltage [6]. In this case, the required flying capacitance can be determined using Eq. (1).

In this paper, the primary focus is on synchronous switching.

### 2.2 Voltage balance

Maintaining voltage balance in the flying capacitors is crucial, as it directly affects the blocking voltage applied to individual switches. The following considerations must be addressed to ensure proper voltage balancing:

1. No-load voltage balancing is achieved using balancing resistors ($R_{bal}$). The selection of $R_{bal}$ involves a trade-off between the required balancing dynamics and acceptable power loss. Under synchronous switching, $R_{bal}$ must be chosen to ensure stable flying capacitor voltage balancing in steady-state operation.

2. Modulation-based balancing for staggered switching can be achieved by adjusting the

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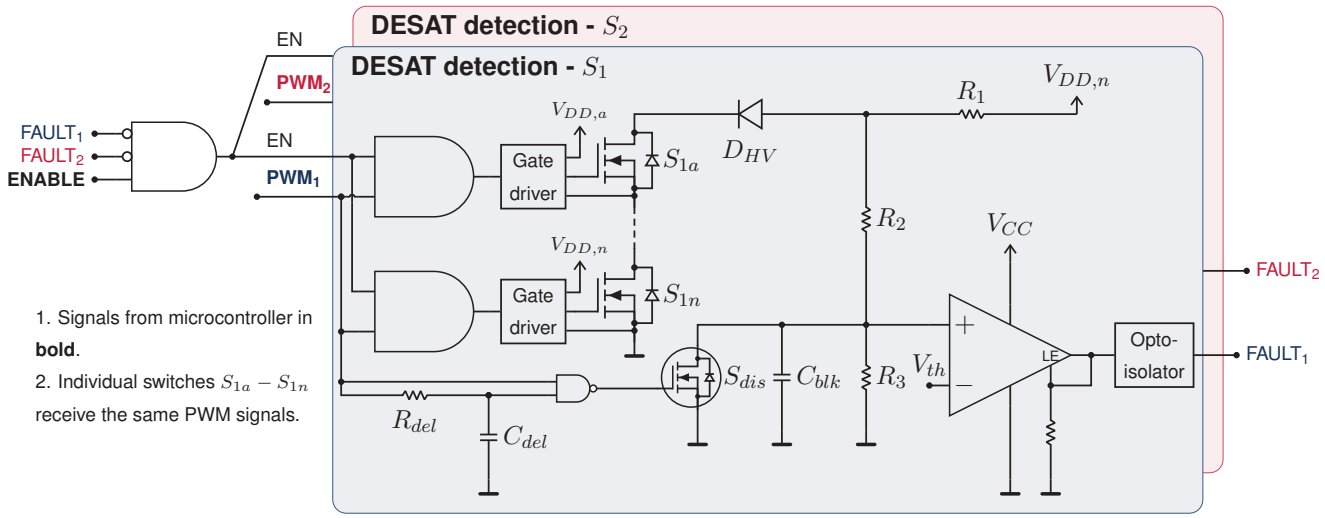


**Fig. 2:** The proposed DESAT-detection circuit which works by measuring the overall voltage across $S_{1a}$ to $S_{1n}$. The detection circuits are referenced to the bottom-most switches i.e. $S_{1n}$ and $S_{2a}$ respectively. The comparator shown has a Latch-enable (LE) input, due to which the output is latched when the logic goes HIGH. The isolated gate-drivers employed are simple opto-isolated gate-drivers without inbuilt protection features to reduce the overall cost of the system.

phase shift between individual switches [7], [8]. This can be implemented either in an open-loop manner using pre-determined switching states or in a closed-loop approach by actively measuring the flying capacitor voltage. Further details on implementation can be found in the relevant literature [7], [8].

By applying the aforementioned methods, capacitor charge balance is maintained, ensuring stable voltage across the semiconductor devices. With these design considerations in place, the next step is to develop the DESAT-based protection system.

# 3 Proposed DESAT based protection design for Q2L converters

With the converter design established, the various types of short circuits are examined. This is followed by a discussion on DESAT circuit design guidelines and key considerations specific to Q2L converters.

## 3.1 Short-circuit protection based on DESAT detection

Short circuits with low inductance can be classified into two types: fault under load, where the switch is already conducting load current when the fault occurs, and hard-switching faults, where the short circuit happens during the turn-on transition of the device [9], [10], [11].

High-inductance short circuits are typically caused by external events and are limited by the impedance of the surrounding circuit. As a result, the $^{\mathrm{d}i}/_{\mathrm{d}t}$ is significantly lower compared to low-inductance short circuits, reducing the impact on the semiconductor device [11]. This study focuses solely on low-inductance short circuits, specifically the hard-switching type.

The DESAT-based protection is one of the most widely implemented short-circuit protection methods in power converter switching bridges. It originates from IGBT short-circuit protection, where the collector-emitter voltage is monitored to detect when the IGBT enters desaturation during a fault [11]. This method is highly effective for IGBTs, as they can withstand short-circuit conditions for relatively long durations [11]. For MOSFETs, the same principle can be applied; however, their short-circuit withstand time is significantly lower than that of IGBTs [11], [12]. This necessitates much faster response times to effectively protect the device.

## 3.2 DESAT detection circuit design

DESAT protection operates by triggering a protective response when the drain-source voltage of a MOSFET exceeds a predefined threshold. In a Q2L converter, however, each switch consists of $n$ series-connected semiconductor devices instead of a single switch. To protect the entire bridge against short circuits, the total effective drain-source voltage of $S_1$ and $S_2$ is monitored as shown in Fig. 1. If this voltage exceeds the threshold, the protection mechanism is activated.

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The implementation of the detection circuit is depicted in Fig. 2. The DESAT protection operates as follows:

– Off-state: During the off-state of the switch, the PWM signal is LOW, and the corresponding gate signal for $S_{dis}$ is HIGH. This implies that the the non-inverting input of the comparator is pulled low, and thus, the drain-source voltage of the equivalent switches are not measured.

– On-state: When the device is turned on, the PWM signal is HIGH, and the corresponding gate signal for $S_{dis}$ is LOW. The diode $D_{HV}$ is forward-biased and thus, the non-inverting input measures a scaled value of the effective drain-source voltage. The detection voltage is controlled by the resistive divider $R_2$ and $R_3$. The diode, $D_{HV}$ helps clamp the voltage to a reasonable value set by $R_1$ such that the comparator common-mode input voltage limits of the comparator are respected. The detection threshold voltage is given by:

$$V_{det} = V_{th} \cdot \frac{R_2 + R_3}{R_3} - V_{F,D_{HV}} \tag{2}$$

where $V_{det}$ is the threshold effective drain-source voltage for DESAT detection, $V_{th}$ is the comparator threshold reference voltage that is implemented with a separate resistive voltage divider, $R_2$ and $R_3$ form a resistive voltage divider, $V_{F,D_{HV}}$ is the diode forward-voltage drop of the high-voltage diode ($D_{HV}$).

– Blanking time: To prevent false triggering of the DESAT, blanking times are introduced. There are two blanking times implemented. The first blanking time is set by the $RC$ time delay of the resistive divider along with $C_{blk}$. The shortest time response of this circuit is determined by the maximum voltage measured across the devices above which the diode $D_{HV}$ is reverse-biased and the voltage across the resistive divider is clamped. The maximum non-inverting voltage input is given by:

$$V_{+,max} = V_{DD} \cdot \frac{R_3}{R_1 + R_2 + R_3} \tag{3}$$

where $R_1$, $R_2$ and $R_3$ are a resistive voltage divider and $V_{DD}$ is the gate-driver voltage (here 15 V). Based on Eq. (3), the blanking time can be calculated by:

$$t_{blk,1} = -\frac{R_1 + R_2}{R_1 + R_2 + R_3} \cdot R_3 \cdot C_{blk} \cdot \ln\left(1 - \frac{V_{th}}{V_{+,max}}\right) \tag{4}$$

where $C_{blk}$ is the blanking time capacitor.

The second blanking time is set by the turn-off delay implemented for the gate-signal of $S_{dis}$. This is given by:

$$t_{blk,2} = R_{del} \cdot C_{del} \tag{5}$$

The effective blanking time is the sum of both Eqs. (4) and (5). It is noted that the blanking time set by $C_{blk}$ can be set to adjust the sensitivity of transients triggering the DESAT and the sensitivity during normal commutation can be adjusted by Eq. (5). The operation of the DESAT protection in normal on-state is shown in Fig. 3.

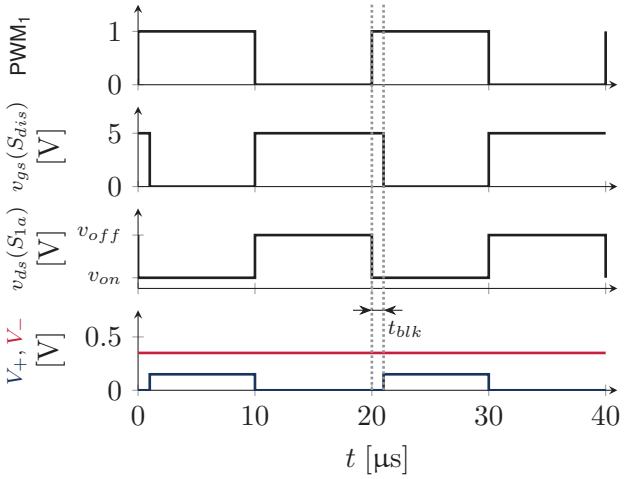


**Fig. 3:** The DESAT detection logic in $S_1$. When $S_1$ is turned on, $S_{dis}$ is turned-off with a delay tuned by $R_{del}$ and $C_{del}$ allowing for blanking time during the commutation. When $S_1$ is turned off, $S_{dis}$ pulls down the non-inverting input of the comparator, thus preventing false-triggering of the FAULT. The non-inverting voltage rise-time can be tuned by $C_{blk}$ which also contributes to the blanking time (not indicated in the figure).

– FAULT latch: It is important that once the fault is detected, the state remains latched. This can be done with a comparator with a latch-enable pin (shown in Fig. 2), or with an external latch circuit. This needs to then be given as part of the ENABLE signal for the whole bridge

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to ensure the protection shuts down the switching operation of the switch when the fault is detected.

### 3.3 Q2L considerations

In the Q2L converter, the individual switches ($S_{xa}$ to $S_{xn}$) experience unequal energy dissipation during a short circuit. This imbalance arises from the energy stored in both the decoupling capacitor and the flying capacitors. The inner switch $S_{xd}$ in this case endures the highest stress, as it must dissipate energy from all these capacitors. This behavior can be demonstrated through both simulations and hardware prototypes.
In the Q2L converter, two types of hard-switching faults can occur.

1. Full-bridge shoot-through: A shoot-through of the bridge due to possible control logic mismatch.

2. Single half-bridge shoot-through: The more probable type of short-circuit is one that occurs in only one complementary switching pairs, for example: $S_{1b}$ and $S_{2b}$ being turned on together. This could occur due to one of the devices failing as a short and thus, creating an undesirable shoot-through.

The maximum energy dissipation across one semiconductor can be calculated from Eq. (6):

$$E_{SC} = \frac{t_{SC} \cdot \Delta T_j}{Z_{jc}} \tag{6}$$

where $t_{SC}$ is the short-circuit time, $\Delta T_j$ is the maximum allowable temperature rise (in K) and $Z_{jc}$ is the transient thermal impedance between junction-to-case for the specified device for an applied pulse of time $t_{SC}$.
Based on the device datasheet [13], the thermal impedance is estimated to be 0.01 K/W for a 10 µs short-circuit pulse and the allowable temperature-rise is set to 100 K for more margin. The maximum allowable energy dissipation is calculated from Eq. (6) to be 100 mJ for the considered device, though it is advisable to allow sufficient margin. It is to be noted that this is only considering the power-dissipation based failure of the device during the short-circuit. Other modes of failure can exist and need to be considered during the design process [14].

**Tab. 1:** Simulation parameters

| Parameter | Value |
|---|---|
| Semiconductor device | IPB036N12N3 G |
| Parallel devices per switch | 2 |
| DC-link voltage | 400 V |
| DC-link capacitance | 300 µF |
| Decoupling capacitance | 500 nF |
| Flying capacitors | 500 nF |
| Short-circuit time | 1 µs |
| Protection | OFF |

## 4 Simulation of the short-circuit behavior

The simulations are done in InfineonSPICE for both kinds of fault to verify the energy dissipation for a worst-case 1 µs fault without protection. The parameters considered for the simulation are provided in Tab. 1.

### 4.1 Full-bridge shoot-through

The first short-circuit tested is the full-bridge shoot-through. This is done by keeping PWM 1 on and turning on PWM 2 simultaneously for 1 µs. The currents through the individual switches can be seen in Fig. 4. The maximum current through $S_{1a}$ is observed to be 680 A during the first peak at approximately 600 ns into the fault, whereas that of $S_{1d}$ is 1.1 kA. This is due to all the flying capacitors releasing energy into $S_{1d}$. It can also be observed in $S_{1a}$ that the main DC-link capacitor is also providing energy starting at around 250 ns into the fault. This is the reason that the second peak is almost similar for all the switches since the bulk of the energy is now provided by the main DC-link capacitor. The energy dissipation is also shown in Fig. 4 and it can be observed that the dissipated energy in $S_{1d}$ is higher than that of $S_{1a}$ until the bridge shuts down, during which the energy dissipation in $S_{1a}$ becomes higher due to charging of the flying capacitors. The voltage inputs to the comparator are also shown and it can be seen that the detection is done fairly early before the main DC-link capacitor dissipates significant energy into the bridge. Thus, the bridge can be well protected by measuring the total voltage across $S_{1a}$ to $S_{1d}$.

### 4.2 Single half-bridge shoot-through

The next short-circuit scenario to be tested is a single half-bridge shoot-through. In this case, the

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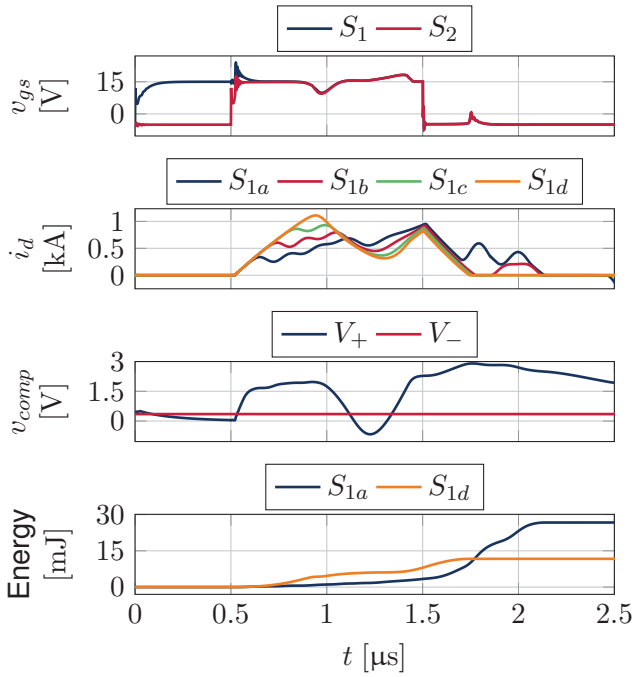


**Fig. 4:** Simulation of full-bridge short-circuit of the Q2L converter. The short-circuit occurs between 0.5 µs to 1.5 µs, and the currents through individual devices in $S_{1a}$ to $S_{1d}$ are shown (Each switch consists of two devices in parallel).

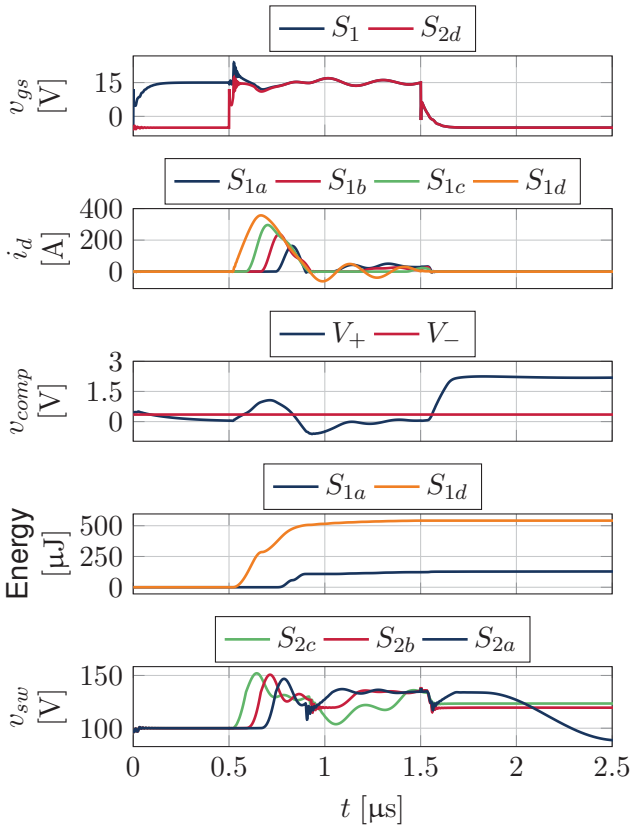


**Fig. 5:** Simulation of a single-bridge short-circuit which occurs with $S_{2d}$ falsely turning on between 0.5 µs to 1.5 µs ($S_{2a,b,c}$ are turned-off). The current through $S_{1d}$ can be observed to rise rapidly after which device voltage across $S_{2c}$ also rises due to the flying capacitor being discharged. The protection time is critical for such a scenario to prevent device overvoltage from occurring.

inner switches $S_{1d}$ and $S_{2d}$ are short-circuited for 1 µs as shown in Fig. 5. The peak current through $S_{1d}$ is simulated to be 356 A and the peak current through $S_{1a}$ is measured to be 163 A. It can be observed that the energy dissipation is much lower than that of the full-bridge shoot-through. However, a more critical problem in this scenario is the voltage applied across the turned-off devices. It can be observed that the voltage across $S_{1c}$, i.e. the device right next to the short-circuited device starts shooting up rapidly as the flying capacitor discharges into the short-circuited bridge. This can lead to destruction of devices if this is not shut-down in time. From the voltage inputs to the comparators, it can be observed that the fault can be detected quickly, and the bridge can be shut-down well in advance to prevent overvoltage across the semiconductors. In such a scenario, a trade-off between the propagation delay, additional overvoltage detection, and device voltage blocking capability exists and it needs to be done individually for each selected semiconductor. Thus, such a fault has the potential to be even more severe than the full-bridge shoot-through due to the change in flying capacitor voltages.

## 5 Experimental validation of hardware prototype

Based on the simulation, the hardware prototype is designed, which is shown in Fig. 6. In the current work, the hardware is tested only for the full-bridge shoot-through scenario.

The hardware is commissioned with IPB036N12N3-G devices, with two in parallel for each switch for better current carrying capability. There is an option on the board to command with synchronous switching or separate gate-pulses for each switch. For the purpose of this test, the synchronous switching is used. This board can also be commissioned as a true FCML, by soldering film capacitors in the provided footprints. For the purpose of this test, small ceramic capacitors of 500 nF (can be observed below the heatsink) are used.

The short-circuit operation is tested at a lower voltage of 80 V. To test this scenario, $S_1$ is kept ON,

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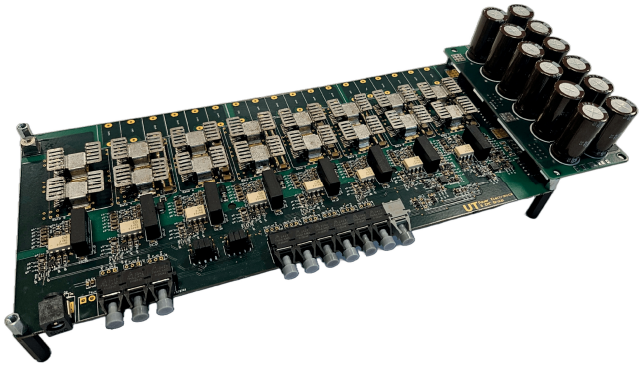

**Fig. 6:** Hardware prototype for experimental verification of the proposed DESAT-based protection of the Q2L converter. Two devices are used in parallel for each switch. The switches can either be controlled synchronously (shorted on a header) or controlled separately using the additional optical ports to do staggered switching sequences.

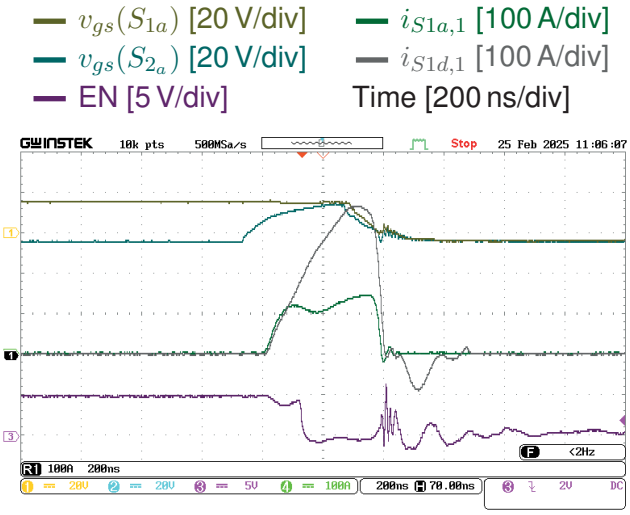


**Fig. 7:** Experimental verification of the full-bridge short-circuit. The currents through one device of $S_{1a}$ and $S_{1d}$ are measured to represent the significant difference in the energy dissipation during the short-circuit. The fault is detected within 100 ns (EN signal goes LOW) and the gate-source voltage is pulled down within 300 ns.

and $S_2$ is turned on for 1 µs to create a full-bridge shoot-through. The pulse timing and the voltage are limited to prevent damage of the prototype in case of short-circuit detection failure. The test results can be seen in Fig. 7. The voltages are measured using MicSig DP1007 high-voltage differential probe that have a bandwidth of 100 MHz. The currents are measured on one device ($S_{1a}$ and $S_{1d}$) using PEM CWT Ultra-mini Rogowski current coil which can measure up to 600 A up to a bandwidth of 50 MHz.

The fault is detected within approximately 100 ns, with the gate-source voltages pulled-down in another 100 ns. The whole system is shut down within 400 ns from the occurrence of the short-circuit. It can be seen that the current in $S_{1d}$ is much higher than that through $S_{1a}$. This is explained due to the fact that the inner switch dissipates the energy of all the flying capacitors as well as explained in section 3. Since the fault lasts for a relatively short time, the main DC-link capacitor has not yet fully started providing energy to the bridge and thus, the current through $S_{1a}$ is limited.

## 6 Conclusion

A DESAT-based protection scheme is introduced for Q2L converters, utilizing the measurement of effective voltage across both the top-side and bottom-side switches. The design guidelines for this protection circuit, along with the associated trade-offs in Q2L converters, are discussed in detail. Simulations demonstrate that the scheme effectively prevents shoot-through in both the entire bridge and individual half-bridges, provided propagation delays remain minimal. Additionally, low-voltage experimental results validate the effectiveness of the proposed protection technique. In the future, the prototype will be tested in different fault scenarios to verify its safe and advantageous applicability in Q2L converters.

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