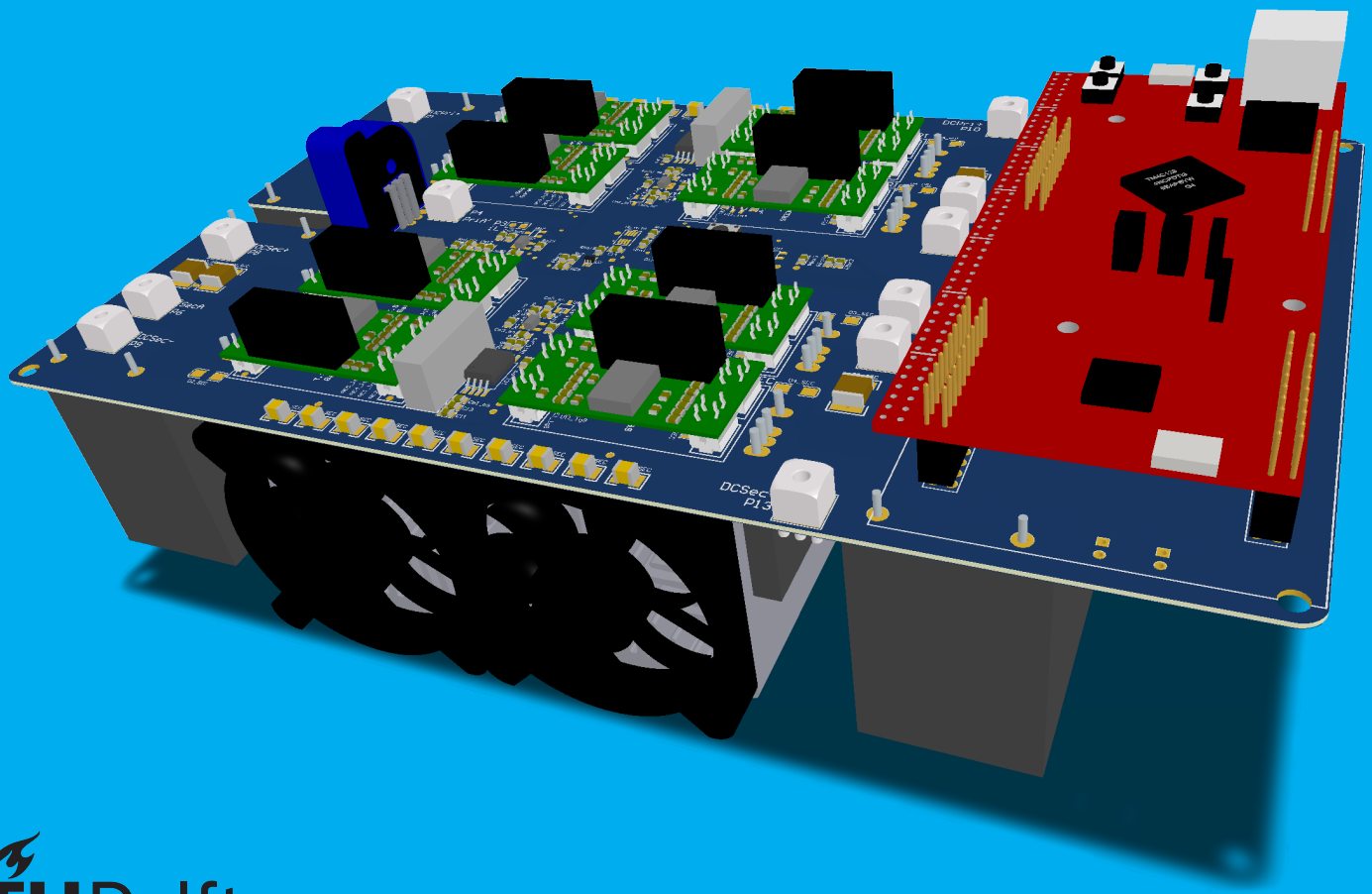
Electric Vehicle Charger

for Future DC Grids

T.M. Al

Design of an isolated bidirectional DC-DC power converter capable of transferring **10 kW** at any output voltage between **300 V** and **1000 V**.

Department of DC Systems, Energy Conversion & Storage



TU Delft

Electric Vehicle Charger

for Future DC Grids

by

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Abstract

Over the last decade the share of electric vehicles has increased and will continue to increase in the future in order to reduce the carbon footprint by transportation. However, the battery voltage is not standardised and can differ per car model. To reduce the charging time, a high power converter is preferred. Moreover, in order to utilise the car as a storage element and enable the Vehicle to Grid functionality, the capability of a bidirectional power flow is needed.

In this master thesis a DC-DC converter is designed for a wide output voltage range, with the focus on a high efficiency. Firstly a literature review is done, where the Dual Active Bridge (DAB) converter is chosen as a promising topology. The rectangular (single phase shift), triangular and trapezoidal current modulation are all investigated. For the actual design, two types of transistors are considered, followed by the design of a transformer and inductor. In the end a prototype according to the design is made and the modulation method is implemented in a digital controller.

Due to some extraordinary circumstances, building the converter and measuring the performance was not possible. This means this project ended with a finished theoretical design, with the expected performance verified later.

Acknowledgements

I would like to take the opportunity to thank my supervisors, starting with Thiago. He offered an interesting project and gave me confidence to shape it in the way I liked most. I appreciated the freedom that was given to me to choose something I really found interesting. Whenever I had doubts or questions I could walk by his office where he took time for me to discuss these issues. After some months I met Lyu, who was also supervising me. He always took time helping me and I have enjoyed the time discussing certain problems or the progress with him. I have learned a lot from you both and it was great to have you for supervision. Lastly, a special thanks to Calvin for helping me getting started with the control.

Despite the need to adapt the objectives slightly given the circumstances, I am happy with the way it went. However, it remains a bit sad that I could not perform the practical part in the laboratories to verify my work, which was actually one of the reasons for choosing this topic. I appreciate the way we could reshape the objectives and am sure someone will take over my work and finish it completely.

T.M. Al
Wormer, July 2020

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1 Introduction

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1.1. Background

Over the last years, the attention for climate change is increasing. As a result, a trend has started to reduce the amount of carbon that is produced by the production of energy. However, still a large part of the used energy has a significant carbon footprint [1], where transportation also has a significant contribution. One way to reduce the amount of emitted carbon is the use of electricity, provided that this electricity is generated in a so-called *green* manner. The use of more electrical energy instead of fossil fuels for all kinds of processes is called the energy transition. Big challenges are lying ahead where electricity has to be produced in a clean way, and more and more processes should rely on this type of energy.

Given that transportation was a significant contributor to the carbon footprint, electric cars are a type of transportation without emissions. Direct current (DC) is needed to charge the battery of an electric vehicle, and generally a higher current means faster charging.

The voltage of the battery while charging the electric vehicle (EV) is not constant, but varies depending on the state of charge [2] of the battery. Furthermore, the voltage is not standard for every electric vehicle, but differs [3], resulting in varying voltages of 400 V up to 800 V for electric vehicles [4, 5]. Lower voltages are found in the hybrid electric vehicles, and higher voltages are expected in newer models. To have a universal charger for many different car models, the power converter of the charger needs to be capable of delivering high power in a wide voltage range.

This thesis focusses on designing a DC-DC converter, which can supply high power under a wide output voltage range and with high efficiencies. The converter should be operating most of the time as a charger, i.e. delivering electricity from the grid to the vehicle (G2V), while having the possibility to deliver energy from the vehicle back to the grid (V2G). In this case the battery of the car can help balancing the supply and demand of electrical energy in the grid, which will be a future challenge with increasing amounts of renewable energy sources connected to the grid [6].

Lastly, the designed converter can be used in an AC grid, where it is a part of the system, but also in a DC grid. This promising idea of a DC distribution grid exist, since there is a large share of electricity sources providing, and electric appliances operating on DC. Having a DC distribution grid will eliminate the need of conversion steps in between, which may result in a higher overall energy conversion efficiency. In such a DC grid, the to be designed DC-DC converter is the complete interface between the electric vehicle and the grid.

1.2. Charging an electric vehicle

As already mentioned in the previous section, the voltage across the battery of an electric vehicle is not constant during charging. The voltage of the battery depends on the State Of Charge (SOC) of the battery. A typical charging profile of a lithium-ion battery is given in Figure 1.1 [2]. It can be seen that the charging of a

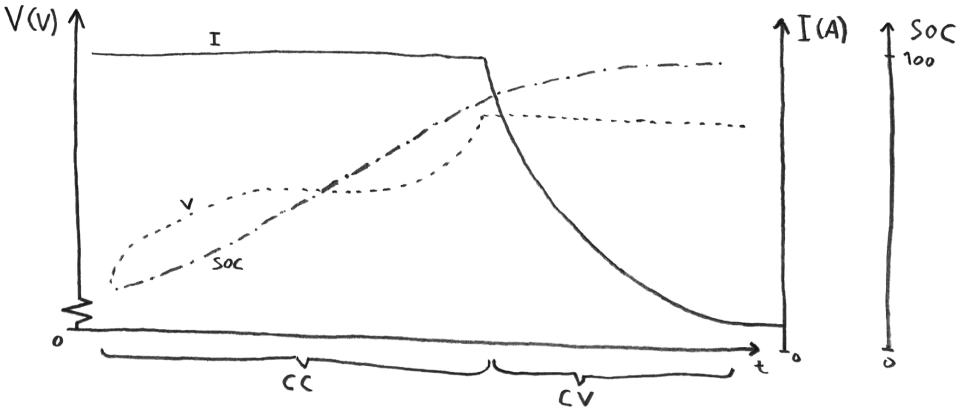


Figure 1.1: Typical charging profile of a lithium-ion battery

battery consist of two periods; the part of charging with constant current (CC) first and then the part of charging with constant voltage (CV). In the first phase of CC, the current rate is limited by the power the charger/ converter can supply. After that, constant voltage is applied until the battery is fully charged.

1.3. Requirements

The electric vehicle charger should be of a DC-DC converter type and be able to deliver 10 kW of power. There are of course electric vehicles that can be charged with much more power. Therefore, it is possible to put multiple converters in parallel (also known as interleaving) with a maximum power of 10 kW of each individual converter. Based on the actual load, an optimum can be found in the loading of each converter which can lead to an even higher efficiency [7] of the total system. The converter should be able to deliver power from the grid to the vehicle as well as from the vehicle to the grid. The grid voltage on which the converter should operate is 600 V and the voltage to the car battery can vary between 300 V up to 1000 V. This is because there is not a standard voltage level of the battery of an electric vehicle [3] and the to be design converter needs to be as versatile as possible. The upper limit is set to 1000 V because the battery voltages are increasing to reduce losses especially during fast charging. Furthermore, the converter should for safety reasons be galvanically isolated from the grid. Furthermore the circuit will demand for high power efficiency as well as low costs. All requirements are summarised in Table 1.1.

Table 1.1: Requirements of the converter

Requirements	
Type	DC-DC converter
Isolation	Galvanically
Input voltage	600 V
Minimum output voltage	300 V
Maximum output voltage	1000 V
Maximum output power	10 kW
Maximum output voltage ripple	10 V

1.4. Objective

The objectives of the research performed in this master thesis are as follows:

- Do a literature review on different types of DC-DC converters, with emphasis on chargers for electric vehicles;
- Select a proper topology for the DC-DC converter;
- Design, simulate and construct an advantageous DC-DC converter for EV charging application.

This research focusses on designing a single power converter with an output power of the specified 10 kW. No survey is done on how many of these converters can be put in parallel and how the load among those is most efficiently spread. Furthermore is this research only about designing a converter for the given purpose. No study is done on any communication protocols or interaction with either the car or the grid with respect to required power transfer.

1.4.1. Extraordinary circumstances

During the second half of this project society suffered from the *Coronavirus disease 2019*. Therefore, the actual construction of the prototype did not happen, as well as the phases of testing the converter and measuring the performance. These parts are considered as future work.

1.5. Overview

The introduction, background and requirements are given here. Next, an overview of different DC-DC converter topologies is given in Chapter 2, in which at the end a converter topology is chosen for further investigation. In Chapter 3 the chosen converter is discussed more in depth, where mathematical equations are derived and limits for operation are given. Chapter 4 introduces other operation techniques for the converter, in order to increase the efficiency. In this part also equations are derived which describe the operation of the converter. In Chapter 5 the design of the converter will start, in this chapter by choosing the switches and investigating their losses. Chapter 6 will continue with the design of the magnetic components, consisting of the inductor and transformer. Chapter 7 will discuss some other small parts of the design and ends with a designed Printed Circuit Board (PCB).

2

DC-DC converter topologies

In this chapter, different DC-DC converter topologies will be reviewed. All have been classified into converters with and without isolation. In the requirements (Section 1.3) is given that the converter should provide galvanic isolation, therefore the focus is on the converters with isolation. The types of converters discussed without isolation provide a basis, which might be helpful for understanding some of the isolated converters (which are derived from their non-isolated converters). At the end of the chapter a topology is chosen which will fit best to the needs specified.

Contents in this chapter

2.1. Non-isolated converters

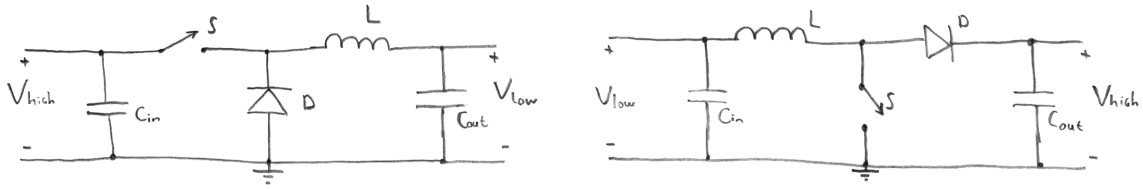
The first type of DC-DC converters that is being discussed is the type of non-isolated converters. Advantages of these topologies is that they require no transformer, which saves cost, decreases the volume and weight of the converter and also reduces the losses, since no transformer is lossless.

2.1.1. Buck and boost converter

The buck and boost converter are two basic types of DC switched mode converters with a very low number of elements. Both converters are formed around a switch, diode and an energy storage component which is an inductor. The buck converter, shown in Figure 2.1a is able to step down the voltage, and the boost converter, shown in Figure 2.1b is able to step up the voltage.

The voltage ratio between input (high voltage side) and output (low voltage side) is simply controlled by only the duty cycle D. For continuous conduction mode the voltage ratio of the buck converter is given in Equation (2.1) below:

$$\frac{V_{out}}{V_{in}} = \frac{V_{low}}{V_{high}} = D \tag{2.1}$$



(a) Step-down DC-DC (buck) converter

(b) Step-up DC-DC (boost) converter

Figure 2.1: Basic types of DC switched mode converters

For the boost converter the output voltage can also be controlled by only varying the duty cycle D. The ratio between input (low voltage side) and output (high voltage side) is given in Equation (2.2).

$$\frac{V_{out}}{V_{in}} = \frac{V_{high}}{V_{low}} = \frac{1}{1-D} \tag{2.2}$$

Both of these converters can also be operated in discontinuous conduction mode, which means that the current flowing through the energy storage element (the inductor) comes to zero every period. In this way the switch turns on at zero inductor current, which reduces the switching losses and hence, a higher efficiency can be achieved. The downside of operating in discontinuous conduction mode compared to the continuous conduction mode is the higher peak value of the inductor current, when the same power has to be transferred.

Both the buck and boost converter only allow a unidirectional power flow, either from high voltage side to low voltage side or vice versa. In order to obtain a bidirectional power flow, the buck and boost converter can be combined. The equivalent circuit is given in Figure 2.2. It can be noticed that this converter works as

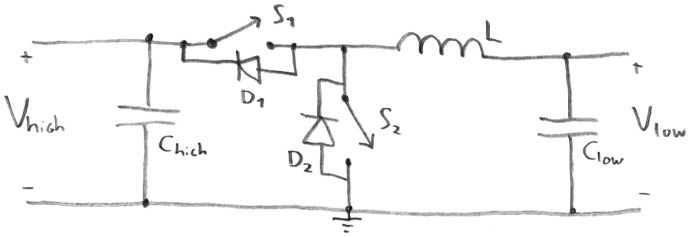


Figure 2.2: The buck and boost converter combined to obtain bidirectional power flow

a buck converter from high voltage to low voltage, while operating as a boost converter in reverse direction.

2.1.2. Buck-boost converter

The buck-boost converter is also a basic DC switched mode converter. As opposed to the buck and boost converter, this buck-boost converter can step-up, as well as step-down the voltage level. The circuit of the buck-boost converter is shown in Figure 2.3. Then a closer look is taken to the circuit, it can be seen that

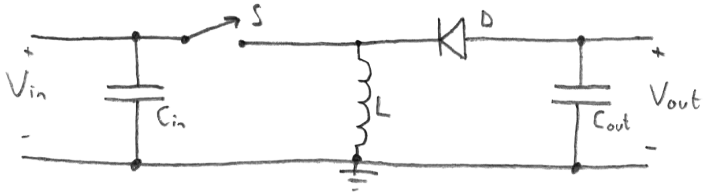


Figure 2.3: The buck-boost converter

there is no direct path for power transfer from input to output. This means that every period all energy that has to be transferred must be stored in the inductor. This differs from the buck and boost converter, which had always a path for power transfer from input to output. The ratio from input to output voltage of the buck-boost converter is given in Equation (2.3).

$$\frac{V_{out}}{V_{in}} = -\frac{D}{1-D} \tag{2.3}$$

Hence there is a minus sign in front of the equations, which means that the output voltage of the buck-boost is negative. This negative output polarity may be a desired feature with respect to the common terminal of the input voltage.

In order to make the buck-boost converter a bidirectional converter, the same method is applied as when transforming the unidirectional buck and boost converter to a bidirectional version. The circuit of the bidirectional buck-boost converter is given in Figure 2.4.

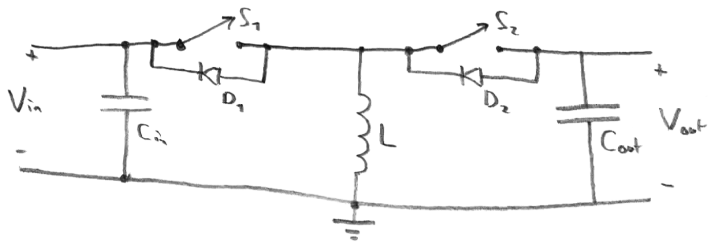


Figure 2.4: The bidirectional buck-boost converter

2.1.3. Other topologies

There exist of course a lot of other non-isolated DC-DC converters, including a Cúk converter, Zepic, Zeta and all kinds of resonant converters, of which a lot are discussed in [8, 9]. Since one of the requirements is to find an isolated converter, they will not be discussed in depth here. The buck and boost and buck-boost converters discussed previously were investigated to get a better understanding and isolated topologies are derived from these non-isolated versions.

2.2. Isolated converters

Next, a number of different DC-DC converter topologies is discussed with galvanic isolation. For this isolation, a transformer has to be added to the converter which will increase the volume, weight and costs of the converter, as well as introduces some extra losses. However, the galvanic isolation is often a requirement for safety. Furthermore, the transformer allows the converter to step-up or step-down the voltage at much higher ratings compared to converters without a transformer.

2.2.1. Flyback converter

The first converter discussed is the flyback converter, which is derived from a buck-boost converter by replacing the inductor with a transformer. The circuit of the flyback converter is given in Figure 2.5. Because of

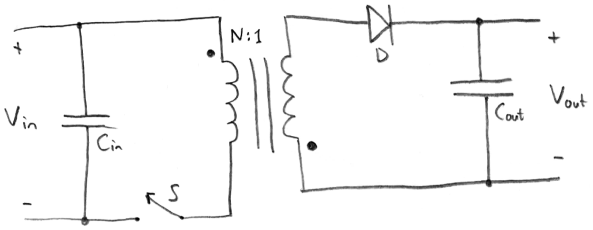


Figure 2.5: The flyback converter

the transformer in this converter, it is possible to obtain either a positive or a negative output voltage. Also, the turns ratio of the transformer enables a larger step in voltage ratio. The voltage ratio between input and output is given by Equation (2.4), where a minus can be added if the secondary coil is flipped.

$$\frac{V_{out}}{V_{in}} = \frac{1}{N}\frac{D}{1-D} \tag{2.4}$$

Again, this unidirectional converter can also be transformed to a bidirectional converter [10]. Using the same procedure as before, the circuit of the bidirectional flyback converter is obtained in Figure 2.6. With this type of converter, the transformer design procedure needs to be taken into account and a voltage clamp

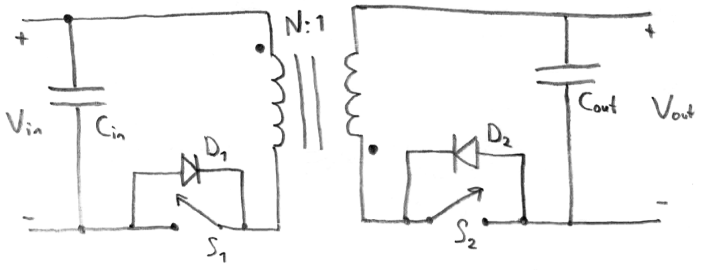


Figure 2.6: The bidirectional flyback converter

snubber is required to suppress the leakage current of the flyback transformer [9]. An advantage of the flyback converter is the low number of components required. Disadvantages can be found in the relative high voltage stresses on the switches and the flyback converter also has a unidirectional core excitation, which means that only half of the BH-curve is used. However, when two switches are used at a side of the transformer, as well as two diodes, switches with a lower voltage rating can be selected and the dissipative snubber is not needed [8]. A bidirectional flyback converter with active clamping can also be found in [11]. Flyback converters are mostly found in lower power applications.

2.2.2. Forward converter

The next converter being discussed is the forward converter. Just as with the flyback converter, the bidirectional version is derived from the circuit depicted in Figure 2.7. This converter is derived from the buck

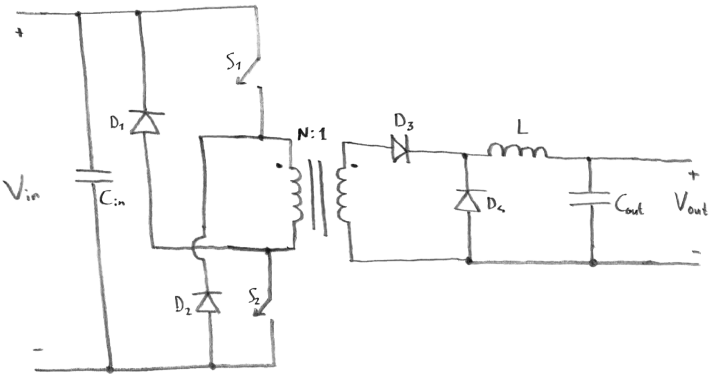


Figure 2.7: The forward converter

converter, as can be seen on the right side with the placements of the inductor, diode and capacitor. The relation between input and output voltage is also very similar compared to the one of the buck converter and is given in Equation (2.5).

$$\frac{V_{out}}{V_{in}} = ND \tag{2.5}$$

This forward converter has two switches with are turned on and off simultaneously, therefore the voltage rating is half of that in a single switch topology, this also eliminated the need for a separate demagnetizing winding or snubber [8].

Since there is a need for a bidirectional converter rather than a unidirectional one, some components are added and the circuit is modified. The circuit of this bidirectional forward converter is given in Figure 2.8 [12]. Besides this version of the bidirectional forward converter, also other versions are mentioned in literature, which includes a resonant network where the leakage inductance of the transformer is used to resonate with an added capacitor [9]. Furthermore versions exist which are a combination of multiple topologies, for example a forward converter combined with a flyback converter [13, 14]. On the primary side of the transformer one of the topologies is used, with the other on the secondary side. An advantage of the forward converter is the continuous output current due to the inductor. However, the forward converter is limited to low and medium power applications [15].

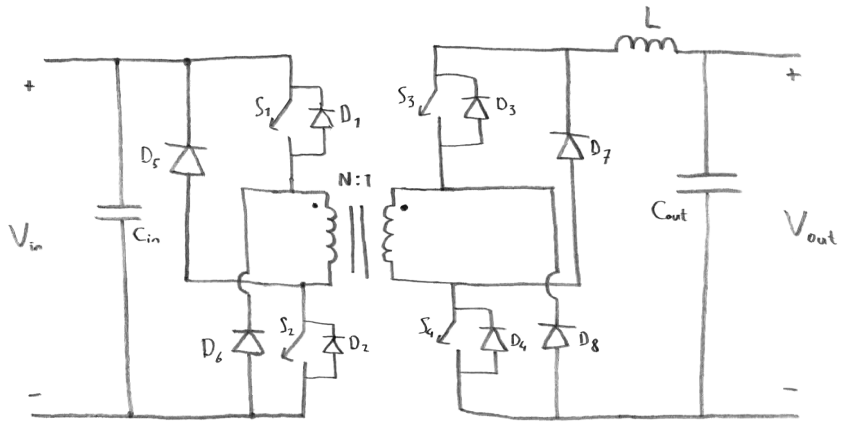


Figure 2.8: The bidirectional forward converter

2.2.3. Push-Pull converter

The next converter that will be discussed shortly is the push-pull converter. Equal to converters discussed before, the regular unidirectional topology is once again modified to a bidirectional topology [16]. This converter uses a transformer with a centre tap and the circuit is shown in Figure 2.9. The relation between input

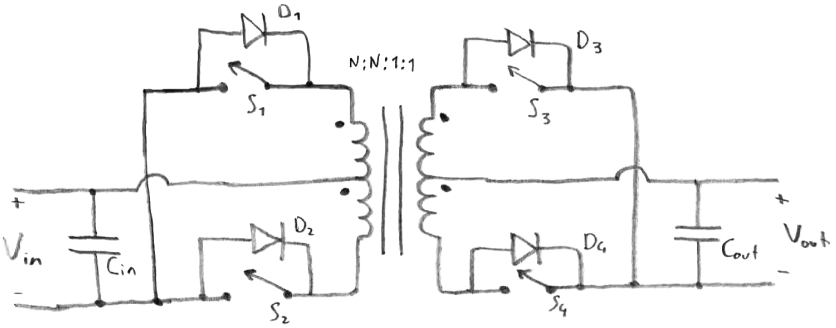


Figure 2.9: The bidirectional push-pull converter

and output voltage of the push pull-converter is equal to the one of the forward converter given in Equation (2.5), where it can be noted that also the push-pull converter is derived from the buck converter. Note that in the figure given also an inductor can be added before the capacitor. An advantage of this converter is also the continuous output current and it has a medium power capability [9]. However, if a three phase transformer is used, high power can be transferred. A disadvantage is the required transformer, which should have multiple windings.

2.2.4. Half bridge converter

A dual bridge converter with two actively switched bridges on both sides of the (high frequency) transformer. Both bridges have a 50 % duty cycle and the phase shift between these two square waves determines the power transfer. The leakage inductance L has a voltage difference across it of the input and output voltage and is used to transfer the power. The circuit of a half bridge converter is given in Figure 2.10. The given half bridge converter has just like the flyback converter only a unipolar flux swing on the transformer, which results in inefficient use of the magnetic core. Also, this type of converter needs large input and output capacitors to lower the voltage ripple on both sides and the switches have a high voltage stress. Advantages of this half bridge converter are the wide operating voltage range, low number of switches and the immunity to the parasitic inductance [11]. Also the current waveform in the inductor reduces the RMS current in the switches and transformer.

Besides this first type of half bridge converter, the magnetic core of the transformer can be used more efficiently by a bipolar flux operation. When the number of switches is not increased, a midway voltage point can be created by making use of capacitors. Such a half bridge converter with capacitors is given in Figure 2.11. Now the magnetic core is much more effectively utilised compared to the previous types of converters, while

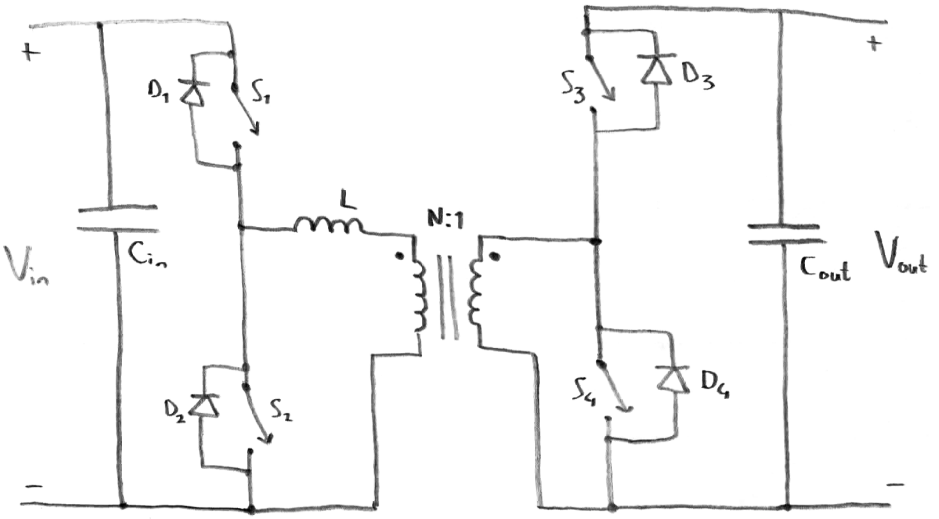


Figure 2.10: The half bridge converter

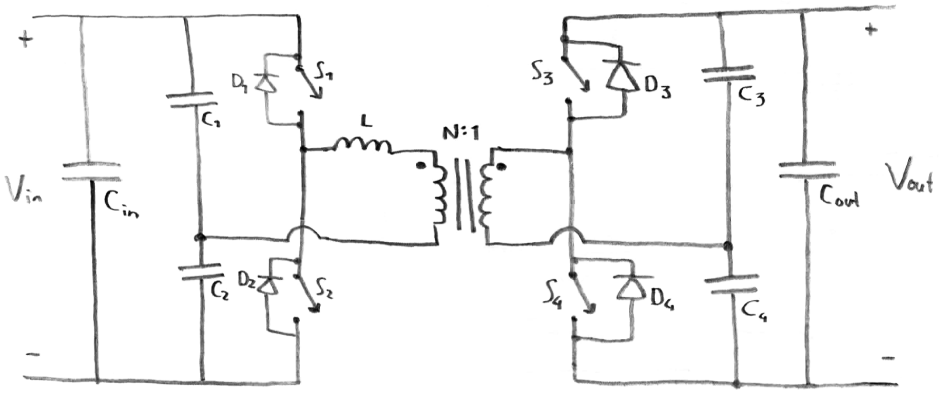


Figure 2.11: The half bridge converter with capacitors

still keeping the number of switches low. However, a disadvantage to this type of converter is that the capacitors used to split the voltage (C_1 to C_4) have to handle the full load current. Also sensing can be difficult and a complex controller is needed to strictly regulate the magnitude and period of the current in the transformer.

The use of these half bridge converters is limited to low or at most medium power applications.

2.2.5. Dual active bridge

Instead of using two times a half bridge as in the previous converters, also two full bridges can be used. This dual active bridge converter has a similar way of operating, but because of the extra switches, in total three voltage points can be set on each side ($V_{in}, 0, -V_{in}$) compared to only two voltage levels for the half bridge converter ($V_{in}, 0$). This allows for more flexibility with respect to the modulation techniques. The circuit of a full bridge dual active bridge is given in Figure 2.12. The leakage inductance of the transformer (eventually in series with an extra inductor in series) is used to transfer power, and the phase shift between the two voltage sources determines the amount of power. Advantages of this converter are the low number of components used for having two full bridges, soft switching is possible without adding auxiliary components, multiple modulation techniques possible [9, 17] and the bipolar flux swing in the transformer allows for a higher power capability compared to the half bridge topologies. A disadvantage of this converter is that large input and output capacitors are needed for a low ripple at both sides. Furthermore, the simple phase shift modulation method can lose soft switching for light loads and with this modulation method the conduction loss is high due to circulating power [11]. There are more sophisticated current modulation techniques available which can improve the soft-switching range and can reduce the circulating reactive power, this will require a more

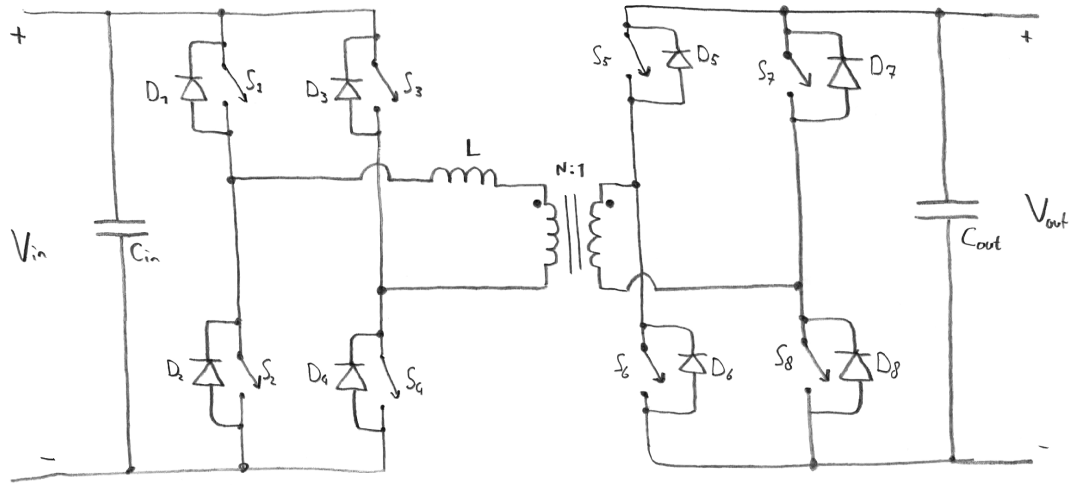


Figure 2.12: The dual active bridge converter with two full bridges

complex controller compared to other methods.

2.2.6. Three phase dual active bridge

The dual active bridge discussed above can be extended with an extra leg on each side and a three phase transformer [18, 19] to obtain the converter shown in Figure 2.13. This type of converter needs the largest

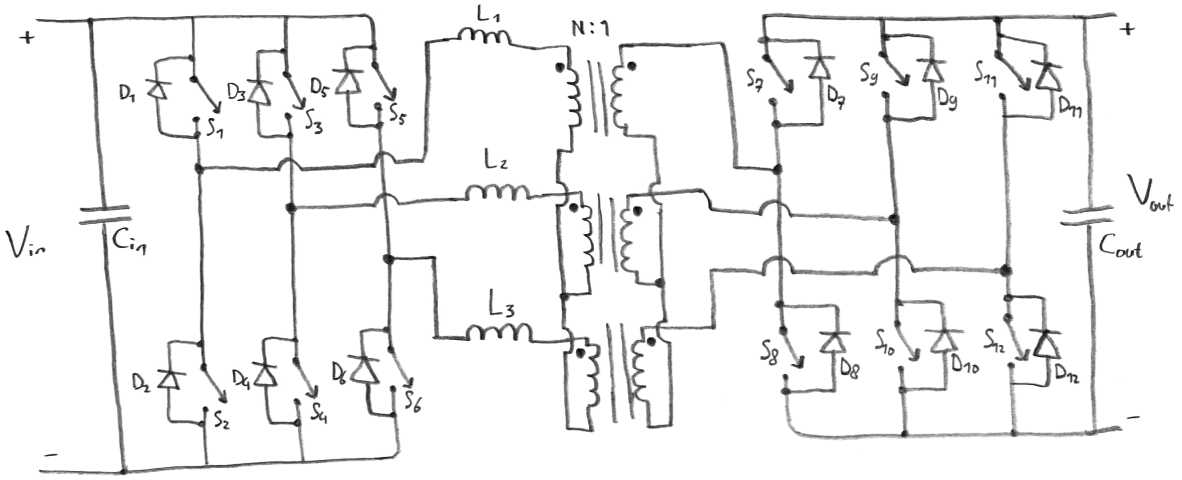


Figure 2.13: The three phase dual active bridge converter

number of switches (12 in total) of all discussed converters and also needs a three phase transformer. This leads both to an increased volume and weight of the total converter compared to the single phase dual active bridge. However, the three phase dual active bridge (DAB) has quite a few advantages. For the same amount of transferable power, the transformer VA ratings are lower, as well as the ratings of the switches and the current ripple is lower. This makes the three phase DAB suitable for high power applications. A difficulty with this type of converter is to achieve the same required leakage inductance in all inductors (L_1 to L_3), therefore this will lead to an extra inductor in series with the leakage inductor. Another disadvantage is that this type of converter only allowed the conventional modulation technique, which can lead to high losses if the converter is operated in wide voltage and power ratings [20, 21].

2.2.7. Dual active bridge with resonant tank

Another solution to the decreased soft switching range and decreased efficiency when voltages are not matched on the dual active bridge under single phase shift, it the use of a resonant tank in between. Due to its advan-

tages of operation, the converter can be operated under a higher frequency and efficiency, but additional resonant components also bring extra size and costs [17]. A so called *LLC*-type resonant topology is given in Figure 2.15, where *LLC* means the resonant tank consists of two inductors (L) and one capacitor (C). Com-

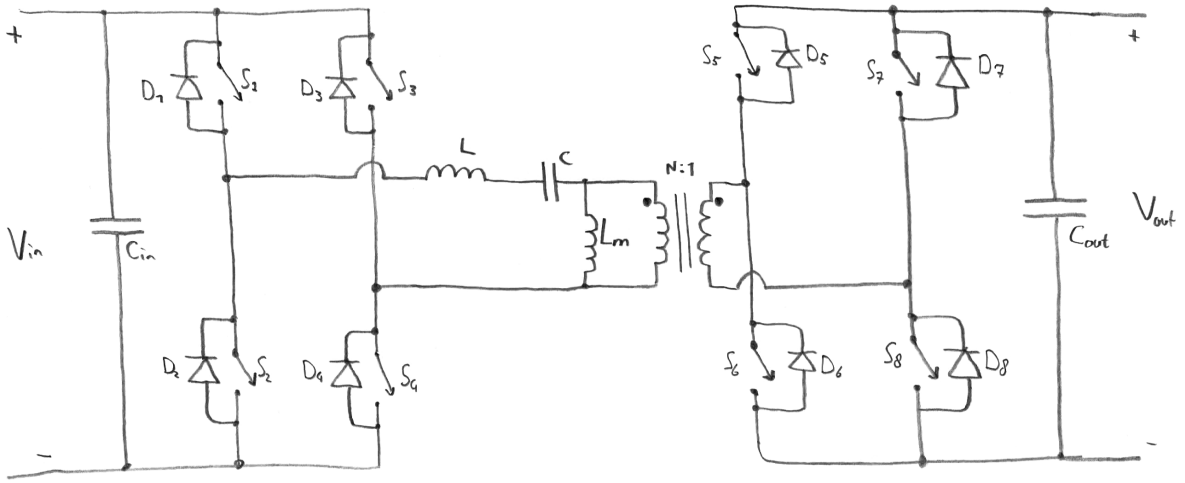


Figure 2.14: Dual active bridge converter with a LLC-resonant tank

pared to the dual active bridge converter, even at light load zero voltage switching (ZVS) is possible in forward operating mode [22]. Furthermore a slightly higher average efficiency can be achieved, but a larger value of the required magnetic storage capability occurs. Also, the electric energy stored in the resonance capacitor forces the transformer current to change during the freewheeling time interval, which causes the RMS current to increase. The LLC converter is more suitable if a variable switching frequency is permitted [21]. Also, in reverse mode (transferring energy in the opposite direction, for example from the vehicle to the grid) when the operating frequency is deviates from the resonant frequency high losses can occur [23].

In order to overcome the problem of a reduced ZVS range in backward or reverse mode of operation, the converter can be made symmetrical, by adding another capacitor [22, 23]. The circuit of this *CLLC*-type resonant converter is given in Figure 2.15, where *CLLC* means that the resonant tank consists here of two capacitors as well as two inductors. Both good performance can be expected in both forward and reverse mode of

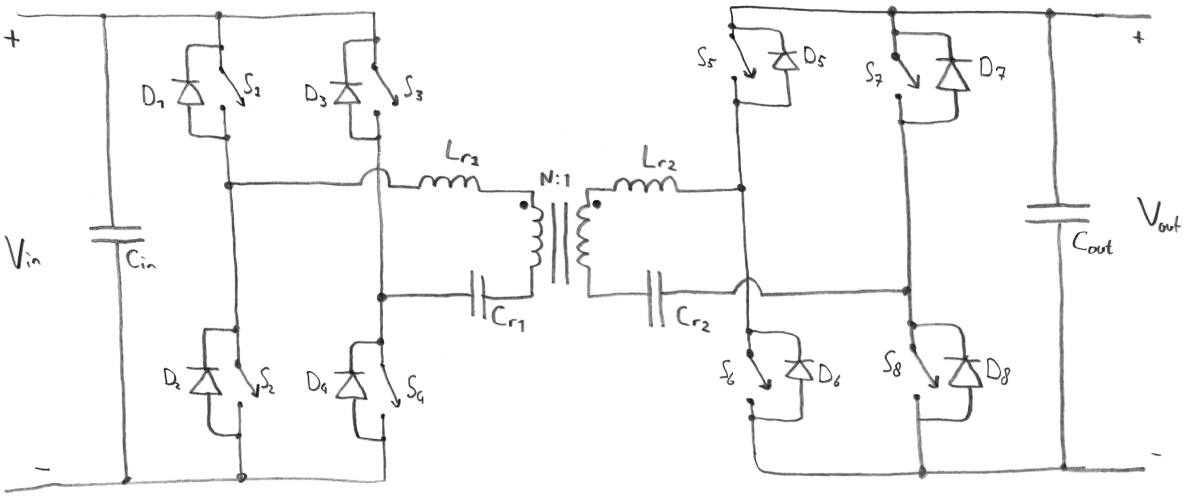


Figure 2.15: Dual active bridge converter with a CLLC-resonant tank

operation [23]. However, in the frequency regions below the resonant frequency and in increased load conditions, the converter can have difficulties in getting the required voltage gain. This is because the zero voltage switching can be lost when the switching frequency increases [24]. Compared to the dual active bridge, this *CLLC*-type converter has a wider soft switching range. Disadvantages are the slow transition from forward

to reverse mode of operation [17] and the extra resonant components, which will increase cost, volume and weight of the total converter. Furthermore, the power control is performed by frequency modulation.

2.3. Two-stage topologies

The isolated topologies discussed in Section 2.2 are operated most efficiently if the input to output ratio matches the turns ratio of the transformer. In a two stage topology, an isolated topology is used with a fixed input to output ratio as first stage, preferable equal to the turns ratio of the transformer and then an additional buck and/ or boost converter is added [21]. The first converter provides the required galvanic isolation, while the second one sets the correct output voltage. This means however, that the second stage must be highly efficient in order to obtain a higher overall efficiency compared to a single isolated converter topology. Furthermore will such a converter require a larger volume and the total weight will increase.

2.4. Promising topologies

The above mentioned bidirectional power converters are compared based on all kinds of aspects, including expected efficiency, complexity, component count (including volume and weight) and power delivery. The following two topologies are selected as most promising regarding the requirements given in Section 1.3:

- Dual active bridge (full bridge, Section 2.2.5),
- Two stage dual active bridge with resonant tank (Section 2.2.7) followed by a combined buck and boost converter (Section 2.1.1).

It can in general be said that the higher the number of switches in a bridge converter, the lower the stresses per switch and thus the higher the power capability of the converter. The dual active bridge is chosen because of the simplicity of the converter and the minimal component count (relatively small size and low weight). The leakage inductance of the transformer can eventually be used to save even more space. This topology is chosen above the half bridge solutions, because of the required power the converter has to deliver. The three phase version was another good candidate for the high power specification, however, since this converter can only be used with single phase shift modulation, the expected losses over the wide output voltage range will increase. The single phase dual active bridge can be operated with different modulation techniques to overcome this problem.

The second chosen promising topology is a two stage version, where a resonant dual active bridge is chosen as first stage, because of the high expected efficiency and galvanic isolation. Not a single dual active bridge with resonant tank has been chosen, because of the variable frequency operation and moving outside a specific frequency range will increase the losses. Therefore the frequency of this converter will be fixed and the voltage transfer ratio will be set close to the turns ratio. A secondary high efficiency combined buck and boost converter will be used to set the correct voltage level.

Overall, the first solution of the dual active bridge will be further investigated. The slightly higher expected efficiency does not outweigh the more complex circuit (far less components compared to the second two-stage proposal) and the challenges of optimising two actual converters to the highest possible efficiency. Especially the design of the second stage combined buck and boost converter. In order to come close to the efficiencies of this two stage solution, the single stage dual active bridge will probably need advanced modulation techniques.

3

Simple dual active bridge

In this chapter the basic working principle of the dual active bridge will be discussed with the standard simple phase shift modulation in steady state. Firstly, the equivalent circuit will be given, whereafter waveforms will be shown. Then, equations will be derived for the power transfer, phase angle and regions for zero voltage switching will be given. Finally conclusions will be drawn based on the results and solutions for a wider zero voltage switching region will be given.

Contents in this chapter

3.1. Equivalent circuit

The analysis of the dual active bridge (DAB) is started by drawing the circuit, which is given in Figure 3.1. In this circuit, the combination of a switch (S_x), diode (D_x) and capacitor (C_x) is denoted by a single Q_x.

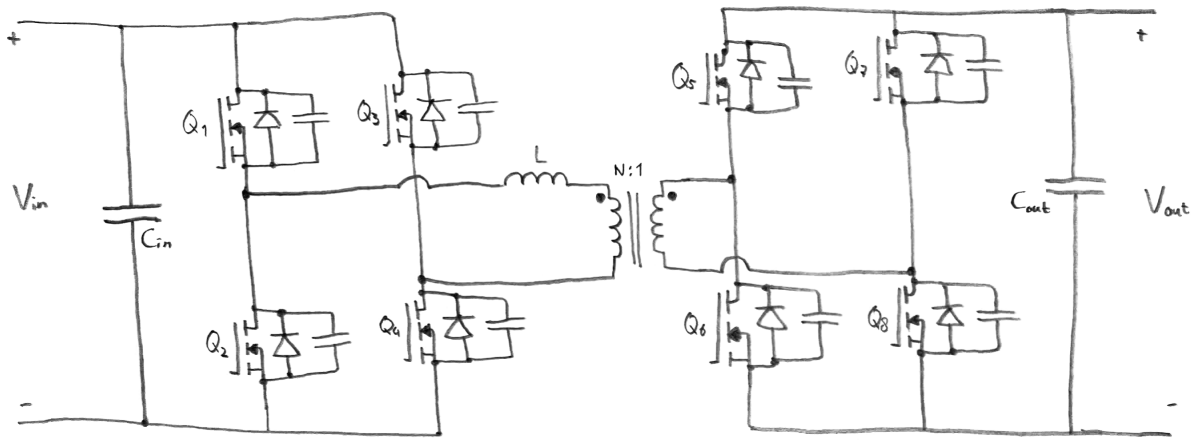


Figure 3.1: The circuit of the dual active bridge converter

The parallel capacitor can be either the parasitic drain-source capacitance or an auxiliary capacitor, added to reduce switching losses by create zero switching switching in combination with a small dead time [25].

In order to simplify the coming analysis, the circuit can be simplified and redrawn to an equivalent circuit consisting of two square wave voltage sources and a single inductor. This equivalent circuit is given in Figure 3.2. The output voltage is now changed to $n \cdot V_{out}$ due to the transformer turns ratio. The full bridges on

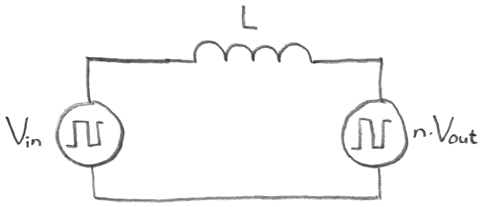
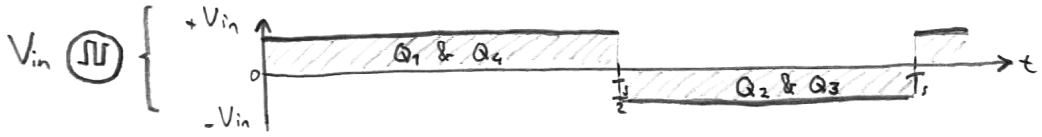


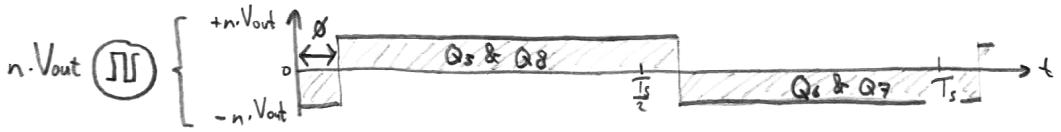
Figure 3.2: The equivalent circuit of the dual active bridge converter

both sides can be transformed to a square wave voltage source, since the voltage V_{in} on the input is either directly supplied to the primary side of the bridge (switches 1 and 4 conducting) or flipped $-V_{in}$ supplied to the primary side of the bridge (switches 2 and 3 conducting). The same holds for the secondary side of the converter.

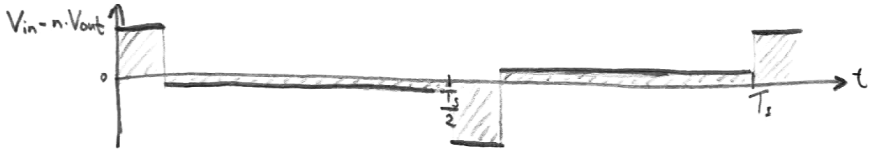
A graphical representation is given in Figure 3.3. Here the phase shift is denoted by ϕ and the input voltage V_{in} is set to a higher value compared to the output voltage $n \cdot V_{out}$, taken the transformer turns ratio into account. The voltage across both square wave voltage sources given as a function of time (Figure 3.3a



(a) Voltage of the primary square wave voltage source



(b) Voltage of the secondary square wave voltage source



(c) Voltage across the inductor

Figure 3.3: The voltages in the equivalent circuit of the DAB converter with corresponding conducting switches

and Figure 3.3b), as well as the voltage across the inductor (Figure 3.3c), which is the difference between these two voltage sources as given by Equation (3.1).

$$v_L = V_{in} - n \cdot V_{out} \tag{3.1}$$

Furthermore, for the ease of analysis in this chapter a lossless circuit is assumed, where Equation (3.2) holds.

$$P_{in} = P_{out} \tag{3.2}$$

3.2. Inductor current waveform

Now the voltages in the equivalent circuit of the DAB converter are known, the currents will be investigated. Due to the simplifications the model has reduces to a circuit with only an inductor, on which a varying voltage is applied. The current through an inductor is given by Equation (3.3).

$$i_L(t) = i_L(t_0) + \frac{1}{L}\int_{t_0}^{t_1} V_L dt \tag{3.3}$$

The waveform of the inductor current is given in Figure 3.4. Here the voltage source on the left side V_{in} has a

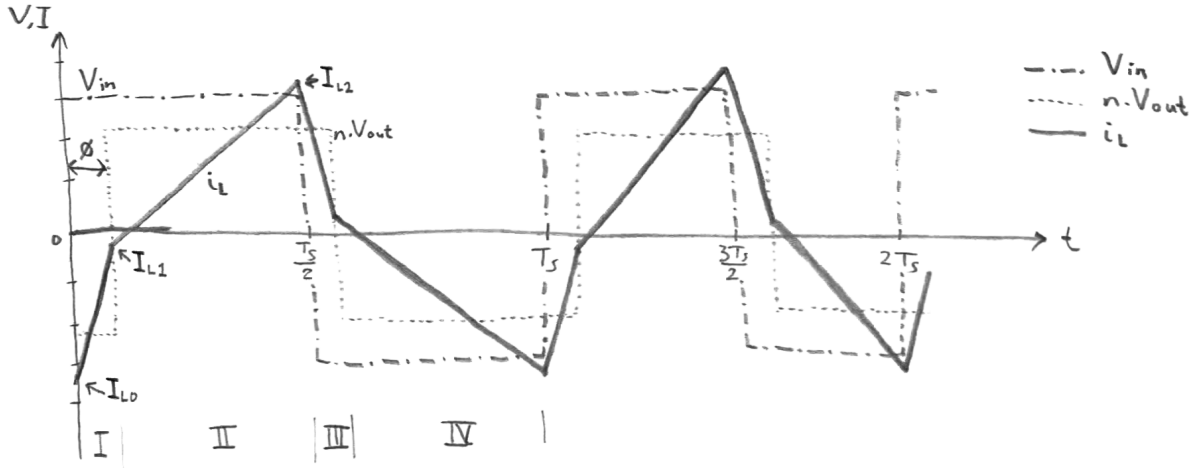


Figure 3.4: The inductor current waveform if $V_{in} > n \cdot V_{out}$

larger value than the one on the right side $n \cdot V_{out}$. When the first part of the current waveform is inspected (part 1, also specified on the bottom of the figure in Roman numbers), making use of Equation (3.3) results in Equation (3.4). In this equation I_{L0} is the inductor current at $t = t_0$, also shown in the figure.

$$i_{L,1}(t) = I_{L0} + \frac{V_{in} + n \cdot V_{out}}{L} t \tag{3.4}$$

Following the same procedure, the current in the second part can be derived. Starting with Equation (3.5), where I_{L1} equals the inductor current at $t = T_\phi$, with ϕ as phase shift.

$$i_{L,2}(t) = I_{L1} + \frac{V_{in} - n \cdot V_{out}}{L} (t - T_\phi) \tag{3.5}$$

Which can also be written using I_{L0} instead of I_{L1} as given in Equation (3.6).

$$i_{L,2}(t) = I_{L0} + \frac{n \cdot V_{out}}{L} 2T_\phi + \frac{V_{in} - n \cdot V_{out}}{L} t \tag{3.6}$$

Due to symmetry, the current I_{L0} should be equal to the current $-I_{L2}$. Using this property in combination with Equation (3.4) and Equation (3.6) results in Equation (3.7).

$$I_{L0} = \frac{(n \cdot V_{out} - V_{in})\pi - 2n \cdot V_{out} \cdot \phi}{4\pi L f_s} \tag{3.7}$$

In this equation the relation of Equation (3.8) is used. The phase shift is specified between $-\pi$ and π.

$$T_\phi = \frac{\phi}{2\pi f_s} \tag{3.8}$$

The values of I_{L1} and I_{L2} can be either positive or negative, depending on the voltage levels on both sides and the phase shift, more on this later in Section 3.5. The current waveforms in part 3 and 4 can be derived in a similar way due to the before mentioned symmetry. This can be done by flipping the signs of the initial current as well as the slope of both the waveforms in part 1 (Equation (3.4)) and part 2 (Equation (3.6)).

Using Equation (3.4), Equation (3.7) and Equation (3.8), the current I_{L1} can be derived at $t = T_\phi$. This current is given in Equation (3.9):

$$I_{L1} = \frac{V_{in}}{2\pi L f_s} \left(\phi - \frac{\pi}{2}\right) + \frac{n \cdot V_{out}}{4 L f_s} \tag{3.9}$$

Following the same steps for the current I_{L2} it can be verified that indeed $I_{L2} = -I_{L0}$.

In the case that the voltage of the right hand square wave voltage source ($n \cdot V_{out}$) is larger than the voltage on the left hand side (V_{in}), the current waveform will look like the one depicted in Figure 3.5. Note that the equations of the current waveforms derived previously do not change.

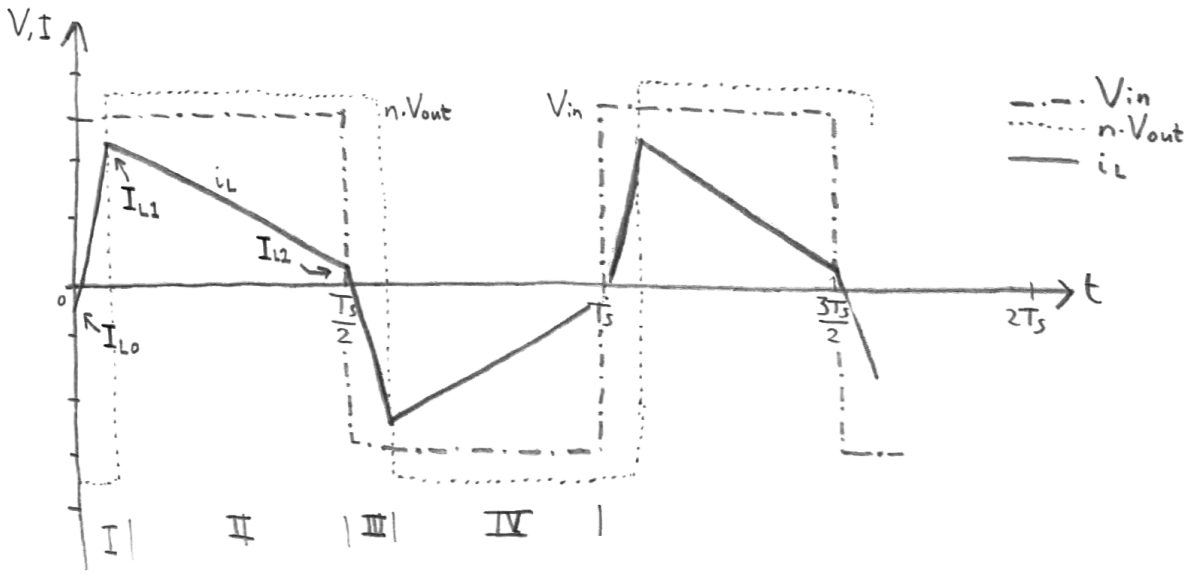


Figure 3.5: The inductor current waveform if $V_{in} < n \cdot V_{out}$

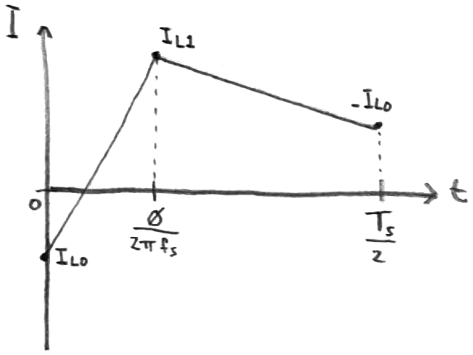


Figure 3.6: Current waveform to calculate the RMS

In order to calculate the RMS current, one specific part of the current waveform is considered. This part of the waveform is given in Figure 3.6. As can be seen in the figure, the current I_{L2} is set to $-I_{L0}$. To obtain the RMS current of this waveform, both integrals of Equation (3.10) can be worked out.

$$I_{RMS} = \sqrt{2f_s\left(\int_0^{\frac{\phi}{2\pi f_s}} i_{L,1}^2(t)dt + \int_{\frac{\phi}{2\pi f_s}}^{\frac{\pi}{2\pi f_s}} i_{L,2}^2(t)dt\right)} \tag{3.10}$$

In this equation $i_{L,1}(t)$ and $i_{L,2}(t)$ refer to Equation (3.4) and Equation (3.6) respectively. Simplifying this equation results in Equation (3.11) for the current in the inductor.

$$I_{RMS} = \sqrt{\frac{1}{3}\left(I_{L1}^2 + I_{L0}^2 - I_{L1}I_{L0}\left(1 - 2\frac{\phi}{\pi}\right)\right)} \tag{3.11}$$

The primary current of the transformer is equal to the inductor current and the secondary current of the transformer differs a factor n, which is the turns ratio of the (for now assumed ideal) transformer.

Based on the shape of this current waveform, in literature [11, 21] this modulation method is also known as *rectangular* mode of operation. From now on this will be used when referring to this modulation method.

3.3. Transferred power

It is known that power is the product of voltage and current. Using this property in combination with the equivalent circuit, Equation (3.12) should be solved.

$$P = \frac{1}{T_s}\int_0^{T_s} p(t)dt = \frac{1}{T_s}\int_0^{T_s} v(t)\cdot i(t)dt \tag{3.12}$$

Due to symmetry, the first part and second part of one period transfer the same amount of power. Also, if half of a period is chosen where the voltage is constant, it can be taken out of the integral. Choosing the first half period, the voltage at the input is constant and equal to V_{in}, while the current through the inductor is the only one varying. This will lead to Equation (3.13).

$$P = \frac{2V_{in}}{T_s}\int_0^{\frac{T_s}{2}} i_L(t)dt \tag{3.13}$$

Filling in the equations for the currents in both different parts of the first half period and the above equation can be rewritten as in Equation (3.14).

$$P = \frac{2V_{in}}{T_s}\left(\int_0^{T_\phi} i_{L,1}(t)dt + \int_{T_\phi}^{\frac{T_s}{2}} i_{L,2}(t)dt\right) \tag{3.14}$$

After integrating, writing the times as a function of the switching frequency f_s and simplifying one will end up with Equation (3.15).

$$P = \frac{n\cdot V_{out}V_{in}\phi(\pi-\phi)}{2\pi^2 f_s L} \tag{3.15}$$

This equation will give the correct power transfer for a positive phase shift between 0 and π. However, the dual active bridge converter can also operate in reverse mode of operation. In this way power is transferred from the output (right side) to the input (left side). This will happen for a negative phase shift between $-\pi$ and 0. Therefore, Equation (3.15) can be modified to a more universal form. The final equation for the power transfer of the DAB converter in rectangular mode is given in Equation (3.16).

$$P = \frac{n\cdot V_{out}V_{in}\phi(\pi-|\phi|)}{2\pi^2 f_s L} \tag{3.16}$$

This equation will hold for the complete range of the phase shift, which is between $-\pi$ and π.

As can be seen in Equation (3.16), the transferred power depends on several different parameters. The input and output voltage are set by the grid and load respectively, while the turns ratio of the transformer and the inductance of the inductor are often fixed values. If the switching frequency is then set to be a fixed value, the power transfer is controlled by only varying the phase shift between the primary and secondary bridge (ϕ). Therefore, the maximum to be transferred power can be calculated. Given Equation (3.16), the maximum power transfer will occur if $\phi = \pm\frac{\pi}{2}$. The resulting maximum power transfer for the DAB converter in rectangular mode is then as in Equation (3.17).

$$|P_{max}| = \frac{n\cdot V_{out}V_{in}}{8 f_s L} \tag{3.17}$$

In order to control the level of power being transferred, the phase shift can be varied. Starting with Equation (3.16), the equation for the phase shift will be written as a function of the to be transferred power. The phase shift required for a given transfer of power is given in Equation (3.18), for $|P| \leq |P_{max}|$.

$$\phi = \frac{\pi}{2}\cdot\left(1-\sqrt{1-\frac{8 f_s L\cdot|P|}{n\cdot V_{out}V_{in}}}\right)\cdot\text{sign}(P) \tag{3.18}$$

3.4. Simulations

In order to verify the equations derived in the previous sections, the circuit is built and simulated. This is done with the aid of the software called *Gecko Circuits*. The equivalent circuit of Figure 3.2 is built first as well as the corresponding control logic. With the electrical circuit in blue and the control logic below in green,

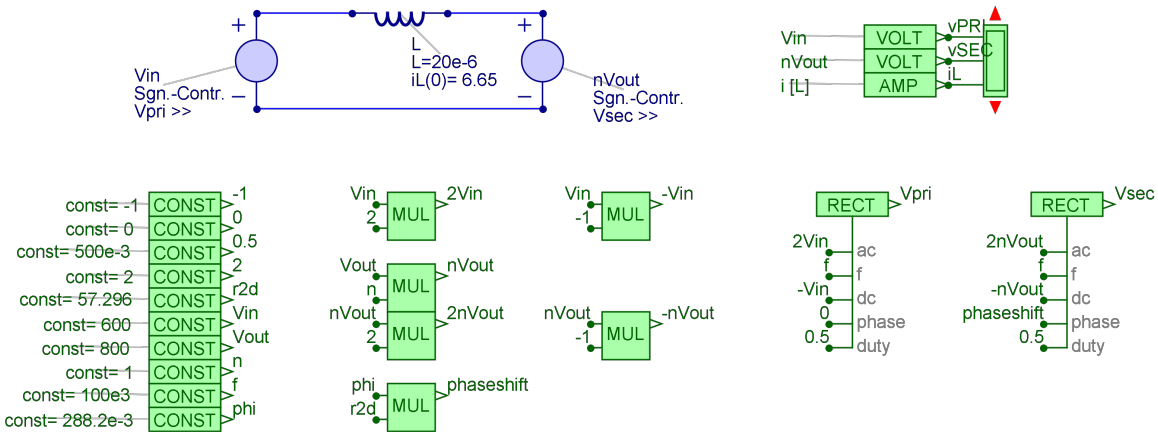


Figure 3.7: The electrical circuit and control logic of the DAB (rectangular mode) in Gecko Circuits

Table 3.1: Parameters for the simulation of the equivalent DAB in rectangular mode

Parameter	**Value**
Input voltage V_{in}	600 V
Output voltage V_{out}	800 V
Transformer turns ratio $n:1$	1
Switching frequency f_s	100 kHz
Inductance L	20 µH
Transferred power P_{out}	10.0 kW

a screenshot of the simulated circuit is given in Figure 3.7. For clarity purposes are all lines between the control blocks removed. As also can be seen in the figure, the parameters are set just as shown in Table 3.1. Making use of Equation (3.18), the corresponding phase shift can be calculated, which is given the parameters in Table 3.1 a phase shift of 0.2882. If the simulation is executed over two periods, the resulting waveforms are given in Figure 3.8. In the simulation results it can be seen that the voltage levels are correct, as well as their shape. This can also be said about the current. When a look is taken to the phase shift between the two voltage waveforms, this time of 0.46 µs is indeed equal to the time calculated with Equation (3.8) and a phase shift of 0.2882. In the software also the power transfer is calculated, which is equal to the set 10.0 kW. The two calculated current points of I_{L0} and I_{L1} do also match the simulation results, which are 6.6 A and 38.8 A respectively. Lastly, the calculated RMS current of 21.1 A is also equal to the RMS current obtained from the simulation.

If the phase angle is inverted ($\phi = -0.2882$), it can be noted in the simulation that the current waveform will flip along the x-axis while the voltage waveforms remain the same. As expected, the 10 kW of power transfer is now in the opposite direction, which follows both from the derived equations as well as the simulation results.

Instead of using pure rectangular voltage sources, the dual active bridge can also be simulated with eight MOSFETs. When simulating in this way, the simulation program *Gecko Circuits* used non-ideal MOSFETs with among others a finite turn on and turn off resistance. Furthermore the control circuit in green is slightly more complex, since each MOSFET requires a gate signal. The complete circuit can be seen in Appendix B. The results obtained with this circuit were very close to the ones obtained with the equivalent circuit with two rectangular voltage sources. Therefore, discussing this results will not lead to a better insight.

All in all it can be concluded that the equations for the dual active bridge converter with rectangular current modulation are derived in a correct way and the converter works as expected.

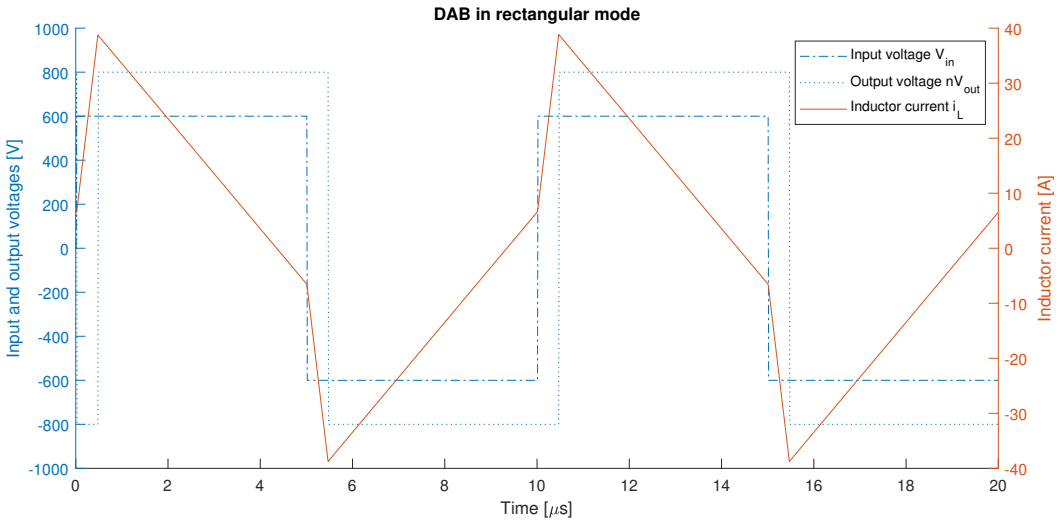


Figure 3.8: The simulated waveforms of the DAB in rectangular mode

3.5. Zero voltage switching

In order to obtain a high efficiency dual active bridge converter, the switching losses should be kept to a minimum. An advantage of the DAB converter is that it can switch at zero voltage, without the need of adding extra components as already discussed in Section 2.2.5. However, zero voltage switching (ZVS) is not always possible. For this the conditions listed in must be satisfied [25, 26]. ZVS occurs when there is a small dead time between two intervals; the energy stores in the inductor while switching will circulate through a completely turned off bridge, thereby charging and discharging the capacitors parallel to the switches. For example when referring to Figure 3.5, when switching from interval 1 to interval 2, the primary side switches Q_1 and Q_4 (see Figure 3.1) continue conduction, while on the secondary side Q_6 and Q_7 turn off. The capacitors across Q_5 and Q_8 will now be discharged to zero and the capacitors across Q_6 and Q_7 will charge to the secondary side voltage. Finally Q_5 and Q_8 will (after the short dead time) be turned on at zero voltage. This whole process of zero voltage switching depends on the energy stored in the inductor (Equation (3.19)) and the energy that can be stored in the capacitor (Equation (3.20)).

$$E_L = \frac{1}{2} L I^2 \tag{3.19}$$

$$E_C = \frac{1}{2} C V^2 \tag{3.20}$$

Table 3.2: Conditions for zero voltage switching of the DAB in rectangular mode

Parameter	Primary bridge	Secondary bridge
$I_{L1} > 0$ and $I_{L2} > 0$	ZVS	ZVS
$I_{L1} > 0$ and $I_{L2} < 0$	no ZVS	ZVS
$I_{L1} < 0$ and $I_{L2} > 0$	ZVS	no ZVS
$I_{L1} < 0$ and $I_{L2} < 0$	no ZVS	no ZVS

In order to have zero voltage switching at the secondary side bridge, the current I_{L1} should be positive as given in Table 3.2. Starting from the corresponding Equation (3.4) and demanding it to be positive, the condition for the phase shift is given in Equation (3.21).

$$\phi > \frac{\pi}{2}\left(1 - \frac{n \cdot V_{out}}{V_{in}}\right) \tag{3.21}$$

In a similar way the equation of the current I_{L0}, which is equal to $-I_{L2}$ can be used to obtain the zero voltage switching condition at the primary side bridge. Rewriting this equation for the phase shift will result in the

condition of Equation (3.22).

$$\phi > \frac{\pi}{2}\left(1 - \frac{V_{in}}{n \cdot V_{out}}\right) \tag{3.22}$$

The simulation of the previous section can be used to verify that a phase shift between these two limits will indeed results in a positive current for both I_{L1} and I_{L2}.

Knowing these limits is nice, however, the input and output voltages, as well as the turns ratio are not easy to vary and therefore it would be more useful to translate these conditions on the phase shift to a condition on the power. This is possible, since it was earlier states that the amount of power being transferred can be varied by only changing the phase shift. Starting with the condition for the secondary side bridge in Equation (3.21) and the equation of the power as function of the phase shift from Equation (3.15). The condition on the to be transferred power is as given in Equation (3.23).

$$P_{out} > \frac{n \cdot V_{out}}{V_{in}} \cdot \frac{V_{in}^2 - (n \cdot V_{out})^2}{8 f_s L} \tag{3.23}$$

This equation is only applicable if the voltage on the primary side (V_{in}) is larger than the voltage on the secondary side ($n \cdot V_{out}$).

Using the condition for zero voltage switching on the primary side bridge as given in Equation (3.22) in combination with the same equation for the power as just before (Equation (3.15)) the condition for the to be transferred power can be derived and is given in Equation (3.24). This equation is only applicable if the voltage on the primary side (V_{in}) is smaller than the voltage on the secondary side ($n \cdot V_{out}$), as opposed to the condition for ZVS on the secondary side bridge.

$$P_{out} > \frac{V_{in}}{n \cdot V_{out}} \cdot \frac{(n \cdot V_{out})^2 - V_{in}^2}{8 f_s L} \tag{3.24}$$

In order to gain some insight in the regions of zero voltage switching, the limits will be plotted. For this, the parameters of the converter will be quickly set to a minimal value. On the y-axis the power will be plotted above ZVS is achieved and on the x-axis the output voltage will be set. This is done for four different turn ratios for the transformer, namely $1.33:1$, $1:1$, $0.8:1$ and $0.67:1$. The inductance of the inductor and the switching frequency will be set in such a way that the maximum power transfer at 300 V is equal to 10 kW. However, this is not done with the maximum phase angle. As shown in [26], an increasing phase shift will lead to an enormous reactive power which will cause high conduction losses. Therefore, the maximum phase angle is set to $\phi = \pm\frac{\pi}{4}$. This will lead to a product of inductance and frequency as given in Equation (3.25):

$$f_s L = \frac{3n \cdot V_{out} V_{in}}{32 P_{out}} \tag{3.25}$$

The computed results for the region of zero voltage switching are plotted in Figure 3.9. In this figure, the area above the line indicates that ZVS is possible. In for example the red line is taken, that is for a DAB converter with a turns ratio of $1:1$. At 600 V, there is at every power level ZVS possible. However, if the output voltage is decreased to 500 V, it can be seen that below 6.8 kW the secondary side bridge is hard switching. It can be observed that the ZVS region is shrinking quickly if the output voltage (taken the turns ratio into account) differs from the input voltage. If there is not much variation between input and output voltage, the turns ratio can be chosen based on this input/ output ratio and a converter is obtained with easy control and zero voltage switching. However, with a large variation in output voltage, the region where ZVS applies becomes very small.

3.6. Conclusions

In this chapter the Dual Active Bridge with its most simple and popular modulation scheme is discussed. Firstly, an equivalent circuit was given based on two square wave voltage sources and an inductor. The assumption of ideal components was made and based on this waveforms of the voltages and current were given. The waveforms of the currents were further inspected and multiple equations were derived, among others for the RMS current in the inductor. Then there was a section about the transferred power and derivations were done on how the phase shift influences the power transfer before everything was simulated to verify the correctness of the given equations. Finally a section was dedicated to the zero voltage switching, again equations were derived and a plot was given to show in which regions zero voltage switching was possible. However, this

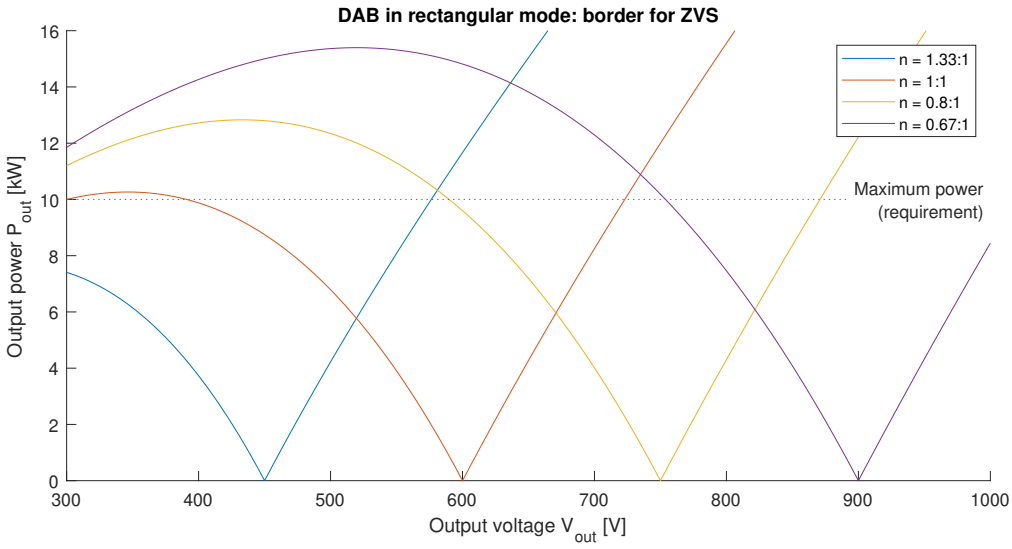


Figure 3.9: Minimum power for ZVS for different output voltages and turn ratios

specific figure showed that the ZVS was very narrow, and in order to make a converter with a high efficiency, no ZVS in such a wide region will probably result in too much losses. Therefore, a look should be taken into ways on how to reduce the losses, or in this case specific; how to increase the zero voltage switching region. Possible solutions to enhance the performance of this DAB converter are listed below:

- Varying switching frequency;
- Use of advanced modulation techniques;
- Use of a transformer with different turn ratios;
- Introduce a resonant tank;
- A combination of multiple options listed above.

The first option to vary the switching frequency can indeed increase the ZVS range, however, for very light loads the switching frequency can become very high, which will in place result in increased switching losses. Also designing for different switching frequencies can be a challenge. The use of advanced modulation techniques can increase the ZVS region as well, with its downside being the more complex waveform, which will require a more advanced controller. The use of a transformer with different turn rations will also increase the ZVS range, which can already be seen when one looks to Figure 3.9. This can be possible, because one specific type of car battery will vary in required voltage during charging, however, it will not vary over the complete range from 300 V up to 1000 V. Therefore, when the car connects, a turns ratio can be chosen before charging starts so there is no need to change the turns ratio during charging. The different turn ratios can be set by either a pair of MOSFET/ IGBTs or a relay, depending on which solution has the lowest losses. The downside of this solution is the more expensive transformer with an increased volume and weight and there is still a lack of ZVS at light loads. A fourth option can be to again dive into the converters with a resonant tank, as was already given as a promising topology in Section 2.4. The same advantages and disadvantages as given then still apply.

Finally it is chosen to operate the dual active bridge converter with more advanced modulation techniques. In this way there is no need to add extra components and in literature a significant increase in ZVS region and hence performance is seen. In the next chapter two more complex modulation techniques will be investigated.

4

Advanced modulation techniques

As concluded in the previous chapter, operating the dual active bridge converter with a rectangular mode of operation will probably result in too high switching losses. Therefore it was said to investigate some advanced modulation techniques. In this chapter two of these advanced modulation techniques will be investigated, namely the triangular and trapezoidal one. The structure is comparable to that in the previous chapter; the waveforms in the inductor will be shown first and equations will be derived, followed by the power transfer, and the results are verified by a simulation.

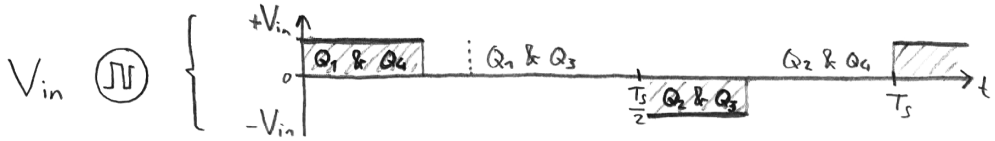
Contents in this chapter

4.1. Triangular current modulation

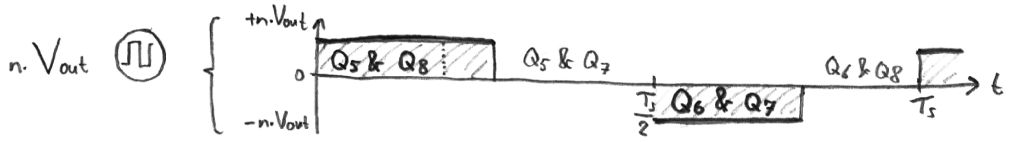
In order to analyse the operation of the dual active bridge under triangular current modulation, the same equivalent circuit as in the previous chapter is used. Again the circuit is assumed to be lossless for this analysis. In the previous chapter, where the rectangular current modulation was described, all switches had a duty cycle of 50 %, which is still the case for triangular current modulation. However, the resulting waveforms do not have an exact duty cycle of 50 %, which will become clear in the following sections. Also, for triangular current modulation a clear distinction is made between two different cases:

1. A voltage on the secondary side of the transformer lower than the input voltage: $V_{in} > n \cdot V_{out}$;
2. A voltage on the secondary side of the transformer larger than the input voltage: $V_{in} < n \cdot V_{out}$.

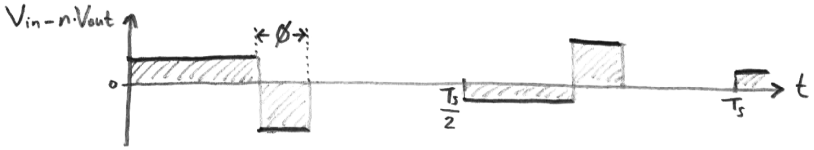
Firstly, the voltage levels of the square wave voltage sources will be given, for now without the current waveforms. For an input voltage larger than the voltage on the secondary side (first case), the voltage waveforms in the equivalent circuit look like the ones depicted in Figure 4.1. As can be seen, instead of only two voltage levels, each square wave voltage source is also able to generate a third level of 0 V. This can either be done by turning on the two top switches or the two bottom switching in the full bridges. To make this even more



(a) Voltage of the primary square wave voltage source



(b) Voltage of the secondary square wave voltage source

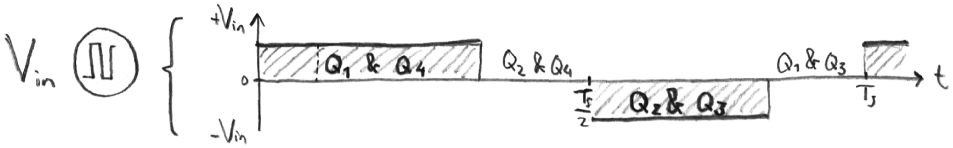


(c) Voltage across the inductor

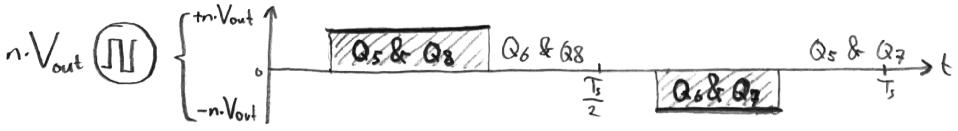
Figure 4.1: The voltages in the equivalent circuit of the DAB converter (triangular current modulation) with corresponding conducting switches for $V_{in} > n \cdot V_{out}$

clear, in Figure 4.1a en Figure 4.1b also the switches which are turned on at each specific moment are indicated. The numbering corresponds with the numbers of the switches from Figure 3.1. The phase shift is now defined as the difference between two moments when both voltage sources turn off, as indicated by the ϕ, just as before.

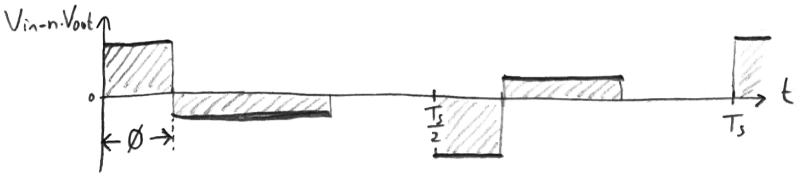
Similarly, it can also occur that the voltage on the secondary side of the transformer is larger than the voltage on the primary side. This is the second case and the resulting voltage waveforms of the square wave voltage sources are given in Figure 4.2. The waveforms will look more or less equal to the ones for the first



(a) Voltage of the primary square wave voltage source



(b) Voltage of the secondary square wave voltage source



(c) Voltage across the inductor

Figure 4.2: The voltages in the equivalent circuit of the DAB converter (triangular current modulation) with corresponding conducting switches for $V_{in} < n \cdot V_{out}$

case, where the voltage on the primary side was larger. Again there are three voltage levels instead of two for the rectangular current modulation and the corresponding switches that are turned on in each interval are indicated. One thing that needs attention is the way how the phase shift ϕ is defined in this mode. Now the

phase shift is the difference between the rise of both square wave voltage sources.

In the case of a reverse power flow, the voltage source with the longer duty cycle will remain the same, while the one with the shorter duty cycle will shift. If the two voltage sources turned on at the same time while transferring power from input to output, the two voltage sources will turn off at the same time to let the power flow in the reverse way. Vice versa if the voltage sources turned off with positive power flow, this will let the current flow in the opposite direction. More details on this in the remaining part of this chapter.

4.1.1. Inductor current waveform

Now the waveforms of the voltages are shown in the previous section, the currents are added to the analysis. In the equivalent circuit the voltage across the inductor is still determined by the voltage applied to in by the two voltage sources. For a positive power flow, the inductor current waveform is given in Figure 4.3, the mode is analysed for a primary voltage larger than the secondary voltage first: $V_{in} > n \cdot V_{out}$. In order to see the relation between the voltage across the inductor and the current through it even better, the voltage across the inductor is also given in the same plot by the dotted line. Different parts of the waveform are

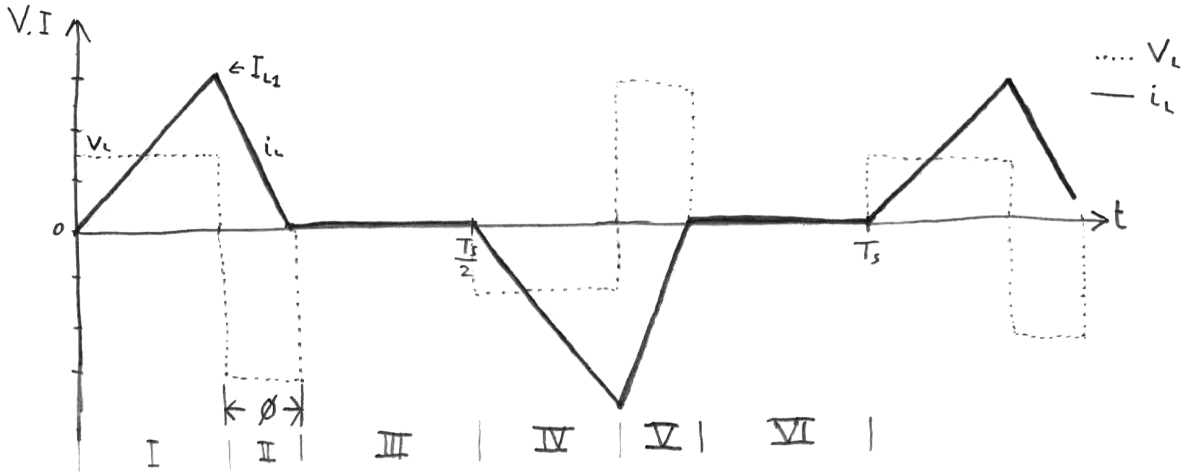


Figure 4.3: The inductor current waveform if $V_{in} > n \cdot V_{out}$ for triangular current modulation

labelled by numbers in Roman. In the first part, the voltage across the inductor is equal to $V_{in} - n \cdot V_{out}$. Using Equation (3.3), the current in the first part is described by Equation (4.1).

$$i_{L,1}(t) = \frac{V_{in} - n \cdot V_{out}}{L} t \tag{4.1}$$

Following the same procedure, the current in the second interval can be written as in Equation (4.2).

$$i_{L,2}(t) = I_{L1} - \frac{n \cdot V_{out}}{L}(t - T_1) \tag{4.2}$$

In this equation T_1 is the duration of the first interval. A derivation for the time T_1 will follow soon. During the third interval, there is no voltage drop across the inductor and as can be seen in Figure 4.3 there is no current flowing, hence Equation (4.3).

$$i_{L,3}(t) = 0 \tag{4.3}$$

As said earlier and can be seen in the figure of the waveforms, the phase shift is related to the duration of the second interval. This is expressed by Equation (4.4):

$$T_\phi = T_2 = \frac{\phi}{\pi f_s} \tag{4.4}$$

Next, the duration of interval 1 (T_1) can be written as a function of the duration of interval 2, and thus the phase shift. In order to do that, one should note that the current starts from 0 A at the beginning of the first interval and is again equal to 0 A at the end of the second interval. Given the relation of the voltages across the inductor, Equation (4.5) holds.

$$T_1 = T_2 \cdot \frac{n \cdot V_{out}}{V_{in} - n \cdot V_{out}} \tag{4.5}$$

The peak value of the current in the inductor I_{L1} can now easily be derived, either from the duration of T_1 or T_2. When using T_2 (which will lead to a more readable equation when using the phase shift later on) the peak value can be expressed by Equation (4.6).

$$I_{L1} = \frac{n \cdot V_{out}}{L} T_2 \tag{4.6}$$

Substituting the duration of the second interval with the phase shift given in Equation (4.4) will result in Equation (4.7).

$$I_{L1} = \frac{n \cdot V_{out}}{L} \cdot \frac{\phi}{\pi f_s} \tag{4.7}$$

The equations for the intervals 4, 5 and 6 are again similar to the ones of 1, 2 and 3 respectively. Due to symmetry the slopes and initial values are negative, just as with the rectangular modulation.

The next step is calculating the RMS current through the inductor. As already has been seen and looking at the name of this modulation waveform, the current has the shape of a triangle. Due to symmetry reasons, only the first half of a period is considered, the second half has the same RMS current. The intervals numbered 1 and 2 have the shape of a triangle. Before the actual calculation on the RMS current is done, a general form is discussed first to find the RMS current in a triangular shape. For this the waveform in Figure 4.4 is investigated. The current in this figure can be described as Equation (4.8). With a starting value of 0 and a

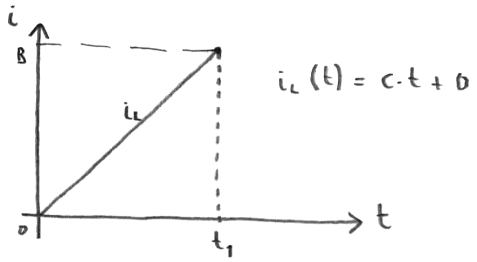


Figure 4.4: Triangular waveform to derive an equation for the RMS current

slope of c.

$$i_L(t) = c \cdot t + 0 \tag{4.8}$$

The RMS value is then calculated as in Equation (4.9).

$$I_{RMS,triangle} = \sqrt{\frac{1}{t_1} \int_0^{t_1} c^2 \cdot t^2 dt} \tag{4.9}$$

Integrating the equation above and working out results in Equation (4.10).

$$I_{RMS,triangle} = \frac{1}{\sqrt{3}} \cdot |c| \cdot t_1 \tag{4.10}$$

If one takes again a look at the actual waveform of the current in Figure 4.3, the slope in the first interval is given in Equation (4.11) and the slope in the second interval is given in Equation (4.12).

$$c_{tri,1} = \frac{V_{in} - n \cdot V_{out}}{L} \tag{4.11}$$

$$c_{tri,2} = \frac{n \cdot V_{out}}{L} \tag{4.12}$$

The corresponding times were already given before as T_1 and T_2 in Equation (4.5) and Equation (4.4) respectively. If both RMS currents of the individual intervals are calculated, the RMS current of the complete waveform can be obtained by using Equation (4.13):

$$I_{L,RMS} = \sqrt{\frac{T_1}{0.5T_s} I_{RMS,1}^2 + \frac{T_2}{0.5T_s} I_{RMS,2}^2} \tag{4.13}$$

The second case is that the voltage on the secondary side is larger than the voltage on the primary side, which can be expressed as $V_{in} < n \cdot V_{out}$. Again the voltage across the inductor of the equivalent circuit is

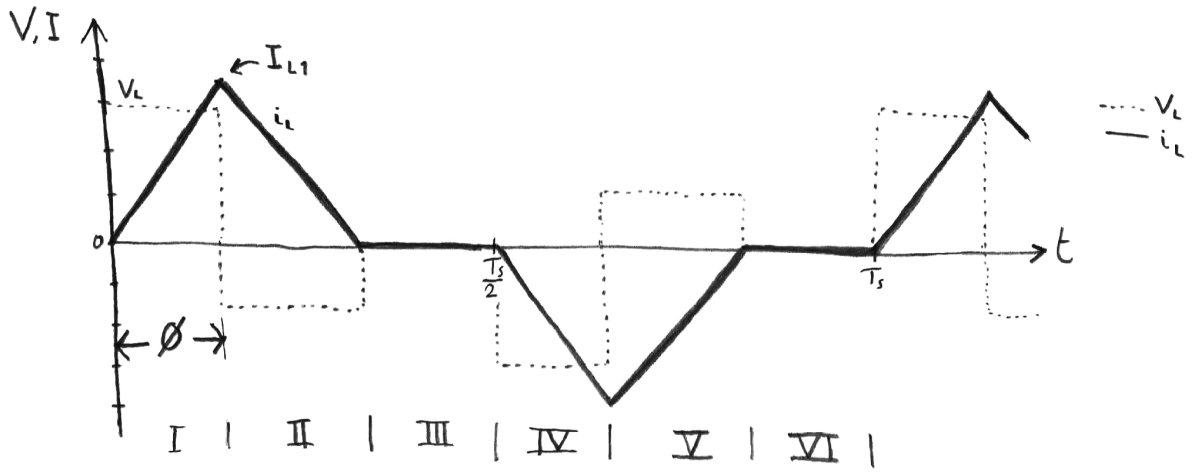


Figure 4.5: The inductor current waveform if $V_{in} < n \cdot V_{out}$ for triangular current modulation

given in the plot as well as the current through the inductor. One period is given in Figure 4.5. Again the intervals are labelled by numbers in Roman. In the first part, the voltage across the inductor is equal to V_{in}. The current in the first interval is then described by Equation (4.14).

$$i_{L,1}(t) = \frac{V_{in}}{L} t \tag{4.14}$$

In the same way, the voltage in the second interval is equal to Equation (4.15).

$$i_{L,2}(t) = I_{L1} - \frac{n \cdot V_{out} - V_{in}}{L} (t - T_\phi) \tag{4.15}$$

Where T_ϕ depends on the phase shift, which is also shown in Figure 4.5. In the third interval, there is again no current flowing through the inductor and thus the waveform is described by Equation (4.16).

$$i_{L,3}(t) = 0 \tag{4.16}$$

It was already said in the first part of this chapter, but the phase shift is different depending on the output voltage. In the case of an output voltage larger than the input ($V_{in} < n \cdot V_{out}$), the phase shift is related to the duration of the first interval T_1. This is expressed by Equation (4.17):

$$T_\phi = T_1 = \frac{\phi}{\pi f_s} \tag{4.17}$$

The current at the end of the second interval is equal to the current at the beginning of the first interval; 0 A. Therefore, the durations of T_1 and T_2 are related to each other, depending on the voltage levels. This relation is given in Equation (4.18).

$$T_2 = T_1 \cdot \frac{V_{in}}{n \cdot V_{out} - V_{in}} \tag{4.18}$$

The peak value of the current in the inductor I_{L1} is easily found and expressed in terms of the phase shift and can be seen in Equation (4.19).

$$I_{L1} = \frac{V_{in}}{L} \cdot \frac{\phi}{\pi f_s} \tag{4.19}$$

To obtain the RMS currents in this case, the same general equation derived previously can be used to get the RMS current of a triangular waveform. Take again a look at the waveform of the current in Figure 4.5, the slope in the first interval is given in Equation (4.20) and the slope in the second interval is given in Equation (4.21).

$$c_{tri,1} = \frac{V_{in}}{L} \tag{4.20}$$

$$c_{tri,2} = \frac{n \cdot V_{out} - V_{in}}{L} \tag{4.21}$$

The corresponding times were also given in Equation (4.17) and Equation (4.18) respectively. Starting by calculating both the RMS currents of the individual intervals, whereafter Equation (4.13) can be used to obtain the RMS current of the complete waveform of the inductor current.

4.1.2. Semiconductor currents

Besides knowing the currents flowing through the inductor, the current flowing through each of the semiconductors can be determined. This will be done for each of the eight switches, as well as eight diodes in the circuit of the dual active bridge converter. The current that flows through the inductor, flows at each moment also through four semiconductors, which follows from simple circuit analysis. Therefore the current waveforms of each of the switches will look similar to the one of the inductor current. Sketches of the waveform are given in Figure 4.6. Note that only the currents through Q_x are given. A positive current means the semicon-

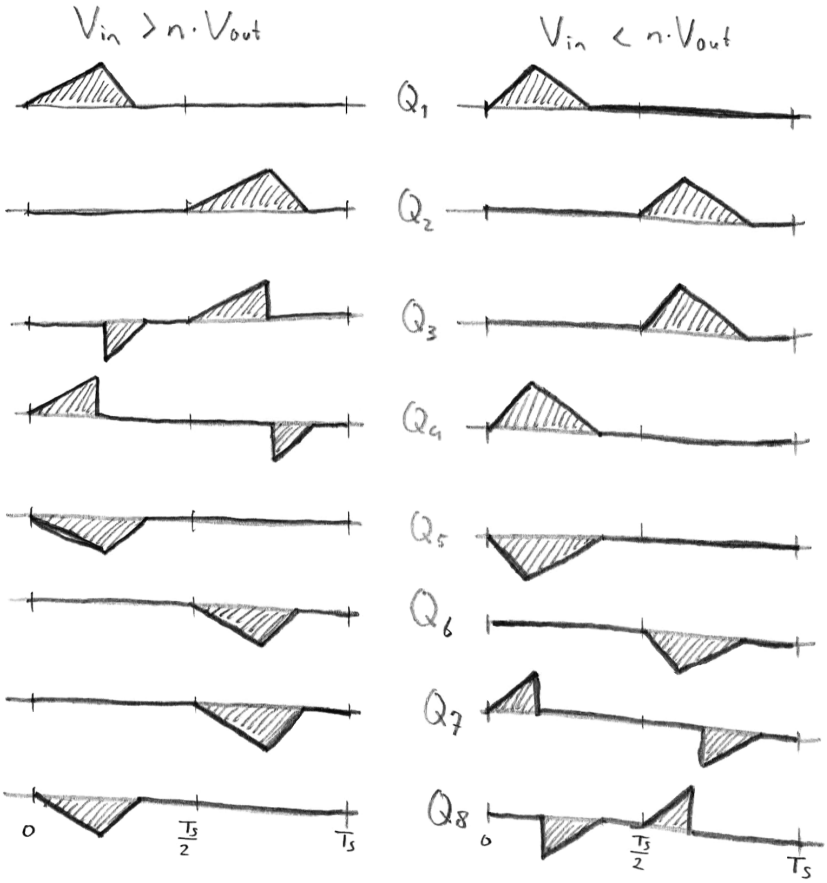


Figure 4.6: The current waveforms through the semiconductors for positive power transfer under triangular current modulation

ductor switch is conducting, while a negative current indicated the diode is conducting. The peak values of course correspond to the peak values of the inductor current, given in Section 4.1.1. With respect to the RMS current, it makes sense that previously the waveform of the inductor was separated in parts with for each part the RMS current calculated. For the calculation of the RMS current in each semiconductor, Equation (4.13) can be modified into Equation (4.22):

$$I_{Q_x,RMS} = \sqrt{p_1 \cdot \frac{T_1}{T_s} I_{RMS,1}^2 + p_2 \cdot \frac{T_2}{T_s} I_{RMS,2}^2} \tag{4.22}$$

Here, $I_{RMS,1}$ and $I_{RMS,2}$ are the RMS values in the first and second interval respectively, which were defined in the previous section. The constants p_1 and p_2 are either 0, 1 or n^2, depending on their presence in the current waveform of the chosen semiconductor. A zero means not present and a 1 or n^2 means present, where the n^2 corrects the current for the secondary side of the transformer (all diodes and semiconductors with subscripts 5-8). These constants can be derived from the given sketch in Figure 4.6, and are given in Table 4.1.

If there is a reverse power flow, so power from *out* to *in*, the constants of the diodes should be swapped with the constants of the semiconductor switches.

Table 4.1: List of constants p_1 and p_2 for calculating the RMS current in semiconductors under triangular current modulation

	$V_{in} > n \cdot V_{out}$		$V_{in} < n \cdot V_{out}$	
Semiconductor	p_1	p_2	p_1	p_2
Switch S_1	1	1	1	1
Switch S_2	1	1	1	1
Switch S_3	1	0	1	1
Switch S_4	1	0	1	1
Switch S_5	0	0	0	0
Switch S_6	0	0	0	0
Switch S_7	0	0	n^2	0
Switch S_8	0	0	n^2	0
Diode D_1	0	0	0	0
Diode D_2	0	0	0	0
Diode D_3	0	1	0	0
Diode D_4	0	1	0	0
Diode D_5	n^2	n^2	n^2	n^2
Diode D_6	n^2	n^2	n^2	n^2
Diode D_7	n^2	n^2	0	n^2
Diode D_8	n^2	n^2	0	n^2

4.1.3. Zero voltage switching

The reason to find an alternative modulation technique for the rectangular current modulation, was the high expected switching loss. This section will discuss the soft switching performance of the triangular current modulation. Referring back to Figure 4.6, the current in the individual switches can be seen. This makes it easy to identify the switches with switching losses. Both turning on and turning off the switches happens at zero voltage [11], so only a look will be taken at the current. It can be seen that in all cases the current starts from zero, which indicates the switches turn on at zero current. Turning on switches at zero voltage and zero current will result in negligible switching losses. Then the turning off of the switches. Looking again at Figure 4.6, there are every period two switches turned off while there was still current flowing. For $V_{in} > n \cdot V_{out}$ this occurs for switches S_3 and S_4, and if $V_{in} < n \cdot V_{out}$ this occurs for switches S_7 and S_8. So there are two switches turning off at zero voltage, but at a finite current, which will result in a non-negligible switching loss. The other six switches turn off at zero voltage and zero current, which means those losses can be neglected.

4.1.4. Transferred power

Now the voltage and current waveforms are clear, the equation for the transferred power can be derived. Again the case is considered where $V_{in} > n \cdot V_{out}$ first. The power is found by multiplying the voltage with the current. Referring back to the waveforms, it can be seen that the voltage of the secondary side is constant while current is flowing. Due to symmetry again the first half period is considered and the power can be calculated with Equation (4.23).

$$P_{tri} = \frac{2}{T_s}\left(\int_0^{T_1} \frac{V_{in} - n \cdot V_{out}}{L} t\,dt + \int_{T_1}^{T_1+T_2} \frac{V_{in} - n \cdot V_{out}}{L} T_1 - \frac{n \cdot V_{out}}{L}(t - T_1)\,dt\right) n \cdot V_{out} \tag{4.23}$$

Writing out the integrals and simplify the obtained equation results in Equation (4.24).

$$P_{tri} = \frac{n \cdot V_{out}}{LT_s}\left(V_{in} T_1 (T_1 + 2T_2) - n \cdot V_{out}(T_1 + T_2)^2\right) \tag{4.24}$$

Filling in the equation for the phase shift and thereby substituting for T_1 and T_2 gives the final equation of the power for triangular mode, with $V_{in} > n \cdot V_{out}$ in Equation (4.25).

$$P_{tri} = \frac{\phi^2 V_{in} (n \cdot V_{out})^2}{\pi^2 f_s L (V_{in} - n \cdot V_{out})} \tag{4.25}$$

Just as with the rectangular modulation, the power can be controlled by modifying the phase shift. Starting from the equation of the power given in Equation (4.25), the phase shift can be given as function of the power, which is shown in Equation (4.26)

$$\phi_{tri} = \pi \cdot \sqrt{\frac{P_{tri} f_s L (V_{in} - n \cdot V_{out})}{V_{in} (n \cdot V_{out})^2}} \tag{4.26}$$

By adjusting the phase shift, the amount of power being transferred can be controlled. However, attention should be paid to the limits of the phase shift. When taking a closer look to Figure 4.3, the phase shift is related to the width of the triangle. Note that the current should be zero again halfway the period, at $t = \frac{T_s}{2}$. This means that the triangle should be completed within this time, formulated in Equation (4.27).

$$T_1 + T_2 \leq \frac{T_s}{2} \tag{4.27}$$

If the phase shift is plugged into this equation instead of the times T_1 and T_2, the maximum phase shift os given in Equation (4.28).

$$\phi_{tri,max} = \frac{\pi}{2} \cdot \left(1 - \frac{n \cdot V_{out}}{V_{in}}\right) \tag{4.28}$$

Having a maximum phase shift means having a maximum on the to be transferred power. Plugging the maximum phase shift back into the formula of the power (Equation (4.25)), the maximum power is obtained in Equation (4.29).

$$P_{tri,max} = \frac{(V_{in} - n \cdot V_{out}) \cdot (n \cdot V_{out})^2}{4 V_{in} f_s L} \tag{4.29}$$

The same procedure can be followed for the second case, where $V_{in} < n \cdot V_{out}$. This results in a transferred power as function of times given in Equation (4.30).

$$P_{tri} = \frac{V_{in}}{L T_s} \left(V_{in} (T_1 + T_2)^2 - n \cdot V_{out} T_2^2\right) \tag{4.30}$$

Which can also be written as a function of the phase shift ϕ in Equation (4.31).

$$P_{tri} = \frac{\phi^2 n \cdot V_{out} V_{in}^2}{\pi^2 f_s L (n \cdot V_{out} - V_{in})} \tag{4.31}$$

Expressing the phase shift as a function of the power is done in Equation (4.32)

$$\phi_{tri} = \pi \cdot \sqrt{\frac{P_{tri} f_s L (n \cdot V_{out} - V_{in})}{V_{in}^2 n \cdot V_{out}}} \tag{4.32}$$

Using the same limit as in Equation (4.27) gives the maximum phase shift in Equation (4.33).

$$\phi_{tri,max} = \frac{\pi}{2} \cdot \left(1 - \frac{V_{in}}{n \cdot V_{out}}\right) \tag{4.33}$$

With the according maximum power given by Equation (4.34).

$$P_{tri,max} = \frac{V_{in}^2 (n \cdot V_{out} - V_{in})}{4 n \cdot V_{out} f_s L} \tag{4.34}$$

To show graphically the limits on the transferred power, a plot is given in Figure 4.7. For different turns ratios, the frequency and inductor is set equal to the values previously used in the graph of Figure 3.9. The numbers do not have a real meaning, more important is the shape of the curves. As can be seen, the curve of maximum power can be shifted (along the x-axis) by varying the turns ratio. Also, the curve can be scaled by modifying the inductance of the inductor or the switching frequency. However, there is one point where actually no power transfer is possible. This is the case if the voltages on both sides of the inductor are equal; $V_{in} = n \cdot V_{out}$.

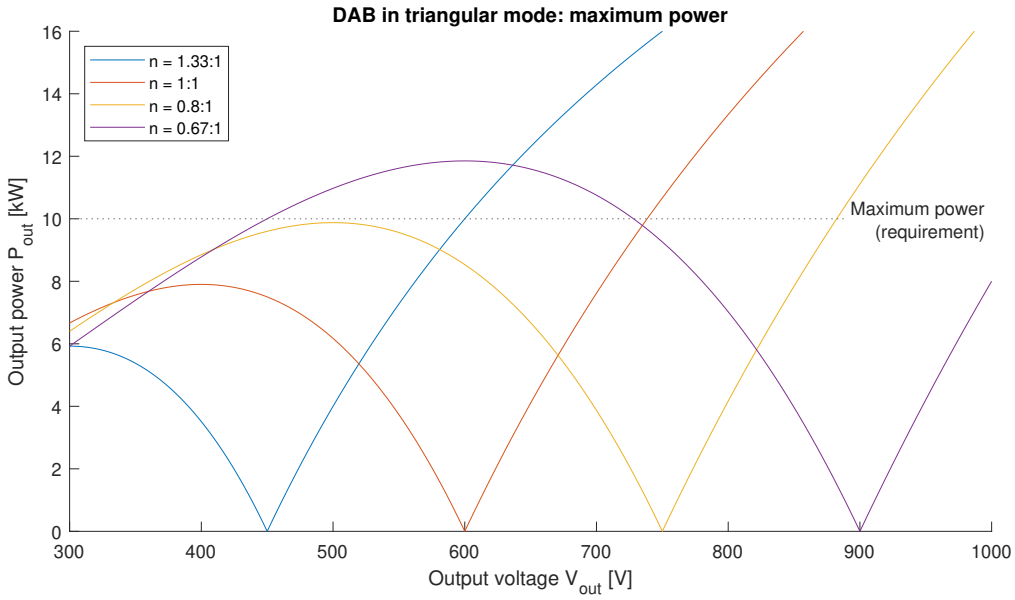


Figure 4.7: The maximum power transfer under triangular current modulation for different turns ratios

4.1.5. Simulations

The next step is to verify the obtained results by performing some simulations. This time, the circuit is made out of MOSFETs to create a waveform, rather than ideal square wave voltage sources. The circuit is depicted in Figure 4.8. The corresponding control logic is slightly more complex in order to deal with all different kinds of situations (i.e. positive and negative power flow, $V_{in} > n \cdot V_{out}$ and $V_{in} < n \cdot V_{out}$). For each pair of switches a separate square wave voltage is generated, where the gate signals for Q_1 and Q_2 are equal to the gate signals of Q_5 and Q_6. The control logic is given in Figure 4.9. The parameters as given in Table 4.2 are set to cover all four different type of waveforms. Making use of Equation (4.26) and Equation (4.32), the corresponding required phase shift is calculated, which is for ±6.0 kW at 400 V output a phase shift of ±0.4967 and for an output power of ±10.0 kW at 800 V a phase shift of ±0.3702. Plugging in the parameters results in the expected waveforms, and the power transfer is indeed 6.0 kW at 400 V and at 800 V the output power is 9.9 kW. This is slightly less than the required 10.0 kW. This can be explained by the fact that the equations were derived from ideal voltage sources and the simulation is performed with lossy MOSFETs. It is also simulated, that for a power transfer of 10.0 kW a phase shift of 0.3708 is required to compensate for the losses in the circuit. Furthermore it is concluded, that the sign of the phase shift determines indeed the power transfer, a positive sign lead to a power transfer from input to output, and a negative sign a power flow in the opposite direction.

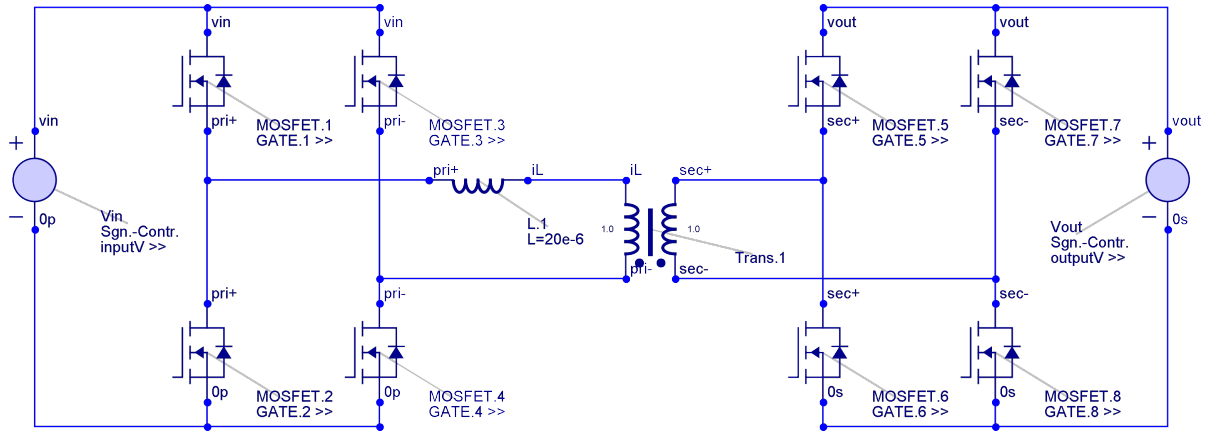


Figure 4.8: The electrical circuit of the DAB (triangular mode) in Gecko Circuits

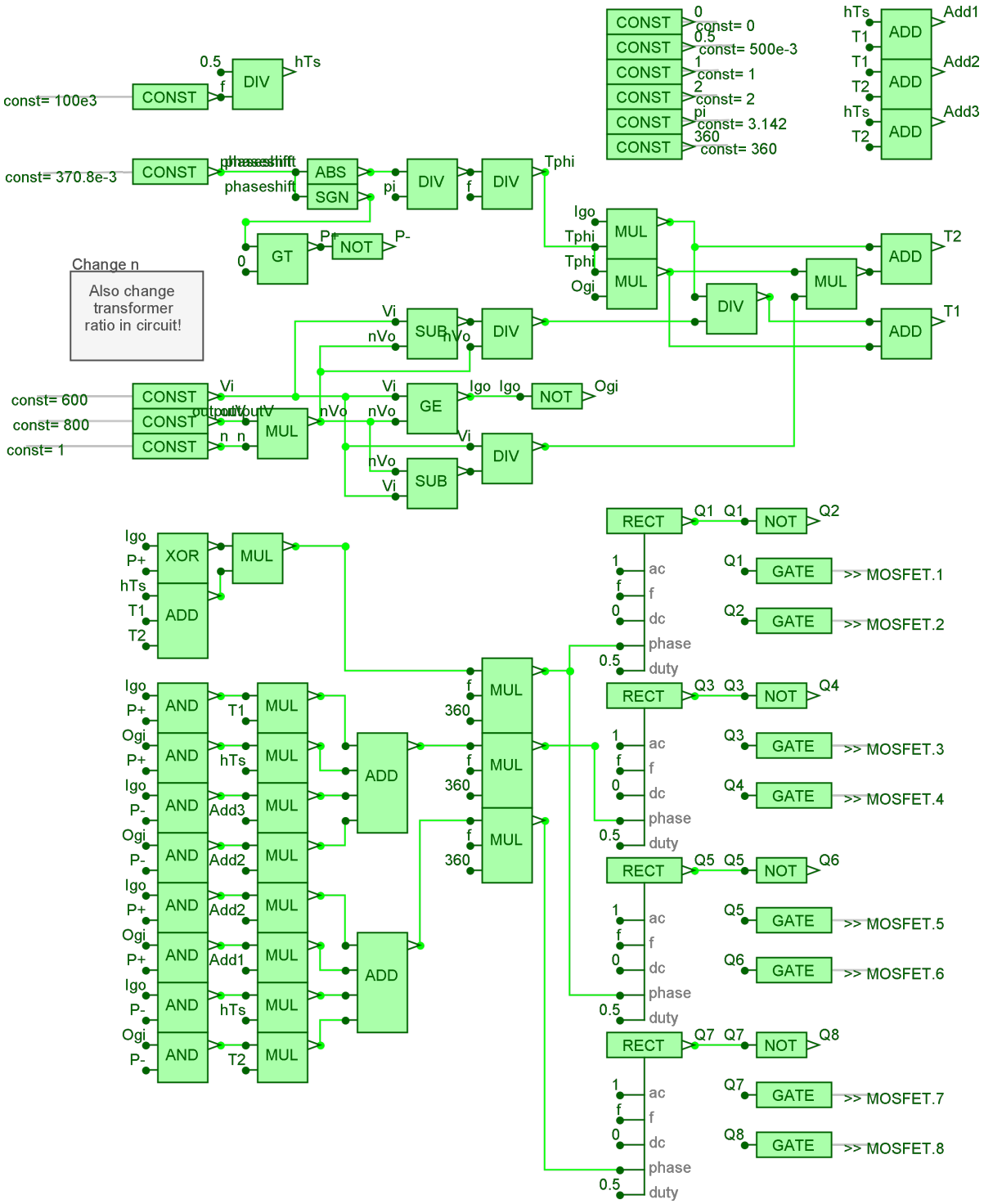


Figure 4.9: The control logic of the DAB (triangular mode) in Gecko Circuits

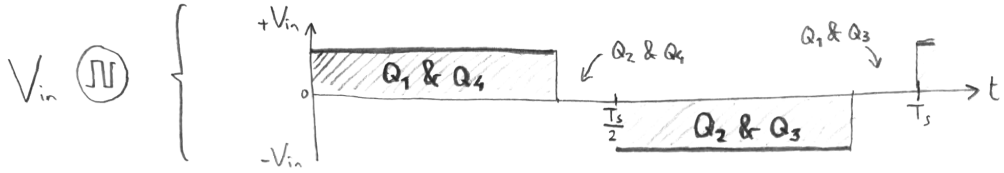
So if some losses in the circuit are taken into account, the actual transferred power can be slightly less. This can be solved by a better modelling (including losses into the derived equations) or in practise, a feedback loop which measures the output power and changes the phase shift accordingly. Furthermore it can be said that everything behaves as expected and the derived formulas were correct.

Table 4.2: Parameters for the simulation of the equivalent DAB in triangular mode

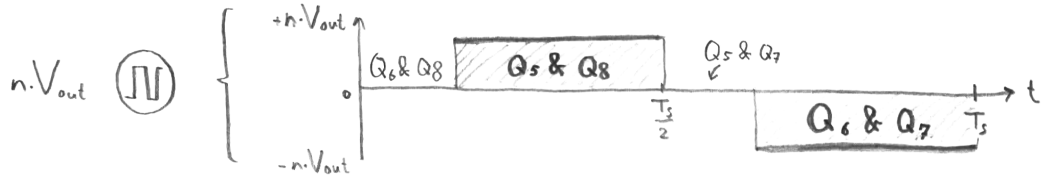
Parameter	Value
Input voltage V_{in}	600 V
Output voltage V_{out}	400 V & 800 V
Transformer turns ratio $n:1$	1
Switching frequency f_s	100 kHz
Inductance L	20 µH
Transferred power P_{out}	±6.0 kW (400 V output)
	±10.0 kW (800 V output)

4.2. Trapezoidal current modulation

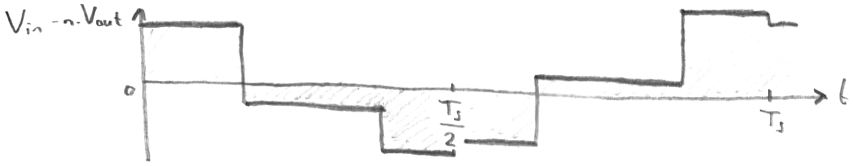
Another advanced modulation technique possible is the trapezoidal current modulation, which will be discussed in the following pages. Again the lossless circuit will be analysed and the voltage waveforms will be given. In this section only the trapezoidal current modulation is discussed, without a *zero voltage time*. This is a moment where there is no voltage difference across the inductor, as was the case for the triangular waveform modulation (T_3). The voltage across the inductor varies between V_{in}, V_{out} and $V_{in}-V_{out}$ and the corresponding negative values. The voltage waveforms of the equivalent voltage sources are given in Figure 4.10, with in Figure 4.10c the voltage across the inductor $V_L = V_{in} - n \cdot V_{out}$.



(a) Voltage of the primary square wave voltage source



(b) Voltage of the secondary square wave voltage source



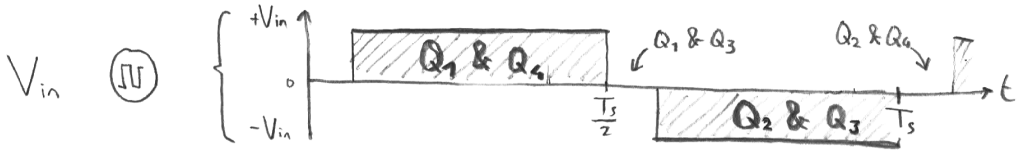
(c) Voltage across the inductor

Figure 4.10: The voltages in the equivalent circuit of the DAB converter (trapezoidal current modulation) with corresponding conducting switches for a positive power transfer

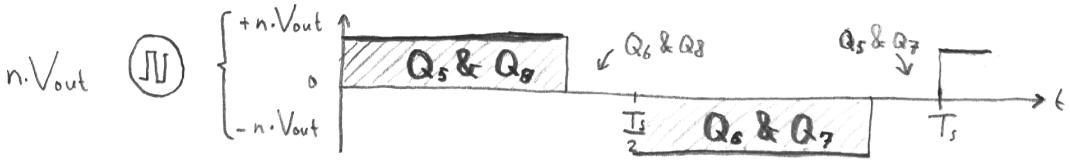
The phase shift is defined as the difference between the turning on of the equivalent voltage source on one side (V_{in}) and the turning on of the equivalent voltage source on the other side ($n \cdot V_{out}$) of the inductor. If the power flow is negative, the zero period of each equivalent voltage source of each half period is moved to the other side of the half period, as indicated in Figure 4.11.

4.2.1. Inductor current waveform

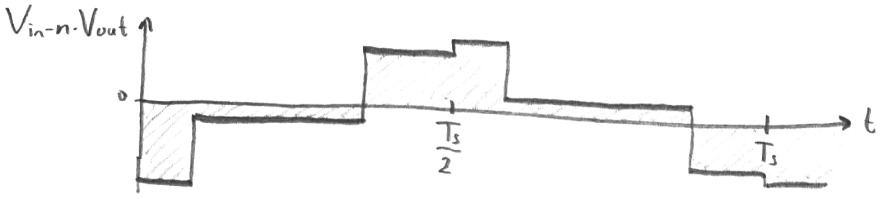
With the voltage waveforms known, the currents can be analysed. The voltage across the inductor determines the current through it. In Figure 4.12, the voltage across the inductor is given as well as the current through it. In the figure the situation is depicted for a positive power flow and $V_{in} < n \cdot V_{out}$. The intervals are again labelled with numbers in Roman and the equations are given which describes the current waveform in all



(a) Voltage of the primary square wave voltage source



(b) Voltage of the secondary square wave voltage source



(c) Voltage across the inductor

Figure 4.11: The voltages in the equivalent circuit of the DAB converter (trapezoidal current modulation) with corresponding conducting switches for a negative power transfer

intervals. The first part is given by Equation (4.35).

$$i_{L,1}(t) = \frac{V_{in}}{L} t \tag{4.35}$$

During the second interval, both equivalent voltage sources are turned on, so the voltage difference is related to the slope, as is seen in Equation (4.36), which is slightly simplified. T_1 is the duration of the first interval.

$$i_{L,2}(t) = \frac{n \cdot V_{out}}{L} T_1 + \frac{V_{in} - n \cdot V_{out}}{L} t \tag{4.36}$$

Depending on the voltage levels of both equivalent voltage sources on both sides of the inductor with levels V_{in} and $n \cdot V_{out}$, the slope in this second interval can be either positive or negative. This also determines if the peak inductor current is I_{L1} or I_{L2}. The third interval can then be described by Equation (4.37).

$$i_{L,3}(t) = \frac{V_{in} - n \cdot V_{out}}{L} T_1 + \frac{V_{in}}{L} T_2 - \frac{n \cdot V_{out}}{L} t \tag{4.37}$$

Given there is no moment where the current through the inductor stays zero for a while, the relation given by Equation (4.38) holds.

$$T_1 + T_2 + T_3 = \frac{T_s}{2} \tag{4.38}$$

The duration of the second (T_2) and third interval (T_3) can be expressed in Equation (4.39) and Equation (4.40).

$$T_2 = \frac{n \cdot V_{out}}{V_{in}} \left(\frac{T_s}{2} - T_1 \right) - T_1 \tag{4.39}$$

$$T_3 = \frac{T_s}{2} - \frac{n \cdot V_{out}}{V_{in}} \left(\frac{T_s}{2} - T_1 \right) \tag{4.40}$$

The duration of the first interval is related to the phase shift as can be seen in Figure 4.12, this relation is given in Equation (4.41) below:

$$T_\phi = T_1 = \frac{\phi T_s}{\pi} \tag{4.41}$$

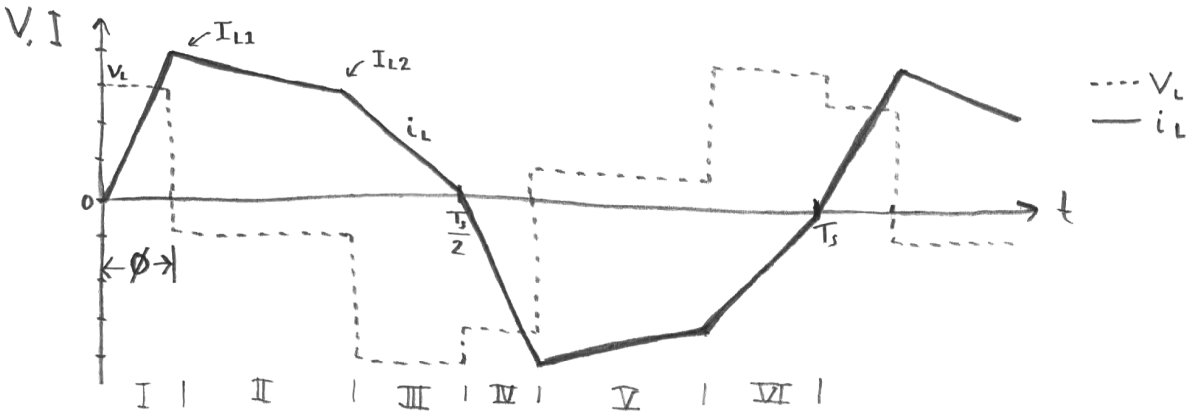


Figure 4.12: The inductor current waveform for trapezoidal current modulation

Using Equation (4.39), Equation (4.40) and Equation (4.41) all intervals can be expressed as a function of the phase shift. Due to symmetry the durations T_4, T_5 and T_6 are equal to T_1, T_2 and T_3 respectively.

The peak values of inductor current I_{L1} and I_{L2} can be expressed both as a function of the interval durations and a function of the phase shift. For the first peak, the peak is given in Equation (4.42).

$$I_{L1} = \frac{V_{in}}{L} T_1 = \frac{V_{in}}{L} \cdot \frac{\phi T_s}{\pi} \tag{4.42}$$

The second peak as function of the duration of the third interval is given by Equation (4.43), which eventually can be expressed as a function of the phase shift.

$$I_{L2} = \frac{n \cdot V_{out}}{L} T_3 \tag{4.43}$$

The highest one of both peaks is I_{L1} in the case $V_{in} < n \cdot V_{out}$ and I_{L2} if $V_{in} > n \cdot V_{out}$. In the case $V_{in} = n \cdot V_{out}$, both peaks have the same value. This can be seen by the fact that the slope in the second interval is zero.

Now the RMS current through the inductor is calculated. The shape of the current is that of a trapezoidal, hence the name of this current modulation scheme. Firstly, the RMS value of a standard waveform pattern is investigated. This waveform is given in Figure 4.13. With a slope c and a starting value of a, the RMS current

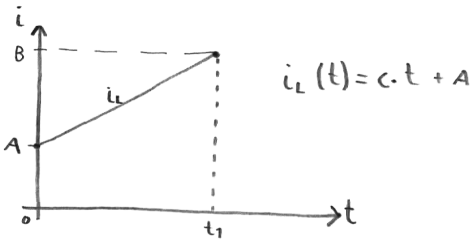


Figure 4.13: Trapezoidal waveform to derive an equation for the RMS current

is found as in Equation (4.44).

$$I_{RMS,trapezoidal} = \sqrt{\frac{1}{t_1} \int_0^{t_1} (ct + a)^2 dt} \tag{4.44}$$

Simplifying this expression results in Equation (4.45).

$$I_{RMS,trapezoidal} = \sqrt{\frac{1}{3} c^2 t_1^2 + act_1 + a^2} \tag{4.45}$$

For each interval, the values of the slope c and starting value a are given in Table 4.3. If the RMS values of all different intervals are calculated, the RMS value of the complete waveform can be obtained with Equation (4.46). In this equation, $I_{RMS,x}$ is the previously calculated RMS current in the inductor in interval x.

$$I_{L,RMS} = \sqrt{\frac{T_1}{0.5T_s} I_{RMS,1}^2 + \frac{T_2}{0.5T_s} I_{RMS,2}^2 + \frac{T_3}{0.5T_s} I_{RMS,3}^2} \tag{4.46}$$

Table 4.3: List of constants for the slope and starting value of different intervals for trapezoidal current modulation

Interval	Slope c	Starting value a
First	$\frac{V_{in}}{L}$	0
Second	$\frac{V_{in}-n\cdot V_{out}}{L}$	$\frac{V_{in}}{L}\cdot\frac{\phi}{\pi f_s}$
Third	$\frac{n\cdot V_{out}}{L}$	0

4.2.2. Semiconductor currents

The next step is to determine the currents in the semiconductors. Since there are always four semiconductors which carry the same current as the inductor (they can be seen as if they are in series), the peak values in the semiconductors are the same as the peak currents in the inductor. The only difference is when which semiconductor is conducting. Sketches of the current through each semiconductor is given in Figure 4.14 for each interval. Note that a negative current indicates the diode is conducting and by a positive current the semiconductor switch is conducting. In order to determine the RMS current of each switch, a similar pro-

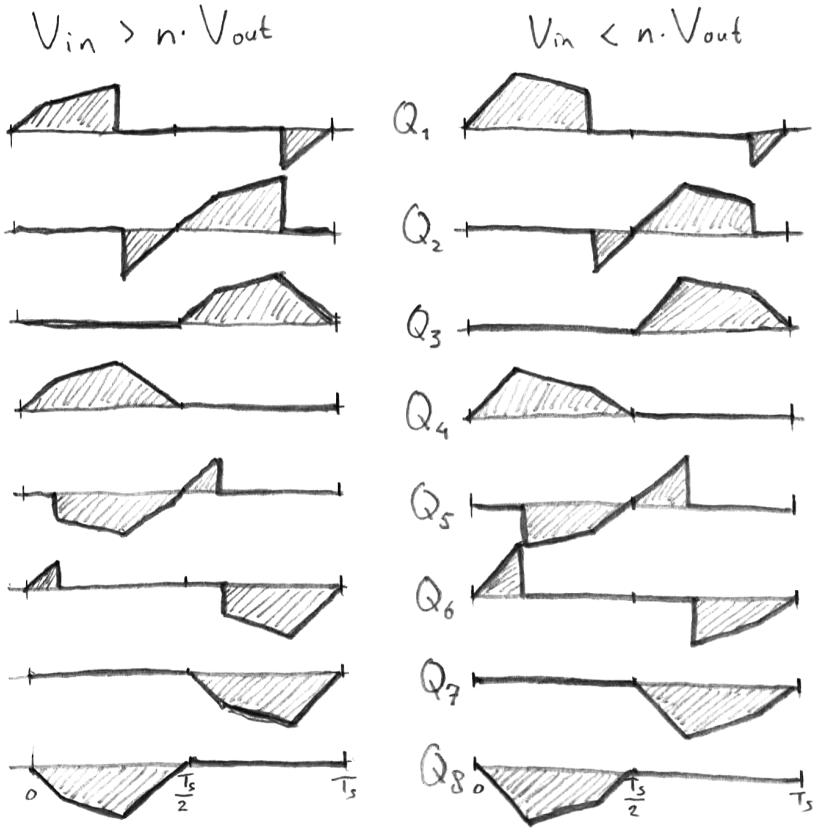


Figure 4.14: The current waveforms through the semiconductors for positive power transfer under trapezoidal current modulation

cedure is used when the RMS current through the inductor was calculated. The values of $I_{RMS,1}$, $I_{RMS,2}$ and $I_{RMS,3}$ are the same, however, the RMS current of an individual semiconductor depends on which intervals it is conducting. The total RMS current can be calculated using Equation (4.47)

$$I_{Q_x,RMS} = \sqrt{p_1 \cdot \frac{T_1}{T_s} I_{RMS,1}^2 + p_2 \cdot \frac{T_2}{T_s} I_{RMS,2}^2 + p_3 \cdot \frac{T_3}{T_s} I_{RMS,3}^2} \tag{4.47}$$

In this formula, p_1, p_2 and p_3 are constants, the values depend on the semiconductor being investigated. The constants can be derived from the sketches and are shown in Table 4.4. The factor n^2 compensates for

Table 4.4: List of constants p_1, p_2 and p_3 for calculating the RMS current in semiconductors under trapezoidal current modulation

Semiconductor	p_1	p_2	p_3
Switch S_1	1	1	0
Switch S_2	1	1	0
Switch S_3	1	1	1
Switch S_4	1	1	1
Switch S_5	n^2	0	0
Switch S_6	n^2	0	0
Switch S_7	0	0	0
Switch S_8	0	0	0
Diode D_1	0	0	1
Diode D_2	0	0	1
Diode D_3	0	0	0
Diode D_4	0	0	0
Diode D_5	0	n^2	n^2
Diode D_6	0	n^2	n^2
Diode D_7	n^2	n^2	n^2
Diode D_8	n^2	n^2	n^2

the turns ratio of the transformer. If the power transfer is negative, the current through the diodes should be swapped with the current through the semiconductor switches.

4.2.3. Zero voltage switching

In order to identify the switching losses, the previously used sketch of the semiconductor currents can be investigated. Looking at the turn on transition, it can be seen that the current always starts from zero. However, there are always four switches turning off at a nonzero current, namely S_1 and S_2 on the primary (input) side and S_3 and S_4 on the secondary (output) side. These two primary side switches turn off at a current of $I_{L,2}$ and the two secondary side switches turn of a current of $n \cdot I_{L,1}$. The remaining four switches turn off at zero current, which will result in a negligible switching loss.

If the soft switching performance of the three current modulation techniques discussed is compared, the result given in Table 4.5 is obtained [11]. ZVS means only Zero Voltage Switching and ZVZCS means it is switching at both Zero Voltage and Zero Current. It should hereby be noted, that for the rectangular current modulation scheme, it is assumed the converter is operating in the soft switching range, as was discussed in Section 3.5.

Table 4.5: Soft switching behaviour under the three described current modulation schemes

	Turning on		Turning off	
Modulation method	ZVS	ZVZCS	ZVS	ZVZCS
Rectangular	0	8	8	0
Triangular	0	8	2	6
Trapezoidal	0	8	4	4

4.2.4. Transferred power

With the voltages and currents known, the equation for the power transfer can be derived. The inductor current is taken during the first half period and multiplied with the voltage V_{in}. During interval T_3 the voltage is zero, so that part can be left out of the integral. To obtain the power, Equation (4.48) should be used.

$$P = \frac{2}{T_s} V_{in} \left(\int_0^{T_1} \frac{V_{in}}{L} t\,dt + \int_{T_1}^{T_1+T_2} \frac{V_{in}}{L} T_1 + \frac{V_{in} - n \cdot V_{out}}{L} (t - T_1)\,dt \right) \tag{4.48}$$

Working out the integral results in Equation (4.49).

$$P = \frac{V_{in}}{T_s L}\left(V_{in}(T_1+T_2)^2 - n\cdot V_{out}T_2^2\right) \tag{4.49}$$

Using Equation (4.39) and Equation (4.41) the power can be expressed as function of the phase shift, which is done in Equation (4.50). This formula is slightly modified to accept both a positive and negative phase shift, for either a positive or negative power transfer.

$$P = \text{sign}(\phi)\cdot\frac{n\cdot V_{out}}{4\pi^2 f_s L V_{in}}\left(4\phi^2(V_{in}n\cdot V_{out} - (V_{in}+n\cdot V_{out})^2) + 4\pi|\phi|(n\cdot V_{out})^2 + \pi^2(n\cdot V_{out}(V_{in}-n\cdot V_{out}))\right) \tag{4.50}$$

More interesting is calculating the required phase shift for a certain level of power transfer. This can be done by expressing the phase shift as function of power, starting by Equation (4.50). To solve this, one should rewrite it in a form of $a\phi^2 + b\phi + c = 0$, in which it is already almost written. Then, the ABC-formula of Equation (4.51) can be used and should be solved.

$$\phi = \frac{-b \pm \sqrt{b^2-4ac}}{2a} \tag{4.51}$$

After carefully working out, one can obtain two solutions for ϕ. Selecting the right one and rewrite for both ways of power flow will result in Equation (4.52).

$$\phi = \text{sign}(P)\cdot\frac{(n\cdot V_{out})^3 - \sqrt{V_{in}^3(n\cdot V_{out})^3 - 4|P|f_s L\left(V_{in}(n\cdot V_{out})^3 + V_{in}^2(n\cdot V_{out})^2 + V_{in}^3(n\cdot V_{out})\right)}}{\frac{2}{\pi}n\cdot V_{out}\left((n\cdot V_{out})^2 + n\cdot V_{out}V_{in} + V_{in}^2\right)} \tag{4.52}$$

Next, the trapezoidal current modulations has limits on the power transfer, both a minimum and a maximum level of power transfer. Starting with the minimum amount of power transfer. For this, a distinction is made based on the voltage levels. For $V_{in} > n\cdot V_{out}$, note that there is no special limit. If $\phi = 0$, the trapezoidal current waveform changes into a triangular waveform. This does however not mean the minimum amount of power transfer if equal to zero in this region. The minimum amount of transferable power can be found by plugging $\phi = 0$ into Equation (4.50), of which the result is given in Equation (4.53).

$$P_{trap,min} = \frac{n\cdot V_{out}}{4\pi^2 f_s L V_{in}}\left(\pi^2(n\cdot V_{out}(V_{in}-n\cdot V_{out}))\right) \tag{4.53}$$

Next, the region of $V_{in} < n\cdot V_{out}$ is reviewed. Here the restriction $T_3 > 0$ applies. Rewriting this restriction in terms of T_1 using Equation (4.40) and then in terms of the phase shift using Equation (4.41) will result in the limit given in Equation (4.54).

$$\phi > \frac{\pi}{2}\cdot\left(1 - \frac{V_{in}}{n\cdot V_{out}}\right) \tag{4.54}$$

This may look familiar, since this is the same limit on the phase shift for the maximum power transfer in triangular mode. Also, the exact power level is the same; so the maximum transferable power in triangular mode is equal to the minimum amount of transferable power on the trapezoidal mode. This minimum amount of power is given in Equation (4.55).

$$P_{trap,min} = \frac{V_{in}^2(n\cdot V_{out} - V_{in})}{4n\cdot V_{out}f_s L} \tag{4.55}$$

Furthermore the maximum amount of power transfer is interesting. Looking back to Equation (4.50) where the power is expressed as function of the phase shift, the maximum power transfer can be found by differentiating and setting $\frac{dP}{d\phi} = 0$. Differentiating with respect to the phase shift will result in Equation (4.56).

$$\frac{dP}{d\phi} = \frac{n\cdot V_{out}}{4\pi^2 f_s L V_{in}}\cdot\left(8\phi\left(V_{in}n\cdot V_{out} - (V_{in}+n\cdot V_{out})^2\right) + 4\pi(n\cdot V_{out})^2\right) \tag{4.56}$$

This will result in a phase shift for maximum power transfer of Equation (4.57).

$$\phi_{maxP} = \frac{\pi(n\cdot V_{out})^2}{2\left((n\cdot V_{out})^2 + V_{in}nV_{out} + V_{in}^2\right)} \tag{4.57}$$

Substituting this result back into the equation of the power and the maximum transferable power is obtained in Equation (4.58).

$$P_{max} = \frac{(n \cdot V_{out})^2}{4 f_s L V_{in}} \cdot \left(\frac{(n \cdot V_{out})^3}{(n \cdot V_{out})^2 + V_{in} n \cdot V_{out} + V_{in}^2} + V_{in} - n \cdot V_{out} \right) \tag{4.58}$$

Now several different inductor current modulation techniques are discussed, it makes sense to compare them all in one plot. This plot is given in Figure 4.15. In this plot, a turns ratio of $n = 1$ is chosen with an input

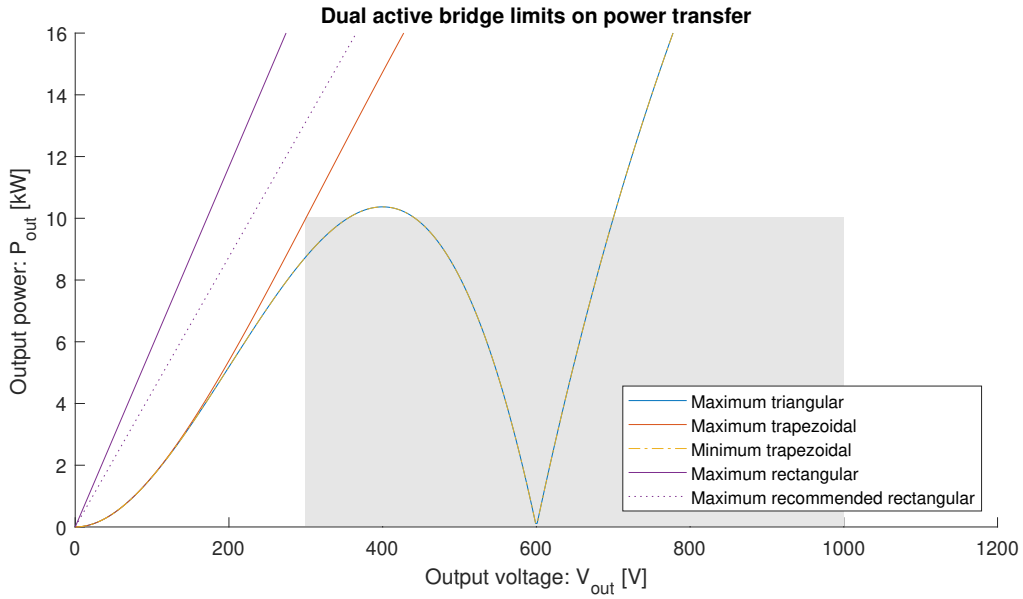


Figure 4.15: Limits on power transfer for different modulation techniques

voltage of 600 V. The inductance and switching frequency are chosen in such a way a power transfer of 10 kW is possible at an output voltage of 300 V. The area in grey indicates the limits as given by the requirements in Section 1.3. As can be seen, the maximum power transfer in triangular mode is equal to the minimum power transfer in trapezoidal mode. For the lower output powers triangular modulation can be chosen, while above the maximum the trapezoidal current modulation is an alternative. For comparison, also the limits of the rectangular current modulation are given, which has the largest power transfer capability. The second maximum of the rectangular modulation, indicating the recommended limit, limits the phase shift to $\frac{\pi}{4}$ in order to limit the amount of circulating power in the circuit as explained in Chapter 3.

4.2.5. Simulations

To verify the simulation results the same standard circuit of the dual active bridge is used, of which the electrical circuit is again given in Figure 4.16. The control logic for the trapezoidal current modulation is less complex compared to the triangular current modulation and given in Figure 4.17. To cover all operating modes (power flow in both directions and both an input voltage smaller than, equal to and greater than the output voltage), the parameters given in Table 4.6 are set. In order to transfer with the given parameters 10 kW of power at an output voltage of 550 V, the requires phase shift can be calculated using Equation (4.52) and will be equal to 0.1948. Using this value in the simulation for the phase shift and analysing the waveform will result in a power transfer of 10.0 kW, which is as expected, just as the shape of the waveform depicted in Figure 4.18a. The next case, in which the input and output voltages are the same is considered. For triangular current modulation, no power transfer was possible in this case, but with trapezoidal current modulation there is. The phase shift is calculated and should be 0.2213. The simulated waveforms are given in Figure 4.18b and the power transfer is again 10.0 kW. Next the last case is inspected, with an output voltage larger than the input voltage. In this case a phase shift of 0.2552 is required in order to have a power transfer of 10.0 kW. The simulations show again a power transfer of 10.0 kW and the waveforms look as expected. In Figure 4.18 the waveforms are given for power transfer in the forward direction (from input to output). For the power flow in the opposite direction the current waveform will each half period be flipped along the x-axis

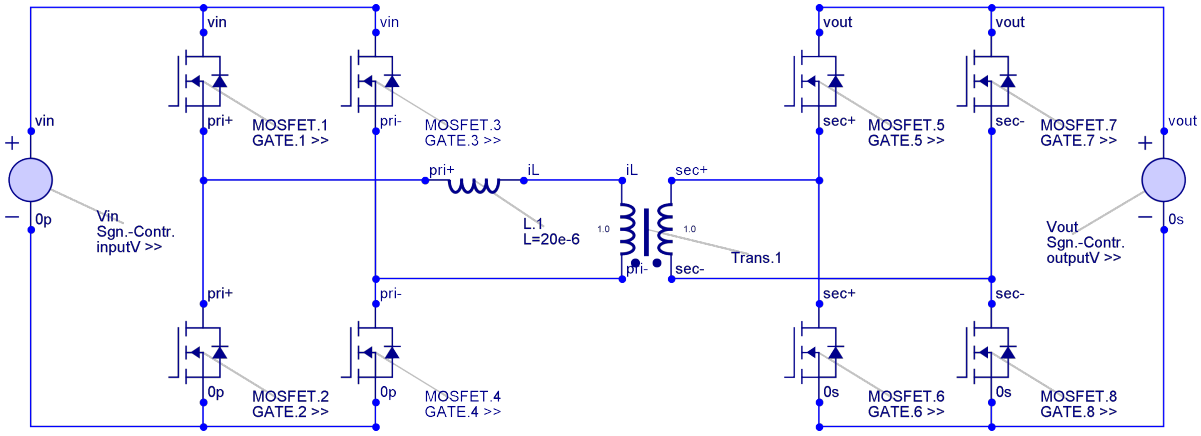


Figure 4.16: The electrical circuit of the DAB (trapezoidal mode) in Gecko Circuits

Table 4.6: Parameters for the simulation of the equivalent DAB in trapezoidal mode

Parameter	Value
Input voltage V_{in}	600 V
Output voltage V_{out}	550 V, 600 V & 650 V
Transformer turns ratio $n:1$	1
Switching frequency f_s	100 kHz
Inductance L	20 µH
Transferred power P_{out}	±10.0 kW

and the y-axis. This means the durations of the intervals are consecutively T_3, T_2, T_1, T_6, T_5 and T_4. Two waveforms of negative power flow are given in Figure 4.19, again with an output voltage of 550 V in Figure 4.19a for comparison and one with an output voltage of 650 V in Figure 4.19b.

All in all it can be concluded that the calculations done under the trapezoidal current modulation were correct.

4.2.6. Extension

As discussed before, the trapezoidal current modulation has a minimum on the to be transferred power. However, with a slight modification it is possible to keep working with a trapezoidal current waveform while the output power is lower. This can be done by adding a *zero voltage time* in between intervals 3 and 4 (and symmetrically between interval 6 and 1). In this interval, the current through the inductor remains zero for a while. This interval starts when the current naturally went to zero at the end of the third interval. Having this extra interval, one has an extra degree of freedom and it is possible to have a reduced power transfer with a trapezoidal current waveform. The downside of this is that the converter switches are operating with reduced soft switching characteristics compared to using the triangular current modulation (see Table 4.5). The advantage is in the lowered peak value of current. Finding out whether it is better to use the trapezoidal current modulation with a zero voltage time of a triangular current modulation scheme depends on the losses generated by switching and conduction. For now, this type of modulation is not discussed, but it can be easily added later given the similarities with the trapezoidal current modulation discussed previously.

4.3. Summary

In this chapter the triangular and trapezoidal current modulation are investigated. Equations are derived for the duration of all intervals, instantaneous current, RMS current, power and phase shift. The analytical results were verified by performing simulations on a computer. Furthermore the limits on minimum and maximum power transfer were derived for both modulation schemes and it was concluded that both triangular and trapezoidal current modulation should be used to cover the complete output region. For the lower loads the triangular current modulation will be used, which will go over in a trapezoidal current modulation if more power is required.

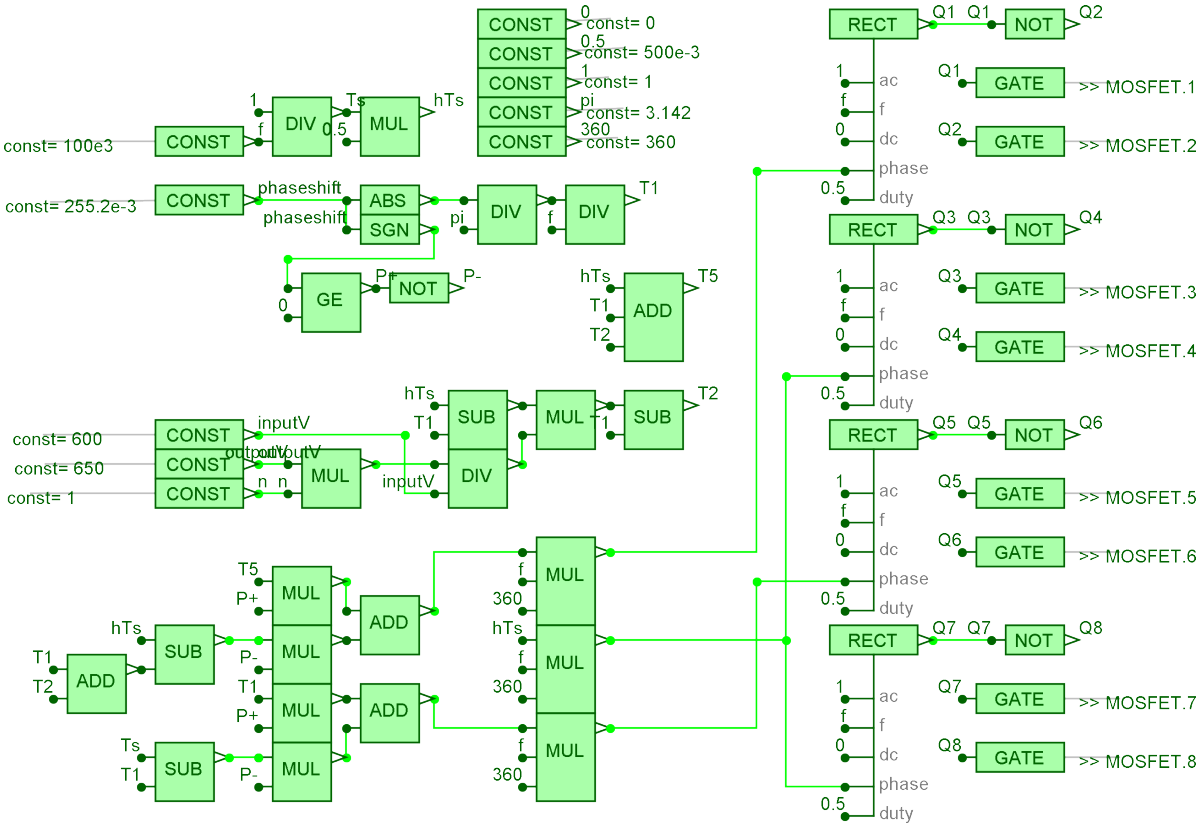
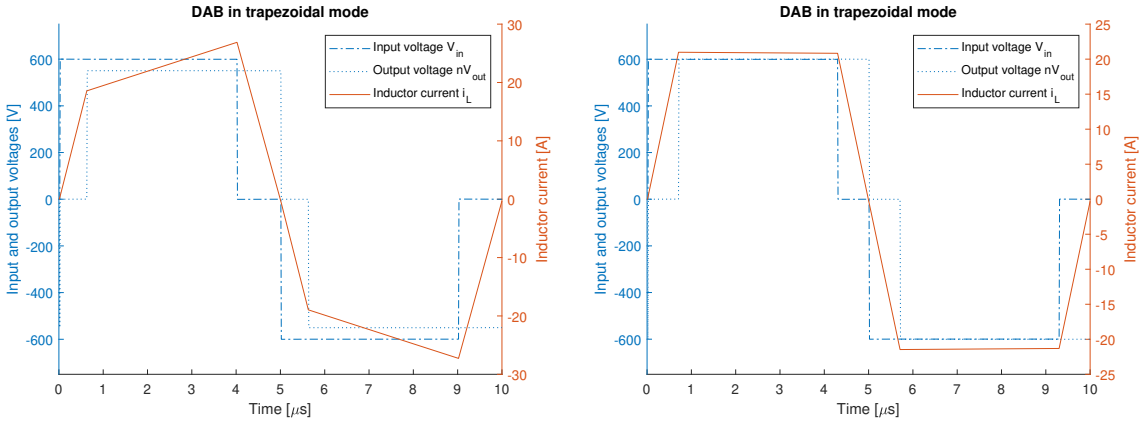


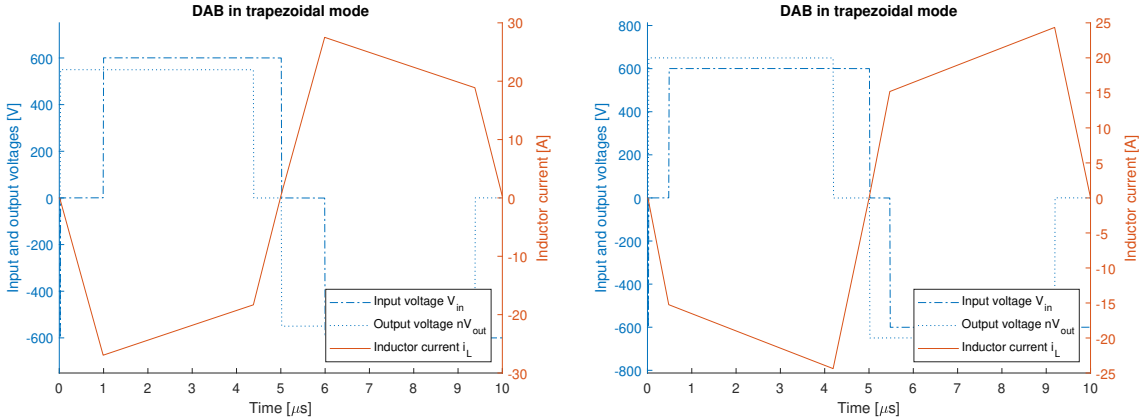
Figure 4.17: The control logic of the DAB (trapezoidal mode) in Gecko Circuits



(a) Output voltage of 550 V

(b) Output voltage of 600 V

Figure 4.18: Simulated waveforms under trapezoidal current modulation with positive power flow



(a) Output voltage of 550 V

(b) Output voltage of 650 V

Figure 4.19: Simulated waveforms under trapezoidal current modulation with negative power flow

5

Design: switches

Now the topology of the converter and the corresponding modulation techniques are clear, the design of the actual DAB converter can start. In this first chapter about the design, the switches will be chosen. However, before this can be done, the turns ratio of the transformer must be known, which determines the amount of current flowing through the switches. So prior to choosing the switches the best turns ratio will be investigated.

Contents in this chapter

5.1. Turns ratio transformer

As mentioned in the introduction above, the turns ratio of the transformer must be set first. Recall that this transformer was present in the circuit to provide galvanic isolation, but since it is there it gives an extra degree of freedom for the design. It is expected that most of the losses that occur in the converter are related to the current which is flowing. Therefore, for choosing the turns ratio the goal is to minimise the RMS currents in the circuit. In the previous chapter the formulas for the RMS currents in the inductor were given under different modulation schemes. Given that the inductor is placed in series with the transformer, the current is the same. The current in the secondary turns of the transformer has to be scaled with the turns ratio, as given in Equation (5.1).

$$I_{sec} = n \cdot I_{pri} \tag{5.1}$$

5.1.1. Algorithm

As was stated in the requirements, the converter must operate in a wide output voltage range, as well as be able to deliver power up to 10 kW. To find the best turns ratio, a script is written and using Matlab the best solution is eventually found.

Firstly, an initial turns ratio n is set and then the product of frequency and inductance $f_s L$ is calculated in such a way a total power transfer of 110 % of the required value is possible. This is chosen, because up till now all formulas derived were for the ideal (lossless) case. To make sure the converter is able to deliver the required power in presence of losses, this higher value of maximum power transfer is chosen for design.

Next, the maximum RMS and maximum peak current will be calculated. For this, multiple points in the complete spectrum will be evaluated. This means output voltages within the range of 300 V up to 1000 V (intervals of 5 V) and output powers within the range of 0 W up to 11 kW (intervals of 10 W).

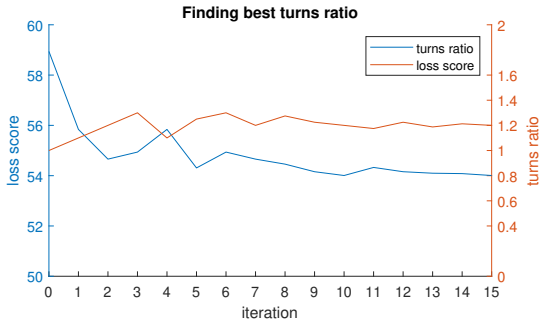
To determine the *score* of the evaluated turns ratio n, the current must be as low as possible. For this, the primary and secondary currents have the same weight, as well as the RMS current and the peak current.

After the *score* of one turns ratio is calculated, the turns ratio will either be increased or decreased. This is based on the result of the previous results. If the losses are decreasing if the turns ratio also was decreasing, the turns ratio will again be decreased to see if the losses are still decreasing. Otherwise, the turns ratio will be increased.

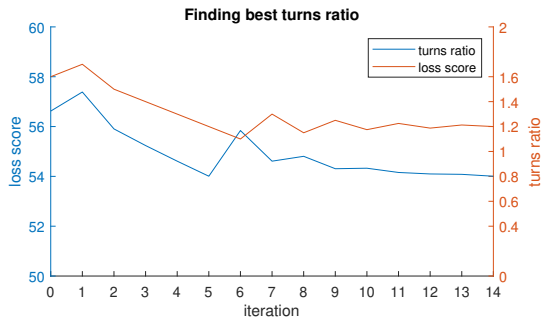
If the direction (increasing or decreasing turns ratio) is changed multiple times in a row, the step size in which the turns ratio is changing will be reduced until a certain threshold is reached. At that moment, the best turns ratio is found, which has the lowest expected losses based on how the *score* was defined.

5.1.2. Result

The script is executed with different values of turns ratio as initialisation and with different step sizes, to prevent ending up in a local minimum. The results of this procedure is given in Figure 5.1. As can be seen



(a) Turns ratio at initialisation: $n_{init} = 1.0$



(b) Turns ratio at initialisation: $n_{init} = 1.6$

Figure 5.1: Result of finding the best turns ratio

in the plot, the best turns ratio equals 1.2. A graphical representation of the RMS and peak current for this specific turns ratio is given in Figure 5.2. The darker the colour, the higher the value of the current. Note that this is the current on the primary side. One can conclude that the minimum current over the complete power output is at $V_{in} = n \cdot V_{out}$, so with an input voltage of 600 V this is at an output voltage of 500 V. At this output voltage the converter works only in trapezoidal mode. The larger the mismatch between input voltage and reflected output voltage across the inductor, the higher the RMS and peak currents will be, with the highest currents in the top left (trapezoidal mode) and the top right (triangular mode). A more detailed view of the modulation scheme at each point is given in Figure 5.3.

5.2. MOSFET and IGBT

Next, two switches will be chosen; one MOSFET and one IGBT. Both switches will be chosen based on the availability (at `https://www.digikey.com/`) and minimum requirements. Some specifications that must be met are listed below:

- Drain-source or collector-emitter voltage of 1200 V, slightly higher than the ideal maximum situation of 1000 V on the secondary side. This leaves some headroom for any possible small voltage spikes;
- Current capability of at least 70 A. The peak calculated current on the primary side is around 55 A and about 66 A at the secondary side. With a margin added the MOSFET or IGBT should at least withstand a current of 70 A;
- Furthermore, for placing the device on the printed circuit board (PCB) the switch should have a package of either *TO 247-3* or *TO 247-4*.

With filters applied, from the remaining list of switches there will be devices chosen based on low conduction losses (for a MOSFET this can be related to the value of $R_{DS,on}$). It must be noted, that the decrease in conduction is seen with respect to the increase in costs of the device.

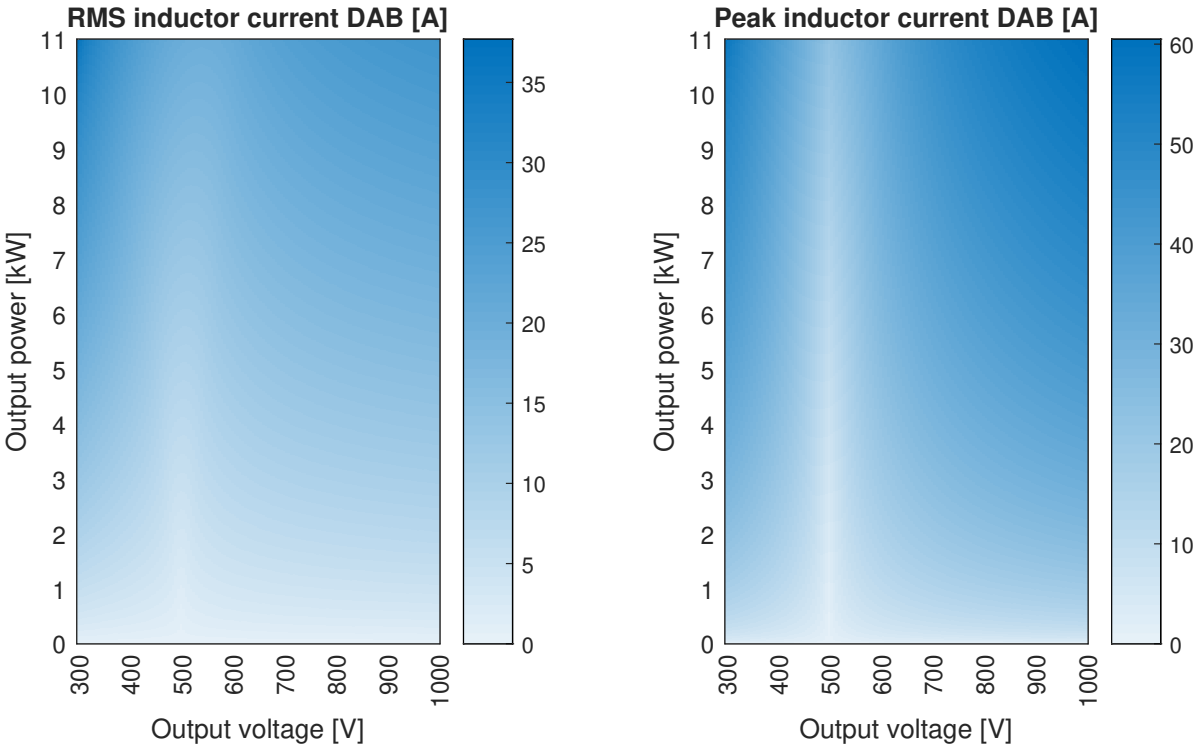


Figure 5.2: Heatmap of the RMS and peak current for a turns ratio of 1.2

Finally, the two switches that have been selected for further inspection are listed in Table 5.1. It must be

Table 5.1: Switches selected for further inspection

	MOSFET	**IGBT**
Manufacturer	Cree	Infineon
Model	C3M0021120k	IKQ75N120 CS6
Package	*TO 247-4*	*TO 247-3*
V_{DS}/ V_{CE}	1200 V	1200 V
I_D/ I_C (at 100 °C)	74 A	74 A

said, that the MOSFET is far more expensive (almost a factor 2.5 in March 2020) than the IGBT. Therefore, the IGBT will be preferred if the losses are manageable, even though there was no requirement specifying the costs of the complete converter.

5.3. Estimating conduction losses

With the devices chosen, the losses in the semiconductors will be estimated, starting with the conduction losses. These conduction losses are relatively easy to calculate and they are also independent of the chosen switching frequency.

5.3.1. MOSFET

The conduction losses of the MOSFET are found in the datasheet [27]. Using the provides figures, for a temperature of 25 °C an on-resistance of 21 mΩ is found. The influence of the drain to source current is very limited, less than 1 mΩ in until 50 A, where the maximum RMS current on the secondary side was no more than 43 A. This means the conduction losses of the MOSFET can be calculated according to Equation (5.2):

$$P_{MOSFET,cond.} = R_{DS,on} \cdot I_{RMS}^2 \tag{5.2}$$

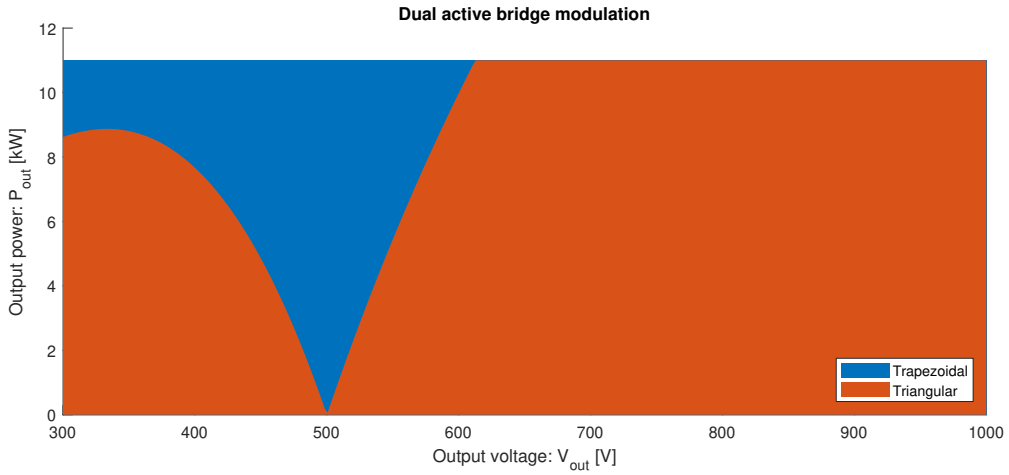


Figure 5.3: Modulation technique at every output voltage and every output power

However, there is a slight dependence on temperature. Using the curve fitting toolbox from Matlab, the dependency in Equation (5.3) is found for the temperature on the resistance.

$$f_T = 2.10 \times 10^{-5} \cdot T_j^2 + 6.11 \times 10^{-4} \cdot T_j + 0.98 \tag{5.3}$$

For a junction temperature of $T_j = 120\,°C$, this per unit scaling factor will be 1.36 so that the total on resistance $R_{DS,on}$ will be 29 mΩ. The RMS currents in each semiconductor were already given in Chapter 4. For the conduction of current in the anti-parallel diode, the forward voltage is about 4.4 V [27], which is quite high. However, using the concept of synchronous rectification [28] the resulting losses for conducting current in the opposite direction can be reduced significantly. With synchronous rectification, the gate of the MOSFET is activated so that only the on-resistance of the MOSFET has to be considered. Referring back to the control logic in both modulation schemes, it can be seen that the gates were also set high during the conduction of current in the opposite direction in the MOSFET. This means this principle of synchronous rectification can easily be used. In short, the conduction losses for a reverse current flow can also be calculated using Equation (5.2).

5.3.2. IGBT

For the IGBT, the conduction losses are slightly different. Here, there is not only an on-resistance between the collector and emitted while conducting, but there is also a forward voltage drop across the collector and emitter. Based on the figures in the datasheet [29], an on resistance of roughly 13 mΩ is found with a forward voltage drop of 1.0 V, both at a temperature of 100 °C. The power loss in the IGBT can then be calculated using Equation (5.4):

$$P_{IGBT,cond.} = R_{CE,on} \cdot I_{RMS}^2 + V_{CE,fw} \cdot I_{AVG} \tag{5.4}$$

In this equation, $R_{CE,on}$ is the on-resistance of 13 mΩ and $V_{CE,fw}$ is the forward voltage drop of the IGBT of 1.0 V. For an IGBT, there is no such thing as synchronous rectification possible. If the IGBT has to conduct current in the opposite direction, the anti-parallel will carry the current. From the datasheet the forward voltage and resistance and again found, and for the conduction of current in the opposite direction the losses are as described in Equation (5.5):

$$P_{IGBT,rev.cond.} = R_{D,on} \cdot I_{RMS}^2 + V_{D,fw} \cdot I_{AVG} \tag{5.5}$$

Where the derived on-resistance of the internal anti-parallel diode $R_{D,on}$ is equal to 5 mΩ and the forward voltage drop $V_{D,fw}$ is 2.1 V.

5.4. Estimating switching losses

The second part of losses in the semiconductors is for the switching losses. As concluded in Section 4.2.3, it is said that the turning on losses of the switches is negligible. However, losses at switching off are still present. This section will investigate these turning off losses for both the MOSFET and IGBT.

5.4.1. MOSFET

The datasheet of the MOSFET [27] has given two figures with the switching loss in Joules as a function of drain to source current. One figure for a voltage V_{DD} of 600 V and one for 800 V. A look is taken to the curve of 600 V first, because that is the voltage on the primary side and on the secondary side this voltage is a reasonable average between 300 V and 1000 V. Several points on the graph are copied and using the curve fitting toolbox of Matlab a second order polynomial is found for the turn off losses. This fitted curve for the turning off losses is given in Equation (5.6):

$$E_{MOSFET,turn-off} = 5.89 \times 10^{-8} \cdot I_{turn-off}^2 + 5.32 \times 10^{-7} \cdot I_{turn-off} + 1.70 \times 10^{-5} \tag{5.6}$$

A plot of these losses is given in Figure 5.4. Since the switching losses are not only dependent on the current,

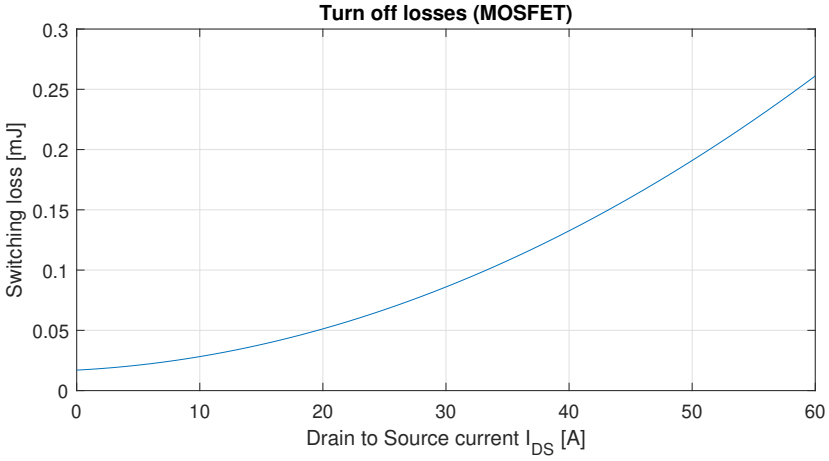


Figure 5.4: Turn off losses of the inspected MOSFET at $V_{DD} = 600$ V

also a correcting factor for the voltage is taken into account. This is based on both figures provided for V_{DD} of 600 V and 800 V. For this a function with a power is chosen, with the coefficients as given in Equation (5.7).

$$f_V = 7.16 \times 10^{-5} \cdot V^{1.49} \tag{5.7}$$

So the new approximation of the turning off losses is given by Equation (5.8):

$$E_{MOSFET,turn-off,new} = f_V \cdot E_{MOSFET,turn-off} \tag{5.8}$$

If one might remember an equivalent circuit model of a MOSFET, there are several parasitic capacitances present. As in the model in Figure 5.5, there are capacitances placed between each of the pins. A capacitance between drain and source (C_{ds}), between drain and gate (C_{dg}) and between gate and source (C_{gs}). In the datasheet, these values are not directly given, but combinations, among others the output capacitance (C_{oss}) which is defined as in Equation (5.9) [30].

$$C_{oss} = C_{ds} + C_{gd} \tag{5.9}$$

The parasitic output capacitance helps reducing the turning off losses. This is because when the switch turns off, remaining current can continue to flow to charge this parasitic capacitance. In this way the parasitic capacitance behaves as a kind of turn off snubber. The amount of energy stored in the output capacitance C_{oss} depends on the drain to source voltage, of which the relation is given in the datasheet [27]. Again, a relation is derived by curve fitting in Matlab and the resulting second order polynomial is given by Equation (5.10):

$$E_{oss} = 7.9 \times 10^{-11} \cdot V^2 + 2.12 \times 10^{-8} \cdot V + 7.84 \times 10^{-7} \tag{5.10}$$

The amount of stored energy is also plotted in Figure 5.6. The amount of energy that can be stored in the output capacitance will not be dissipated as heat in the MOSFET during turning off. So this reduces the losses at turning off. The power loss is given in Equation (5.11), this is of course dependent on the number of times a device is switching a second, hence the switching frequency is present in this equation.

$$P_{MOSFET,turn-off} = \left(E_{MOSFET,turn-off,new} - E_{oss}\right) \cdot f_s \tag{5.11}$$

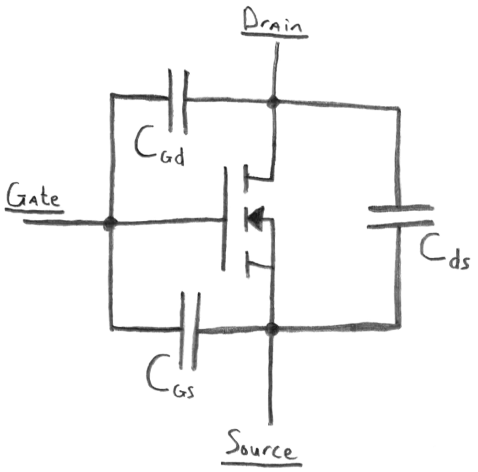


Figure 5.5: An equivalant circuit model of a MOSFET with parasitic capacitances

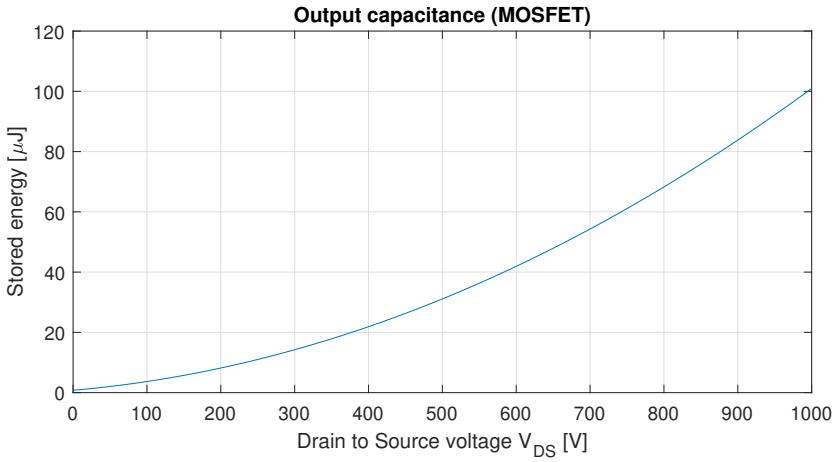


Figure 5.6: Stored energy in the output capacitance C_{oss} of the MOSFET

The corresponding output voltage is equal to the input and output voltage for the primary and secondary side respectively, while the current is at the moment the switch turns off. Equations for these peak values were given in Chapter 4. The influence of the junction temperature on the turn off losses is according to the datasheet negligible.

5.4.2. IGBT

A similar approach is followed for the switching losses of the IGBT. The switching losses as a function of current is investigated first using a graph from the datasheet [29]. The resulting relation between switching energy losses and collector current is found by curve fitting and given in Equation (5.12):

$$E_{IGBT,turn-off} = 6.53 \times 10^{-5} \cdot I_{turn-off} + 5.00 \times 10^{-4} \tag{5.12}$$

As can be seen, now a first order polynomial was sufficient to describe the behaviour. A plot of the losses is given in Figure 5.7. However, these switching losses depend on the junction temperature, which is not constant. Therefore, a scaling factor for this dependency is introduced in Equation (5.13).

$$f_T = 9.906 \times 10^{-6} \cdot T_j^2 + 1.011 \times 10^{-3} \cdot T_j + 5.254 \times 10^{-1} \tag{5.13}$$

Another graph is given in the datasheet which gives the relation between voltage (between collector and emitter) and the turn off switching energy loss. This graph is used to scale the results of the current dependent turn off energy, just as done for the MOSFET. The voltage scaling factor is given by Equation (5.14):

$$f_V = 5.77 \times 10^{-3} \cdot V^{0.806} \tag{5.14}$$

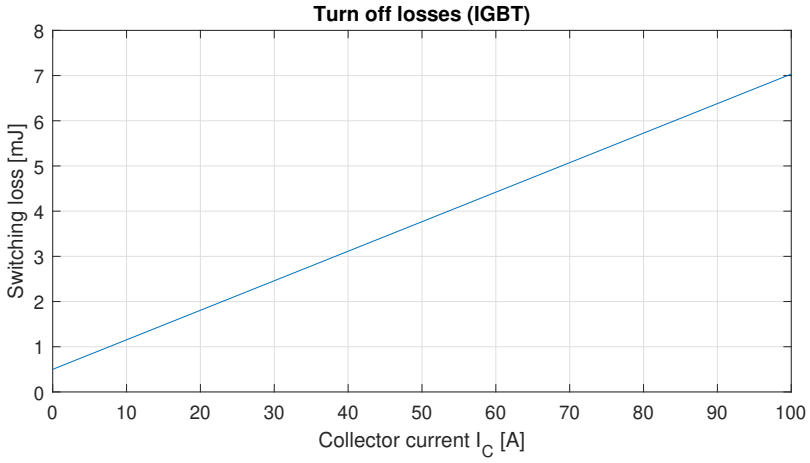


Figure 5.7: Turn off losses of the inspected IGBT at $V_{CE} = 600\,\text{V}$

The new approximation of switching energy loss is then given by Equation (5.15):

$$E_{IGBT,turn-off,new} = f_T \cdot f_V \cdot E_{IGBT,turn-off} \tag{5.15}$$

The output capacitance C_{oes} of the IGBT is comparable to the C_{oss} for the MOSFET. However, no graph was given in the datasheet showing the energy loss E_{oes} as function of the voltage. Therefore, the graph of the output capacitance C_{oes} as a function of the voltage is used for curve fitting. This resulted in Equation (5.16):

$$C_{oes} = 1.43 \times 10^{-9} \cdot V_{CE}^{-0.426} \tag{5.16}$$

Then, knowing the relation of Equation (5.17), a polynomial for the stored energy in the output capacitance is obtained and shown in Equation (5.18).

$$E = \frac{1}{2} \cdot C \cdot V^2 \tag{5.17}$$

$$E_{oes} = 1.00 \times 10^{-10} \cdot V^2 + 2.00 \times 10^{-9} \cdot V - 2.47 \times 10^{-9} \tag{5.18}$$

A note must be made, because this equation is based on data of V_{CE} between 0 V and 30 V since nothing else was available in the datasheet. Given the familiar shape of the curve, this data is now extrapolated for use in the region of the to be designed converter. A plot is given in Figure 5.8. In the same way as with the MOSFET,

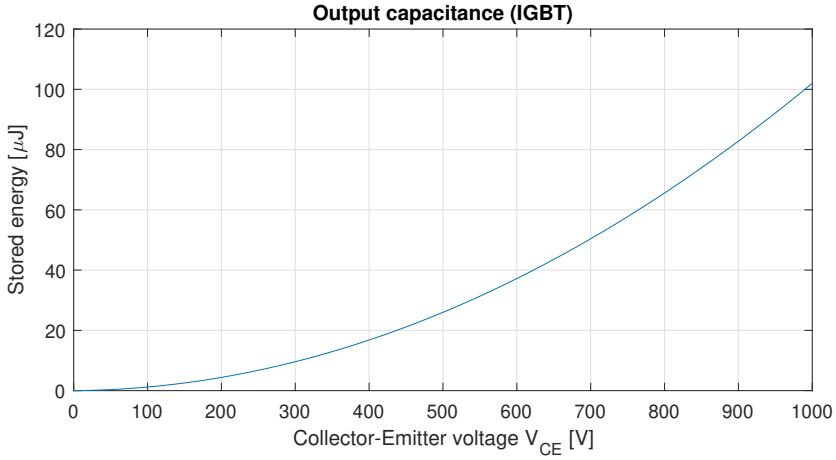


Figure 5.8: Stored energy in the output capacitance C_{oes} of the IGBT

the final equation for the IGBT turning off switching losses is given by Equation (5.19).

$$P_{IGBT,turn-off} = \left(E_{IGBT,turn-off,new} - E_{oes}\right) \cdot f_s \tag{5.19}$$

5.5. Maximum switching frequency

Now the two most important losses can be calculated, namely the conduction losses and switching losses, an estimation can be done on the total losses in a semiconductor. Given that the switching losses depend on the switching frequency, the total losses are also dependent on the switching frequency. If a maximum is set on the power dissipation of a switch, the maximum frequency can be determined. The maximum power dissipation is in this case limited by the temperature. The maximum temperature of the junction is set to 135 °C. The heat sink, that will be mounted on the switches for cooling, can be hold at a temperature of 100 °C. Later on in the design phase, the exact type of heat sink and eventual additional fans will be chosen. For now it is said that this part will be able to keep the temperature at 100 °C. The temperature difference between the junction (of the semiconductor) and the case (which will be mounted to the heat sink) can then be calculated using Equation (5.20).

$$\Delta T = T_j - T_c \tag{5.20}$$

The maximum power dissipation of a single semiconductor is then found by their thermal resistance of junction to case, $R_{\theta,j-c}$. These thermal resistance are given in the datasheets and listed in Table 5.2.

Table 5.2: Selected switches with their thermal resistances

	MOSFET	**IGBT**
Switch $R_{\theta,j-c}$	$0.32\,°CW^{-1}$	$0.17\,°CW^{-1}$
Diode $R_{\theta,j-c}$	$0.32\,°CW^{-1}$	$0.41\,°CW^{-1}$

If now the maximum switching frequency is calculated where the temperature difference between the junction and case of any semiconductor will not exceed the 35 °C, the maximum frequencies are found. For the MOSFET, the maximum switching frequency is around the 150 kHz, which is quite high. For the IGBT, the maximum switching frequency is considerably lower, only 18 kHz.

Preferable switching frequencies are at leat above the 20 kHz, which is above the maximum audible frequency a human is able to perceive. Also, to avoid large filters to filter out electromagnetic interference (EMI) the switching frequency should be kept below 150 kHz. Third, it is advised to keep the switching frequency for now below 48 kHz. This is, because at a higher switching frequency it is more difficult to control, because it sets higher constrains on the timing of the controller for the converter.

Before the operating frequency is investigated further, a closer look to the losses can be taken by looking at Figure 5.9. However, before interpreting this figure requires some explanation. First of all, this is a plot at a power output of 10 kW at a switching frequency of 18 kHz. On the left side the values are given for the converter with IGBTs and on the right side with the MOSFETs. The two plots on top indicate a positive power transfer, in other words a power flow from Grid to Vehicle (G2V). The two lower plots indicate an opposite power flow, Vehicle to Grid (V2G). The losses are given at different output voltages between 300 V and 1000 V with intervals of 100 V. Each coloured *component* of a single bar, represents the maximum loss of all *four* semiconductors. For instance, looking at the top left plot (IGBT, G2V) to the output voltage of 300 V. The blue component represents 29 W of losses, corresponding to primary conduction in a switch. The orange component of the bar on top of it represents 31 W of losses, corresponding to primary conduction in a diode. These are both the maximum values of all four devices on the primary side, and this does not mean these losses occur in the *same* switch. The maximum conduction losses (both diode and switch) of one specific semiconductor is not 60 W, but this can not be concluded from these plots. So adding the values of individual bars does not give one any information.

Now it is clear how to read the figure, it is time to see if some conclusions can be drawn. One obvious one is that in case of positive power transfer there are more diode conduction losses on the secondary side (green component, this bridge rectifying) compared to an opposite power transfer where the diodes on the primary side have higher losses (orange component, now this side is rectifying). In the same way the differences between the blue and purple components about primary and secondary conduction in the switch can be explained. Another thing to note, is that both the switching losses (yellow and cyan components) are relatively lower for the converter with MOSFETs compared to the converter with IGBTs. This can be explained by the huge difference in turning off switching energy, while the stored energy due to the output capacitance is in the same order. Furthermore it can be seen that the losses in the MOSFET are a lot lower compared to the losses in the IGBT, which was also concluded looking at the maximum frequency that was possible.

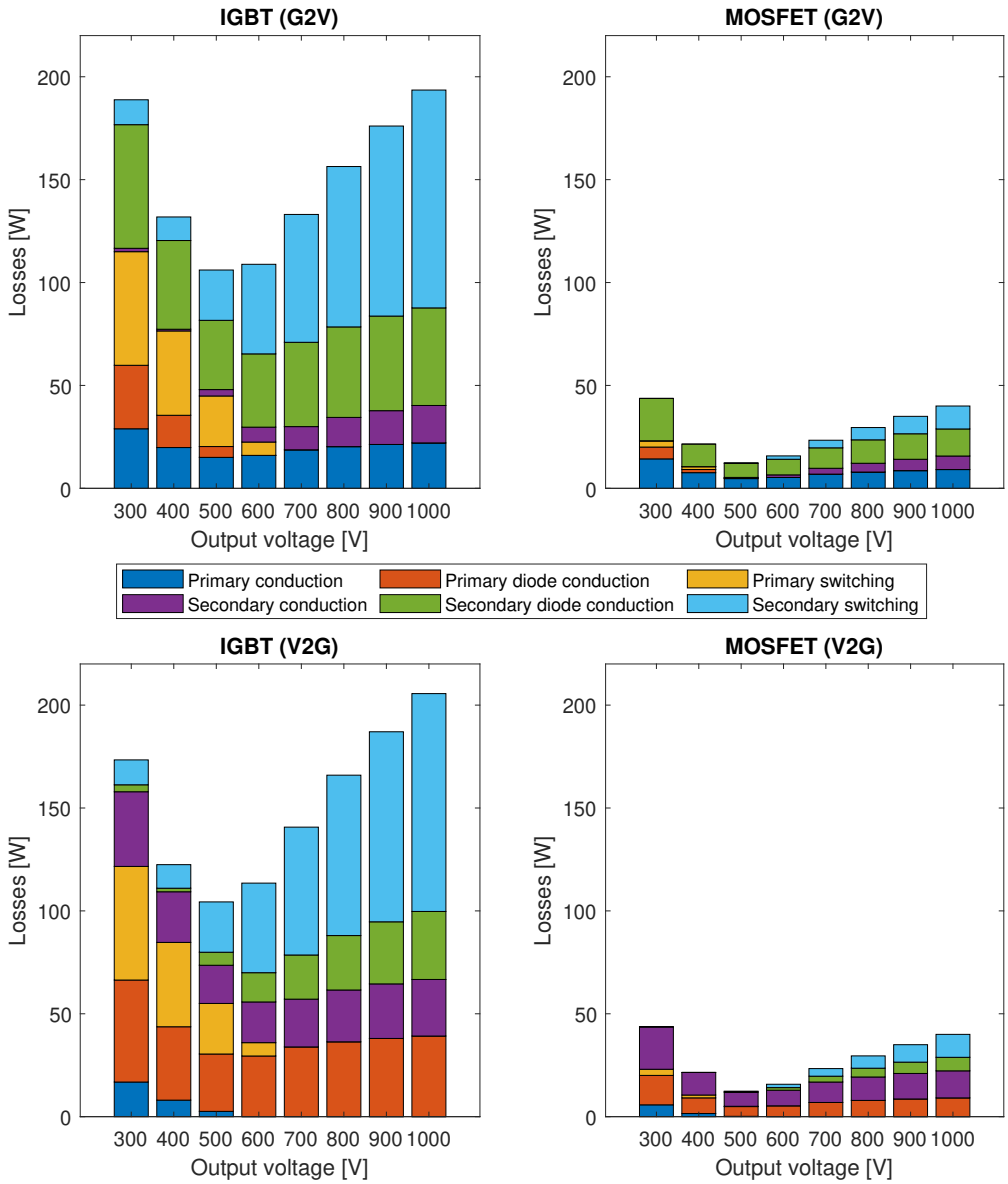


Figure 5.9: Maximum losses per component for IGBT and MOSFET at 18 kHz

Coming back to the preferred switching frequency range, which was between the 20 kHz and 48 kHz one can see that the converter which consists of IGBTs is unable to operate in this range because of thermal limitations. The operate the IGBTs in the preferred range, one or multiple measures could be taken:

- Adding an external antiparallel diode. As can be seen in Table 5.2, conduction losses of the internal antiparallel diode of the IGBT will lead to a relatively large increase in temperature. Using an external antiparallel diode, the internal one is not used, so does not generate any additional heat. However, in this case mainly the losses are moved to another component which also need to be cooled. If it is assumed that the extra required cooling capacity of the diode is no problem, the converter with IGBTs can achieve a switching frequency of 31 kHz.
- Placing multiple IGBTs in parallel. More or less the same idea as the previous one. Multiple IGBTs in

parallel will not reduce the total switching losses, but merely the switching losses per individual device. This makes the removing of heat more manageable. However, this will of course cause a significant increase in semiconductor costs. The difference in costs between two IGBTs in parallel and one MOSFET is then a lot smaller, while the MOSFETs have far less losses which will reduce costs in later stages of the design.

- Placing capacitors in parallel to the IGBTs. These capacitors can behave as a turn-off snubber, just as the parasitic C_{oes} did. This can somewhat increase the switching frequency, but one must take case of the following. If the parallel capacitance becomes too large and the converter is not able to discharge this capacitance in the period of dead-time, the assumption of zero voltage turning on is not valid any longer. Resulting in additional turning on losses.

All these measures will increase the costs of the total converter, making the gap between the more expensive version of the converter consisting of MOSFETs smaller. Except for the last measure, the total loss is mainly only spread more, which makes managing the dissipated heat easier. Therefore, it is chosen to use the MOSFETs in this converter. Their expected losses are lower, the heat sink can be smaller and cheaper and there is no need for more components.

The converter consisting of MOSFETs can cover the complete range of preferable switching frequencies, from 20 kHz up to 48 kHz. Since the conduction losses are independent of the switching frequency and the switching losses increase with switching frequency, the lowest switching frequency will result in the lowest semiconductor losses. However, also the magnetic components will contribute to the overall losses. Therefore, the inductor and transformer will be designed first before a final switching frequency is chosen. Because the design of the magnetic components depends on the switching frequency, the procedure will be as follows:

1. Choose a few different operating frequencies;
2. Design both magnetic components (inductor and transformer) for each frequency;
3. Estimate the losses of both the semiconductors and magnetic components at each of the chosen switching frequency.

Within the preferred switching frequency range, the following three different possible operating frequencies are chosen; 25 kHz, 35 kHz and 45 kHz. The design of the magnetic components will be described in the next chapter.

5.6. Summary

This chapter was the beginning of the actual design. Firstly, the turns ratio of the transformer was set, this was done using an algorithm that found the best turns ratio with the lowest currents. After this, two types of semiconductor switches were chosen; one MOSFET and one IGBT. For both devices equations were given to calculate the conduction losses and the turning off losses. Conduction losses for both the conduction phase of the switch and the conduction phase of the antiparallel diode. For the turning off losses, the parasitic capacitance across the switch was considered. Then, based on the thermal limits the maximum achievable switching frequency was set and this was compared to a preferred range. Based on the results, it was chosen to use the MOSFETs in the converter. The next step is to design the magnetic components at different frequencies and find the switching frequency which will give the lowest sum of both the semiconductor and magnetic losses.

To summarise the steps taken so far and the coming steps are all listed below:

1. Get the requirements of the converter clear (Chapter 1);
2. Choose a suitable topology for the converter (Chapter 2);
3. Select a modulation technique for the converter (Chapter 3 & Chapter 4);
4. Select the turns ratio of the transformer;
5. Select one or multiple switches;
6. Calculate the maximum switching frequency of the switches based on thermal constraints;

7. Define multiple possible operating frequencies;
8. Design the transformer and inductor for each defined frequency (Chapter 6);
9. Estimate the losses for each frequency of both the semiconductors and magnetic components (Chapter 6);
10. Set the switching frequency based on lowest estimated losses (Chapter 6).

Steps four up to seven were covered in this chapter and steps eight up to ten will be covered in the next chapter.

6

Design: magnetics

In the dual active bridge converter there are two magnetic components required. One transformer to provide the galvanic isolation and to set a possible change in voltage levels, and one inductor, which is responsible for the actual power transfer. The transformer will be designed first, because a practical transformer has a nonzero leakage inductance which will end up in series with the other inductor that has to be designed. After the transformer has been designed, the inductor will be next to bring the total series inductance of the leakage of the transformer and the inductor itself to the required value.

It is possible to leave out the separate inductor, and design the leakage inductance of the transformer in such a way it is equal to the required inductance.

Both the transformer and inductor will be designed for each of the three chosen switching frequencies in the previous chapter. Because of the similar procedure, this will only be explained for a switching frequency of 25 kHz. For the other two cases the final chosen parameters will be given later on in the chapter. Please pay attention to the symbols in this chapter, flux is denoted by ϕ, where this symbol was previously used for the phase shift. This is clarified by text in this chapter as much as possible.

Contents in this chapter

6.1. Transformer

In order to design a transformer, the design steps of [8] and [31] will be followed. This procedure starts with assembling the design inputs. For clarity, they are given below in Table 6.1. Where the rated primary voltage is equal to the input voltage V_{in} and the rated primary current is the maximum primary current in the complete operating range, for which 35 A is chosen, which was the maximum RMS current at 10 kW under the chosen turns ratio. The turns ratio was chosen in the previous chapter based on the lowest currents. For the surface temperature a commonly used value of 100 °C is used [8].

Table 6.1: Assembling design inputs of the transformer

Parameter	Value
Rated RMS primary voltage V_{pri}	600 V
Rated RMS primary current I_{pri}	35 A
Turns ratio n_{design}	1.2
Operating frequency f_s	25 kHz
Maximum body temperature T_s	100 °C
Maximum ambient temperature T_a	40 °C

Having assembled the design inputs, the voltage-ampere (VA) rating S can be computed using Equation (6.1). This will result in 21 kVA.

$$S = V_{pri} I_{pri} \tag{6.1}$$

6.1.1. Core selection

Before diving into the selection of the core, some background will be given about magnetics, starting with the law of Faraday in Equation (6.2).

$$V = N \cdot \frac{d\varphi}{dt} \tag{6.2}$$

Where the slope of the flux is represented by $\frac{d\varphi}{dt}$. Due to the bipolar flux excitation, the slope of the flux can be written as in Equation (6.3). Where ϕ_{min} and ϕ_{max} are the minimum and maximum flux in the core respectively, they are the same in magnitude, but with opposite sign ($\phi_{max} = -\phi_{min}$). Once per period both the minimum and maximum flux are reached.

$$\frac{d\varphi}{dt} = \frac{\phi_{max} - \phi_{min}}{T_s/2} = \frac{4\phi_{max}}{T_s} = 4\phi_{max} f_s \tag{6.3}$$

When Equation (6.2) and Equation (6.3) are combined, Equation (6.4) results:

$$V = 4N\phi_{max} f_s \tag{6.4}$$

Where ϕ_{max} can be written as the product of maximum flux density and effective core area, see Equation (6.5):

$$\phi_{max} = \hat{B} A_e \tag{6.5}$$

Also, the space in the window of the core can be expressed as in Equation (6.6).

$$N_{pri} A_{pri} + N_{sec} A_{sec} = k_w A_w \tag{6.6}$$

Here N_{pri} and N_{sec} are the primary and secondary number of turns respectively, and A_{pri} and A_{sec} their corresponding copper area of one turn. On the right side, k_w is the window fill factor which indicates the part of the window that is filled with copper. The remaining part is occupied by insulation. For solid wire, k_w is about 0.6, while for Litz wire k_w is only 0.35. A_w is the available window area obtained from the datasheet of a core.

For a transformer the relation $N_{pri} I_{pri} = N_{sec} I_{sec}$ holds, using this in Equation (6.6), as well as expressing the currents in current densities as in Equation (6.7) will lead to Equation (6.8).

$$J = \frac{I}{A} \tag{6.7}$$

$$N_{pri} = \frac{k_w A_w J}{2 I_{pri}} \tag{6.8}$$

Here, J is the copper current density. If Equation (6.4), Equation (6.5) and Equation (6.8) are combined and rewritten, Equation (6.9) follows.

$$A_e A_w = \frac{V I_{pri}}{2\hat{B} f_s k_w J} = \frac{S}{2\hat{B} f_s k_w J} \tag{6.9}$$

With Equation (6.9) clear, the selection on the core material and size can start. Firstly, take a look at the variables in that equation. The effective core area A_e and the window area A_w depend of course on the shape and size of the core. The VA-rating S is set by design, just as the switching frequency f_s. Given the relative high switching frequency and large currents, for now Litz wire will be chosen so k_w is also set. Later on in the design, it might be that solid wire is a better choice, in that case the result can vary by at most a factor two. The current density is set to $4.0\,\mathrm{A\,mm^{-2}}$. The maximum flux density $\hat{B}$ will be set by the core material. So with some values known by design constrains, several cores with different A_e, A_w and $\hat{B}$ can be reviewed, to see which one has the best match.

In the ideal situation, a core database is present with all values listed. But as it happens, it was not. Therefore a small core database was made, from selected cores listed in [32]. Several E-cores were included, as well as some UI-cores and some stacked versions. This core database is created using Microsoft Excel and can be found in Appendix C.

As can be seen, for nearly all cores the material can be chosen; either *N27* or *N87*. To find out which core material will perform best in the situation, the performance factor [8] is taken into account. This performance factor can be expressed as in Equation (6.10) and is usually given as function of frequency.

$$PF = f_s B_{ac} \tag{6.10}$$

The performance factor of a material is proportional to the VA-rating of the transformer. So it is said the higher the value of the performance factor, the better the performance of the core material. With aid of the TDK Ferrite Magnetic Design Tool [33], the plots for the performance factors of both materials are obtained and given in Figure 6.1. The commonly used maximum temperature of 100 °C is used, and for the power

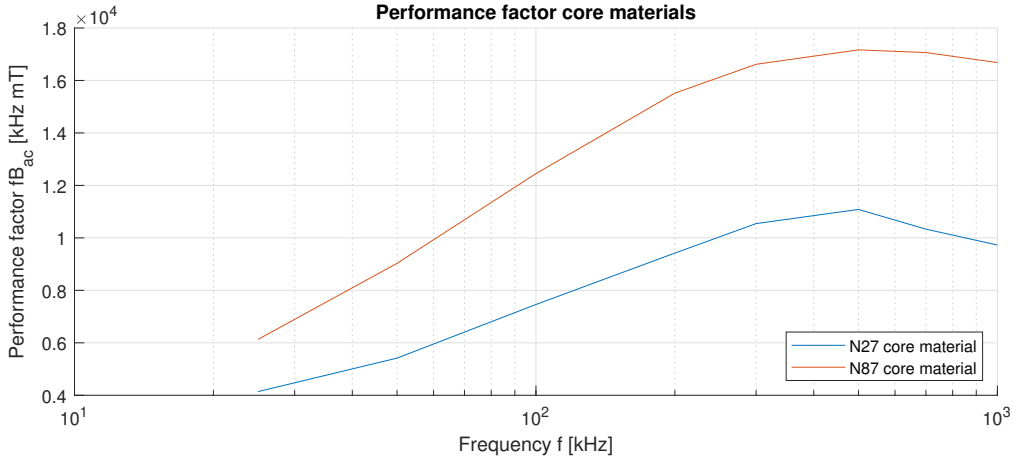


Figure 6.1: The performance factor of different core materials

density P_{core} a value of $100\,\mathrm{mW\,cm^{-3}}$ is used. The figure shows, that the N87 material will perform better in the region of interest. Therefore, the *N87* core material is chosen.

Now the core material is chosen, the maximum flux density $\hat{B}$ can be found in the datasheet. This maximum value is equal to around 0.25 T. Having that said, the area product AP ($A_e A_w$) listed in the core database can be compared to the right hand side of Equation (6.9). This results in a minimum AP of 1,200,000 $\mathrm{mm^4}$, so only the *UI126/119/20* cores can be used.

6.1.2. Wires

The number of primary turns is based on Equation (6.4) and is rewritten in Equation (6.11).

$$N_{pri} = \frac{V_{in}}{4 f_s A_e B_{rated}} \tag{6.11}$$

In this equation B_{rated} is the rated flux density and it can be chosen anywhere between zero and $\hat{B}$, which was 0.25 T for *N87* core material. The secondary number of turns is then found by Equation (6.12).

$$N_{sec} = \frac{N_{pri}}{n_{design}} \tag{6.12}$$

Both primary and secondary number of turns are rounded to the integer above *and* below, and of the four resulting turn ratios the one is chosen with the turns ratio that best matches the designed turns ratio.

With the number of primary and secondary turns known, the difference between solid and Litz wire can be investigated, starting with the solid type. Based on Equation (6.6) and Equation (6.7), it can be seen that half of the window area can be filled with primary turns while the other half with secondary turns. This is valid, given the relation between current in and number of turns on the primary and secondary side. Therefore, the copper area of one single turn can be expressed as in Equation (6.13). Note that for solid wire k_w can be 0.6.

$$A_{Cu,pri} = \frac{k_w A_w}{2N_{pri}} \tag{6.13}$$

The copper current density can then be calculated using Equation (6.7), which will be quite low. However, if the skin effect is taken into account, which is the effect that at higher frequencies the current is mainly present on the surface of the conductor, large currents are found. The skin depth can for copper wire be calculated (in mm) using Equation (6.14), which is for 25 kHz about 0.41 mm.

$$\delta_{Cu} = \frac{65}{\sqrt{f_s}} \tag{6.14}$$

The equivalent copper area for wires with a diameter larger than $2\delta_{Cu}$ is calculated using Equation (6.15).

$$A_{Cu,eq} = \pi \cdot \left(\frac{A_{Cu}}{\pi} - \left(\sqrt{\frac{A_{Cu}}{\pi}} - \delta_{Cu} \right)^2 \right) \tag{6.15}$$

The total copper loss is calculated using Equation (6.16).

$$P_{Cu} = I_{rms}^2 R = I_{rms,pri}^2 \rho_{Cu} \cdot \frac{N_{pri} l_N}{A_{Cu}} + I_{rms,sec}^2 \rho_{Cu} \cdot \frac{N_{sec} l_N}{A_{Cu}} \tag{6.16}$$

The other type of wire is called Litz wire. When a wire is chosen which consist of multiple thin wires in parallel, each of them with a diameter smaller than two times the skin depth, the skin effect can be neglected. However, the copper fill factor in the window k_w is now only 0.35. Using the same procedure as with the solid wire, the copper area is calculated and then the number of strands (thin wires) inside the Litz wire is calculated, to fill the complete window. Using some geometry, Equation (6.17) is derived.

$$N_{strands} = \frac{A_{Cu}}{\pi \cdot \delta_{Cu}^2} \tag{6.17}$$

In this way, the resulting copper losses are considerably lower.

Besides the skin effect, there is another known effect which can increase the losses under AC, namely the proximity effect [34]. Using more layers on top of each other will increase the AC losses with a fair amount. For that reason, the number of layers will be limited to two; two primary and two secondary.

Now it is not possible any more to use Equation (6.13), since not the complete window can be filled always. Therefore, the number of layers is estimated first. This is done by looking at the total number of turns that need to be wound. Then, based on the height/ width ratio of the window, an estimation is done for the number of layers. If this means the number of layers will be seven, the window area will be multiplied by a factor of $\frac{2}{7}$ to obtain the usable window area (where 2 is the maximum number of layers allowed). After that, the procedure of wire calculation is the same. Note that given the twisted nature of Litz wire, the individual strands do not count as separate layers. If the number of strands in the Litz wire is known, the diameter of the overall Litz wire is calculated using Equation (6.18). In this equation, $A_{win,eq}$ is the equivalent copper area of Litz wire (one turn), with the maximum number of layers taken into account.

$$d_{Litz} = \sqrt{\frac{4A_{win,eq}}{\pi k_w}} \tag{6.18}$$

Based on the estimated losses, Litz wire was chosen with a diameter of a single strand of $2\delta_{Cu}$. If the diameter of the overall Litz wire is calculated, the number of layers will be verified by dividing the window height by the number of turns and diameter of one turn, as in Equation (6.19).

$$N_{layers} = \frac{h_w}{N \cdot d_{Litz}} \tag{6.19}$$

For calculating the losses in this case, again Equation (6.16) can be used. However, attention must be paid, since the value of l_N from the core database can no longer be used. l_N, which is the average turn length is in the core database based on a completely filled window. Since the number of layers is now restricted, the window is not completely filled. Hence, the average turn length is smaller. Based on the core geometries the new average turn length is calculated using Equation (6.20), note that this equation is for E-cores only, slight changes are needed for U-cores.

$$l_N = w - 2w_w + 2d + \pi b_{Cu} \tag{6.20}$$

In this formula, the width of the core (w), width of the window area (w_w) and depth of the core (d) are taken from the core database. b_{Cu} is the copper width in the window, based on the diameter of the Litz wires (d_{Litz}) and the maximum number of layers allowed, see Equation (6.21).

$$b_{Cu} = N_{layers,max,pri} \cdot d_{Litz,pri} + N_{layers,max,sec} \cdot d_{Litz,sec} \tag{6.21}$$

6.1.3. Leakage inductance

The leakage inductance of the transformer is calculated using Equation (6.22) [8].

$$L_{leak} = \frac{\mu_0 N_{pri}^2 l_N}{p^2 h_w} \left(\frac{b_{Cu}}{3} + b_i \right) \tag{6.22}$$

In this equation μ_0 is the permeability of a vacuum (constant), N_{pri} the primary number of turns, l_N the mean length of a turn (Equation (6.20)), h_w the height of the window and b_{Cu} the copper width in the window (Equation (6.21)). The number of interfaces p and the insulation thickness b_i depend on the arrangement of the turns. For the to be designed transformer, it is chosen to wind all primary turns first and on top of that all secondary turn will be wound. Hence, in between the primary and secondary turns is only one interface, which means $p = 1$. In this way, a higher leakage inductance is achieved compared to using two ($p = 2$) or more interfaces. Two interfaces means winding half of all primary turns first, then all secondary and finally the other half of the primary turns. Having a higher leakage inductance means the inductance value of the external inductance can be lower, which means a smaller inductor resulting in less core losses. The insulation thickness between the primary and secondary turns b_i is for now set to 2 mm, but can be adjusted later, since the impact on the leakage inductance is limited.

6.1.4. Heat management

An important part of the design of a transformer is the heat management. Since all power transfer from the primary to secondary side or vice versa is through the transformer. This means the core of the transformer will constantly be excited with changing magnetic flux, resulting in hysteresis or core losses. To reduce these losses, the number of turns can be increased. However, this will result in more conduction losses through the longer copper wires. In any case, the losses of in the transformer consist of losses in the wires as well as in the core and they will both heat up the transformer. Therefore, there is a need to remove this heat because both the core and (insulation of the) wires are limited by a maximum temperature.

In order to start with the removal of the heat, all the losses have to be clear. Starting with the wires, the copper loss in the wires was discussed in Section 6.1.2 and using Equation (6.16) the power loss could be calculated. The losses in the core are calculated from the Steinmetz coefficients. The formula is given in Equation (6.23).

$$P_c = k \cdot V_e \cdot p_{vsin} \cdot \left(\frac{f_s}{f_b} \right)^{\alpha} \cdot \left(\frac{B}{B_m} \right)^{\beta} \tag{6.23}$$

The corresponding coefficients for N87 core material at an operating temperature of $T_s = 100\,^{\circ}\text{C}$ and $B_m = 0.2\,\text{T}$ are given in Table 6.2 [33]. In order to use the formula and coefficients, the frequency f_b is selected first which matches best with the switching frequency f_s. This specified which row of the table will be used. Then, these coefficients will be substituted in Equation (6.23), with f_s the actual switching frequency, B_m the one of the table (0.2 T), which matches best with the rated flux density of the material and B the rated flux density. The constant k is to compensate for the current waveform, since p_{vsin} is for sinusoidal currents. A number of constants k can be obtained from [33], in this case the one for a push-pull converter is chosen ($T = 100\,^{\circ}\text{C}$ & $B = 0.2\,\text{T}$), which matches best with the bidirectional core excitation of the dual active bridge. The corresponding value of k is 1.28.

Table 6.2: Steinmetz coefficients for N87 core material (T_s = 100 °C & B_m = 0.2 T)

f_b	p_{vsin}	α	β
25 kHz	60.36	1.5184	3.0699
50 kHz	141.18	1.5184	2.9104
100 kHz	392.92	1.5184	2.7726
200 kHz	1200.0	1.5184	2.5334
300 kHz	2650.0	1.5184	2.4544

With all losses clear, the thermal resistances of the core can be calculated. Both radiative and convective heat transfer will contribute to the cooling of the transformer. Starting with the radiative heat transfer, which can be calculated using Equation (6.24).

$$R_{\theta,rad} = \frac{\Delta T}{5.1A\left(\left(\frac{T_s}{100}\right)^4 - \left(\frac{T_a}{100}\right)^4\right)} \tag{6.24}$$

In this formula, the value of 5.1 is for black oxidized aluminium and this value can be used for transformer design [8]. This value is used for the core, as well as for the wires wound around it. The same constant is used, since the emissivity of the black oxidized aluminium is comparable to the plastic insulation of the wires [35]. A is the outer surface area of the transformer, including the wires. For an E-core with all wires wound around the middle leg, this area A can be calculated based on geometry and is given in Equation (6.25).

$$A_{E-core} = 2\left(dw + \pi\left(\frac{w}{4} - \frac{w_w}{2} + b_{Cu}\right)^2 + dh + wh - \left(h_w\left(\frac{w}{2} + w_w\right)\right) + \pi\left(\frac{w}{4} - \frac{w_w}{2} + b_{Cu}\right)h_w\right) \tag{6.25}$$

With all dimensions of the cores given in Appendix C and b_{Cu} in Equation (6.21).

Next is the convective heat transfer, the thermal resistance can be calculated using Equation (6.26).

$$R_{\theta,conv} = \frac{1}{1.34A_{vert}}\sqrt[4]{\frac{h}{\Delta T}} \tag{6.26}$$

With A_{vert} the vertical outside area of the transformer and h the height of the core. A_{vert} is given by a modified version of the total outside area and given in Equation (6.27):

$$A_{vert} = 2\left(dh + wh - \left(h_w\left(\frac{w}{2} + w_w\right)\right) + \pi\left(\frac{w}{4} - \frac{w_w}{2} + b_{Cu}\right)h_w\right) \tag{6.27}$$

To combine both the radiative and convective heat transfer, one should note they are in parallel. Which means the total thermal resistance is given by their combination in Equation (6.28):

$$R_\theta = \frac{R_{\theta,rad}R_{\theta,conv}}{R_{\theta,rad} + R_{\theta,conv}} \tag{6.28}$$

This has consequences for the maximum to be generated power, the relation is given in Equation (6.29).

$$P = \frac{\Delta T}{R_\theta} = \frac{T_s - T_a}{R_\theta} \tag{6.29}$$

6.1.5. Final design parameters

With all formulas known, they are put into an Excel sheet where the design parameters can be edited, and all results are directly calculated. The cores which satisfy the relation given in Equation (6.9) are tried and by varying the rated flux density B_{rated} the best parameters have been found based on the minimum losses. The B_{rated} parameter influences the number of turns and so the ratio between core and conduction losses. The design procedure has been done for three different frequencies, of which the results are given in Table 6.3.

As can be observed, with the frequency increasing the total losses in the transformer will be lower. With the transformer design finished, the design of the inductor is the next phase.

Table 6.3: Designed parameters for the transformer

Parameter	**Value** (25 kHz)	**Value** (35 kHz)	**Value** (45 kHz)
Core type	UI126/119/20 (2× as E)		
Primary number of turns	26	20	19
Primary number of parallel strands	14	31	42
Secondary number of turns	22	17	16
Secondary number of parallel strands	17	36	49
Diameter strand	0.82 mm	0.69 mm	0.61 mm
Copper current density	4.56 A mm^{-2}	3.00 A mm^{-2}	2.85 A mm^{-2}
Turns ratio	1.18	1.18	1.19
Leakage inductance	26.7 µH	19.9 µH	18.6 µH
Conduction losses	33.4 W	17.7 W	16.2 W
Core losses	30.6 W	43.6 W	26.4 W
Total losses	64.0 W	61.3 W	42.6 W
Thermal resistance	0.88 KW^{-1}	0.83 KW^{-1}	0.83 KW^{-1}
Maximum temperature	96 °C	91 °C	75 °C

6.2. Inductor

The second magnetic component is the inductor, which is put in series with the transformer. Due to the leakage of the transformer, the inductance value of the inductor is only the remaining part. A design procedure similar to the one of the transformer is performed, also described in [8]. This design procedure also starts with assembling the design inputs, given in Table 6.4. This inductor is also designed for the three chosen

Table 6.4: Assembling design inputs of the inductor

Parameter	**Value**
Rated RMS voltage V_{in}	600 V
Rated RMS current I_{rms}	35 A
Rated peak current I_{peak}	55 A
fsL-product f_sL	1.503 Hz – H
Operating frequency f_s	25 kHz
Maximum body temperature T_s	100 °C
Maximum ambient temperature T_a	40 °C

frequencies. The fsL-product is the same as before, again for a power transfer of 11 kW.

6.2.1. Core selection

When the design parameters are clear, the Stored Energy Value (SEV) is computed before choosing a core. The stored energy value is given in Equation (6.30).

$$SEV = LI_{rms}I_{peak} \tag{6.30}$$

Where the value of the inductance L is obtained by Equation (6.31) using the fsL-product.

$$L = \frac{f_sL}{f_s} - L_{leak} \tag{6.31}$$

This stored energy relation given by Equation (6.30) is found starting from the familiar Equation (6.32):

$$LI = NBA \tag{6.32}$$

The number of turns N in this equation can be expressed based on the available area in the window of the core, as in Equation (6.33):

$$N = \frac{k_wA_w}{A_{Cu}} \tag{6.33}$$

Where for the wire again Litz wire is chosen, with the same diameter of a strand as for the transformer operating on the same frequency. For this Litz wire the utilisation factor k_w is again 0.35. If Equation (6.7), Equation (6.32) and Equation (6.33) are combined, Equation (6.34) is obtained:

$$LI_{rms}I_{peak} = k_w J_{rms}\hat{B}A_w A_e \tag{6.34}$$

With the left hand part known as the stored energy value, rewriting results in Equation (6.35):

$$\frac{SEV}{k_w J_{rms}\hat{B}} = A_w A_e \tag{6.35}$$

Remember the area product, which was also used for the transformer and a known value in the core database in Appendix C. This gives the ability to again select a core based on the input parameters where the copper current density J_{rms} can be varied to some extend while keeping an eye on the losses. Again the *N87* core material is chosen and the same list of cores will be used, however, this time also the smaller cores are investigated, given the result of Equation (6.35).

6.2.2. Wires

The window of the core will again be completely filled with wires, using the same maximum of two layers. Based on the set copper current density and the RMS value of the current, the size of a conductor will be determined using Equation (6.7). With this copper area, the number of turns that fits into the window is calculated with Equation (6.36).

$$N = \left\lfloor \frac{k_w A_w}{A_{Cu}} \right\rfloor \tag{6.36}$$

Next, the maximum inductance L_{max} will be verified using Equation (6.37):

$$L_{max} = \frac{NA_e B_{rated}}{I_{peak}} \tag{6.37}$$

This value of L_{max} should be close to the required inductance calculated with Equation (6.31). The skin depth in the inductor is of course the same as for the transformer with the same frequency. Therefore, the diameter of a strand of Litz wire is the same as for the transformer, which was 0.82 mm in case of a 25 kHz switching frequency. Based on the conductor area A_{Cu}, the number of parallel strands is calculated by Equation (6.17). The copper loss is obtained in a similar way as for the transformer.

6.2.3. Air gap

The inductor consists of an air gap. The length of the air gap can be found by starting with the reluctance of the magnetic path. For any E-core, all flux goes through the middle leg, then splits whereafter half of the flux goes through the left leg and the other half through the right one. So if the E-cores are separated in order to create an air gap, the air gap is crossed twice in the magnetic path. The reluctance $\Re_m$ is given by Equation (6.38).

$$\Re_m = \Re_{m,core} + \Re_{m,gap} = \frac{l_e}{\mu_0 \mu_r A_e} + \frac{\sum l_g}{\mu_0 A_g} \tag{6.38}$$

Here, l_e is the effective length of the magnetic path in the core, l_g is the length of the air gap and A_g the area of the air gap. The other symbols should be known by now. For a core of magnetic material, the relative magnetic permeability is very high, which means this contribution can be neglected. Making use of this property and $A_g = A_e$, Equation (6.39) is obtained.

$$\Re_m = \frac{\sum l_g}{\mu_0 A_e} \tag{6.39}$$

Which can be combined with Equation (6.40) and rewritten to Equation (6.41), where N_g is the number of air gaps in a magnetic path.

$$\Re_m = \frac{NI_{peak}}{A_e \hat{B}} \tag{6.40}$$

$$l_g = \frac{\mu_0 NI_{peak}}{N_g \hat{B}} \tag{6.41}$$

One must pay attention, that the length of an air gap does not become too large in order to avoid extensive fringing. In order to limit these effects, the maximum length of the air gap is given by Equation (6.42) [34].

$$l_g < \frac{\sqrt{A_e}}{10} \tag{6.42}$$

6.2.4. Final design parameters

The section about heat management of the inductor is identical to that of the transformer in Section 6.1.4, therefore it is not being discussed again. Now all formulas are known, again an Excel sheet is used to directly see the influence of changing parameters on the losses and final temperature. There are in the end roughly three parameters that can be varied while the best design is found. These are:

- the selection of the core;
- the copper current density;
- the rated flux density.

The copper current density influences just as with the transformer directly the number of turns. After some iterations of changing the above three parameters and evaluating the results, the final design parameters of the inductor found are given in Table 6.5.

Table 6.5: Designed parameters for the inductor

Parameter	**Value** (25 kHz)	**Value** (35 kHz)	**Value** (45 kHz)
Core type	E70/33/32	E70/33/32	E65/32/27
Total required inductance $L + L_{leak}$	60.1 µH	42.9 µH	33.4 µH
Remaining inductor inductance L	33.4 µH	23.0 µH	14.8 µH
Set copper current density	3.0 A mm^{-2}	2.5 A mm^{-2}	2.4 A mm^{-2}
Set rated flux density	0.21 T	0.17 T	0.17 T
Number of turns	13	11	9
Number of parallel strands	22	37	49
Diameter strand	0.82 mm	0.69 mm	0.61 mm
Air gap	2.14 mm	2.24 mm	1.83 mm
Conduction losses	3.7 W	2.6 W	1.8 W
Core losses	8.7 W	7.7 W	7.4 W
Total losses	12.4 W	10.3 W	9.3 W
Thermal resistance	3.11 K W^{-1}	3.57 K W^{-1}	0.83 K W^{-1}
Maximum temperature	79 °C	72 °C	73 °C

6.3. Loss calculations

When the design of both magnetic components is done, the loss estimation of the total converter can be extended. In the previous chapter all losses of the semiconductors were discussed and this chapter adds an estimation of the losses in the magnetic components.

6.3.1. Conduction losses

The conduction losses occur due to the finite resistance of the copper. Equations were already given for the resistance of the wires and the resulting losses. These losses depend on the value of the current, which changes through the complete operating range.

6.3.2. Core losses

The core losses of the inductor can be calculated with Equation (6.23), where the flux density B is given by Equation (6.43), where I_{peak} depends on the current power transfer and output voltage.

$$B = \frac{LI_{peak}}{NA_e} \tag{6.43}$$

To calculate the losses of the transformer under different conditions, the equation for the voltage over the transformer will be derived. This is done in Equation (6.44), where v_{in} and v_{out} are the varying voltages which can between $+V_{in}$, 0 and $-V_{in}$ and $+V_{out}$, 0 and $-V_{out}$ respectively.

$$V_{tr} = v_{in} - v_L = v_{in} - (v_{in} - n \cdot v_{out}) = n \cdot v_{out} \tag{6.44}$$

The result that the voltage on the primary side of the transformer equals $n \cdot v_{out}$ makes sense, given the nature of the transformer. For a transformer, using Equation (6.2) the change in flux (denoted by ϕ) can be found by Equation (6.45). Here $n \cdot v_{out}$ is the voltage on the primary side of the transformer and N_{pri} the number of primary turns.

$$d\phi = \frac{V}{N} dt = \frac{n \cdot v_{out}}{N_{pri}} dt \tag{6.45}$$

Next, each time only the first half of a period is considered, just as with the investigation of the current waveforms in Chapter 4. Within half a period the flux will go from the negative peak to the positive peak. To find the corresponding time dt in Equation (6.45), one must find the time where there is a voltage $n \cdot V_{out}$ across the transformer. This duration depends on the current waveform. Firstly, the triangular shape will be investigated, for $V_{in} > n \cdot V_{out}$.

According to Chapter 4, the voltage $n \cdot V_{out}$ is present during the first and second time interval $dt = (T_1 + T_2)$. If this is inserted in Equation (6.45) and simplified, Equation (6.46) is obtained, with the phase shift denoted by φ.

$$d\phi = \frac{n \cdot V_{out}}{N_{pri}} \frac{V_{in}}{V_{in} - n \cdot V_{out}} \frac{\varphi}{\pi f_s} \tag{6.46}$$

The same procedure can be followed for the case $V_{in} < n \cdot V_{out}$, then the voltage $n \cdot V_{out}$ is only present during the second time interval, so the change in flux can be described by Equation (6.47).

$$d\phi = \frac{n \cdot V_{out}}{N_{pri}} \frac{V_{in}}{n \cdot V_{out} - V_{in}} \frac{\varphi}{\pi f_s} \tag{6.47}$$

Lastly the derivation for the changing flux under trapezoidal current modulation, where the voltage $n \cdot V_{out}$ is present during the second and third interval. The change in flux is then described by Equation (6.48).

$$d\phi = \frac{n \cdot V_{out}}{N_{pri}} \frac{\pi - 2\varphi}{2\pi f_s} \tag{6.48}$$

With the change in flux known, the flux density is found by Equation (6.49), where A_e is the effective core area and the division by two is due to the bidirectional core excitation.

$$B = \frac{d\phi}{2A_e} \tag{6.49}$$

Making use of the Steinmetz coefficients, Equation (6.23) can be applied to find the resulting power losses. In Figure 6.2 the resulting flux density is given as a function of the output voltage, for four different power ratings and at a switching frequency of 25 kHz. The peak of the flux density is for every output power at about 0.206 T.

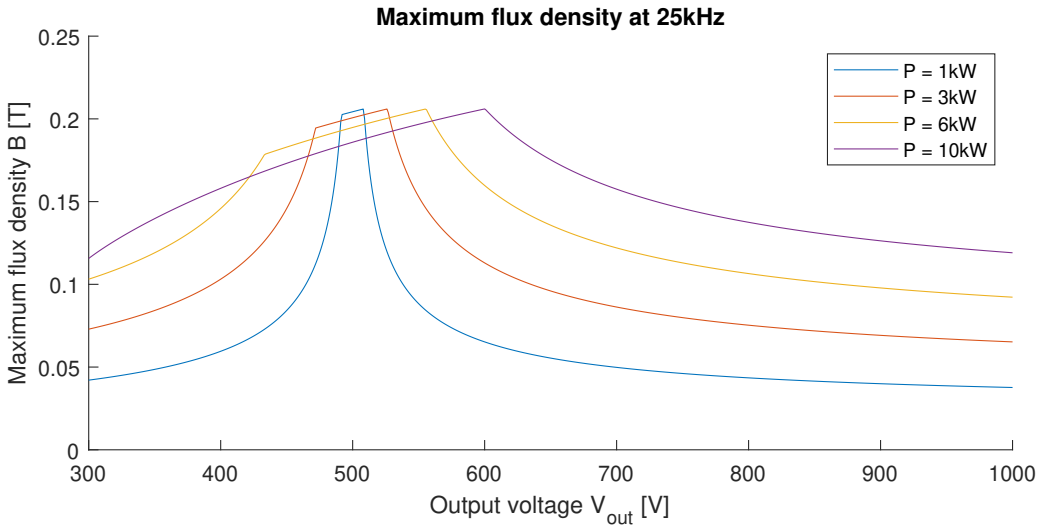


Figure 6.2: Maximum flux density at any output voltage and at different output powers

6.3.3. Overall losses

With the possibility to calculate the losses in the magnetic, as well as the semiconductor devices, a comparison can be done on the total losses for each of the three chosen switching frequencies. This comparison will be done at three different power levels, namely 2 kW, 6 kW and 10 kW. The total losses are displayed in Figure 6.3. The total conduction losses of the MOSFET are in blue, the switching losses in orange, diode

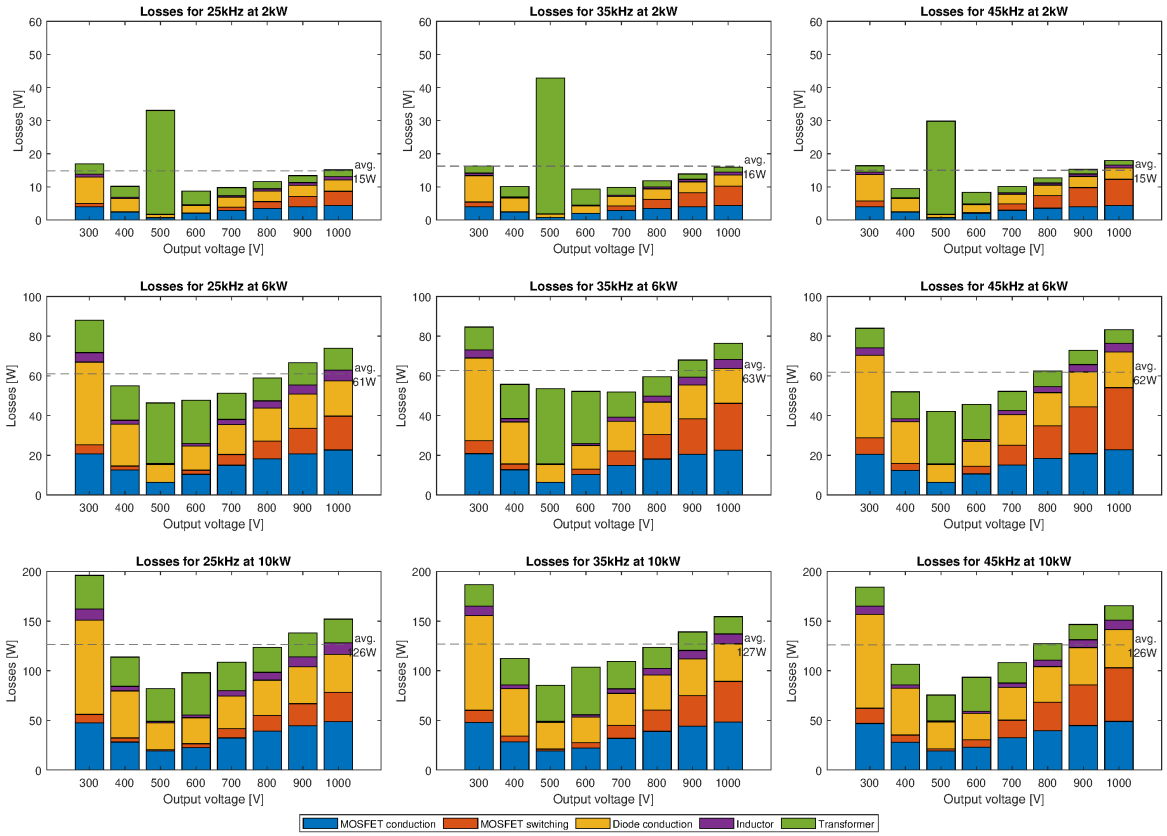


Figure 6.3: Comparison of the overall losses for different switching frequencies

conduction losses in yellow, inductor losses in purple and the transformer losses in green. For both the inductor and transformer the conduction and core losses are added. Given this result, it is clear that there is not one design significantly better in terms of average estimated efficiency. The switching frequency which has the lowest peak losses is 45 kHz, which gives this switching frequency a slight advantage. However, the final decision of switching frequency will be made based on the availability of materials in the laboratory.

6.4. Summary

In this chapter the design steps for the transformer and inductor were discussed. All equations were gathered first as well as a core database which was made. Using an Excel sheet with all equations inserted, design parameters could be changed while directly observing the consequences in terms of expected losses and rise in temperature. Finally, for each switching frequency both a transformer and an inductor were designed. An overview of both semiconductor and magnetic losses was given and it was concluded that there was no significant difference in terms of overall losses.

7

Design: PCB layout

In this chapter, the design steps until the finished printed circuit board (PCB) will be described. Before starting with the design of the PCB, all schematics need to be finished first. With respect to the power electronics part, the capacitors need to be selected as well as the heat sink. Then, the control logic is shortly described since it is necessary for the converter to operate, but not the main objective. Finally the actual PCB will be designed.

Due to the circumstances described in the introduction during the second half of this graduation project, accessing the laboratories was not possible. Where it was stated in the previous chapter that the switching frequency should be chosen based on the availability of materials in the laboratory, this also was no longer possible. As a switching frequency 25 kHz was chosen. Mainly since this gives the largest amount of ripple. By choosing the capacitors in such a way the requirement of the maximum ripple is satisfied, the requirement is also satisfied for a higher switching frequency. The magnetic components will not be placed on the PCB and can therefore be changed much easier than for example the capacitors.

Contents in this chapter

7.1. Capacitors

The DAB converter needs capacitors on the output in order to reduce the ripple voltage. The maximum ripple voltage is given by the requirements in Section 1.3 and is 10 V. To calculate the required values of the capacitors, the charge need to be calculated first. This differs for the triangular and trapezoidal current modulation, firstly, the triangular current modulation is described.

7.1.1. Triangular

A typical waveform of the current is given in Figure 7.1. The shaded area represents the charge ΔQ which will be calculated. Therefore, the average output current I_o will be written as in Equation (7.1). As with

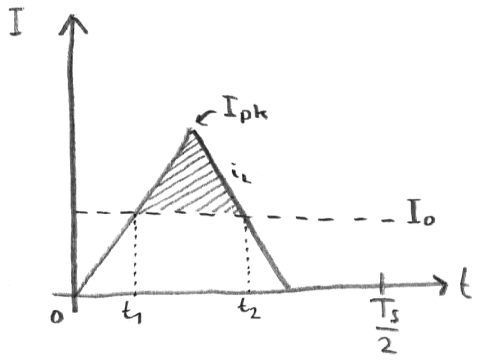


Figure 7.1: Current waveform to calculate the charge (triangular)

all calculations that will follow for the calculation of the required charge, everything will be referred to the primary side.

$$I_o = \frac{P_{out}}{V_{out}} \cdot \frac{1}{n} \tag{7.1}$$

Firstly, the charge will be calculated in case of $V_{in} > n \cdot V_{out}$. Using Equation (4.1), t_1 can be written as Equation (7.2).

$$t_1 = \frac{LI_{out}}{V_{in} - n \cdot V_{out}} \tag{7.2}$$

Using a modified version of Equation (4.2) as given in Equation (7.3), the value of t_2 is found in Equation (7.4). In this equation the duration of the first interval T_1 is written as a function of the phase shift ϕ.

$$i_{L,2}(t) = I_{pk} - \frac{n \cdot V_{out}}{L}(t_2 - T_1) = I_o \tag{7.3}$$

$$t_2 = \frac{(I_{pk} - I_o)L}{n \cdot V_{out}} + T_1 = \frac{(I_{pk} - I_o)L}{n \cdot V_{out}} + \frac{\phi}{\pi f_s} \frac{n \cdot V_{out}}{V_{in} - n \cdot V_{out}} \tag{7.4}$$

The values of t_1 and t_2 can also be calculated in case of $n \cdot V_{out} > V_{in}$. The procedure is similar and the value of t_1 is found in Equation (7.5).

$$t_1 = \frac{I_o L}{V_{in}} \tag{7.5}$$

The value of t_2 depends once again on the phase shift ϕ, and this is shown by the relation in

$$t_2 = \frac{\phi}{\pi f_s} + \frac{(I_{pk} - I_o)L}{n \cdot V_{out} - V_{in}} \tag{7.6}$$

The charge in both cases is finally calculated using Equation (7.7), where the multiplication with n is needed in order to refer the result back to the secondary side.

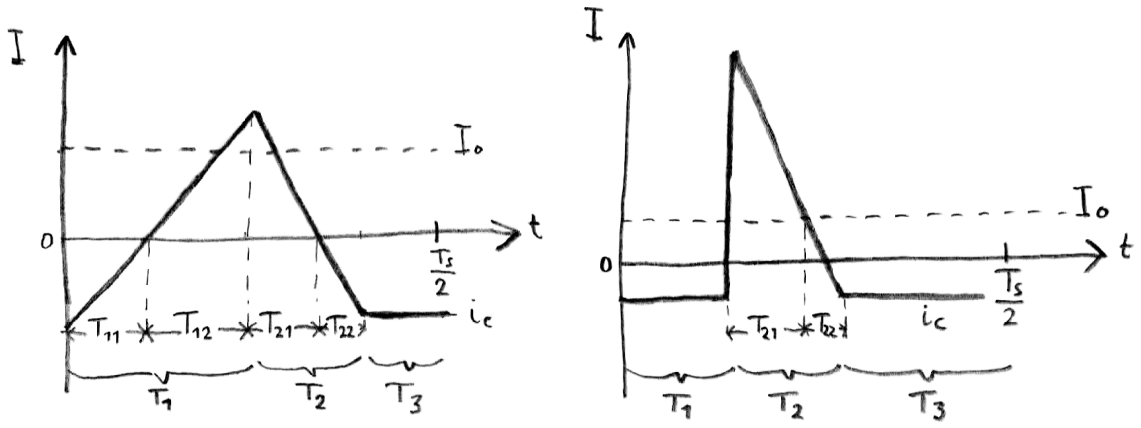
$$\Delta Q = 0.5(t_2 - t_1)(I_{pk} - I_o)n \tag{7.7}$$

Besides the charge, the RMS current flowing in and out of the capacitor should be calculated. This is useful for determining the losses as a consequence of a parasitic resistance in series with the capacitor. For triangular current modulation, the waveforms of the output capacitor are given in Figure 7.2. The case of $V_{in} > n \cdot V_{out}$ will be discussed, drawn in Figure 7.2a. The average output current is given by Equation (7.8), note that this is not reflected to the input. The calculation of RMS current will be done with the current values at the output.

$$I_o = \frac{P_{out}}{V_{out}} \tag{7.8}$$

The durations of each interval T_1, T_2 and T_3 were all given in Chapter 4, as well as the slopes. However, they are now reflected to the output:

$$\frac{di_1}{dt} = n \cdot \frac{V_{in} - n \cdot V_{out}}{L} \tag{7.9}$$



(a) $V_{in} > n \cdot V_{out}$

(b) $V_{in} < n \cdot V_{out}$

Figure 7.2: Capacitor current waveforms under triangular current modulation

$$\frac{di_2}{dt} = n \cdot \frac{-n \cdot V_{out}}{L} \tag{7.10}$$

For the calculation of the RMS value, the current waveform will be split in different parts. Each zero-crossing or change in slope will be the beginning of a new interval. The duration of some new intervals originating from the zero-crossings should be calculated. This can be done making use of the following equations:

$$T_{11} = \frac{n \cdot I_{L,pk} - I_o}{\left|\frac{di_1}{dt}\right|} \tag{7.11}$$

$$T_{12} = T_1 - T_{11} \tag{7.12}$$

$$T_{21} = \frac{n \cdot I_{L,pk} - I_o}{\left|\frac{di_2}{dt}\right|} \tag{7.13}$$

$$T_{22} = T_2 - T_{21} \tag{7.14}$$

Using the general expressions for calculating the RMS value of such a general waveform as in Figure 4.4, leads finally to the correct RMS value given by Equation (7.15):

$$I_{C,RMS} = \sqrt{\frac{T_3}{0.5T_s} \cdot I_o^2 + \frac{T_{11}}{0.5T_s} \cdot I_{RMS,T_{11}}^2 + \frac{T_{12}}{0.5T_s} \cdot I_{RMS,T_{12}}^2 + \frac{T_{21}}{0.5T_s} \cdot I_{RMS,T_{21}}^2 + \frac{T_{22}}{0.5T_s} \cdot I_{RMS,T_{22}}^2} \tag{7.15}$$

The procedure for $V_{in} < n \cdot V_{out}$ is comparable, but easier, since there is only one zero-crossing during T_2.

7.1.2. Trapezoidal

If the converter is operating under a trapezoidal waveform, the charge also need to be calculated. In order to do this, all different kinds of waveforms are inspected. They are given in Figure 7.3. Starting with the cases depicted in Figure 7.3a and Figure 7.3b, where both peaks I_{pk1} and I_{pk2} are larger than the output current. The value of time interval t_x can be expressed by Equation (7.16).

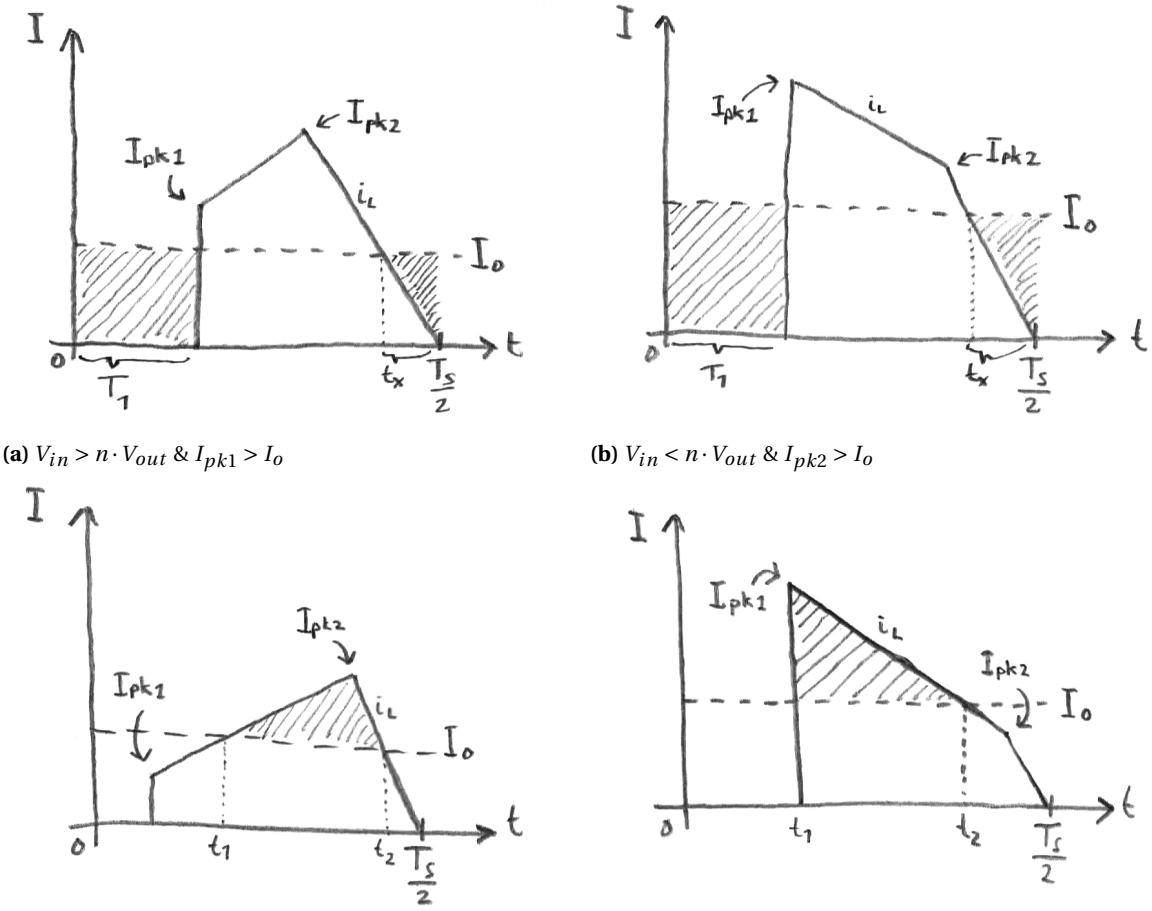
$$t_x = \frac{I_o L}{n \cdot V_{out}} \tag{7.16}$$

Combining with the duration of the first time interval T_1 and the charge (shaded area) can be calculated with Equation (7.17), again referred to the secondary side.

$$\Delta Q = 0.5 n I_o t_x + n I_o T_1 = 0.5 n I_o t_x + n I_o \frac{\phi}{\pi f_s} \tag{7.17}$$

The next case is the one of Figure 7.3c, using the expression for the current in the second time interval, t_1 is given by Equation (7.18) and t_2 is given in Equation (7.19).

$$t_1 = \frac{(I_o - I_{pk1})L}{V_{in} - n \cdot V_{out}} + T_1 \tag{7.18}$$



(a) $V_{in} > n \cdot V_{out}$ & $I_{pk1} > I_o$

(b) $V_{in} < n \cdot V_{out}$ & $I_{pk2} > I_o$

(c) $V_{in} > n \cdot V_{out}$ & $I_{pk1} < I_o$

(d) $V_{in} < n \cdot V_{out}$ & $I_{pk2} < I_o$

Figure 7.3: Different current waveforms to calculate the charge under trapezoidal current modulation

$$t_2 = \frac{(I_{pk2} - I_o)L}{n \cdot V_{out}} + T_1 + T_2 \tag{7.19}$$

The charge is then calculated using Equation (7.20).

$$\Delta Q = 0.5(t_2 - t_1)(I_{pk2} - I_o)n \tag{7.20}$$

The last case, depicted in Figure 7.3d is calculated similarly. t_1 is equal to the duration of the first time interval T_1 and t_2 is given by Equation (7.21).

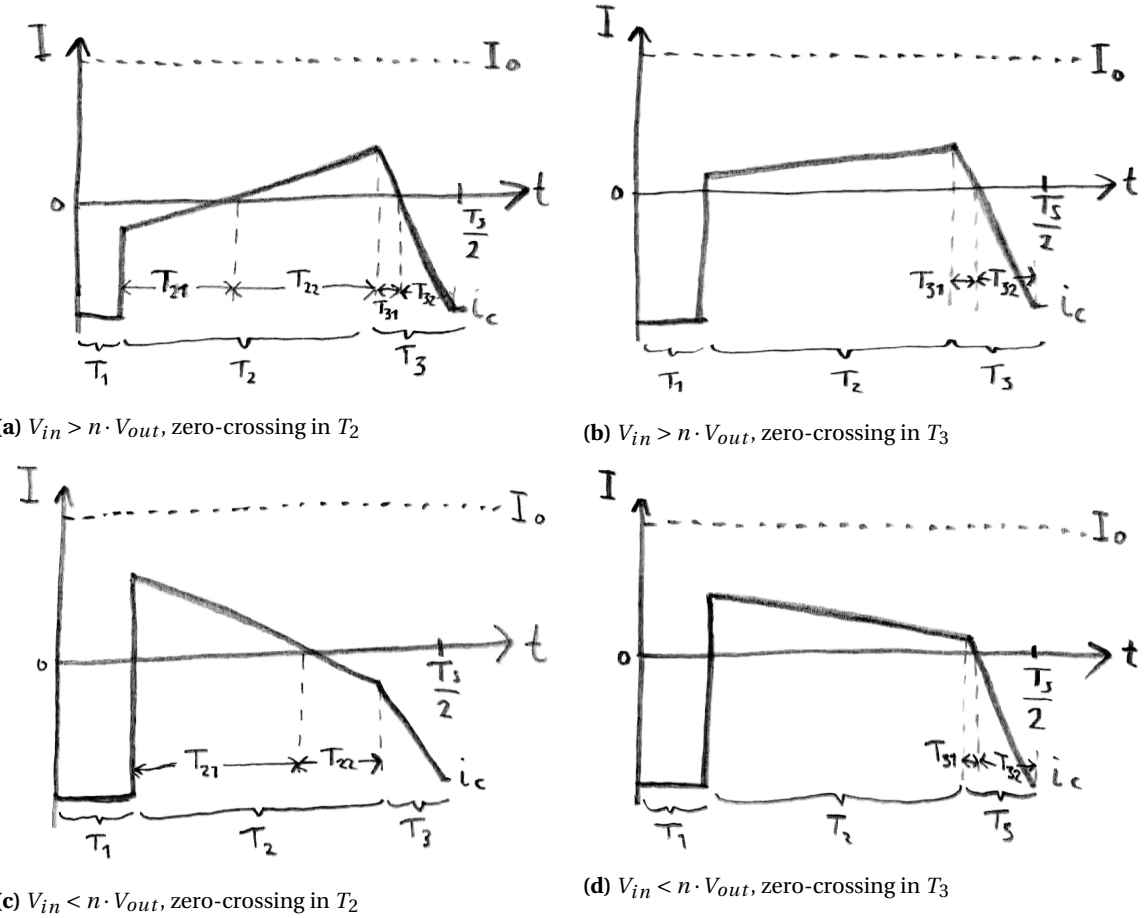
$$t_2 = \frac{(I_{pk1} - I_o)L}{n \cdot V_{out} - V_{in}} + T_1 \tag{7.21}$$

The charge is found with Equation (7.22).

$$\Delta Q = 0.5(t_2 - t_1)(I_{pk1} - I_o)n \tag{7.22}$$

With the charges clear, the focus is on the calculation of the RMS currents flowing in and out of the capacitor. Similar to the procedure as for the triangular current modulation, firstly, the current waveforms are given in Figure 7.4. Given that the procedure for calculating the RMS value of the current is very similar to the triangular current modulation, only one case will be considered. This is the case for $V_{in} > n \cdot V_{out}$, where there is a zero-crossing of the current in the third interval, refer to Figure 7.4b. Derivations for T_1 and T_2 in trapezoidal mode were given in Chapter 4, but the third interval is split due to the zero-crossing in T_{31} and T_{32}. The current value peaks between the second and third interval, using the peak value of the inductor at that moment given in Equation (4.43), the peak of the capacitor current is shown in Equation (7.23):

$$I_{C,pk,trap} = n \cdot I_{L2} - I_o \tag{7.23}$$



(a) $V_{in} > n \cdot V_{out}$, zero-crossing in T_2

(b) $V_{in} > n \cdot V_{out}$, zero-crossing in T_3

(c) $V_{in} < n \cdot V_{out}$, zero-crossing in T_2

(d) $V_{in} < n \cdot V_{out}$, zero-crossing in T_3

Figure 7.4: Capacitor current waveforms under trapezoidal current modulation

Using the slope of current in the third interval given in Equation (7.24), the duration of the intervals T_{31} and T_{32} is given in Equation (7.25) and Equation (7.26) respectively.

$$\frac{di_3}{dt} = n \cdot \frac{-n \cdot V_{out}}{L} \tag{7.24}$$

$$T_{31} = \frac{I_{C,pk,trap}}{\left|\frac{di_3}{dt}\right|} \tag{7.25}$$

$$T_{32} = T_3 - T_{31} \tag{7.26}$$

With the durations of each interval known, the RMS values of the specific intervals can be calculated. Note however, that for the calculation of RMS current not only the triangular waveform of Figure 4.4 should be used, but also the trapezoidal waveform of which the shape is depicted in Figure 4.13. Referring to the second interval, this is indeed the case, which means the RMS current in this interval can be calculated using Equation (7.27), where I_{L1} is the value of the current at the transition between the first and second interval, given in Equation (4.42).

$$I_{C,RMS,T_2} = \sqrt{\frac{1}{3} \cdot \frac{di_2}{dt}^2 \cdot T_2^2 + (n \cdot I_{L1} - I_o) \cdot \frac{di_2}{dt}^2 \cdot T_2 + (n \cdot I_{L1} - I_o)^2} \tag{7.27}$$

The RMS value of the current during interval T_{31} and T_{32} is of triangular form and calculated using Equation (7.28).

$$I_{C,RMS,T_{31}} = \frac{1}{\sqrt{3}} \left|\frac{di_3}{dt}\right| \cdot T_{31} \tag{7.28}$$

The final expression for the RMS current in Figure 7.4b is then given in Equation (7.29):

$$I_{C,RMS} = \sqrt{\frac{T_1}{0.5T_s} \cdot I_o^2 + \frac{T_2}{0.5T_s} \cdot I_{C,RMS,T_2}^2 + \frac{T_{31}}{0.5T_s} \cdot I_{C,RMS,T_{31}}^2 + \frac{T_{32}}{0.5T_s} \cdot I_{C,RMS,T_{32}}^2} \tag{7.29}$$

Having all equations derived for the two cases in triangular mode and four cases in trapezoidal mode, the RMS current can be calculated for each combination of output voltage and power. This is shown in Figure 7.5. The maximum RMS current flowing in or out of the capacitor is 18.7 A. The results of the capacitor currents

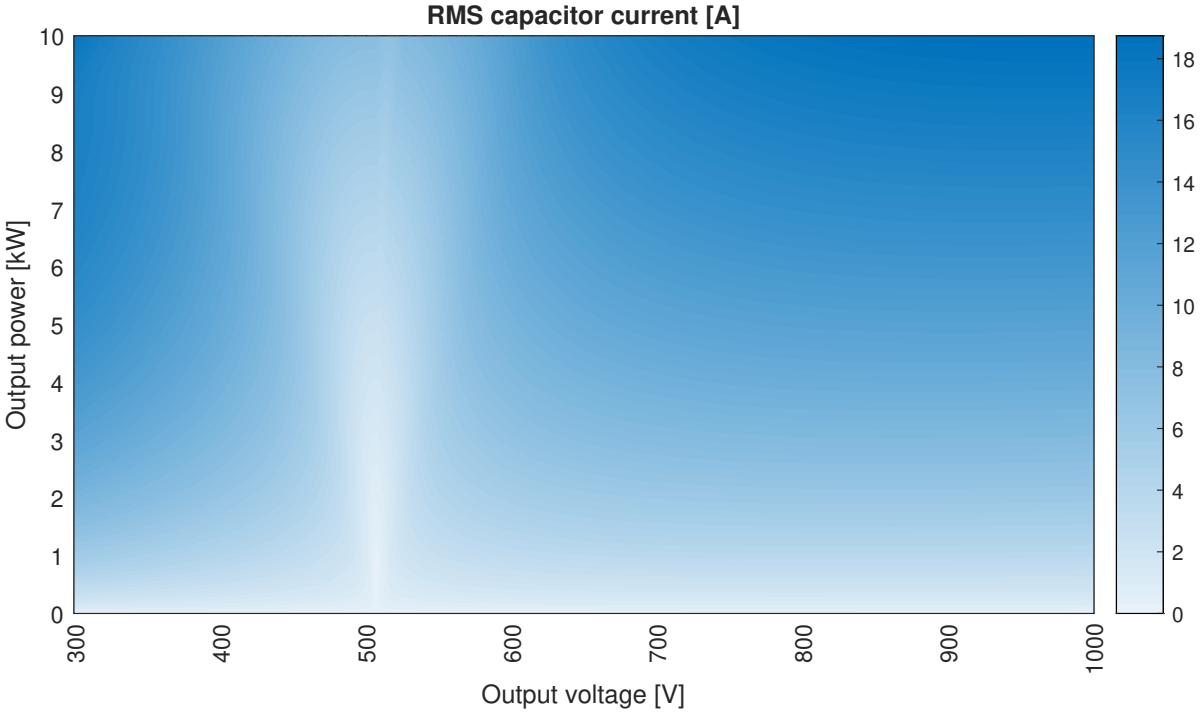


Figure 7.5: RMS capacitor current for all output combinations

are verified by simulation using Gecko Circuits (Appendix D).

7.1.3. Required capacitance

With the charges known, the required capacitance can be calculated via Equation (7.30), with a voltage ripple of 10 V as requirement.

$$C_{out} = \frac{\Delta Q}{\Delta V} \tag{7.30}$$

This depends of course on the charge and thus on the modulation technique, which on its place depends on the output voltage and transferred power. If the required capacitance is plotted for all possible variations in output voltage and power, the plot in Figure 7.6 is obtained. So in the worst case, an output capacitor of 29.3 µF is needed.

7.1.4. Input capacitance

If the same voltage ripple of 10 V is allowed on the primary side, the story is the same for the input capacitors. Using the relation of the transformer given by Equation (7.31), the input capacitance can be calculated with Equation (7.32).

$$i_{in} = \frac{i_{out}}{n} \tag{7.31}$$

$$C_{in} = \frac{C_{out}}{n} \tag{7.32}$$

This results in a minimum required input capacitance of 24.4 µF.

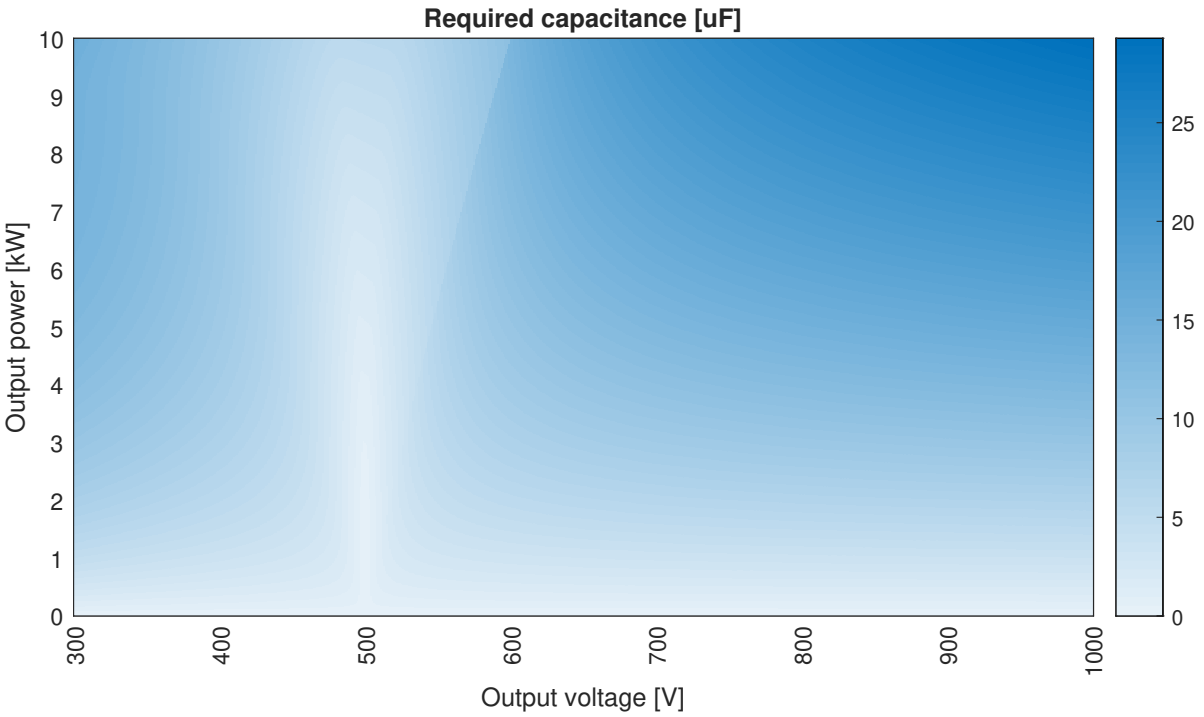


Figure 7.6: Required output capacitance for a voltage ripple of 10 V and 25 kHz switching frequency

7.1.5. Selected capacitors

With the properties of both the input and output capacitor known, the physical components can be selected. For this, a look is taken into aluminium electrolytic capacitors and metallised polypropylene film capacitors. Given the requirements of the voltage and capacitance, ceramic capacitors are not suitable and will not be considered. If the other two types of capacitors are compared, one can use Figure 7.7 [36]: It can be seen

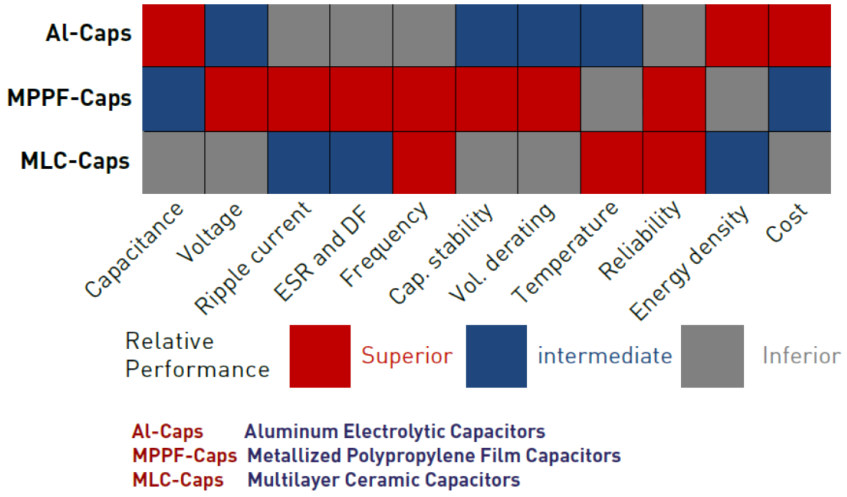


Figure 7.7: Performance comparison of three types of capacitors

that the electrolytic capacitors win in terms of cost, temperature performance and energy density. However, the performance of film capacitors is better when it comes to ripple current, equivalent series resistance (ESR), frequency behaviour, stability and reliability. Therefore a film capacitor will be chosen, namely the C4AQQBW5300A3MJ from KEMET. This capacitor is relatively cheap, able to withstand a DC voltage of 1100 V, has a capacitance of 30 µF (±5 %) and a low ESR of 5.2 mΩ [37].

The losses in the capacitor can be calculated using the equivalent series resistance and the RMS current flowing through it. This will lead to a power loss of 1.83 W as a maximum at the output capacitor. Given the

lower current at input, the losses of the input capacitor are expected to be lower. With a power loss of 1.83 W and the corresponding thermal resistance of 12 °CW^{-1}, the temperature of the capacitor will be in the worst case 22 °C above ambient temperature. This means there is no need for an additional heat sink or multiple capacitors to spread the heat dissipation.

As a measure of safety the capacitors should discharge when the converter is turned off. This is done by adding resistors in parallel. Given a maximum allowable voltage drop of 100 V over an SMD (surface mounted device) resistor, at least ten resistors should be placed in series. Using resistors of each 50 kΩ is considered safe enough and the total power loss is then at most 2.72 W (600 V on the primary bridge and 1000 V secondary).

7.2. Heat sink

In order to keep the temperature of the MOSFETs below the maximum values, an additional heat sink is required. In order to determine which heat sink is able to cool the MOSFETs sufficient, a thermal model is build. It is chosen to use one heat sink, where the isolation is ensured by placing pads between the MOFETs and the heat sink. The thermal model is given in Figure 7.8. In this model, the current sources represent

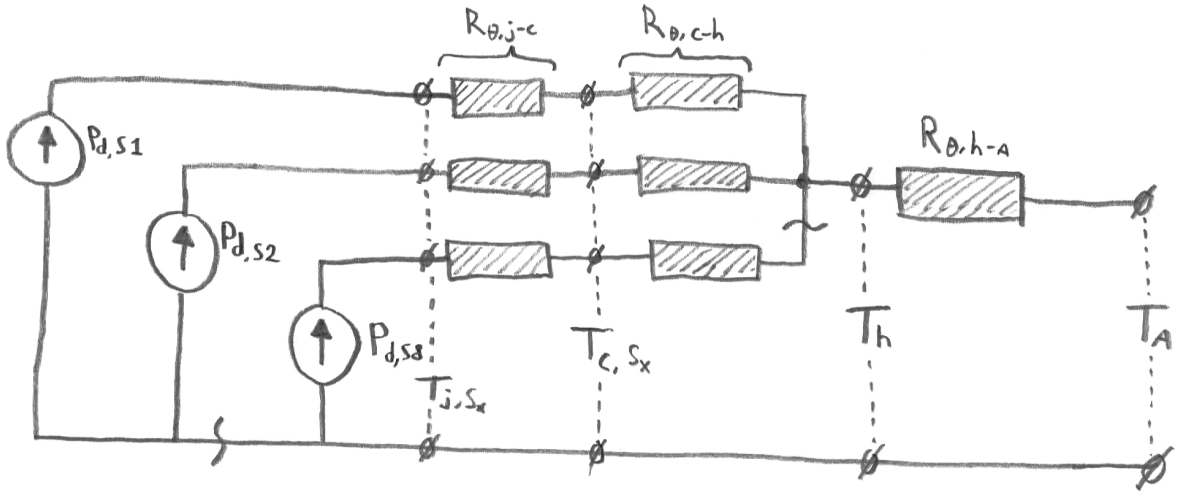


Figure 7.8: Thermal model for the MOSFETs of the converter

the MOSFETs with each their corresponding dissipated power P_d. Each MOSFET has a thermal resistance from the function to the case, $R_{\theta,j-c}$, indicated by the left column of resistors, each followed by a thermal resistance from case to heat sink, $R_{\theta,c-h}$. Lastly, all MOSFETs are mounted on the same heat sink with a thermal resistance from heat sink to ambient of $R_{\theta,h-a}$.

The maximum dissipation of a single MOSFET (conduction and switching losses) in the converter is calculated as 27.4 W. The maximum junction temperature of the MOSFET is limited by 135 °C and $R_{\theta,j-c}$ is 0.32 °CW^{-1} [27]. The interface between the case of the MOSFET and the heat sink will be an isolation pad, for which a thermal resistance of 0.1 °CW^{-1} is used. Using the maximum junction temperature, the maximum temperature of the heat sink can be calculated using Equation (7.33).

$$\Delta T_{j-h} = P_{d,max} \cdot (R_{\theta,j-c} + R_{\theta,c-h}) \tag{7.33}$$

This results in a temperature difference of 11.5 °C, so a maximum allowed heat sink temperature of 123 °C.

With the maximum temperature of the heat sink known, the thermal model can be somewhat simplified to the one depicted in Figure 7.9. Now, the heat source is the sum of the dissipated power of the eight switches. This maximum value is also calculated including both conduction and switching losses and found to be 151 W. Using an ambient temperature of 40 °C, the required thermal resistance of the heat sink can be calculated using Equation (7.34).

$$R_{\theta,h-a} = \frac{T_h - T_a}{\sum_{x=1}^{8} P_{d,Sx}} \tag{7.34}$$

So the thermal resistance of the heat sink $R_{\theta,h-a}$ should be smaller than 0.55 °CW^{-1}. However, this is an absolute maximum, there are several reasons why a heat sink with lower thermal resistance should be chosen,

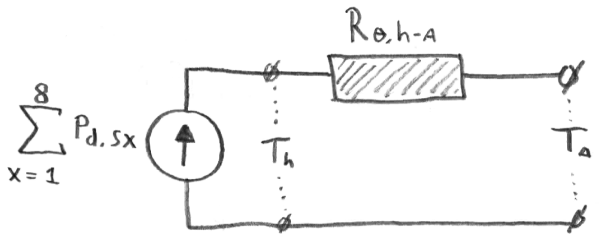


Figure 7.9: Simplified thermal model

namely:

- As written in Chapter 5, turn on losses are set to be neglected as well as several turning off transitions. It might be possible that these switching transitions introduce additional losses which will result in more dissipation;
- The heat will not be spread equally in the heat sink, resulting in higher temperatures at the sources;
- With insufficient air flow, the ambient temperature in the vicinity of the heat sink can become more than the designed value of 40 °C;
- The lifetime of a MOSFET reduces significantly when it is used under high temperatures. A lower temperature than the maximum is always preferable.

Taking this into consideration and applying the following assumptions:

- Losses can be 20 % higher than calculated;
- Ambient temperature in the vicinity of the heat sink can rise an additional 10 °C.

The maximum thermal resistance of the heat sink is again calculated and now found to be slightly above 0.40 °CW^{-1}. Based on the available space on the PCB, as well as the distance between the MOSFETs a look is taken to several different heat sinks. Finally a miniature cooling aggregate from Fischer Elektronik, the LAM 5 D K 125 12. This heat sink has a thermal resistance of 0.40 °CW^{-1} [38] which should be sufficient for this converter. However, this cooling performance is only achieved with two 12 V fans, which consume together about 2.5 W.

7.3. Control circuit

Besides the power electronics part, there is also a need to control the power and voltage output. Although it is not the main objective, the control circuitry will be discussed shortly. There are not much design choices involved here, since as much as possible is copied from another converter build by my supervisor. The main controller is a development board from Texas Instruments (LAUNCHXL-F28379D) and for the gate drivers external PCBs are used, which provide isolation and were already designed by my supervisor.

7.3.1. Power

The power for the control board is coming from an external 5 V DC power source. The gate drivers and also other ICs (integrated circuits) demand a 5 V supply, while the controller board from Texas Instruments requires a voltage level of 3.3 V. This is established by a linear voltage regulator. To prevent noise from the fans propagating through the control circuit, the fans are fed from a secondary DC power supply. The schematics for the power section of the control circuit are given in Appendix E.1.

7.3.2. Voltage measurement

For the controller it is required to know the input and output voltages in order to determine how to trigger the MOSFETs for a given amount of power. Therefore the voltages on the input and output should be known and thus a voltage measurement is required. To keep the isolation, a Texas Instruments AMC1300 isolation amplifier is used in combination with a Traco Power TMA0505S isolated DC-DC converter. Since the isolation amplifier can only handle an input voltage of ±250 mV [39], the voltage level is stepped down using a resistive division. The schematic is given in Appendix E.2.

7.3.3. Current measurement

A current measurement is not strictly required for operating. However, the ability to measure the current can eventually be used to verify the performance of the converter or it can help detecting moments of zero current flowing. Therefore, it is decided to add one current sensor to the board, in series with the inductor. For measuring primary current, the LEM CKSR 50-NP will be used, this device can handle a nominal current of 50 A and peaks of ±150 A [40], which is sufficient for the currents on the primary side. Since this device already provides isolation, only an operational amplifier is used before the measured signal is fed into the Texas Instruments controller. The schematic is shown in Appendix E.3.

7.4. PCB

For prototyping the described converter all components need to be placed on a PCB. This section will describe how this PCB is designed. First of all, the PCB consists of different layers stacked on top of each other. The structure is shown in Figure 7.10. It can be seen that the PCB has four different copper layers, where on the

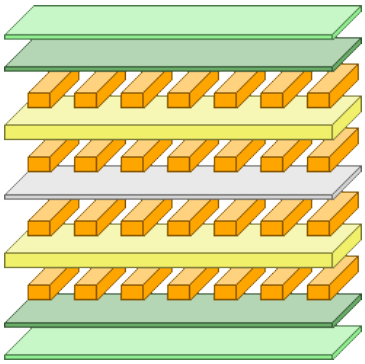


Figure 7.10: Cross section of the PCB with its layers

top and bottom layer components can be placed. In between these copper layers there are dielectrics, with on the top and bottom an overlay.

The PCB itself is divided into three different sections; the low voltage control circuit, the high power primary side and the high power secondary side. These sections are all isolated from each other as a measure of safety. Between these sections there is everywhere at least a clearance of 2.75 mm.

The top and bottom layer consist mainly of signal paths between all components. The two middle layers are mostly used for transferring power. The nets they are connected to are given in Table 7.1.

Table 7.1: Connected nets on each layer of the PCB

Section:	**Low voltage control**	**High power primary side**	**High power secondary side**
Top layer		*Interconnections of mounted components*	
Signal layer 1	5 V or 3.3 V	Primary positive DC	Secondary positive DC
Signal layer 2	Ground	Primary negative DC	Secondary negative DC
Bottom layer		*Interconnections of mounted components*	

Before the actual routing is started, all components are grouped in such a way all components that belong to the same part are placed close to each other. For example all resistors, capacitors and ICs for voltage measuring are placed on an area as small as possible. Then, all these grouped parts are placed on the actual PCB. For the design a basic sketch is made first of the placements of the large components. This includes the following components:

- Heat sink;
- Gate drivers;
- Texas Instruments control board;
- Primary and secondary capacitors.

These components can either be placed on the top or the bottom layer. If a location for the heat sink is chosen, the MOSFETs need to be attached to this heat sink and close to the MOSFETs the gate drivers are placed. On this part both the top and bottom layer are now more or less occupied with the big components. Next to this, the control board can be placed, with on the other side of the board the big capacitors. In this way, almost everywhere on the board are big components placed on top and bottom, so one can think of it as it could be placed in a box with minimal dimensions. Given the huge size of the transformer, the imaginary box that could fit around the PCB can be extended and matches relatively close the size of the transformer. Since the transformer was a bit longer in the x (horizontal) direction, the PCB of the converter is extended on the left side and two more capacitors were added. This is done since there was space available in the imaginary box around the PCB and magnetics and this will result in a lower ripple voltage, which is a useful way of filling up unused space. Given there are now two capacitors on each bridge, it is chosen to use two capacitors with

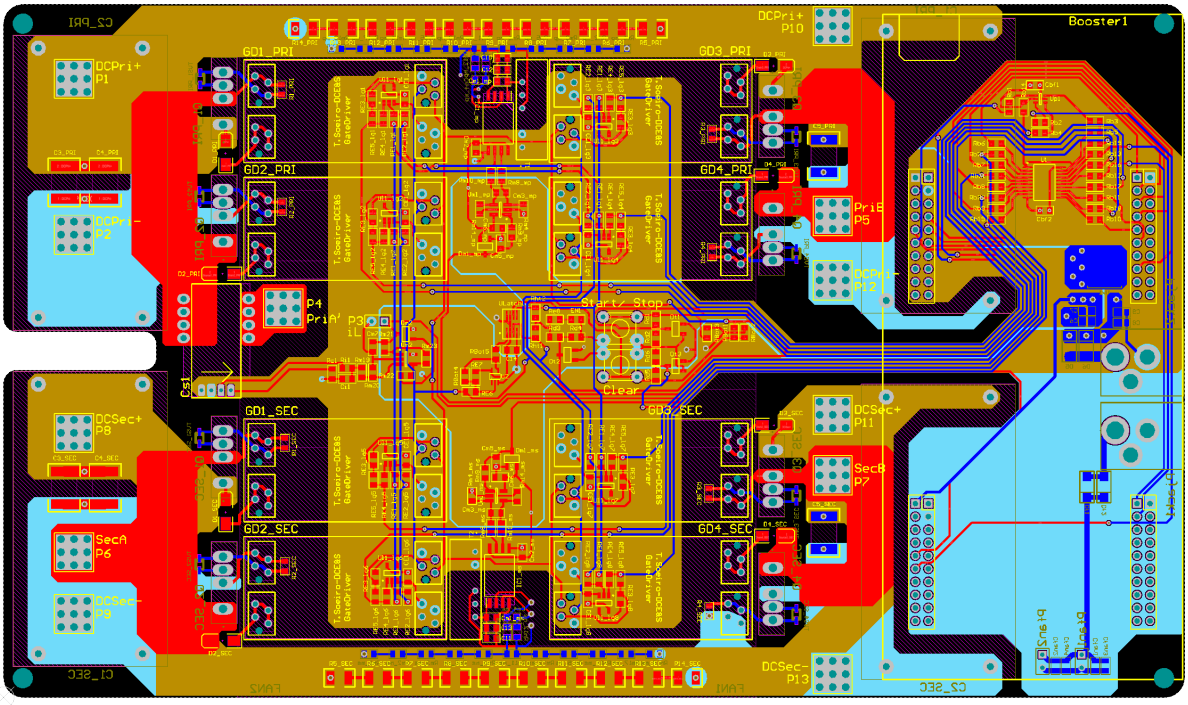
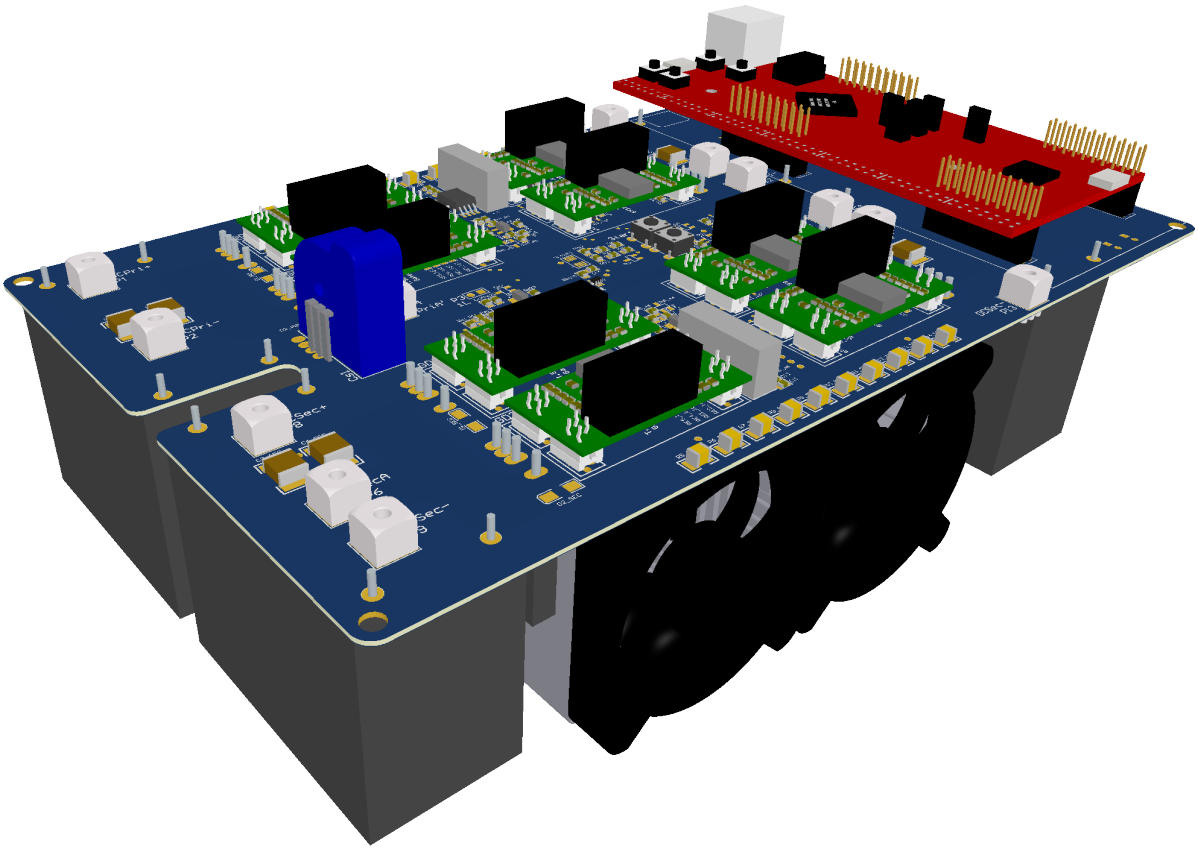
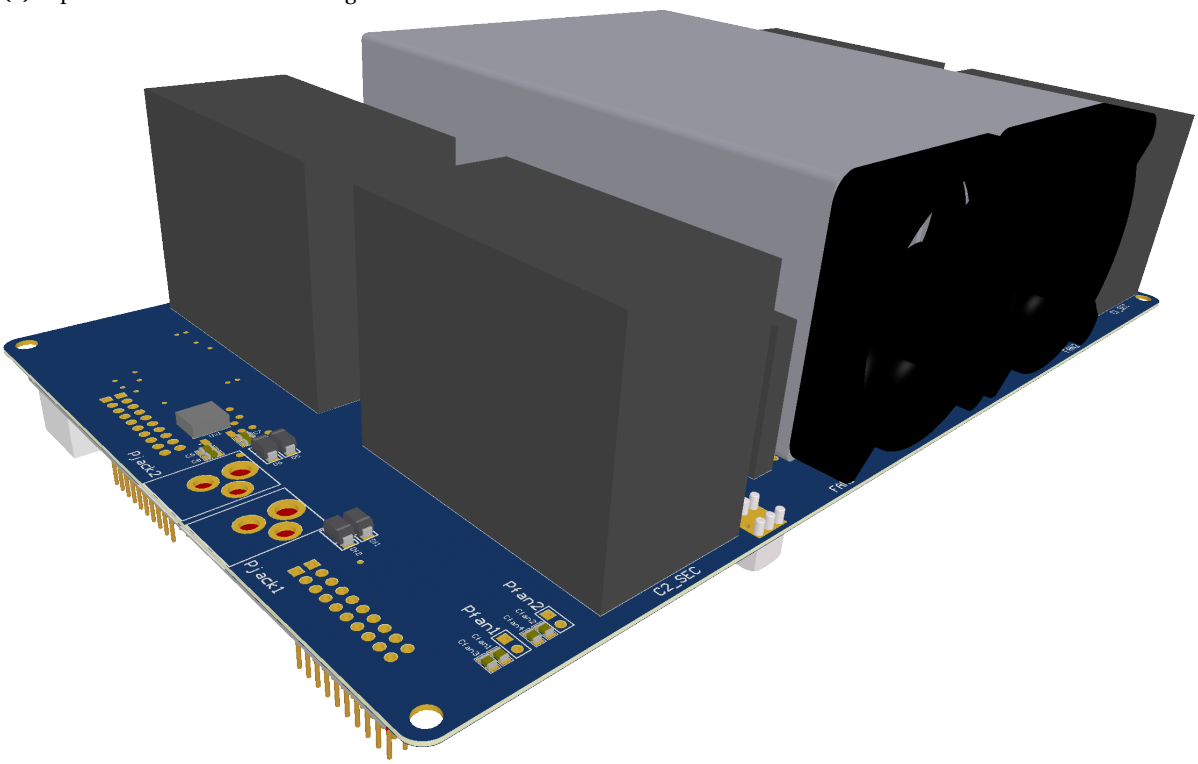


Figure 7.11: 2D overview of the final routed PCB

a lower capacitance (20 µF each instead of 30 µF), but with a higher maximum voltage rating (1300 V instead of 1100 V). This given a little more room for possible voltage spikes and the requirement on the capacitance was already met, most important, these capacitors are less expensive. These new chosen capacitors are from the same series from Kemet, namely the *C4AQUBW5200A3MJ*. This capacitor has the same dimensions and thermal resistance as the old one, but a slightly higher ESR. This higher ESR (6.5 mΩ instead of 5.2 mΩ) is no problem, since there are now two capacitors, so there is less current flowing per capacitor, hence the losses are lower. An overview of the final routed PCB design is given in Figure 7.11. In the middle and on the right side the low voltage control section can be seen, on the top the high power primary and on the bottom the high power secondary section. The Texas Instruments control board is placed on the right and the gate drivers can be seen in the middle, with the corresponding MOSFETs on the outside. In between the gate drivers the isolated voltage measurement parts can be observed on the top and bottom. Also, between each section the clearance is visible and for all DC connections of the high power part two connectors are placed, which should be connected both when using the converter to its full extend. This alternative is chosen, since the board can be a bit smaller. Copper PCB tracks would have caused a lot of losses resulting in heat or have made the board larger in the y (vertical) direction. An overview of the 3D model of the PCB with its components is given in Figure 7.12. Note however, that of some components there was no 3D model available. Some are left out, while for the Texas Instruments control board an alternative 3D model is used which looks similar.



(a) Top of the 3D model of the designed PCB



(b) Bottom of the 3D model of the designed PCB

Figure 7.12: Overview of the 3D model of the PCB

7.5. Estimated overall efficiency

Since this thesis no longer includes the building of the converter and measuring the performance in terms of efficiency, a final estimation will be done for the efficiency throughout the complete operating range of the converter. This includes losses in the following components:

- Semiconductors (conduction and switching);
- Transformer (conduction and core);
- Inductor (conduction and core);
- Capacitors (equivalent series resistance and discharge);
- Cooling (two fans);
- Control logic (estimation of a constant 5 W).

Next to the losses that were neglected earlier (switching on MOSFETs, proximity effect), also copper losses of the PCB are not taken into account in this estimation. Over the complete output region (300 V up to 1000 V, 50 W up to 10 kW output) this results in an average efficiency of 98.6 %, with a minimum of 94.9 %. The peak efficiency is 99.2 % and for power levels down to 10 W the minimum efficiency equals 49.7 %. An overview of the efficiency in the complete output region is given in Figure 7.13. In the region where the input voltage

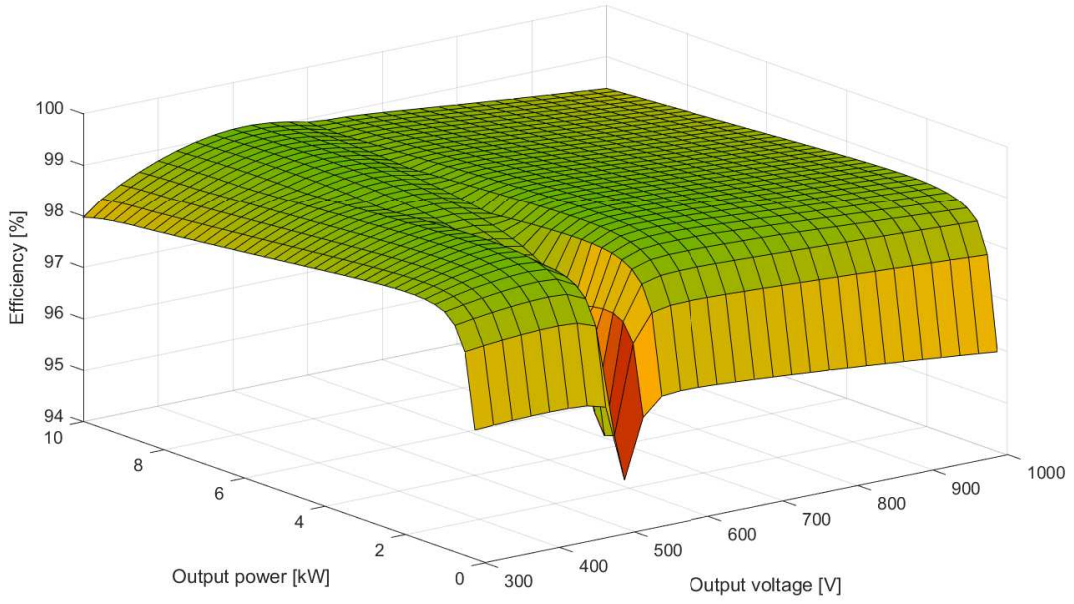


Figure 7.13: Estimated efficiency of the converter in the complete operating area

equals the reflected output voltage ($V_{in} = n \cdot V_{out}$) and trapezoidal current modulation is applied, the largest differences are seen in efficiency with respect to changing power, which is due to the relatively large losses in the transformer core at low powers.

7.6. Summary

In this chapter the design of the converter is finished. In Chapter 5 the turns ratio of the transformer and switches were chosen, in Chapter 6 the transformer and inductor were designed and this chapter the capacitors and heat sink were set. After some parts of the control circuitry were discussed, such as the isolated voltage measurement circuit the PCB was designed in Altium. At the end an overview was given with the estimation of the converter efficiency.

8

Control

This last chapter is dedicated to the programming of the Texas Instruments control board. This control board should trigger all MOSFETs at the right moment in order to create the desired waveforms and power transfer between primary and secondary side. Next to the Texas Instruments control board, a desktop computer is used to interact with. On this computer Simulink will be running, where the user is able to change the settings of the controller. A serial connection between computer and control board will facilitate this communication.

Contents in this chapter

8.1. Communication overview

Firstly, an overview will be given with the signals from the control board to the computer and vice versa. This can be seen in Figure 8.1. On the computer MATLAB Simulink is running where the user can modify

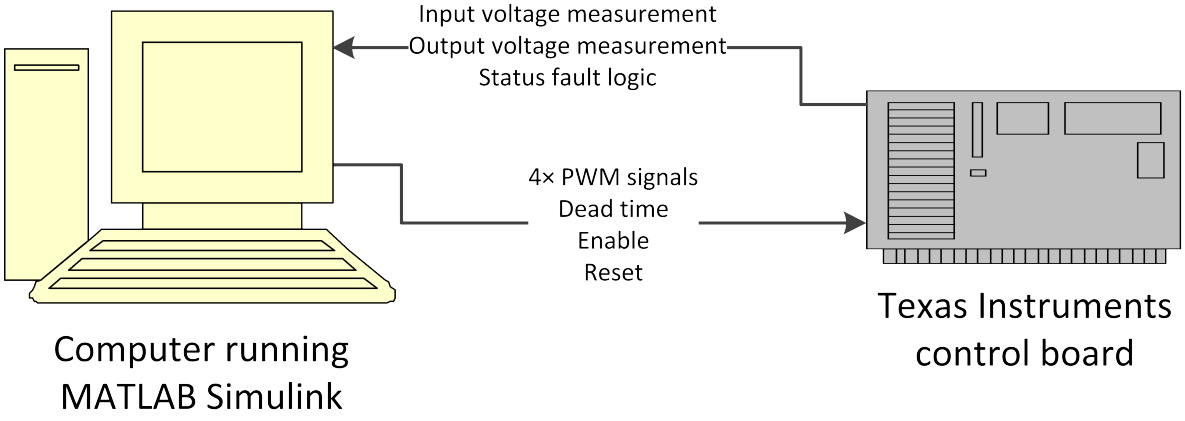


Figure 8.1: Overview of the communication between the computer and control board

the parameters, while the Texas Instruments control board drives the actual converter. The control board will send the measured input and output voltages and the status of the fault logic. The computer will send four signals with information for the control board to generate the actual Pulse Width Modulation (PWM) waveforms for each switch. Given there is always one switch in a leg triggered, transferring only four signals

is sufficient. Next, a signal for the dead time is send, which is the time there is no switch conduction in a single leg between transitions. Lastly there are two more signals, one called *enable* to either enable or disable the converter and one to reset the converter after a fault. All signals will be transferred as *INT16* data type.

8.2. Texas Instruments control board

Then the programming of the control board, starting with the data that will leave the board and will be transmitted to the computer. The voltage measurements are nothing more than a simple Analogue to Digital Converter (ADC) read out and a digital input for the trip zone signal connected to the fault logic. Everything will be send and received using the Serial Communication Interface (SCI) blocks for the C2000.

Moving on the the main task of the control board, the generation of the PWM signals. First of all a clock is used which should be set to $f_s = 25\,\text{kHz}$, which was the switching frequency. Using the clock frequency of the board ($SYSCLKOUT$, 200 MHz), together with the PWM clock division ($EPWMCLKDIV$,2) the number of count per period can be calculated using Equation (8.1):

$$\text{Counts per period} = \frac{\text{SYSCLKOUT}}{\text{EPWMCLKDIV} \cdot f_s} - 1 \tag{8.1}$$

In this case, after 3999 counts a new period will start. The next thing required for the generation of the PWM signals is the duty cycle. Referring back to Chapter 4, all duty cycles are constant and 50 %. However, they all have a different offset, depending on the operation. Information about this offset will be received from the computer. The computer will calculate this value in clock counts, which is convenient given the *INT16* data type. What remains for the controller, is triggering the top switch after the calculated offset and after half a period the other (bottom) switch. This is done, by adding half the number of counts a period to the received offset value, followed by a modulo operation on the number of clock counts a period. In this way the set and clear signals for a counter comparison are obtained. Using blocks in Simulink, this will look like Figure 8.2. The duration of the dead band will also be in counts and this value can be modified using the computer. The

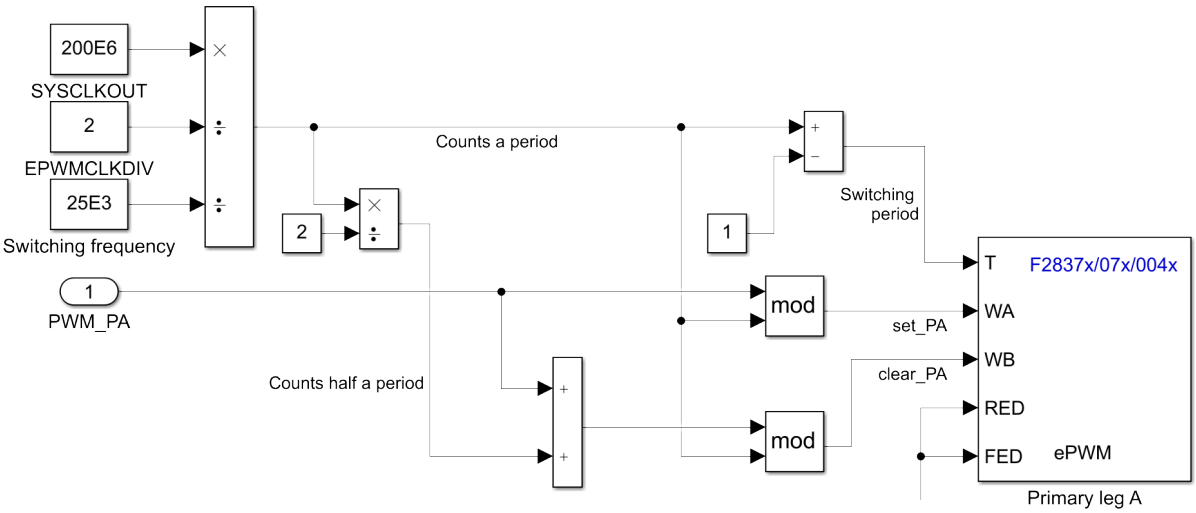


Figure 8.2: Generating a PWM signal

default value will be set to 200 ns, which are 20 clock counts. The deviation from this default value will be obtained from the computer. Lastly, the received *enable* and *reset* signals are connected to a digital output block. The correct GPIO (General Purpose Input Output) ports can be found in [41].

There were also two onboard LEDs present on the control board. The blue is configured to light up if the program on the controller is ready, while the red one will light up if the *enable* signal from the computer is received. A complete overview of the Simulink block diagrams can be seen in Appendix G.1.

8.3. Computer

The second part of the control consists of the program running on the computer. This program mainly calculates the offset values based on given parameters from the user. It has two modes of operation:

- Auto: user sets the power level and the program determines based on the input and output voltages the operating mode (triangular or trapezoidal) and corresponding phase shift;
- Manual: user chooses the operating mode (triangular or trapezoidal) and enters the phase shift. Input and output voltages can eventually be set manually.

Having these possibilities, the program should be able to perform several different functions.

8.3.1. Voltage measurement

The read value of voltage coming from the ADC of the control board has to be converted to the correct voltage. All different steps in the analogue voltage measuring path has to be taken into account, including the resistive division, gain of the (isolated) operational amplifier and the resolution of the ADC (12 bits [41]). To transform the read digital value to the real voltage, a factor of about 3.6 is needed, see Table 8.1. However, it is best to apply a few different voltages, measure these levels with a multimeter and determine the precise correction factor.

Table 8.1: Overview of the stages in the voltage measuring circuit

Stage	Range
At the high power side	0 V - 1000 V
After the resistive division	0 V - 0.22 V
After the isolated operational amplifier	0 V - 2.9 V
After the differential amplifier	0 V - 2.9 V
At the input of the analogue to digital converter	0 V - 2.9 V
Digital value at the TI control board	0 - 3600
Digital value received at the computer	0 - 3600

8.3.2. Determine operating mode

In automatic mode, the program itself should determine if triangular or trapezoidal current modulation should be used. This is done by running a MATLAB script called from Simulink. This one determines the maximum power the converter can transfer under triangular current modulation. If the to be transferred power is less, it chooses triangular, otherwise trapezoidal. Next to this, it gives the corresponding phase shift. All will be determined from the equations derived in Chapter 4.

8.3.3. Determining offsets

Given the phase shift, the offsets for each leg should be found. This can be done by finding the moment the upper switch turns on. This differs for each operating mode. Using which switches are triggered when, as well as the corresponding durations of all intervals provided in Chapter 4, these offsets can be calculated. These offsets are finally converter to clock counts and these values will be transmitted as *INT16* to the control board.

8.3.4. User interface

In order to allow the user to change all parameters, some switches in signal paths are added and the user interface is built to control the converter. The user interface is shown in Figure 8.3. On the top left the user can specify the operating mode and the dead time in nanoseconds. If the operating mode is set to automatic, in the top middle one can enter the to be transferred power in watts. If one has selected a manual operating mode, in the top right the phase shift (between π and $-\pi$) can be set as well as the input and output voltages. For the voltages it is also possible to use the measured values. On the bottom left one finds the switch for turning on and off the converter, as well as a reset button in case a fault occurred. Furthermore displays the converter the operating mode, input and output voltages, actual phase shift, if the PWM is enabled and if the fault logic was triggered.

An overview of the Simulink block diagrams can be found in Appendix G.2. Note that these models are not yet tested on the specific hardware, so keep in mind to verify the operation carefully.

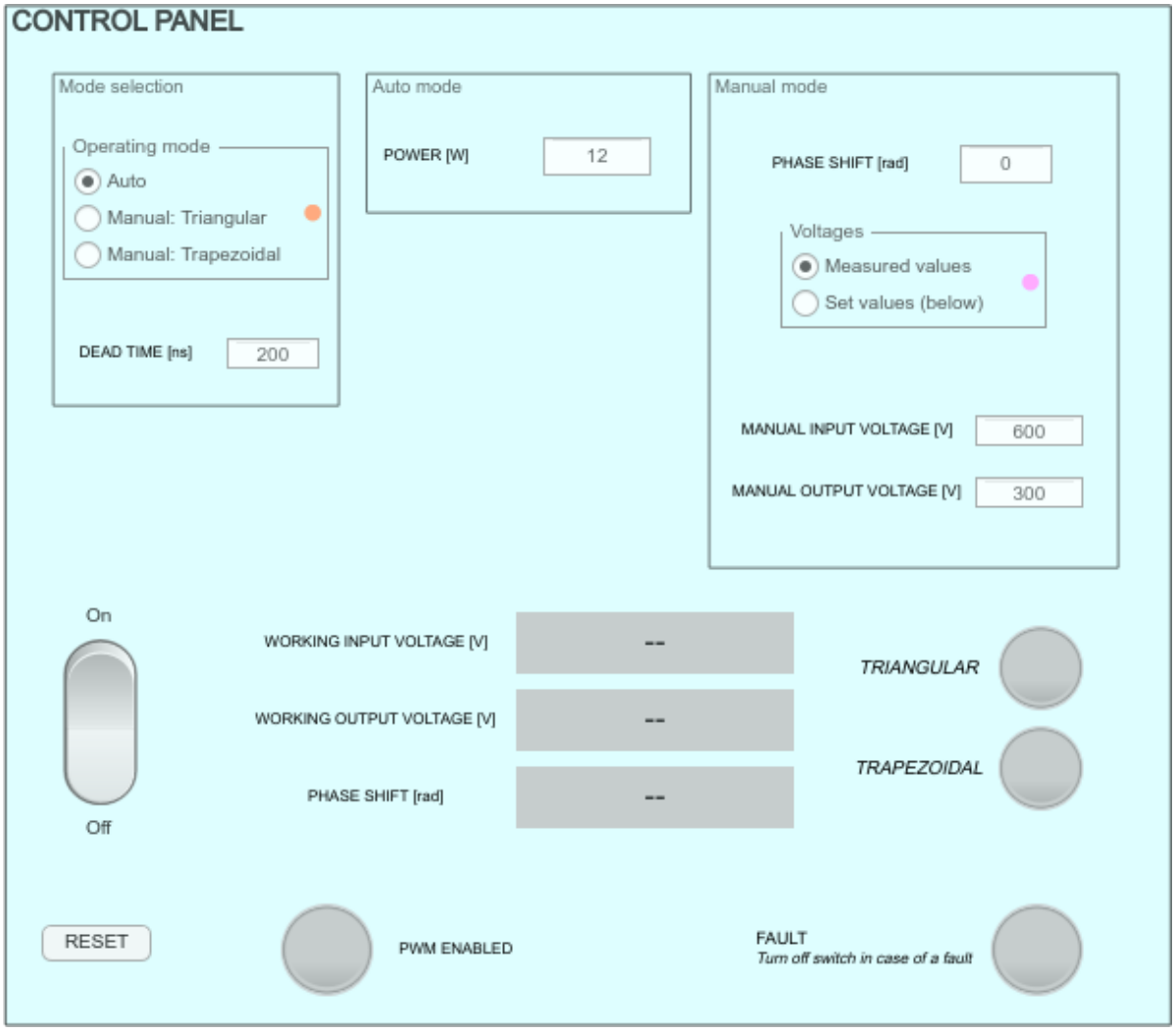


Figure 8.3: User interface of the Simulink model

9 Conclusion

In this thesis the goal was to design a bidirectional DC-DC converter with a wide output voltage range. At every output voltage between 300 V and 1000 V, any amount of power up to 10 kW should be transferred.

Firstly a literature review was done and different converter topologies were discussed. From this overview, the Dual Active Bridge (DAB) converter was chosen as most promising. This topology was first explored with the rectangular current modulation, which was the most popular and easy modulation scheme. While investigating the performance, the zero voltage switching region under rectangular current modulation was found to be too narrow. given the requirement on the wide output voltage and it was expected the resulting losses were too high. Therefore, two more modulation schemes were investigated, namely the triangular and trapezoidal current modulation. Together these modulation schemes were capable of providing zero voltage switching covering the complete operating region.

With the topology and modulation techniques clear, the design of the converter started. Firstly, by choosing a transformer turns ratio. This turns ratio was chosen after iteratively finding the ratio with the lowest current stress. Then, two switches were compared in terms of losses, a MOSFET and an IGBT. The conduction losses and switching losses were for each individual case calculated based on information from the datasheet, where dependencies on current, voltage and junction temperature were taken into account. Based on the thermal limits of the devices, the maximum switching frequency was determined, which was then compared to a preferable range. Based on the expected losses, the MOSFET was finally preferred over the IGBT.

The design of the magnetic components followed. Firstly, the transformer was designed, the leakage inductance calculated and the remaining inductance was added by an inductor which was designed next. For this design, a core database was made and formulas for flux density, losses and efficiency were put all together in an Excel file. This enabled the possibility for changing parameters and directly seeing the results. Both the transformer and inductor were designed for three different frequencies, which together with the semiconductor losses an overview was created to evaluate the losses at each switching frequency. The overall losses did not vary considerably and 25 kHz was chosen as the switching frequency.

After choosing a set of capacitors and a proper heat sink for the semiconductors, the schematics of the control logic were finished and the PCB was designed. An estimation was done for the efficiency of the designed converter, with a resulting average efficiency of 98.6 %.The last chapter in this thesis was dedicated to the programming of the Texas Instruments control board.

Overall the project ended with a finished design of a bidirectional DC-DC converter with a wide output voltage range. The DAB was chosen with triangular and trapezoidal current modulation. MOSFETs were chosen to reduce the losses and thereby increasing the expected efficiency. The efficiency of the converter over the operating range is evaluated. Prototype including the PCB and the control is made according to the design.

9.1. Future work

The last part of this thesis originally was the building and testing of the converter and measuring the performance. The converter can be build on the designed PCB, the list of required components is found in Appendix F and the components can be placed according to the schematics in Appendix E. A testing plan is furthermore available in Appendix H.

After the building, testing and measuring are done, the origin of all losses can be determined. In this way conclusions can be drawn if all calculations and estimations were valid. For example if it also in practise holds true that all turn on switching transitions can be assumed lossless. Furthermore, generating detailed information about the efficiency for all operating points (output voltages and power) can be useful for using this converter on a more system level.

If one might need to charge with a larger power than 10 kW, multiple converters can be placed in parallel. By optimising the spreading of the loads across different parallel placed converters, a higher overall efficiency can be obtained, as well as a lower output voltage ripple.

Another idea is to try other switching frequencies by choosing another magnetic design, or completely redo the design of the magnetics in more detail or with other constrains involved, such as a maximum volume of the transformer.

A

List of Abbreviations

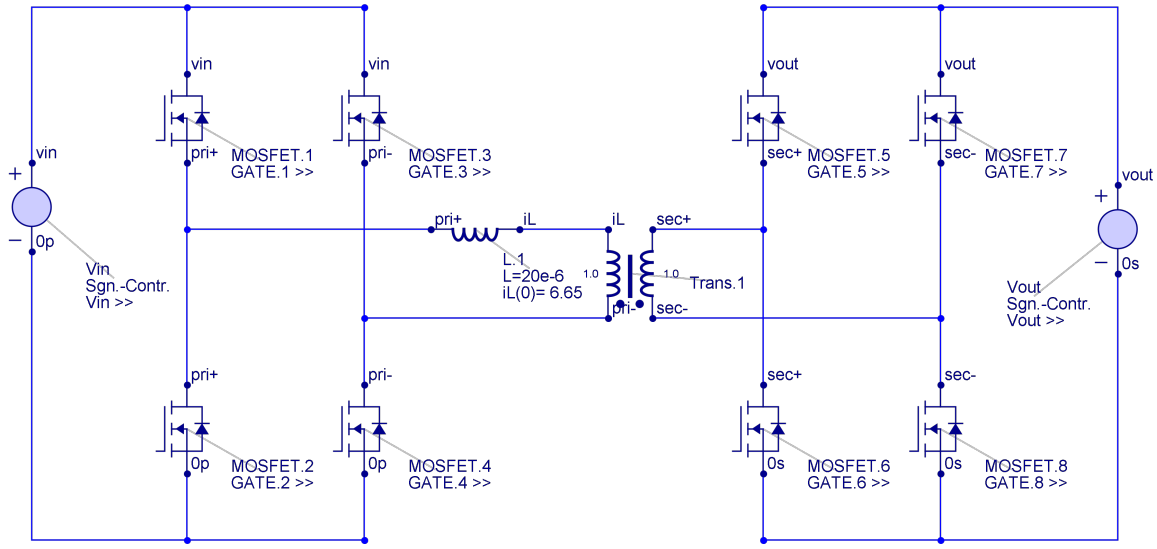
A list of all abbreviations and their meaning used in this master thesis is given below:

Abbreviation	**Meaning**
AC	Alternating Current
ADC	Analogue to Digital Converter/ Conversion
AP	Area Product of the (magnetic) core (A_e) and window (A_w) area
BH-curve	Curve of the flux density (B) and magnetic field density (H)
CC	Constant Current (charging of a battery)
CV	Constant Voltage (charging of a battery)
DAB	Dual Active Bridge
DC	Direct Current
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance (capacitor)
EV	Electric Vehicle
fsL-product	Product of switching frequency f_s and inductance L
G2V	Grid to Vehicle
GPIO	General Purpose Input Output
HV side	High Voltage side
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
LED	Light Emitting Diode
LV side	Low Voltage side
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PV	Photovoltaic
RMS	Root Mean Square
PWM	Pulse Width Modulation
SCI	Serial Communication Interface
SEV	Stored Energy Value
SMD	Surface Mounted Device
SOC	State Of Charge
V2G	Vehicle to Grid
VA-rating	Voltage-Ampere rating
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

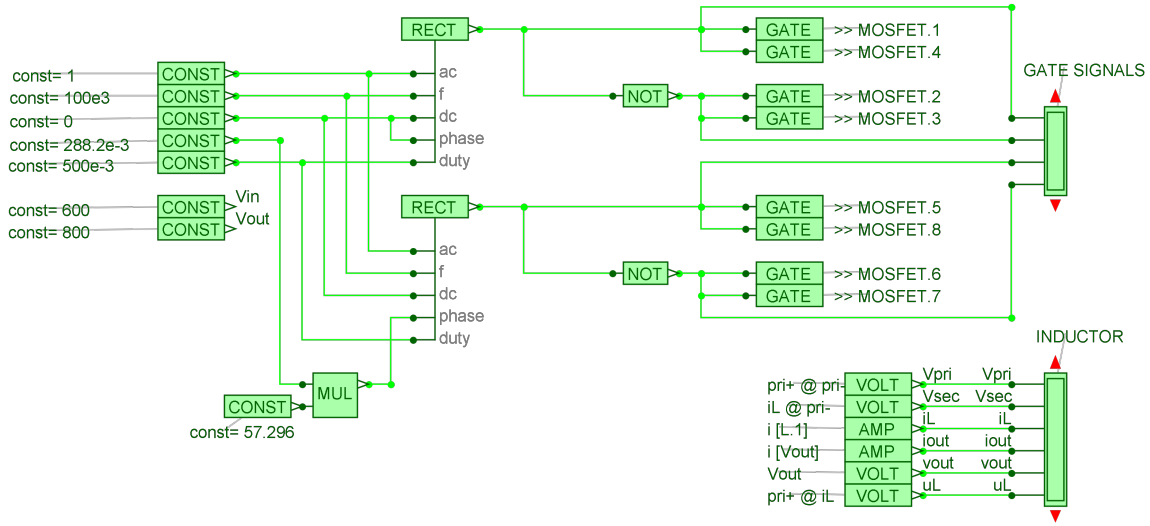
B

Simulation - Rectangular with MOSFETs

Besides simulating the performance of the dual active bridge under rectangular current modulation with two square wave voltage sources and an inductor, it can be simulated with eight MOSFETs, a transformer and an inductor. The MOSFETs of the simulation program are not lossless, where the square wave voltage sources were. The circuit (in blue) and control logic (in green) are given in Figure B.1.



(a) Electrical circuit



(b) Control logic

Figure B.1: Rectangular operation mode in Gecko Circuits using MOSFETs

C

Core database

The core database, based on selected cores from [32] is made in Microsoft Excel. Dimensions of the cores, as well as the effective magnetic path length (l_e), effective and minimum cross section (A_e and A_{min}), effective magnetic volume (V_e) and window area (A_w) are copied from TDK. The remaining core properties, as well as properties of stacked cores are calculated based on the data mentioned earlier. Because of the size of the table, it is split among several individual tables on the coming pages. The last core in the database is an E-core formed by two U-cores, this combination is shown in Figure C.1. By placing the U-cores on their side, the height of the window is increased, allowing a higher number of turns to fit when the number of layers is restricted.

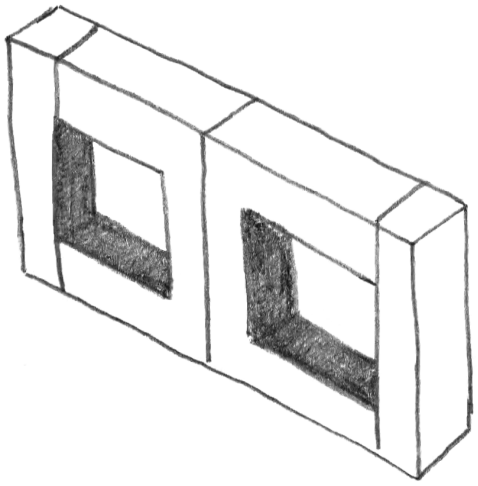


Figure C.1: Combining two U-shaped cores to form an E-core

Table C.1: Core database, part 1

Core type, eventually stacked	Materials ungapped	l_e (mm) effective magnetic path length	A_e (mm^2) effective magnetic cross section	A_{min} (mm^2) minimum cross section	V_e (mm^3) effective magnetic volume	A_w (mm^2) window area	l_N (mm) average turn length	AP (mm^4) area product	A_c (mm^2) total outside area	$A_{c,v}$ (mm^2) vertical outside area
E56/24/19	N27 & N87	107	340	327	36,400	204	113	69,190	12,929	8587
E55/28/25	N27 & N87	124	420	420	52,100	280	125	117,600	15,441	10,464
E65/32/27	N27 & N87	147	535	529	78,650	415	144	222,025	21,043	14,357
E70/33/32	N27 & N87	149	683	676	102,000	445	161	303,935	24,373	16,204
E80/38/20	N27 & N87	184	390	388	71,800	844	159	329,160	28,144	19,379
E65/32/27 (2×)	N27 & N87	147	1070	1058	157,300	415	308	444,050	28,200	17,952
UI93/104/16	N27 & N87	258	448	448	116,000	530	160	237,440	45,158	25,866
E70/33/32 (2×)	N27 & N87	149	1366	1352	204,000	445	353	607,870	33,135	20,454
E80/38/20 (2×)	N27 & N87	184	780	776	143,600	844	280	658,320	34,487	22,490
UI93/104/20	N27 & N87	258	560	560	144,000	530	168	296,800	47,011	26,698
UI93/104/30	N27 & N87	258	840	840	217,000	530	257	445,200	51,643	28,778
E70/33/32 (3×)	N27 & N87	149	2049	2028	306,000	445	673	911,805	41,896	24,703
E80/38/20 (3×)	N27 & N87	184	1170	1164	215,400	844	482	987,480	40,829	25,600
UI93/104/16 (2×)	N27 & N87	258	896	896	232,000	530	325	474,880	52,569	29,194
UI93/104/20 (2×)	N27 & N87	258	1120	1120	288,000	530	357	593,600	56,275	30,858
UI93/104/30 (2×)	N27 & N87	258	1680	1680	434,000	530	437	890,400	65,539	35,018
UI93/104/30 (2× as E)	N27 & N87	258	1680	1680	434,000	530	435	890,400	92,591	55,856
UI126/119/20	N87	354	560	560	198,000	3996	376	2,237,480	100,769	48,595
UI126/119/20 (2×)	N87	354	1120	1120	396,000	3996	496	4,474,960	113,369	53,355
UI126/119/20 (2× as E)	N87	354	1120	1120	396,000	3996	498	4,474,960	155,340	89,149

Table C.2: Core database, part 2

Core type, eventually stacked	h (mm) height	w (mm) width	d (mm) depth	h_w (mm) height window	w_w (mm) width window	R_{rad} (KW^{-1}) radiative thermal resistance	R_{conv} (KW^{-1}) convection thermal resistance	R_{th} (KW^{-1}) total thermal resistance
E56/24/19	47.2	56.1	18.8	29.2	9.65	9.32	14.55	5.68
E55/28/25	55.6	55	25	37	10.15	7.81	12.44	4.80
E65/32/27	65.6	65	27.4	44.4	12.1	5.73	9.45	3.57
E70/33/32	66.4	70.5	32	43.8	13	4.95	8.40	3.11
E80/38/20	77	80	20.2	55.8	19.35	4.28	7.29	2.70
E65/32/27 (2×)	65.6	65	54.8	44.4	12.1	4.27	7.56	2.73
UI93/104/16	104	93	16	48	34.6	2.67	5.89	1.84
E70/33/32 (2×)	66.4	70.5	64	43.8	13	3.64	6.65	2.35
E80/38/20 (2×)	77	80	40.4	55.8	19.35	3.50	6.28	2.25
UI93/104/20	104	93	20	48	34.6	2.56	5.70	1.77
UI93/104/30	104	93	30	48	34.6	2.33	5.29	1.62
E70/33/32 (3×)	66.4	70.5	96	43.8	13	2.88	5.51	1.89
E80/38/20 (3×)	77	80	60.6	55.8	19.35	2.95	5.52	1.92
UI93/104/16 (2×)	104	93	32	48	34.6	2.29	5.22	1.59
UI93/104/20 (2×)	104	93	40	48	34.6	2.14	4.93	1.49
UI93/104/30 (2×)	104	93	60	48	34.6	1.84	4.35	1.29
UI93/104/30 (2× as E)	104	186	30	48	34.6	1.30	2.73	0.88
UI126/119/20	119	126	20	63	70	1.20	3.24	0.87
UI126/119/20 (2×)	119	126	40	63	70	1.06	2.95	0.78
UI126/119/20 (2× as E)	119	252	20	70	63	0.78	1.77	0.54

D

Simulation - Triangular and trapezoidal

Given the decision to use both the triangular and the trapezoidal current modulation, one simulation file is made in Gecko Circuits which can use both. Previously in the simulations the phase shift should be set, however, in this simulation one sets only the power level. The value of the resistor should then be calculated accordingly with the equation provided. The control logic computes then the corresponding phase shift and the operating mode (triangular or trapezoidal). Furthermore, with this simulation model it is only for verification of a power flow form the grid to the car and not the other way around. Therefore the voltage source one the left should be swapped with the resistor and capacitor on the right. With this simulation it also possible to set a dead time, as well as to see the resulting voltage ripple on the output. For the MOSFETs a loss model is used derived from the datasheet.

D.1. Electrical circuit

The electrical circuit for this simulation is given in Figure D.1.

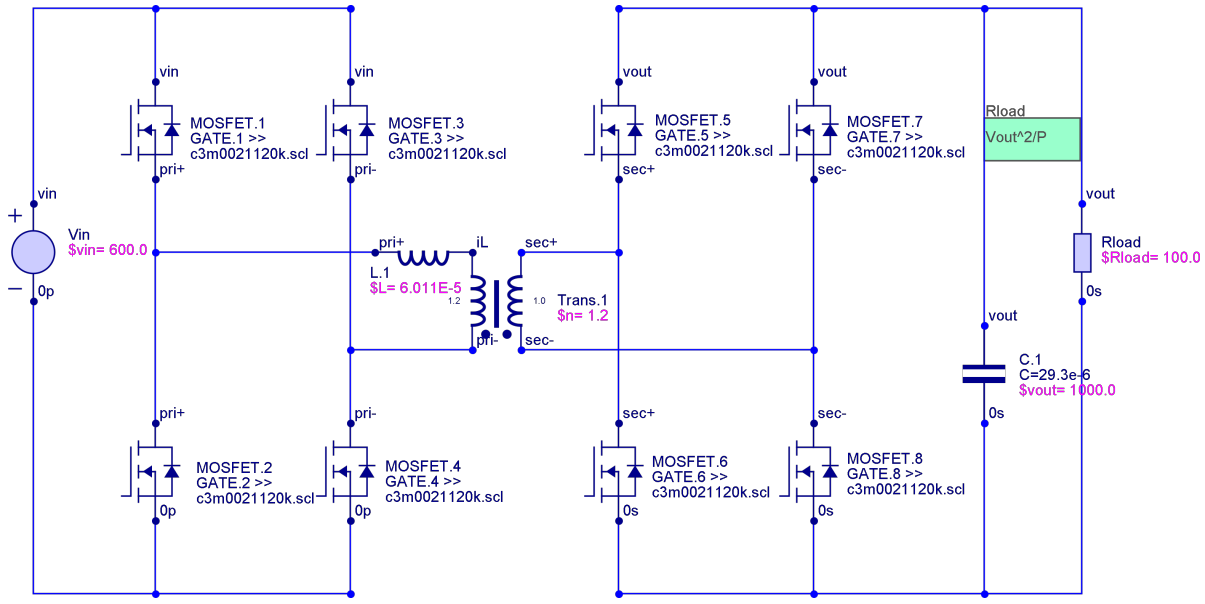


Figure D.1: The electrical circuit of the DAB in Gecko Circuits

D.2. Control circuit

Next, the slightly more complicated control logic is given in Figure D.2, Figure D.3 and Figure D.4.

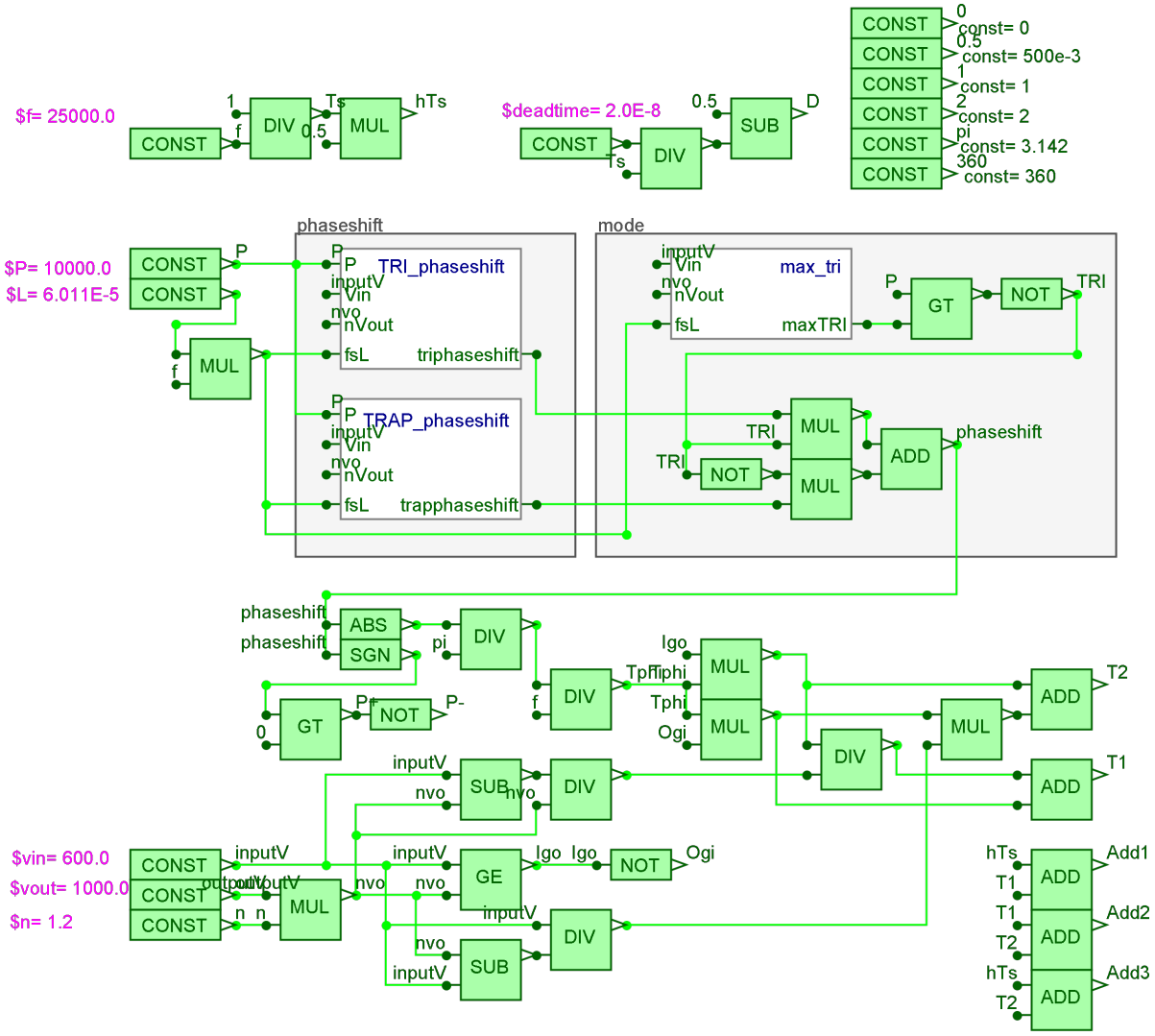


Figure D.2: The control logic determining the phase shift and triangular waveforms

The sub circuits for determining the triangular phase shift, trapezoidal phase shift and the border between triangular and trapezoidal operating mode are given in Figure D.5, Figure D.6 and Figure D.7 respectively.

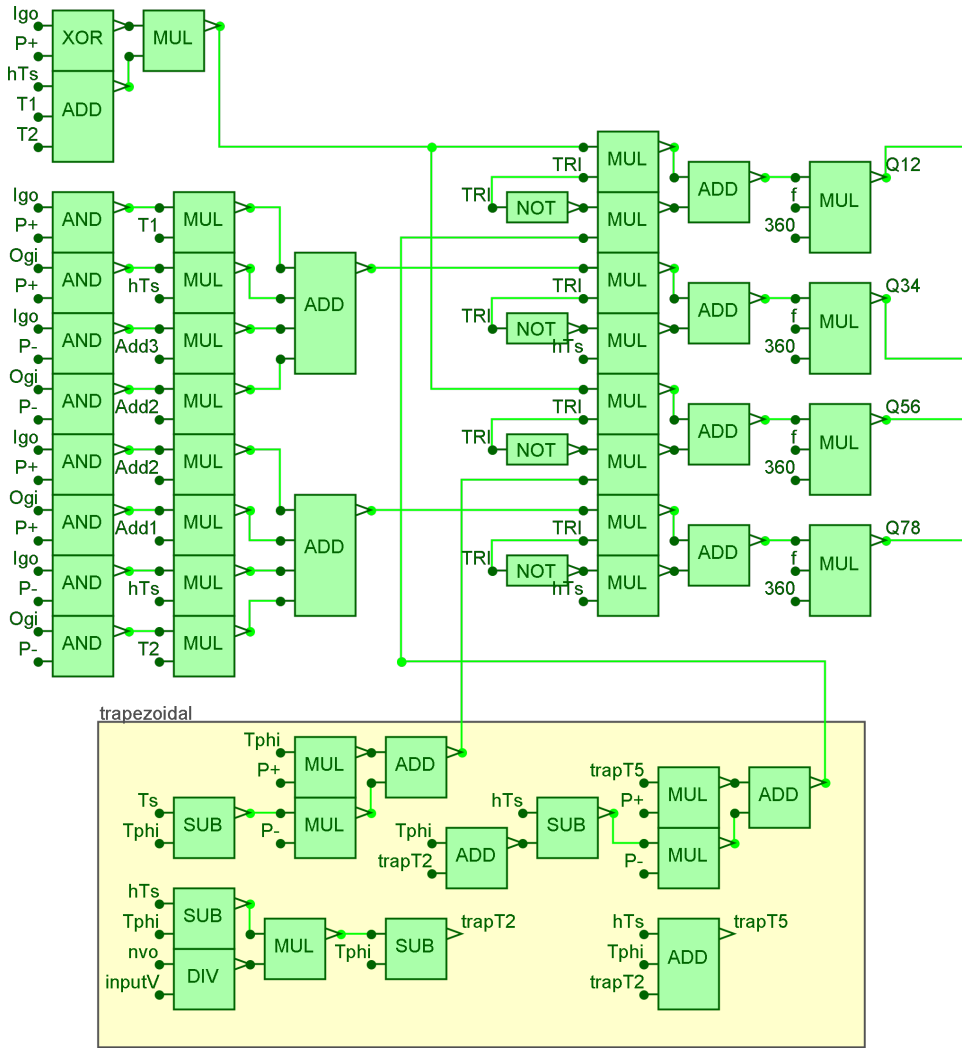


Figure D.3: The control logic determining trapezoidal waveforms

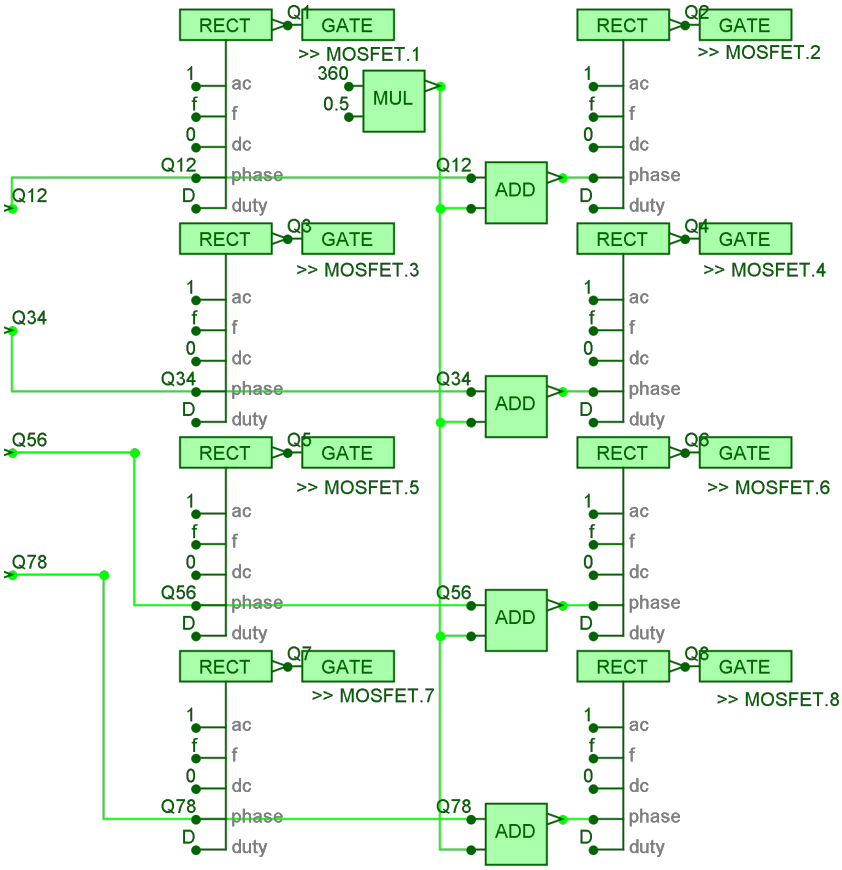


Figure D.4: The control logic for the gate signals

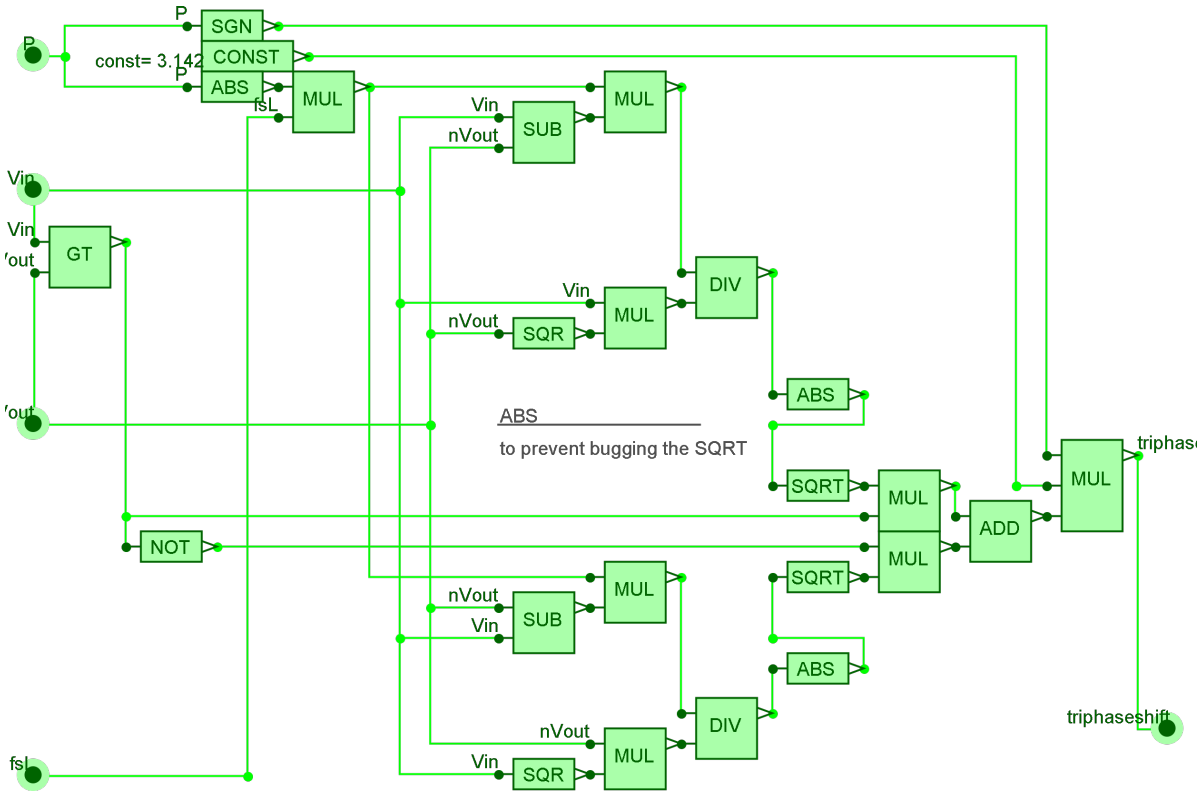


Figure D.5: The sub circuit for determining the triangular phase shift

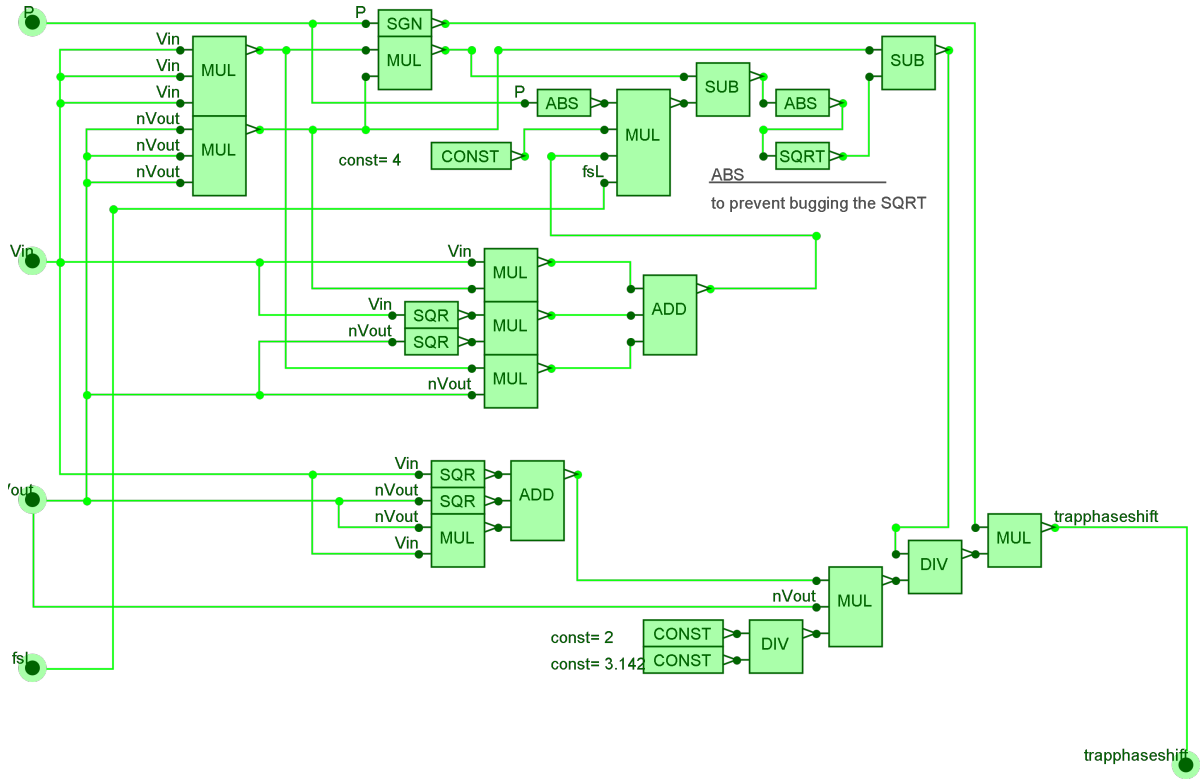


Figure D.6: The sub circuit for determining the trapezoidal phase shift

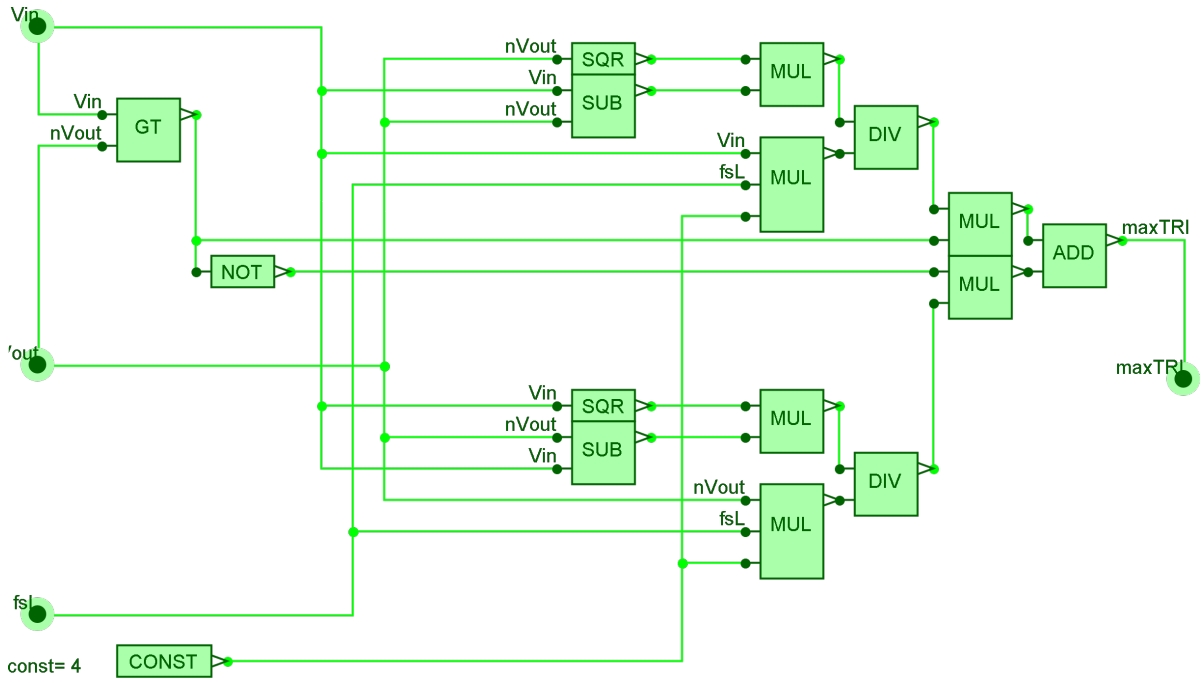


Figure D.7: The sub circuit for the border between triangular and trapezoidal operating mode

D.3. Measurement scopes

The blocks for measuring the signals are finally given in Figure D.8.

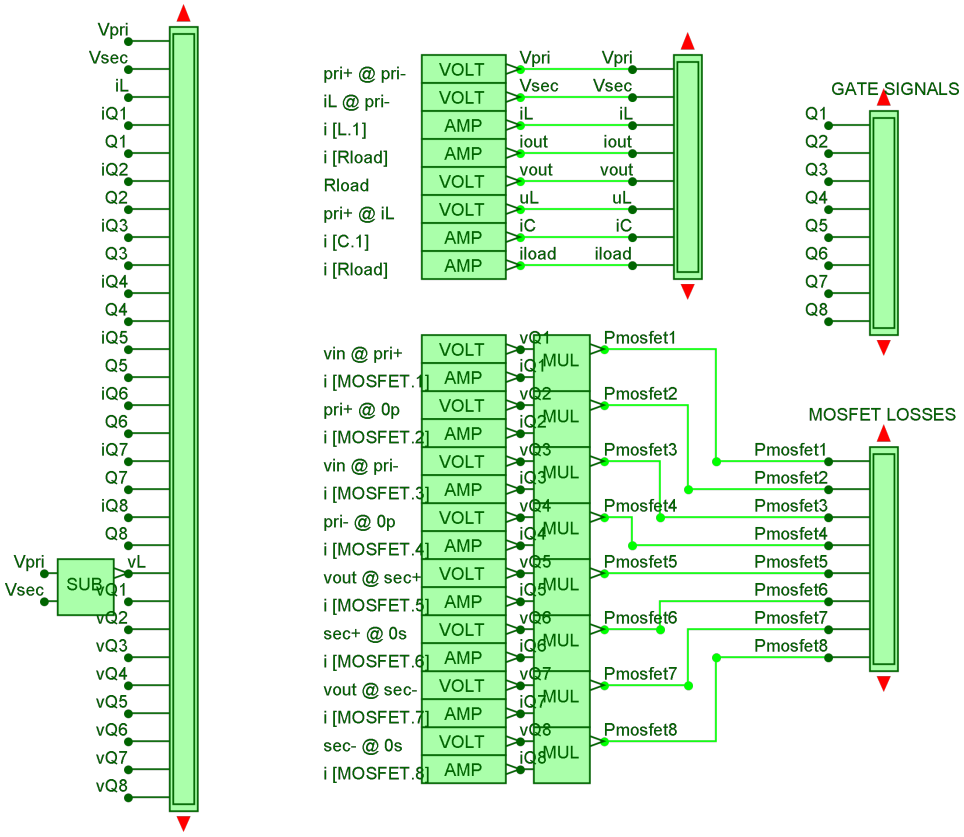


Figure D.8: Scopes in the simulation

E

Schematics

The drawn schematics in Altium Designer.

E.1. Control circuit power

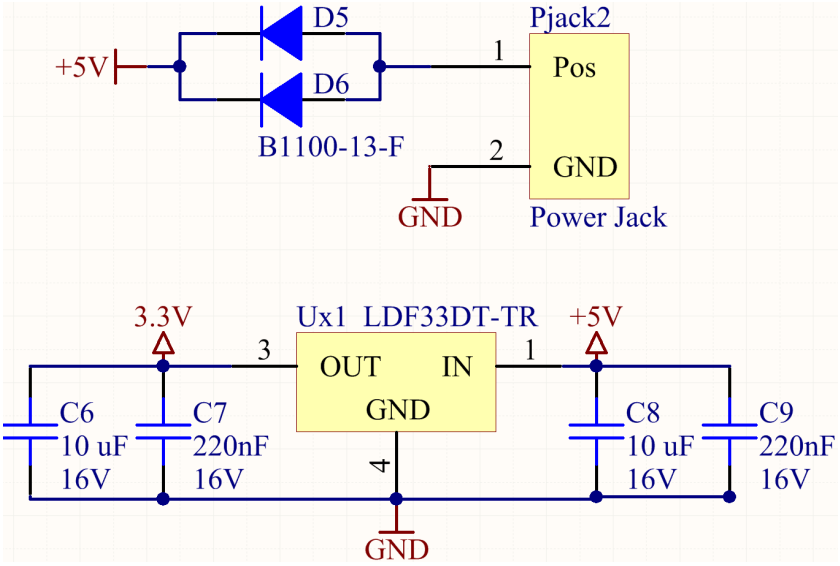


Figure E.1: Power to the control parts

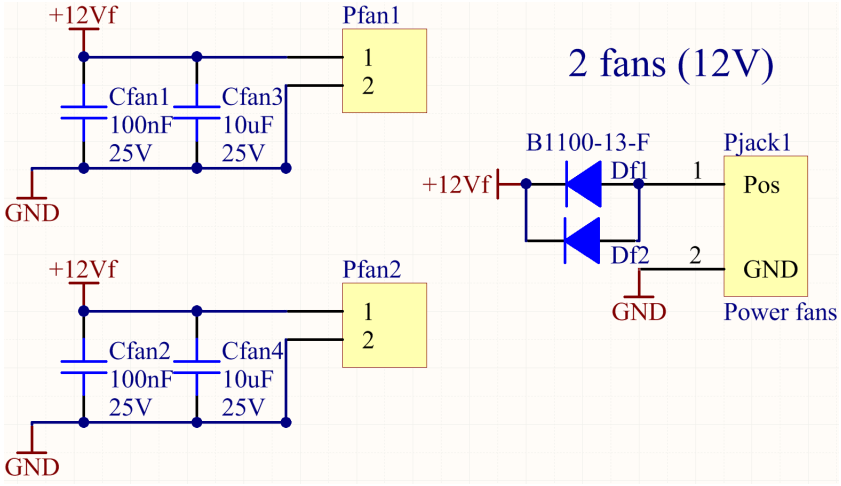


Figure E.2: Power to the fans

E.2. Isolated voltage measurement

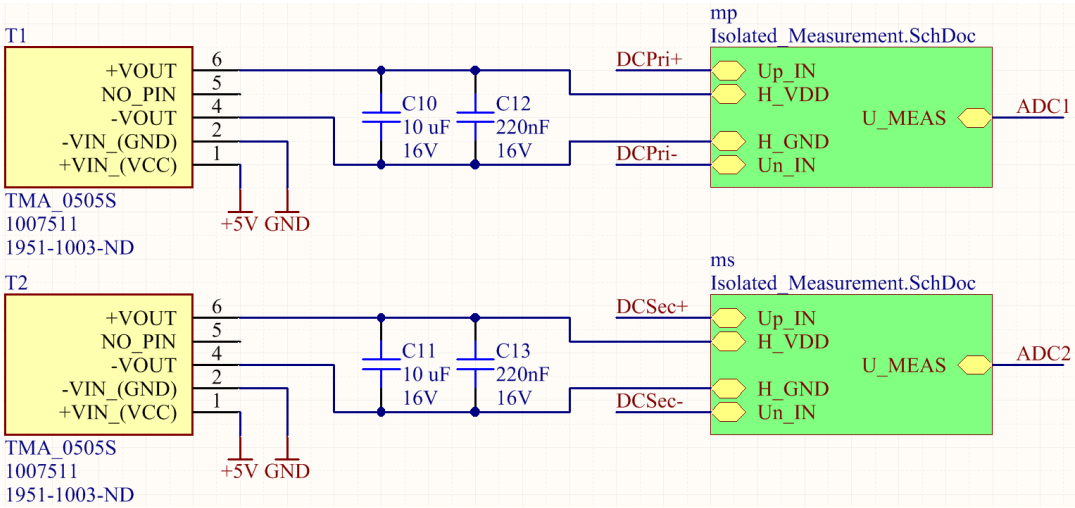


Figure E.3: Isolated power to the voltage measurement

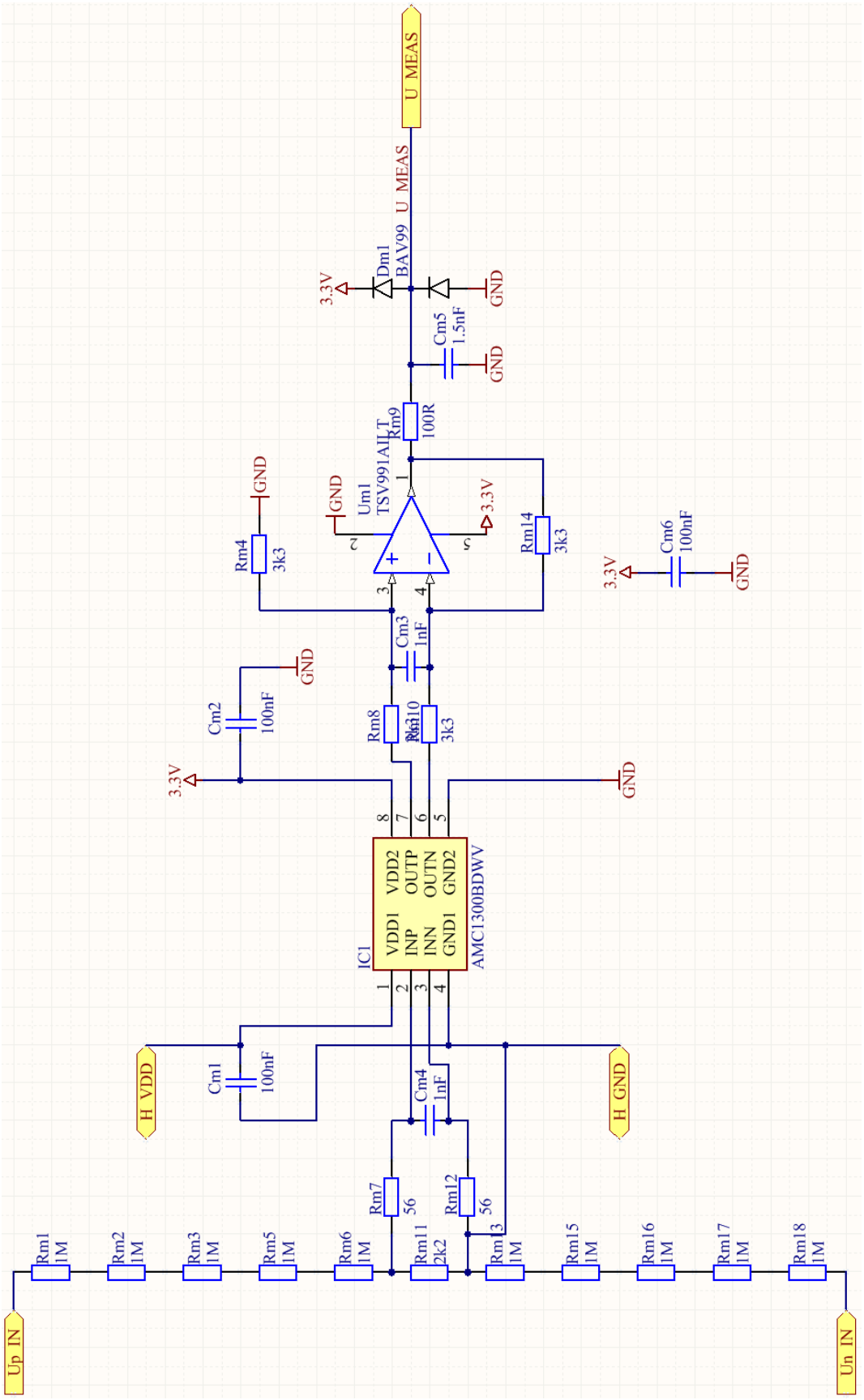


Figure E.4: Isolated voltage measurement

E.3. Current measurement

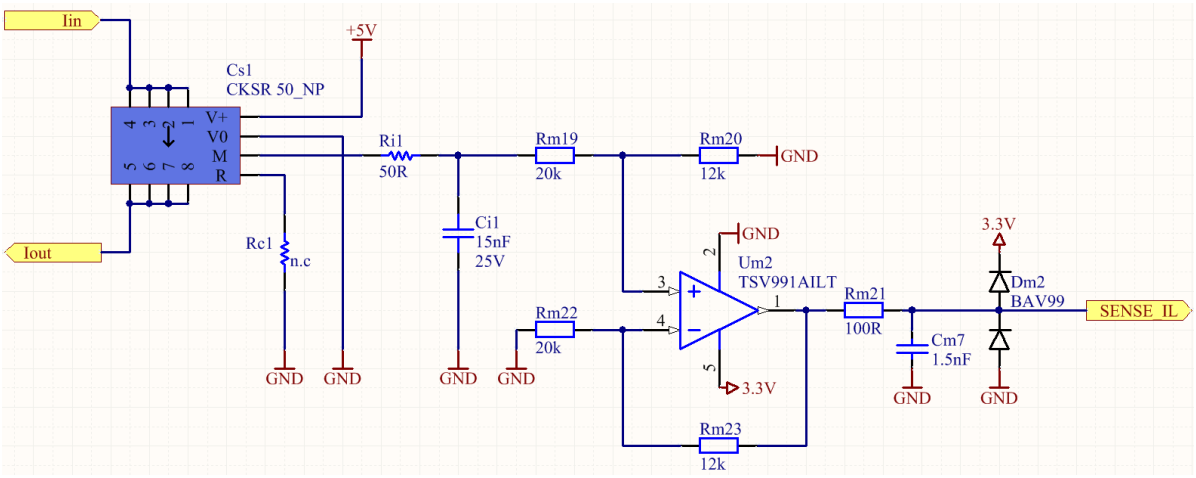


Figure E.5: Current measurement

E.4. Full bridge

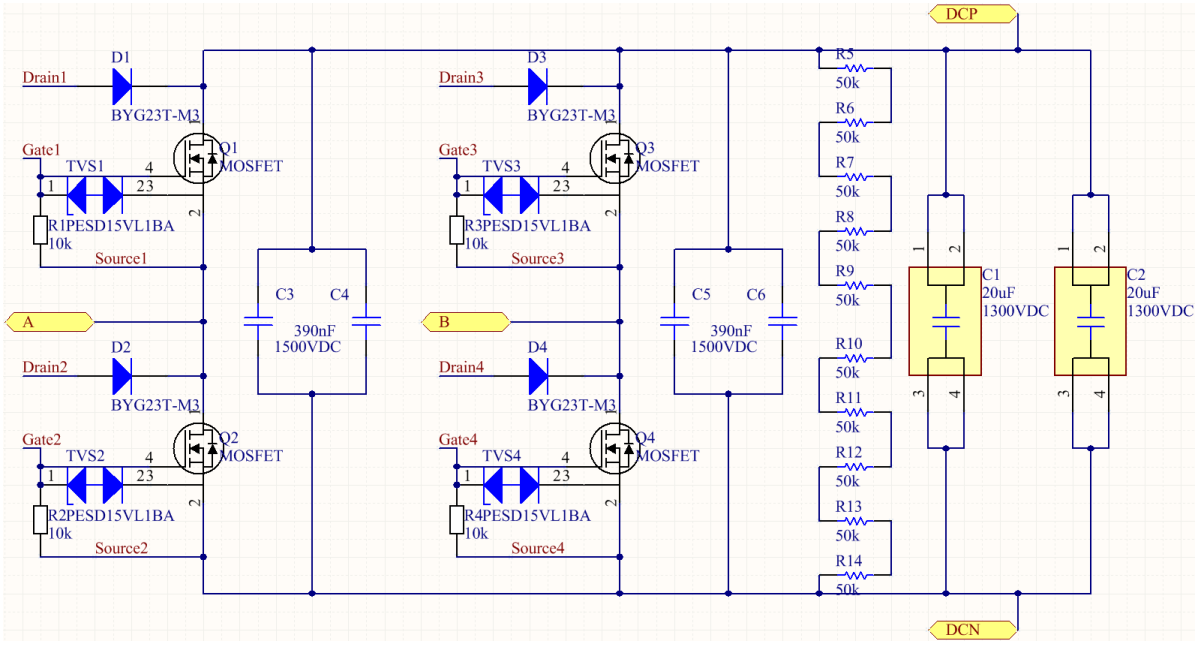


Figure E.6: Full bridge

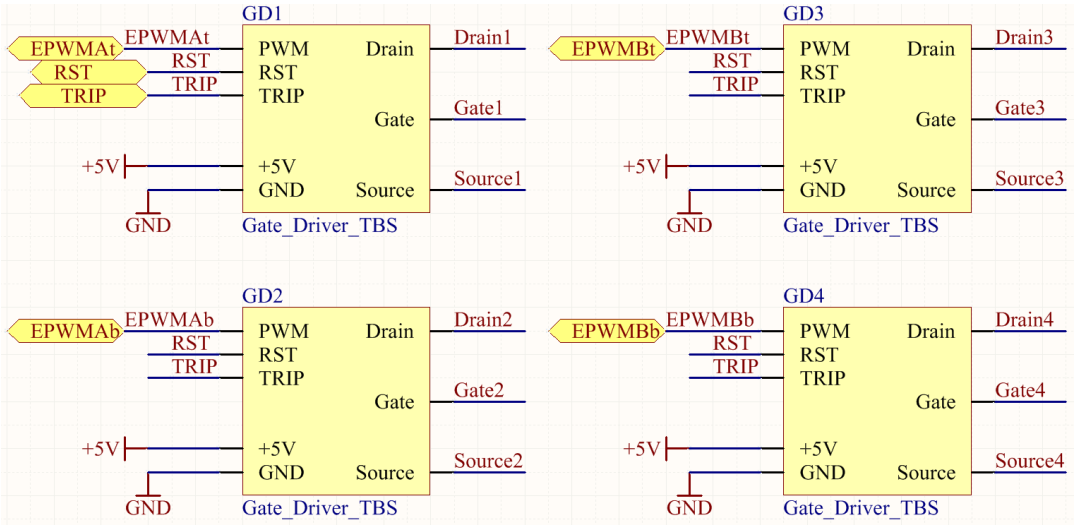


Figure E.7: Gate drivers of the full bridge

E.5. Control

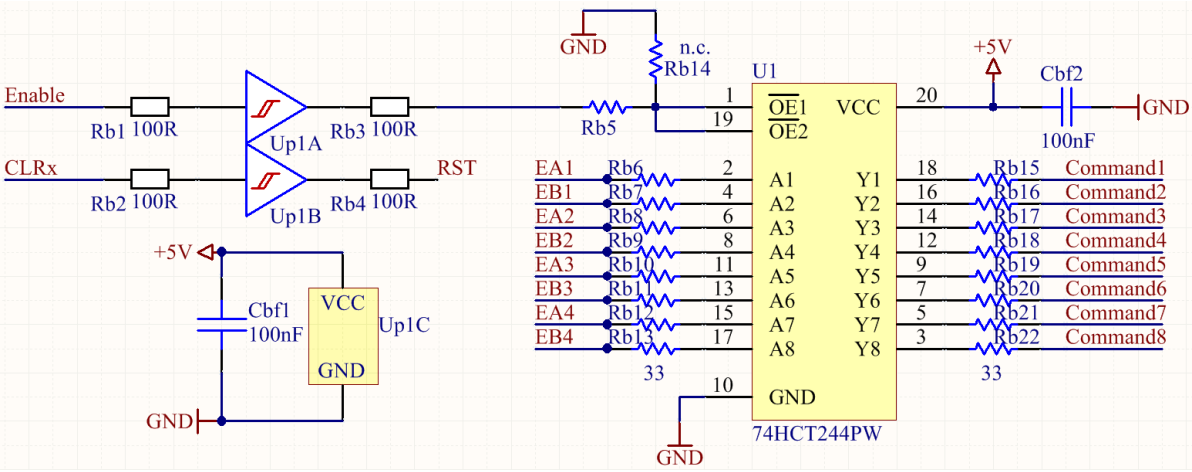


Figure E.8: Connections around the 74HCT244PW for enabling PWM signals

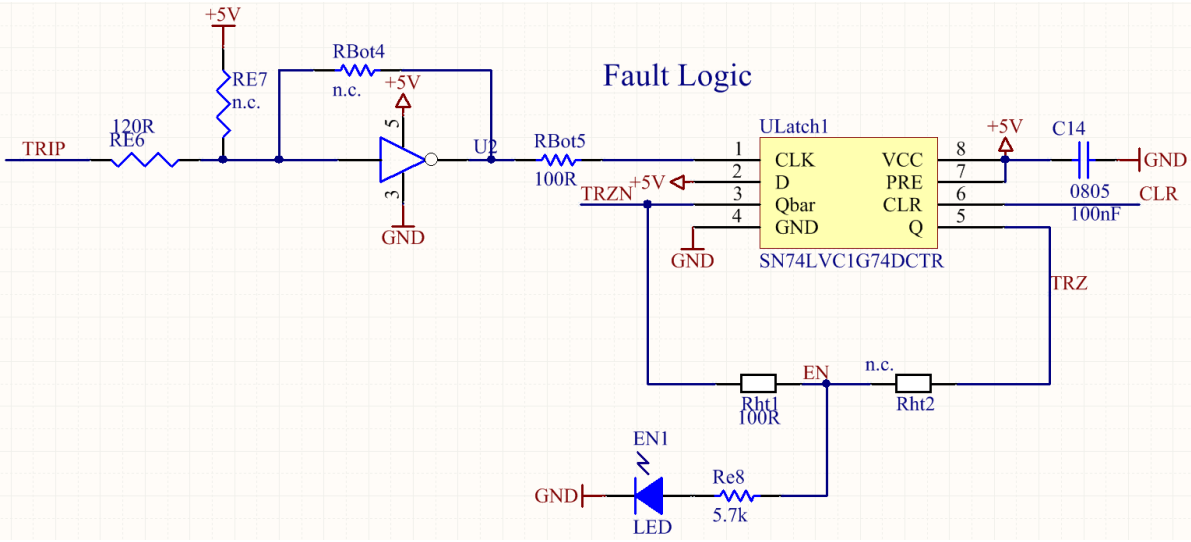


Figure E.9: Fault logic

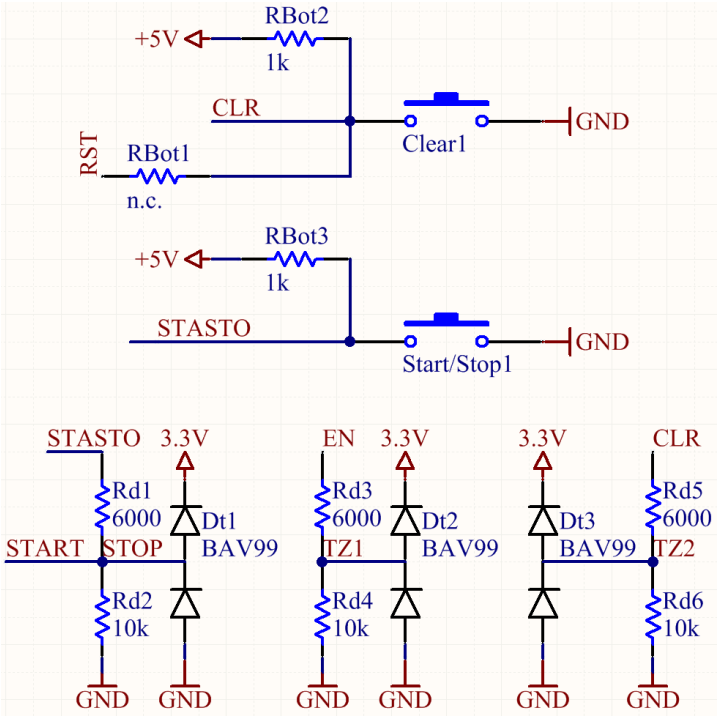


Figure E.10: Signals to the TI controller

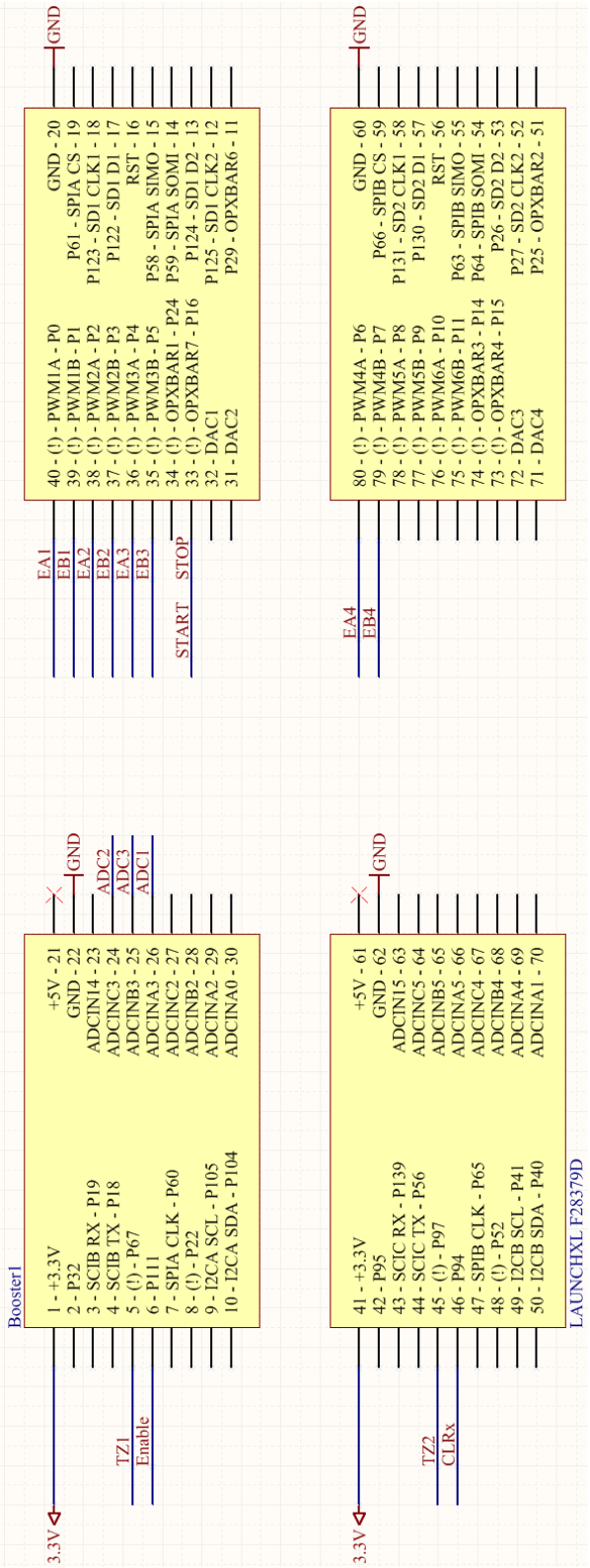


Figure E.11: Connections to the TI F28379D control board

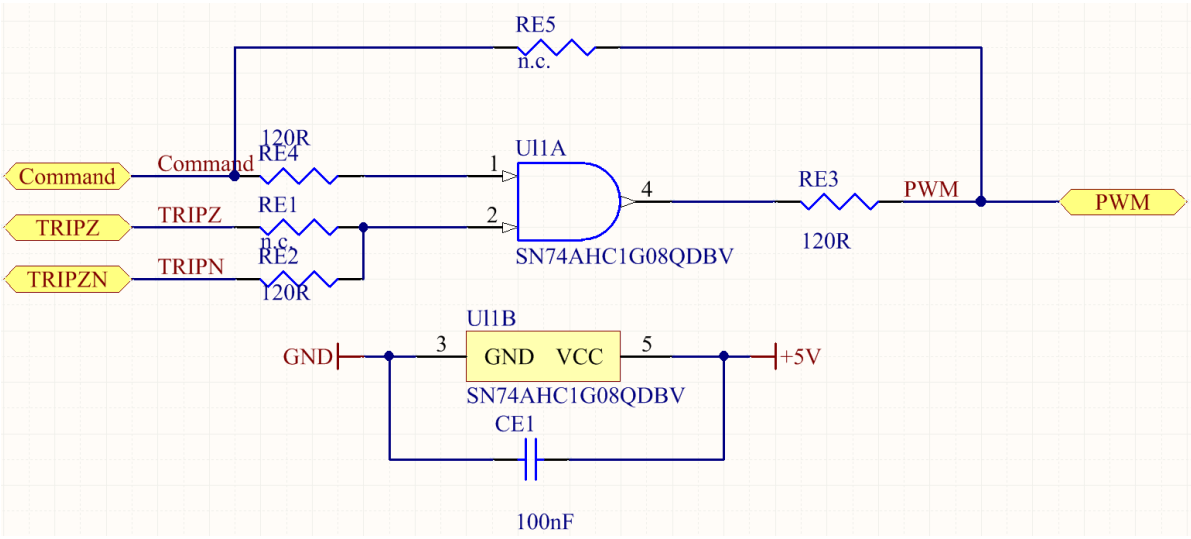


Figure E.12: AND logic to interrupt the gate drivers in case of a failure

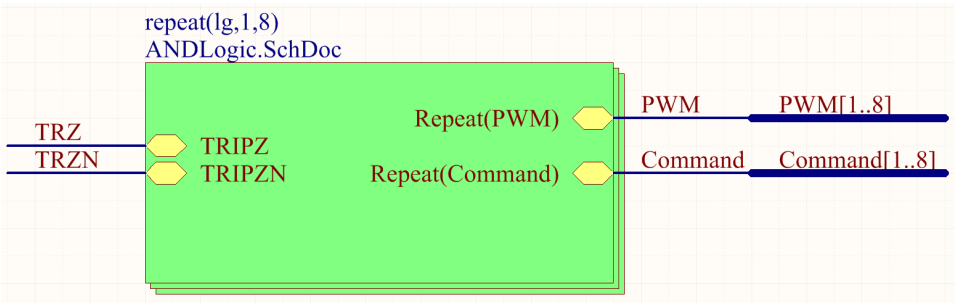


Figure E.13: AND logic to all gate drivers

F

List of components

List of the required components on the PCB is given in Table F.1. Note that this list does not include the materials for the magnetic components. For each component the corresponding identification number (ID) to the supplier (Digi-Key) is given. The gate drivers are separate PCBs with its own components and can therefore not be bought directly from Digi-Key. The pin headers are available at the laboratory, as well as female connectors that can be placed on the end of the wires of the fans. The heat sink and the two fans can be ordered from Fischer Elektronik via the following page: `https://www.fischerelektronik.de/web_fischer/en_GB/heatsinks/D02/Miniature%20cooling%20aggregates/$catalogue/fischerData/PR/LAM5D_K_/search.xhtml`

Table F.1: List of components

Quantity	Component	Value	Digi-Key ID
1	Development board	TI F28379D	296-46713-ND
4	Capacitor	20 µF, 1300 VDC	399-16987-ND
8	Capacitor	390 nF, 1500 VDC	478-8054-1-ND
4	Capacitor	10 µF, 16 V	490-6473-1-ND
4	Capacitor	220 nF, 16 V	490-5418-1-ND
10	Capacitor	100 nF, 50 V	490-11955-1-ND
9	Capacitor	100 nF, 25 V	399-8000-1-ND
2	Capacitor	10 µF, 25 V	490-10503-1-ND
1	Capacitor	15 nF, 25 V	732-8056-1-ND
2	Switch	Nonlocking	679-2428-ND
4	Capacitor	1 nF, 25 V	732-8050-1-ND
3	Capacitor	1.5 nF, 25 V	732-12280-1-ND
1	Current sensor	CKSR 50 NP	398-1098-ND
8	Diode	BYG23T-M3	BYG23T-M3/CT-ND
4	Diode	B1100-13-F	B1100-FDICT-ND
6	Dual switching diode	BAV99	BAV99LT3GOSCT-ND
1	LED		732-4983-1-ND
2	Isolation amplifier	AMC1300B	AMC1300BDWV-ND
12	M3 plug	Wuerth	732-3200-ND
2	Power jack	RAPC722	SC3832-ND
8	MOSFET	C3M0021120K	1697-C3M0021120K-ND
11	Resistor	10 kΩ	RMCF0805FT10K0CT-ND
20	Resistor	50 kΩ, 0.5 W	P49.9KAACT-ND
9	Resistor	100 Ω	RMCF0805FT100RCT-ND
17	Resistor	33 Ω	RMCF0805FT33R0CT-ND
2	Resistor	1 kΩ	RMCF0805FT1K00CT-ND
3	Resistor	6 kΩ	RMCF0805FT6K04CT-ND
25	Resistor	120 Ω	738-RMCF0805FT120RCT-ND
1	Resistor	5.7 kΩ	RMCF0805FT5K76CT-ND
1	Resistor	50 Ω	RMCF0805FT49R9CT-ND
20	Resistor	1 MΩ	RMCF0805FT1M00CT-ND
8	Resistor	3.3 kΩ	RMCF0805FT3K30CT-ND
4	Resistor	56 Ω	RMCF0805FT56R0CT-ND
2	Resistor	2.2 kΩ	RMCF0805FT2K20CT-ND
2	Resistor	20 kΩ	RMCF0805FT20K0CT-ND
2	Resistor	12 kΩ	RMCF0805FT12K0CT-ND
2	Isolated DC-DC converter	TMA 0505S	1951-1003-ND
8	TVS diode	PESD15VL1BA	1727-3812-1-ND
1	Buffer	74HCT244PW	296-26494-5-ND
1	Schmitt trigger	74HCT1G14GW	1727-6057-1-ND
8	AND gate	SN74AHC1G08QDBV	296-23875-1-ND
1	Flip flop	SN74LVC1G74DCTR	296-25553-1-ND
3	Op amp	TSV991AILT	497-5833-1-ND
1	Schmitt trigger	NC7WZ17	NC7WZ17P6XCT-ND
1	Voltage regulator	LDF33DT-TR	497-14661-1-ND
3	2-pin header		
2	2-pin female connector		
8	Gate Driver	TBS	
1	Heat sink	LAM 5 D K 125 12	
2	12V DC FAN	50 × 50 × 10mm	

G

Control - Simulink models

An overview of the Simulink models used for the control, starting with the model used on the control board, next for the one that runs on the computer.

G.1. Control board

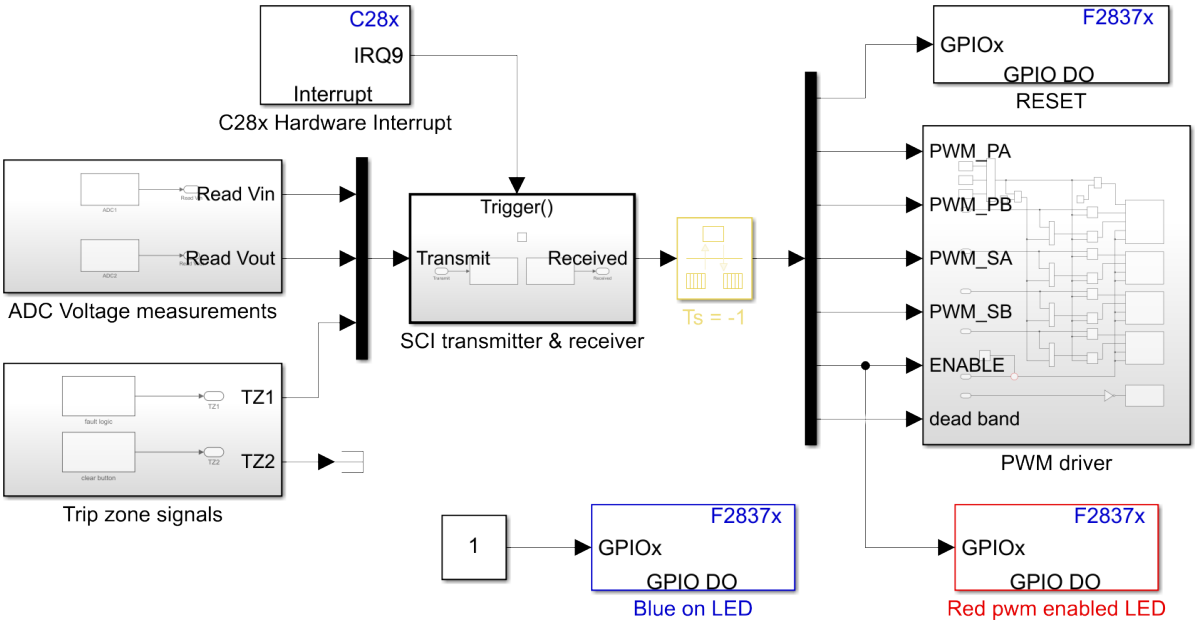


Figure G.1: Overview of the model for the control board

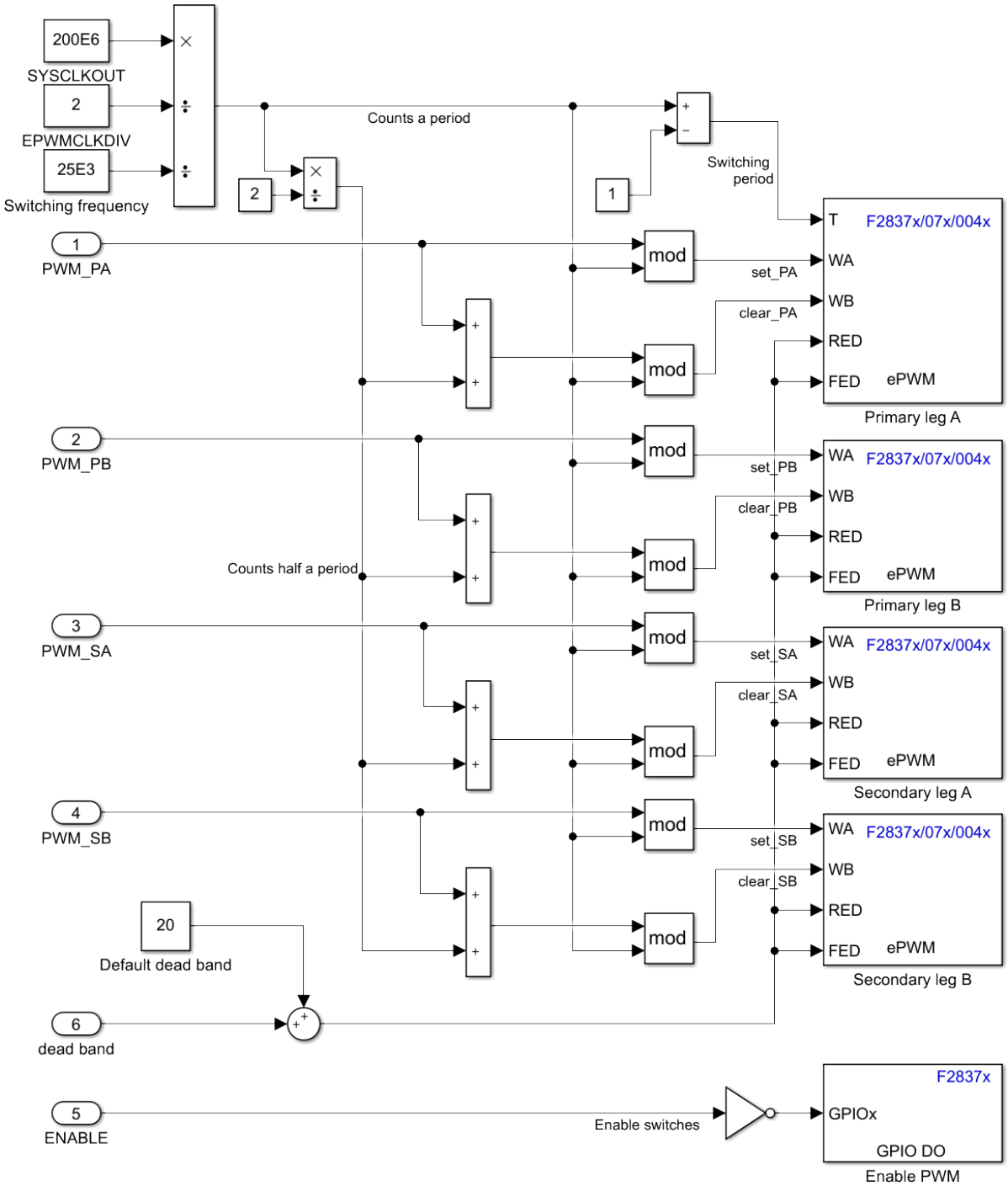


Figure G.2: The PWM driver of the control board

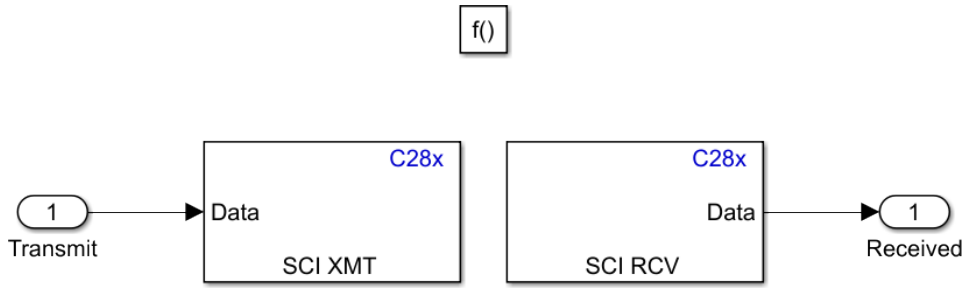


Figure G.3: The transmitter and receiver of the control board

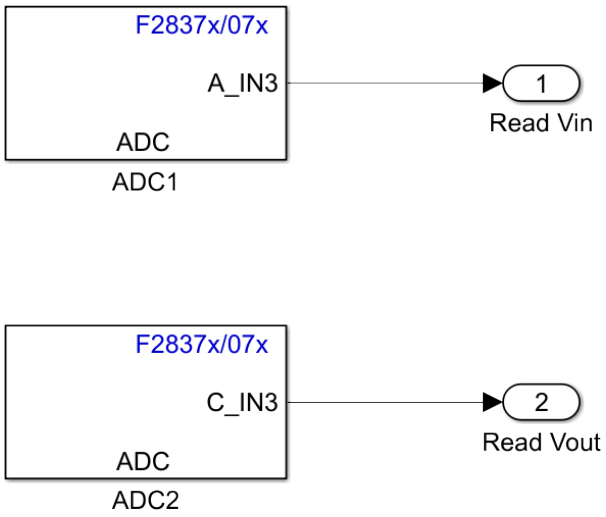


Figure G.4: The voltage measurements on the control board

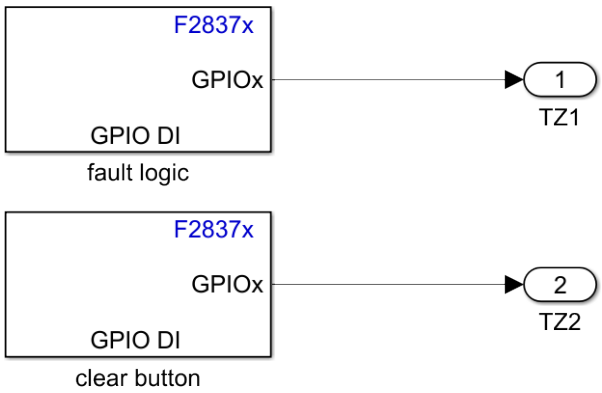


Figure G.5: The inputs for the trip zones of the control board

G.2. Computer

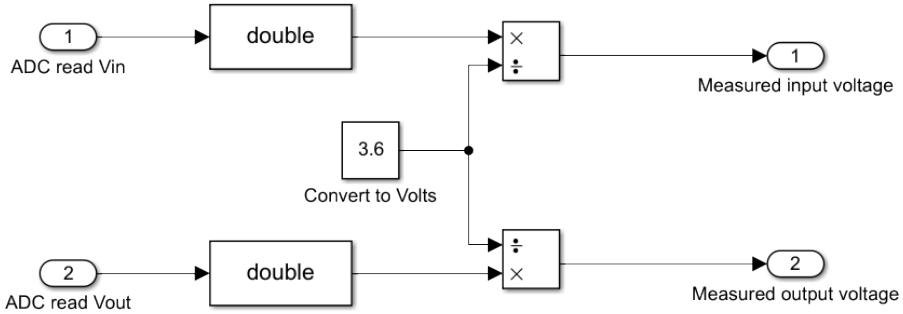


Figure G.6: The voltage measurements on the computer

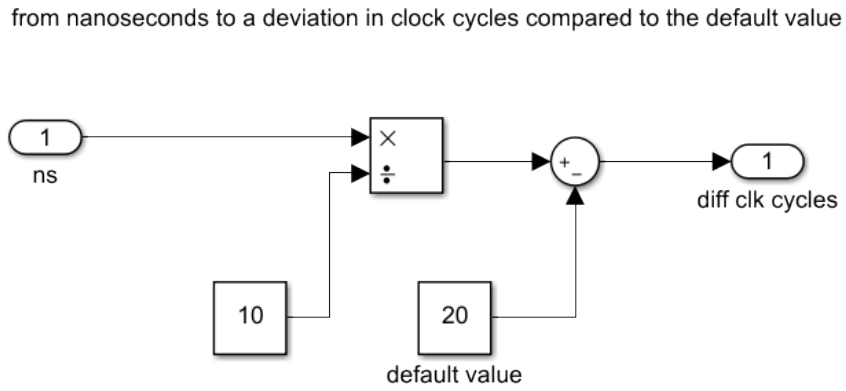


Figure G.7: The conversion stage for the default dead band

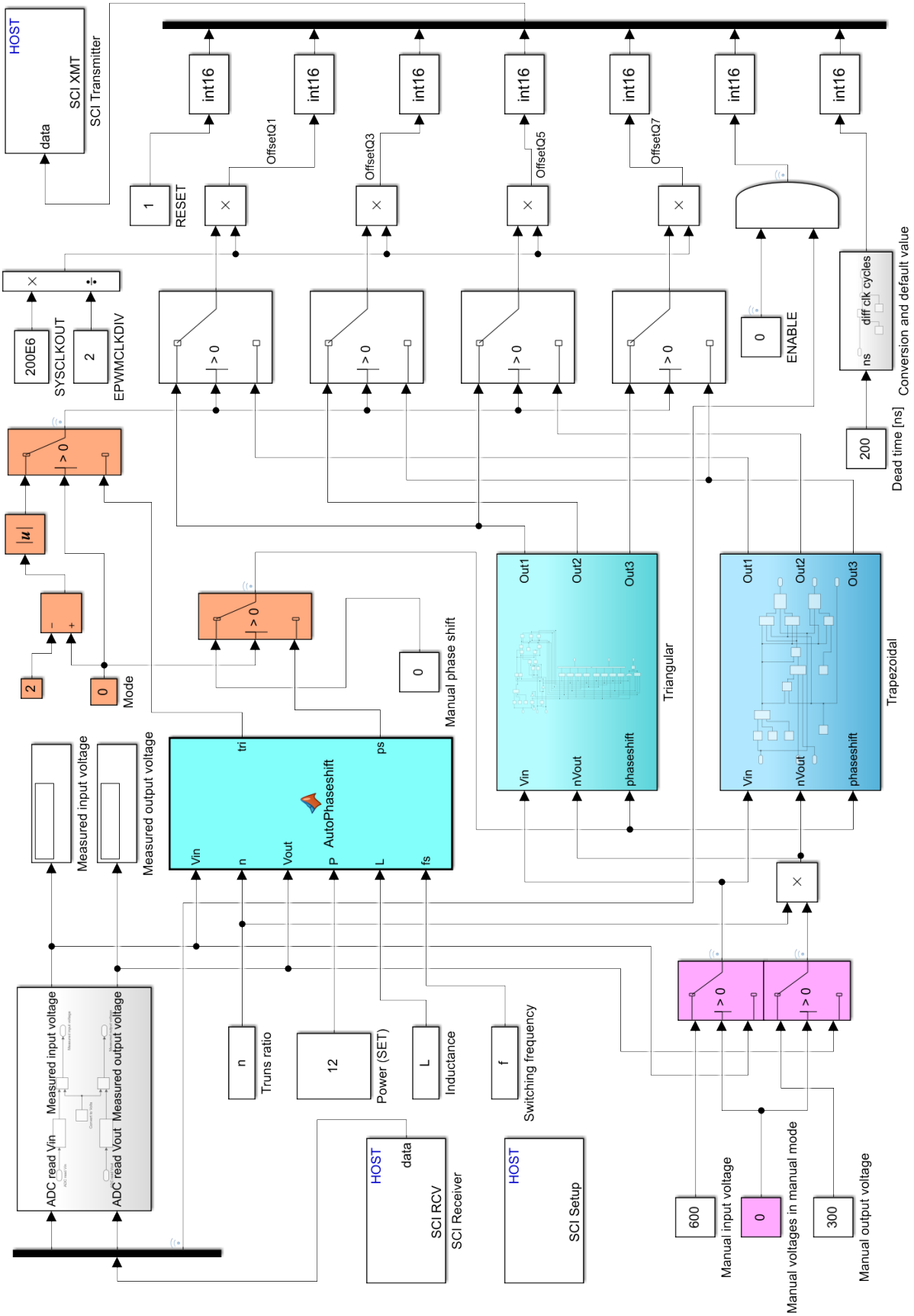


Figure G.8: Overview of the model on the computer

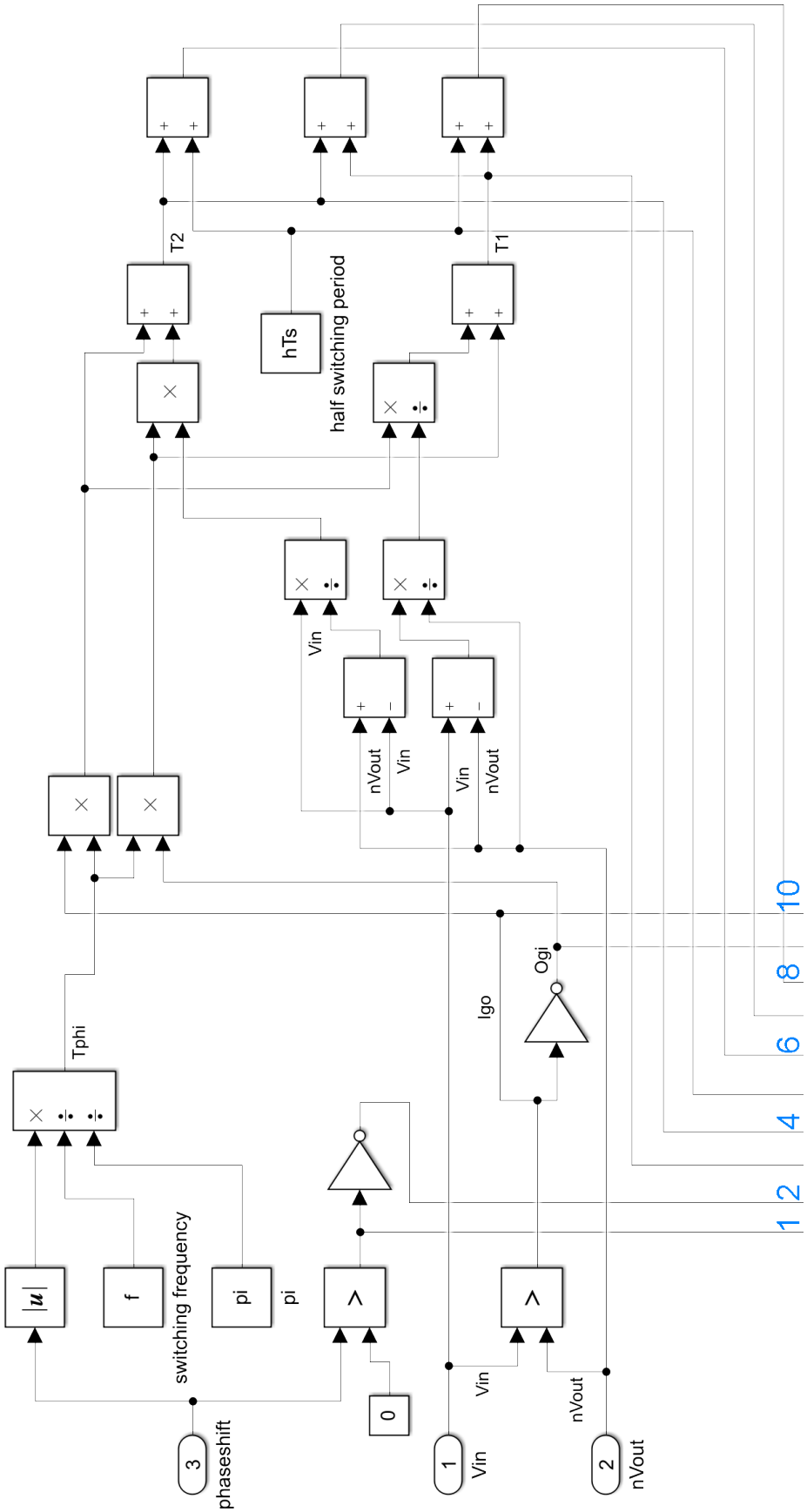


Figure G.9: Calculation triangular offset part 1

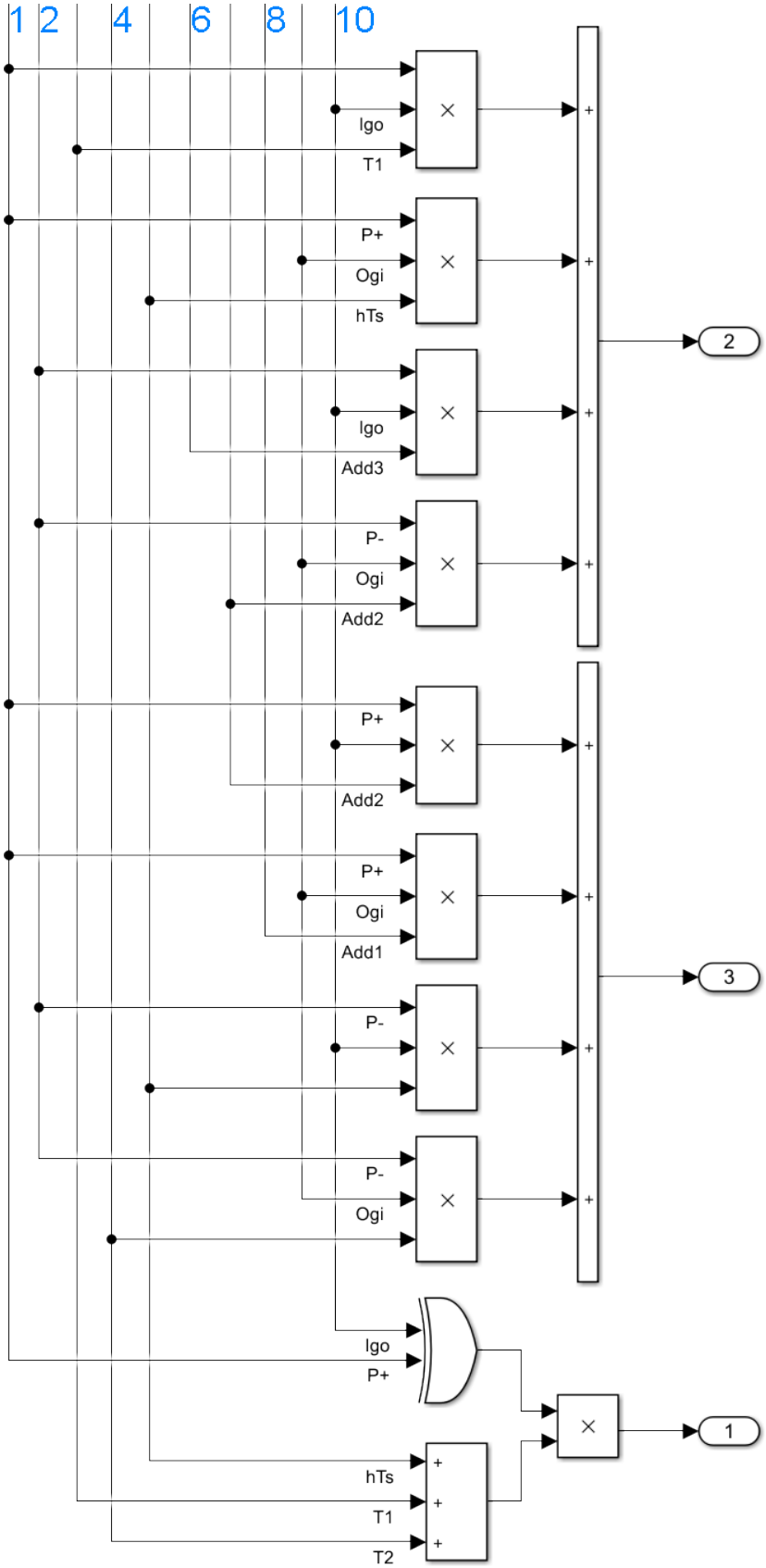


Figure G.10: Calculation triangular offset part 2

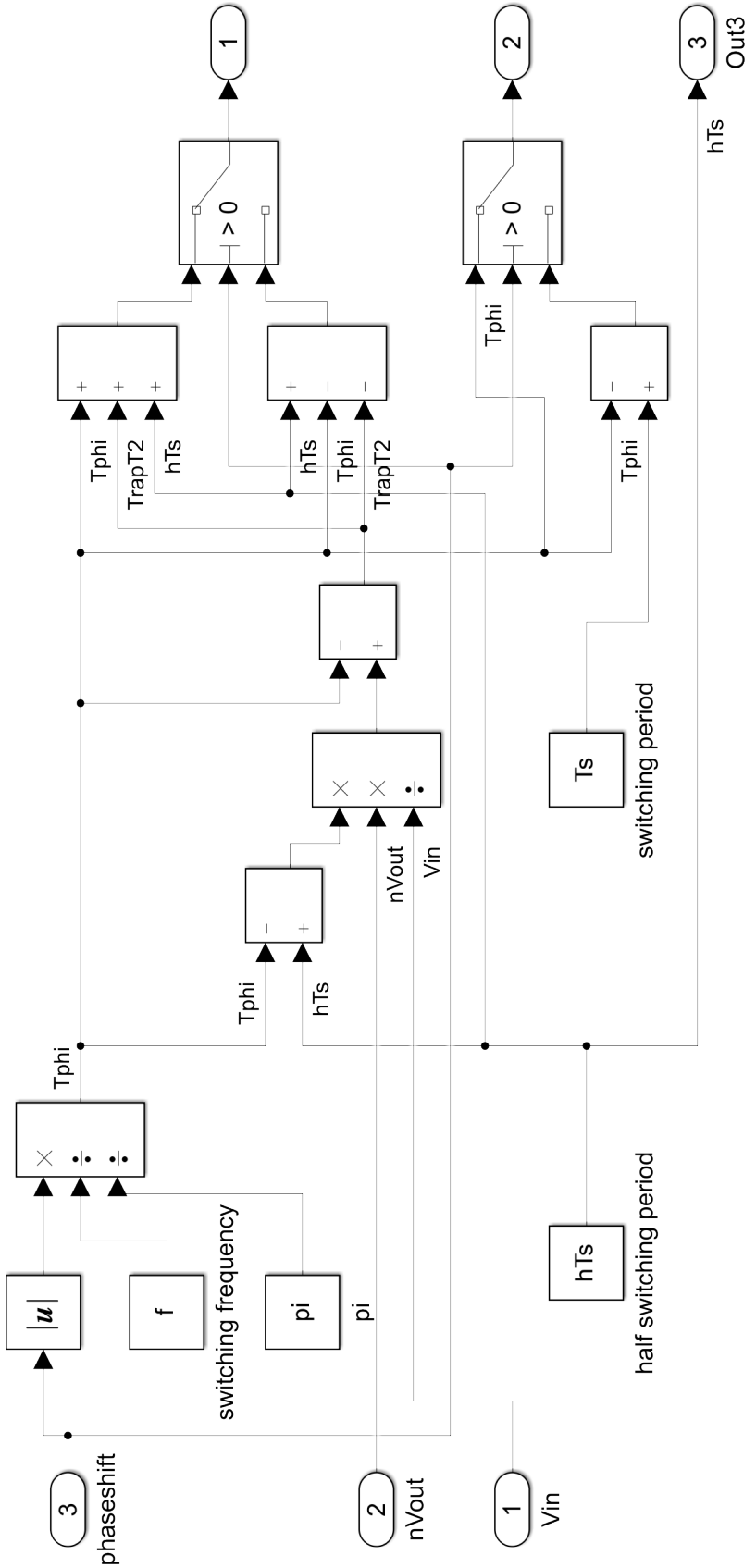


Figure G.11: Calculation trapezoidal offset

H

Testing procedure

After all components are placed on the PCB and the magnetic components are build as well, the converter can be tested. Make sure that during testing no accidental shorts are created and the isolation pads are placed between the MOSFETs and heat sink. In order to test the converter, the following steps can be followed:

1. Test the communication of the computer with Simulink and the Texas Instruments control board;
2. Measure all output signals (PWM, reset, enable) of controller both in triangular and trapezoidal and verify if everything works properly;
3. Measure the inductance of the coil;
4. Measure leakage inductance of the transformer;
5. Verify that both inductances add up to the designed value;
6. Verify the turns ratio by applying low voltage AC waveform on the primary side and a resistor on the secondary side;
7. Measure the 5 V and 3.3 V supply on the PCB;
8. Install the Texas Instruments control board on the PCB;
9. Verify the working of the fault signal;
10. Apply high voltages on the primary and secondary DC side and calibrate the voltage measurements;
11. Disconnect the high voltages;
12. Install all gate drivers;
13. Measure voltage across an installed MOSFET, to see if its responding to the signal of the gate driver;
14. Install all devices without the transformer; verify the converter works properly (but take into account the 1:1 turns ratio and lowered inductance, since there is no leakage inductance of the transformer in this case);
15. Check constantly the temperature of all devices and make sure they are below the maximum specified values;
16. Verify if the inductor current is as expected (no saturation) at both triangular and trapezoidal current modulation;
17. Add the transformer in between, measure again if the converter works;
18. Again, measure the temperatures (especially the transformer) and see if the current waveform is still okay;

19. Check the output voltage ripple;
20. Determine efficiency at different operating points;
21. Try to find out which components are responsible for the losses by looking at the temperature first, then measure to verify. Measure for example the voltage over and current through a MOSFET.

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