Voltage Calibration of BJT Based Temperature Sensor

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1 Introduction

A temperature sensor or temperature to digital converter (TDC) is used to quantify the temperature of its environment. Based on various temperature-dependent physical characteristics, different types of temperature sensors can be designed and implemented, from clinical thermometers to thermostats. It would seem that temperature sensors are only used to determine external temperatures. However, due to the temperature dependence of nearly all systems, temperature sensors are often used to measure internal temperatures, e.g.revealing temperature drift in wafer steppers. To fulfill this function in small devices, the area and power consumption are limited. This has led to the development of integrated temperature sensors based on CMOS technology.

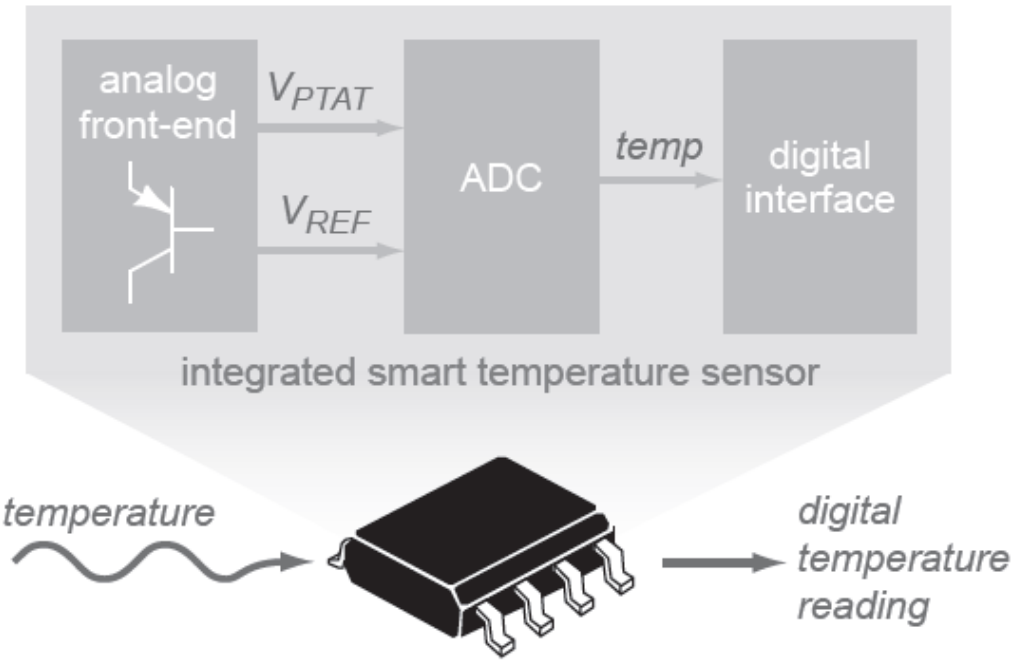

Figure 1: Block diagram of integrated temperature sensor [1]

As shown in Fig 1, the basic principle of a CMOS integrated temperature sensor is to generate a temperature dependent signal (V_{PTAT}) and a temperature independent signal as a reference (V_{REF}). Then the temperature dependent signal is compared with the reference signal and processed by an analog to digital converter (ADC). There are three main types of CMOS temperature sensors: bipolar junction transistors (BJT) based, MOSFET based and resistor based temperature sensors. Among these, BJT based temperature sensors are the most widely used. This is because it is easy to use BJTs to generate a voltage which is proportional to absolute temperature (PTAT) as well as a bandgap reference voltage. However, process spread causes a large error in BJT-based temperature sensors, therefore calibration is necessary. Currently, thermal calibration is the only method used in industry even though it is costly. More details of thermal calibration are introduced in section 1.3.1. In this thesis, a voltage calibration technique is proposed which should achieve the same accuracy as thermal calibration but should be much cheaper to apply [2]. In this project, voltage calibration will be added to a precision BJT-based temperature sensor manufactured by SmarTec BV known as the SMT-172.

1.1 Principle of BJT based temperature sensors

As introduced in the previous paragraph, integrated temperature sensors usually require the generation of a temperature dependent signal and a reference signal. Due to the characteristics of BJTs, these two signals can be easily generated.

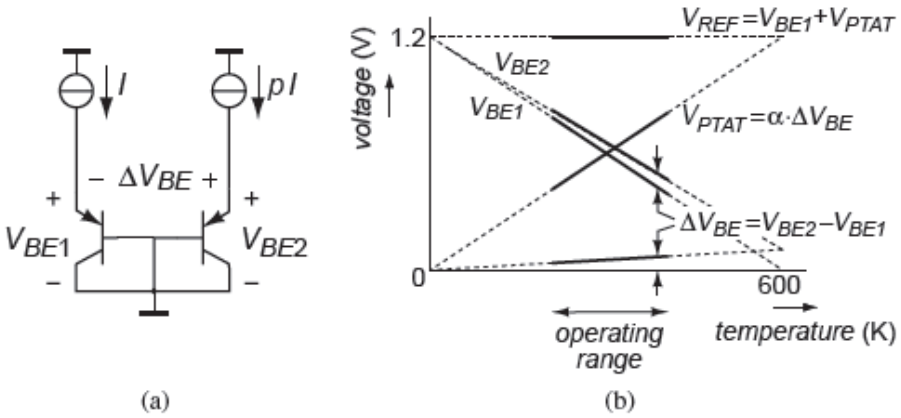

Figure 2: Basic principle of a BJT-based temperature sensor: (a) two diode-connected transistor biased by current source (b) generation of bandgap voltage [1]

Fig 2 illustrates the principle of a BJT-based temperature sensor. A transistor is biased by a current source, and the voltage between its base and emitter is given by [1]

$$V_{BE} = \frac{kT}{q} ln \frac{I_C}{I_S} \tag{1}$$

This is a complementary to absolute temperature voltage (CTAT) where k is the Boltzman Constant, T is the absolute temperature, q is the electron charge, I_C is the bias current and I_S is the saturation current, which is strongly process-dependent.

Obviously, V_{BE} is a non-linear function of temperature. Furthermore process spread may cause large errors in it due to variations in I_C and I_S. Therefore, V_{BE} is not suitable as a sensing signal. To eliminate the process error, the bases of two transistors are connected together. The difference between the two V_{BE}s is given by:

$$\Delta V_{BE} = V_{be2} - V_{be1} = \frac{kT}{q} ln \frac{I_{C2}}{I_{C1}} = \frac{kT}{q} ln(p) \tag{2}$$

As a result, the process-dependent I_S is canceled out. Ideally ΔV_{BE} is proportional to absolute temperature(PTAT).

Fig 3 shows the typical readout topology of a temperature sensor. Since V_{BE} has negative temperature coefficient and that of ΔV_{BE} is positive, with a well designed ratio α, the temperature dependency can be compensated.

$$V_{ref} = V_{BE1} + \alpha \Delta V_{BE} \tag{3}$$

This V_{ref} is essentially temperature independent [3]. To process these signals, usually an ADC is employed. This will output a ratio is given by [1]

$$\mu = \frac{\alpha \Delta V_{BE}}{V_{ref}} = \frac{\alpha \Delta V_{BE}}{\alpha \Delta V_{BE} + V_{BE}} \tag{4}$$

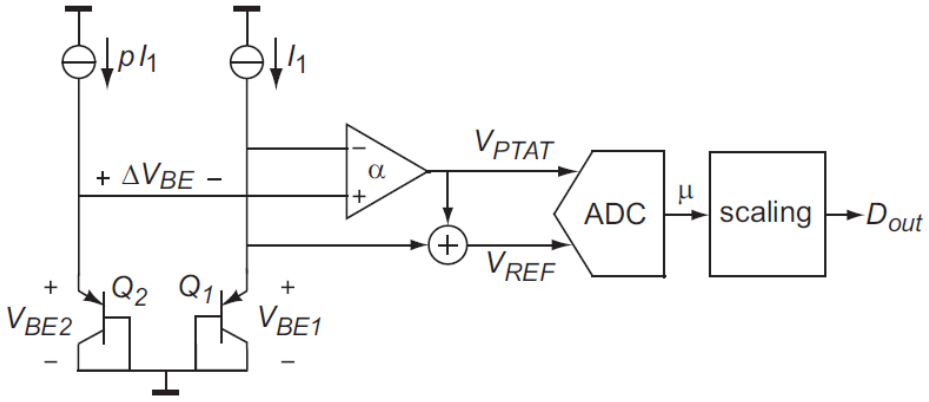

Figure 3: Basic principle of generic readout of temperature sensor

which is PTAT. The range of the digital output is from 0 to 1 corresponding to temperature range of about 600K. Converting the ratio into D_{out} in degrees Celsius, the final digital output is

$$D_{out} = A \times \mu + B \tag{5}$$

where A is about 600K and B is about -273K.

1.2 Inaccuracy of BJT based temperature sensor

1.2.1 A PTAT Error in V_{BE}

Due to process spread, V_{BE} deviates from the designed nominal value. Two main factors that influence V_{BE} are the spread of the saturation current and the spread of the current gain on V_{BE}. If the transistor has a deviation ΔI_S on the saturation current, the resulting V_{BE} is given by [1]

$$\begin{aligned} V_{BE} &= \frac{kT}{q} ln(\frac{I_C}{I_S + \Delta I_S}) \\ &= \frac{kT}{q} ln(\frac{I_C}{I_S}) - \frac{kT}{q} ln(1 + \frac{\Delta I_S}{I_S}) \\ &\approx V_{BE}|_{\Delta I_S = 0} - \frac{kT}{q}\frac{\Delta I_S}{I_S} (\Delta I_S << I_S) \end{aligned} \tag{6}$$

The variation can be estimated based on the saturation current.

$$I_S = \frac{kTAn_i^2\mu_p}{W_B N_d} \tag{7}$$

where A is the area of emitter, n_i is the intrinsic carrier concentration, μ_p is the mobility of majority carrier, W_B is the width of base and N_d is the base doping.

The variation of doping N_d can be obtained according to [4], which is up to $\pm 50\%$. This variation results in ± 13mV error in V_{BE}, which is about $\pm 6.5^{\circ}C$ in temperature.

Another source of error is caused by variations in the base width W_B and area A, which are determined by diffusion and lithography which have a tolerance of about $\pm 20\%$ [5]. If an area of $20\mu m \times 20\mu m$ spreads by $\pm 1\%$, this will correspond to ± 0.25mV voltage error. Therefore, the maximum voltage error caused by spread of area could be 1mV.

The spread of common-base current-gain also causes error in V_{BE}. If the common-base current-gain suffers variation by an amount $\Delta\alpha_F$, the practical base-emitter voltage is

$$\begin{aligned} V_{BE} &= \frac{kT}{q} ln(\frac{(\alpha_F + \Delta\alpha_F)I_E}{I_S}) \\ &= \frac{kT}{q} ln(\frac{\alpha_F I_E}{I_S}) + \frac{kT}{q} ln(1 + \frac{\Delta\alpha_F}{\alpha_F}) \\ &\approx V_{BE}|_{\Delta\alpha_F=0} + \frac{kT}{q}\frac{\Delta\alpha_F}{\alpha_F} (\Delta\alpha_F << \alpha_F) \end{aligned} \tag{8}$$

Similar as the spread of saturation current, the $\frac{\alpha_F}{\alpha_F}$ causes a PTAT spread of V_{BE} [1].

Overall, considering these two factors, the total error in V_{BE} is quite large. Fortunately, most of these errors can be removed after PTAT trimming. This can be done by employing an array of BJTs and a multiplexer to effectively change the area of the transistor producing V_{BE}.

1.2.2 Mismatch in ΔV_{BE}

Compared with V_{BE}, ΔV_{BE} only suffers from components mismatch. If the ratio p in equation 2 deviates by Δp resulting from the mismatch between transistors or current sources, the final ΔV_{BE} becomes

$$\begin{aligned} \Delta V_{BE} &= \frac{kT}{q} ln(p + \Delta p) \\ &\approx \frac{kT}{q} lnp(1 + \frac{\Delta p}{plnp}) \\ &\approx \Delta V_{BE}|_{\Delta p=0} + \frac{kT}{q}\frac{\Delta p}{p} (\Delta p << p) \end{aligned} \tag{9}$$

If $\frac{\Delta p}{p} = 0.1\%$, the error in ΔV_{BE} is about $26\mu V$ at T=300K, which is much smaller than the typical value of error in V_{BE}. Moreover, error cancellation technique such as dynamic elements matching (DEM) can help remove the errors due to mismatch.

1.2.3 Non-ideality Factor in BJT

Beside the PTAT errors in V_{BE} and the mismatch in ΔV_{BE}, the spread in BJTs non-ideality factor may also cause errors. Using it, V_{BE} and ΔV_{BE} can be more accurately expressed as

$$V_{be} = \eta \frac{kT}{q} ln \frac{I_C}{I_S} \tag{10}$$

and

$$\Delta V_{BE} = \eta_F \frac{kT}{q} ln \frac{I_{C1}}{I_{C2}} = \eta_F \frac{kT}{q} ln(p) \tag{11}$$

where η_F is the non-ideality factor [6]. This factor is process and temperature dependent. Thus, the value of V_{BE} and ΔV_{BE} differ from the designed value. However, according to equation 4, the digital output is the ratio of ΔV_{BE} and V_{ref}, so η_F can be eliminated. The final output is not influenced by the non-ideality factor.

Therefore, V_{BE} is the major source cause error in BJT based temperature sensor, and so it must be trimmed. Thus, in turn, requires a calibration step.

1.3 Calibration of BJT-based temperature sensor

To reduce error in temperature sensor, trimming is necessary. Before the sensor is trimmed, the temperature error need to be known. At present, the thermal calibration is the only method used to calibrate temperature sensors. However, it is usually costly. Due to the unique feature of BJT based temperature sensors, an alternative method called voltage calibration is proposed. In this section, both methods are briefly described and some comparisons are made.

1.3.1 Thermal Calibration

The principle of thermal calibration is to measure the output of the temperature sensor at one or several exact temperature points. Since the real temperature is known by other accurate reference sensors, the temperature errors can be calculated. Based on these errors, the sensor can trimmed such that its output is equal to the known temperature. For a BJT based temperature sensor, one-point trim is efficient due to its PTAT temperature error (further discussed in Chapter 5) and the trimming is normally at room temperature.

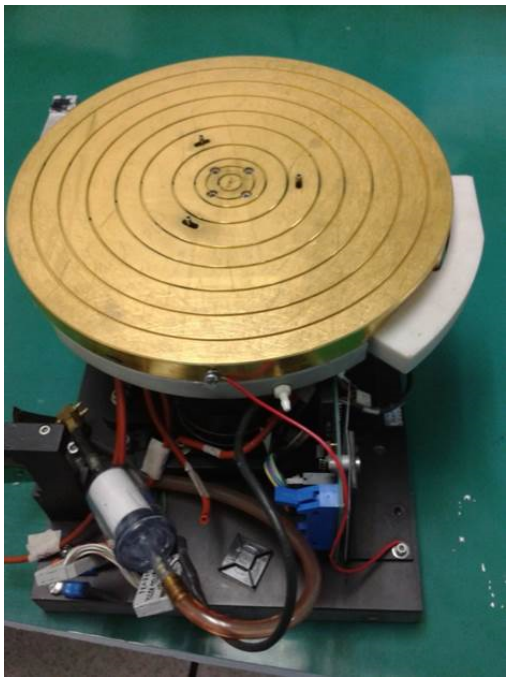

Figure 4: Chuck for thermal calibration

Fig 4 shows the chuck for thermal calibration. The wafer is put on the top of chuck. Due to the good thermal conductivity of silicon, the wafer temperature is the same as that of the chuck. The sensor output is compared with T_{ref}. Trimming is performed so that the sensor output equals to T_{ref} Finally, the sensor is trimmed to eliminate the temperature error between digital output and reference temperature [7].

However, considering the stabilization time and cost for the equipment like Pt_100 temperature sensors, thermal calibration is a costly method. Thus, another convenient method called voltage calibration is proposed.

1.3.2 Voltage Calibration

As introduced in section 1.2, ΔV_{BE} can be designed accurately by applying DEM, thus temperature can be calculated accurately if ΔV_{BE} is known. The basic principle of voltage calibration is to determine the value of ΔV_{BE} based on the digital output [2]. As shown in Fig 5, V_{BE} on chip is

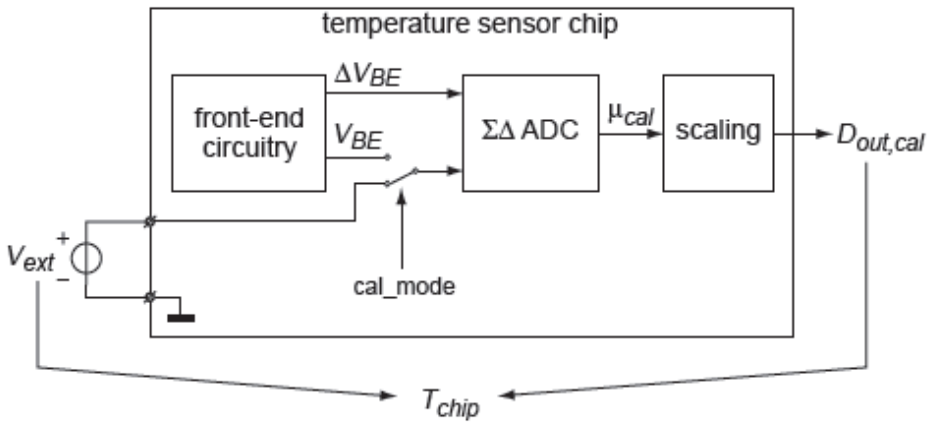

Figure 5: Principle of voltage calibration [2]

replaced with an accurate external voltage, V_{ext}. Similarly, the digital output is given by:

$$\mu_{cal} = \frac{\alpha \Delta V_{BE}}{\alpha \Delta V_{BE} + V_{ext}} \tag{12}$$

If the ratio α and V_{ext} are known, ΔV_{BE} is then calculated as

$$\Delta V_{BE} = \frac{\mu_{cal}}{\alpha(1 - \mu_{cal})} V_{ext} \tag{13}$$

In this indirect way, ΔV_{BE} has beem measured. And then, chip temperature T_{chip} can be calculated and used as reference temperature, T_{ref}. Afterwards, the same trim method as thermal calibration can be taken to ensure the output equals T_{chip}.

1.3.3 Error of voltage calibration

However, accuracy of voltage calibration suffers is limited by two factors: errors in V_{ext} and non-ideality in ΔV_{BE}. The errors in V_{ext} usually result from noise and variation. If the noise of V_{ext} is larger than that of V_{BE}, the resolution during voltage calibration becomes worse. Besides, the variation of V_{ext} results in error in temperature calculated from ΔV_{BE}. For instance, 2mV error in V_{ext} may induce $1°C$ error in T_{ref}.

Finally, according to equation 11, the calculated temperature suffers from the non-ideality factor. As a result, the equation 2 is used, the calculated temperature may be far from the real temperature. This kind of error is further discussed in Chapter 5.

1.3.4 Comparisons

Obviously, the voltage calibration can only be applied for BJT-based temperature sensors. Compared to general thermal calibration, voltage calibration has several advantages.

Firstly, voltage calibration does not require precise temperature environment compared to thermal calibration. Moreover, the procedure of voltage calibration is simpler.

Secondly, thermal calibration is done at wafer level, which means that after packaging, mechanical stress will be introduced and extra package calibration is needed. However, voltage calibration can be carried out after packaging and the trim is done in digital domain that is cost efficient.

Therefore, if the result of voltage calibration is similar to that of thermal calibration, voltage calibration can be adopted as a practical calibration technique in industry in the future.

1.4 Outline of the thesis

The whole thesis is divided into 6 chapters. Chapter 2 provides a brief introduction to the working principle of SMT172. Chapter 3 describes the implementation of on-chip reference voltage which is used for voltage calibration. Different types of reference voltage are compared and the most proper one is chosen. In Chapter 4 and 5, the measurement set up and final results are discussed to illustrate the difference between thermal and voltage calibrations. Finally, Chapter 6 gives the conclusion whether voltage calibration is comparable to thermal calibration based on the results.

2 SMT 172

This section describes a precision BJT-based temperature sensor, SMT172 implemented in $0.7\mu m$ CMOS technology. In this sensor, bipolar transistors are applied to generate the temperature dependent signals in the current domain. Compared to other BJT based temperature sensors, the SMT172 does not employ a traditional analog to digital converter(ADC) such as a $\Sigma\Delta$ADC but employs a continuous-time duty-cycle modulator whose duty-cycle is proportional to temperature. This special architecture results in high resolution and energy efficiency. After one-point trim, the sensors' inaccuracy is 0.15°C(3σ) from -45°C to 130°C [8].

2.1 Principle of SMT172

The operating principle of the SMT172 is shown in Fig 6. Under the control of a Schmitt trigger(ST), a capacitor C is periodically charged by a current I_1 up to a threshold voltage V_2 and then discharged by a current I_2 down to a threshold voltage V_1 shown in Fig 6(a) [8]. As can be deduced from the timing diagram shown in Fig 6(b), the time intervals of T_1 and T_2 are determined by

$$T_1 = \frac{(V_2 - V_1)C}{I_1}, T_2 = \frac{(V_2 - V_1)C}{I_2} \tag{14}$$

the duty-cycle D of the resulting output signal equals:

$$\begin{aligned} D_{out} &= \frac{T_2}{T_1 + T_2} \\ &= \frac{\frac{(V_2-V_1)C}{I_2}}{\frac{(V_2-V_1)C}{I_1} + \frac{(V_2-V_1)C}{I_2}} \\ &= \frac{I_1}{I_1 + I_2} \end{aligned} \tag{15}$$

where the duty cycle D is independent of the exact value of the threshold voltage V_1 and V_2 of the Schmitt trigger and of the capacitance C.

I_1 has been designed to be with positive temperature coefficient while I_2 with negative temperature coefficient. And the sum $I_{out} = I_1 + I_2$ has been designed to be temperature independent as indicated in Fig 6(c), as a result the duty-cycle is linearly proportional to temperature.

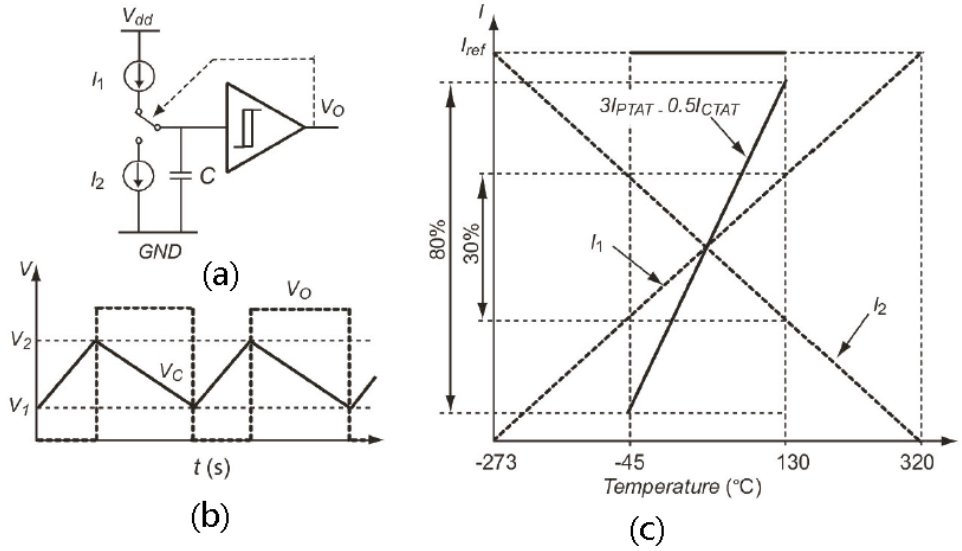

Figure 6: Operating Principle of SMT172

The simplified block diagram of the actual sensor is shown in Fig 7. Q1 and Q2 are used to generate PTAT voltage. The ratio of biasing current is 3:1 while the ratio of emitter area is 1:3 as a result the ratio of the biasing current density for Q_1 and Q_2(p in equation 2) is 9. Therefore, the PTAT voltage equals:

$$\Delta V_{BE} = \frac{kT}{q} ln(9) \tag{16}$$

This voltage is then forced across resistor R_{PTAT} by OP_1 and converted into $I_{PTAT}(I_{PATA} = \frac{\Delta V_{BE}}{R_{PTAT}})$. Similarly, V_{BE} from Q_3 has been applied to generate I_{CTAT} by OP_2 and $R_{be}(I_{CTAT} = \frac{V_{BE}}{R_{BE}})$. Then, the currents I_{PTAT} and I_{CTAT} are combined to generate the currents I_1 and I_2 as

$$I_1 = 3I_{PTAT} - 0.5I_{CTAT}; I_2 = I_{CTAT} - I_{PTAT} \tag{17}$$

The sum $I_{out} = I_1 + I_2 = 2I_{PTAT} + 0.5I_{CTAT}$ has been designed to have a slight positive temperature coefficient, in the way the curvature of V_{BE} can be effectively compensated [8].

By proper design of the circuit parameters and the nominal value of V_{BE}, the target equation for duty-cycle versus temperature can be realized. Over the whole temperature range from -45°C to 130°C, the duty-cycle changes from about 10% to 90%.

Temperature error occurs due to the finite gain of OP_1 and OP_2. To ensure that the error is smaller than 50mK, the gains of OP_1 and OP_2 must reach 90dB and 70dB respectively. Besides, OP_1 and OP_2 need to be able to handle input voltage (V_{BE}), which down to 0.3V. Thus, OP_1 and OP_2 have been designed as folded cascode amplifier with PMOS inputs pairs.

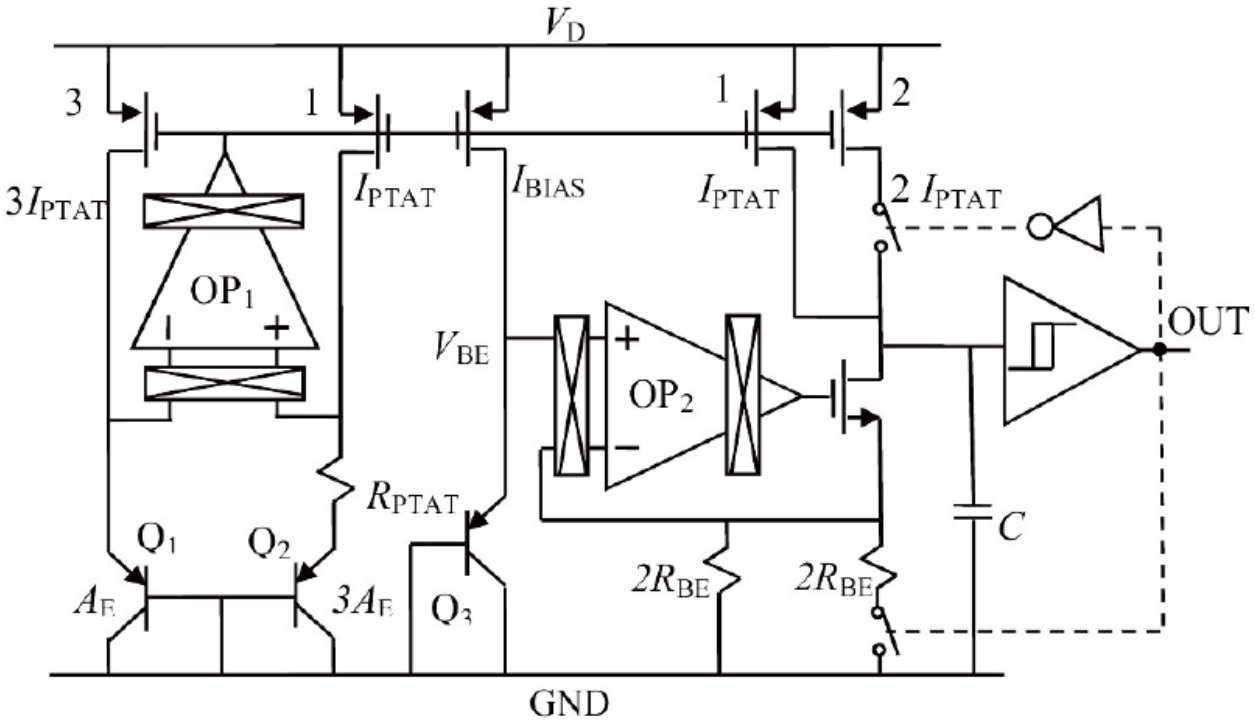

Figure 7: Simplified Schematic of SMT172

Fig 8 shows the structure of Schmitt trigger. It consists of 2 inverter and a positive feedback loop. The threshold voltage of ST is determined by M2 and M3 respectively. The total swing range $(V_2 - V_1)$ is approximately $V_{DD} - 2$V. The large swing range ensures that the input referred noise has negligible impact to the duty-cycle. Together with the large capacitor C(150pF), the output frequency has been designed to be low enough (7¡kHZ) so that the error caused by the switch time of ST can be neglected.

The duty-cycle can be written as

$$D = \frac{t_2}{t_1 + t_2} = \frac{I_1}{I_1 + I_2} = \frac{3I_{PTAT} - 0.5I_{CTAT}}{2I_{PTAT} + 0.5I_{CTAT}} = \frac{3\frac{\Delta V_{BE}}{R_{PTAT}} - 0.5\frac{V_{BE}}{R_{be}}}{2\frac{\Delta V_{BE}}{R_{PTAT}} + 0.5\frac{V_{BE}}{R_{be}}} \tag{18}$$

This equation indicates that the duty cycle is independent of the absolute value of the threshold voltage of ST.

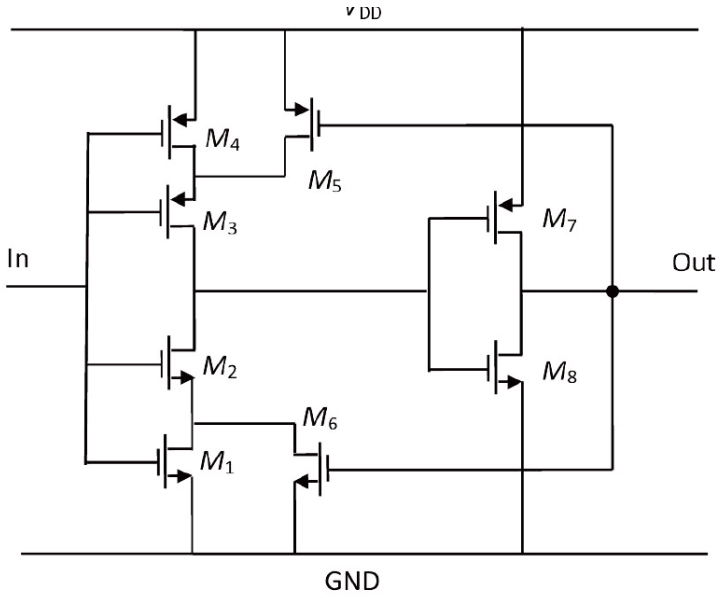

Figure 8: Structure of Schmitt trigger

2.2 FPGA

The SMT172 has a rail-to-rail square wave output. The frequency varies from 500Hz to 7kHz depend on the temperature and the supply voltage. But the duty-cycle contains the actual temperature information. A FPGA board can be used to digitize the time intervals and calculate the duty-cycle. Fig 9 gives the principle of the digitization. The square wave is sampled by a high frequency clock signal. The counted number N_L and N_H correspond to the time intervals of t_L(low state) and t_H(high state) respectively. Afterwards, the duty-cycle is calculated by

$$D = \frac{N_H}{N_H + N_L} \tag{19}$$

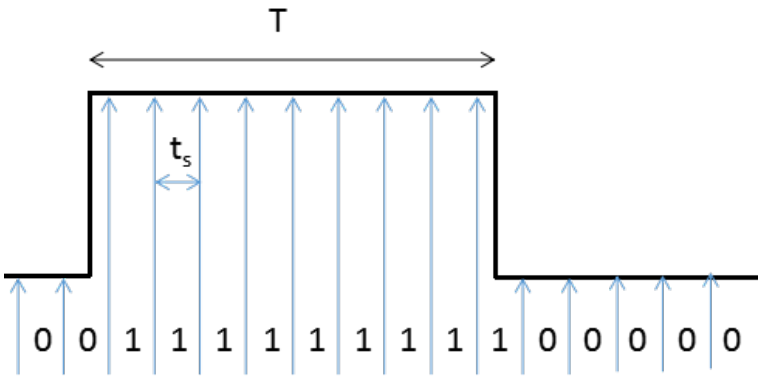

Figure 9: The principle of digitizing square wave

Thus the quantization noise occurs at both the beginning and the end of time interval t_L and

t_H. The uncertainty at each edge is given as [9]

$$\sigma^2 = \frac{1}{t_s}\int_0^{t_s}(t - \frac{1}{2}t_s)^2 dt = \frac{t_s^2}{12} \tag{20}$$

where σ is the standard deviation of the uncertainty. Since the quantization error at the up-going edge and the down-going edge are not correlated, the total variation in time domain can be taken as $2\sigma^2$. The relative standard deviation is

$$\varepsilon = \frac{\sqrt{2}\sigma}{T} = \frac{1}{\sqrt{6}}\frac{t_s}{T} \tag{21}$$

In order to minimize the quantization noise, the highest clock frequency of 100MHz has been used to digitize the time intervals of the sensor output [8]. As a result, the sensors' thermal noise will be dominate, and this determines the resolution.

3 Implementation of voltage calibration

To realize the function of voltage calibration, an accurate reference voltage is needed. In previous works [2] [10], an external reference voltage has been applied to replace V_{BE}. In this thesis we presented an alternative way to generate the reference voltage on-chip for voltage calibration. The advantages of such option are:

A No external voltage reference is needed

B One connection pin for V_{ref} can be saved

The on-chip voltage reference should meet the requirements:

A High accuracy

B The value should be compatible with that of V_{BE} at calibration temperature

C Low power, extra power consumption increase self-heating

D Small chip area

The main reason not to use a conventional on-chip bandgap reference [11] is that it also requires calibration to achieve high accuracy, which leads the design into a dead loop.

Therefore, a passive reference voltage from voltage divider is proposed.

3.1 Voltage divider

The idea of voltage divider is to divide the supply voltage by passive components with an accurate factor. The main advantage is that accuracy of the passive reference voltage only depends on how accurately the supply voltage can be measured and how accurate the divider factor can be realized. With a general multi-meter the supply voltage can be measured accurately. The main limit of the accuracy of the reference voltage is then the accuracy of the voltage divider. Component mismatch can cause error in voltage divider. By applying dynamic elements matching (DEM) [12] and averaging the mismatch induced error in voltage divider can be eliminated significantly.

Fig 10 shows the block diagram of voltage calibration. The left part is the voltage divider, which generates the reference voltage for calibration. PD pin of the chip determines which mode the chip is in. In normal mode, the SMT172 is connected with V_{BE} while in calibration mode, the SMT172 is connected with V_{ref}.

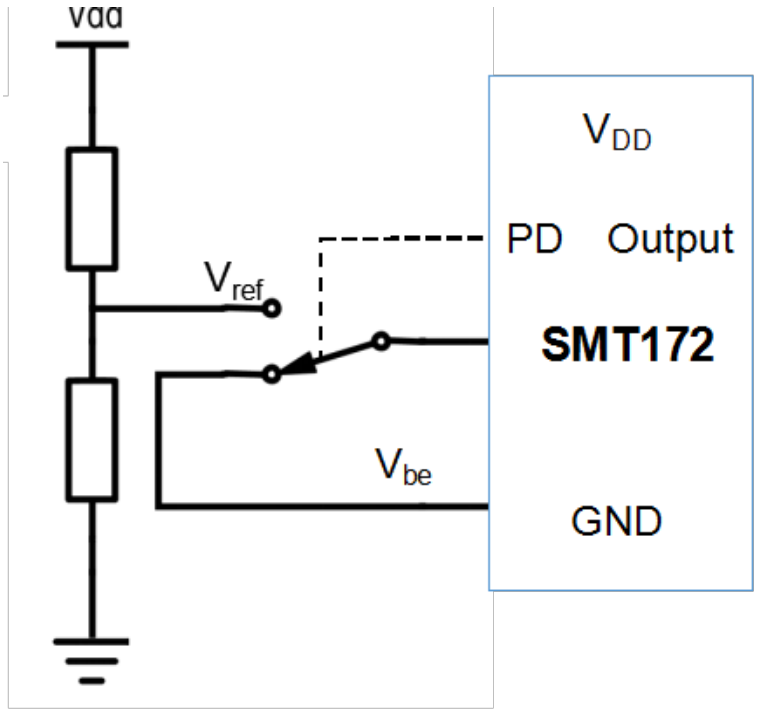

Figure 10: Block diagram of voltage calibration

There are two types of passive voltage dividers, the resistive divider and the capacitive divider. The resistive divider has been chosen for the design. The main reason not to use a capacitive divider is because a capacitive divider cannot provide a continuous-time reference voltage, which is required for temperature sensor SMT172 for voltage calibration. In the following section, the resistive divider will be discussed.

3.1.1 Resistive voltage divider

Two structures of resistive voltage divider are shown in Fig 11. Fig 11(a) shows a serial resistive voltage divider while Fig 11 is parallel [13]. DEM techniques can be applied for both resistive voltage dividers [12]. The following case takes ratio of 1/3 as an example.

For instance, the voltage divider ratio $\frac{1}{3}$, for the serial resistive voltage divider, the three identical resistors($R_1 = R_2 = R_3$) are connected in serial. The current through the resistors are $I = \frac{V_{DD}}{3R}$, the reference voltage is

$$V_{ref} = R \times I = \frac{1}{3} V_{DD} \tag{22}$$

For the parallel resistive voltage divider, the three identical resistors are connected as: one resistor is connected in serial with other two parallel connected resistors. The equivalent resistance of two parallel resistors is $R_{eq} = \frac{1}{2}$, so the reference voltage is

$$V_{ref} = \frac{V_{DD}}{R + \frac{1}{2}R} \times \frac{1}{2} R = \frac{1}{3} V_{DD} \tag{23}$$

So the divider ratio of 1/3 can be achieved for both structures. To eliminate the error caused by the mismatch between resistors, DEM can be applied. Fig 12 shows the structures of both resistive voltage dividers with DEM applied. According to these equations, both resistive voltage dividers can achieve the target ratio.

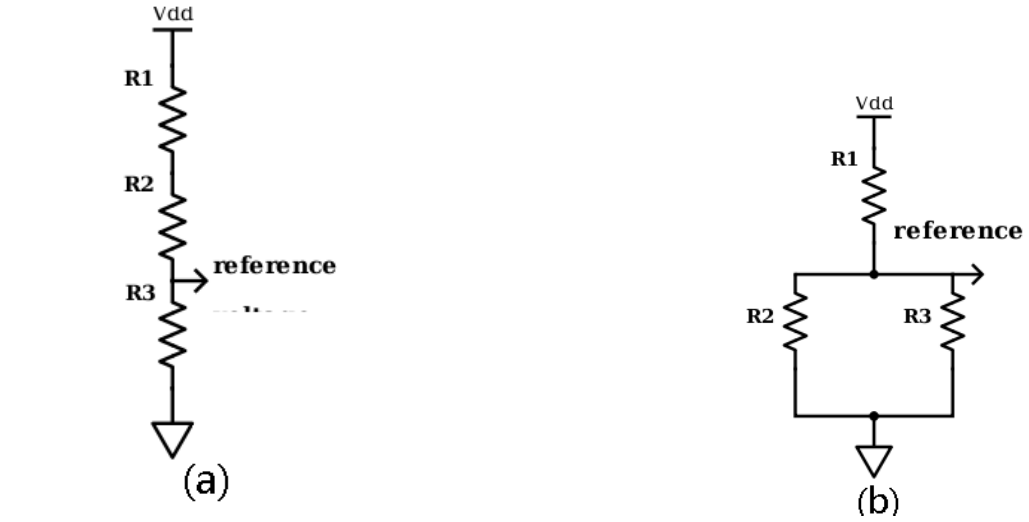

Figure 11: Structure of resistive voltage divider

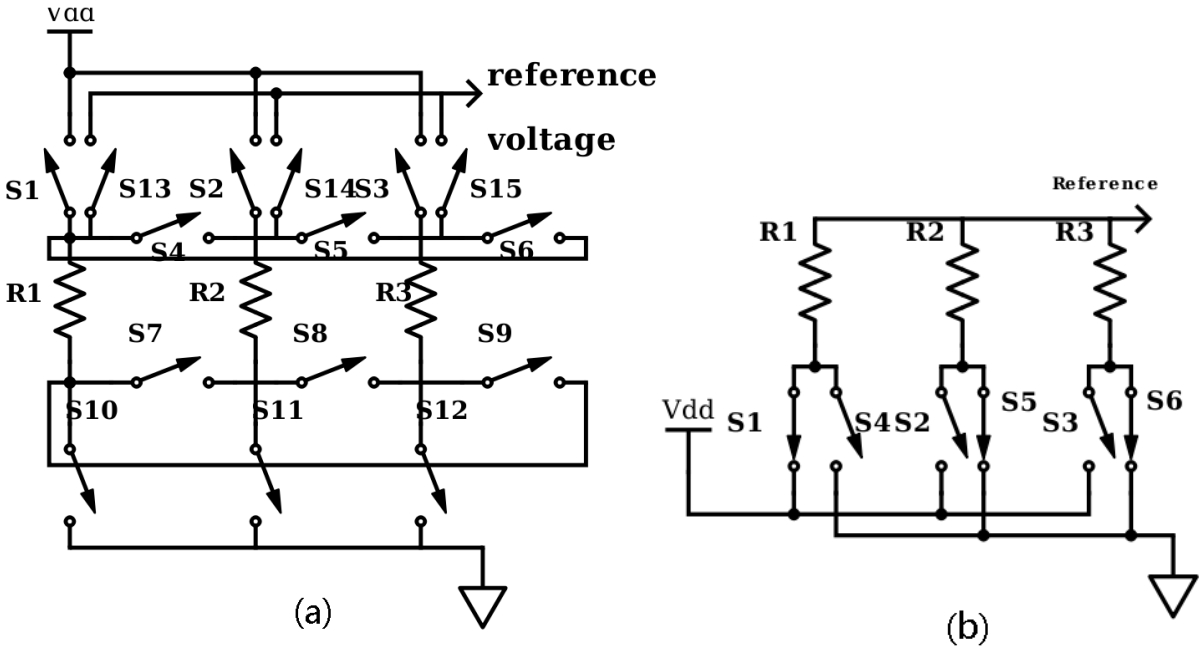

Figure 12: Structure of resistive voltage divider with DEM applied

Due to mismatch, there are:

$$\begin{aligned} R &= (R_1 + R_2 + R_3)/3 \\ R_1 &= R(1+\sigma_1) \\ R_2 &= R(1+\sigma_2) \\ R_3 &= R(1+\sigma_3) \\ \sigma_1 + \sigma_2 + \sigma_3 &= 0 \end{aligned} \tag{24}$$

where σ_1,σ_2 and σ_3 represent the relative mismatch of R_1,R_2 and R_3 respectively.

For serial resistive divider, DEM is applied as: for the first step, the connection is like Fig 12(a), R_1 is connected to GND. Next step, the positions is shifted. R_2 is connected to GND, the other two resistors are in serial connected on top of R_2, and so on. After three steps, all three resistors have been at the position connected to GND once. Taking average of the output voltage of these three steps(V_1, V_2 and V_3) results in:

$$\begin{aligned} V_{ave} &= \frac{V_1 + V_2 + V_3}{3} \\ &= \frac{V_{DD}}{3}(\frac{1+\sigma_1}{3} + \frac{1+\sigma_2}{3} + \frac{1+\sigma_3}{3}) \\ &= \frac{V_{DD}}{3}(\frac{3+\sigma_1+\sigma_2+\sigma_3}{3}) \\ &= \frac{V_{DD}}{3} \end{aligned} \tag{25}$$

For parallel resistive divider, DEM is applied as: for the first step, the connection is like Fig 12(b). R_1 is connected to V_{DD}. Next step, the positions is changed. R_2 is connected to V_{DD}, the other two resistors are in parallel connected to GND, and so on. After three steps, all three resistors have been at the position connected to V_{DD} once. Taking average of the three steps(V_1, V_2 and V_3) results in:

$$\begin{aligned} V_{ave} &= \frac{V_1 + V_2 + V_3}{3} \\ &= \frac{V_{DD}}{3}(\frac{(1+\sigma_2)(1+\sigma_3)}{(1+\sigma_1)(1+\sigma_2)+(1+\sigma_1)(1+\sigma_3)+(1+\sigma_2)(1+\sigma_3)} \\ &+ \frac{(1+\sigma_1)(1+\sigma_3)}{(1+\sigma_1)(1+\sigma_2)+(1+\sigma_1)(1+\sigma_3)+(1+\sigma_2)(1+\sigma_3)} \\ &+ \frac{(1+\sigma_1)(1+\sigma_2)}{(1+\sigma_1)(1+\sigma_2)+(1+\sigma_1)(1+\sigma_3)+(1+\sigma_2)(1+\sigma_3)}) \\ &= \frac{V_{DD}}{3}\frac{(1+\sigma_1)(1+\sigma_2)+(1+\sigma_1)(1+\sigma_3)+(1+\sigma_2)(1+\sigma_3)}{(1+\sigma_1)(1+\sigma_2)+(1+\sigma_1)(1+\sigma_3)+(1+\sigma_2)(1+\sigma_3)} \\ &= \frac{V_{DD}}{3} \end{aligned} \tag{26}$$

Above analysis shows that by applying DEM, the mismatch induced error can be removed completely for both serial and parallel and resistive divider.

In general, the number of DEM steps ia arranged to 2^n(n is an integer number), which is easy to be implemented.

Fig 12 shows how DEM can be implemented to serial and parallel divider. Switches are used to control the resistors being connected to the right positions for different DEM steps. For serial resistive divider, each resistor has 5 switches, which control the resistor to be connected to V_{DD}, GND and the neighbor resistors and to the voltage output. While for parallel divider, each resistor

Demand	Limit
Area	<10% of original area
Power Consumption	<50mK self heating
Thermal Noise	Comparable to noise of V_{BE}
Ratio Error	<50mK in temperature error

Figure 13: Requirements of voltage divider

has only 2 switches to connect it to V_{DD} and GND. For the simplicity point of view, the parallel divider is a better choice.

Besides, the on-resistance of switches are hard to control in serial resistive voltage divider due to the different overdrive voltage. Mismatch of the on-resistance of switches at different voltage levels causes extra error in divider ratio and cannot be completely removed by DEM. While for parallel divider, matching can be implemented by proper design the size of NMOS switches(connect the resistor to GND) and PMOS switches(connect the resistor to V_{DD}) for the selected supply voltage where calibration is performed.

On the other hand, for the same value of total resistance, the serial resistive divider consumes less current. For the same current consumption, the total resistance of parallel divider need to twice of serial divider for the divider ratio of 1/3. In general, for a divider ratio of 1/n, the total resistance of parallel divider needs to be (n-1) times of serial divider to have the current consumption.

Although for the limited current consumption, the parallel resistive divider consumes more area for resistors, but it save some area for less number of switches.

Finally, the parallel resistive voltage divider is chosen for generating an on-chip reference signal for voltage calibration.

3.2 specifications of the parallel voltage divider

The given basic requirements for the on-chip voltage calibration part is shown below:

The aim of the voltage divider is to generate a reference voltage with similar amplitude to that of V_{BE}(550mV) at room temperature. Since the supply voltage can be from 3.3 to 5.5V, the divider ratio of 1/8 for the supply voltage of 4.4V would be the proper choice.

Fig 14 illustrates the circuit of voltage divider for the ratio of 1/8 with DEM technique. The two-side switch can be implemented by one NMOS switch for GND-side connection and one PMOS switch for V_{DD} connection. Thus the final schematic of parallel resistive voltage divider is as shown in Fig15.

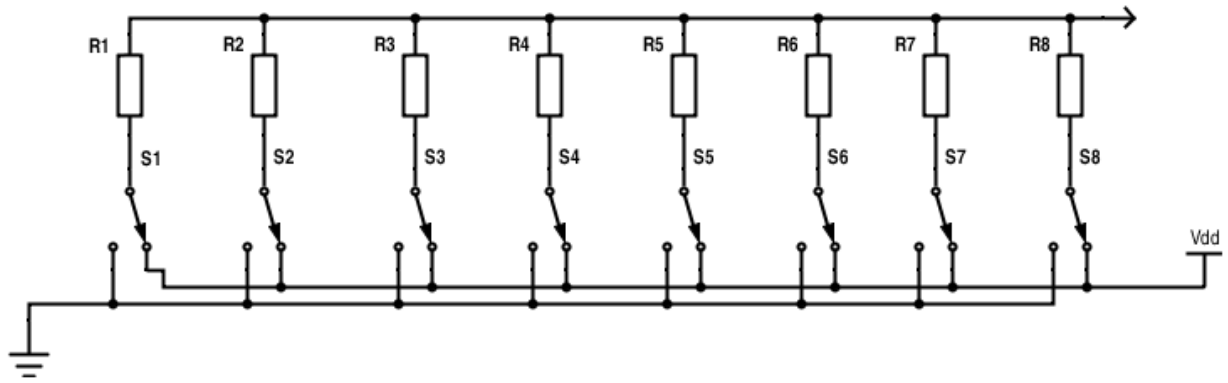

Figure 14: Parallel resistive voltage divider of 1/8 ratio with DEM

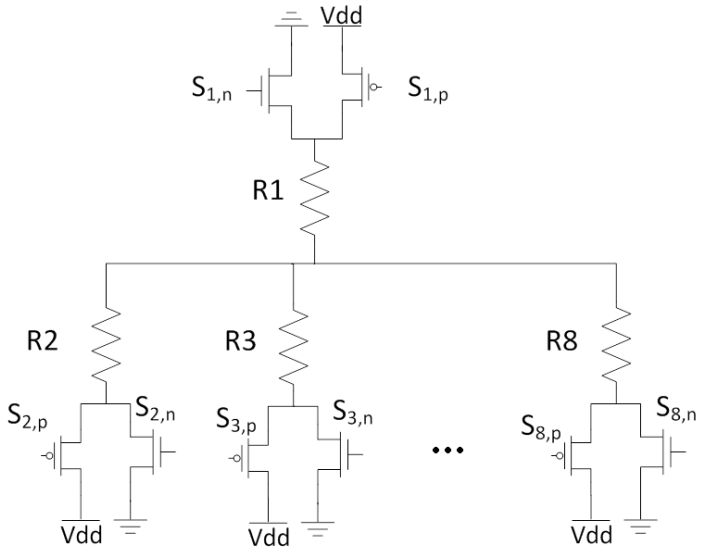

Figure 15: Parallel resistive voltage divider of 1/8 ratio with DEM

The specification in Fig 13 determines the design of resistance and the switch size, which are analyzed in the following sections.

3.2.1 Self-heating

The power consumption of the voltage divider causes extra self-heating induced error. With the thermal resistance of 270K/W and the maximum temperature error due to self-heating of 50mK, the maximum power that voltage divider can consume is

$$P_{max} = \frac{50mK}{270K/W} = 185\mu W$$

The minimum resistance for each resistor R_n(n=1 to 8) is then

$$R_{n,min} = \frac{7}{8}\frac{V_{DD}^2}{P_{max}} = 91.6k\Omega$$

3.2.2 Thermal Noise

The design target is the circuit noise will not increase significantly after replacing V_{BE} with the reference voltage from the voltage divider. Circuit design and analysis show that the total circuit noise is mainly controlled by the noise in PTAT current. The noise in CTAT current is non-dominate. So it is acceptable that the noise from voltage divider is compatible with that of CTAT current.

By the design of SMT172, the total current noise in I_{PTAT} at room temperature(T=300K) is

$$i_{n,PTAT} = 5.1 \times 10^{-13} A/\sqrt{Hz}$$

The equivalent voltage noise in V_{BE} equals

$$v_{n,be} = i_{n,PTAT} \times R_{BE} = 9.3 \times 10^{-8} A/\sqrt{Hz}$$

The value of the equivalent resistor(R_{eq}) which generates the same amount of the thermal noise, based on $v_n^2 = 4kTR_{eq}$ amounts to

$$R_{eq} = \frac{v_{n,be}^2}{4kT} = 522k\Omega$$

In order not to generate thermal noise larger than that of I_{PTAT}, the resistance for each resistor should be less than

$$R_{m,max} = \frac{7}{8} R_{eq} = 456k\Omega$$

$R_{n,min}$ and $R_{n,max}$ indicate the range of the parallel voltage divider. For the concern of the chip area, the resistance R_n was chosen to be 91.6kΩ.

3.2.3 Ratio error due to mismatch in on-resistance

Although it is proven that DEM can remove the ratio error resulting from the mismatch between resistors, the difference between the on-resistance of PMOS and NMOS switches also causes error in on-resistance between NMOS and CMOS less than 50mK in temperature domain.

With given design parameters of SMT172, T=300K, V_{BE} = 550mV, the duty cycle is 0.4238. If 1mV increase in V_{BE}, the duty cycle is changed to 0.4227 corresponding to a change of in -0.24K in temperature output.

Therefore, the error in V_{ref} caused by mismatch between on-resistance of NMOS and PMOS is limited to $\pm 0.2mV$. This corresponds to an ratio error of $\pm 3.6 \times 10^{-4}$ for 4.4V supply voltage. With the resistance of $R_n = 91.6k\Omega$, the maximum difference between the on-resistance of PMOS and NMOS switches is then

$$\Delta R_{on,max} = \frac{8}{7} \times R_n \times \sigma_{r,max} = 37.6\Omega$$

SMT172 has been fabricated in $0.7\mu m$ CMOS technology of On-Semiconductor. Based on its technique document, the variation of MOS is about 30%. The on-resistance of NMOS and PMOS switches should not be larger than 63Ω.

The on-resistance of a MOS transistor is given by

$$R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L} V_{gt}} \tag{27}$$

where μ is the mobility of majority carrier, C_{ox} is capacitance of silicon oxide, $\frac{W}{L}$ is the width-length ratio of MOS transistor and V_{gt} is the overdrive voltage. To get low on-resistance of transistor, either increasing V_{gt} or $\frac{W}{L}$ is sufficient. Since V_{gt} is determined by supply voltage, which is fixed, the only way to reduce the on-resistance is to enlarge the ratio. With given technical parameters, the $\frac{W}{L}$ of NOMS and PMOS switch have been calculated to be $64\mu m/0.7\mu m$ and $198.4\mu m/0.7\mu m$ respectively.

3.3 Logic control

As shown in Fig 16, PD pin of SMT172 has been reused to control the sensor switching between calibration mode and normal operation mode. When PD pin is set to LOW(PD pin connected to GND), the sensor is in voltage calibration mode, the voltage divider is in working condition, V_{ref} is connected to INP; when PD pin is set to HIGH (PD pin connected to V_{DD}), the sensor is in the normal operation mode, V_{BE} is connected to INP, the voltage divider part is not in use and thus turned off. To eliminate the leakage, the size of two NMOS switches in Fig 16 is chosen to be 10 $\mu m/1\ mum$.

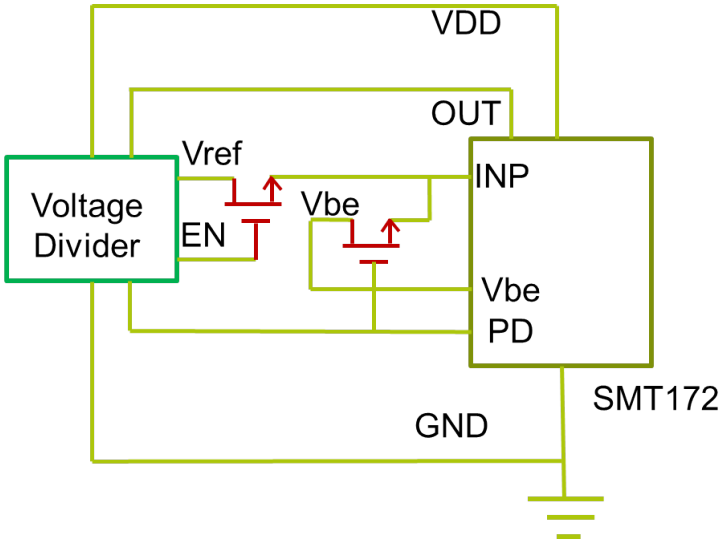

Figure 16: Structure of switch between $V_{ref}$and V_{BE}

In order to control the switches in Fig 16 during DEM, a logic control circuit has been designed, as shown in Fig 17.To determine the mode that SMT172 is in, the PD pin is reused to control the sensor. Unlike other sensors employing external clock, the output signal of SMT172 can be used to generate clock and control signal. Fig 17(a) is a 3-bit clock circuit based on three flip-flops, and the clock signals Q1 to Q3 are used to generate control signal S1 to S8 for switches in Fig 15. In the clock circuit, EN=NOT PD, which enables the clock circuit is working only when PD is set to LOW for voltage calibration.

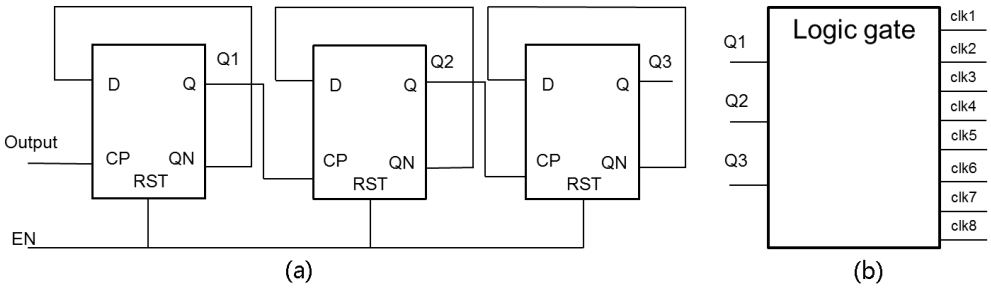

Figure 17: Generator of DEM control signal

The waveforms of clock signals Q1 to Q3 and the switch control signals are shown in Fig 18

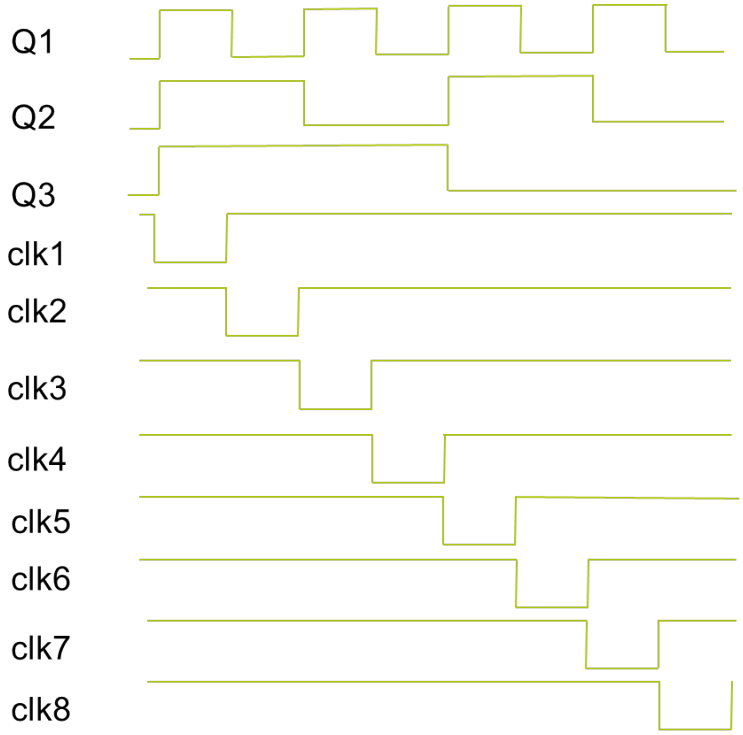

Figure 18: Waveforms of clock signals and control signals for voltage divider with DEM

Additionally, the PD signal is also combined with above control signals to ensure that the voltage divider is only activated in voltage calibration mode (PD = 0), which means that PD=HIGH, controls signals are all set in the way that all PMOS switches are OFF and NMOS switches are ON. In this situation, $V_{ref} = 0$.

3.4 Simulation result

With the design parameters: R1=R2=...=R8=91.6kΩ, W/L=64μm/0.7μm for NMOS switches and W/L=198.4μm/0.7mum for PMOS switches, the clock and logic circuit in Fig 17, the complete circuit of voltage divider has been simulated with software Cadence.

The waveform of the output signal V_{ref} is shown in Fig 19 when PD equals is set to LOW. The spikes result from clock overlaps and switch charge injections. Calculations show that the total

temperature error caused by the spikes is approximately 1.94mK, which is negligible.

With DEM control, the final reference voltage is shown in Fig 19 when PD equals 0.

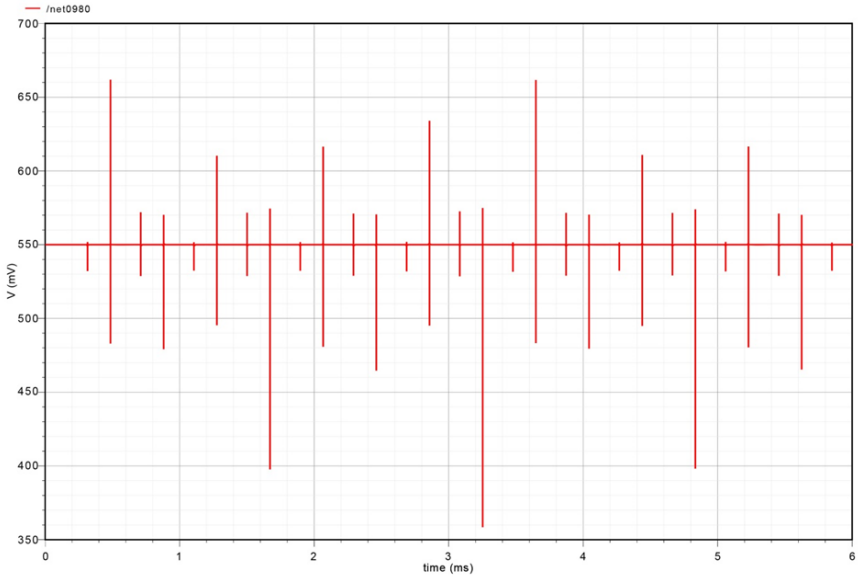

Figure 19: Reference voltage

The spikes result from clock overlaps. The temperature error caused by spikes is 1.94mK, which is negligible.

When PD signal is set to HIGH, voltage divider will be turned off as in Fig 20. The reference signal V_{ref} goes to zero and it disconnected to the input of the sensor circuit.

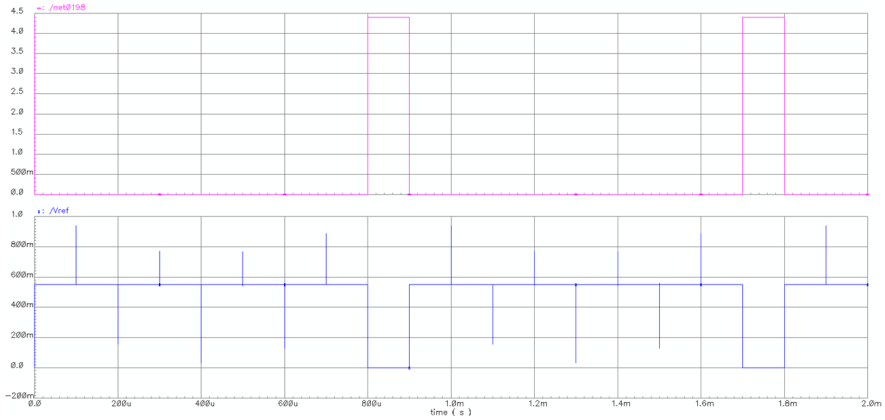

Figure 20: Reference voltage at different PD status

The ratio error occurs due to mismatch in on-resistance of switches has been simulated using Monte Carlo analysis and corner analysis for higher temperatures. Fig 21 shows the Monte Carlo analysis with 100 runs. The maximum corresponding temperature error is 35mK. The simulation shows that the design meets the target requirements.

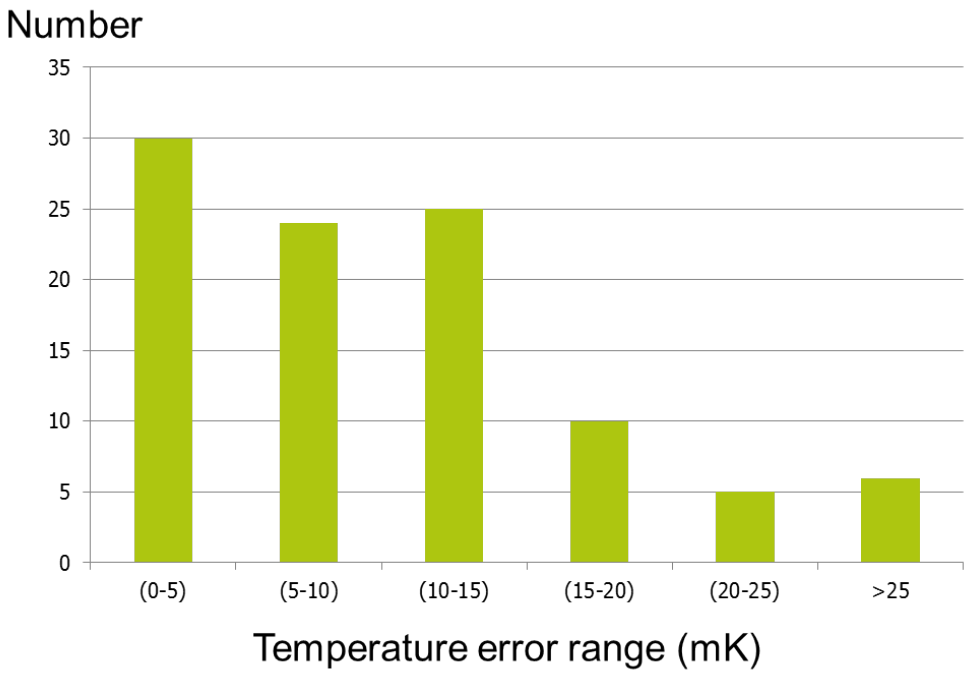

Figure 21: Monte Carlo analysis for temperature error caused by variation of voltage divider

Fig 22 shows the simulation of the corresponding temperature error for different MOS corner models versus temperature. The dash line indicates the limit of temperature error. The simulation results show that the temperature error caused by mismatch in on-resistance of switches is above the design limit at temperature higher than $100°C$. in order not to exceed the limit of temperature error, the voltage calibration should be performed at temperature lower than $100°C$. In most of the case, the calibration is performed at room temperature.

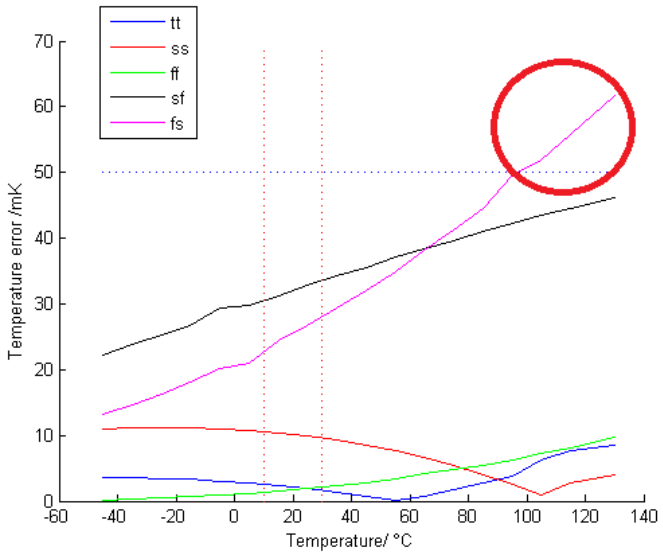

Figure 22: Conner analysis among different temperatures

Component	Value
R_1 to R_8	91.6kΩ
NMOS switches	W=64µm L=0.7µm
PMOS switches	W=198.4µm L=0.7µm

Figure 23: The value of the components for voltage divider

The table above summarized the values of the components for voltage divider. The simulation results show that the voltage divider with DEM can provide a reference signal for voltage calibration, where the extra error due to mismatch in on-resistance of switches can be less than 50mK for all corner model provided that the calibration is performed at temperature lower than $100°C$.

3.5 Layout

In order to avoid any potential crosstalk between analog circuits and digital circuits, the layout of voltage divider was separated in four pars: Resistors, PMOS switches, NMOS switches and clock/logic circuit, as shown in Fig 24. The digital bus and analog bus are lied at two sides of the whole block [5].

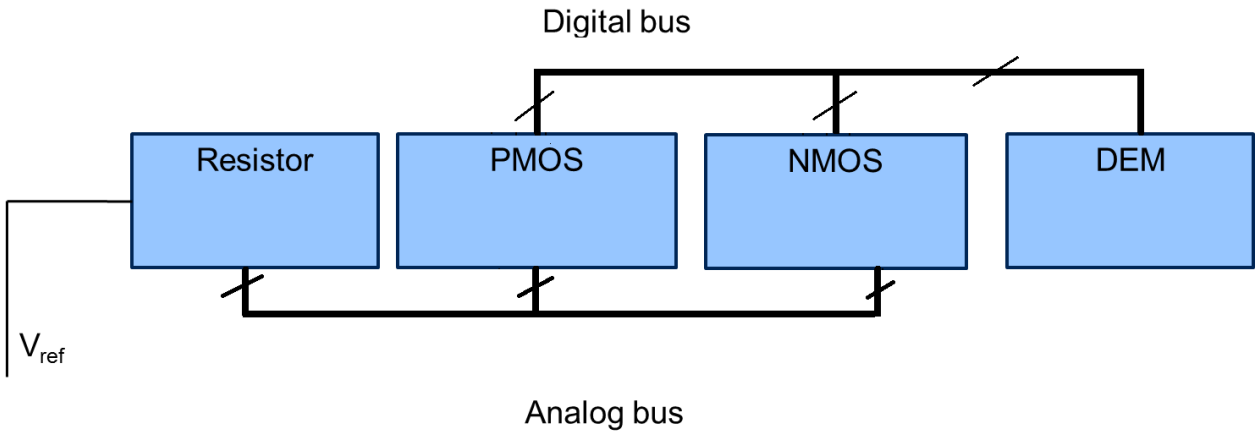

Figure 24: Layout diagram of voltage divider

The layout of total voltage divider with DEM control is illustrated in Fig 25. From left to right, there are the resistors in gray, PMOS and NMOS switches in orange and clock/logic in purple. The total area is $1200\mu m \times 107\mu m$ which occupies about 10% of the original sensor.

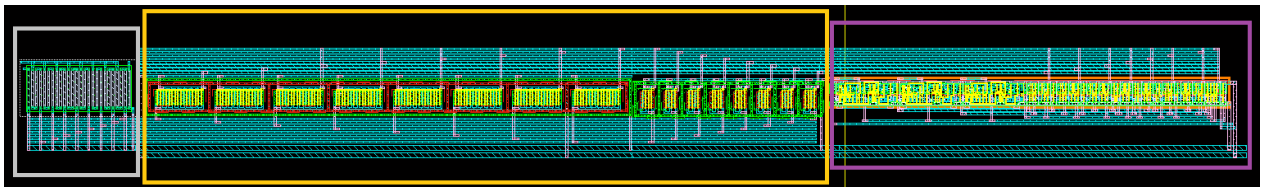

Figure 25: Layout ot voltage divider with DEM control

Fig 26 shows the layout of the whole sensor including voltage divider(on top side). Beside the voltage divider, an extra PAD is added to detect the value of V_{ref} for further experimental investigation.

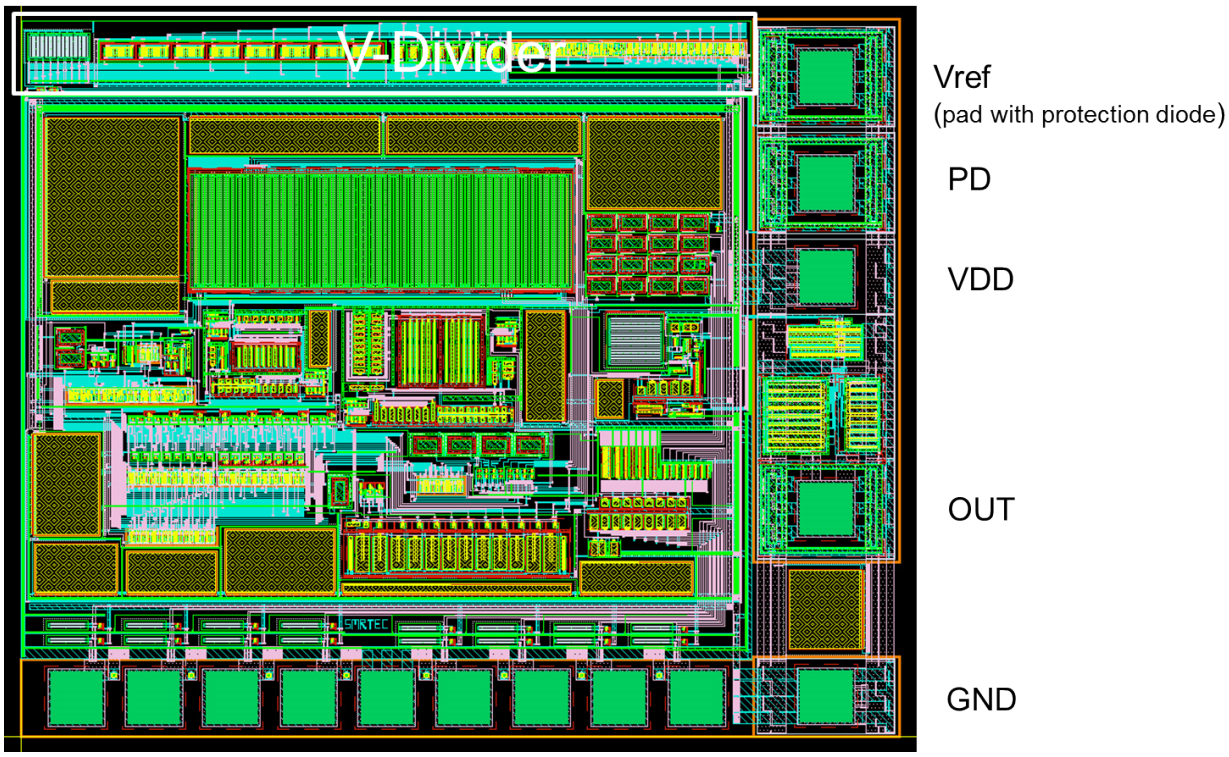

Figure 26: Layout ot voltage divider combined with original sensor

4 Measurement Set up

The sensor with on-chip voltage divider for voltage calibration has been fabricated in the same technology of $0.7\mu m$ CMOS of On-Semiconductor. Fig 27 shows the photomicrograph. The total chip area is $1.7\mu m \times 1\mu m$.

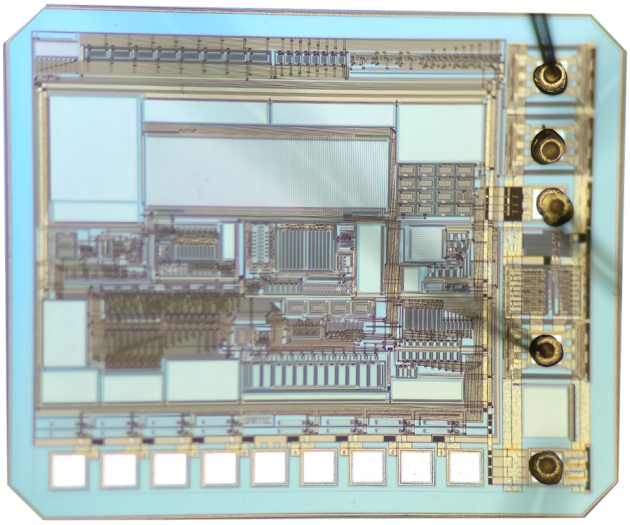

Figure 27: Photomicrograph of the chip

The sensor has been packaged in $TO-5$ due to the good thermal conductivity as in Fig 28. There are 5 pins representing V_{dd},V_{ref},GND,PD and $Output$ respectively.

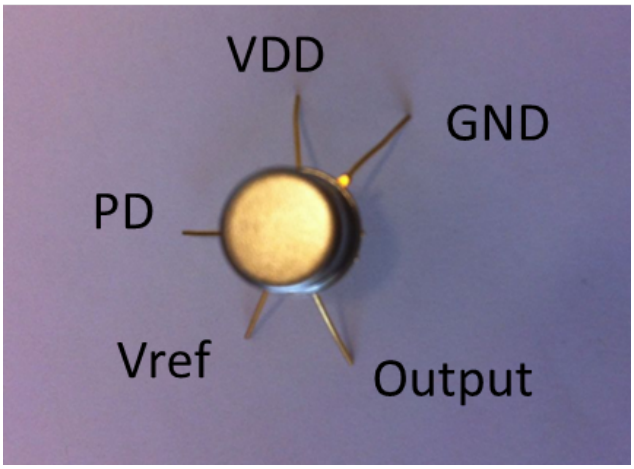

Figure 28: Photo of packaged sensor

4.1 Inside the oven

To stabilize the ambient temperature, an aluminum block as in Fig 29 is used as a good thermal conductor. Due to the much higher thermal conductivity of aluminum than that of air, this block acts as the thermal buffer to prevent fast temperature fluctuations. As Fig 29 shows, the oven PCB is placed on the top of the block and the sensors are placed in the holes on the surface. Besides, the

gap between the sensors and the holes has been filled with thermal paste to ensure good thermal contact. Such set up can ensure that the temperature of the sensors is identical to that of the reference temperature sensor, which is a well calibrated platinum resistor $Pt100$ reference [7]. The red circle indicates where the $Pt100$ temperature sensor is located.

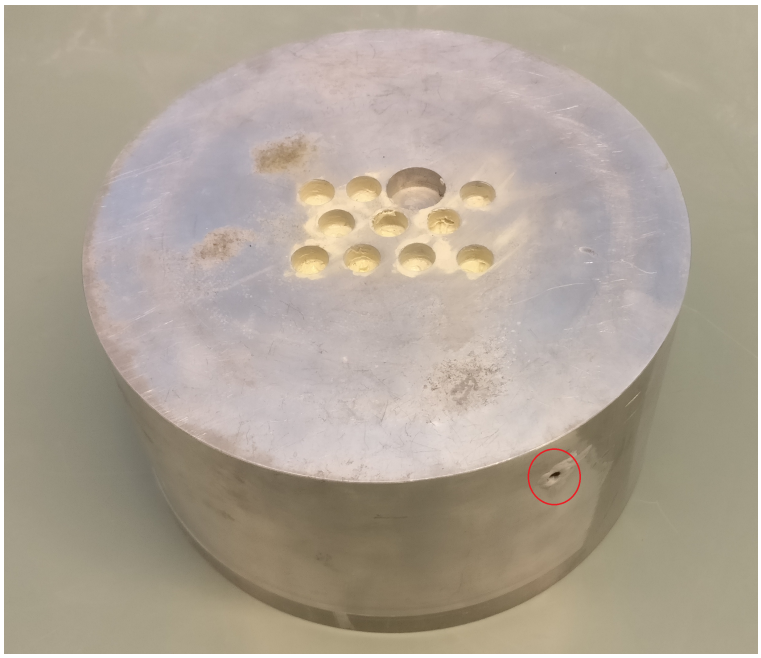

Figure 29: Aluminum block as thermal low pass filter

4.2 Measurement diagram

Fig 30 shows the complete block diagram of the measurement set up. The oven PCB is the PCB where all sensors are place on inside the oven. The selector PCB is used to choose one sensor at one time for measurement. Instead of choosing electronic selector such as Multiplexer, relay has been used as a passive switch here. The first reason is multiplexer changes the rising and falling edge of square wave output of sensor, which may cause extra reading error. Besides, the on-resistance of multiplexer is much higher than relay($50m\Omega$) which results in a certain voltage drop in supply voltage, which causes extra error for voltage divider and thus the accuracy of reference voltage is affected.The FPGA board reads the output of sensors as described in Section 2.2. The voltmeter is used to monitor the reference voltage.

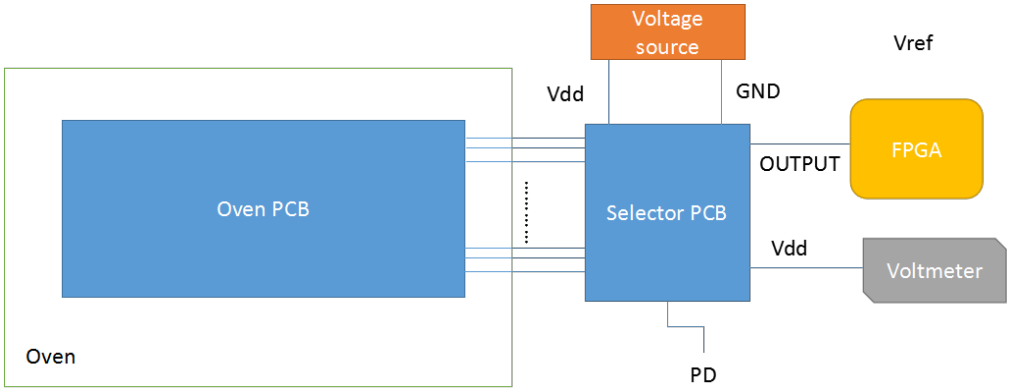

Figure 30: The block diagram of the measurement set up

4.3 Measurement flow

The measurement consists of:

a Accuracy of divider ratio, the accuracy of the reference voltage determines the accuracy of the voltage calibration.

b Measure the sensor output at normal operation mode.

c Measure the sensor output at calibration mode.

d Measure the temperature of the metal block use the reference temperature sensor $Pt100$.

Measurement b, c and d are measured at different temperatures. At each temperature point, the oven temperature was kept stable during the measurement.

By data processing the information, the measurement b to d have been performed over the whole temperature range from -45°C to 130°C with a step of 20°C.

5 Results and discussion

This section presents the measurement results of temperature sensor with voltage calibration. Since we want to calculate the value of V_{ref} relying on the ratio of voltage divider, the first step is to check whether the ratio is accurate enough. Then the original temperature error is presented. Finally, the error after trim based on different calibration methods is shown and comparison is made according to these results.

5.1 Ratio of voltage divider

Fig 31 shows the voltage error of voltage divider at different supply voltages. The figure indicates that the inaccuracy increases with lower voltage. A possible reason is that lower supply voltage results in higher on-resistance of switches (see equation27), which causes larger absolute mismatch of on-resistance difference between NMOS and PMOS switches. Even so, the error at supply voltage of 4.4V is still less than the target limit of 0.2mV. The output of voltage divider with DEM is accurate enough to be used as a reference in voltage calibration.

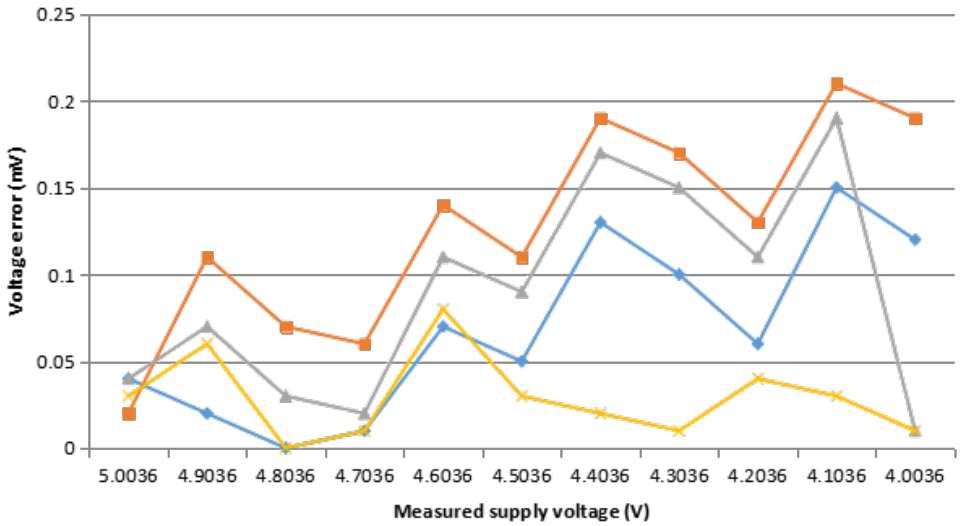

Figure 31: Voltage error at different supply voltages

5.2 Temperature error

For SMT172, the traditional calibration method is to adjust the area of V_{BE3} of Q_3 in Fig 7. As shown in Fig 32, during calibration,extra transistors $Q_{3-0,7}$ can be added in parallel to Q_{3A} until the sensor's output is equal to that of the reference sensor (within a trimming inaccuracy limit of 50 mV).

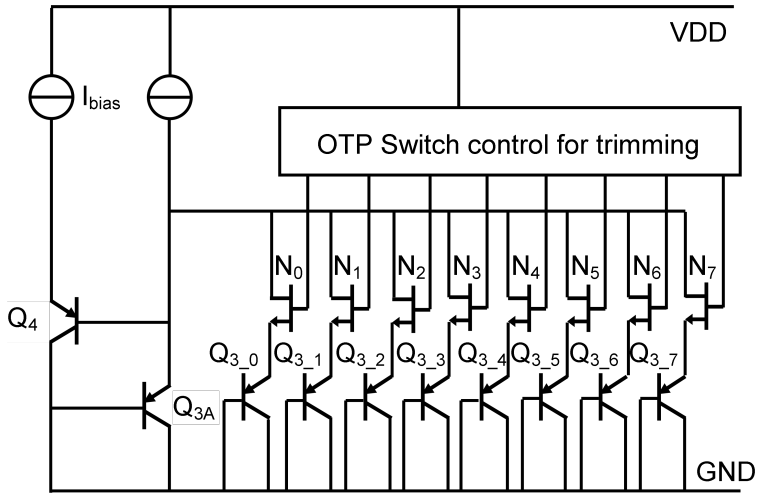

Figure 32: Calibration network of SMT172

5.2.1 Original temperature error and PTAT trimming

Since emitter area of Q_3 can only be added from its minimum value (V_{BE3} at maximum value), which is not the nominal design value, the untrimmed sensor in general shows a negative temperature error compared to reference sensor (larger V_{BE3} causes duty cycle to decrease). Fig 33 shows the measured temperature sensor output and that of reference sensor.

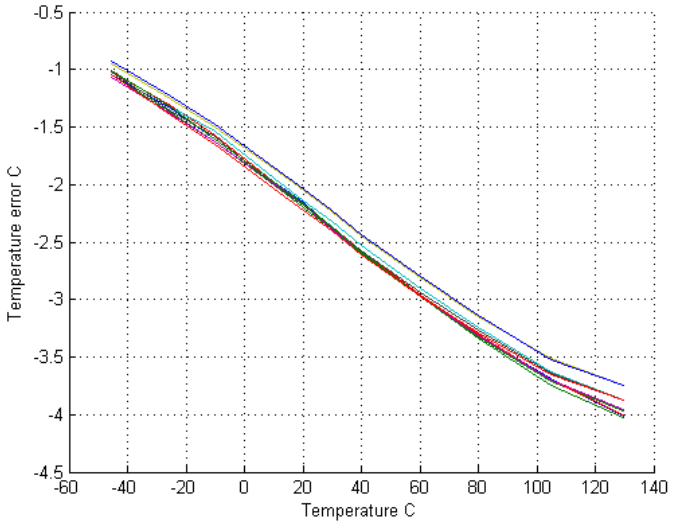

Figure 33: Original temperature error of SMT172

The relationship of temperature error and temperature can be taken linear. Therefore, an average master curve can be generated and used to perform the batch calibration. Based on this master curve, the linear errors have been removed, as shown in Fig34.

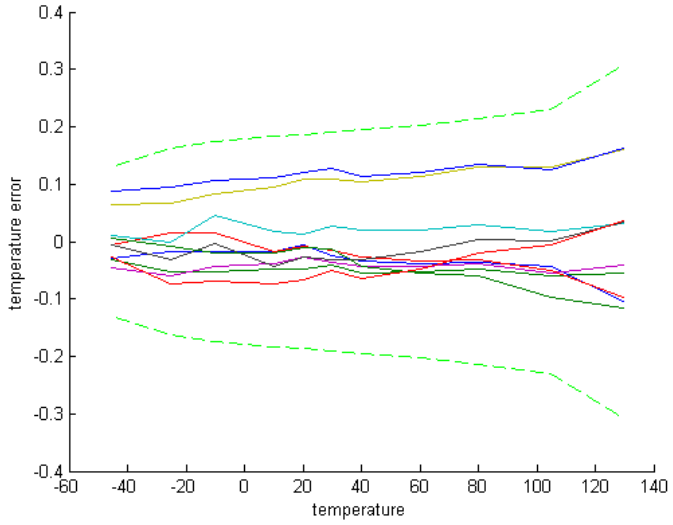

Figure 34: Temperature error after PTAT trimming

The green dash lines indicates the 3σ of 0.3°C.

5.2.2 One point trim

Since the temperature error is linear to temperature (PTAT), if one exact point is known, the temperature error curve for the specific sensor can be estimated accurately. Fig 35 shows the result from one point thermal calibration at room temperature ($30°C$). The trimming is done in software

by removing the calculated error. Compared to error after PTAT batch trimming, the 3σ is reduced to 0.16°C.

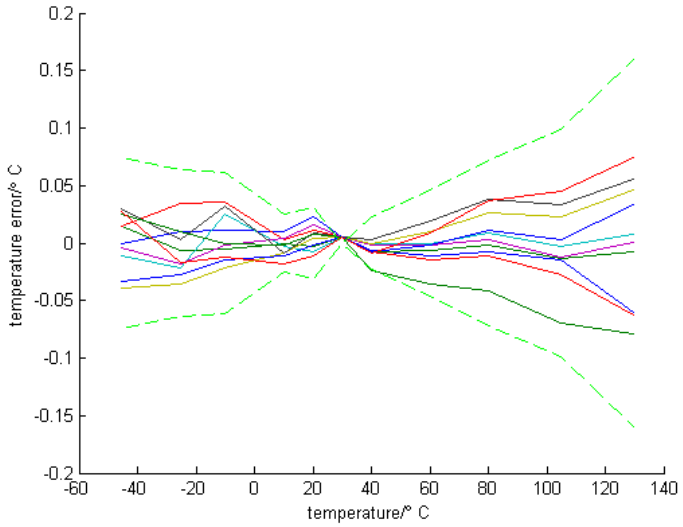

Figure 35: Temperature error after one point trimming based on thermal calibration

As it is introduced in Section 2.2, the idea of voltage calibration is to indirectly "measure" the temperature based on reference voltage and digital output. In SMT172, the original output is described in equation18. Replacing V_{BE} with V_{ref}, the new digital output is

$$D_{cal} = \frac{3\frac{\Delta V_{BE}}{R_{PTAT}} - 0.5\frac{V_{ref}}{R_{be}}}{2\frac{\Delta V_{BE}}{R_{PTAT}} + 0.5\frac{V_{ref}}{R_{be}}} \tag{28}$$

Because V_{ref} and D_{cal} are known and other parameter are well designed, ΔV_{BE} is calculated as

$$\Delta V_{BE} = \frac{D_{cal}+1}{3-2D_{cal}}\frac{R_{PTAT}}{2R_{be}}V_{ref} \tag{29}$$

The extracted ΔV_{BE} versus temperature shows that the measured values deviate from the Cadence simulation result, as shown in Fig 36. A the master curve has been extracted as the red dash line while the black dash line indicates the relationship based on Cadence simulation. The difference between the simulation and measurement corresponds to a constant offset of $95\mu V$, which may be due to residual offset.

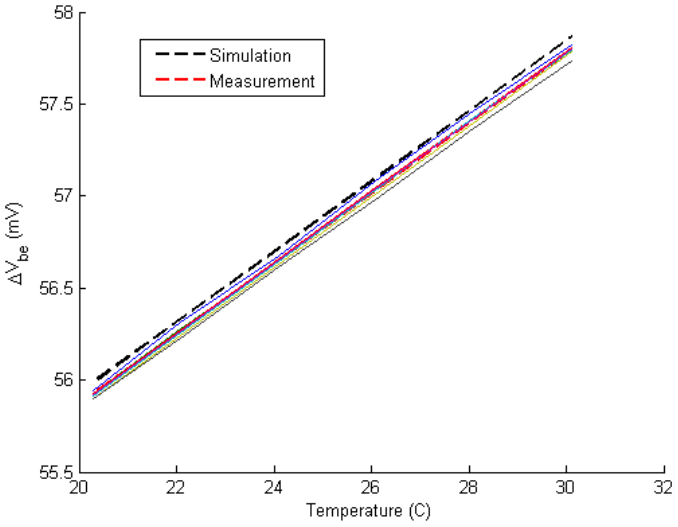

Figure 36: Relationship between calculated ΔV_{BE} and temperature with simulation curve and real master curve

Although there is difference between the measured ΔV_{BE} and the calculation result, it is still possible to perform voltage calibration based on the measured ΔV_{BE} around room temperature, providing the variation from sample to sample, from batch to batch is whithin certain limit. Fig 37 shows the temperature error between the extracted sensor temperature based on ΔV_{BE} calculation. T_{chip} and the value measured by reference temperature sensor $Pt100$ over temperature range from $20°C$ to $30°C$ for 10 samples. According to this, the calibration error will be within $0.12°C$.

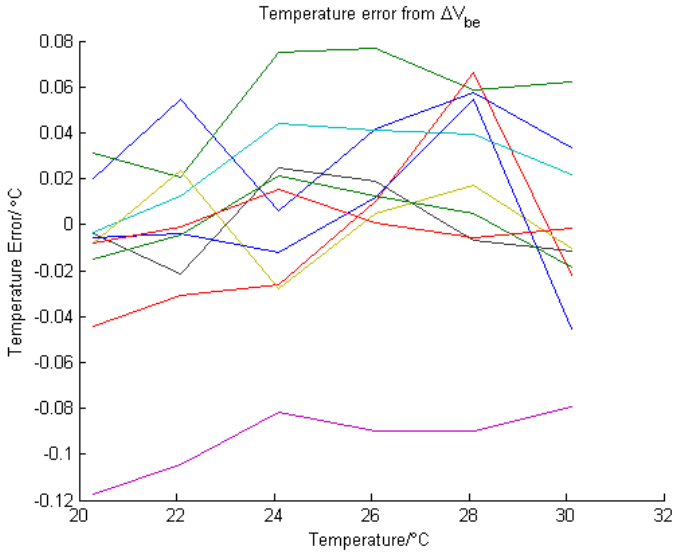

Figure 37: Temperature error results between T_{chip} and reference temperature

Based on the temperature extracted from the ΔV_{BE} calculation at $30°C$(red dash line of Fig 36), the temperature error is corrected over the whole temperature range digitally, the result is shown in Fig 38, which indicates the result after voltage calibration.

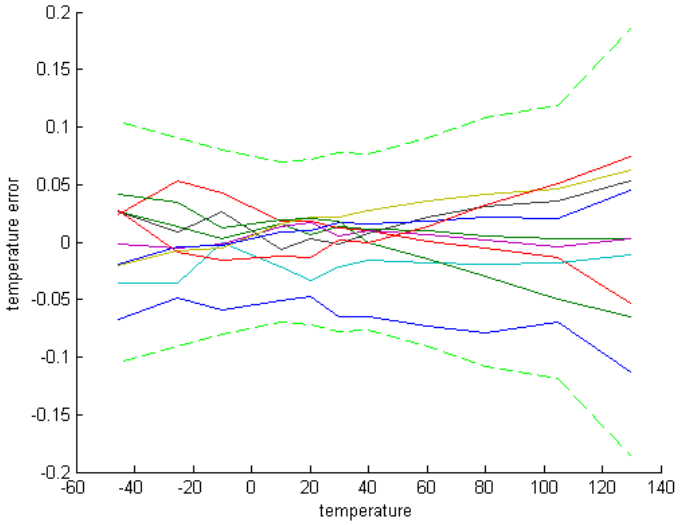

Figure 38: Temperature error after one point trimming based on voltage calibration

The 3σ of voltage calibration in Fig 38 amounts to 0.185°C, which is only slightly larger than that of one point thermal calibration. This means that with voltage calibration similar accuracy can be achieved.

5.3 Work to be done

The voltage calibration is based on the accuracy of ΔV_{BE} calculation. Variation of ΔV_{BE} versus temperature between samples and batches will cause extra inaccuracy in voltage calibration. Fig 38 shows that the variation between samples in one batch is smaller than $0.185°C$.

The variation of ΔV_{BE} versus temperature for different batches needs to be investigated to see if the master curve of ΔV_{BE} versus temperature from one time investigation can be applied to other different batches.

6 Conclusion

In this thesis, the principle and implementation of voltage calibration of BJT-based temperature sensors has been presented. In order to perform voltage calibration without using external reference signal, an on-chip voltage divider has been designed and implemented. The voltage signal from the divide has been used as reference for voltage calibration. Measurement results of 10 samples show that the inaccuracy of the reference signal from the voltage divider is less than the target limit of 0.2mV, and is accurate enough for performing voltage calibration.

Measurement result shows that the signal ΔV_{BE} is not exactly equal to that in Cadence simulation. Based on the master curve of ΔV_{BE} versus temperature, the accurate ΔV_{BE} at room temperature has been derived. Voltage calibration has been performed digitally based on the temperature information calculated from the derived ΔV_{BE} value at $30°C$. The result of 10 samples show that the spread of temperature error(3σ) is $0.185°C$, which is very close to that of one-point thermal calibration of $0.16°C$.

Compared to conventional thermal calibration, the voltage calibration does not require expensive reference temperature sensors, which makes the calibration cost much lower. Moreover the voltage calibration does not require the whole set up to wait until the wafer temperature is identical to that of the reference temperature sensor, which makes the calibration fast. It only requires that the wafer temperature does not change above a certain limit(say 10mK) during calibration mode and normal operation mode to prevent extra calibration error.

More investigations of ΔV_{BE} versus temperature for different batches need to be done, which determines if one master curve can be applied to all batches.

References

[1] Micheal AP Pertijs and Johan Huijsing. *Precision temperature sensors in CMOS technology*. Springer Science & Business Media, 2006.

[2] MAP Pertijs, AL Aita, KAA Makinwa, and JH Huijsing. Voltage calibration of smart temperature sensors. In *Sensors, 2008 IEEE*, pages 756–759. IEEE, 2008.

[3] Gerard CM Meijer. Thermal sensors based on transistors. *Sensors and Actuators*, 10(1):103–125, 1986.

[4] Anton Bakker and Johan H Huijsing. Micropower cmos temperature sensor with digital output. *IEEE Journal of Solid-State Circuits*, 31(7):933–937, 1996.

[5] Ray Alan Hastings. *The art of analog layout*. Prentice Hall, 2006.

[6] T Quarles, AR Newton, DO Pederson, and A Sangiovanni-Vincentelli. Spice3 version 3f3 users manual. *University of California, Berkeley, CA*, 94720, 1993.

[7] Kamran Souri and Kofi Makinwa. Ramp calibration of temperature sensors. In *Advances in Sensors and Interfaces (IWASI), 2011 4th IEEE International Workshop on*, pages 67–70. IEEE, 2011.

[8] Ali Heidary, Guijie Wang, Kofi Makinwa, and Gerard Meijer. 12.8 a bjt-based cmos temperature sensor with a 3.6 pj· k 2-resolution fom. In *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pages 224–225. IEEE, 2014.

[9] William Ralph Bennett. Spectra of quantized signals. *Bell System Technical Journal*, 27(3):446–472, 1948.

[10] Kamran Souri, Youngcheol Chae, and Kofi AA Makinwa. A cmos temperature sensor with a voltage-calibrated inaccuracy of 0.15 c (3) from 55 c to 125 c. *IEEE journal of solid-state circuits*, 48(1):292–301, 2013.

[11] Gerard CM Meijer, Guijie Wang, and Fabiano Fruett. Temperature sensors and voltage references implemented in cmos technology. *IEEE Sensors Journal, 1 (3)*, 2001.

[12] Albert D Helfrick and William David Cooper. *Modern electronic instrumentation and measurement techniques*. Prentice Hall, 1990.

[13] Buran I Keprta Jr and William A West. Resistive voltage divider, June 30 1970. US Patent 3,518,603.