Virtual Thermo-Mechanical Prototyping of Microelectronics Devices

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Contents

Glossary

ARE	Area Release Energy
ASTM	American Society for Testing and Materials Standards
BEOL	Back End of Line
BOM	Bill Of Materials
BT	Bismaleimide Triazine
BGA	Ball Grid Array
CMOS	Complementary Metal Oxide Semiconductor
COB	Chip On Board
C-SAM	C-mode Scanning Acoustic Microscopy
CSP	Chip Scale Package or Chip Size Package
CME	Coefficient of Moisture Expansion
CTE	Coefficient of Thermal Expansion
CVD	Chemical Vapour Deposition
DBS	DIL Bent SIL power package
DIP	Dual Inline Package
DNP	Distance to Neutral Point
DOE	Design Of Experiment
DRAM	Dynamic Random Access Memory
DSP	Digital Signal Processors
EGO	Efficient Global Optimisation
EI	Expected Improvement
FC	Flip Chip
FEM	Finite Element Method
FET	Field Effect Transistor
FR4	Flame Retardant Type 4
Ge	Germanium
GQS	General Quality System
HAST	Highly Accelerated Stress Test
HBGA	Heatsink Ball Grid Array
HTOL	High Temperature Operating Life
HTSL	High Temperature Storage Life

IC	Integrated Circuit
IEC	International Electro technical Commission
IEEE	Institute of Electrical and Electronics Engineers
IMAPS	International Microelectronics And Packaging Society
IMC	Inter Metallic Compound
IO	Input Output
IPC	Institute for Interconnection and Packaging electronic Circuits
ITRI	Interconnection Technology Research Institute
ITRS	International Technology Roadmap for Semiconductors
JEDEC	Joint Electron Device Engineering Council
LED	Light Emitted Diode
LEFM	Linear Elastic Fracture Mechanics
LH	Latin Hypercube
LSI	Large Scale Integration IC
LTCC	Low Temperature Co-fired Ceramic
MCM	Multi Chip Module
MEMS	Micro Electro Mechanical Systems
MPW	Multi Project Wafer
MSL	Moisture Sensitivity Level
NEMI	National Electronics Manufacturing Initiative
NIST	National Institute of Standards and Technology
PCB	Printed Circuit Board
PoP	Package on Package
ppm	parts per million
ppf	pre-plated frame
PPOT	Pressure POT test
Precon	Preconditioning
PSG	PhosphoSilicate Glass
PV	PassiVation
QFN	Quad Flat package No lead
QFP	Quad Flat Package
RF	Radio Frequency

RH	Relative Humidity
RSM	Response Surface Model
SEM	Scanning Electron Microscope
SEMATECH	SEmiconductor MAnufacturing TECHnology consortium
SEMI	Semiconductor Equipment and Materials International
Si	Silicon
SIL	Single In Line package
SiP	System in Package
SMD	Surface Mount Device
SMT	Surface Mount Technology
SO	Small Outline package
SOC	System On Chip
SOT	Small Outline Transistor
SSOP	Shrink Small Outline Package
TEOS	TetraEthylOxiSilane
TFBGA	Thin Fine pitch Ball Grid Array
TO	Transistor Outline
Tg	Glass transition temperature
TMCL	Temperature Cycling Testing
UBM	Under Bump Metallisation
UPOT	Unsaturated Pressure POT test
VCCT	Virtual Crack Closure Technique
VLSI	Very Large Scale Integration
VP	Virtual Prototyping
WLP	Wafer Level Package

Chapter 1

Introduction

1.1 Microelectronics Development

The semiconductors industry and its suppliers are the cornerstones of today's high-tech economy, representing a worldwide sales value of 250 billion euros in 2004 (ITRS, 2005). The microelectronics sector supported a global market of more than 6 trillion euros in terms of electronic systems and services. For the past fifty years, microelectronics products have pervaded our lives, with massive penetration into health, mobility, security and identification, communications, education, entertainment and virtually every aspect of human life.

The era of semiconductors started in 1959, when Jack S. Kilby, then at Texas Instruments, submitted a patent request on *miniaturized electronic circuits*. His invention demonstrated the feasibility of realizing resistors and capacitors based on semiconductor technology together with transistors in one and the same substrate. With that, the integrated circuit (IC) was born and Jack S. Kilby received the Nobel Prize in Physics in 2000, together with Zhores I. Alferov and Herbert Kroemer. Just a few years later, in 1965, Fairchild engineer Gordon E. Moore postulated a bold theorem that predicted exponential growth in the semiconductors industry [Moore, 1965]. He stated that:

> *The complexity for minimum component costs has increased at a rate of roughly a factor of two per year.*

Through the years, this growth in circuit complexity has become known as Moore's Law. Moore's Law, however, is not a law of nature, but rather an economic argument. Today, Moore's Law is the main mechanism behind the major technology trends in the microelectronics industry: miniaturization and function integration. From a business point of view, miniaturization and function integration means more features, less weight, handy size, less resources employment, more mobility and low price. The shift from the past era of microelectronics, where semiconductor devices were measured in microns, to the new era of microelectronics where they shrink to

dimensions measured in nanometers will make the semiconductor sector even more pervasive than it is today.

The smallest feature sizes on ICs are already falling to 65nm and beyond. The International Technology Roadmap for Semiconductors projects that in 15 years the smallest feature size will be even smaller than 10nm. Comparing it with the well-known quote from the Scientific American in 1977, stating that:

Present technology can routinely reproduce elements a few μm's across,

and it appears possible to reduce the smallest features to about one μm,

and one instantly grasps the enormous development over years. Modern semiconductor technology is characterized by key requirements such as development speed (lowest possible time to volume, first-time-right), optimised cost structures and highest quality (zero defects). But with the increase of the interconnect density, also an increase of power dissipation density and thus temperature is anticipated. The combination of both miniaturization and function integration trends drives microelectronics technology into an unknown level of complexity, characterized by ongoing miniaturization down to nano-scale, heterogeneous and multi-functionality, multi-discipline, multi-scale, multi-technology, multi-process, multi-material/interface, multi-damage and multi-failure mode. As consequences, we are confronted with ever increased design complexity, dramatically decreased design margins, increased chances and consequences of failures, decreased product development and qualification times, increased gap between technology advance and development of fundamental knowledge and increased difficulties to meet quality, robustness and reliability requirements. If the industry is going to rapidly decrease these sizes at high volume production during the next 15 years, then we need to face the challenges to design for sufficient product reliability today.

1.2 IC Packaging Development

The major development trends of miniaturization and function integration can also be recognized in IC packaging. Packaging has evolved during the last 3 decades, starting with 2 pins transistors (TO) in the late 1960s, wire bonding technologies in the mid 1970s, surface mount technologies (SMT) in the 1980s and Flip Chip (FC) technologies in the 1990s. Figure 1.1 indicates the packaging development trend over the years.

With the introduction of transistors in the late 1960's, protective packaging methods were needed. In the beginning, ceramic materials were the mostly used carrier, covered by a cap. As time progresses, metal-based carriers, leadframes, were introduced, which are substantially cheaper. As the volume increased, and the production became automated, metal leadframes became the favourite carrier for IC packaging technologies. As time progressed, many leadframe-based variants were introduced ranging from Dual In Line (DIP) and Small Outline (SO) in the 1970s, Quad Flat Packages (QFP) and DIL Bent SIL packages (DBS) in the 1980s. Exposed pad packages were introduced because of their excellent thermal and electrical performance. An example for this is HTQFP and HTSSOP were H stands for heat and T for thin. The exposed pad is a standard feature for QFN (Quad Flat No lead) packages, which is just recently introduced.

In the early 1990s, BGA-like packages were introduced based on a new multi-layer process; double-sided flex circuit pairs were stacked and laminated using adhesives to provide vertical connections. During the development stage, ideas emerged that moved closer to the current BGA packaging concept. The BGA family allows for low profiles and outlines and is currently the standard for high-density IO packages. The concept is based on using an organic laminate, be it FR4 or BT, including copper traces that connect to the IC using wire bonds and further on encapsulated by using a moulding compound. Many different variations are available on the market, such as TFBGA and HBGA, were F stands for fine pitch.

To replace the wire bonding technology, Flip Chip (FC) technology entered the packaging world in 1964, when IBM introduced its Controlled Collapse Chip Connection (C4) to directly interconnect ICs to their substrates. FC is the mounting of an IC with its active side facing the substrate. The electrical interconnection between the IC and substrate can be established by either solder bumps, metallurgy bumps, conductive polymers, anisotropic conductive adhesives, compliant bumps or pressure contacts. In microelectronics devices, the FC technology is primarily being used because of its high IO capability, small form factor and excellent electrical performance. Associated package formats are known as Flip Chip Ball Grid Array (FCBGA). Production cost, packaged device performance and overall size determine the choice between FC or wire bonding for IC interconnecting. Currently, FC has become the standard interconnect technology for microprocessors and logic chips for high-performance mainframe servers.

Continuing the drive for a small package, Chip Scale or Wafer Level packages (CSP, WLP) are introduced in the mid 1990s. CSP is a potentially attractive technology for a large variety of microelectronics applications. It is one of the most advanced packaging concepts. It combines the advantages of flip chip and conventional surface mount technologies. Like flip chips, CSP offer area array arrangements of interconnects and can be solder bumped efficiently at the back end structures of wafer processes. The increasing interest for CSP is mainly due to the fact that it offers the smallest form factor available - a real chip size! Combined with the fact that CSPs are generally manufactured at lower cost then conventional packages makes it the perfect choice for products in the low cost and handheld market. The strength of this concept - that it is real chip size - also is its limitation: the number of IOs that the package will allow is the number of IOs that can be routed in the application, usually at a pitch of 0.5mm or at best 0.4mm.

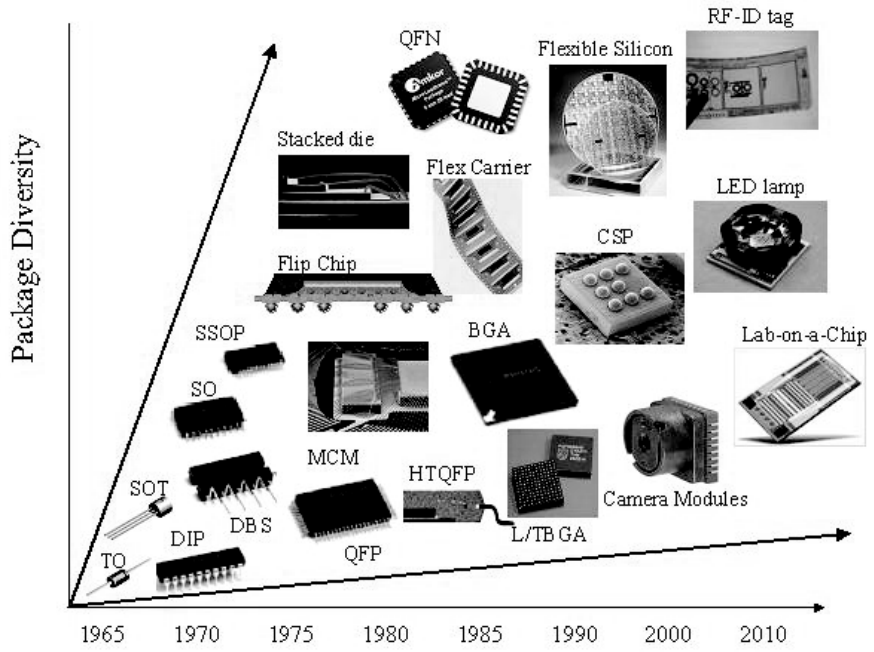


Figure 1.1: Packaging development trend.

Function integration into one package is covered by the development of the Multi Chip Module (MCM) in which several dies are placed into one package. Another level of integration can be reached by stacking multiple dies instead of placing them next to each other. An approach competing with stacking dies in one

package is stacking multiple packages leading to the so-called Package on Package (PoP) technology.

Due to the introduction of semiconductor solutions into other fields, the added value of packaging technologies have increased substantially. Examples are Micro Electro Mechanical Systems (MEMS), digital cameras in mobile phones and Light Emitted Diodes (LED). In these applications, packaging is a critical factor affecting the final costs. As such, the economic and technical importance of electronic packaging has greatly increased. According to the road maps, ICs will have more IOs, larger sizes, smaller pitches and higher operation temperatures in the next years. IC packages will be subjected to harsher environments, not only increased temperatures but also increased mechanical loading conditions such as vibration and impact. The key question for next-generation packaging is whether it can fill its traditional role of interconnecting, powering, cooling and protecting semiconductor ICs while also addressing these consequences. Combined with the business trends, mainly represented by cost reduction and shorter time-to-market, IC packaging technologies are driven into an unknown level of complexity. Again, the consequences are clear: dramatically decreased design margins, increased chances and consequences of failures, decreased product development and qualification times, increased gap between technology advance and development of fundamental knowledge and increased difficulties to meet quality, robustness and reliability requirements.

1.3 Thermo-Mechanical Reliability: Literature Review

Thermo-mechanical reliability of microelectronics devices is one of major concerns in the industry. Based on root cause analyses from observed failures of microelectronics components, it is found that these reliability problems are often triggered by various thermal and mechanical loadings associated with manufacturing processes. For example, during the backend process (metal depositions, etching and chemical vapour deposition) stresses are developed in IC layer stacks. The packaging manufacturing processes (such as moulding) further induce additional stresses in IC stacks. These deformations and stresses can become critical for product assembly, and may eventually endanger the targeted lifetime of the product during operations. It has shown that approximately 65% of all failures can be attributed to thermo-mechanical related effects during manufacturing processes [Bisschop, 2002; Zhang, 2003; Zhang *et al.*, 2006b]. In most cases, these thermo-mechanical reliability problems originate

from the design phase of product and process. Examples of failures are cracks, voids, delamination, buckling, hillocks, wire fatigue and many more. Thermo-mechanical reliability is becoming one of the major bottlenecks for both current and future microelectronics technologies.

Mechanics have been playing a prominent role in industrial and technological development for decennia, such as in aerospace and transport industries and in a very broad application spectrum of mechanical and civil engineering. Computational mechanics, such as Finite Element Methods, have also been impacting various industries and technologies for several decades, especially due to the rapid development of computational capability. Microelectronics products can be recognized as multi-layer structures. The earliest study in thermal stress of multi-layered structures is presented by Timoshenko [1925], who proposed a general theory, based on the beam theory, of bending of a bi-material subjected to a uniform thermal loading. With the introduction of the Finite Element (FE) method [Hughes, 1987; Zienkiwicz and Taylor, 1989], both 2D and 3D models are created that facilitate to predict stress and strain levels in bonded dissimilar materials under thermal loading conditions [Suhir, 1989; Eischen *et al.*, 1990; Pan and Pao, 1990; Jiang *et al.*, 1997]. At present, FE techniques are widely used to predict the stress and strain levels and their evolution during the different manufacturing stages of microelectronics devices.

Shen *et al.* [1996] investigated the stress and strain response of patterned lines on silicon wafers using the traditional Al/SiO_2 CMOS technology. van Silfhout *et al.* [2001] gave an overview on the state-of-the-art of thermo-mechanical modelling of ICs during backend processes and identified an industry need to speed up the development and application of advanced numerical techniques to optimise the mechanical behaviour of ICs. With the introduction of the Cu/lowk technology, to replace the traditional Al/SiO_2, this need became urgent to investigate new failures modes in ICs, such as debonding between the different layers [Du *et al.*, 2002]. This debonding turned out to be related with the (changed) backend process as investigated by Gonda *et al.* [2004] and Orain *et al.* [2004] and the metal layout as investigated by van Silfhout *et al.* [2004].

Numerous studies are performed to investigate the stress response of microelectronics during packaging manufacturing processes, with overviews reported by Kelly [2000] and Zhang *et al.* [2000]. Van Gestel [1994] combined FE modelling with a specially developed test IC capable of judging the reliability performance of

plastic packages. Liu and Mei [1995] studied the stress response of IC packages during epoxy moulding, moisture absorption and subsequent wave soldering processes, Yueng and Yuen [1996] during IC packaging and included the time-dependent response of the epoxy. Chen *et al.* [2000, 2002] used Raman spectroscopy to measure the IC stress levels after being manufactured into a package. FE studies on the wire bonding process indicate a strong interaction with the thin IC layers to which the wire is bonded to [Degryse *et al.*, 2004; Liu *et al.*, 2004, Srikanth *et al.*, 2005; Viswanath *et al.*, 2005].

All of the above mentioned FE studies have investigated a certain process, be it somewhere during IC or packaging processes, but none of them have integrated both. For the successful development of IC structures and processes, it is essential to take into account the influence of packaging manufacturing and reliability qualification. In this thesis, this so-called integral approach, accounting for all the major loading sources and history during the complete product creation process, will be demonstrated.

Given the large size differences from a nm-scale IC layer to a mm-scale package size, reliability predictions of the integral IC package level require advanced modelling techniques. These techniques include the use of contact algorithms, multi-level (or multi-scale) modelling, element birth and death (also referred to as activation and deactivation) techniques, advanced material constitutive models to include the time- and temperature-dependent response of the constitutes, and advanced mechanics theory, such as fracture mechanics to predict interface delamination and/or hygro-mechanics to predict the effect of moisture in the microelectronics device. The reminder of this section presents literature and background information on these topics.

Mercado *et al.* [2003a, 2003b] and Wang *et al.* [2003a] have used multi-level techniques to predict debonding in Cu/lowk technology for Flip Chip packages, where Fiori and Orain [2005] used it to evaluate bondpad architectures subjected to wire bonding forces. Their results showed that multi-level techniques can be successfully applied to cover the large size differences between ICs and packages. In this thesis, multi-level techniques combined with contact algorithms and element (de-) activation is used to cover the integral IC package approach.

Regarding constitutive material models for thermosetting resins, Kiasat [2000], Jansen *et al.* [2004a] and van Silfhout *et al.* [2005] describe a linear visco-elastic

theory and associated measurements for epoxy moulding compounds. Yi and Sze [1998] and Yueng and Yuen [1996] reported that by using a visco-elastic model for the moulding compound, the predicted stresses and deformations are closer to the real situations. A cure-dependent visco-elastic constitutive model is established as well to describe the evolution of material properties during the curing process of a thermosetting polymer [Ernst *et al.*, 2002; Ernst *et al.*, 2004; Jansen *et al.*, 2004b; Yang *et al.*, 2004b; van 't Hof, 2006]. The need for such a constitutive model is that package concepts such as QFN and BGA will be assembled in full map systems instead of the traditional strip systems. One critical issue for manufacturing such map systems is the warpage induced during the curing of the moulding compound, which has a significant contribution [Yang *et al.* 2004a; Yang *et al.* 2005]. In this thesis, where applicable, epoxy moulding compounds are described by a linear visco-elastic behaviour and the effect of this, compared to a linear approach, to accurately predict packaging induced warpage is presented.

For the metals used in packages, typically, visco-plastic constitutive models are used [Neu *et al.*, 2001; Sharma and Dasgupta, 2002; Schubert *et al.*, 2003; Wiese and Meusel, 2003; Erinc *et al.*, 2004; Dudek, 2006]. A variety of metals are available, including copper for leadframes and solders as interconnect material. Different solder compositions can be applied with the traditionally applied alloys containing lead, which is currently going to be replaced by other materials because of its toxic nature. But the solder still typical for electronic applications is the near-eutectic Sn60Pb40 alloy, frequently with 1-2% Ag and have been studied for decades [Dudek, 2006]. Much less is known about the lead-free alloys [Lau and Chang, 1998b; Wiese and Meusel, 2003]. The mechanical behaviour of solder is non-linear and temperature dependent and creep processes dominate the deformation kinetics. A variety of studies have been published concerning creep constitutive models and related properties of different solders [Grivas *et al.*, 1979; Darveaux and Banerji, 1998; Schubert *et al.*, 2003; Pang *et al.*, 2003; Clech, 2005]. In this thesis, where applicable, metal leadframes are described as an ideally elasto-plastic material and solders by a visco-plastic constitutive model based on Darveaux and Banerji [1998].

For glass like materials, which Silicon is, linear elastic and isotropic material behaviour is often used. However, given the nature of the silicon material itself, which is a crystal, rather anisotropic behaviour is expected. In this thesis, where applicable, an anisotropic material model for Silicon is used.

For packaging materials, above mentioned constitutive models and related material data refer to bulk properties, where the thin films used in ICs may behave significantly different [Pelletier *et al.*, 2002]. Based on isotropic assumptions, numerous experimental techniques are available to measure thin film properties, including wafer warpage, nano-indentation, bulge test, impulsive stimulated thermal scattering, X-ray diffraction and dual capacitor method. Measuring the warpage of processed wafers at room temperature is a regular method and provides a value for the total stresses in the layer at room temperature [Zhao *et al.*, 2000a; Lee and Bae, 2000]. With a small adaptation of the theory, material properties as Young's Modulus and CTE of thin films can be determined [Stoney, 1909]. Nano-indentation is derived from the hardness test for bulk materials in which a diamond tip is forced into the test surface at a selected rate and to a selected maximum force. During both the loading and the unloading operation the force and the tip displacement are recorded. A detailed analysis of the force-displacement curve then yields material parameters such as the elastic modulus and the hardness [Oliver and Pharr, 1992; Bolshakov and Pharr, 1998; Hay *et al.*, 1999; den Toonder *et al.*, 2003]. The bulge test is used for the determination of the residual stresses and the Young's modulus of a film. In this technique, the deflection of a suspended film is measured as a function of applied pressure [Neugebauer *et al.*, 1959]. It has been applied for metals [Tsakalakos *et al.*, 1981], semiconductors, dielectric materials and polymer thin films [Zheng *et al.*, 2000]. In the bulge test, a uniform pressure is applied to one side of a free standing thin film window, causing it to deflect outwards. From this test, stress and strain in the film can de determined from measurements of pressure, the window deflection, the film's thickness and the window dimension. Impulsive stimulated thermal scattering is a time resolved optical spectroscopy method that has been used extensively for characterization of bulk samples, determination of elastic constants and thermal diffusion rates [Wu, 1999; Wu and Liu, 1999]. A modification of this technique allows real-time characterization of acoustic waves propagating on a thin film [Duggal, 1992], determination of elastic moduli, thickness and thermal diffusion rate [Rogers *et al.*, 1994; Cockson *et al.*, 1995, Banet *et al.*, 1998]. X-ray diffraction is used to measure the evolution of residual strain in a metal substrate layer covered by a polymer coating. The method is simple, non destructive and does not require special sample preparation [Nishino *et al.*, 2000]. The bulk modulus of thin films can be measured by the dual capacitor method [Patel *et al.*, 1998; Patel *et al.*, 2000; van

Soestbergen *et al.*, 2006]. The dielectric film is constrained by two parallel aluminium electrodes of which the bottom electrode is bonded onto the substrate. A uniform pressure is applied around the free edges of the capacitor. Due to this pressure the capacitor will be compressed and the thickness of the dielectric film will decrease, causing a measurable change in the capacitance. In this thesis, due to the simplicity of the method, wafer warpage is used to determine the isotropic properties of the thin IC layers.

Using fracture mechanics theory [Gdoutos, 2005] to predict delamination in microelectronics devices involve close interaction between numerical (for the prediction) and experimental (for the determination of adhesion strength values) techniques [Tay and Lin, 1998; Tay *et al.*, 1999; Saitoh *et al.*, 2000; Merril and Ho, 2004; Tay and Ma, 2004]. At present, numerous numerical techniques are available to predict delamination, such as Virtual Crack Closure, J-integral method, Cohesive Zones and the Area Release Energy method. The Virtual Crack Closure Technique (VCCT) can be used to calculate the energy release rate both in 2D and 3D [Bucholz *et al.*, 1998]. Since the critical energy release rate is a function of mode mixity, the components of the energy release rate corresponding to the three basic fracture modes I, II and III can be separately determined. Software codes apply dedicated crack tip elements to calculate these values. Kreuger [2002] used the technique to predict energy release rates for interface cracks at specific positions and with a specified length. The major disadvantages of VCCT is that the crack locations need to be fixed in the model, in other words the exact location of the delamination needs to be a priori known. The same holds for the J-integral method. J-integral methods are widely used in rate-independent quasi-static fracture analysis to characterize the energy release rate associated with crack growth [Cherepanov, 1967; Rice, 1968]. It found worldwide interest and applications in the 1970s, and with increasing capabilities of computers and finite element methods, J-integral based elastic-plastic fracture mechanics became also an option [Wilson and Osias, 1978]. The J-integral method needs a so-called crack-tip mesh. Through a path-independent contour integral, the available energy to delaminate the given interface can be calculated. It is shown that the J-integral is identical with the energy release rate. Big advantage of this method is the relative short calculation time; major disadvantages are identical to the ones for the VCCT method. The cohesive zone method is based on a dedicated element-description for the given interface [Ortiz and Pandolfi, 1999; De Borst, 2003]. As

such, the interface is mimicked by so-called interface elements which properties describe the adhesion between the two materials. Due to this nature, cohesive zone methods require more (material) input, for instance, the (initial) interface stiffness. Dedicated experiments are required to obtain this input. Besides this, when using cohesive zone techniques long calculation times are to be anticipated, especially when many and brittle interfaces are present [Chandra *et al.*, 2002; Tomar *et al.*, 2004]. This is due to the fact that when describing the fracture properly, high mesh densities are needed. Major advantage of this method, besides the fact that it is easy to use (relative to the other techniques), is the ability to predict initiation and propagation of interface delamination. For analysing and comparing different back end structures, a novel failure index, the so-called Area Release Energy (ARE) is recently developed [van Gils *et al.*, 2005; van der Sluis *et al.*, 2006]. This value predicts the change of delamination of critical interfaces without knowing a priori the exact location of the delamination. The amount of energy is calculated that is released upon delamination for any position along a critical interface. The advantage of the ARE method is that it does not require any presupposed position of any initial crack. Instead, at any desired positions within the specimen, an area energy release value is calculated which basically results from releasing an area (having a defined dimension) around each point in the specimen. In this thesis, the numerical techniques for interface delamination mainly focus on the J-integral method.

To determine the interface strength between two materials requires loading of a sample consisting of two material layers in such a manner that the crack growth can be controlled. Numerous techniques exist, such as button shear or pull, four point bending, double cantilever beam, wedge test, modified ball-on-ring and/or mixed mode bending. Button shear or pull tests are part of the common procedure tests within microelectronics [Szeto, 2000; Yuen, 2003]. For example, for measuring the adhesion of moulding compounds on silicon simple pull and shear tests are often performed on small studs made of compound. These traditional adhesion tests have many weaknesses, including poor repeatability; sensitivity to variables that are unrelated to adhesion, or unduly complicated analysis. While such techniques can be useful for making qualitative comparisons of the adhesion in similar material systems, it is difficult to obtain quantitative information about dissimilar systems. The interface strength values obtained are not applicable as input in quantitative simulations. Initially, the four-point bending adhesion test was developed as a method for

characterizing the fracture resistance of bi-material interfaces [Charambalides, 1989]. In a four point bending test, the sample consists of a bi-material sample with an initial notch loaded. The major advantage of this test is the stable crack propagation, which simplifies the determination of the adhesion strength since the crack length does not need to be measured. Recently, the adhesion strength in ICs for low-k materials with its adjacent materials is measured using this technique [Wang *et al.*, 2003b]. Yoa and Qu investigated the interface strength of polymers to a metal frame using the method. They showed that a mechanical term (roughness, 80%) and a chemical binding (20%) term dominate the adhesion between these materials. The Double (or Dual) Cantilever Beam test method is a well-known method for determining mode-I fracture toughness of materials and interfaces. Taweeplengsangsuke and Pearson [1998] and Dai *et al.* [2000] conducted a series of experiments to investigate the adhesion of the underfill-silicon (around $10J/m^2$), underfill-substrate (around $200J/m^2$) and die-attach-copper interfaces (around $400J/m^2$). Samples used are sandwich like specimens where on both ends cantilevers are connected to apply a vertical load. The interface fracture energy can be measured at a mode angle $\psi \sim 4^o$ (nearly mode I) with the double cantilever beam specimen. An alternative version is the Tapered Double Cantilever Beam, which is designed so that, over a large range of values of crack length, the rate of change of compliance with crack length is constant and independent of the value of crack length. In recent years, the Boeing Wedge test has been widely used to evaluate surface treatments under adverse environmental conditions as a means of determining the durability of bonded joints. The test introduces a known tension in an adhesive joint. This fracture test is an ASTM standard (ASTM D 3762) and utilizes a mode I specimen configuration [Dostal, 1990; Xu and Dillard, 2003]. The force is produced by elastic deformation of two adherent plates through the introduction of a wedge. The test consists of creating an initial crack by inserting a wedge and then following the propagation of the crack with time. The driving force for the propagation of crack originates primarily from the stiffness of the beams being separated by the wedge and this driving force decreases as the crack propagates. It is important to notice that in this test the cracked specimen also experiences simultaneous environmental attack at the crack site (when the specimens are placed in that environment). The length of the crack at equilibrium gives both the effective fracture energy and the peel strength of the adhesive assuming no plastic yielding in the specimen. In the modified ball-on-

ring or shaft-loaded-blister test a stainless steel cylindrical shaft with a concave end is attached to the load-cell of a universal-testing machine. The specimen with the hole facing up is put on a ring support so that the path of the shaft will not be obstructed. A steel ball is placed inside the blind hole and the shaft is adjusted to just touch the steel ball. A crosshead speed is set on the universal testing machine. The applied load versus shaft displacement is recorded simultaneously throughout the entire loading process. Tay *et al.* [1999] used this set-up to measure the adhesion in a QFP package between moulding compound and leadframe as a function of temperature and moisture. Their test set-up is different in that sense that the load is placed on the moulding compound instead of on the frame. Using this set-up, Tay *et al.* [1999] measured an interface strength of $4.5J/m^2$ ($\psi = 0^o$) for the leadframe – compound interface. The mixed mode bending test can be regarded as a superposition of the dual cantilever beam test, which is pure mode I, and the end notched flexure test, which is pure mode II. The mixed mode bending test provides stable crack growth over the full range of mode angles [Reeder and Crews, 1990]. Via a lever balance system, the magnitudes of the forces acting on the sample can be changed and, thus the mode mixity can be varied. Merrill and Ho [2004] used a mixed mode loading apparatus to conduct an asymmetric dual cantilever beam test, which exhibits stable crack growth. However, their test apparatus involves a complex loading mechanism, which will cause a substantial amount of anticipated friction. Thijsse et al. [2006] improved their set up and applied it to measure the interface strength between moulding compound and leadframe. An advantage of the mixed mode bending test is that only one type of sample geometry is needed. Off course, the mode mixity should not change during crack growth, as this would complicate the interpretation of experimental data. In this thesis, the experimental techniques for interface delamination mainly focus on the four point bending method.

Hygro-mechanics theory is used to predict the occurrence of moisture-induced failures in microelectronics devices, such as popcorn. First studies on popcorn problems are reported in 1985 by Fukuzawa *et al.* Tay and Lin [1998] conducted a series of work on the moisture diffusion and heat transfer in plastic IC packages, and studied the dynamics of moisture diffusion, hygro-thermal stresses and delamination using an interface fracture mechanics approach. Liu and Mei [1995] also published a series of work on the behaviour of delaminated plastic IC packages subjected to

encapsulation cooling, moisture absorption and wave soldering. Galloway and Miles [1997] made an excellent contribution to the moisture diffusion modelling and characterization for various kinds of plastic materials. Wong *et al.* [1998, 2000] followed Galloway's approach to propose an alternative variable for moisture diffusion modelling. Tee and Zhong [2003] and Tee *et al.* [2004] developed a fully integrated modelling approach to investigate the moisture behaviour during reflow. Dudek *et al.* [2002] presented parametric studies on moisture diffusion to investigate popcorn cracking. Liu *et al.*, [2003] and Fan *et al.* [2004] recently introduced a micromechanics approach to study the moisture behaviour and delamination initiation, and studied the impact of non-uniform moisture distribution on characterising hygroscopic material behaviours of materials. In this thesis, the wetness approach is used for moisture diffusion modelling and measurement results on the diffusivity as function of humidity and temperature conditions as well as hygroscopic swelling values for epoxy materials are presented.

To verify simulation results in microelectronics, different techniques exist to measure package stresses and/or deformations among which are micro-raman, interferometry, digital image speckle correlation and strain gauges. Micro-Raman spectroscopy is used to measure Silicon stress levels [Chen *et al.*, 2000; Chen, *et al.*, 2002]. Important feature of micro-Raman spectroscopy is the fact that the frequency of the Silicon Raman peak depends on the level of mechanical stress. If tensile stress is present, the Silicon Raman frequency will shift downwards, for compressive stress, it will shift upwards. For more complicated stress distributions, the relation between the stress tensor components and the measured Raman shift is not so straightforward, and special modelling is necessary if quantitative stress values are required. Interferometry is mainly used to measure package deformation (warpage). Several techniques exist, such as [Dai *et al.*, 1990; Post *et al.*, 1990; Shield and Kim, 1991]:

- Laser profile Interferometry, using a laser beam that scans the surface of the sample;
- Projection/Shadow Moiré Interferometry, for out-of-plane deformation measurement;
- Twyman/Green Interferometry, for in-plane deformation measurement;
- Holograpic Interferometry;
- Speckle Interferometry or Electronic Speckle Pattern Interferometry.

Basically all above techniques can be used to measure package deformation with different levels of resolutions and/or sensitivity in the order of 0.3-0.5μm/fringe. Digital image speckle correlation is a technique, which correlates a pair of digital speckle patterns obtained at two different loading conditions [Shi *et al.*, 2004]. Next, it searches for the location of any one point within one speckle pattern spreading all over another one speckle pattern, by maximizing the correlation coefficient of the pair of digital speckle patterns, and determines the deformation of the specimen subjected to any loading. Digital image correlation can be used as an experimental tool to characterize properties of electronic materials and verify findings of theoretical and/or numerical models. Other techniques that can be used for this purpose are, for instance, classical strain gauges that are able to measure strain levels at certain locations in microelectronics products. In this thesis, Interferometry measurements are presented to verify the prediction of process-induced warpage of microelectronics devices.

1.4 Virtual Prototyping

Experience-based design and qualification methods cannot lead to competitive products with shorter time-to-market, optimised performance, low costs and guaranteed quality, robustness and reliability. Therefore, there is an urgent need to develop and exploit virtual prototyping methods. There are more and more companies today using increasing levels of simulation or optimisation tools to support physical prototyping and testing for designing and qualifying their products. The engineer starts by defining key design parameters (geometry, materials, process history, etc.) and their design spaces based on application feasibilities and experience. The problem is then modelled and simulated to determine a certain product performance attributor such as stress, damages and failure probability, reliability, durability and dynamic behaviour. If a reliability problem is detected via either modelling or experiment, the design is modified (by changing the design parameters), the corresponding model is modified, and the simulation is run again. With pre-knowledge and proper execution, these simulation supports can be considerably faster, less expensive and able to provide more insights than physical prototyping and subsequent testing. In general, virtual prototyping involves the evaluation of response functions, based on, and integrated with, advanced simulation models and optimisation tools that can predict the product behaviour reliably and efficiently. The ultimate target is to find settings

for a number of design parameters that are optimal with respect to the responses. Since there are many possible design parameter settings and non-linear FE simulations are often time consuming, the crucial question becomes how to find the best possible parameter settings with a minimum number of simulations. Direct optimisation is one technique to obtain optimal parameter settings in such situations [Toropov *et al.*, 1993; van Keulen and Toropov, 1997]. The major disadvantage of direct optimisation approaches is that little insight is obtained in the behaviour of the model in terms of the complete design space. Moreover, when the optimisation problem changes, the optimisation procedure has to be restarted. This thesis uses an optimisation strategy focused on the development of a reliable Response Surface Model (RSM) for the underlying non-linear responses based on an efficient selection of Design Of Experiments (DOE). The DOE method is to answer the question how to design the experiment so it can be done in a minimum number of tests and at the same time deliver enough information. Once the RSM has satisfied the specified accuracy criteria, virtual prototyping can be carried out efficiently.

1.5 Objectives and Approach

In this thesis, the research objectives are set as follows:

- The development of a general virtual thermo-mechanical prototyping framework that is able to predict the non-linear responses in microelectronics devices during manufacturing and testing. This includes:
    - The development of accurate and efficient DOE and RSM methods.
    - The development of accurate and efficient thermo-mechanical prediction models.
- The application of the developed virtual prototyping framework to several reliability problems in microelectronics devices during manufacturing and testing.

To meet the first objective, a general virtual thermo-mechanical prototyping framework is developed; Figure 1.2 shows a schematic representation of the framework, wherein two core building blocks are present:

1. **Simulation-based Optimisation Methods**

   Simulation-based optimisation is optimisation based on and integrated with advanced simulation models that can predict the product and process behaviour accurately and efficiently. Optimisation here refers to different design needs, such as to find the maximum or minimum, to know the parameter sensitivity, to obtain robust design, to develop design rule and to know the probability of failures according to the given derivation of design parameters.

2. **Accurate and Efficient Prediction Models**

   Accurate and efficient prediction models are the other key factors to the success of thermo-mechanical virtual prototyping that can cover the complicated non-linear, multi-physics and stochastic behaviour under given design spaces (material, geometry, process and use conditions), accurately and efficiently. Accuracy is essential, but depending on the application requirements, it can be either qualitative or quantitative. Efficiency is needed due to the fact that it is expensive (if not impossible) to simulate the complicated responses of microelectronics covering the whole design space and whole life cycle, and to conduct global design optimisation, such as finding the maximum or minimum, robust design and parameter sensitivity.

Both above-mentioned factors are seamlessly integrated, in order to predict, qualify, optimise and design microelectronics against the actual requirements prior to major physical prototyping, manufacturing investments and reliability qualification tests, in an effective and efficient manner. This is part of the second objective in which the techniques are applied to various reliability problems in microelectronics. This includes: the occurrence of die crack in power packages; the interaction between IC and packaging processes to obtain the IC package stress design rules; the generation of structural similarity rules for BGA packages in order to reduce reliability testing; and delamination related reliability problems in exposed pad packages. This variety of practical problems demonstrates the applicability of the developed techniques to a wide range of industrial problems in microelectronics.

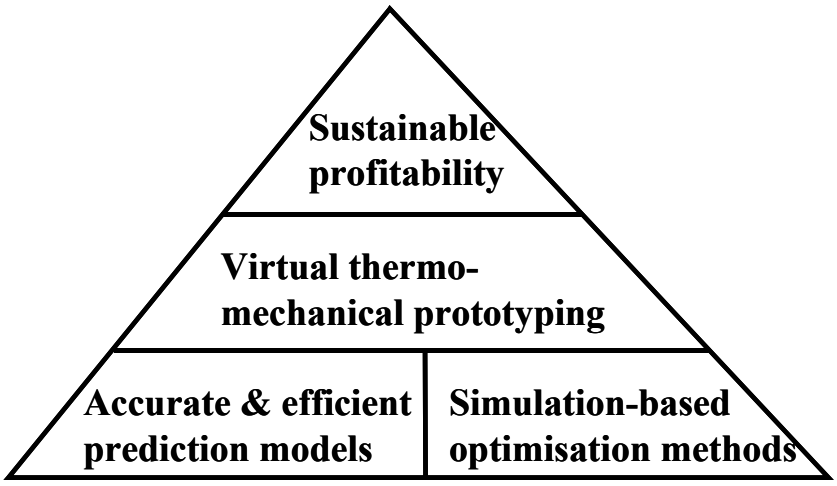


Figure 1.2: General virtual thermo-mechanical prototyping framework.

1.6 Outline of the Thesis

The structure of the thesis is as follows. The thesis consists of 9 chapters. Chapter 2 gives an overview of microelectronics processes as used in IC backend and packaging manufacturing. The manufacturing processes for ICs and packages are briefly discussed. The chapter ends with listing all the testing methods to assess the reliability of microelectronics products and the failure modes found as a result of these tests. Chapter 3 and Chapter 4 further describe the fundaments of the virtual thermo-mechanical prototyping frameworks, as indicated in Figure 1.2. Chapter 3 describes the developed optimisation methods and includes a description of the RSM and DOE

techniques. Chapter 4 describes the numerical and experimental techniques used to obtain accurate and efficient prediction models. Chapters 5, 6, 7 and 8 describe the application of the developed virtual prototyping framework through a series of examples. Finally, the conclusions of the present research work and recommendations for future work are presented in Chapter 6. The outline of the thesis is schematically depicted in Figure 1.3. This scheme may serve as a guideline for the reader. Chapter 3 and 4 contain descriptions of techniques and results that are used in the application Chapters 5, 6, 7 and 8.

It should be noted that all chapters are written on the basis of journal publications and/or contributions to conference proceedings, they can be read independently but may contain some overlap of content.

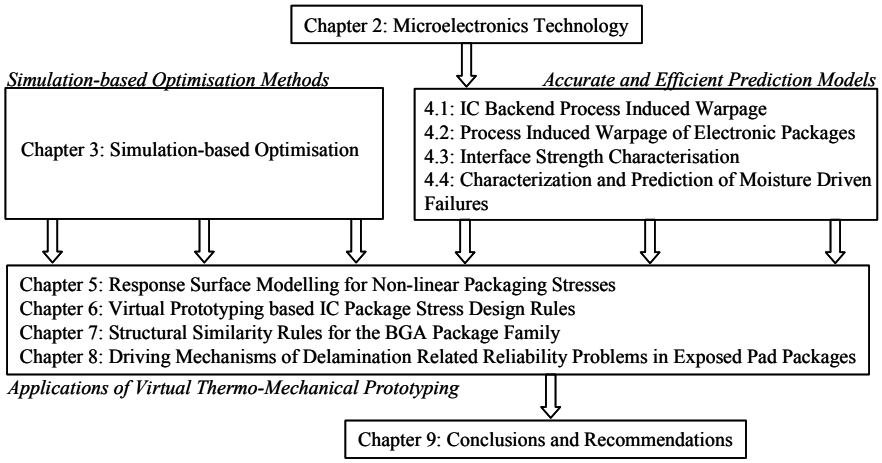


Figure 1.3: Outline of the thesis.

Chapter 2

Microelectronics Technology

The semiconductor industry has seen the continuous development of new and improved processes leading to highly integrated and reliable circuits and packages. From the circuit side, these improvements led to a variety of different technologies to make logic functions, high- and low-voltage transistors, diodes, bipolar transistors and/or field-effect transistor (FET) either made in germanium (Ge) of silicon (Si). From the packaging side, new and cheaper concepts entered the market with better electronic performance; examples are ball grid arrays (BGA), quad flat no lead (QFN) and/or chip scale packages (CSP). This chapter describes the major processes to manufacture electronic devices, with an example for complementary metal oxide semiconductor (CMOS) and leadframe-based packages such as QFP. In the end of this chapter all testing methods are listed to assess the reliability of microelectronics products and the failure modes found as a result of these tests.

2.1 IC Backend Processes

Over 80% of today's microelectronics products depend on CMOS baseline technology, with Moore's Law as guiding light. A basic description of the CMOS device and how it can be made is given here; details about physical design in CMOS technology can be found in [van Zant, 2000]. An IC is a layered stack of substrate and thin films with thicknesses ranging from approximately 100nm to 1μm. For a typical CMOS process these films include semiconductors (as active part), metal interconnects and via plugs (as carrier for current), dielectrics (for electrical isolation) and passivation layers (for mechanical protection). The relatively thick single crystal silicon substrate serves as ground material and as a mechanical carrier during processing. Total IC processing can be divided into 2 serial processes:

1. Frontend process: semiconductors are constructed on the silicon substrate. This is done through so-called doping processes leading to positive (p-type) and negative (n-type) regions in the silicon substrate.

2. Backend process: metal interconnect lines, dielectrics, via plugs and passivation layers are deposited on the frontend wafer. This multi-layered stack of ductile and brittle thin films are deposited by cycles of:

- *Deposition of the thin film material* (and further treatment if necessary). The growth of the number of thin film materials has resulted in a number of deposition techniques. Still, the majority of the films are deposited by a Chemical Vapour Deposition (CVD) technique. Chemicals containing the atoms or molecules required in the final film are mixed and reacted in a deposition chamber to form a vapour. The atoms or molecules deposit on the wafer surface and build up or form a film. During the process the deposited film grows until the required thickness is obtained. Typical process temperature is 400˚C.
- *Lithographically patterning*. Photolithography is one of the most critical operations in semiconductor processing. It is the process that sets the surface dimensions on the various parts of the devices and circuits. The required pattern is formed by using reticles or photomasks and takes place in two steps. First, the pattern on the reticle or mask is transferred into a layer of photoresist. Exposure to light will change the photoresist from a soluble condition to an insoluble one, which enables the formation of the pattern. Typical process temperature is 450˚C.
- *Removal of the photoresist*. The second step in the patterning is the removal of the soluble photoresist material. The chemistry of photoresists is such that they do not dissolve in the chemical etching solutions.
- *Annealing if necessary*. Disruption of crystal structures and/or metal alloying is obtained by a heat treatment between 450-1000°C called annealing.

Figure 2.1 shows a schematic representation of the step-wise photomasking process. Remind that in this case seven steps are indicated to create one metal layer, where current advanced CMOS process may include up to six metal layers.

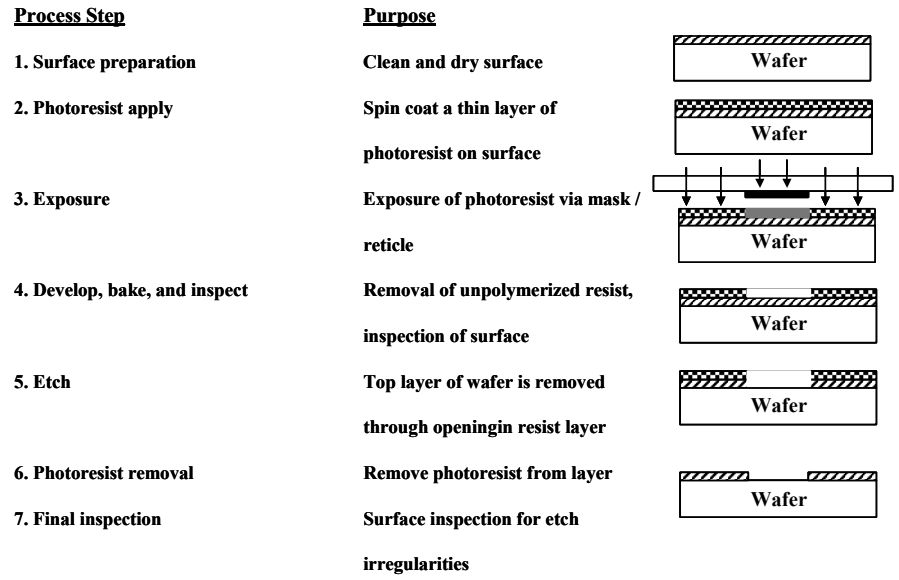


Figure 2.1: Schematic representation of the step-wise photomasking process.

Backend processes are carried out in a waferfab, where continuous monitoring is carried out. Monitoring regularly takes place after each process step, regarding film thickness, warpage of the wafer and interference of moisture and dust. The measured bending of the wafer (warpage) derives a biaxial stress state in a thin film bonded to a thick substrate. During and after the backend process, significant stress levels are observed in ICs. The total stress level in a particular film is considered as the result of two stresses; intrinsic stresses and thermo-mechanical stresses. Intrinsic stresses are induced at the deposition process due to the non-equilibrium microstructure of the film. Subsequently, during cool down from the deposition temperature, thermo-mechanical stresses occur due to thermal mismatch between the different materials. Failures observed during and after backend processes can be attributed to these stress levels. Typical backend related materials are listed in Table 2.1. Figure 2.2 shows a cross-section of a typical IC.

Table 2.1: Typical backend materials.

Application	Material
Substrate	Silicon (Si)
Metal interconnects	Stack of (Ti), TiN, Al(Cu), TiN , Copper (Cu)

Application	Material
Via plugs	Tungsten (W), filled up with Cu / Al
Dielectric	Amorphous Silicon Oxide (SiO_2), TetraEthylOxiSilane (TEOS), Polymers (FPI, FPAE), BoroPhosphosilicate glass (BPSG), Black Diamond BDI / BDII (SiOC:H)
Planarisation	Spin on glass (SOG), Silicon Nitride (Si_3N_4), PhosphoSilicate Glass (PSG), Benzocyclobutene (BCB)

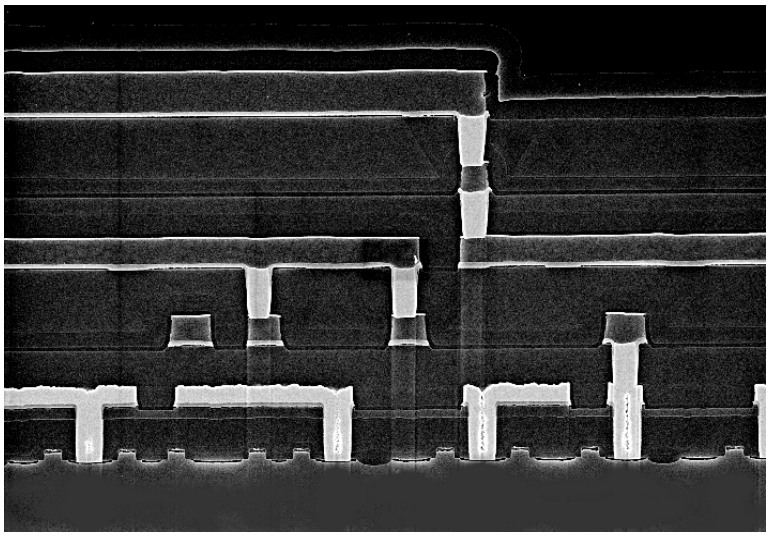


Figure 2.2: Cross-section of a typical IC.

2.2 Packaging Processes

After IC manufacturing in the waferfab, packaging is the next step in the assembly process. Traditionally, the major functions of a package are to allow an IC to be handled for PCB assembly, , for mechanical and chemical protection against the environment, to enhance thermal and electrical properties and to allow standardization (footprints). Like ICs, many different packages exist with different classifications. International organisations like JEDEC (Joint Electron Device Engineering Council), IPC (Institute for Interconnection and Packaging Electronic Circuits), IEC (International Electro technical Commission) allow for standardization of the different

packages developed by the assembly companies. Most used classification is the distinction between:

I. Through Hole Mounted IC Packages

II. Surface Mounted IC Packages

III. Contactless Mounted IC Packages

Packages are manufactured through a series of sequential processes, widely using metals and polymers in various forms such as in leadframes, encapsulants, adhesives, underfills, moulding compounds and coatings [Seraphim *et al.*, 1989; Harper, 1991; Tummula *et al.*, 1997; Lau, 1998a]. For a surface mounted package the manufacturing process involves:

0. *Probing* of each individual IC on the wafer. By means of a probing card, each IC on the wafer is tested, using a so-called probing station, towards the desired electrical function. Only functional ICs will be packaged, this is denoted as the 'Known Good Die' concept.
1. *Grinding*, *Etching* and *Sawing* of the wafer. ICs are cut out of the wafer and can be used for further 'single' processing. This is done at room temperature using a circular sawing or a laser cutting process.
2. *Die-attach*. The single IC is attached on a carrier material, here a metal, by using some kind of glue. Typical process temperature is 150-175˚C and strongly depends on the die-attach type. Many different die-attach types exist; all are related either to their function or either to specific processing demands. For example, die-attach may be thermally and/or electrically conductive (by adding silver flakes), non-bleeding, snap-cured or oven-cured.
3. *Wire bond*. Connections are made between the IC and the carrier by using thin wires. Wire bonding is still the major form of first level interconnection in the world today. At present, over 95% of the manufactured packages (in volume) are wire bonded. Wire bonding technology is changing due to the increasing demands placed on wire bond pad pitch. The techniques that are being used today are wedge bonding and ball bonding. Ultrasonic and thermosonic technologies are used to create contact between the ball and the bondpad and between the stitch and the lead. At present, the majority of wire bonding is done with thermosonic gold ball bonding. The mostly used wire material is gold (Au) but is being replaced (because of material costs) by copper (Cu). Typical process temperature is 200-220˚C.

4. *Chipcoat*. To protect the IC top surface a chipcoat material can be used. Chipcoat is a highly viscous liquid or paste that encapsulates the IC - mostly epoxies or silicones, with some inorganic fillers. Typical process temperature is 150˚C.
5. *Mould*. IC, wires and carrier are encapsulated by an epoxy. Moulding compounds are very complex mixtures of epoxy resin(s), hardener(s), mixture of accelerator(s), (very) high filler loadings, adhesion promoters, release agents, flow additives, carbon black, ion trapping agents, stress absorbers and flame retarders [Bressers *et al.*, 2006]. The chemistry of widely used moulding compounds can be described by a combination of different building blocks with epoxy and hydroxyl reactive groups. Phenol novolac and cresol novolac based resins and hardeners are common, but also newcomers such as biphenyl- and multi-aromatic based precursors and mixtures thereof are being used regarding environmentally green and/or very good performing materials when it comes to 260°C reflow soldering conditions. The moulding compound is injected under high pressure at a process temperature of about 175˚C, followed by a 3 to 4 hours curing step at 175˚C.
6. *Solder plate*. The leads are treated as to obtain a better contact with the Printed Circuit Board (PCB) in later manufacturing stages. Plating is done at room temperature in a plating bath.
7. *Mark*, *Trim and Form*. Package is marked and by a trim and form process redundant material is removed.
8. *Final test*. Package is electronically tested whether it fulfils the aimed function.
9. *Pack*. A number of packages are packed in either tubes, trays, or reels. This is done for reasons of easy transport to the (end-) customer.

Figure 2.3 shows the flowchart of the assembly process for a leadframe based package. Typical packaging related materials are listed in Table 2.2. Figure 2.4 shows pictures of a leadframe, a QFP cross-section and a 3D view of a package.

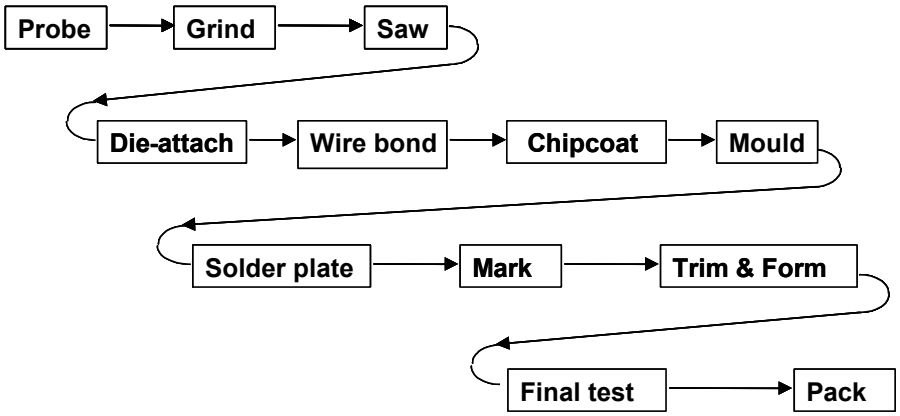


Figure 2.3: Assembly process flowchart for a leadframe based package.

Table 2.2: Typical packaging materials.

Application	**Material**
Leadframe and Heatsink	Copper (Cu), Copper-alloys ($CuNi_3$), Iron ($FeNi_3$)
Substrate (BGA-like)	BT (bismaleimide triazine) based, Flame Retardant Type 4 (woven glass reinforced epoxy resin), Tape, teflon or polyimide based (PTFE, PI), Ceramic
Die-attach	Conductive and non-conductive adhesive, Metal-filled epoxies (thermoset) or polyimide siloxanes, Underfill (silica-filled epoxy resins)
Wire bond	Gold (Au), Copper (Cu), Aluminium (Al)
Compound	Granulated and powdered resin, with hardener, accelerator, fillers, flame retardents and other modifiers
Solder	Lead containing (Pb-5Sn, Pb-10Sn, etc) or Lead free (Sn69.5/Ag3.5, Sn96.3/Ag3.2/Cu0.5, etc)

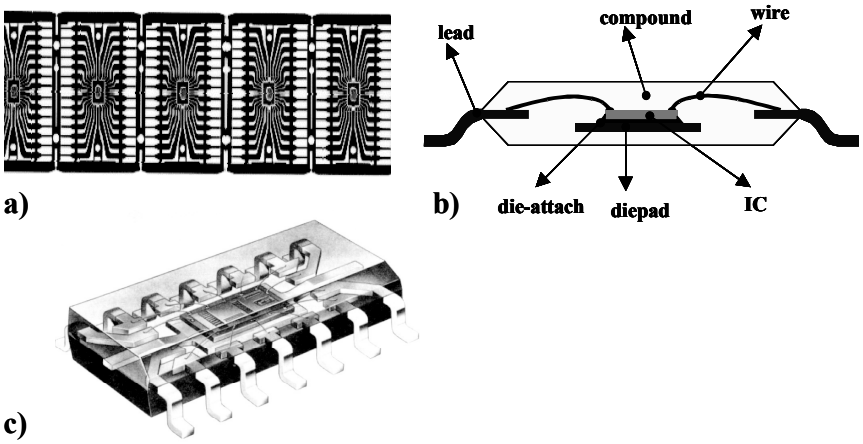


Figure 2.4: Picture of a) leadframe, b) QFP cross-section and c) 3D view of a package.

2.3 Reliability Testing for IC Packages

Reliability is defined as the probability that a product in operation will survive under certain conditions during a certain period of time [Kuper and Fan, 2006]. From this definition it is clear that all products always fail eventually, a probability of zero is physically impossible. Nevertheless, for semiconductor devices, zero is approached quite closely and the probability that a device returns within the guarantee period is typically expressed in failed '*parts per million (ppm)*'. To uncover specific construction, material and/or process related marginalities, semiconductor devices are qualified using specially designed tests to ensure that they have sufficient life so that failures do not occur during the normal usage period. These test are called reliability tests and the specific purpose is to determine the failure distributions, evaluate new designs, components, processes and materials, discover problems with safety, collecting reliability data and to perform reliability control.

Reliability tests are classified in the so-called Qualification System under various names according to the test format, purpose, method of applying stress and other factors. In reliability tests, environmental conditions (temperature, moisture) are extrapolated such as to accelerate the circumstances under which the product could fail. Historically, a number of standard tests have been defined by worldwide consortia like the Joint Electron Device Engineering Council (JEDEC), the Institute for interconnection and Packaging electronic Circuits (IPC) and the International

Electro technical Commission (IEC). Table 2.3 lists typically used test conditions and requirements for currently classified reliability tests.

Table 2.3: Typical reliability tests and their conditions.

Test (abbreviation)	**Typical Condition**	**Typical Requirement**
Preconditioning (PRECON)	Per MSL 1 - 6	Pas level
Temperature Cycling (TMCL)	-65ºC to +150ºC, unbiased	200 or 500 cycles
Pressure Cooker Saturated (PPOT) Unsaturated (UPOT)	 121ºC, 100%RH, unbiased 130ºC, 85%RH, unbiased	 96 hours 96 hours
Temperature Humidity Bias Static / Cycled (THBS/C)	85ºC, 85%RH, biased	1000 hours
Highly Accelerated Stress Test (HAST)	130ºC, 85%RH, biased	96 hours
High Temperature Storage Life (HTSL)	150ºC, biased	1000 hours

Below a short description of the different test methods.

1. *Preconditioning (Precon)*

Moisture preconditioning is required prior to reliability testing for all parts that are surface mounted to boards. It was introduced as a requirement with the release of plastic IC packages because of 'popcorning' during the surface mount reflow process. The popcorn effect results from expanding steam that is evolved during this process. Besides this dramatic effect, moisture is also believed to be hazardous for interface delamination in an IC package. Given the different humidity conditions throughout the world, IC packages will be subjected to moisture during assembly and transport. Preconditioning tests insure that these conditions are met before assessing the reliability. As such, moisture sensitivity levels (MSL) are introduced and for each IC package this level should be deducted. MSL levels are 1 to 6, with 1 being the most severe and 6 being the less severe. MSL levels are obtained via a MSL assessment, which can be coupled with the actual floor life before further assembly on the printed circuit board (PCB). Examples are:

- MSL1: unlimited floor life under a 85%RH and a temperature lower then 30°C. In a MSL assessment, the IC package should withstand experimental conditions of 85%RH/85°C for a period of 168 hours.
- MSL3: limited floor life of 168 hours under a 60%RH and a temperature lower then 30°C. In a MSL assessment, the IC package should withstand experimental conditions of 60%RH/30°C for a period of 168 hours.
- MSL6: limited floor life of 6 hours under a 60%RH and a temperature lower then 30°C. In a MSL assessment, the IC package should withstand experimental conditions of 60%RH/30°C for a period of 6 hours.

2. *Temperature Cycling (TMCL)*

Temperature cycling is used to simulated both ambient and internal temperature changes that result during device power up, operation and ambient storage in controlled and uncontrolled environments. During the test, IC packages are subjected to a typical temperature change from -65°C to 150°C for a number of cycles. Typical numbers of cycles are 200 to 500, and depend on the application. For instance, the demand for IC packages aimed for an automotive application (under the hood of a car the temperature change is large) is higher than those aimed for an end-customer application (for instance a mobile phone).

3. *Combined Pressure, Moisture and Temperature (PPOT, THB, HAST)*

A combination of pressure, moisture and temperature are used to accelerate the penetration of moisture into the IC package. Bias can be applied to even further accelerate the test. The tests are used to identify failure mechanisms internal to the IC package, like metal migration, corrosion, dielectric breakdown, and are destructive for the device.

4. *High Temperature Storage Life (HTSL)*

This test is used to simulate a use environment where a device is continuously powered or stored at high temperature. The IC package is subjected to a temperature of 150°C and will switch on and off continuously. In the test, the operational life is accelerated and the product is qualified if it can sustain 1000 to 2000 hours under these conditions.

As mentioned before, testing conditions are standardized throughout the complete microelectronics industry via international organisations like JEDEC, IPC and IEC. For each developed IC package the tests will be performed to investigate

whether the long-term reliability demands can be met. From virtual prototyping point of view, these tests form part of the loading regime that the IC packages are subjected to.

As a consequence of the reliability test, which mimics the real life operation of the device, failures may occur in the IC packages. Figure 2.5 lists the currently observed failure modes that are thermo-mechanically related. The modes include overstress modes, such as die, package, passivation and substrate crack and fatigue modes, such as broken wires and solder fatigue. For die crack, surface scratching and cracks in dies may form during packaging processes, such as dicing. If an initial flaw equals to or greater than the critical crack size exist, the die can catastrophically fracture in a brittle manner during temperature cycling. Interface delamination between two adjacent materials is one of the major problems in microelectronics. Moisture ingress, either through the bulk epoxy or along the interface can accelerate delamination in plastic IC packages. So-called C-mode Surface Acoustic Microscopy (C-SAM) can be used to identify delamination. From virtual prototyping point of view, these failure modes are to be transformed into allowable stress and strain levels to form the objectives that can be optimised.

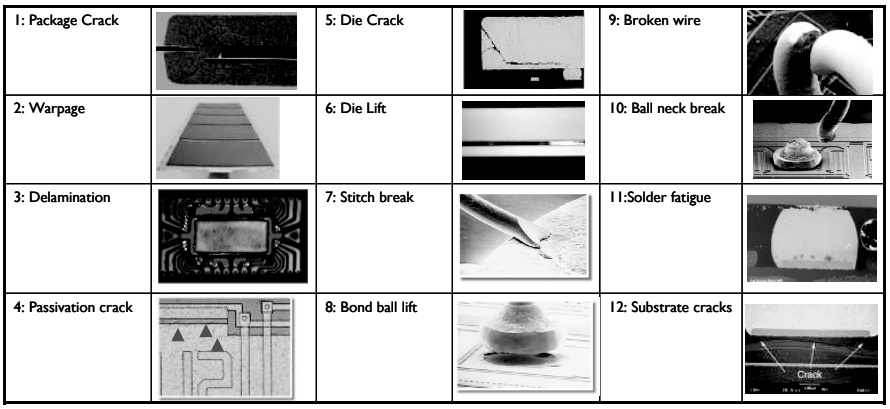


Figure 2.5: Observed thermo-mechanical related failure modes in IC packages.

Chapter 3

Simulation-based Optimisation

Currently, the microelectronics industry is driven by an experience-based design and qualification method that cannot lead to competitive products with shorter time-to-market, optimised performance, low costs and guaranteed quality, robustness and reliability. Therefore, there is an urgent need to develop and exploit virtual prototyping methods. With pre-knowledge and proper execution, these simulation supports can be considerably faster, less expensive and able to provide more insights than physical prototyping and testing. As mentioned in the introduction, the developed virtual thermo-mechanical prototyping framework consists of two building blocks: accurate and efficient prediction models and advanced simulation-based optimisation methods. This chapter describes the developed advanced simulation-based optimisation methods based on the theories and methodologies of simulation-based optimisation, consisting of Design Of Experiments (DOE), Response Surface Models (RSM) and optimisation methods. The chapter contains three sections. The first section describes the developed strategy, methodology and procedures, the second part fundamental DOE, RSM and design optimisation techniques. The final section presents a developed improved approach, called Efficient Global Optimisation (EGO), in which DOE points are automatically chosen in such a way as to provide accurate response surfaces.

3.1 Strategy, Methodology and Procedures

Figure 3.1 shows the methodology and procedure to conduct the simulation-based optimisation. The procedures consist of the following steps:

1. *Problem specification*

The first task is to set up the sequence of analysis that describes the complete simulation - much like setting up the test laboratory apparatus. In this first step, the flow of information from the design factors (which determine the design parameters that the engineer is free to change) to the responses (the design attributors which characterize the product performance) needs to be specified. An important aspect here as well is the communication between the different simulation programs, which can

be any FE code combined with a statistical evaluation code. Once the problem of study is targeted, the next step is to specify the design parameters and their ranges and define the design space. These ranges are bounded by values that can be manufactured.

2. *Sampling the design space*

In this step, one has to select from a number of pre-defined experimental plans to sample the design space. This is similar to generating several physical prototypes and testing them to see how each of them perform. Design of Experiment (DOE) methodologies automatically generates several designs composed of certain combinations of the design parameters. In this thesis, the Latin Hypercube DOE method is used.

3. *Generation of Response Surfaces*

Using a simulation tool, in this case a FE code, for each DOE set, response parameters will be generated, for instance deformations, stress levels at certain critical locations, etc. A Response Surface Model (RSM) approximates the response in a form of a functional relationship between the response and the design space. Remind that the response surface is an approximation, which should be mimicked to certain statistical criteria, such as accuracy. In this thesis, both quadratic and Kriging RSM methods are used.

4. *Selecting the best design*

The selection of the best design among all the alternatives generated in the previous step is achieved through interactive search, visualization and data analysis techniques. This step answers questions such as:

- Which of the design parameters affect the responses the most?
- What amount of change is necessary for each design parameter to achieve the target values for the responses?
- How robust are the responses with respect to the design parameters?
- Which constraints limit the design?

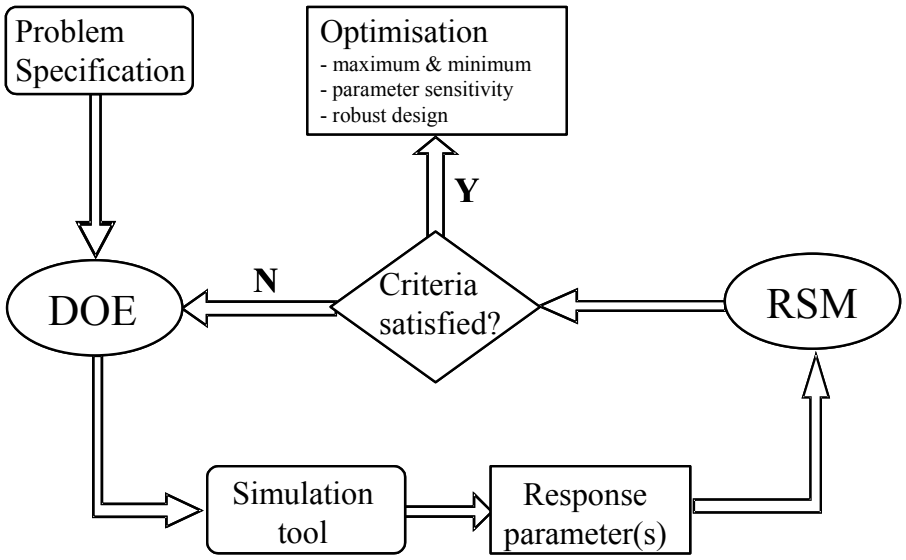


Figure 3.1: Simulation-based optimisation methodology and procedure.

3.2 DOE, RSM and Design Optimisation Techniques

3.2.1 Design of Experiments

The Design of Experiments (DOE) technique is a systematic approach to get the maximum amount of information out of various types of experiments while minimizing the amount of them. Unfortunately, the number of experiments to be done grow exponential with the number of design parameters. Therefore, the basic challenge is to design the optimal DOE, which include experiments that provide appropriate information to the model and skip those experiments that are overlapped or not required [Beauregard *et al.*, 1989; Trocine and Malone, 2000]. Until now, many DOE methods are developed and available for different kind of applications. No attempt will be made here to summarize all of those methods. In principle, DOE methods can be classified in two categories, being orthogonal and random designs.

The most popular and classical DOE schemes are based on orthogonal arrays. Orthogonal indicates that the model parameters are statistically independent; the effect of one factor does not interfere with the estimation of the effect of the other factor. Widely used methods are Taguchi designs, fractional and full factorial designs, central composite designs and Box-Behnken designs. Figure 3.2 gives a schematic representation of some of these designs in case of three design parameters, p_1, p_2 and

p_3. The starting point in such a classic orthogonal DOE design for constructing response surfaces is that experiments are subject to noise. This typically holds for physical experiments. This approach of DOE takes the response surface as a deterministic function of which one can only observe noisy values. To control the effect of the noise, linear of quadratic functions are fitted through the responses to obtain the response surface. As such, model fitting becomes a statistical parameter estimation issue that can be resolved by using regression techniques [Green and Launsby, 1995; Montgomery, 2005]. In order to get more confidence in the eventual response surface, the number of experiments can be increased. In case of orthogonal designs, the number of experiments, *N*, increases exponential with the number of design parameters, *p*:

$$\begin{aligned} N &= 2^p \quad \text{for a 2 level DOE} \\ N &= 3^p \quad \text{for a 3 level DOE} \end{aligned} \tag{3.1}$$

In fact, orthogonal designs can be accepted only for a limited number of design parameters otherwise the number of experiments becomes too large. Besides this, other disadvantages are:

- Initially it is usually not clear which factor is important and which not. Since the underlying function is deterministic there is a potential hazard that some of the initial design points collapse and one or more of the time consuming computer experiments become useless. This is called the collapse problem.
- Most classic DOEs are only applicable for rectangular design regions.

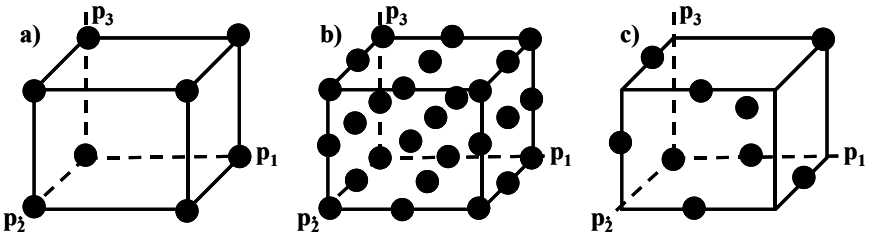


Figure 3.2: Examples of classical orthogonal DOE designs with a) Taguchi; b) full factorial and c) fractional factorial designs in case of three design parameters p_1, p_2 and p_3. Each black dot represents one experiment.

In the case that the DOE is build up by a certain amount of computer simulations and as long as the simulation models are verified and reliable, the concern for experimental noise can be eliminated. In case of numerical experiments it is almost a rule of thumb to use experiments that are:

- Space filling. Space filling indicates that numerical experiments are evenly spread out throughout the design region.
- Non-collapsing. Every experiment gives information about the influence of the other design parameters on the response.
- Sequential. Numerical experiments allow minimizing the required number of experiments by selecting an initial scheme and then carrying out additional experiments in order to improve the accuracy of the response surface.
- Able to handle non-box design regions. In most cases the feasible design region is non-box as points outside this region may have no physical interpretation.

Another widely used DOE technique is a random DOE. The most common-used random DOE is the so-called Latin Hypercube design (LH) and is mostly applied when using numerical experiments [Olsson *et al.*, 2003]. A LH design can be constructed as follows. Let p be the number of design parameters and n is the number of runs that we are willing to simulate. Latin Hypercube provides an array that randomly samples the entire design space broken down into n^p equal-probability regions. The design is obtained to select for each dimension a permutation of the levels and combine these. In this way each level is present in the design and the number of levels is maximized. LH designs do not suffer from the collapse problem, because if one or more of the parameters appear not to be important, every point in the design still gives information about the influence of the other parameters on the response. In this way none of the time-consuming numerical experiments become useless. There is still complete freedom in assigning levels to dimensions and therefore numerous LH designs exist. Assigning levels can for instance be done randomly. An efficient way to construct a LH design is to assign the levels in such a way that the resulting design is space filling. Intuitively, a design is space filling if the points are spread out and do not cluster in one portion of the experimental region. As a measure for the space-fillingness of a design we take the minimal distance between two of its design points. The larger this minimal distance is, the better the design. A design for which the minimal distance is maximal is called a maximum distance

design. The required number of experiments for a LH design is determined by the complexity of the underlying model (linear, non-linear, continuous or discontinuous). Figure 3.3 gives a schematic representation of a LH design in case of two design parameters, p_1 and p_2.

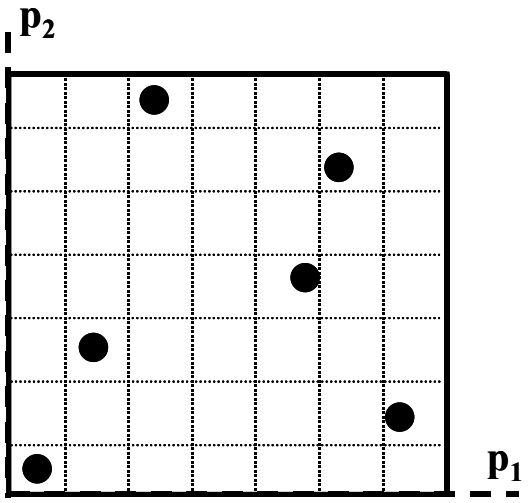


Figure 3.3: Example of a random LH design in case of two design parameters p_1 and p_2. Each black dot represents one experiment.

3.2.2 Response Surface Models

A Response Surface Model (RSM) is a collection of mathematical and statistical techniques used for the modelling and analysis of problems in which a response of interest is influenced by several variables. Using the DOE method combined with the response surface method, the response between the points set up by the design, can be predicted efficiently [Greenwood *et al.*, 1998]. The RSM methodology allows for further processing of the DOE results, examples are optimisation and robust design. Using RSM technologies not only time-consuming and costly simulation runs can be reduced, but also the inherent trend (often non-linear) can be predicted. When utilizing RSM techniques for optimisation one has to always be cautious and take explicit actions relating to the RSM quality. There are three major categories of RSM methods, namely RSM based on least squares approximations, RSM based on stochastic interpolating methods and RSM based on neural network methods [Box *et al.*, 1987; Myers *et al.*, 1989; Meyers and Montgomery, 1995; Khuri and Cornell,

1996; Meyers 1999]. In this thesis, the least squares based RSM methodology and the stochastic interpolating Kriging based method are used.

Given a set of observations, one often wants to condense and summarize the data by fitting it to a model that depends on adjustable parameters. The basic relation between a given set of input design parameters X and measured and/or simulated output variables Y can be described as:

$$Y = f(X, Z) \tag{3.2}$$

Where $X = (x_1, \ldots, x_i)$, $Y = (y_1, \ldots, y_i)$ and Z reflects the unknown or uncontrollable variables, such as noise. In case of physical experiments this noise cannot be neglected and approximation RSM techniques are most common response surface functions to use. Polynomials are mainly used because of simplicity. Examples are linear and quadratic functions, described as:

$$y = \alpha_0 + \sum_{i=1}^{k} \alpha_i x_i \quad \text{for linear functions}$$
$$y = \alpha_0 + \sum_{i=1}^{k} \alpha_i x_i + \sum_{i=1}^{k} \alpha_{ii} x_i^2 + \sum_{i=1}^{k-1} \sum_{j=i+1}^{k} \alpha_{ij} x_i x_j \quad \text{for quadratic functions} \tag{3.3}$$

Where $\alpha = (\alpha_0, \ldots, \alpha_{ij})$ are a set of adjustable parameters. The general method of least square is to figure out the parameters α in the model, so that the sum of squares of the error takes out a minimum, that is:

$$\min_{\alpha} \sum_{i=1}^{k} \left[y_i - y(x_i; \alpha) \right]^2 \tag{3.4}$$

Other approximation functions that can be used are higher order polynomials and spline functions. The basic approach becomes like this: choose or design a function that measures the agreement between the data and the model with a particular choice of parameters. The parameters of the model are then adjusted to achieve a minimum in the function, yielding best-fit parameters. Employ the linear least squares method using the sum of squares of the error between the approximated value and the exact observation, which one can show is a maximum likelihood estimator.

Numerical experiments tend to give the same results when an experiment is repeated and stochastic interpolating RSM techniques are the most common response surface functions to use [Sacks *et al.*, 1989; Ghiocel, 2002]. The stochastic technique

is based on considering the deterministic response *y(X)* as a realization of a stochastic process, which means that an error is replaced by a random process. One of the most popular methods for such a stochastic model interpolation is Kriging. Kriging is extremely flexible due to the wide range of correlation functions that may be chosen. Depending on the choice of a correlation function, Kriging can either result in exact interpolation of the data points or smooth interpolation, providing an inexact interpolation. It is worth noticing that Kriging is different than fitting splines and in fact it is believed even better than splines. Numerical analysis is deterministic and not subjected to a measurement error. Therefore the usual uncertainty derived from least squares residuals has no meaning. Because of this the response model can be treated as a combination of a polynomial model and an additional factor referring to the deviation from the assumed model. The most straightforward way to fit a response to a data is by linear regression (approximation of the sampled data):

$$y = \sum_{i=1}^{k} \alpha_i f_i(x_i) + \varepsilon(x_i) \qquad (\mathbf{3.5})$$

Where $f(x_i)$ can be a linear or non-linear function, α are the unknown coefficients to be estimated and finally $\varepsilon(x_i)$ are error terms of the systematic deviation with a normal distribution. In this way we can get an interpolation of the sampled data. The function $\varepsilon(x_i)$ represents the realization of a stochastic process and is assumed to have zero mean and the covariance V between two inputs u and v is given by:

$$V(u,v) = \sigma^2 R(u,v) \qquad (\mathbf{3.6})$$

Between $\varepsilon(u)$ and $\varepsilon(v)$ where σ^2 is the process variance and $R(u,v)$ is a correlation. The covariance structure of ε relates to the smoothness of the approximating surface. For a smooth response, a covariance function with some derivates might be adequate, whereas an irregular response might call for a function with no derivates. The fitting procedure can be viewed as a two-stage problem:

- Calculation of the generalized least-squares predictor.
- Interpolation of the residuals at the design points as if there were no regression.

Because computer simulation is deterministic by nature, the error is totally due to modelling error and not to e.g. measurement error, and then it is justified to treat the error ε_i as a continuous function of x_i. As the error is a continuous function then the errors could be considered as correlated by the distance function between the

points. If the points are close together, then the errors should also be similar, which means high correlation. Following this approach it can be assumed that the correlation between errors would be related to the distance between the corresponding points. A special weighted distance formula can be used, which in comparison to the Euclidean distance does not weight all the variables equally:

$$d(x_i, x_j) = \sum_{h=1}^{k} \Theta \left| x_i^h - x_j^h \right|^{p_h} \qquad (\mathbf{3.7})$$

Where $\Theta \geq 0$ and $p_h \in [1,2]$. Using this distance function, the correlation between the errors can be defined as follows:

$$r_{ij} = corr\left[\varepsilon(x_i), \varepsilon(x_j)\right] = e^{-d(x_i, x_j)} \qquad (\mathbf{3.8})$$

The so defined correlation function has obvious properties, which means that in case of small distance the correlation is high while in case of large distance the correlation will approach zero. The values of the correlation function r_{ij} define the correlation matrix R and it is possible to get a simple linear regression model and avoid a quite complicated functional form of the response. The functional form of the stochastic interpolating Kriging technique can be written as:

$$f(x_1, ...x_k) = \mu + \sum_{i=1}^{k} \delta_i \cdot exp(\sum_{j=1}^{k} - \theta_j \cdot | x_j - x_{ij} |^{p_j}) \qquad (\mathbf{3.9})$$

It is required to estimate 2k+2 parameters to define the Kriging model: μ, $\delta_1, \ldots, \delta_k$, $\theta_1, \ldots, \theta_k$, $p_1, \ldots, p_k$. This task can be achieved by maximizing the likelihood function F of the sample, which is defined as follows:

$$F = \frac{1}{(2\pi)^{n/2} (\delta^2)^{n/2} |R|^{1/2}} \frac{1}{e^{\frac{(y-1\mu)' R^{-1} (y-1\mu)}{2\delta^2}}} \qquad (\mathbf{3.10})$$

Where 1 denotes the n-vector of ones and y denotes the n-vector of observed function values. One of the most crucial factors of the Kriging method is the estimation of the θ parameter.

3.2.3 Design Optimisation, Robust Design and Parameter Sensitivity

Design optimisation deals with the selection of the "best" alternative amongst the many possible designs [Schwefel, 1981; Gill *et al.*, 1981; Rao, 1996; Edwards and Jutan, 1997; Papalambros and Wilde, 2000]. It involves the:

- Selection of a set of variables to describe the design alternatives.
- Selection of one or more objectives, expressed in terms of the design variables, which we seek to optimise.
- Determination of a set of constraints, expressed in terms of the design variables, which must be satisfied by any acceptable design.
- Determination of a set of values for the design variables that optimise the objective(s), while satisfying all the constraints.

In mathematical terms, design optimisation is to minimize the set of functions describing the relation between design parameters and output variables under the above constraints, described as:

$$\min_{x \in \Re^n} \vec{f}(x) = (f_1(x), ..., f_k(x))^t \qquad (\mathbf{3.11})$$

Note that the above functions (objectives and constraints) can be linear or non-linear, continuous or non-continuous and include continuous and discrete design variables. There are two major classes of solution methodologies that solve general optimisation problems, being local and global optimisation methods.

Local optimisation methods assume continuity and unique optimal solutions. In solving optimisation problems with the aim of finding a local optimum, gradient-based numerical iterative methods can be deployed. A number of methodologies exist, utilizing first order derivatives of the objective and constraint functions in order to iteratively progress towards the optimum. Two of the well-known and established methodologies are the Sequential Quadratic Programming method and the Generalized Reduced Gradient methodologies [Powell, 1978; Papalambros and Wilde, 2000]. There exist a number of other methods like for instance the Moving Asymptotes method [Svanberg, 1987].

Global optimisation methods address discontinuities of the design space as well as the possibility of multiple optimal solutions. Single objective optimisation problems are usually addressed with single objective optimisation methodologies,

while multiple objective optimisation problems are addressed with multi-objective optimisation methodologies that produce the so-called Pareto set [Toropov, 1992; Toropov *et al.*, 1993; van Keulen and Toropov, 1997; Smith *et al.*, 1999]. In many numerical and/or experimental situations, a number of responses are measured. The goal of the multi-response analysis would be to find out the optimal solution due to a few responses. Multi-objective optimisation algorithms allow performing optimisations taking into account multiple objectives at the same time. There exist a number of numerical methods to find global optima, such as Self Adoptive Evolution, Normal Boundary Intersection method, Weighted Objective method, Weighted Tchebycheff method, the majority of them are based on response surface approximations [Gill *et al.*, 1981; Schwefel 1981; Meyers and Montgomery, 1995; Roa, 1996; Edwards and Jutan, 1997].

Besides design optimisation to find the optimal parameter values in a sense of the expected output, whether maximum or minimum, design selection should also include additionally stages as robust design and parameter sensitivity [Benjamin *et al.*, 1995; Khattree, 1996; Li and Chen, 2001]. Given a product or a process with a selected response, then its value will differ from product to product or along timescale due to noises, variations in operation conditions, random distributions of geometrical dimensions or material properties and variations in material or process parameters.

In an industrial environment one is to choose that product and process combination that will lead to the highest yield, defined as the % of products operating at the required functionality. Taking into account all the above, the selected combination can be described by a random distribution with an average and variance response. As long as its average is close to the expected one and the variance is low, the yield will be high. Additional to that, parameter tolerances and/or sensitivities should arrive at acceptable levels. The most straightforward numerical approach to solve a yield problem is by performing a number of simulations with randomly selected parameter combinations for the given distribution, and to verify for each combination if this results in a failure. One then divides the number of failures by the number of simulations, which yields an approximation of the actual failure probability. This is the standard Monte Carlo simulation approach. Improvements of the standard approach are the so-called Importance Sampling method, the general idea is to place more samples in the failure range of the parameter space. Examples are

Importance Sampling Monte Carlo and the Transformed Importance Latin Hypercube Sampling methods.

In summary, optimisation-based simulation includes the following topics:

Design Optimisation: the objective is to find the operating conditions or factor levels X that would optimise the system response y. The common problem of the optimisation is how to distinguish the local optimum from the global one.

Robust Design: The aim is to make a product or process less sensitive (more robust) in the face of variation over which we have little or no control. The robust design can be based on the Monte Carlo approach.

Parameters Sensitivity: A parameter sensitivity analysis can be performed if the robust design is not enough. The goal is to tighten up the tolerances of the input parameters so as the response can be set up in the acceptable range.

3.3 Efficient Global Optimisation (EGO)

A major drawback of the methodology and procedure to conduct the simulation-based optimisation as described previously is the inability to automate the selection of DOE points to obtain an accurate RSM. In the previous procedure, a criteria step is manually performed after the generation of the RSM, see Figure 3.1. The Efficient Global Optimisation (EGO) approach aims at a procedure in which DOE points are automatically chosen in such a way as to provide accurate response surfaces. As such, EGO allows for saving the total number of required DOEs in order to achieve a reliable RSM. The EGO approach is based on fitting response surface models (Kriging Response Surface, for example) to data collected by evaluating the objective and constraint functions at a few points. These response surfaces are then used to visualize input-output relationships, estimate the location of the optimum and suggest points where additional function evaluations may help improve this estimate.

Sequential RSM optimisation methods were introduced mainly in reference to computer-aided design of experiments [Schagen, 1984; Sacks *et al.*, 1998; Jones *et al.*, 1998; Wang and Dong, 2000]. The main idea of sequential methods is to find a good fitting curve to the optimum of an unknown function of several variables in a minimum number of function evaluations. This can be achieved by sequential exploring the domain of interest. Next to that, the sequential approach aims to improve the accuracy of the response surface by adding additional one at a time DOE points to the experiment. As such, the method is based on a two-step approach:

- Initial experiments based on a space filing DOE scheme, e.g. LH.
- Iteratively adding experiments based on interpolation error estimation, e.g. Kriging.

At the first stage an initial number of experiments is selected using a Latin Hypercube design. Next, additional experiments are added, to improve the model accuracy. At each stage an interpolating function, derived from a stochastic RSM model (Kriging), is set up, and this is used to determine the location of the next evaluation. This process continues until agreement is reached between the optimum interpolating function value and the true value of the objective function. A balance between exploring unknown regions and optimising the function in known regions is struck by means of a weighting factor, which varies as new data are accumulated. A measure of the interpolating error estimation is the so-called Expected Improvement (EI):

$$EI(\mathbf{x}) = (f_{\min} - \hat{y})\Phi\left(\frac{f_{\min} - \hat{y}}{\hat{s}}\right) + \hat{s}\varphi\left(\frac{f_{\min} - \hat{y}}{\hat{s}}\right) \qquad (\mathbf{3.12})$$

A combination of the EI and the global search for the optimum is obtained by adding a term in the objective function that introduces the standard deviation of the design variable space:

$$f(x) - n \cdot \sigma(x) \qquad (\mathbf{3.13})$$

A large value of n will guide the EGO algorithm to add points in a wider region within the design space, while a value closer to zero will make the algorithm behave more as a local optimisation methodology. Points are added then accordingly. Depending on convergence the algorithm continues by calculating a new Kriging model and calculating the new EI measure. Termination is reached upon determination of the optimum point, or upon reaching an acceptable value for the EI. The EI method is schematically shown in Figure 3.4.

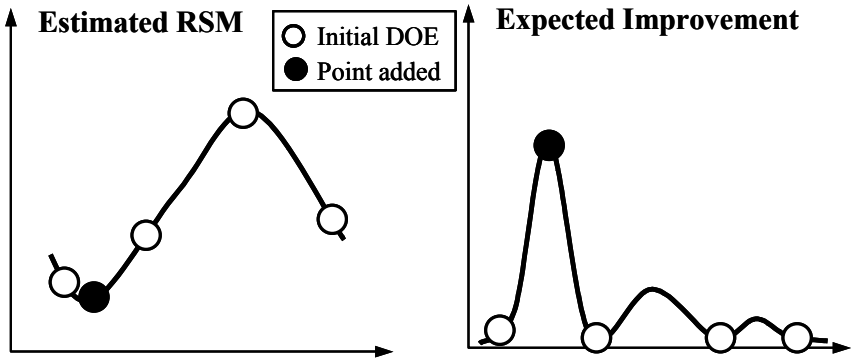


Figure 3.4: Principle of the Expected Improvement method.

The main problem in the EGO approach remains the choice of the initial DOE scheme. If the number of initial experiments is to large, then more function evaluations will be carried out than are required, if it is too small, then the exploration will be insufficient and possible optimum locations may be overlooked. Obviously, the number of data points needed to "explore" the design space domain effectively depends on a structure of the function, which is not known a priori. Data points are inserted into the region of interest one at a time and the parameters of the interpolating function are constantly updated. In the early stage, a new point is positioned as far as possible away from all existing points. In the later stages, new points tend to concentrate around optimum values of the interpolating function. The balance between these criteria is defined by means of a weighting factor, which depends not only on the current number of data points but also on the apparent structure of the objective function. The main advantage of the sequential approach is that it embeds the choice of the DOE with the optimization process. It is demonstrated that by using theoretical known functions, the EGO approach needs about 50% less DOE points to obtain the same level of RSM accuracy [Knowles, 2006].

The full process flow of the EGO approach is given Figure 3.5 and consists of the following steps:

1. *Problem specification*

This task is identical to those previously described.

2. *Sampling the design space*

The design space is sampled by using a Modified Latin Hypercube (MLH) DOE. The MLH is based on the standard LH design but includes prior knowledge of an expert

on the domain behaviour. In most of the engineer cases it is a priori known that certain points are more valuable than others, especially from the expert point of view. In the MLH approach, points or sub-domains can be added in regions where high non-linearity is expected, include the points close to the domain border, or exclude sub-domains that seem to be less essential in the response analysis. In the created sub-domains, a LH DOE scheme is generated.

3. *Generation of a interpolating RSM*

An interpolating or approximating response surface (Kriging) is fitted through the response data, as described previously.

4. *Adding additional DOE points based on the Expected Improvement*

By sequentially adding additional DOE points basing on the estimation of the interpolation error, or Expected Improvement, the quality of the response surface is improved until certain pre-defined criteria are met.

5. *Selecting the best design*

Once the response surface is reliable enough, one can run analysis such as optimisation for minimum or maximum, parameter sensitivity and/or robust design.

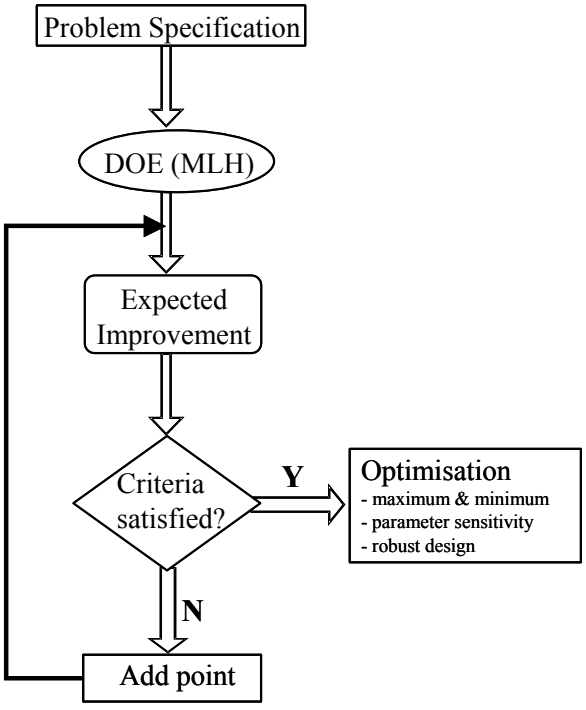


Figure 3.5: EGO algorithm flowchart.

Chapter 4

Accurate and Efficient Prediction Models

The second precondition for executing virtual prototyping are 'accurate and efficient reliability prediction models'. Of course, the success of virtual prototyping depends also on many other factors, such as the proper specifications of accuracy for the developed response surfaces. Accuracy should be specified properly and in an integrated way to achieve optimal balance between the desired design accuracy on one hand and the resulting efficiency on the other hand. Accurate and efficient reliability prediction models contains a wide research field, composed of factors indicated in Figure 4.1, such as:

1. *Product and Process Inputs*

It is essential to have reliable inputs, namely the parameters defining the product design and process settings, in order to establish accurate and efficient thermo-mechanical prediction models. There are two types of these inputs. The first type is the design variables or design freedoms. By choosing different values of the selected design variables, design engineers can change and influence the performance of the products. For all these design variables, one needs not only the nominal design value, very often, also the allowed range of variation - the so-called design space. The second type is the inherited deviation of some design variables. They are so-called deviation parameters corresponding to some fixed value of design parameters. Compared with design variables, deviation parameters are usually probabilistic in nature. Still one can classify the causes of variation into two categories: random (chance) causes and assignable causes that can be identified and corrected. For all the materials used in microelectronics, their properties are all probabilistic in nature, depending on not only the material batch itself, but also the process windows. Product and process inputs determine the product design, actual loading and loading history, boundary conditions, damage initiation and evolution, material behaviour and eventually the life time and performance of the final product. However, the acquisition of reliable design variables and deviation parameters is not a trivial task. Especially, it is technically difficult, time and money consuming to extract the probabilistic data via in-situ measurements and observations. Due to business pressure

it is often neglected or over-simplified by industries. Therefore, sufficient effort should be spent on acquiring accurate design inputs, to be able to obtain reliable predictive thermo-mechanical models.

2. *Material and Damage Models*

For new product development of microelectronics, especially associated with new technologies, new materials and new product concepts, industries would like to know upfront the probability of failures and the associated failure modes and mechanisms, before building and testing multiple physical prototypes, so that the first-time-right design can be achieved. Failure inputs herein refer to the failure modes and their ranking, failure evolution (the history from damage initiation to actual failure), failure location, failure root causes/mechanisms, their interactions and failure probabilistics. Knowing failure inputs is of paramount importance for predictive modelling of microelectronics. Failure prediction cannot be realized without the pre-knowledge of failure criteria and dedicated damage models. Developing failure criteria and damage models is time consuming and therefore a specialist work. Since many materials used in microelectronics are usually time, geometric scale and processes dependent, it adds extra difficulties to obtain quantitatively accurate failure criteria and damage models. Reliable models describing the time, process and size dependent behaviour (properties, damage initiation, evolution and failure criteria) of materials and their interfaces are essential for not only predictive modelling, but also for material development, material pre-selection and process optimisation. The characterization and modelling of material behaviour are based on constitutive and damage models that describe the material properties and their failures. Quantitatively accurate material and damage models are needed for accurate failure predictions in microelectronics devices.

3. *Experimental and Computational Methods*

Experiments play an important role in the content of virtual prototyping. First, they are needed in characterizing material and their interface behaviour. Secondly, very often, the correctness and accuracy of the developed prediction models need to be verified via experiments for the whole range of the design spaces, and by covering all the critical processes. Three types of experiments are widely used in supporting thermo-mechanical modelling of microelectronics, namely, experiments for material and interface characterization to provide data for constitutive modelling, experiments for damage and failure criteria extraction to provide quantitative data on the allowable

strengths and experiments for model verification to validate the correctness and accuracy of the developed models. Computational methods need to be developed for the applications and needs of microelectronics, such as both multi-physics and multi-scale techniques. It includes the development of efficient and robust algorithms and solvers. A proper numerical integration scheme should be both numerically stable and computationally efficient. For sure, virtual prototyping cannot be efficiently conducted without efficient and robust algorithms and solvers.

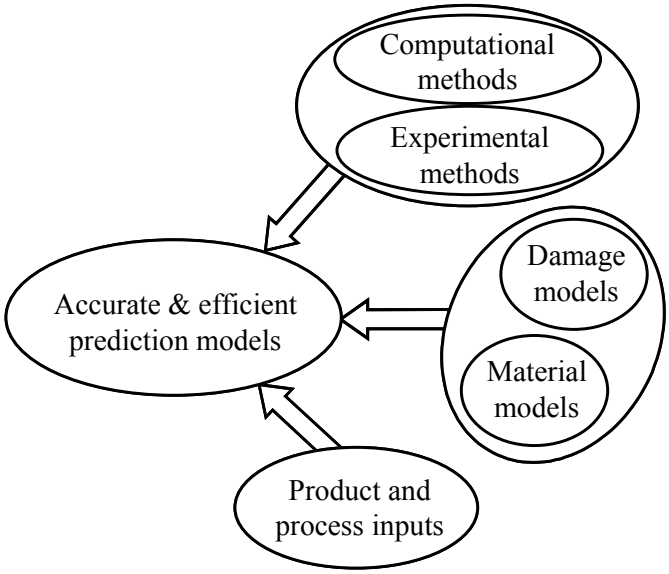


Figure 4.1: Factors determining the accuracy and efficiency of prediction models.

This chapter describes the results of numerical and experimental techniques used to obtain accurate and efficient prediction models for the microelectronics applications presented in Chapters 5, 6, 7 and 8. `The chapter consists of four sections. The first section describes the experimental characterization to determine isotropic properties for thin IC films and the effort to obtain accurate prediction models for IC backend processes. The second section presents such effort on the packaging level. The third section describes the characterization of interface strength using the four point bending technique. The fourth section describes the characterization and prediction of microelectronics materials under moisture conditions.

4.1 IC Backend Process Induced Warpage

The total mechanical stress σ_{total} in a brittle film without plasticity deposited on a Si-substrate consists of two components, the thermal stress $\sigma_{thermal}$ and the intrinsic stress $\sigma_{intrinsic}$:

$$\sigma_{total} = \sigma_{thermal} + \sigma_{intrinsic} \tag{4.1}$$

The thermal stress is due to the difference in coefficient of thermal expansion (CTE) between the film and the substrate. During cool down from deposition temperature to room temperature the thermal stress develops according to the material properties of the film and the substrate. A simple expression for the (maximum) thermal stress is given by:

$$\sigma_{thermal} = \frac{E_f}{1-\upsilon_f}(\alpha_s - \alpha_f)\Delta T \tag{4.2}$$

where α_f and α_s are the CTE of the film and substrate, respectively. E_f and ν_f are the Young's modulus and Poisson ratio of the film and ΔT is the temperature difference between deposition temperature and the temperature of interest. The total stresses in the film σ_{total} are calculated using the warpage R of the processed wafers measured at room temperature. Assuming that the film is thin compared to the thickness of the wafer the total film stress can be calculated using the modified Stoney's equation [Stoney, 1909]:

$$\sigma_{total} = \frac{E_s}{6(1-\upsilon_s)}\frac{t_s^2}{t_f}\left(\frac{1}{R_2} - \frac{1}{R_1}\right) \tag{4.3}$$

With E_s and ν_s the Young's modulus and Poisson ratio of the substrate, respectively, t_s the substrate thickness and t_f the film thickness. R_2 is the radius of curvature after processing and R_1 the initial radius of curvature of the wafer before film deposition. For thickness ratios $t_f/t_s < 0.1$, the error in Stoney's equation remains below 5%. For thicker films, a more rigorous analysis shows that a correction factor equal to $(1+\gamma\delta^3)/(1+\delta)$ is required [Klein, 2000], where $\delta = t_f/t_s$ and $\gamma = M_f/M_s$, with the biaxial modulus: $M=E/(1-\nu)$. For thick films ($0.1< \delta < 0.4$) with unknown film properties, the film modulus contribution can be neglected and $1/(1+\delta)$ can be used as a correction factor [Atkinson, 1995]. Others presented a correction factor, which includes the

effects of a finite film thickness and film modulus as well as the effect of a large deflection [Freund *et al.*, 1999].

Intrinsic stresses are the result of the depositioning process of the layer. These intrinsic stresses are already present at depositioning temperature and are influenced by the parameters of the depositioning process. The intrinsic stresses remain constant with changing temperatures if the properties of the film are not influenced by the temperature (for example viscous flow at high temperatures) or the environment (influence of humidity). The intrinsic stresses are believed to depend on the thickness of the film. For thin films (<300 nm) an increase of intrinsic stresses is observed where above this level the intrinsic stresses are constant with thickness. This influence of thickness is the result of nucleation phenomena of the film on the substrate. The intrinsic stresses can play a significant role and for some type of films the intrinsic stresses are comparable or even larger than the thermal stresses. Modern equipment allows control over the intrinsic stress, which gives the process technicians a method of controlling the overall warpage of the wafer at room temperature. It is important that the intrinsic stress is accounted for in FE simulations. Measuring the intrinsic stresses is difficult due to the fact that the measured total stress is usually a combination of thermal and intrinsic stresses. Intrinsic stresses can be both tensile and compressive. There are several mechanisms for forming intrinsic stresses, such as [Stadtmueller, 1992]:

- Density of film-building atoms in absorbed state,
- Absorption of by-products,
- Increased surface mobility of reactive species,
- Ion bombardment,
- Cross-linking.

For siliconoxide (SiO_2) based layers the intrinsic stress is not a constant value. The as-deposited intrinsic stress is influenced by several factors, which can play a large factor in the total stresses in the SiO_2 based layer. For oxynitride, metal or ceramic layers this effect is usually not present. The different factors, which influence this change in intrinsic stresses, are absorption of water in the layer, densification of the layer due to temperature increase and/or visco-elastic relaxation of the stresses at temperatures above the softening point. CVD deposited phosphosilicate glass (PSG) films subjected to humidity will absorb the water atoms and swell in the process. This

will decrease the tensile stress and eventually lead to compressive intrinsic stresses. PSG films with lower intrinsic stresses will show less reactivity with water [Wu and Rosler, 1992]. For SiO_2 based films increasing the temperature causes the formation of additional Si-O-Si bonds. This leads to densification of the film and the development of bond strains. These bond strains result in intrinsic tensile stresses in the film. After cooling to room temperature these tensile stresses do not disappear but remain in the film. The result of this phenomenon is the occurrence of hysteresis during thermal cycling of the film. This thermal cycling plays a role in practice due to the deposition of additional films [Ramkumar and Saxena, 1992]. SiO_2 based films are usually amorphous, glass type structures which exhibit a time-dependent, visco-elastic behaviour. For temperatures above the softening point of the material the viscosity of the material will be low enough for the occurrence of flow phenomena and rearrangement of molecules. The temperature of the softening point will depend on the chemical composition of the layer. For pure SiO_2 films this temperature will be higher than for SiO_2 films with impurities (such as PSG). The complete stress behaviour during a temperature cycle to high temperatures shows initially the development of tensile stresses due to the densification. At higher temperatures these stresses will relax and decrease to zero.

4.1.1 Characterization of Thin Films

Measuring the warpage of processed wafers at room temperature is a regular method and provides a value for the total stresses in the layer. This value is the sum of the thermal and intrinsic stresses and is used by process technicians as a controlling parameter for the depositioning process. By measuring the warpage as function of temperature the intrinsic stress levels can be obtained, since at deposition temperature no thermal stresses exist and the warpage at this temperature is a direct result of the intrinsic stresses. From the slope of the stress versus temperature it is theoretically possible to calculate the CTE of the film. This is only possible if the intrinsic stresses remain constant with temperature. This is not usually the case and only valid during cooling to room temperature. The expression for the slope follows from differentiating 4.2 with respect to temperature:

$$\frac{d\sigma}{dT} = \frac{E_f}{1-\upsilon_f}\left(\alpha_s - \alpha_f\right) \qquad \textbf{(4.4)}$$

For the CTE of the film this can be rewritten to:

$$\alpha_f = \alpha_s - \frac{d\sigma}{dT}\frac{1-\upsilon_f}{E_f} \qquad \textbf{(4.5)}$$

With the material parameters and the slope, the CTE of the film can be calculated. Experiments with two different substrates, on the other hand, allow the determination of both α_f and M_f [Zhao *et al.*, 2000a]. The substrate curvature method can be further extended to extract the Poisson ratio by using films with periodic line patterns.

The out-of-plane thermal expansion coefficient can, in principle, be obtained by monitoring the thickness change as a function of temperature. Care should, however, be taken with the interpretation of this data since the substrate constraining effect may result in an increase of the CTE with a factor of 2 to 3. The apparent constraint CTE can be expressed in terms of the Poisson ratio and the free film expansion coefficients [Lee and Bae, 2000]:

$$\alpha_f^{constr} = \left(\frac{1+\nu_f}{1-\nu_f}\right)\alpha_f - \left(\frac{2\nu_f}{1-\nu_f}\right)\alpha_s \qquad \textbf{(4.6)}$$

The substrate curvature (or curved beam) method is a useful tool to determine stresses in multi-layer structures. The curvature of a multi-layer structure, κ_{multi} results from a linear superposition of bending effects originating from the stresses in the individual film layers [Kim *et al.*, 1999; Klein, 2000]:

$$\kappa_{multi} \cong \frac{6}{M_s h_s^{\,2}} \sum_i M_{fi} h_{fi} (\alpha_{f\,i} - \alpha_s)\Delta T \qquad \textbf{(4.7)}$$

With M=E/(1-ν), the biaxial modulus. The measurement of substrate curvature and/or wafer thickness can be achieved with either a stress analyser that is equipped with a laser, a hot stage in dry nitrogen gas atmosphere or a laser interferometer [Kook and Kim, 2000; Zhoa *et al.*, 2000b; Pelletier *et al.*, 2002].

Wafer warpage measurements can also be used to determine the material properties of the metals used in ICs. Drawback in this case is that the material properties of the metal lines in ICs are different than the bulk properties. This is caused by the small dimensions, the texture, the deposition process and the presence of constraining volumes (substrate, dielectrics). Measurements on free standing films may give an indication of the intrinsic properties of the metal film, revealing lower Young's modulus than the bulk value and a higher yield strength [de Lima *et al.*,

1999; Huang and Spaepen, 2000; Kalkman *et al.*, 2001]. Keep in mind that the actual configuration of aluminium lines consists of a stack of Ti/TiN/Al. The mechanical response of such a stack is different than that of the pure aluminium line. Also, aluminium is being replaced by copper in the latest and to be developed CMOS technologies (90nm up to 45nm feature size).

Sample Silicon wafers with a 725µm thickness are deposited with different layers and after processing, the warpage at room temperature is measured to deduct the total stress in the film. Table 4.1 lists the different deposited layers and the corresponding total stress in the layer at room temperature. For example, a layer of 300nm TEOS is deposited on a 725µm Silicon wafer at a temperature of 400˚C. For the Silicon, E = 165.7GPa in the relevant plane, ν=0.23 and the CTE equals 3.0ppm/˚C. The warpage of this wafer at room temperature is measured at -330m, where the warpage of the blank Silicon wafer is measured at -3500m. Using equation 4.3 the total mechanical stress in the deposited layer is be calculated as:

$$\sigma_{total} = \frac{165.7E3}{6(1-0.23)} \frac{0.725^2}{300E-6}\left(\frac{1}{-330}-\frac{1}{-3500}\right) = -172MPa \qquad \textbf{(4.8)}$$

Table 4.1: Deposited layers and corresponding total stress at room temperature.

Substrate	**Film**	**Film thickness [nm]**	**Deposition temperature [°C]**	**Warpage [m]**	**Total stress (RT) [MPa]**
725µm Si	SiON	604	400	-174	-170
725µm Si	PSG	502	400	471	90
725µm Si	TEOS	300	400	-330	-172

The wafers are used to measure the warpage as function of temperature. For this, the wafer is subjected to two temperature cycles from RT to 400°C. The heating rate is 5°C/minute. Figure 4.2 shows the measured warpage as a function of temperature for the wafer with the 300nm deposited TEOS layer. The intrinsic stress in the film can be found from the measured stress at deposition temperature. The intrinsic stress for these TEOS films is approximately –60 to -70MPa (compressive intrinsic stress). The slope of the stress-temperature curve is positive which indicates that the CTE of

TEOS is lower than the CTE of the silicon. With the fitted line a CTE for the TEOS can be predicted according to equation 4.5:

$$\alpha_{TEOS} = 3.0E-6 \ -(0.20)\frac{1-0.25}{70e3} \ = \ 0.86\,ppm/°C \qquad (\mathbf{4.9})$$

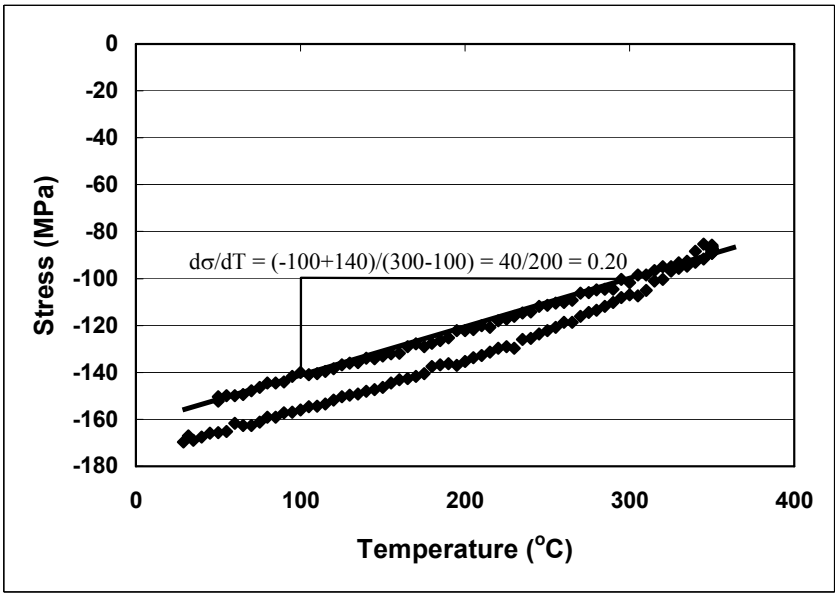


Figure 4.2: Measured warpage as a function of temperature for a 300nm TEOS layer deposited on a 725μm Silicon wafer.

The above procedure is also performed for the SiON and the PSG films. The resulting properties for the thin film materials are listed in Table 4.2. This table includes values for Young's modulus, Poisson ratio, CTE, intrinsic stress levels and yield stress (for the metals). The values for Si_3N_4 and Al (0.5% Cu) are taken from the literature [de Lima, 1999 *et al.*; Kalkman *et al.*, 2001; Kasthurirangen and Ho, 1998].

Table 4.2: Properties for IC materials.

Material	**E [GPa]**	**ν [-]**	**CTE [ppm/°C]**	**Intrinsic stress [MPa]**
Si	165.7 (relevant plane)	0.23	3.0	-
PSG	70	0.25	3.15	+80
SiON	110	0.25	2.9	-140

Material	**E** **[GPa]**	**ν** **[-]**	**CTE** **[ppm/°C]**	**Intrinsic stress** **[MPa]**
TEOS	70	0.20	0.6	-70 (low stress variant) +70 (high stress variant)
Si_3N_4	190	0.20	2.0	-140
Al (0.5% Cu)	60	0.35	20	200 (yield stress)

4.1.2 Prediction of Thin Film Warpage and Stresses

To predict wafer warpage levels, both analytical and numerical modelling techniques, combined with experimental verifications will gain insight into the physics of the backend processes. 3D FE modelling results are verified by a series of experiments using specially designed backend wafers to monitor the warpage during manufacturing. Figure 4.3 shows a 3D FE model representing a silicon wafer with diffused metal and dielectric layers. Because of symmetry, only one quarter is necessary. The model is meshed with 3600 solid 8-noded brick elements. Appropriate boundary conditions are used along both symmetry axes. Six silicon wafers from a 0.5µm CMOS process with a diameter of 200mm are used from experimental side. Layer thicknesses are 800µm bare Si, 0.5µm TEOS, 1µm Al, 1.0µm TEOS, 0.5µm PSG and 0.5µm SiON. The last three layers are the so-called passivation (PV) layers, which provide scratch protection to ICs. An analytical model is developed to predict the in-plane layer stresses and the warpage of the wafer during the building up of the thin films. For each method, analytical, numerical, or experimental all process steps are taken into account.

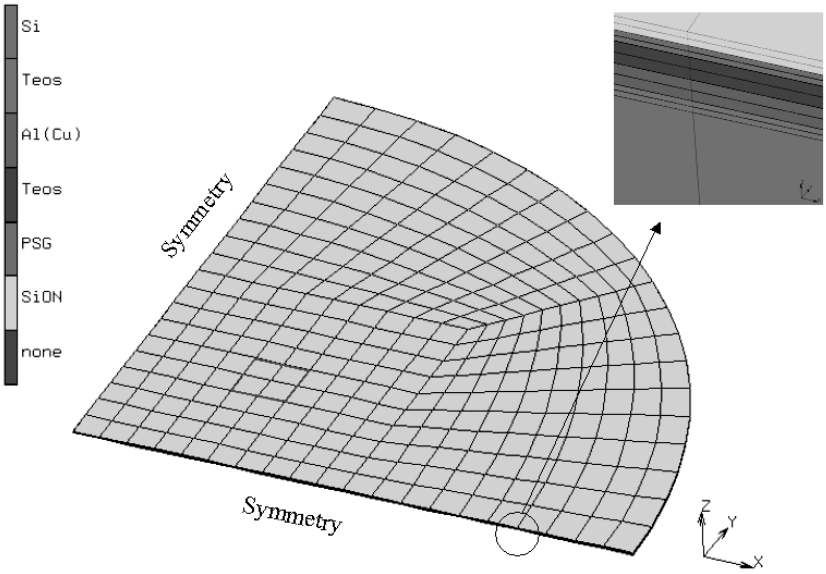


Figure 4.3: 3D FE wafer model including diffusion layers.

Element birth and death methods are used to activate deposited layers correctly. However, the deposited layer should have a changed geometry but exert no stress and strain, since deposition is done at high temperatures. To simulate this successive build-up correctly a special procedure is developed using stiff beam elements. These beam elements transport the nodes of the solid elements that are not yet activated. For not yet deposited layers, the solid elements are deactivated and the beam elements (located at the edges of each solid elements) are activated. By doing so, the deformations of the layer are properly taken into account. An important feature of this method is that the solid elements are in a stress- and strain-free condition when they are activated, this cannot be achieved by using a trick based on temperature dependent material properties. For the six wafer samples, the change in warpage $\Delta\kappa$ is measured after each of the following steps:

- Step 0: Bare silicon (initial warpage).
- Step 1: After TEOS deposition (at 400ºC).
- Step 2: After Metal deposition (at 450ºC).
- Step 3: After TEOS, PSG and SiON deposition (at 400ºC).

The effect of metal deposition is significant: metal deposition changes the curvature of the wafer from convex (n-shape or grumpy, denoted with - sign) to concave (u-shape or smiley, denoted with + sign). The metal patterning reduces the warpage change with approximately 50%. This reduction is driven by the coverage of the metal, which is approximately 50% in the wafer samples. The experimental warpage change of the wafer after thin film deposition is used to calculate the stress level in the film. Both the warpage change and the analytically calculated stress levels are compared with the numerical predictions. Table 4.3 lists the results of the experimental, analytical and numerical predictions. For the warpage, a good agreement between experiment and numerical FE prediction is obtained. Large deviation, approximately 30%, is found for the warpage change due to thermo-mechanical effects of the metal. Several explanations can be found for this difference. First, the metal behaviour is quite complex including plasticity, phase transformation and position dependent material properties. Secondly, annealing of the wafer is observed to influence the warpage significantly. Finaly, in the FE model no time dependency is taken into account.

Regarding the stress levels a good agreement is found between the analytical and numerical models. Note that for both predictions no intrinsic stresses and metal yielding are included. The FE simulations show that the stress in a thin film is hardly influenced by the warpage changes caused by subsequent processes. Also, it is found that the total film stresses are a summation of thermo-mechanical and intrinsic stress levels. For instance, in case of the TEOS layer with an intrinsic stress of –70MPa (see Table 4.2), the total stress in the layer is actually –87-70 = -157MPa. The added intrinsic stresses hardly relax, because the films of TEOS, PSG and SiON are very thin compared to the substrate. However, adding initial stresses in a thin film does influence the warpage of the wafer. Tensile intrinsic stress leads to a more positive warpage change (upward bending) and compressive intrinsic stress leads to a more negative warpage change (downward bending).

In conclusion, the results show that in order to obtain accurate and reliable prediction models for wafer build-up processes, both the intrinsic stresses and the manufacturing process should be taken into account. Chapter 6 consists of an application using the material properties and numerical methods described above.

Table 4.3: Resulting warpage and stress levels after thin film deposition; experiments vs. analytical and numerical predictions.

Process Step	Experimental	Analytical	Numerical (without intrinsic stress / yielding)
TEOS			
ΔK [m^{-1}]	-0.00168		-0.00169
σ_{total} [MPa]	-	-87	-62
Metal			
ΔK [m^{-1}]	0.00872		0.01139
σ_{total} [MPa]	-	679	666
PV 1, 2 and 3			
ΔK [m^{-1}]	-0.00188		-0.00225
σ_{total} [MPa]	-	-87 (PV1)	-87 (PV1)
		+4 (PV2)	+4 (PV2)
		-7 (PV3)	-6 (PV3)

4.2 Process Induced Warpage of Electronic Packages[1]

Experiments are necessary to verify numerical results in order to be sure that the results obtained from FE models are reliable and accurate enough from both quantitative and qualitative perspectives. Currently, optical methods have been used widely as characterisation tools, but the conventional methods have disadvantages when applied to the electronic packages. They are usually limited to one or two-dimensional measurements. Although 3D characterisation can be found occasionally, 3D measurement is not made during the same procedure. Recently, a 3D Interferometry measurement system that can measure simultaneously out-of plane and in-plane deformations has been developed, see Figure 4.4. Besides the capability of 3D measurement, this system has the following unique features:

[1] Reproduced from: van Driel, W.D., G.Q. Zhang, J.H.J. Janssen, L. J. Ernst, F. Su, K.S. Chian, S. Yi, Prediction and verification of process induced warpage of electronic packages, Microelectronics Reliability 43 (5), pp. 765-774, 2003a.

- Capability of displaying fringe patterns of U-, V- and W-fields on the screen simultaneously; where . deformations in U-, V- and W-field coincide with deformations in orthogonal x-, y- and z-directions.
- Capability of phase shifting in U- and V-field easily and simultaneously.
- Wide range of the magnification of images.
- Specially designed thermal and mechanical loading system.

In this section, firstly, FE models are developed to predict the thermal deformations of certain electronic packages and naked die samples under packaging and testing loading. For all the package constituents, appropriate material properties and models are used, including temperature-dependent visco-elasticity, anisotropy and temperature-dependent elasticity and plasticity. Secondly, the basic principle of the developed 3D interferometry measurement system is highlighted. Comprehensive warpage measurements are performed after two specific manufacturing processes, i.e., die-attach and post-mould-curing. Thermally induced deformations are obtained using 3D interferometry techniques during two thermal cycles. Finally, the results of the warpage measurements are compared with the results of non-linear FE modelling.

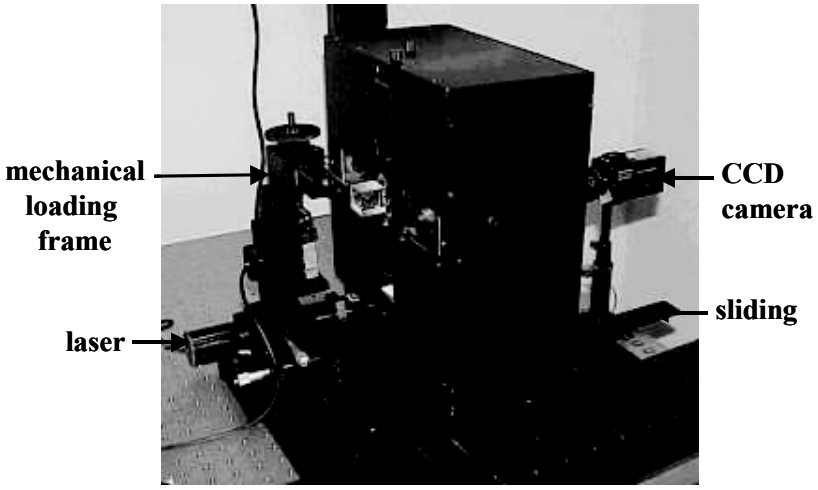


Figure 4.4: Feature of the integrated Interferometry system.

4.2.1 Finite Element Models

Parametric 3D FE models representing both the naked die and package samples are developed. Because of symmetry, only one quarter of the sample is modelled. The effect of element sensitivity is explored by using several distributions and/or discretisations. In total, the naked die model consists of approximately 4,000 8-noded

elements, the package model of approximately 12,000 elements. Both FE models are presented in Figure 4.5. In both FE models, along the xz-symmetry axis all nodes are constrained in y-directions, along the yz-symmetry axis all nodes are constrained in x-directions. To avoid rigid body movements, one node is constrained in z-direction.

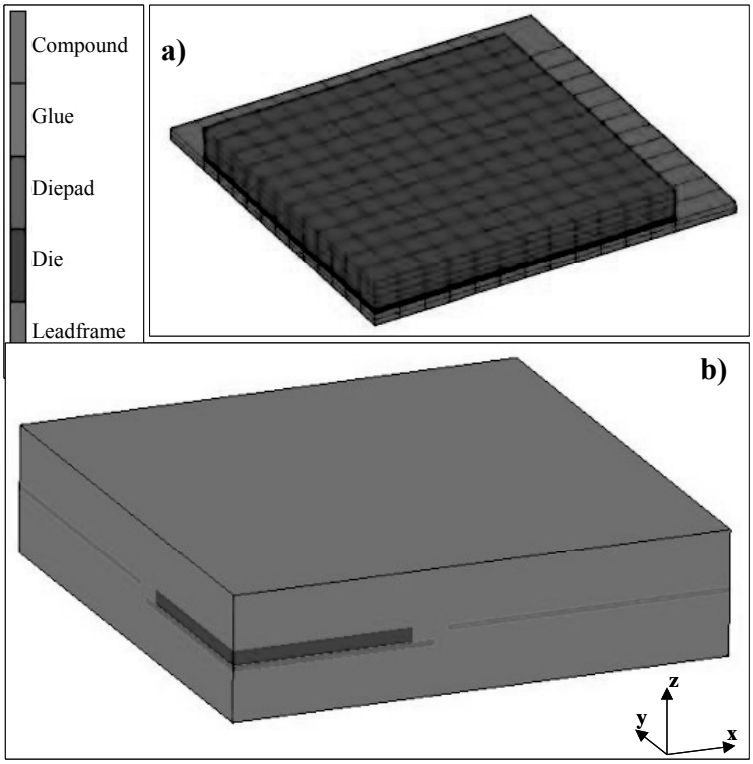


Figure 4.5: ¼ FE model for naked die sample (a, with mesh discretisation) and package sample (b).

The single crystal silicon die is modelled as temperature independent anisotropic. For a linearly elastic material, a general equation relating the stress tensor σ_i to the strain tensor ε_j can be expressed as follows:

$$\sigma_i = C_{ij}\varepsilon_j \;;(i,j = 1,..,6) \qquad \textbf{(4.10)}$$

Where C_{ij} is a stiffness tensor. For the silicon crystal, due to the cubic symmetry of its structure in the orthogonal ([100] [010] [001]) coordinate system, the anisotropic properties of the stiffness can be presented by the 6×6 matrix C_{ij}. However, for a silicon crystal lying in the [001] plane, these values should be rotated to the

orthogonal coordinate system as used in the FEM simulations. Therefore, the stiffness matrix C_{ij} undergoes the following transformation:

$$[C_{ij}^{'}] = [T][C_{ij}][T]^{T} \quad \textbf{(4.11)}$$

where [T] and $[T]^{T}$ are the transformation matrix and its transverse, respectively. If [001] is chosen as the z-direction and [110] as x- and y-directions, after undergoing the rotation, the crystal silicon orientation is lined up with the FEM coordinate system. Ultrasound measurements (20/40 MHz) were used to obtain the stiffness values in the different directions for the silicon crystal [McSkimin and Andreatch, 1964; Nikanorov *et al.*, 1972; George, 1999]. It was reported that the stiffness values at temperature 273 K range from 170 GPa in the *[110]* plane to 130GPa in the *[100]* plane. The temperature dependence of the stiffness values was found to be negligible, for instance the in plane value at 473K is only 0.5% lower. Previous research work also showed that the temperature independence of the thermal expansion coefficient (CTE) for the silicon crystal is valid within a certain temperature range [Maissel, 1960; Ibach, 1969, Shah and Straumanis, 1972].

For the compound and die-attach materials, linear visco-elastic models are used. The time and temperature dependent Young's, shear and bulk moduli of the die-attach and compound material are obtained through bending and torsion Dynamic Mechanical Analysis (DMA) tests. Specimens are prepared according to the geometrical and curing conditions of the materials in the electronic package. For the bending tests, the specimen is clamped as a single cantilever beam. A sinusoidal deflection is applied to one end of the beam at various frequencies. For the torsion tests, a cyclic twist is applied to one end of the specimen, and the torque responded by the specimen is measured. Frequency-temperature sweep DMA tests are performed in order to determine the frequency dependence of the moduli at any constant temperature. In order to obtain master curves, the moduli at 30°C are taken as the moduli at the reference temperature. The master curves are fitted by a fractional series, which is the conversion of the exponential Prony series into the frequency domain:

$$E^{'}(\omega) = \sum_{n=1}^{N} E_n \frac{(\omega\tau_n)^2}{1+(\omega\tau_n)^2} \quad \textbf{(4.12)}$$

where ω is the frequency in radians/s. For the fitting of the fractional series, the relaxation times τ_n are set at selected values and the coefficients E_n are obtained through the fitting procedure. The moduli curves at the temperatures below and above 30°C are horizontally shifted until they meet the master curve. As such, the shift factor *a* is determined and under the assumption of thermo-rheological simplicity, a 3rd order polynomial is used to describe this shift factor. Following the procedure, the master curves for the relaxation Young's, shear and bulk modulus are obtained for both the compound and die-attach material and implemented in the commercially available non-linear finite element code MARC.

For the leadframe material, ideally plastic behaviour is assumed. All material properties are listed in Table 4.4.

Table 4.4: Material properties.

Material	**Elastic Modulus [MPa]**	**Poisson Ratio [-]**	**Coeff. Thermal Expansion [ppm/°C]**	**Yield Stress [MPa]**
Die	Anisotropic properties $C_{11} = C_{22} = C_{33} = 165700$ $C_{12} = C_{21} = C_{13} = 63900$ $C_{31} = C_{23} = C_{32} = 63900$ $C_{44} = C_{55} = C_{66} = 79600$		3.0	-
Leadframe QFP44 QFP120	 145000 130000	 0.35 0.35	 5.3 17.6	 480 600
Encapsulate	Visco-elastic, T_g=170ºC, CTE= 14.1 $T<T_g$ resp. 68.4 ppm/ºC $T>T_g$			
Die-attach	Visco-elastic, T_g=55ºC, CTE= 52 $T<T_g$ resp. 134 ppm/ºC $T>T_g$			

For both sample types, the complete time and temperature profile during manufacturing, i.e. die-attach, wire bonding, moulding, post mould cure and marking, is used in the simulations, followed by the experimental thermal cycle. To develop reliable and efficient non-linear thermo-mechanical prediction models for the product/process designs of electronic packaging, various simplifications and assumptions are needed:

- The curing of the die-attach material was investigated in a heat production test. In such a test, the heat generated in the material is continuously monitored during temperature increase. The heat production measurements on the die-attach material indicated at a warpage/stress free temperature of 150°C. Therefore, the warpage/stress free state for the silicon die-die-attach-leadframe assembly is set at 150°C. For the compound material a warpage/stress free temperature of 175°C is assumed.
- Isothermal loading conditions are used for both the manufacturing processes and the experimental testing conditions.
- The initial IC warpage/stresses are neglected.
- Perfect adhesion is assumed between die and leadframe, and between die and compound.
- The curing process induced stresses are neglected.

4.2.2 3D Interferometry – Theory and Principle

In the early 1980's, Post *et al.* [1990] proposed a novel Moiré Interferometry system by combining the techniques of high frequency grating and laser interferometry. This system turned out to be a powerful tool to offer non-contact, full field, high resolution approaches for measuring warpage mechanisms. Here, two different 3D interferometry techniques are used, i.e.:

1. Moiré interferometry for the in-plane deformations (U- and V-fields) with a resolution equal to 0.417μm/fringe. Using phase shifting techniques, this resolution can be improved to 0.1043μm/fringe.
2. Twyman/Green interferometry for the out-of-plane deformation (W-field) with a resolution equal to 0.316μm/fringe.

Although there are several explanations to the principle of Moiré interferometry [Post *et al.*, 1990; Shield and Kim, 1991], the wave front interferometry theory suggested by Dai *et al.* [1990] is a strictly and easily visualised explanation. In Moiré interferometry, a high frequency cross-line diffraction grating is replicated on the surface of the specimen and it deforms together with the underlying specimen. Two coherent beams in the horizontal plane incident on the specimen grating at a specific angle and create a virtual reference grating in their zone of intersection. The deformed specimen grating and the reference grating interact to produce the Moiré fringe

pattern (U-field pattern). Two beams in the vertical plane create another set of reference grating which interacts with the second set of lines and produces another set of fringe patterns (V-field pattern). The fringe patterns represent contours of constant U- and V-displacements in orthogonal x- and y-directions, respectively. The displacement can be determined by:

$$U = \frac{N_x}{f} \quad ; \quad \mathrm{V} = \frac{N_y}{f} \tag{4.13}$$

where {U, V} and {N_x , N_y} represent the displacements and fringe order in the U- and V-fields respectively and f represents the frequency of the reference grating. A reference grating with a frequency of 2400lines/mm is used, which provides a basic resolution of 0.417μm/fringe. With the aid of phase shifting techniques, this resolution can be improved by 4 times.

The Twyman/Green Interferometry is also a two-beam interferometry method and similar with that of Moiré interferometry. In this configuration, the incident flat wave front W is split into two; one for reference and another for contour information of the (deformed) sample. After reflected by a flat mirror and the sample surface respectively, these two wave fronts meet again and interfere with each other to form a fringe pattern on the CCD target. The (relative) out-of-plane deformation or warpage W of the sample can be determined with the fringe pattern by:

$$W = \frac{\lambda}{2} N_w \tag{4.14}$$

Where N_w is the fringe order relative to an arbitrary selected reference point of $N_w = 0$ and λ is the wavelength of the laser. In our study, a He-Ne laser with a wavelength of 0.632μm is used, which corresponds to a resolution of 0.316μm/fringe in the out-of-plane direction. Although the principles of Moiré Interferometry and Twyman/Green Interferometry are similar, some basic differences between them should be noted:

- In Moiré interferometry, diffraction behaviour is involved and both of the two wave fronts emerge from the same surface, any one acts as reference for another, and the deformation of the wave front is due to the diffraction behaviour. In Twyman/Green interferometry, no diffraction is involved, the two wave fronts originate from a different surface, one of them is the information carrier, and another is always kept flat and specifically used for reference.

- In Moiré interferometry, the fringe pattern represents the in-plane deformation. While in Twyman/Green interferometry, the fringe pattern represents the contour or shape of the sample in the out-of-plane direction. To measure the net deformation in this direction, two separate measurements should be made and compared.

An effectively integrated, compact 3D testing system is set up based on the Moiré and Twyman/Green Interferometry (Figure 4.4). The light source is induced by an optical fibre. The laser is coupled into a single-mode fibre. The single-mode fibre is split into two branches; one provides the light source for the sub-system of in-plane deformation measurement (2D Moiré system) and another for the sub-system of out-of-plane deformation measurement (Twyman/Green system). The loading system is an important accessory part of the 3D testing system. This system is composed of a mini-mechanical loading frame and a mini-thermal loading chamber, which is specifically designed for microelectronics products. The mini-loading frame and thermal chamber are sited on a six-dimensional adjustable base, which can move or rotate the sample along the x-, y- and z-axis. With this system, the 3D deformation of samples can be measured simultaneously during thermal cycling and/or mechanical loading conditions to give an accurate and 3D characterisation of the thermo-mechanical behaviour of electronic packages.

4.2.3 Samples and Experiments

The use of Moiré interferometry requires grating replication of the sample. For this, a high frequency diffraction grating is replicated onto the surface of the specimen which will deform together with the underlying specimen. For the samples used in this study, the grating is replicated at 175°C, where a warpage/stress free state is assumed. The sample is put into a thermal chamber at room temperature. When the temperature reaches 175°C, the temperature is hold for 30 minutes to i) fully relax the sample and ii) to reach a uniform temperature distribution. Next, a high temperature epoxy adhesive, i.e., TraCon F211, is applied and cured for another 30 minutes at 175°C. When the grating is fully cured, the samples are pealed off from the grating mold (quarts, which has a very low coefficient of thermal expansion) and ready for the measurements. Two types of samples, see Figure 4.6, are used in the verification experiments:

- Naked dies attached to a leadframe, based on a QFP44 leadframe design. A 7.5x7.5mm^2 IC is attached to a 9.0x 9.0mm^2 diepad.
- Real electronic packages, based on a QFP120 outline. A 9.8x9.8mm^2 IC is attached to a 11.0x11.0mm^2 diepad, moulded in a 28.0x28.0mm^2 body.

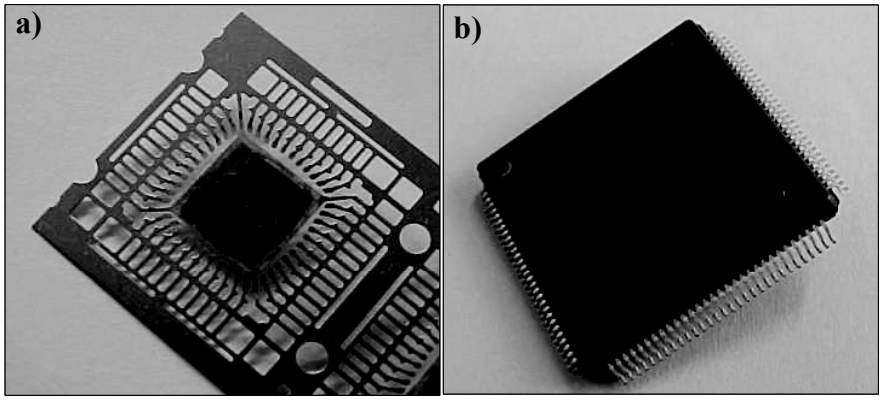


Figure 4.6: Naked die (a) and package (b) samples.

At the start of the experiment, the sample is placed, in a fixed way, in the mini thermal chamber. Starting from a temperature of 25ºC the sample is heated at a rate of 8ºC/minute. When it reaches 175ºC, the temperature is held for about 5 minutes, then it is cooled down naturally with the chamber door closed. The temperature in the thermal chamber is monitored by a thermocouple, placed close to the sample. For one experiment, the temperature of 175ºC was held for about 1 hour, to explore the relaxation effect of the samples. However, this experiment did not give other results. Deformations of the sample is recorded during heating and cooling, respectively. Two temperature cycles are recorded for each sample.

4.2.5 Results and Discussion

The possible thermal deformation in the "∩" shape is called convex and the one in the "∪" shape is called concave. The deformation is measured along the diagonal direction of the die. Deformations in the orthogonal x-, y- and z-directions are called U-, V- and W-field respectively. Notice that for the out-of-plane W-field, the Twyman/Green interferometry technique is used, allowing measuring relative deformations with respect to the central point. For the in-plane U- and V- fields, the Moiré technique is used, allowing to measure relative deformations with respect to a reference shape corresponding to the grating replication temperature.

Measured fringe patterns in the U-, V- and W-fields for a naked die sample at 25ºC, 65ºC, 135ºC and 175ºC during the cooling down stage of the 2nd thermal cycle is depicted in Figure 4.7. Each fringe resembles a deformation of 0.417 μm in the U- and V-field (Moiré Interferometry) and 0.316 μm in the W-field (Twyman/Green Interferometry). As the temperature rises the number of fringes decreases, indicating that the total deformation decreases. At a certain temperature, a minimum for the number of fringes is reached. At that point, the sample is almost flat. For the naked die sample this zero warpage is reached between 120ºC - 130ºC during the heating stage of the 2nd thermal cycle. After this temperature, the number of fringes increases, see the results at 135ºC and 175ºC. This indicates that the shape of the sample changes from convex ("∩") to concave ("∪"). During the cooling stage of the 2nd thermal cycle, the zero warpage temperature is further increased to approximately 140ºC. The zero warpage observations confirmed the assumption of the warpage/stress free temperature for the silicon die-die-attach-leadframe assembly used in the FE models.

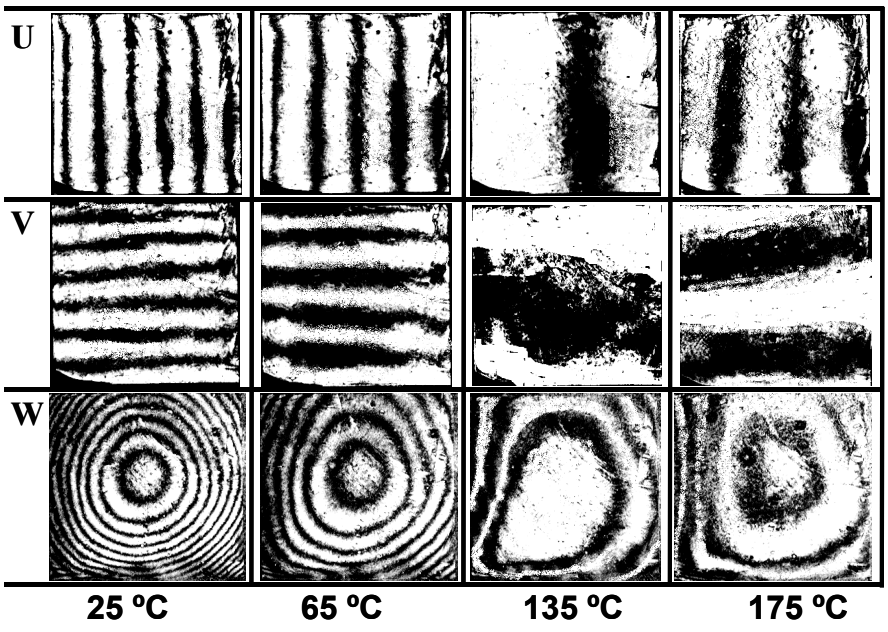


Figure 4.7: Fringe patterns of the naked die sample during the heating stage of the 2nd thermal cycle.

It can be seen that the W-field fringe pattern in Figure 4.7 is non-symmetrical, where a more circular pattern is expected. This non-symmetry pattern is caused by an

asymmetric placement of the die on the diepad and a non-uniform die-attach thickness. Figure 4.8a shows a top view of a naked die sample, indicating that indeed, the die centre does not coincidence with the diepad centre. Also, notice in this figure, that around the die the amount of die-attach filling is very different, i.e., there is more die-attach at the northern part. This indicates a non-uniform die-attach thickness distribution. Both effects will cause a non-symmetrical deformation pattern in the W-field.

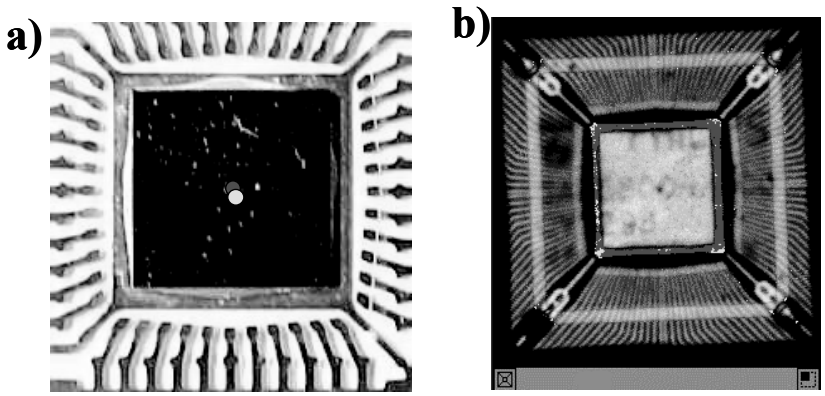


Figure 4.8: Top view on naked die (a) and package sample (b) indicating the asymmetric location of the die (dark point) to the diepad (light point) centre and the occurrence of delamination between diepad and compound. Also notice the different amount of die-attach fillet around the die (a).

Measured fringe patterns in the U-, V- and W-fields for a package sample at 25ºC, 50ºC, 115ºC and 175ºC during the cooling down stage of the 2nd thermal cycle is depicted in Figure 4.9. As the temperature rises the number of fringes decreases, indicating that the total deformation decreases. Largest deformations are found in the centre of the package, where the die is located. Given the large deformations in the centre of the sample, a more or less S-shaped deformation is observed on the top of the package. Outside that area, a fuzzy pattern occurs, which is caused by the 120 internal leads. For the U- and V-field fringe patterns in Figure 4.9, the shape of the fringe lines strongly deflects around the die area. This is caused by delamination at the interface between the diepad and the compound, see Figure 4.8b. At around 160ºC – 170ºC, the sample is almost flat.

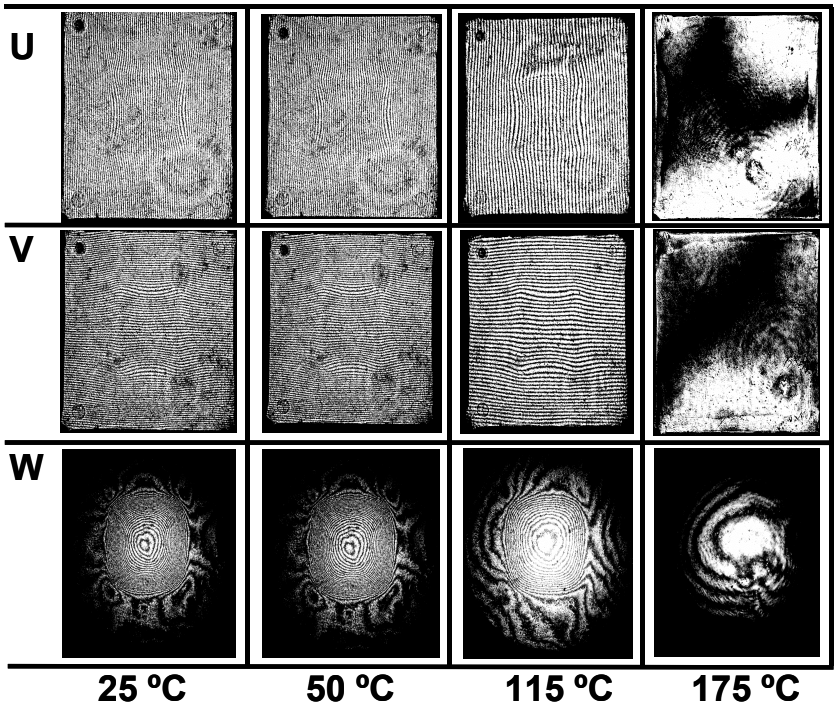


Figure 4.9: Fringe patterns of the package sample during the heating stage of the 2nd thermal cycle.

The results of the FE simulation are compared with the results of the interferometry measurements. For the U- and V-fields this implies a deformation relative to the grating temperature (175ºC), for the W-field a deformation relative to the centre of the sample. For the naked die sample, a dedicated comparison of measured with calculated deformations during two thermal cycles is listed in Table 4.5 These results show that at the end of the 2nd thermal cycle the simulated values are closer to the measured ones than during the 1st thermal cycle. This is due to the relaxation effect within the product, occurred in the time span between manufacturing and measurement. The deformation pattern of the naked die sample at the end of the 2nd thermal cycle at 25ºC on a top view for both the measurements and FE simulations is depicted in Figure 4.10. For the package sample, both the measured and simulated deformation patterns are depicted in Figure 4.12. Both figures clearly show identical pattern for both the measured and simulated results.

Table 4.5: Dedicated comparison of measured with calculated deformations for the naked die sample during 2 successive thermal cycles.

	Measurement [μm]			**Simulation [μm]**		
Temperature	**U**	**V**	**W**	**X**	**Y**	**Z**
1st cycle – heating stage						
25ºC	-2.4	-2.6	-5.8	-2.1	-2.1	-5.8
115ºC	-0.6	-0.6	-1.5	-0.2	-0.2	-1.4
135ºC	0.0	0.0	0.0	-0.1	-0.1	-0.2
175ºC	+0.8	+0.8	+0.9	+0.5	+0.5	+0.8
2nd cycle – cooling stage						
145ºC	0.0	0.0	0.0	-0.1	-0.1	-0.2
100ºC	-1.0	-1.0	-2.0	-1.1	-1.1	-1.9
25ºC	-2.2	-2.4	-5.8	-2.1	-2.1	-5.8

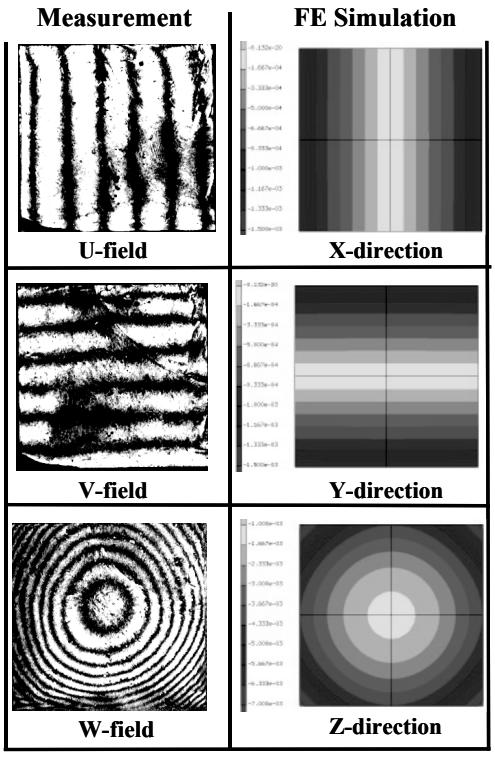


Figure 4.10: Measured U-, V- and W-field vs. calculated x-, y- and z-deformation patterns for the naked die sample at 25ºC.

The warpage of the naked die sample during cool down in the 2nd thermal cycle as a function of temperature is depicted in Figure 4.11a. This figure shows that the mismatch between measured and simulated results during the 2nd thermal cycle for the naked die samples is within 15%. The horizontal and vertical deformation of the package sample from centre to edge after cool-down to 25ºC is depicted in Figure 4.11b. Measured results are compared with those from the FE model using visco-elastic properties versus linear elastic properties for the compound and die-attach materials. Linear elastic properties for both materials are based on supplier data. This figure shows that the mismatch is very large when linear elastic properties are used in the FEM models. The figure clearly demonstrates that the time-dependent effects in IC materials can not simply be neglected for quantitatively reliable prediction of deformations in electronic packages. The largest deviation between measured and simulated results is found nearby the delaminated interface between the diepad and the compound.

Quantitatively, Figure 4.11 shows that the mismatch between the measured and simulated results is within 15%. This difference can be attributed to time effects such as degradation and relaxation, asymmetric placement of the die on the diepad, non-uniform die-attach thickness below the die and possible interface delamination.

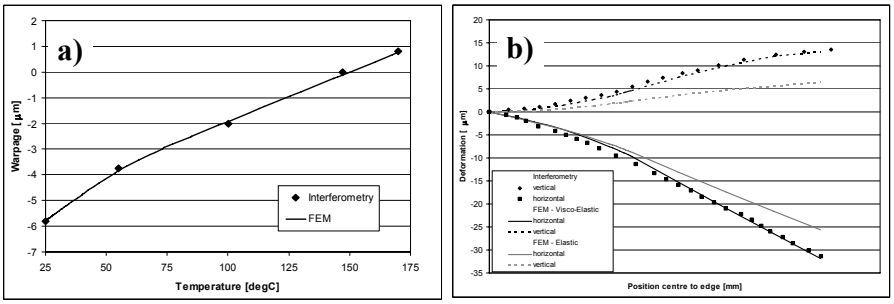


Figure 4.11: Comparison between measured and calculated deformations with: (a) warpage of the naked die sample during cool down in the 2nd thermal cycle as a function of temperature; (b) horizontal and vertical deformation of the package sample from centre to edge after cool-down to 25ºC. Measured results are compared with those from the FE model using visco-elastic properties versus linear elastic properties for the compound and die-attach materials.

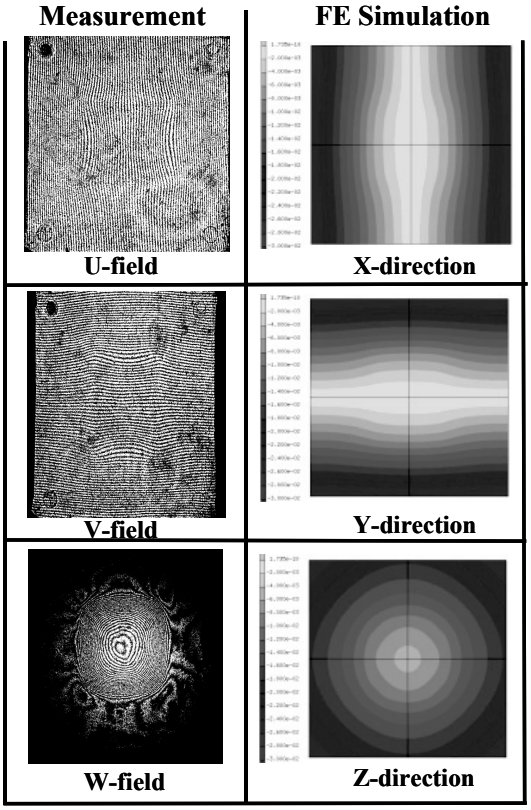


Figure 4.12: Measured U-, V- and W-field vs. calculated x-, y- and z-deformation patterns for the package sample at 25ºC.

The results show that the interferometry technique can be used for both in-plane and out-of-plane deformation measurements of IC packages, with quantitatively reliable accuracy. Thermal deformations obtained from the non-linear FEM models match well with measured deformations for both the naked die samples and the microelectronics package. Chapters 5, 6, 7 and 8 consist of applications using the material properties and numerical methods described above.

4.3 Interface Strength Characterization

The goal of adhesion tests is to obtain a quantitative value for the interface strength, or interface toughness, which can be used as input / comparison with FE results in order to forecast initiation and propagation of failure. Determining the interface strength between two materials requires loading of a sample consisting of two

material layers in such a manner that the crack growth can be controlled. Many different test method are available, among which are the 90º peel test [Shih *et al.*, 1995], three point bending with pre-crack [Tay *et al.*, 1999; Tanaka *et al.*, 1999], single leg bending [Pierraci *et al.*, 1998], wedge test [Dostal, 1990; Xu and Dillard, 2003], brazil nut [Kuhl and Qu, 2000], button shear or pull [Szeto, 2000; Yuen, 2003], four point bending [Charambalides, 1989; Yoa and Qu, 2002; Wang, 2003b], dual cantilever beam [Taweeplengsangsuke and Pearson, 1998; Dai *et al.*, 2000], modified ball-on-ring [Tay *et al.*, 1999; van Gils *et al.*, 2004] and/or three point and mixed mode bending test [Reeder and Crews, 1990; Merril and Ho, 2004; Thijsse *et al.*, 2006]. Examples of these tests methods are given in Figure 4.13. In this section, the application and results of the four point bending test under temperature and moisture conditions for the moulding compound leadframe interface is presented. Chapter 8 consists of an application using these results.

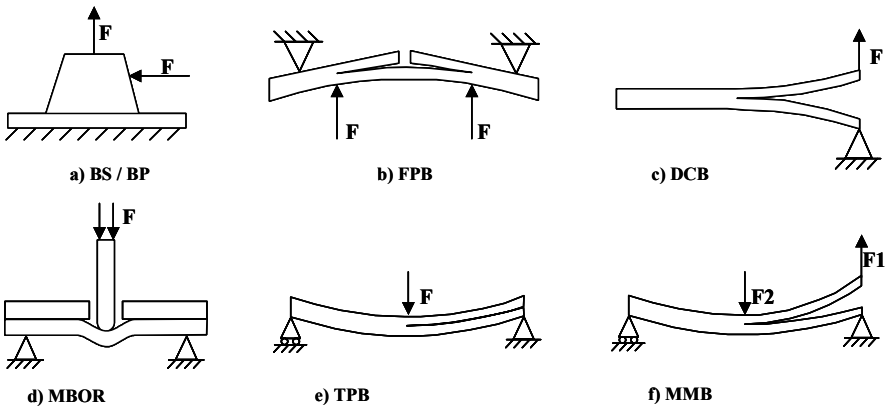


Figure 4.13: Different test configurations for measuring interface strength: a) button shear/pull, b) four point bending, c) double cantilever beam, d) modified ball-on-ring, e) three point bending and f) mixed mode bending.

4.3.1 The Four Point Bending Test

The four point bending adhesion test is developed as a method for characterizing the fracture resistance of bi-material interfaces [Charambalides, 1989]. In a four point bending test, the sample consists of a bi-material sample with an initial notch loaded in the typical four point set up. The characteristics of this test are mixed-mode loading conditions at the crack tip comparable to practical loading condition, Stable crack propagation, Simple sample geometry, and a well-established testing routing with a

minimum of alignment influences. The stable crack propagation results in a constant load during delamination, which simplifies the determination of the fracture resistance because it is independent on the delamination length. Analytical equations for the resulting energy release rate can be determined. Several characteristics and dependencies of the test have been analysed such as the dependency of the mode mixity (or phase angle) on the thickness ratio and the Young's modulus ratio of the two materials [Charambalides, 1989]. A problem with this set up that might occur is vertical cracking of the debonding layer, which prohibits the determination of the interface strength. To solve this problem an additional stiffening layer can be used [Hofinger, 1998]. This additional layer suppresses the segmentation of the (brittle) layer and increases the stored energy in the sample and therefore the driving forces for delamination. With special geometric assumptions, an analytical solution for the energy release rate, or interface fracture toughness, G_c is possible:

$$G_C = \frac{M^2(1-\upsilon_2{}^2)}{2E_2}\left(\frac{1}{I_2}-\frac{\lambda}{I_C}\right) \qquad \textbf{(4.15)}$$

With:

$$\begin{aligned} &\lambda = E_2(1-\upsilon_1{}^2)/E_1(1-\upsilon_2{}^2) \\ &I_2 = \frac{1}{12}h_2{}^3 \\ &I_C = \frac{1}{12}h_1{}^3 + \frac{\lambda}{12}h_2{}^3 + \lambda h_1 h_2 (h_1+h_2)^2 \Big/ 4(h_1+\lambda h_2) \end{aligned} \qquad \textbf{(4.16)}$$

The subscript 1 indicates quantities relevant to the top layer, whereas the subscript 2 denotes the corresponding quantities for the bottom layer. Subscript c refers to the composite beam. Note that the moment per unit width $M = Pl/2B$, with P being the constant load. E and ν denote the Young's modulus and Poisson's ratio, h is the thickness, b is the width of the specimen and l is the distance between the inner and outer support points. Some points should be noted:

1. Steady-state crack growth can be obtained under the condition that the debonding crack length is significantly larger than the substrate thickness and the debonding crack length is smaller than a quarter of the inner span.
2. During debond cracking, a combination of mode I (normal stress) and mode II (shear stress) will act on the crack.

3. Plastic or visco-elastic dissipation that occurs in the layer stack itself will also lead to an increased measured energy release rate. The measured value is then not the intrinsic adhesion energy, but an effective value including other dissipating mechanisms.
4. To draw any meaningful conclusions, the fracture surfaces of the specimens should be chemically analysed after adhesion testing to assess the locus of failure.

There are three basic types of loading that a crack can experience, they are opening (mode I), sliding (mode II) and tearing (mode III) [Gdoutos, 2005]. The ratio of mode I and mode II loading is characterized by the mode angle ψ, or mode mixity, as:

$$\psi = \arctan^{-1} \frac{K_{II}}{K_I} \tag{4.17}$$

With K_I and K_{II} the stress intensity factors which describe the stress state around the crack tip. When describing fracture in one homogeneous material, the mode angle is defined by the orientation of the stress field. In a bi-material, the oscillatory index ε is a measure of the elastic mismatch between the two materials, and can be derived from the stress field around the tip and the Young's modulus and Poisson's ratio of both materials using the so-called Dunders' parameters [Dundurs, 1969]. Because of this oscillatory stress field, ψ will have to be defined at a certain reference length from the crack tip, D. In this situation, equation 4.17 changes to:

$$\psi = \arctan^{-1}\left[\frac{\mathrm{Im}(KD^{ie})}{\mathrm{Re}(KD^{ie})}\right] \tag{4.18}$$

With:

$$\begin{aligned} K &= K_I + K_{II} \\ \varepsilon &= \frac{1}{2\pi}\ln\left(\frac{1-\beta}{1+\beta}\right) \\ \beta &= \frac{\mu_1(\kappa_2 - 1) - \mu_2(\kappa_1 - 1)}{\mu_1(\kappa_2 + 1) + \mu_2(\kappa_1 + 1)} \end{aligned} \tag{4.19}$$

The subscripts *1* and *2* refer to the different materials, the shear modulus is given by $\mu = E/(2(1+\nu))$, with Young's modulus E and Poisson's ration ν and $\kappa = 3-4\nu$ for plane strain conditions. Since each interface will be loaded under a certain mode mixity, it is vital to know this value for each test set up.

4.3.2 Sample and Finite Element Model Description

To investigate the interfacial adhesion between moulding compound and leadframe a dedicated frame is designed existing of a large diepad. This diepad can be overmoulded and in a next process step sawn into the samples needed. The design is a 0.2mm thick, QFN-based, copper frame with a pre-plated (ppf) NiPdAu finish. The leadframes are stored under oxygen-free conditions to avoid oxidation. Using standard processes, a 0.65mm thick layer of moulding compound is added to the frame. For the four point bending tests, pieces of 9mm wide and 60mm long are used and a notch of 85% depth is sawn into the samples. Figure 4.14 shows both the overmoulded frame and two sawn 60x9mm^2 samples. Besides the moulding compound – leadframe samples, samples are created in which first a 25µm thick die-attach layer is spread out over the leadframe after being overmoulded. Interface strength characterisation is performed as function of temperature and moisture content (dry vs. MSL1). Four different commercially available moulding compounds are used, denoted by MCA / MCB / MCC / MCD and two die-attach materials, denoted by DA1 / DA2.

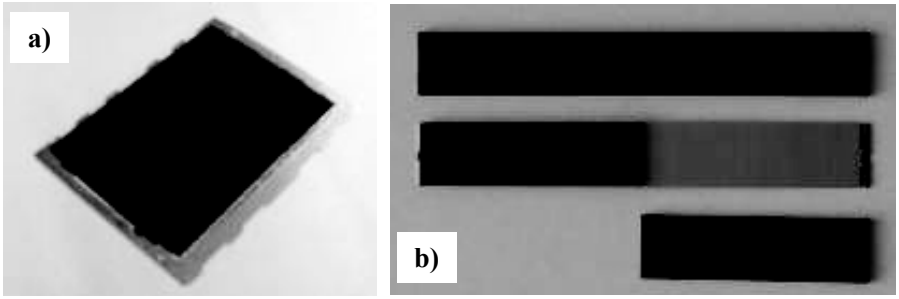


Figure 4.14: Overmoulded dedicated leadframe (a) and sawn samples as used for the four point bending test.

A 2D plain strain FE model is constructed representing the four point bending test. For evaluating the critical interface fracture toughness, linear elastic fracture mechanics is applied using the J-integral technique. The J-integral value is calculated at the interface and represents the available energy to delaminate the interface [Rice, 1968]. Figure 4.15 shows the FE model and a detail of the crack tip mesh. For the compound and die-attach materials, the time-, temperature and moisture-dependent properties are taken into account.

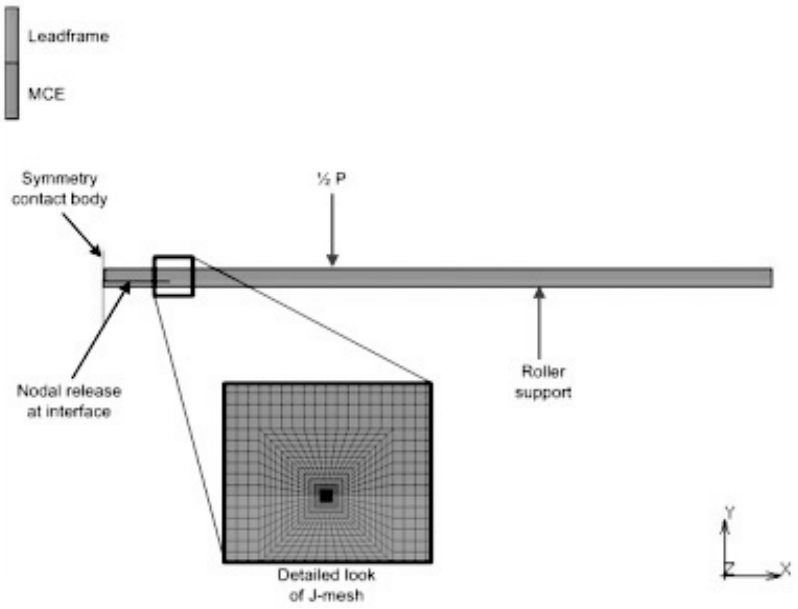


Figure 4.15: 2D Plain strain FE model representing the four point bending test. Detail of the crack tip mesh is shown.

4.3.3 Results and Discussion

Figure 4.16 shows the reproducibility of the four point bending test, in which 8 MCA samples are tested at a temperature of 20ºC. At the initial stage, the response is elastic and the applied load increases with the displacement. At some critical displacement, the load suddenly drops, caused by cracking of the notch. When this crack reaches the interface, the load stabilizes and the crack kinks into the stack. From this constant allowable load, the interface fracture toughness value is derived. For the 8 shown results, a load of 1.84±0.11N is measured, which is a very satisfying reproducibility. For each variation at least 6 tests are executed. The fracture surfaces are visually analysed after the test. The failure path of all the different specimens are always located at the interface nearest to the leadframe.

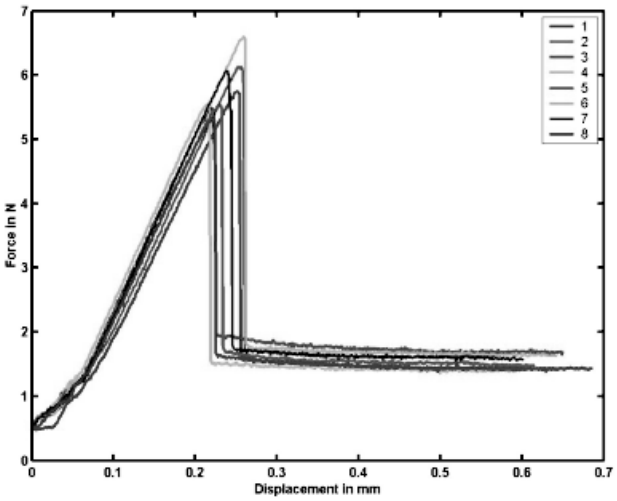


Figure 4.16: Reproducibility of the four point bending test using MCA.

Table 4.6 compares the analytical and FE results for the interface fracture toughness for MCA at different conditions. The mismatch is due to the fact that in the analytical case, the thermal- and hygro-mechanical properties are not taken into account. For the different variations, the FE-model results are used to analyse the experimental data.

Table 4.6: Comparison of derived interface fracture toughness between analytical solution and FE-model.

	Interface Fracture Toughness [J/m^2]	
Condition	**Analytical**	**FE-model**
Dry, 20ºC	6.2	5.7
Wet, 20ºC	5.1	3.2
Dry, 85ºC	6.0	5.8
Dry, 150ºC	5.0	5.1

Table 4.7 lists the results of the different material combinations and various conditions. At 20ºC and under dry conditions, the adhesion strength between compound and leadframe is approximately 6J/m^2. The FE model is used to calculate the mode mixity of the current set-up, revealing a value of 38º. These values comply

with those found in the literature. Tay *et al.* [1999] measured an interface strength of 4.5J/m^2 for the leadframe – compound interface at a mode mixity of $\psi = 0^o$.

Comparing the various compounds at 20ºC, the adhesion strength between MCE A, B and C are close to each other, but MCD has a significant better bonding to the leadframe. When moisture is present at the interface, the results show that the adhesion strength may decrease with 50% for MCA and MCD. MCB is less sensitive to the moisture. Clearly, moisture absorption degrades the interfacial strength. With increasing moisture content, the polymer molecules at the interface bond with water molecules and hydrogen bonds replace the attachment with the leadframe.

The adhesion strength also decreases with increasing temperature, but only become significant above the T_g of the compound (in this case 110ºC). This is both an effect of the mismatch in thermal properties and the degrading effect of a temperature increase itself. The influence of temperature on the interface fracture toughness is a 11% reduction from 20 to 150°C.

To explore the effect of oxidation and contamination, a set of leadframes are exposed to air for 48 hours after being overmoulded. As expected, oxidation and/or contamination shows a strong degrading effect, more than 200%. Surface conditions (contamination, treatment, etc.) and processing have a large influence on the adhesion strength.

The specimens with DA1 and DA2 show a higher adhesion with the leadframe compared with the compounds. This is due to the fact that die-attach materials are chemically tuned to adhere to surface finishes on leadframes. For DA2 the interface fracture toughness is even more that 200% times higher than for DA1. This is an effect of a different chemistry. Again, when moisture is presented at the interface, the adhesion strength may decrease to 50%.

Table 4.7: Interface fracture toughness for the different variations and conditions.

	Interface Fracture Toughness [J/m^2]	
Sample ID	**Dry**	**Wet**
Moulding Compound		
MCA, 20ºC	5.7	3.2
MCA, 85ºC	5.8	-

	Interface Fracture Toughness [J/m^2]	
Sample ID	**Dry**	**Wet**
MCA, 150ºC	5.1	-
MCB, 20ºC	6.2	5.9
MCC, 20ºC	6.9	-
MCD, 20ºC	14.8	7.3
MCA, 20ºC with LF oxidation	2.5	1.9
Die-attach		
MCA + DA1, 20ºC	10.5	-
MCA + DA2, 20ºC	24.0	13.1

The same sample and material set up is used to perform two other interface characterization tests: modified ball-on-ring and three point bending test. For the modified ball-on-ring, a hole with a 3mm diameter is drilled into the moulding compound until the interface is reached, see Figure 4.17. The amount of delamination is measured via C-SAM. A stainless steel cylindrical shaft with a diameter of 3mm is attached to the load cell of a universal testing-machine. The specimen with the hole facing up is put on a ring support of diameter 30mm, so that the path of the shaft will not be obstructed. The shaft is adjusted to just touch the leadframe of the specimen. A crosshead speed of 100mm/min is set on the universal testing-machine to avoid any dynamic effects. The applied load versus shaft displacement is recorded simultaneously throughout the entire loading process. The critical loads needed to propagate the crack are recorded and used afterwards to calculate the interfacial strength using 2D axi-symmetric and full 3D FE models. In the FE models, the J-integral at the crack-tip with from CSAM measured initial crack-length is computed and thermal and hygro-mechanical properties are taken into account. Using the FE models a mode mixity of 64.8º is calculated for this set-up. Three experiments are conducted using MCA, at a temperature of 20ºC and an initial crack length of 4mm, 6mm and 7mm respectively. Combined with the numerical calculations this yielded an interface fracture toughness of 25J/m^2, 24J/m^2 and 27J/m^2, revealing an average value of 25.3±1.3J/m^2.

For the three point bending test the same samples as used in the four point bending test are used. But in this case an initial crack is created in one of the far ends of the bar-shaped samples. During consecutive loading and unloading the crack length is measured. Nine experiments are conducted using MCA, at a temperature of 20ºC. Using 2D FE models a mode mixity of 83º is calculated for this set-up. Combined with numerical calculations this yielded an interface fracture toughness of 26J/m^2, 27J/m^2, 28 J/m^2, 28J/m^2, 30J/m^2, 31J/m^2, 32J/m^2, 36J/m^2, 38J/m^2, revealing an average value of 30.7±3.9 J/m^2.

Combining the four point bending, modified ball-on-ring and three point bending test results show an increasing interface toughness with increasing mode mixity, which is expected.

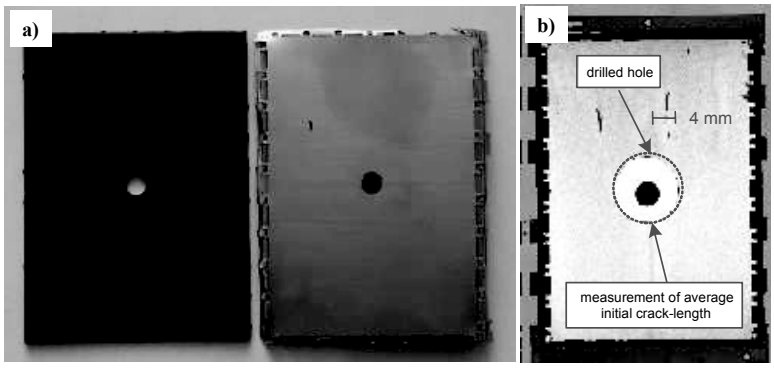


Figure 4.17: a) Geometry of the modified ball-on-ring sample and b) CSAM result indicating the initial crack size.

The adhesion strength between leadframe and epoxy materials is characterized. Based on standard semiconductor designs, processes and materials, specimens are created. Interface strength values as function of temperature, moisture, storing conditions and mode mixity are presented. Using interface characterisation results, numerical simulations are preferred to obtain (correct) interface toughness values. For the investigated compound - leadframe interface, the strength is found to moderately depend on temperature but strongly dependent on storing conditions, moisture and mode mixity. The results also indicate that a proper characterisation of interface strength between two materials as function of process conditions, temperature, moistures and mode mixity involves the use of different test set-ups. There are two reasons why interface strength values within microelectronics devices are needed. First of all, and the most obvious one, the values are needed as an input for FEM

exercises to enable the prediction of delamination. Secondly, proper interface characterisation methods can be used as a method to select your materials a priori. Per today, material selection procedure for microelectronics devices are strongly trial-and-error and experience based. A number of materials is selected based on material expert experience, with the input from the supplier. After this selection, full qualification tests will be executed, which can take about 3-6 months before a final Bill of Material (BOM) is fixed. If interface strength values per selected material and interface are part of this procedure, this will for sure decrease the time spend on material qualification tests. Chapter 8 consists of an application where the presented adhesion results are used.

4.4 Characterization and Prediction of Moisture Driven Failures

Moisture related failures in microelectronics devices are one of the most important failure mechanisms in microelectronics [Fan *et al.*, 2006]. The presence of moisture in the device alters the stress levels through alteration of thermo-mechanical properties, induces hygroscopic stress through differences in swelling, induces vapour pressure, reduces interfacial strength, induces corrosion and alters dielectric properties of materials. Well known moisture driven failure modes are popcorn, delamination and excessive warpage. Moisture sensitivity levels were introduced as one of the major qualification tests, see Chapter 2. This section describes the characterization and prediction of microelectronics failures under moisture conditions.

4.4.1 Characterization of Moisture Properties

Polymeric materials transport moisture primarily by diffusion, following Fick's law:

$$\frac{\partial^2 C}{\partial x^2}+\frac{\partial^2 C}{\partial y^2}+\frac{\partial^2 C}{\partial z^2}=\frac{1}{D}\frac{\partial C}{\partial t} \qquad (\mathbf{4.20})$$

With C the local moisture concentration in g/m^3 and D the moisture diffusivity in m^2/s. As time progresses, moisture ingression into polymeric materials tend to a saturated concentration, C_{sat}. The moisture absorption properties D and C_{sat} can be determined by measuring the weight gain (or loss in case of desorption) as a function of time. For a rectangular bar, an analytical expression for the total weight gain as a function of time is obtained by integrating the local concentration over the volume of the rectangular sample:

$$\frac{\mathrm{M_t}}{\mathbf{M_{sat}}} = 1 - \frac{512}{\pi^6}\sum_{l=0}^{\infty}\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\left\{\frac{e^{[-k^2 Dt]}}{(2l+1)^2(2m+1)^2(2n+1)^2}\right\}$$

with : (**4.21**)

$$\mathrm{k}^2 = \left\{\left(\frac{(2l+1)\pi}{x_0}\right)^2 + \left(\frac{(2m+1)\pi}{y_0}\right)^2 + \left(\frac{(2n+1)\pi}{z_0}\right)^2\right\}$$

Here x_0, y_0 and z_0 denote the size of the rectangular sample, M_{sat} the saturation mass increase and l, m and n are the summing integers. The material properties are determined by minimizing the difference between the analytical expression and the experimental weight gain versus time using least square methods.

For moulding compounds, a specially developed mould is used to create rectangular samples of 90x4.5x2mm^3 and 50x9x2mm^3 sizes. For die-attach materials, a silicone block with a 50x9x2mm^3 opening is used in which the material can be cured. For substrate materials, a sample geometry of 75x9.8x0.57 mm^3 is obtained by a sawing process. Weight gain measurements are performed following a standard procedure:

1. Samples are first put in dry-bake at 125°C for 24 hours.
2. After dry-bake, weight of samples is measured.
3. Samples are put into a humidity-temperature chamber.
4. At specific time steps (0, 2, 4, 6, 8, 24, 48, 72, 144, 168, >168 hours) moisture weight gain is measured of a sample.

Absorption measurements are performed under both MSL1 and MSL3 conditions. To obtain a saturated moisture concentration in the sample under MSL3 conditions, longer measurement times are needed than for MSL1 conditions. Equation 4.21 is used to obtain C_{sat} and D. Figure 4.18 shows an example results of a fitted and measured moisture weight gain under MSL1 and MSL3 conditions. The analytical fit is considered to be quite good. Material moisture diffusion data for several compounds, one die-attach and substrate material are listed in Table 4.8. The activation energy between MSL1 and MSL3 for the diffusion coefficient is calculated using the Arrhenius equation , according to:

$$\mathrm{D(T)} = \mathrm{D_o}\exp\left(-\frac{\mathrm{E_a}}{\mathrm{kT}}\right) \quad (\mathbf{4.22})$$

With D_o the pre-exponential factor for fitted line (mm^2/s), E_a the activation energy (eV) and k the Boltzman's constant ($8.617x10^{-5}$ eV/°K). The data in Table 4.8 shows that for the chosen materials C_{sat} values are in the order of 10^{-2} to $10^{-4}mg/mm^3$ with higher values for the FR4 material. For the moisture diffusivity, D, for ranges are 10^{-6} to $10^{-7}mm^2/s$, with highest values for the die-attach. Typical activation energies for compounds are in the order of 0.30 to 0.45eV.

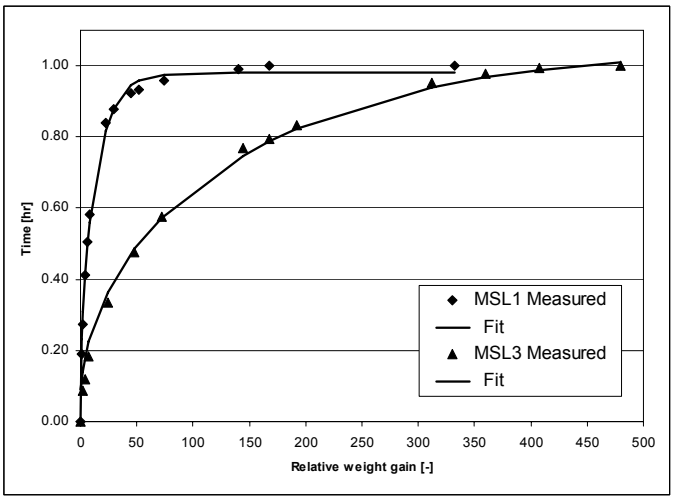


Figure 4.18: Fitted and measured moisture weight gain for MSL1 and MSL3.

Polymeric materials swell when moisture is absorbed. Differential swelling occurs between the different constituents within the microelectronics device. The amount of swelling is linearly proportional to the moisture concentration as:

$$\varepsilon_h = \beta \cdot C \qquad (\mathbf{4.23})$$

With ε_h the hygroscopic strain, β [mm^3/mgr] the coefficient of moisture expansion (CME) and C [mgr/mm^3] the moisture concentration. The CME is measured using the combined Thermal Gravimetric Analyser (TGA) and Thermal Mechanical Analyser (TMA) technique [Wong *et al.*, 2002, Tee *et al.*, 2003]. Using this technique, moisture is desorbed in two identical samples at a constant temperature and change of mass (TGA) and dimension (TMA) as function of time are measured. The change in thickness dimensions can be calculated from the TMA readings, the change in weight from the TGA readings. By combining both the TMA and TGA measurements, the CME can be determined from the slope of the data set. Since the moisture desorption

can take some time, the TGA and TMA tests need to run for at least 1000 minutes. For all materials, a temperature of 85°C is used to determine the CME. Material moisture expansion data for several compounds, one die-attach and substrate FR4 material are listed in Table 4.8. For compounds, expansion values are in the range of 0.3 to 0.5 mm^3/mgr, for the die-attach a factor 2 higher For the FR4 material the CME depends on the direction, in the out-of-plane direction it is 5 times higher.

Table 4.8: Material properties for moisture diffusion and expansion.

	C_{sat} [mg/mm3]		**D [mm2/s]**		**E_a [eV/K]**	**CME [mm3/mgr]**
Material	**MSL1**	**MSL3**	**MSL1**	**MSL3**		**85ºC**
Moulding Compounds						
MCA	$3.6\cdot10^{-3}$	$1.8\cdot10^{-3}$	$1.6\cdot10^{-6}$	$2.4\cdot10^{-7}$	0.32	0.46
MCB	$5.0\cdot10^{-3}$	$2.5\cdot10^{-3}$	$1.2\cdot10^{-6}$	$1.7\cdot10^{-7}$	0.34	0.35
MCC	$6.2\cdot10^{-3}$	$3.1\cdot10^{-3}$	$2.3\cdot10^{-6}$	$3.2\cdot10^{-7}$	0.33	0.29
MCD	$3.7\cdot10^{-3}$	$1.7\cdot10^{-3}$	$1.7\cdot10^{-6}$	$2.9\cdot10^{-7}$	0.30	0.33
MCE	$1.3\cdot10^{-2}$	$7.8\cdot10^{-3}$	$6.9\cdot10^{-6}$	$5.3\cdot10^{-7}$	0.44	0.21
MCF	$3.6\cdot10^{-3}$	$1.4\cdot10^{-3}$	$1.7\cdot10^{-6}$	$2.6\cdot10^{-7}$	0.32	0.19
MCG	$4.6\cdot10^{-3}$	$1.5\cdot10^{-3}$	$2.4\cdot10^{-6}$	$2.9\cdot10^{-7}$	0.36	0.34
MCH	$5.2\cdot10^{-3}$	$2.8\cdot10^{-3}$	$1.2\cdot10^{-6}$	$1.8\cdot10^{-7}$	0.33	0.29
*Die-attac*h						
DA1	$3.8\cdot10^{-3}$	$2.9\cdot10^{-3}$	$7.0\cdot10^{-6}$	$5.4\cdot10^{-6}$	-	1.0
Substrate						
FR4 in-plane out-of plane	$1.1\cdot10^{-2}$	$6.5\cdot10^{-3}$	$1.7\cdot10^{-6}$	$2.3\cdot10^{-7}$	0.34	 0.066 0.38

4.4.2 Prediction of Moisture Driven Failures

Since the discovery of moisture failures much effort has been devoted to the prediction of moisture induced failure mechanisms. A multi-physics FE methodology which can take into account the moisture and thermo-mechanical related mechanisms is required in order to simulate the observed failure mechanisms. Two types of simulations are needed, namely the moisture diffusion modelling and the hygro-

thermal-mechanical modelling. Most commercial FE software are not directly equipped with the capability to model moisture diffusion in microelectronics devices. However, because transient moisture diffusion follows the same governing differential equations as the diffusion of heat, the thermal analogy can be employed to model moisture diffusion. A particular problem arises, however, due to the discontinuity of moisture concentrations at a material interface which is inconsistent with a numerical method. To overcome this problem the 'wetness' approach [Wong *et al.*, 1998] is used, which assumes continuity of the weighted moisture concentration across interfaces of different materials. The wetness is defined as:

$$w = \frac{C}{C_{sat}} \tag{4.24}$$

Which is equivalent to Galloway's [1997] solubility approach [Fan *et al.*, 2006]. Using the wetness approach, the moisture diffusion implementation in a commercial FE software is becoming straightforward using so-called user subroutines. Figure 4.19 shows a comparison between predicted and measured moisture content for a series of substrate-based and leadframe-based packages after 168hrs of MSL3 conditions. The measured results are the outcome of a moisture sensitivity assessment. For the substrate-based family, 2D and 3D FE models are compared showing a 10% mismatch using the 2D models and a <5% mismatch for the 3D models. The result for the leadframe-based family, also show that an accuracy within 5% for the moisture content can be calculated when using 3D FE models.

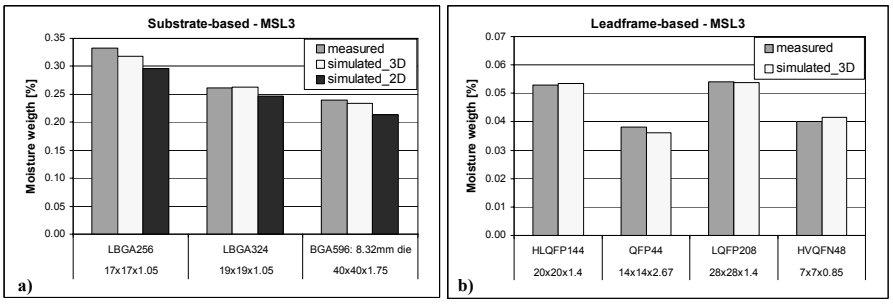


Figure 4.19: Predicted versus measured moisture content under MSL3 conditions for a) substrate- and b) leadframe-based packages.

Moisture ingression induces hygroscopic swelling stresses in the device, which adds to the thermal stress. For the hygro-thermal-mechanical modelling, the predicted

temperature and moisture concentration fields are used as input for the total stress predictions. The total strain is a summation of the thermal strain ε_t and the hygroscopic strain ε_h:

$$\varepsilon = \varepsilon_h + \varepsilon_t = \beta \cdot C_{sat} \cdot W + \alpha \cdot \Delta T \qquad (\mathbf{4.25})$$

With α the CTE and β the CME of the material. Due to the temperature-moisture analogy, the available transient temperature field capabilities within a commercially available FE code are used for solving the moisture field. Because a coupling with the temperature field should also be present, a duplicate mesh is used. Using two identical meshes allows the simultaneous solution of both temperature- and moisture fields. One mesh represents the temperature field and the other mesh the moisture field. The moisture concentration will cause hygro-swelling strains, which together with the thermal strains will result in the total strain, again using a user subroutine. This subroutine allows a manual summation of the thermal strains and the moisture strains for each integration point.

At temperatures above 100˚C, water that is present in the polymeric materials will evaporate. During further heating, the resulting vapour will introduce a vapour pressure in the pores of the material and at delaminated areas. This vapour pressure will not only result in swelling of the polymeric materials due to the internal pressure, but will also results in an additional loading on the existing delaminated areas. The vapour pressure as function of temperature can be found in many handbooks. In the simulations the vapour pressure is placed on the delaminated edges, as an edge load which depends upon temperature. No dependency upon the moisture concentration at the interface is assumed.

Chapters 7 and 8 consist of an application of moisture induced failure prediction using the material properties and numerical methods described above.

Chapter 5

Response Surface Modelling for Non-linear Packaging Stresses [1]

This chapter focuses on the development of reliable Response Surface Models (RSM) for the major packaging processes of a typical microelectronics package. The major objective is to optimise the product/process designs against the possible failure mode of vertical die crack. First, the FEM-based physics of failure models are developed and the reliability of the predicted stress levels was verified by experiments. In the development of reliable thermo-mechanical simulation models, both the process (time and temperature) dependent material non-linearity and geometric non-linearity are taken into account. Afterwards, RSMs are constructed which cover the whole specified geometric design spaces. Finally, these RSMs are used to predict, evaluate, optimise and, eventually qualify the thermo-mechanical behaviour of this microelectronics package against the actual design requirements prior to major physical prototyping and manufacturing investment.

5.1 Introduction

Thermo-mechanical reliability of microelectronics packages is one of the major concerns in the microelectronics industry. Critical stress levels can be reached in the package constituents during the thermal and mechanical processing and testing, causing various failures. This is expected to become even more critical in future products due to further miniaturization and function integration, which causes increased power dissipation, higher interconnection density and higher reliability demands. To face those challenges, much effort has been spend to develop a strategy and methodology of virtual thermo-mechanical prototyping of microelectronics packages by:

- Developing reliable and efficient FEM-based physics of failure prediction models.
- Developing advanced simulation-based optimisation methods.
- Integrating them into an unified virtual thermo-mechanical prototyping procedure.

[1] Reproduced from: van Driel, W.D., G.Q. Zhang, J.H.J. Janssen, L. J. Ernst, Response Surface Modelling for Non-linear Packaging stresses, Journal of Electronic Packaging 125 (4), pp. 490-497, 2003.

The results of virtual thermo-mechanical prototyping can be used to predict, evaluate, optimise and eventually qualify the thermo-mechanical behaviour of microelectronics packages against the actual package requirements prior to major physical prototyping and manufacturing investments, aiming at the realization of "Optimised Designing in Reliability". As a first step to realize such an "Optimised Designing in Reliability", the development of reliable and efficient FEM prediction models for the process-induced stress levels is vital. The packaging processes are strong non-linear, including material non-linearity's, such as visco-plasticity, creep and/or elasto-plastic behaviour; geometric non-linearity's, such as large deformation; and boundary non-linearity's, such as edge and contacting effects. Reliable and efficient FEM-based thermo-mechanical prediction models can only be obtained if such non-linearity's are taken into account. This chapter presents our simulation methods, models and results that are reliable for the specified design space, concluded by the verification results. Secondly, as one of the major building blocks of virtual thermo-mechanical prototyping, reliable Response Surface Models (RSM) should be generated. In this chapter, RSMs are developed using leadframe and die-attach thickness, in this case a solder die-attach material, as part of the design variables and targeted at the critical failure mode of vertical die crack. Using these RSMs, the trend of packaging induced die stresses and eventually the "Optimised Designing in Reliability" rules can be obtained.

5.2 Reliable FEM-based Physics of Failure Models

The chosen microelectronics package consists of a silicon die, attached to the leadframe by using a soft solder as die-attach material and in a later packaging stage encapsulated by a moulding compound. Table 5.1 lists both the nominal geometric design values and design space for all constituents.

Table 5.1: Geometric parameters and variations.

Parameter	**Nominal Value [mm]**	**Variations [mm]**
Compound		
length	6.5	None
thickness	2.3	None

Parameter	Nominal Value [mm]	Variations [mm]
Die		
length	4.3	None
thickness	240 μm	None
Leadframe		
length	5.3	None
thickness	0.6	0.2 – 1.0
Solder Die-Attach		
length	4.3	None
thickness	50 μm	20 – 80 μm

Different element types, i.e. generalized plain strain and axi-symmetric ones, are used and compared to a full 3D model in order to obtain the best approximation for the real 3D stress situation. The predicted stress results using an axi-symmetric element description were found to match best with the reality, see also Kelly [2000]. Figure 5.1 shows the 2D axi-symmetric FE model with local element refinery. The effect of element sensitivity is studied extensively by using several distributions and/or discretizations. Notice that in the final model, five elements in vertical direction (y) is used for the thin solder die-attach layer. In total, the model consists of approximately 15,000 4-noded elements.

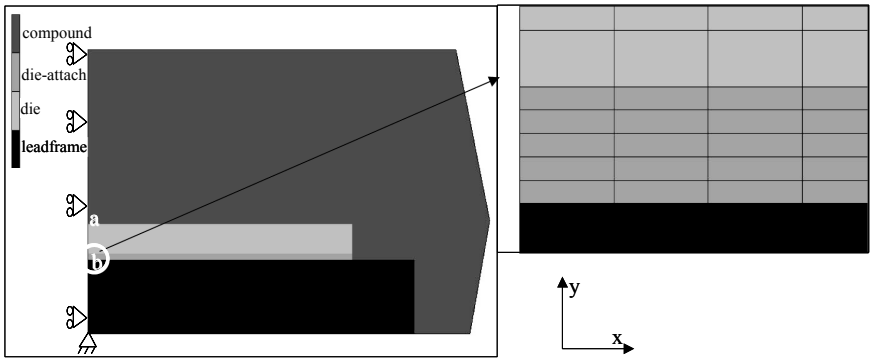


Figure 5.1: 2D axi-symmetric FE model for the package.

The used boundary conditions are also illustrated by Figure 5.1. The displacement in x-direction is fixed along the symmetry axis and the node at the left bottom corner is fixed in both x- and y-directions.

The single crystal silicon die is modelled as a linear elastic material, the leadframe material as an ideally elasto-plastic material, see Chapter 4. For the leadframe, both the Young's modulus and the yield stress are temperature dependent, see Figure 5.2a. For the used moulding compound, the material data are provided by the supplier and are modelled as a linear elastic material where both the Young's modulus E and the coefficient of thermal expansion α are temperature dependent, see Figure 5.2b. The Poisson's ratio for the compound is estimated as 0.33. All material properties are listed in Table 5.2.

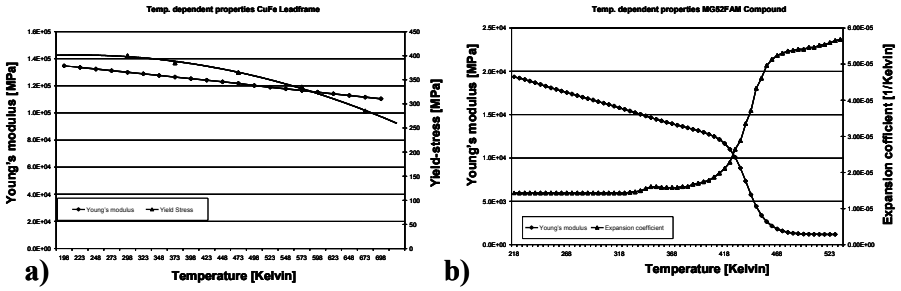


Figure 5.2: Temperature dependent properties for a) the leadframe, Young's modulus and Yield stress and b) compound, Young's modulus and CTE.

A visco-plastic model including creep and work hardening is used for the soft and thin solder die-attach layer, where both the elastic modules and the yield stress are temperature dependent, see Figure 5.3. The Poisson's ratio for the solder die-attach is estimated as 0.4, the coefficient of thermal expansion as 29e-6 /K. The creep behaviour is described as [Darveaux and Banerji, 1998]:

$$\dot{\varepsilon}^{cr} = A(\sigma)^n \exp(-\Delta H / RT) \qquad (\mathbf{5.1})$$

With

$$A = 1.142*10^{10}\ [-],\ \Delta H = 1.25*10^{5}\ [\text{eV}],\ R = 8.3143\ [\text{J mol}^{-1}\ \text{K}^{-1}]$$

$$n = \begin{cases} -2.043*10^{-2}*T + 10.36 & \text{if } T \le 458\ \text{Kelvin} \\ 1.0 & \text{if } T > 458\ \text{Kelvin} \end{cases} \qquad (\mathbf{5.2})$$

Table 5.2: Material inputs.

Material	E [MPa]	ν [-]	CTE [ppm/K]	Type
Die	169000	0.23	2.3	Elastic
Leadframe	Figure 5.2a	0.35	17	Ideally elasto-plastic
Compound	Figure 5.2b	0.33	Figure 5.2b	Temperature dependent
Solder Die-Attach	Figure 5.3	0.4	29	Visco-plastic

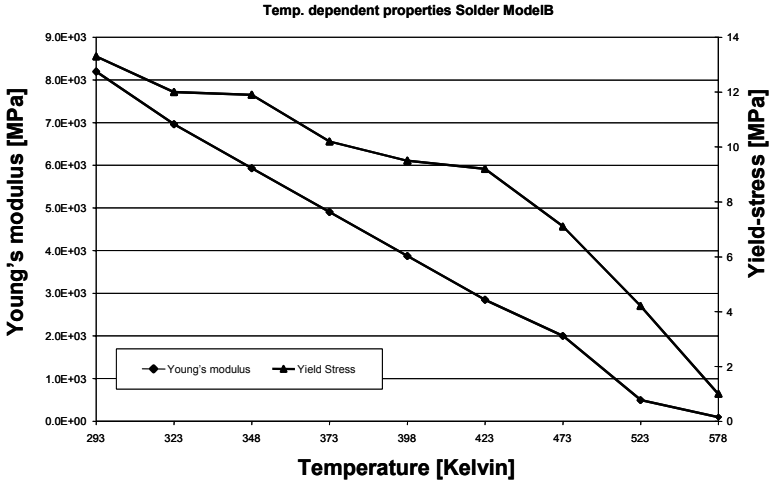


Figure 5.3: Temperature dependent Young's modulus and Yield stress for the solder die-attach.

For the studied package, two packaging processes (die-attachment and moulding) and temperature cycling testing conditions are considered. The simulated processes are shown in Figure 5.4. Notice that the grey points indicate the process locations at which the process-induced die stresses are studied.

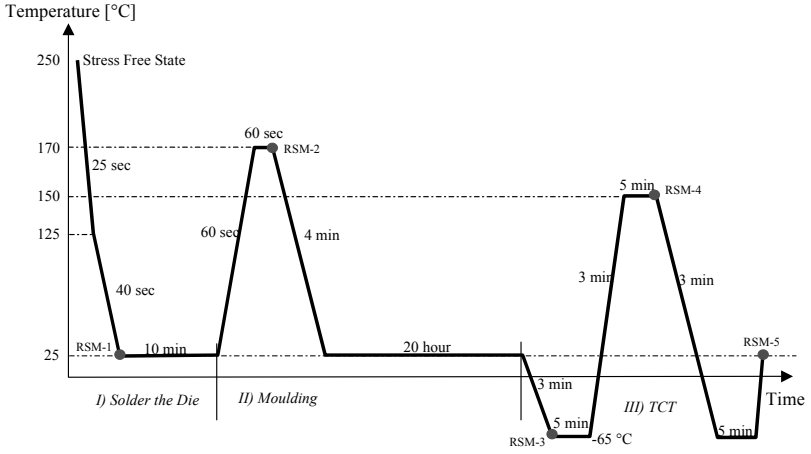


Figure 5.4: Major Packaging Process Specification.

To develop reliable and efficient non-linear thermo-mechanical prediction models for the product/process designs of microelectronics packaging, various justified simplifications and assumptions are commonly used:

- The stress free state for the die, solder die-attach and leadframe are defined as 250°C, which is the melting-solid transition temperature of the solder die-attach. The stress free state for the moulding compound is defined as 170°C. During the die-attachment process, all elements of the moulding compound are deactivated and they are activated during the encapsulation process.
- Isothermal loading conditions are used for the modelling of both the packaging process and temperature cycling testing conditions.
- The initial die warpage/stress is neglected.
- Perfect adhesion is assumed between the die and leadframe and between the die and moulding compound.

5.3 Results for Nominal Design

The maximum stresses in x direction at the bottom and top of the die surface are used as the failure index for vertical die crack (indicated in Figure 5.1 by point a and b). If the calculated stress level is close to/higher than the allowable tension stress of approximately +150MPa, or close to/lower than the allowable compressive stress of approximately –600MPa, the vertical die crack is likely to occur [Wu *et al.*, 2003]. The following trends are observed for the two studied packaging processes:

- *Die-attachment*

Due to the mismatch in coefficients of thermal expansion between the die and leadframe, cooling down from die-attachment temperature to room temperature will result in downwards bending of the die, due to more thermo-shrinkage of the leadframe, see Figure 5.5. Thus, there will be tensile stresses at the top of the die and compression stresses at the bottom of the die. The stress levels depend strongly on the thickness of the leadframe: increasing the thickness will result in changing from tension to compressive stresses for the die top surface. The resulting stress levels during this process are in the order of +200 to –300MPa for the specified design space.

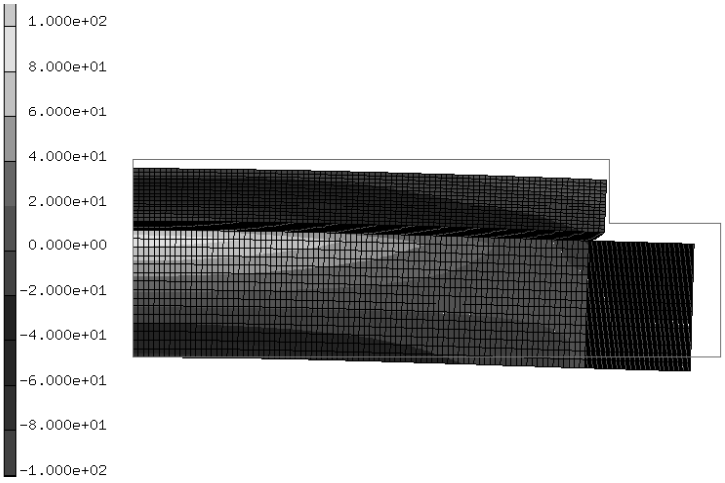


Figure 5.5: Horizontal stress distribution after die-attachment at 25°C.

- *Encapsulation*

During the encapsulation process, the die, solder die-attach and leadframe are heated from room temperature to the temperature at which the moulding compound is added. The elements of moulding compound are activated at this temperature. Figure 5.6 shows the horizontal stress distribution in the die directly after moulding at 170°C. Due to the warming up process the die bends upwards, indicating that plastic deformations have occurred, see Figure 5.6. Still tensile stresses occur at the top of the die surface. However, the stress levels after the encapsulation process are lower compared to those after die-attachment. The resulting stress levels at the die top surface at this process are in the order of +50 to –50MPa for the specified design space.

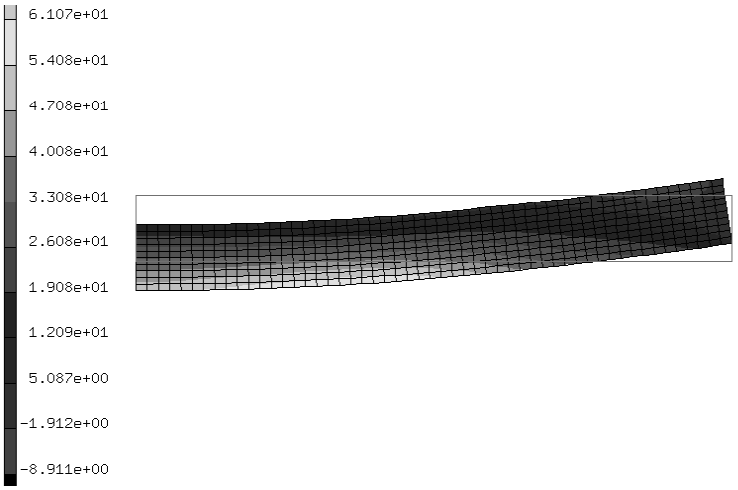


Figure 5.6: Horizontal stress distribution after moulding at 170°C.

- *Temperature Cycling Testing*

During temperature cycling, a temperature drop to –65°C is followed with a temperature rise to 150°C. Cooling down to –65°C results in a compression of the package. Figure 8 shows the horizontal stress distribution in the die after the temperature drop to –65°C. Since there is more compound above the die compared to below it, this results in an upward bending of the die, as illustrated in Figure 5.7. Typical stress levels in the centre of the die for top and bottom –65°C are in the order of –400 to –500MPa. These levels are the highest compressive stresses found at both top and bottom side of the die surface during the complete packaging process.

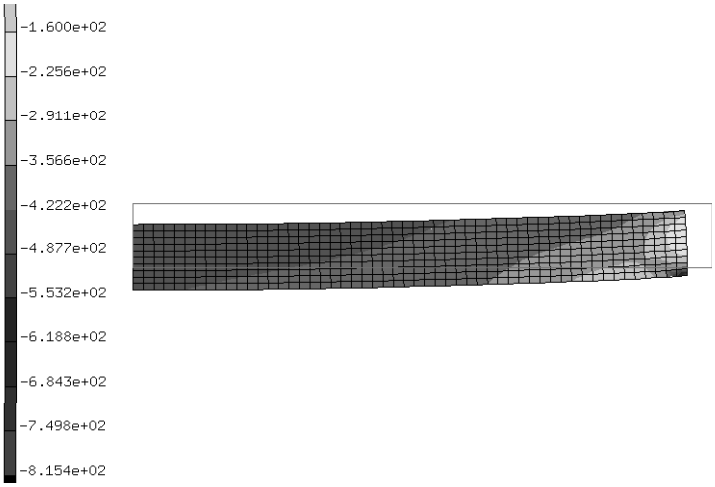


Figure 5.7: Horizontal stress distribution after temperature cycling at -65°C.

- *Edge effects*

Edge effects due to thermal mismatch in microelectronics packages have been investigated extensively in the past, see [Eischen *et al.*, 1990]. In the simulations presented here, the edge effect was assumed to be the root cause for higher stress levels at the boundary of the die. To investigate the relevance of this edge effect, the results obtained from the nominal package model is compared with those obtained from a model with a different leadframe-die configuration, i.e. the leadframe having the same length as the die. Figure 5.8 shows the horizontal stress versus the relative distance (from centre to the edge of the die top surface) for the nominal model and the model with same length for die and leadframe after die-attachment at 25°C. From the centre to the edge of the die, the horizontal stress changes from compressive to tensile for this specific packaging process. The figure demonstrates that the edge effect at the top die surface is always located on the same distance from the edge, in this process at approximately 85% from the centre. Besides this, the edge effect results in identical horizontal stress levels at the die top surface for both cases, indicating that the effect is independent on the die-leadframe length.

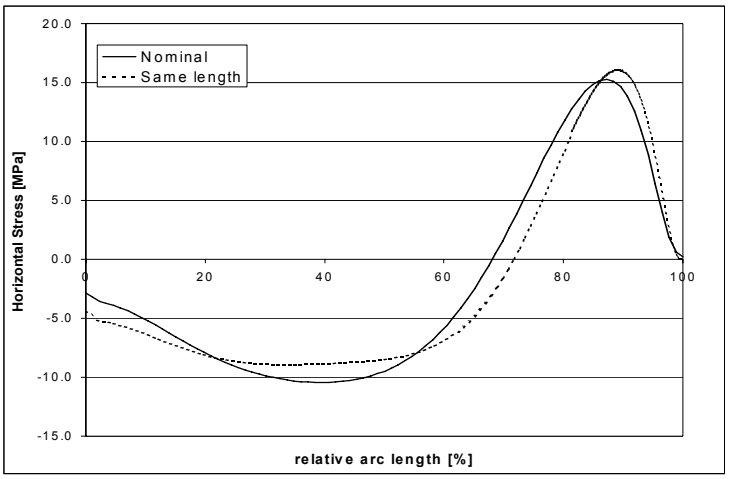


Figure 5.8: Horizontal stress along the top of the die surface from centre to edge for the nominal model and a model with same length for die and leadframe after die-attachment at 25°C.

- *Non-linear effects: Yielding of leadframe*

Figure 5.9 shows the distribution of the Von Mises stress in the leadframe after temperature cycling at -65°C for two leadframe configurations: the nominal design

with a thickness of 0.6mm and a new design with a thickness of 0.2mm. For the nominal leadframe, the maximum stress levels are far away from the yielding stress level of leadframe material (400MPa), however, plastic yielding occurs at the indicated area for the thin leadframe. Figure 5.9 demonstrates that the occurrence of plastic yielding strongly depends on the leadframe thickness.

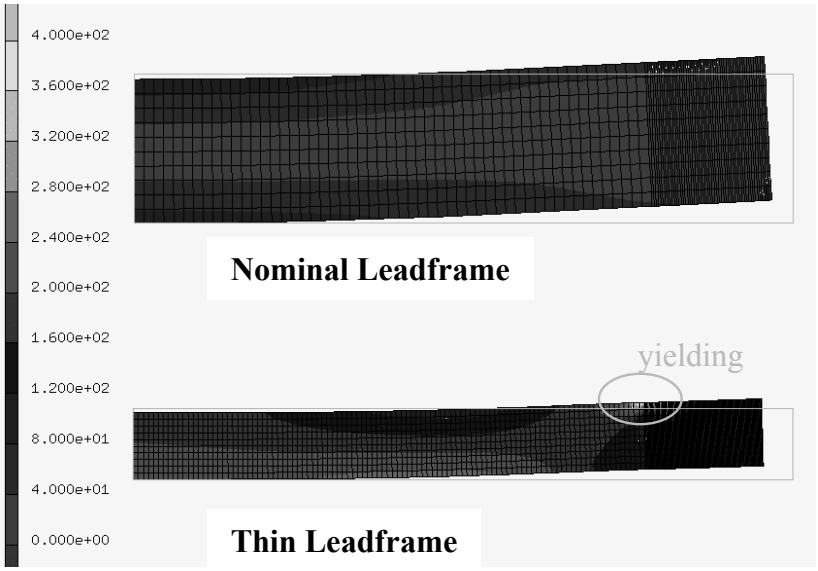


Figure 5.9: Von Mises Stress distribution in the leadframe after temperature cycling.

- *Non-linear effects: Solder Creep*

In general, the creep of the solder results in a reduction of the die stress levels. The following conclusions are observed for the different packaging and testing processes. During the die-attachment dwell period of 30min. after the soldering process at 25°C, the horizontal stress component at the bottom of the die centre (point b in Figure 1) is reduced from –126MPa to –111MPa, which is about 10%. After the moulding process, a major stress reduction to zero occurs after a dwell period of 20 hours at 25°C. The horizontal stresses are reduced from –345MPa to –287MPa for the die centre at the bottom and from –395MPa to –384MPa for the die centre at the top. Figure 5.10 shows the effect of the solder die-attach creep during the packaging process of temperature cycling from –65°C to +150°C. The figure shows the horizontal stress evolution at the top and bottom of the die centre. The strongest stress reduction (about 10%) occurs during the dwell period.

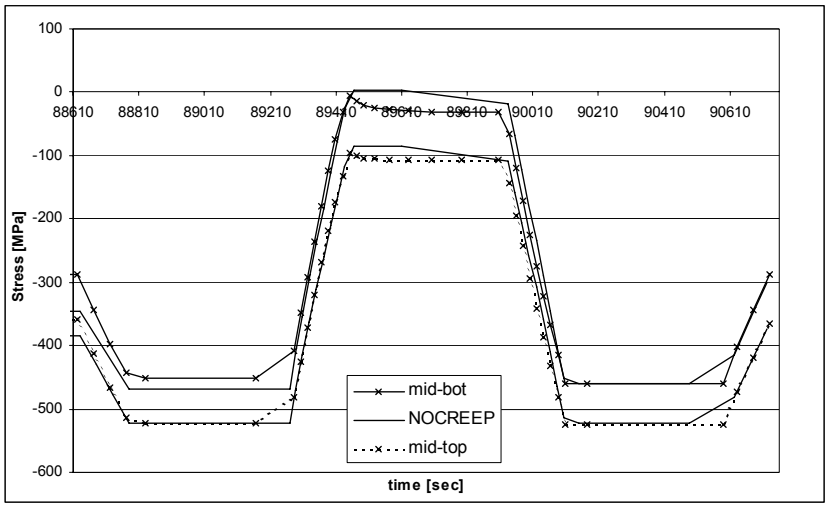


Figure 5.10: Effect of solder die-attach creep during temperature cycling: horizontal stress evolution at the mid-top and mid-bottom of the die.

- *Model Verification*

The developed thermo-mechanical simulation models are compared with experimental results for a typical microelectronics package using different techniques:

- 3D Moiré interferometry to verify the die and package deformations, see Chapter 4;
- micro-Raman spectroscopy to verify the die stress levels [Chen *et al.*, 2000; Chen and De Wolf, 2002]

Measurements are performed on samples of a real microelectronics package and naked dies attached on a leadframe. Dedicated FE models are created to represent the sample geometry and loading history during testing. The study clearly showed the quantitatively match between the tested and predicted results. It is concluded that the models are reliable for the specified product/process designs.

5.4 Response Surface Modelling and Optimisation

Simulation-based optimisation is based on and integrated with advanced simulation models that can predict the product/process behaviour reliably and efficiently. Simulation-based optimisation of packages involves finding settings for a number of packaging design parameters that are optimal with respect to several simulated response characteristics/response parameters of the packages. Since there are many

possible design parameter settings and non-linear FEM simulations are often time consuming, the crucial question becomes how to find the best possible parameter setting with a minimum number of simulations. Many papers describe direct optimisation procedures to obtain optimal parameter settings in such situations [Toropov *et al.*, 1993; van Keulen and Toropov, 1997]. Disadvantage of these approaches is that little insight is obtained for the behaviour of the responses in terms of the complete design space. Moreover, when the optimisation problem changes (e.g., changing in the bound on a response parameter), the optimisation procedure has to be restarted. This chapter uses a newly developed optimisation strategy and method as described in Chapter 3. This strategy focuses on the development of a reliable response surface for the underlying non-linear response by integrating the adaptive (sequential) Design Of Experiments with advanced RSM methodologies. Once the RSM has satisfied the specified accuracy criteria, various types of design optimisations can be carried out efficiently.

- *DOE*

A space-filling Latin Hypercube design consisting of 25 design variations is first constructed. Table 5.3 shows the two design parameters, i.e. leadframe and solder die-attach thickness (see Table 5.1 for the defined design spaces). Using the parametric non-linear FEM models, FEM simulations are carried out for all the 25 designs, and the Die Top Stress (point a in Figure 5.1) and Die Bottom Stress (point b in Figure 5.1) are used as the response parameters. The design optimisation problem is to choose the geometry parameters of the package such that the Die Top and Bottom stress levels are close to zero, within the specified ranges of design variations.

Table 5.3: Latin-Hypercube scheme of 25 package designs.

	Design Parameters	
Nr.	**Leadframe Thickness [mm]**	**Solder Die-Attach Thickness [μm]**
1	0.257	54
2	0.771	20
3	0.200	37
4	0.543	76
5	0.657	46

	Design Parameters	
Nr.	**Leadframe Thickness [mm]**	**Solder Die-Attach Thickness [μm]**
6	0.429	41
7	0.943	33
8	0.886	50
9	1.000	67
10	0.314	71
11	0.600	29
12	0.829	80
13	0.714	63
14	0.371	24
15	0.486	59
16	0.284	26
17	0.579	52
18	0.747	39
19	0.916	61
20	0.453	74
21	0.967	23
22	0.233	65
23	0.633	78
24	0.800	28
25	0.333	47

- *RSM MODELLING*

Model Choice: RSM models are generated at 5 loadsteps, as indicated in Figure 5.4. For both top and bottom die stresses, as a start, quadratic models with interactions are used for RSM generation. Using automatic pruning procedures based on cross-validation, the unimportant model terms were deleted. The regression statistics are listed in Table 5.4, indicating that for some quadratic models the reliability and accuracy requirements are not satisfied. Since these models are not accurate enough, more reliable RSM method, such as Kriging models were applied. When Kriging models are applied in these cases, significant improvement on the resulting regression

is obtained. In Figure 5.11 the simulated top and bottom stresses versus the predicted ones are plotted, showing the accuracy of the stress prediction using the developed RSM model. Figure 5.12 shows an example of RSM plot, indicating that some responses can not be reliably described by a quadratic function.

Table 5.4: Compact model regression statistics.

	Quadratic		**Kriging**	
RSM	***RMSE***	***cv-RMSE***	***RMSE***	***cv-RMSE***
Top1	7.64	10.45		
Top2	7.35	9.23	0.15	1.53
Top3	9.32	11.85		
Top4	7.51	9.07		
Top5	7.69	9.66	0.89	3.71
Bot1	6.51	9.23		
Bot2	5.11	6.95		
Bot3	7.30	8.73		
Bot4	10.20	12.17	0.00	2.43
Bot5	9.76	11.94	0.41	2.65

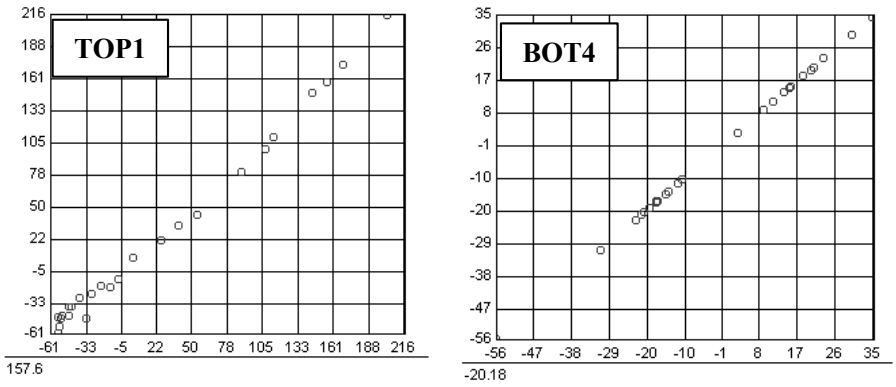


Figure 5.11: Simulated vs. predicted stress: Quadratic (left) and Kriging Model (right).

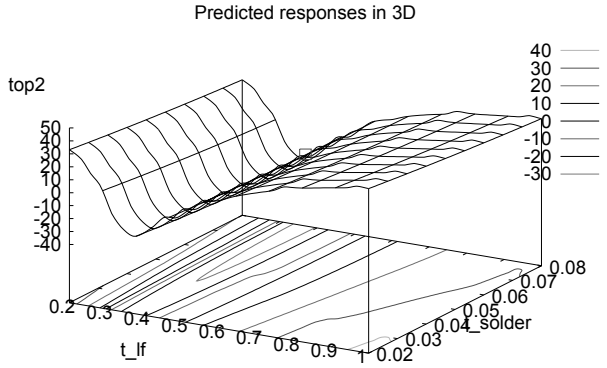


Figure 5.12: Example RSM plot; *t_lf* refers to leadframe thickness, *t_solder* to solder die-attach thickness.

- *Test Case*

As a test case for the generated RSM models, the nominal case with solder die-attach thickness of 50 μm and leadframe thickness of 0.6mm is taken. Table 5.5 shows the results for the stress levels at the centre of the die. Again, for some responses, quadratic models are sufficient, for others more flexible model types like Kriging models are needed. In general, the relative deviation between the FEM results and the results obtained from the RSM are less than 10%.

Table 5.5: Test case: nominal FEM results versus RSM results.

		RSM	
	FEM	Quadratic	Kriging
RSM1 Top	-9.5	-10.0	
Bottom	-144.1	-143.3	
RSM2 Top	10.3	8.3	9.5
Bottom	55.2	55.3	
RSM3 Top	-531.9	-531.1	
Bottom	-473.9	-465.7	
RSM4 Top	-86.2	-88.1	
Bottom	8.2	11.2	9.2
RSM5 Top	-324.1	-327.4	-325.2
Bottom	-242.0	-242.4	-240.8

- *Prediction and Optimisation*

The incorporation of material non-linearity causes strong non-linear stress responses as a function of the design parameters. This is demonstrated by Figure 5.13. For thin leadframes, local plastic yielding occurs (compare with Figure 5.9), resulting in a strong non-linear RSM that is quite different with the one for thicker leadframes. As mentioned before, highest compressive stresses are calculated during the temperature cycling testing at –65°C (RSM3). Highest tensile stress are calculated after cooling down from soldering temperature to 25°C (RSM1). Both these response parameters are used to optimise the microelectronics package.

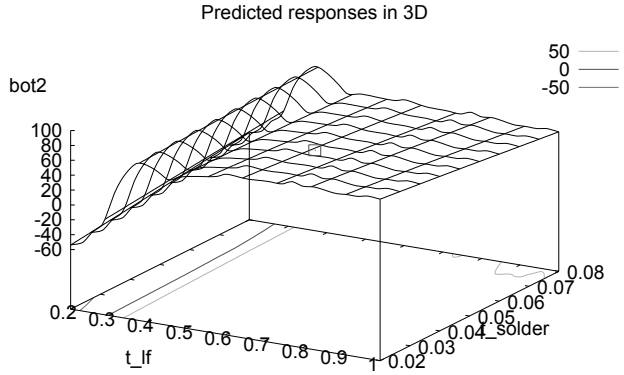


Figure 5.13: 3D RSM plot mid bottom die stresses at 25°C after die soldering.

Figure 14a shows the 3D RSM plot for the top die stresses after TMCL at –65°C as a function of the thickness of solder die-attach and leadframe. This figure indicates that the thicker the solder die-attach layer, the less the compressive stress. This figure also shows that the compression stress is a non-linear function of the leadframe thickness, and there exists a worst-case (leadframe thickness approx. 0.65mm) for which the die experiences the highest compressive stresses. In other words: given the symmetry of the RSM the safe design range for the leadframe thickness is either below 0.6mm or above 0.7mm. Figure 14b shows the 3D RSM plot for the top die stresses at 25°C after die soldering as a function of the thickness of solder die-attach and leadframe. This figure shows that high die tensile stresses are expected for leadframe thickness between 0.3mm and 0.2mm. Compressive stresses are expected for leadframes thicker than 0.50mm.

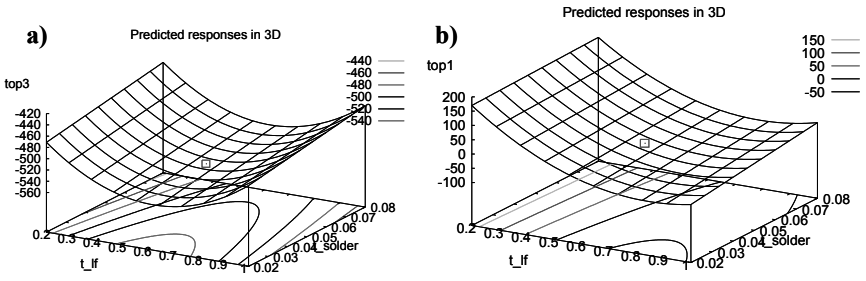


Figure 5.14: 3D RSM plot top mid die stresses after a) TMCL at 25°C and b) after die soldering at 25°C.

The results described above indicate that reliable package optimisation can only be achieved when the important packaging processes are taken into account. The influence of the major packaging processes on the die stresses is depicted in Figure 15a and Figure 15b. Both figures show the horizontal stress on the surfaces of the die as a function of the processes for different leadframe thickness and a fixed solder die-attach thickness of 30 μm. It is observed that:

- Top Die Stress: Critical tensile stresses occur at the top of the die with leadframe thickness in the range of 0.2–0.3mm. Highest compressive stresses, which are close to critical values, occur at the top of the die with a leadframe thickness of 0.6mm. The most favourable leadframe thickness should be in the ranges of 0.4-0.6mm or 0.8-1.0mm.
- Bottom Die Stress: No critical tensile and/or compressive stress values are found on the bottom surface of the die during the major packaging processes. Tensile stresses (lower than the allowable) occur on the bottom surface of the die during moulding, for leadframe thickness of 0.4–1.0mm. As for the top die stresses highest compressive stresses are found at -65°C after the first cooling down in temperature cycling testing.

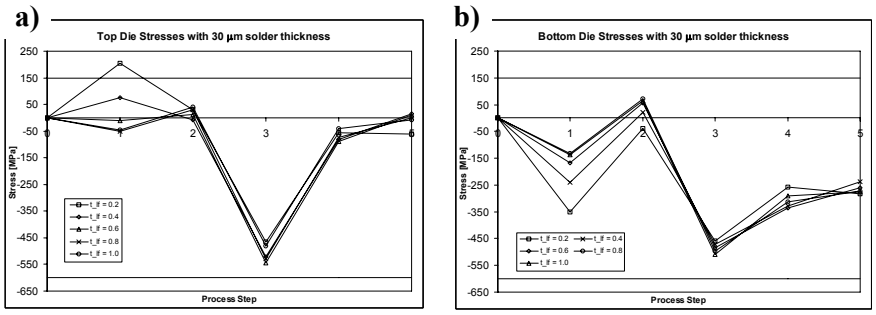


Figure 5.15: Die horizontal stress as a function of the assembly process for different leadframe thickness, a) top and b) bottom side.

- *EGO Results*

In contrast to the previously described method, the EGO method is used to optimise the geometrical feature leadframe thickness of the package. The EGO approach is described in Chapter 3. Remind that EGO is based on an advanced sequential approach and embeds the choice of the DOE points with the optimisation process. Initially, a number of DOE points are executed in order to deduct the main parameters responsible for the maximum stress levels at the top and bottom side of the IC. Next, DOE points are added in order to reduce these stress levels while changing the geometrical parameter. As a response parameter, the stresses at the top and bottom of the IC are combined to give an average value. The initial experiment is based on a Latin-Hypercube design with 16 DOE points. Based on the Expected Improvement, see Chapter 3, an additional 6 DOE points are added to improve the overall accuracy of the final response surface. In order to verify the accuracy of the final response surface, a comparison is made between the predicted results and the simulation results. In order to do that, a few additional numerical experiments are executed and compared with the prediction given by the response surface. The experiment points were selected randomly within the domains. The verification experiment yielded a deviation lower than 2%. The optimisation is combined with a sensitivity analysis due to the induced scatter of the parameter, in this case described by a normal density distribution. The optimal solution can be found by minimizing the both: objective and sensitivity function. This resulted in an optimal leadframe thickness of 0.50-0.55mm. Notice that this results is obtained by executing only 16 numerical experiments, whereas the previously described method needed 25, a reduction of almost 40%.

5.5 Package Qualification

Based on the virtual prototyping results a new leadframe thickness is selected, leadframes are ordered at the supplier, samples are built and a qualification program started. The original thickness of the leadframe within the qualified (and sold) package is 0.89mm and falls within the predicted safe range . For the new thickness a value of 0.5mm is selected. Assembly, ambient electrical and reliability testing are carried out for the devices using the conventional manufacturing line and the same material set as before. A standard qualification program is executed, as described in Chapter 2. Figure 5.16 shows a cross-section of both the original package and the optimised version with a thinner leadframe thickness.

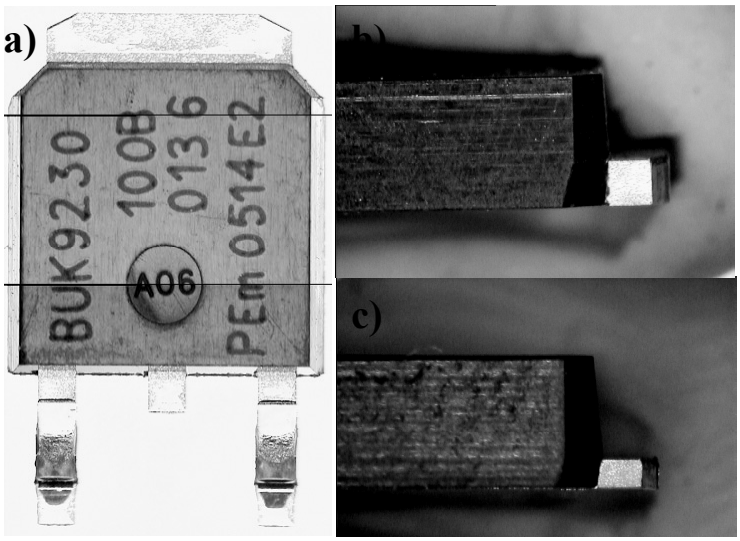


Figure 5.16: a) Top view on the power package with original 0.89mm leadframe thickness and (b) and optimised version with 0.5mm leadframe thickness (c).

Results from the reliability tests using the 0.5mm leadframe thickness are listed in Table 5.6. The results revealed die crack is not an issue after full reliability testing. Finally, thermal and electrical measurements are performed to check any deviation in the 0.5mm package performance compared to the traditional one. The change in the leadframe thickness did not significantly alter the thermal and electrical performance of the package. Due to these positive results, the package is changed to the decreased leadframe thickness. Giving the reduction in material thickness, cost savings are in the order of 260k$ per year.

Table 5.6: Reliability test results using a 0.5mm leadframe thickness.

Reliability Test	Duration	Results
PPOT	96hrs	0/80
TMCL	1000cycles	0/80
THBS	1000hrs	0/80
HTSL	1000hrs	0/80

5.6 Conclusions

Virtual thermo-mechanical prototyping of microelectronics packaging can be achieved through simulation-based optimisation techniques to generate reliable RSM models. This technique is used to optimise a real package case with respect to two geometric design parameters, i.e., the thickness of the solder die-attach and the thickness of the leadframe. The horizontal stress levels at the top and bottom of the die surface are used as the index for vertical die crack. FEM simulations were carried to develop reliable RSM models for the response parameters during the major packaging processes.

It is observed that material, geometric and boundary non-linearity's should be taken into account if reliable FEM models are expected. The non-linearity's will influence not only the die stress levels but also the associated design trends. It is therefore concluded that such non-linear effects in IC constituents can not simply be neglected.

For the microelectronics package investigated, a leadframe thickness smaller than 0.3mm is not preferred, since critical tensile stresses occur at the top of the die after die-attachment. Also, a leadframe thickness of 0.6mm is not preferred, since high compressive stresses, which are close to the allowable values, occur at the top and bottom of the die at –65°C during temperature cycling testing. Using the EGO approach, an optimal leadframe thickness of 0.50-0.55mm is found. By using the EGO approach a 40% reduction in numerical DOEs is obtained. A full qualification program is executed using a 0.50mm thick leadframe yielding no reliability issue. A significant cost reduction is obtained by the new package with no loss in reliability performance.

The presented simulation based optimisation strategy can be used to predict, evaluate, optimise and eventually qualify the thermal and mechanical behaviour of

microelectronics package against the actual requirements prior to major physical prototyping and manufacturing investments. But *reliable product optimisation* can only be achieved when the underlying non-linearity's and the important packaging processes are taken into account.

Chapter 6

Virtual Prototyping based IC Package Stress Design Rules[1]

In this chapter, virtual prototyping is used to generate more accurate and efficient stress design rules for IC backend structures, in combination with packaging processes and geometry. The addressed failure modes are delamination, passivation cracks and pattern shift. When delamination is present, passivation crack occurrence is found to depend on the metal layout and location on the IC. Optimising the metal layout design can even prevent passivation cracks. It is demonstrated that for successful development of IC backend structures and processes, it is essential to take into account the influence of packaging and reliability qualification in the earlier phase of IC backend development. The so-called integral design rules, accounting for all the major loading sources and history of the complete product creation process has to be used for the development of new generation semiconductors devices.

6.1 Introduction

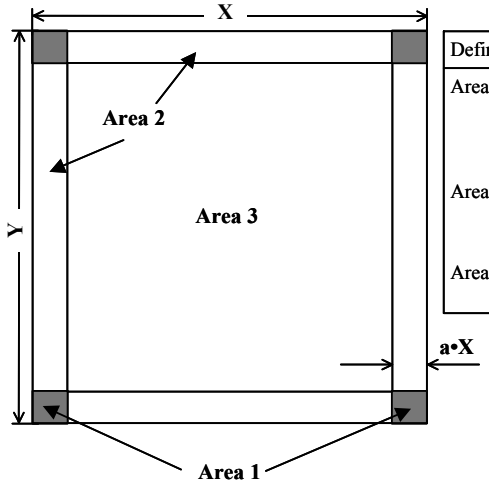
In general an IC needs to be assembled before being put on an microelectronics board by the end customer. The materials of which the IC is made and the materials for the assembly normally have different thermo-mechanical behaviour and temperature changes during manufacturing, testing and application will therefore cause stresses in the materials. These stresses, in extreme cases, may cause serious damages to the ICs, especially at the corners of the chip. Besides efforts of process improvements and material optimisation for both packaging and IC manufacturing, proper measures need to be taken in IC design in order to eliminate/suppress the problem sufficiently. The target of integral IC package modelling is two folded. First of all, it serves to understand the interaction between package processing and testing on the stress/strain response of the IC layers and its deeper structures. Secondly, to deduct IC design rules to prevent possible failures after packaging, manufacturing and testing, the so-called

[1] Reproduced from parts of Chapter 5 and 8: G.Q. Zhang, W.D. van Driel, X.J Fan (editors), Mechanics of microelectronics, Springer Dordrecht, The Netherlands, 2006b.

IC package design stress rules. The IC package stress design rules provide guidelines in the design manual of those measures in the IC design to avoid the IC damages induced by package stresses, by:

- A definition of the areas (the sizes and shapes) in different categories according to the severity of potential damages.
- Regulation of the use of those areas. That is, the rules stipulate what kinds of elements of the IC are allowed/forbidden in each area.
- The ways of using slots in wide metal lines are given (layout of bondpads are not regulated by these rules).

Figure 6.1 gives an example of the *IC package stress design rules* for a given CMOS technology as currently used by the microelectronics industry. The figure shows a top view on the IC and areas are indicated for which certain rules exist, with area 1 is a high risk area, followed by area 2 and then area 3. Typical values for the size of area 1 and 2, denoted by *a*, are 4-5% for an IC of size X·Ymm^2. Design rules valid within each area specify, for instance, maximum line width without a slot, minimum distance between the outer edge of the seal ring and the bondpad edge, etc.



Definition	Rules
Area 1	High risk: active/passive structures not allowed, power bus only with specific layout rules
Area 2	Mediate risk, active/passive devices not allowed, wide metal lines to follow metal layout rules
Area 3	No risk, any structure allowed, no additional layout rules.

Figure 6.1: Example of package stress design rules for a given CMOS technology, typically a = 4-5%.

It is evident that the *IC package stress design rules* will depend on the type of IC, the type of package and/or the materials used. For example, for ceramic packages in which no other materials are present above and next to the dies (except for the

bonding wires) these rules can be much relaxed or even no layout rules are needed at all. However, at this moment the rules are independent of the package type, they only depend on the IC size, see Figure 6.1. Virtual thermo-mechanical prototyping may help to deduce these rules in a very efficient way to answer question like:

- What IC thickness should be used?
- What wire loop height and length should be used?
- What Bill of Material (BOM) list should be used?

6.2 Methodology

Given the large size-differences, reliability predictions for IC package interactions require multi-level (global-local) modelling techniques. At present, these techniques are used to predict the behaviour of low-k debonding in flip chips [Mercado *et al.*, 2003a, Mercado *et al.*, 2003b] and to predict the occurrence of passivation cracks and pattern shift [van Silfhout *et al.*, 2003]. Multi-level modelling can be done by using 3D FE models, 2D FE models and/or coupled 2D-3D FE models. Although the technique is very powerful, it has some major drawbacks:

- The eventual accuracy in the local FE model(s) is strongly connected with the mesh size (read: coarseness) in the global model;
- Displacements calculated in the global FE model serve as boundary conditions in the local model(s), with the risk of creating an over-constrained system;
- No coupling exists between the local FE model back to the global model, indicating that if delamination and/or cracks occur on a local level this will definitely have an effect on the global deformations. This is by far the major drawback of the currently available multi-level techniques.

Other options to predict the reliability of the integrated IC backend and package combination are by using 2D models including the thin IC layers and/or 3D slice models. This cannot be done in full 3D since it will lead to very large FE models.

Passivation cracks and metal interconnect shifting are well-known failure modes inside IC packages. Metal shifting is often called pattern shift and cracking of the passivation layer always precedes this phenomena. Figure 6.2 shows an example of metal shift. Besides that, delamination at the interface between IC and compound is always observed. A combined experimental and numerical approach is used to explore the effect of delamination on the occurrence of passivation cracks and pattern

shift. Multi-level FE models are combined with the J-integral technique in order to predict the crack energy levels in the passivation layer. Besides that, specially designed package samples are developed to observe passivation cracks and to verify the FE predictions. The samples contain ICs with various test structures in each corner, Figure 6.2 shows an example of such a structure.

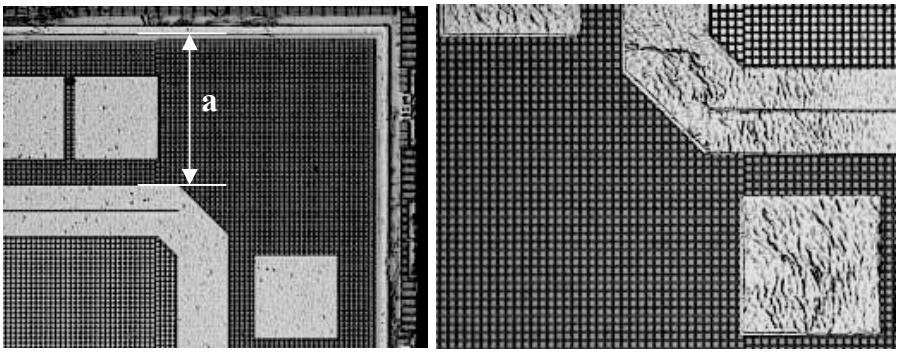


Figure 6.2: Intact (left) and shifted (right) metal lines, distance a indicates the distance between the power line and the seal ring.

- *FE Models*

Different parametric 3D and 2D FE models are created to predict global and local stress and strain levels. The 3D model consists of the IC with moulding compound, leadframe and die-attach to represent a typical QFN package. In these models it is possible to include delamination and predict stresses as a consequence of this. In this way, critical locations for passivation cracking can be determined. The 2D models are used to predict stresses, deformations and crack energy with and without delamination as a function of the metal layout. These models contain the silicon substrate, interlayer dielectrics, top level of interconnect metal layout and moulding compound. The metal layout includes the seal ring, bondpads and power line. By combining the results of both the 2D and 3D models, a 3D J-integral distribution along the power line can be obtained by multiplying the 2D J-integral values with the 3D distribution obtained from the 3D simulations. Both wafer and packaging processes are taken into account to include the thermal history, since significant stresses are already built in the backend processes. Other assumptions and simplifications are:

- Initial passivation cracks are located at the corner of the power line or at the centre between metal lines (or power line and bondpad).

- An initial crack must be put in the models in order to extract crack energy. The initial crack length is 80nm. The corner crack direction is 45° and the centre crack is vertical. The effect of different initial crack propagation was studied in separate models and 45° was found to be critical for a large variety of crack lengths. A length of 80nm was applied to simulate the smallest possible initial crack.
- Delamination at the edge of the IC is taken into account in the models, during TMCL. The delaminated length is 0.5mm from the edge. Delamination growth is not modelled; delamination is used as an input by using contact bodies.
- Appropriate material behaviour is assumed, including time- and temperature-dependent properties.
- The backend structure is modelled as one cool down step from 450°C to room temperature. The individual build-up of metal, interlayer dielectrics and passivation layers are not taken into account.
- Isothermal conditions are assumed.

Figure 6.3 shows the different 2D and 3D FE models as used in the multi-level approach. The 3D model aims at predicting the compound forces on the passivation in the IC corners. Links between the IC and the compound are added to simulate the interlocking effect of a metal line at that position. The distribution of the forces predicted by the 3D model is used to scale the numerical J-integral values predicted by the 2D simulations.

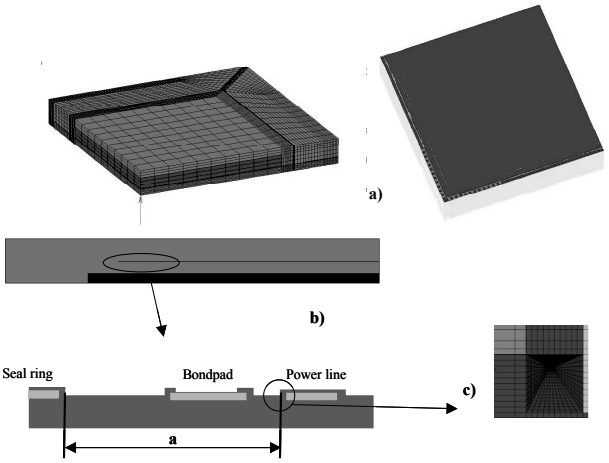


Figure 6.3: Multi-level modelling technique, with a) 3D package model, b) 2D IC layer model and c) J-integral mesh. Distance a is defined as the distance between the power line and the seal ring.

- *Experiments*

Six different test structures, including a seal ring, bondpads and power lines are constructed with varying values for the parameter *a*, which is defined as the distance between the power line and the seal ring. The structures are referred to as S1 till S6 with increasing distance *a*: for S1 a = 78μm; for S2 a = 138μm; for S3 a = 203μm; for S4 a = 269μm; for S5 a = 334μm; for S6 =400μm. CMOS technology with a 0.18μm line width is used to construct the test structures. The structures are created on a Multi Project Wafer (MPW). First, the wafer is thinned to a 280μm thickness. Then, ICs with a 9x9mm^2 size are cut out of the MPW using the standard sawing process, see Chapter 2. Each IC consist of 4 structures placed on the corners, this yielded at least 35 samples per structure. Next, the ICs are assembled in a 14x14x0.85mm^3 plastic encapsulated package of type QFN100 with a 10.8x10.8mm^2 diepad. Standard assembly processes are used, die-attach, moulding, curing, singulation and laser marking. Per IC structure 24 packages are created. After preconditioning under MSL1, MSL2, or MSL3 conditions, the packages are subjected to TMCL testing, with the standard condition -65°C to 150°C. At various stages in the assembly and testing processes, C-SAM analyses are performed to determine the amount of delamination at the IC-compound interface. After testing, packages are decapped and the following analyses are performed to observe the failures. First of all, visual inspection using a microscope is used to detect metal shift and passivation cracks by decapping (removal) of the moulding compound. Secondly, pinhole analyses are used to detect passivation cracks. A pinhole test is putting an etching fluid on top of the IC, which runs through passivation cracks (if present) and etches away the metal. Cracks are visible by the changes in reflection/colour. And finally, scanning Electron Microscopy (SEM) and Focused Ion Beam (FIB) analyses are used to detect more details of both failures in cross-sections.

The experimental results are used to verify the numerical approach, which on its turn can be used to investigate the effect of IC-compound delamination, the effect of distance metal line to the IC edge and the effect of the metal design. The results are described below.

6.3 Results

- *The effect of IC-compound delamination*

For some test structures, large amounts of delamination at the IC-compound interface is found before thermal cycling. Figure 6.4 shows a typical C-SAM result after MSL1 precondition, indicating that the IC-compound interface for samples number 1, 2, 3 and 14 are partially and for sample number 7 even fully delaminated.

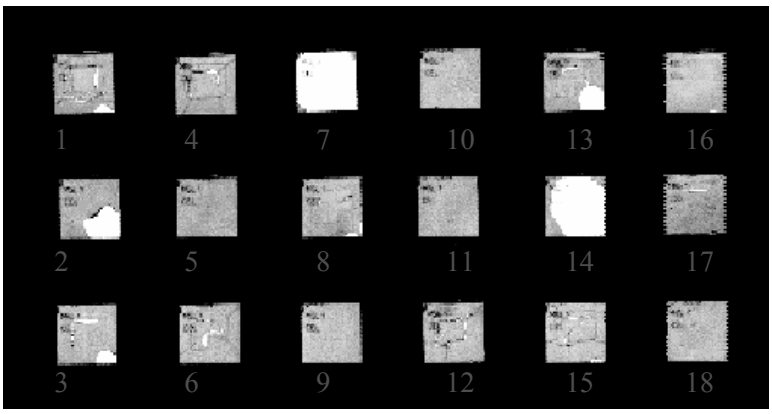


Figure 6.4: Typical C-SAM analysis results, white areas denote a delaminated IC-compound interface.

In the delaminated structures, after decapping, visual inspection clearly showed passivation cracks and metal shift, see for example Figure 6.1 - right picture. The shifting of the metal line and bondpads runs from the corner towards the inside of the IC. The metal surface is wrinkled, showing that the metal is pushed towards the centre of the IC. Again, delamination at the IC - compound interface is always observed in failed samples, making it the major trigger causing passivation crack and metal shift. The physics behind the mechanism is determined by the simulations and agreed with the experimental observations. Figure 6.5 shows the maximum principal stress distribution during thermal cycling in the IC passivation layer for a non-delaminated (left) and a delaminated (right) IC-compound interface. In case of the delaminated interface, the stress level in the passivation material is increased with almost a factor 8 (595MPa versus 4500MPa).

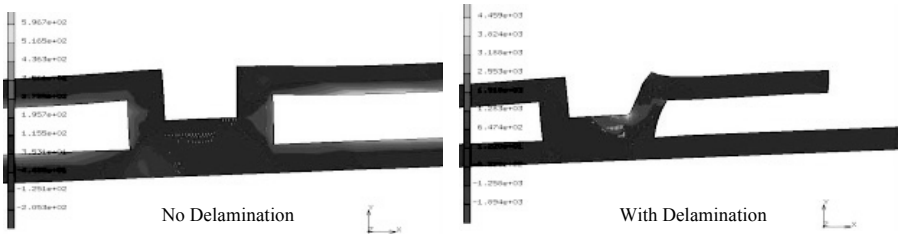


Figure 6.5: Maximum principal stress distributions during thermal cycling in the IC passivation layer: non-delaminated (left) versus delaminated (right) IC-compound interface.

Without delamination high maximum principal stresses in the passivation layers occur close to the metal. They are mainly due to the high CTE of the metal compared to the surrounding materials. When delamination reaches the metal line and starts growing to the inner part of the IC, its effect starts to appear in the passivation layer. As such, the highest maximum principal stresses change progressively of location. Figure 6.6 shows the maximum principal stress distribution in the passivation near the metal for 3 delamination lengths:

- A short delamination length: tensile stresses of 300MPa are maximum in the corner of the passivation near the metal feature.
- A delamination length just until the metal line: the stress level and critical location are similar to the above, maximum is 300MPa.
- The delamination length exceeds the metal line: the compound starts pushing against the passivation and stress levels increase to a peak of 1760MPa in this case.

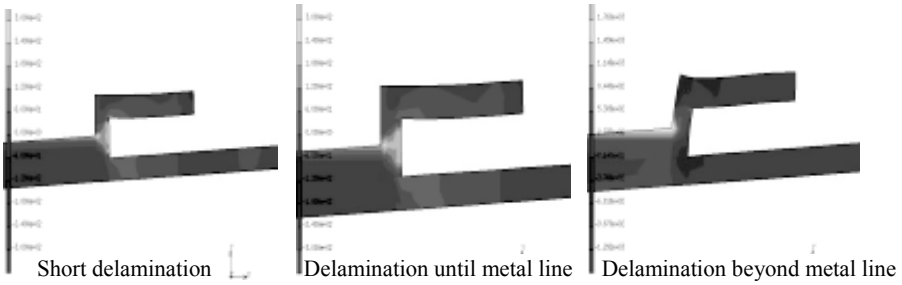


Figure 6.6: Maximum principal stress distribution during thermal cycling in the passivation layer with increasing delamination length (from left to right).

Figure 6.6 also shows that the stress levels increase significantly and the critical location shifts to the corner of the passivation material. If delamination appears, the above part of the moulding is no more continuously constrained by the passivation, but only by the concentrated interlocking due to the topography. The interlocking causes higher stresses compared to continuous contact of compound and passivation. Figure 6.7 explains this mechanism. Actually, delamination and passivation cracking are part of one and the same failure mechanism.

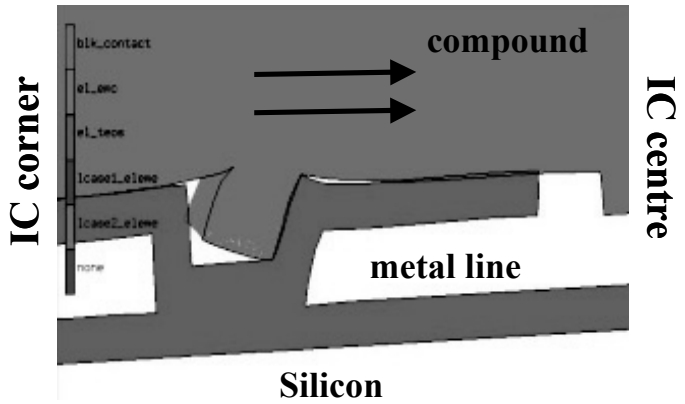


Figure 6.7 Mechanism for delamination related passivation crack and metal shift: compound pushes against the passivation leading to increased stress levels in the corner of the passivation layer.

- *The effect of distance between metal line and IC edge*

When delamination is present, the experimental results for the structures S1 to S6 showed that the structures S2, S1, S3 and S4 consistently showed failures (in this order) to a different extent. For instance: structure S2 showed major cracking and metal shifting, to a lower extend this holds for structure S4. However, the structures S5 and S6 showed no failures at all. Figure 6.8 shows the predicted J-integral values for the different structures. Remind that for the calculations a 10% delamination between the IC and the moulding compound is assumed. Ranking the test structures from worst to best would give the following:

S2 -> S1 -> S3 -> S4 -> S5 -> S6

The calculated and experimental ranking agrees very well. The simulation results show that the distance from the metal line to the IC edge has a significant effect on the crack energy.

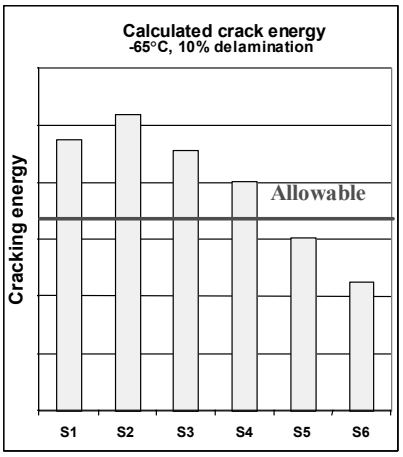


Figure 6.8 Calculated J-integral values at -65ºC during thermal cycling for the different structures S1 to S6. A 10% delamination between the IC and the moulding compound is assumed.

- *The effect of metal design*

Once delamination in the IC-compound interface is present, varying the metal design, in terms of width and distance from edge, influences the passivation stress levels. As such, it is possible to design the metal layout such that delamination will not lead to failures as passivation crack and metal shift. Figure 6.9 shows the maximum principle stress for a safe and a critical metal layout including 10% delamination. The maximum tensile stress reaches about 1700MPa for the safe metal layout and 4450MPa for the critical one. This indicates that certain metal design rules are needed in the corner of the IC. Combining the validated parametric FE models with optimisation techniques, as described in Chapter 3, allows to deduct such rules. This will be described in the next section.

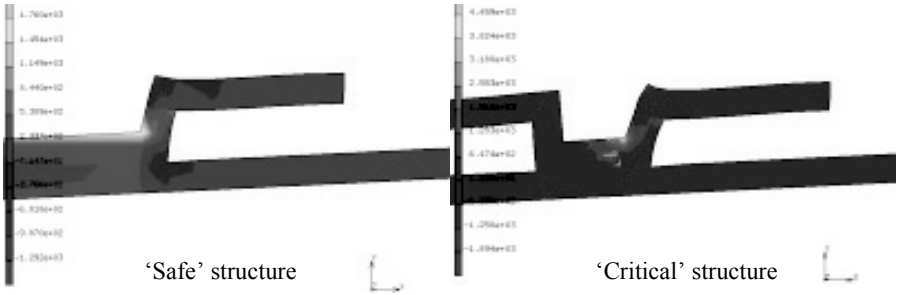


Figure 6.9: Maximum principal stress distributions during thermal cycling in the passivation layer of a delaminated safe (left) and critical structure (right).

6.4 Response Surface based Design Rules

Space-filling Latin Hypercube designs are used to create the response surfaces. Using the parametric non-linear FE models, simulations are carried out for all the designs and the resulting J-integral values are used as the response parameter. Quadratic models with interactions are used for the response surface generation. Figure 6.10 shows the influence of the metal width *w* and the distance to edge *a* on the J-integral value. This response surface is constructed using the 2D FE model and a space-filling Latin Hypercube DOE consisting of 20 variations. The figure clearly shows that the effect of *a* is dominant, whereas the effect of *w* is negligible. This indicates that from a thermo-mechanical perspective the metal design rules should not focus on the width but rather on the placement of the structure.

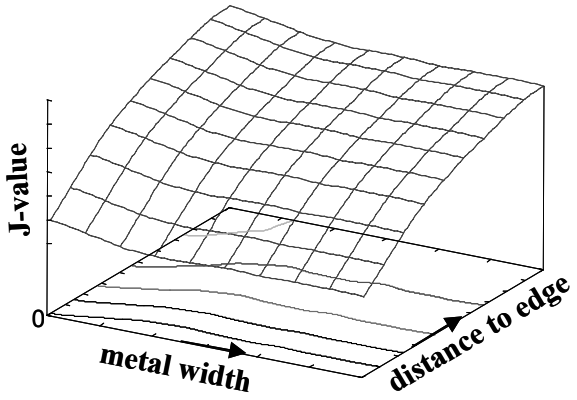


Figure 6.10: J-integral value as a function of metal width w and distance to edge a.

IC package stress design rules for the given CMOS technology and package combination are deducted using the 3D FE models and a space-filling Latin Hypercube design consisting of 60 design variations. The design parameters are:

1. The thickness of the IC, ranging from 0.1 to 0.38mm
2. The width of the power line, ranging from 5nm to 0.10µm
3. The length of the IC, ranging from 6 to 10mm
4. The yield strength of the leadframe, ranging from 150 to 600 MPa
5. The type of passivation material, either TEOS or SiN
6. The type of the moulding compound, either MCA or MCE
7. The intrinsic stress in the IC layers and the critical energy value

Figure 6.11 shows an example view of the design tool built up using the response surfaces. Like Figure 6.1, the figure shows a top view on the IC and areas are indicated that are critical and/or safe. The critical areas are indicated in red, the areas with a 75% critical value in yellow and safe areas in white. The colours and the area will change automatically with the changes of the input parameters on the right. In contrast to the current design rules, see Figure 6.1, Figure 6.11 shows a different pattern of areas according to the thermo-mechanical stresses on the die surface. Instead of being square areas, danger zones are rather triangular shaped.

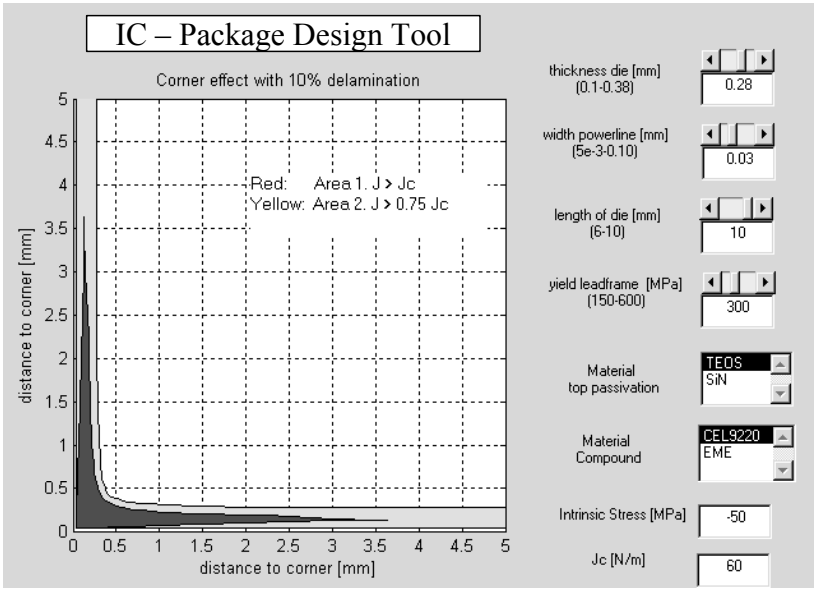


Figure 6.11: View on virtual prototyping based package stress design rules.

Figure 6.12 shows an application example of the design tool. In this example, the effect of IC thickness on the failure risk is studied, by comparing two ICs with a thickness of 150μm and 300μm, respectively. It can be seen clearly that the pattern and the area of the critical areas are different. The thick IC (300μm) has much less chance of failure in this situation (with fixed structure, compound and package type). Besides, it is possible to use more area near the edge, which will lead to direct cost saving. In contrast to the current design rules, see Figure 6.1, Figure 6.12 shows that the situation is much more complex in the sense that the shape and location of the critical area may vary per situation. Due to this complexity, it will be impossible to give a complete overview on the dependence of each design parameter on all those

variables with one graph. For this reason, a design tool is constructed with which selected geometrical and material dependencies of the dangerous area(s) can be visualized. With such a design tool, designers may achieve a first time right IC backend structure prior to any physical testing.

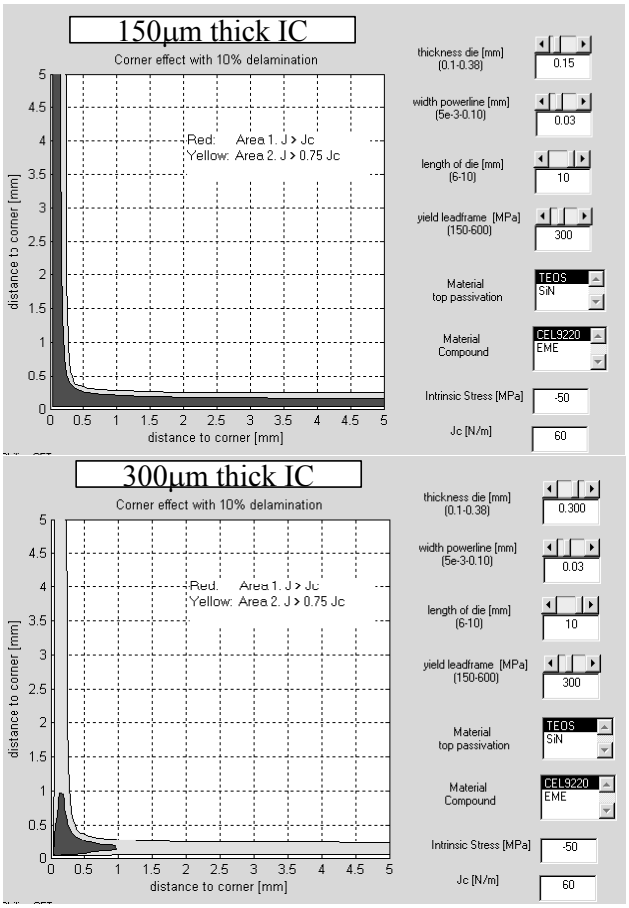


Figure 6.12: Demonstrator tool result: effect of IC thickness.

6.5 Conclusions

Several FE models are built to determine the mechanisms of passivation cracking and metal shift during wafer backend processes and package assembly. Based on the results, the simulation models are capable to predict the effects of metal layout on failure occurrence, critical locations and root causes. Furthermore, a limited number of test samples can be used to verify the FE results and predict failures prior to prototyping of real metal designs.

It is demonstrated how *IC package stress design rules* can be made based on thermo-mechanical simulations. The impact of items such as die size and thickness, metal width, material types and intrinsic stress levels on the package stress induced damages revealed by the simulation show a significantly different picture than what is described by the current design rules. In contrast to the definition of area 1, 2 and 3 in the current design rules, a more realistic definition of the areas according to the potential occurrence of package damages is shown. Instead of being a function of die size only, the size and shape of the dangerous area depend predominantly on IC–compound delamination and strongly on die thickness, die size, moulding material properties, passivation choice and intrinsic stress levels for the passivation layers.

Although the simulations are performed for a given IC and packaging technology, based on the similarities, it is expected that many other will have the same/similar results with respect to the effects of all the variables investigated here. This means that there will be a great possibility to improve the current *IC package stress design rules* based on virtual thermo-mechanical prototyping.

Chapter 7

Structural Similarity Rules for the BGA Package Family[1]

To efficiently select qualification and reliability monitoring programs, structural similarity rules for IC designs, wafer fabrication processes and/or package designs are currently used by the industry. By following the package structural similarity rules, the numbers of reliability qualification tests may be greatly reduced. However, when looking at the present rules it is clear that they are not reliably defined. For instance, geometrical parameters such as die-to-pad ratio are not quantitatively included and it seems that linear relationships are assumed. Besides that, these rules are mainly deducted from experience and industrial trial and error results, not from reliability physics. Driven by the present development trends of microelectronics (miniaturization, integration, cost reduction, etc) it is urgently needed to develop 'advanced based structural similarity rules' based on reliability physics (physics of failures), to meet the industrial development trends. In this chapter, virtual prototyping techniques are used to deduct advanced structural similarity rules through simulation-based optimisation techniques. Parametric 3D non-linear FE models are constructed to explore the responses of the complete Ball Grid Array (BGA) package family for both the thermo-mechanical and moisture-diffusion responses as function of six geometrical parameters. In this way, advanced structural similarity rules are deduced which can be used to shorten design cycles. Even more, by using the accurate 3D non-linear reliability prediction models easy tools can be created for package designers. By using such a tool, the number of reliability qualification tests can be reduced. More importantly, possible failure mechanisms can be (better) understood and/or predicted.

7.1 Introduction

Structural similarity determines the extent to which test results from a specific device or family can be considered representative for other similar types. When applied to reliability aspects, structural similarity is indispensable in predicting the reliability

[1] Reproduced from: van Driel, W.D., A. Mavinkurve, M.A.J. van Gils, G.Q. Zhang, D.G. Yang, L.J. Ernst, Advanced structural similarity rules for the BGA package family, Microelectronics Reliability 47, pp. 205-214, 2007a.

performance of types similar to those that have been specifically subjected to reliability testing. The need for having structural similarity rules is not only because reliability testing of every type is time and money consuming, but also because it is often unnecessary to test all due to the inherited similarity of products. Structural Similarity rules for IC designs, wafer fabrication processes and/or package designs are currently used by the industry to define efficient *Qualification and Reliability Monitoring* programs. They imply that the reliability results from one product may be used for others if they meet the structural similarity criteria. In general, there are three qualification options for an IC/package design or process:

1. Qualification using existing data. Based on existing data the IC/package design or process is being qualified.
2. Bridge Qualification. Based on existing data for one or more similar IC/package designs or processes (so called 'bridge' design or process) qualification is granted. This can only be done when certain criteria, the so-called structural similarity rules, are met.
3. Qualification requiring new/additional testing. When both the needed reliability data and structural similarity rules are not available new or additional testing is required to qualify the design or process.

It is evidential that in the case where a full qualification program is needed, time-to-market and costs will increase significantly. Thus, any qualification data that can be used to minimize the additional testing will be more cost efficient. For assembly and packaging, a structurally similar package means that it:

- Belongs to the same package type, such as BGA, QFP, or others,
- Has the same or smaller body size,
- Has the same or larger inner, outer lead or ball spacing,
- Has the same or smaller diepad size,
- Has the same or smaller die size,
- Has the same materials, for leadframe/die attach/moulding compound,
- Has the same construction characteristic, such as exposed diepad or fused leads.

By following the package structural similarity rules, the numbers of reliability qualification tests may be greatly reduced. However, when looking at these rules it is clear that they are not reliably defined. For instance, geometrical parameters such as die-to-pad ratio are not quantitatively included and it seems that linear relationships

are assumed. Besides that, these rules are mainly deducted from experience and industrial trial-error results, not from reliability physics. Driven by the present development trends of microelectronics, mainly characterized by miniaturization, cost reduction and shorter time-to-market there will be increased chances and consequences of failures, increased design complexity, dramatically decreased design margins and increased difficulty to meet quality, robustness and reliability requirements. Therefore, it is urgently needed to develop 'advanced based structural similarity rules' based on reliability physics (physics of failures), to meet the industrial development trends. This chapter highlights the results to develop advanced structural similarity rules using the state-of-the-art virtual prototyping and qualification techniques. As a carrier, the BGA package family is chosen. The total design space of the BGA family is explored and parameterised with six parameters, being die thickness, pad-to-body ratio (defined as the ratio between the package body and the copper pad size), die-to-pad ratio (defined as the ratio between the die and the diepad size), body size, body thickness and substrate thickness. Parametric 3D, non-linear and multi-physic FE techniques are used to calculate the thermo-mechanical and moisture-diffusion responses of the complete BGA design space as a function of the above parameters. By combining the accurate 3D non-linear reliability prediction models with advanced simulation-based optimisation methods, such as sequence Design Of Experiments (DOE) and stochastic Response Surface Modelling (RSM) techniques, the 'physics of failure based structural similarity rules' are developed and an Excel-based structural similarity tool is created for designers. By using such a tool, the number of reliability qualification tests can be reduced. More importantly, the possible failure mechanisms can be (better) understood and/or predicted.

7.2 The Ball Grid Array Package Family

In the late 1980s, BGA-like packages were introduced based on a new multi-layer process; double-sided flex circuit pairs were stacked and laminated using adhesives to provide vertical connections. During the development stage, ideas emerged that moved closer to the current BGA packaging concept. The BGA family allows for low profiles and outlines and is currently the standard for high-density IO packages. The concept is based on using an organic laminate, be it FR4 or BT, including copper traces that connect to the IC and further on encapsulated by using a moulding compound. Many different variations are available on the market, such as TFBGA's,

μBGA's, HBGA's, die up of die down, tape-based, but in principle all are using the same concept. In our study we focus on the BGA version and have parameterised the total design space of the family with six parameters. Figure 7.1 shows a ¼ schematic of the BGA identifying the parameters. Table 7.1 lists the ranges of these parameters.

Table 7.1: Geometric ranges for the design parameters.

Parameter	Minimum	Maximum
Die thickness [μm]	280	380
Pad-to-body ratio [%]	15	80
Die-to-pad ratio [%]	15	95
Body size [mm^2]	4x4	44x44
Body thickness [mm]	0.9	1.9
Substrate thickness [mm]	0.36	0.56

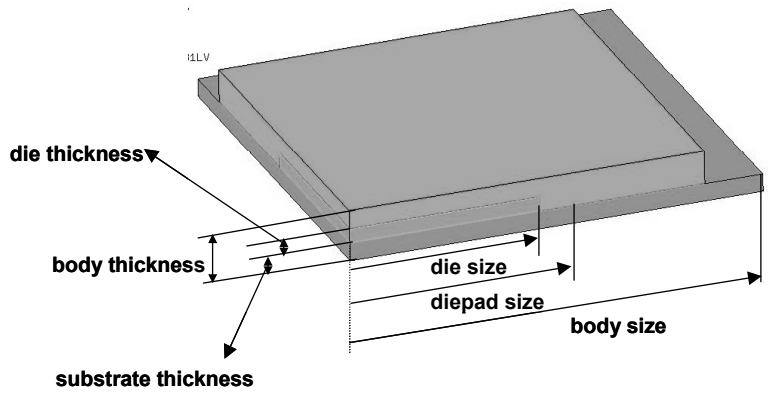


Figure 7.1: The BGA package style identifying the parameterised design space.

Reliability tests are classified in the so-called Qualification System under various names according to the test format, purpose, method of applying stress and other factors. Reliability is defined as the probability that a product in operation will survive under certain conditions during a certain period in time and, as such, failure as the probability that a product is not functioning in that period. Semiconductor products are checked using specially designed tests to ensure that they have sufficient life so that failures do not occur during the normal usage period. In reliability tests, environmental conditions (temperature, moisture) are extrapolated such as to accelerate the circumstances under which the product could fail. Currently classified

reliability tests that can be related to thermo-mechanical and moisture-diffusion conditions are the temperature cycling and moisture sensitivity tests. Moisture is believed to be hazardous for interface delamination in an IC package. Given the different humidity conditions throughout the world, IC packages will be subjected to moisture during assembly and transport. As such, moisture sensitivity levels (MSL) are introduced and for each IC package this level should be deducted. MSL levels are 1 to 6, with 6 being the less severe and 1 being the most severe (85%RH/85ºC). The testing conditions are standardized throughout the complete micro-microelectronics industry via international organizations like JEDEC, IPC and IEC. For each developed package the reliability tests will be performed to investigate whether the long-term reliability demands can be met. A full qualification may take up to 6 months of testing time, so it is urgently needed to develop 'advanced based structural similarity rules'. Table 7.2 shows Moisture Sensitivity data (the level that can be reached before failures are detected) for some typical BGA packages, with varying body size and thickness, pad-to-body ratio and die-to-pad ratio. In this table, conflicting data is marked in bold. For instance, for the LBGA package with a 17x17mm^2 body size, the MSL level depends on the die-to-pad ratio where a value of 89% leads to level 2 but for 65% the level 1 can be reached. Other conflicting data holds for the BGA's in this table, where increasing the body size to 40x40mm^2 may lead to a decreased MSL level compared to a body size of only 17x17mm^2. Typical failure modes in BGA packages related to MSL performance are delamination between the moulding compound and the substrate, see Figure 7.2.

Table 7.2: MSL levels for some typical BGA packages.

		Body Size		Pad Size	Die Size			
Pkg	Pins	Width / Length [mm]	Thickness (mm)	Width / Length [mm]	Width / Length [mm]	Pad to body ratio [%]	Die to pad ratio [%]	MSL level - no failure
BGA	208	17	1.2	4.77	4.24	28	**89**	**4**
BGA	217	23	2.6	7.66	4.80	33	63	3
BGA	225	27	1.55	10.20	8.12	38	80	2
BGA	272	27	1.55	7.10	6.34	26	89	2
BGA	329	31	1.75	8.69	7.42	28	85	2
BGA	388	35	1.75	12.19	11.07	**35**	**91**	**3**
BGA	596	40	1.75	17.27	13.78	**43**	**80**	**3**
LBGA	224	17	1.05	7.13	6.34	42	89	2
LBGA	256	17	1.05	10.40	6.73	61	**65**	**1**
LBGA	324	19	1.05	9.15	7.70	48	84	2
LFBGA	64	7	0.9	4.00	1.26	57	36	1
LFBGA	72	7	0.9	4.03	1.29	58	36	1
LFBGA	208	15	**1.05**	8.59	4.70	57	**54**	**2**

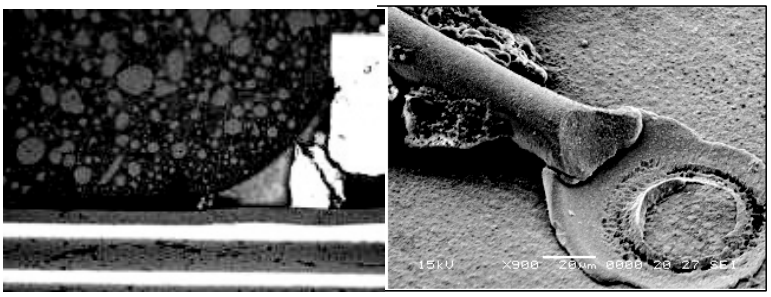


Figure 7.2: Typical BGA failure modes; compound-substrate interface delamination (left) leading eventually to stitch failures (right).

7.3 Multi-Physics Finite Element Modelling

A 3D non-linear FE model including anisotropy for silicon, visco-elasticity for moulding compound and die-attach, elasto-plasticity for copper and orthotropic visco-elasticity for FR4 is constructed, see Table 7.3, and experimentally verified to calculate the responses of:

- Thermo Mechanics: Package warpage, which is believed to play a role in PCB placement, Interface stress levels between moulding compound and substrate, which is related to occurrence of delamination.
- Moisture Diffusion: Moisture content, which is related to MSL performance, Moisture concentration at the interface between moulding compound and substrate, which is related to the occurrence of delamination.

Using advanced simulation-based optimisation methods, such as sequence DOE, stochastic RSMs and adaptive (sequential) techniques above mentioned thermo-mechanical and moisture-diffusion responses are calculated for the complete design space of the BGA family.

Table 7.3: Material properties as used in the 3D FE models.

Material	**Constitutive Relation**	**CTE [ppm/˚C] T_g [˚C]**	**E [GPa]**	**ν [-]**
Si	Anisotropic	3.0	150-169 (main)	0.23
Die-attach	Linear Visco-elastic	$80 < T_g$ $180 > T_g$ T_g: 40	8 (25ºC) 0.2 (>200ºC)	0.35
Compound	Linear Visco-	$6 < T_g$; $35 > T_g$	25 (25ºC)	0.35

Material	**Constitutive Relation**	**CTE [ppm/˚C] T_g [˚C]**	**E [GPa]**	**ν [-]**
	elastic	T_g: 110	0.8 (>200ºC)	
Substrate-FR4	Orthotropic In-plane: Out-plane:	 16 $50 < T_g$; $240 > T_g$ T_g: 180	 18 (25ºC) 7 (>200ºC) 4 (25ºC) 1 (>200ºC)	0.15
Substrate-Cu	Elasto-plastic	17.7	120	0.33

- *Thermo-Mechanics*

A fully parameterised 3D FE model is constructed to resemble the BGA family, see Figure 7.1. The FE model is built in such a way that the element discretisation is kept constant in order to avoid mesh influences. The developed thermo-mechanical simulation models are compared with experimental results for a typical microelectronics package using 3D Moiré interferometry to verify the die and package deformations, see Chapter 4. To develop reliable and efficient non-linear thermo-mechanical prediction models for the product/process designs of microelectronics packaging, various justified simplifications and assumptions are commonly used. The stress free state for each material is set at its process temperature. During the simulations, all elements of a specific material are deactivated and they are activated during the relevant process. For the thermal loading isothermal conditions are used and the initial die warpage/stress is neglected.

Figure 7.3 shows a typical warpage result for a 17x17mm^2 LBGA. In this particular case the maximum deformation in z-direction for the package is equal to 23.8μm and a grumpy shape is found. Figure 7.3 also shows the interface stress (maximum principle stress) as function of the normalized distance from package centre to edge for two typical BGA packages, a 17x17mm^2 LBGA256 and a 19x19mm^2 LBGA324. The stress peak at the die corner will be carried by the die-attach, but the area beyond experiences elevated stress levels, which may cause delamination in that area. Of course, stress levels are only a 1st order estimate for delamination occurrence. In fact, special interface strength tests need to be performed

and combined with fracture mechanics simulations in order to get a quantitative reliable prediction for delamination occurrence.

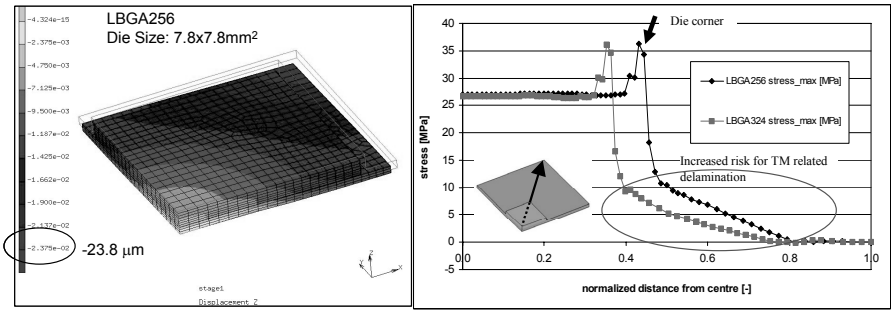


Figure 7.3: Warpage (left) and interface stress (right) results for a 17x17mm² LBGA256 and a 19x19mm² LBGA324.

- *Moisture Diffusion*

We have used the 'wetness' approach [Wong *et al.*, 1998], which assumes continuity of the weighted moisture concentration across interfaces of different materials, see Chapter 4. Using the wetness approach, the moisture diffusion implementation in commercial available FE software codes becomes straightforward with the help of appropriate user subroutines. All the appropriate materials in a BGA package (moulding compound, substrate, solder resist) have been characterized with regard to their moisture behaviour under MSL1 and MSL3 conditions. It is assumed that the moisture uptake in the polymer materials can be described with Fick's Law of Diffusion. Moisture diffusivity, D, and the saturated moisture concentration, C_{sat}, are measured using moisture absorptions measurements at MSL1 (85°C, 85%RH) and MSL3 (30°C, 60%RH) conditions, the results are listed in Chapter 4. Both 2D and 3D models are used to calculate the moisture ingression into the package after 192 hours of the MSL3 conditions.

Figure 7.4 shows a comparison between measured and calculated moisture uptake, both in 2D and 3D, for several BGA packages. It is clear that the 3D result is closer to the measured values, where only a <5% deviation is found.

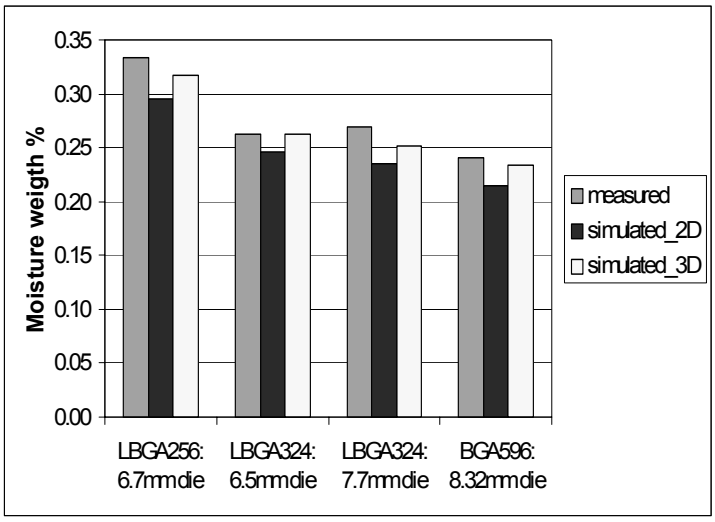


Figure 7.4: Comparison between measured and calculated moisture uptake, both in 2D and 3D, for several BGA packages.

Figure 7.5 shows a comparison of different packages for the moisture concentration at the compound-substrate interface: a 17x17x1.05mm^3 LBGA256, a 40x40x1.75mm^3 BGA596 with a 8.32x8.32mm^2 die and a 21.6x21.6mm^2 die. This figure shows that for a thinner package, more moisture can diffuse to the interface, thus, may reach a worse MSL level. Besides that, a larger die size leads to a slightly increased moisture concentration.

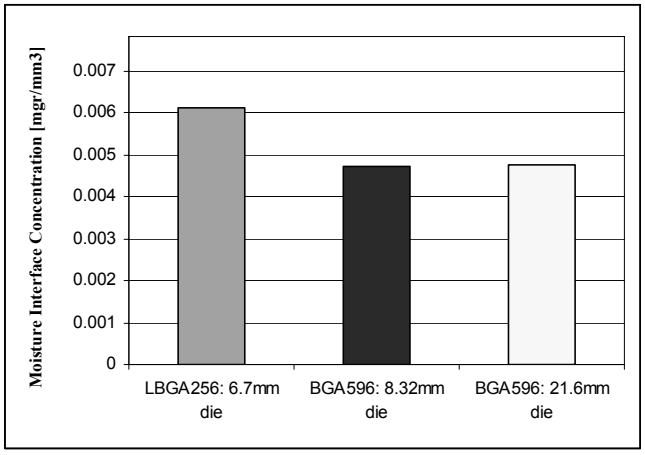


Figure 7.5: Moisture concentration at the moulding compound-substrate interface for different packages.

7.4 Response Surface based Structural Similarity Rules

For both the thermo-mechanical and the moisture-diffusion responses of the BGA package family, a space-filling Latin-Hypercube design is constructed. Since there are 6 input parameters, as given in Table 7.1, and using the rule of thumb that per parameter 10 experiments are needed, at least 60 are required to produce sufficient RSM models. For the given package family, a set of 70 DOE's are needed to obtain this. Figure 7.6 shows the distribution for two design parameters only, i.e. body size and pad-to-body ratio. Using the parametric non-linear 3D FEM models, FEM simulations are carried out for all the 70 designs and the four earlier mentioned output variables (warpage, interface stress, moisture mass and concentration) are used as the response parameters.

For all response parameters quadratic models with interactions are used for RSM generation. Using automatic running procedure based on cross-validation, the unimportant model terms were deleted. The regression statistics are listed in Table 7.4, indicating that for all quadratic models the accuracy requirements are satisfied.

Table 7.4: Compact model regression statistics.

Response Parameter	RMSE
Warpage	0.96
Interface stress	0.85
Moisture mass	1.0
Moisture interface concentration	0.98

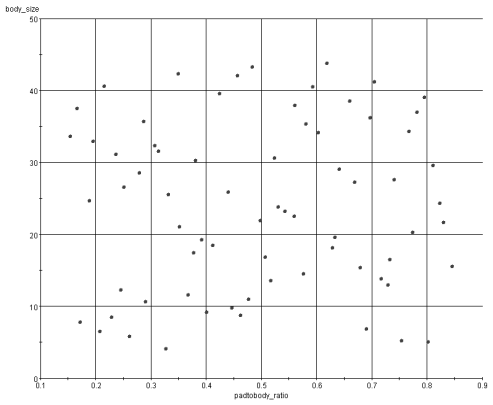


Figure 7.6: Space filling Latin-Hypercube design of experiments: body size vs. pad-to-body-ratio.

Table 7.5 lists the relative importance of the linear polynomial terms describing the RSM functions for i) warpage, ii) interface stress, iii) moisture mass and iv) moisture concentration. The following can be observed from this figure:

- *Thermo-mechanics*

For the warpage, most relevant terms are denoted for the pad-to-body-ratio, body size and die-to-pad ratio. As a consequence, body thickness, die thickness and substrate thickness have a marginal effect on the package warpage. For the interface stress, most relevant terms are denoted for exactly the same ones as those found for warpage. Expect that for interface stress, the substrate and die thickness have some significant effect on the interface stress levels.

- *Moisture-diffusion*

For the moisture mass in the package, the body size and the body thickness are the dominant parameters. The bigger and thicker the package, the more moisture ingresses into the package which seems logical. For the moisture concentration at the compound substrate interface, body and substrate thickness are the dominant parameters (which is the path for the moisture to come in). Die thickness, the die-to-pad and pad-to-body ratios seem to have a significant influence as well. For all these parameters hold that when increasing it, the more moisture will diffuse to the interface.

Essential 2nd order components and/or interaction components are for warpage: pad-to-body-ratio x body thickness and body size x die-to-pad-ratio, for interface stress: pad-to-body-ratio x body size, for moisture mass: body size x body size and for moisture concentration: body thickness x substrate thickness. These interactions confirm the dominant linear parameters, for instance, body size for moisture mass and thickness of substrate and body for moisture concentration.

Table 7.5 Normalized relative importance of the linear polynomial terms for the four response parameters.

Parameter	**Warpage**	**Interface Stress**	**Moisture Mass**	**Moisture Concentration**
Die thickness	0.08	0.13	-0.01	-0.02
Pad-to-body ratio	1.00	0.59	-0.01	-0.04
Die-to-pad ratio	0.98	1.00	-0.02	-0.08

Parameter	Warpage	Interface Stress	Moisture Mass	Moisture Concentration
Body size	0.82	0.48	1.00	-0.01
Body thickness	0.01	0.00	0.12	1.00
Substrate thickness	0.26	-0.18	0.00	0.23

From thermo-mechanical point of view, increasing the body size leads to increased warpage and stress levels. When keeping the body size constant, pad-to-body and die-to-pad ratios play a dominant role in the thermo-mechanical response of the package. This strongly depends on the thickness of the package. This is illustrated in Figure 7.7, which shows the responses of warpage and interface stress as function of the pad-to-body ratio for a 1.05mm (LBGA) and 1.20mm (BGA) package thickness. The following structural similarity rule can be deducted from this figure:

- It is not true by definition that a larger package performs worse:
  - For a package thickness of 1.05mm: above a pad-to-body ratio of 35% package size dominates; below 35% a smaller package performs worse.
  - For a package thickness of 1.20mm this is valid for a pad-to-body ratio of 65% and higher.

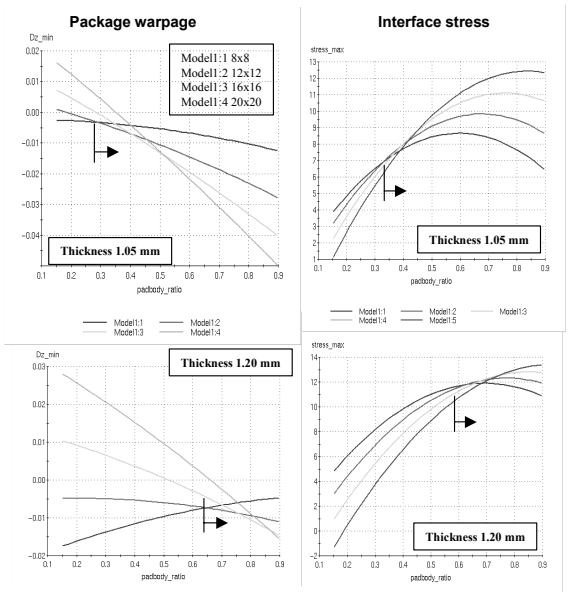


Figure 7.7: Warpage and interface stress response vs. the pad-to-body ratio for a 1.05mm (LBGA, top) and 1.20mm (BGA, bottom) package thickness.

Figure 7.8 and 7.9 show the 3D responses of the four output parameters as function of the dominant input parameters: pad-to-body and the die-to-pad ratios (Figure 7.8) and body thickness and size (Figure 7.9). These 3D responses in it self hold the structural similarity rules for the BGA package family. Both the interface stress and moisture concentration are the parameters that will be responsible for interface delamination at the substrate/compound interface. The moisture will on the one hand decrease the strength and on the other hand create vapour pressure loading. For these responses it is observed that when increasing the die-to-pad ratio the risk of interface delamination will be larger. Increasing the die-to-pad ratio also increases the package warpage and more moisture will ingress into the package. Figure 7.9 shows that the body size effect is very dominant for warpage, stress and moisture mass but not for moisture concentration at interfaces. For the later one, body thickness is a dominant parameter.

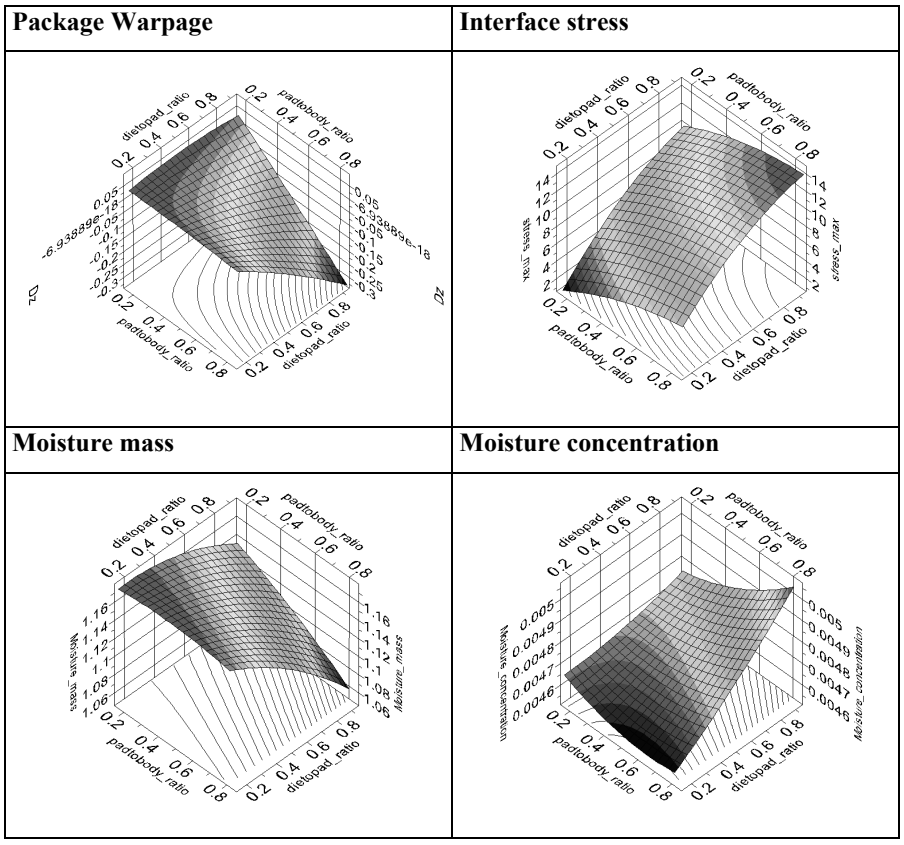


Figure 7.8: 3D responses as function of pad-to-body and die-to-pad ratios.

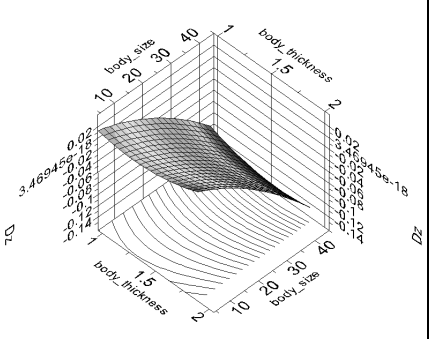
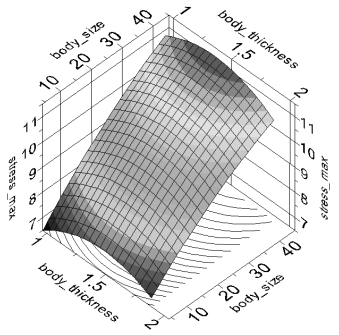
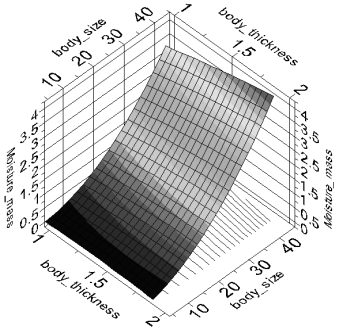
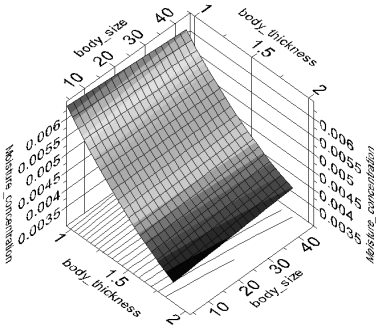
Package Warpage	Interface stress
	
Moisture mass	**Moisture concentration**
	

Figure 7.9: 3D responses as function of body size and thickness.

The structural similarity rules can be deduced from Figures 7.8 and 7.9, and it becomes very clear that the die-to-pad ratio is an important parameter in the eventual response of the BGA package family. It is therefore advised to include this ratio into the structural similarity rules and replace:

- Has the same or smaller diepad size,
- Has the same of smaller die size,

  With:
- Has the same or smaller die-to-pad ratio.

The strength of the presented optimisation technique is that the global non-linear response of package families can be captured in the earliest phases by the RSM models. These RSM models are no more than (polynomial) relationships describing the responses as function of input variables. The polynomial formulas can be transported in to easy software tools such as Excel. In this way, the results of non-

linear FE tools can be made accessible for package designers. An example of such a tool is created, where the specified parameters of the BGA family are input and the resulting thermo-mechanical and moisture-diffusion responses are the output. Such tools may shorten the design cycles for new packages and/or new package concepts.

7.5 Conclusions

Advanced structural similarity rules can be achieved through simulation-based optimisation techniques by generating reliable RSM models. In this chapter, DOE/RMS techniques are used to deduct the thermo-mechanical and moisture-diffusion responses as function of six geometrical parameters. Parametric 3D non-linear FE models are used to explore the responses of the complete BGA family. Advanced structural similarity rules are deduced, which can be used to shorten design cycles. Even more, by combining the accurate 3D non-linear reliability prediction models an Excel-based structural similarity tool is created that can be operated by package designers. By using this tool, the number of reliability qualification tests can be reduced. More importantly, possible failure mechanisms can be (better) understood and predicted.

Chapter 8

Driving Mechanisms of Delamination Related Reliability Problems in Exposed Pad Packages[1]

Exposed pad packages were introduced in the late 1980-1990s because of their excellent thermal and electrical performance. Despite these advantages, the exposed pad packages experience a lot of thermo-hygro-mechanical related reliability problems during qualification and testing. Examples are dielift, which occurs predominantly after MSL conditions and die-attach to leadframe delamination leading to downbond stitch breaks during temperature cycling. In this chapter, non-linear FE models using fracture mechanics based J-integral calculations are used to assess the reliability problems of the exposed pad package family. Using the parametric FE models any geometrical and material effects can be explored to their impact on the occurrence diepad delamination and dielift. For instance the impact of diepad size is found to be of much less importance as the impact of die thickness is. Using the fracture mechanics approach, the starting location for the delamination from thermo-hygro-mechanical point of view is deducted. The results indicate that when diepad delamination is present, cracks are likely to grow beneath the die and dielift will occur. The interaction between dielift and other failure modes, such as lifted ball bonds, are not found to be very significant. The FE models are combined with simulation-based optimisation methods to deduct design guidelines for optimal reliability of the exposed pad family.

8.1 Introduction

Exposed pad packages, such as H(L/T)QFP, QFN, H(T)SSOP, are introduced in the late 1980-1990s because of their excellent thermal and electrical performance. Despite these advantages, a lot of thermo-hygro-mechanical related reliability problems are observed during qualification and testing of the exposed pad family. Examples are:

- Dielift, predominantly after MSL conditions. Dielift means delamination between die-attach and leadframe, and in some cases delamination between die-attach and

[1] Reproduced from: van Driel, W.D., M.A.J. van Gils, G.Q. Zhang, L.J. Ernst, Driving mechanisms of delamination related reliability problems in exposed pad packages, IEEE Transactions on Components and Packaging Technologies, in press, 2007b.

the die. As a result of the dielift, lifted ball bonds may occur during thermal cycling.

- Downbond stitch breaks associated with diepad delamination after MSL assessment and subsequently thermal cycling testing. There might be a correlation between diepad delamination and dielift.

These reliability problems are driven by the mismatch between the different material properties, such as CTE, hygro-swelling, vapor pressure induced expansion and degradation of the interfacial strength due to moisture absorption. The associated negative business consequence is significant. Until now, there is no solution available in the industry that solves the reliability problems of the exposed pad family. Clearly, the driving mechanisms of these delamination related problems should be explored before possible solutions can be found, such as double downset leadframes, grooves in the diepad, locking holes and/or other die-attach types to limit the dielift and/or delamination. This chapter highlights the results to find the driving mechanisms for delamination-related reliability problems in exposed pad packages using state-of-the-art virtual thermo-mechanical prototyping techniques.

First of all, novel interfacial adhesion test techniques are developed to measure the interfacial strength as functions of both temperature and moisture. These techniques are modifications and improvements of the well-known four point bending test. Using smartly designed samples, the interfacial strengths between moulding compound and exposed pad and between die-attach and exposed pad are quantitatively characterized. Secondly, several reliable non-linear FE models in 2D are developed to predict the moisture diffusion, deformation, stress and interfacial energy history as functions of processes, temperature and moisture loading. As such, the effect of hygro-swelling, vapour pressure, interfacial degradation and thermal expansion on the failures in the exposed pad family is predicted. A lot of effort is spent on developing reliable material models, based on our dedicated material characterization methods covering both thermo-mechanical and moisture properties. As a result, accurate material models, such as anisotropy for silicon, visco-elasticity for moulding compound and die-attach, elasto-plasticity model for copper, is used in our multi-physics damage modelling. Finally, by combining the FE modelling with simulation-based optimisation methods, design guidelines can be derived for reducing reliability problems for the exposed pad family. Such results also provide generic

insight in the mechanisms of delamination-related problems for the exposed pad family.

8.2 The Exposed Pad Family

An exposed pad package is a package composed of an IC attached to an exposed pad and in a later stage encapsulated with an epoxy moulding compound. It has been introduced into the semiconductor industry as a thin, cost effective, thermal and high frequency package solution. The exposed pad is a metal plate that is located on the bottom of the package. Exposed pads on the top of the package are less common but they exist. Many variations exist; exposed pads are found on many packages types. Mature package types with gull wing leads, such as TSSOP, offer exposed pads as an optional configuration. The exposed pad is a standard feature for QFN packages. For the leaded packages with a gull wing lead, exposed pad products are made using leadframes with a 'deep downset' paddle which is exposed to the outside of the package after the mould process. Figure 8.1 shows two examples for a gull wing exposed pad package and a QFN package. Exposed pad features and benefits are low profile (1.2mm maximum height), low loop inductance, excellent thermal performance and cost effective. Exposed pads increase the maximum power dissipation of packages due to its increased thermal performance. In most applications, the exposed pad is used as an electrical ground. To do so, so-called down-bonded wires are attached from the IC to the exposed diepad.

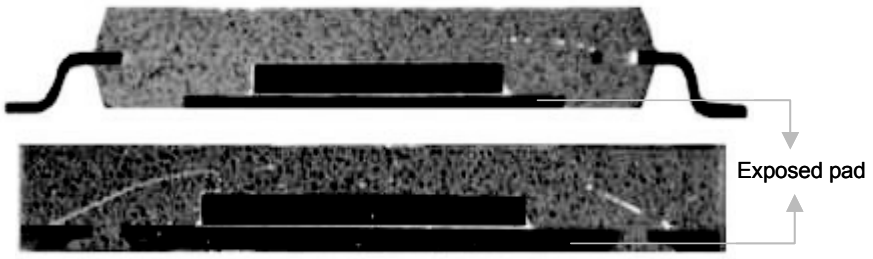


Figure 8.1: Examples for exposed pad packages: gull wing leads (top) and QFN version (bottom).

Despite the advantages, a lot of thermo-hygro-mechanical related reliability problems are observed during qualification and testing of the exposed pad family. A common failure mode in exposed pad packages is downbond stitch breaks after

temperature cycling testing. It is known that this failure mode is associated with diepad delamination after MSL assessment [van Driel, *et al.*, 2004a]. Another common failure mode in the exposed pad family is the so-called dielift mode. Dielift means delamination between die-attach and leadframe, and in some cases delamination between die-attach and die. Dielift is predominantly found after a Moisture Sensitivity Level (MSL) assessment and not only depends on the moisture and temperature conditions but also on material choices and process conditions. Dielift may endanger the thermal performance of the exposed pad package. As a result of the dielift, lifted ball bonds on the IC level may occur during thermal cycling. Even more, there might be a correlation between diepad delamination and the dielift phenomenon. As such, dielift is a complicated failure mode, which needs further analysis to answer the following questions:

- What are the domination factors for occurrence of delamination in exposed pad packages? For instance, what is the impact of diepad size and die thickness?
- What location is the starting point for the delamination from thermo-hygro-mechanical point of view? Is it more likely to occur at the diepad top or side?
- What is the interaction with other failure modes, such as lifted ball bonds?

Figure 8.2 shows typical examples of delamination areas in the exposed pad package.

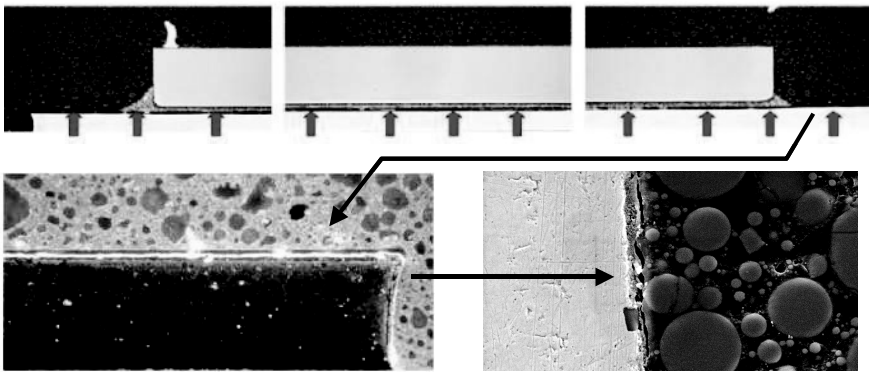


Figure 8.2: Typical delamination locations in exposed pad packages: dielift (top), top diepad delamination (bottom-left) and side diepad delamination (bottom-right).

Delamination in packages is related to the interfacial strength of two adjacent materials. For the given moulding compound leadframe interface different interface strength test methods are used to determine the interface fracture toughness between

the materials. The methods, sample fabrication, test conditions and the results are described in Chapter 4. In short:

- Under dry conditions, a temperature of 20ºC and moulding compound MCA, the fracture toughness is about 6J/m^2 under four-point-bending loading. At a higher mode mixity this value may increase up to 25-30J/m^2.
- There is significant effect of the moulding compound type on the fracture toughness; a 2.5x higher value can be reached.
- Oxidation and/or accumulation of contamination on the Au surface of the leadframe have a very negative effect of the toughness values; a 60% decreased value is found.

8.3 Multi-Physics FE Modelling

A 2D non-linear FE model including anisotropy for silicon, visco-elasticity for moulding compound and die-attach, elasto-plasticity for the copper leadframe is constructed. A multi-physics FE methodology is used which can take into account the moisture and thermo-mechanical related mechanisms. The effects of hygro-swelling, vapour pressure and thermal expansion on the failures in the exposed pad family are modelled. All the appropriate materials in the package (moulding compound and die-attach) have been characterized with regard to their moisture behaviour under MSL1 and MSL3 conditions. It is assumed that the moisture uptake in the polymer materials can be described with Fick's Law of Diffusion. Moisture diffusivity, D, and the saturated moisture concentration, C_{sat}, are measured using moisture absorptions measurements at MSL1 (85°C, 85%RH) and MSL3 (30°C, 60%RH) conditions, the results are listed in Chapter 4. For the determination of the moisture expansion coefficient (CME), combined TMA/TGA experiments have been performed at 85˚C on saturated samples. Combining the obtained results of moisture desorption and shrinkage as function of time, the CME can be estimated [van Gils *et al.*, 2004]. These results are also listed in Chapter 4.

For predicting delamination growth of an existing delamination, LEFM (Linear Elastic Fracture Mechanics) is applied using the J-integral approach. The J-integral value is calculated at the interface and represents the available energy to delaminate the interface. Based on plane strain assumption two-dimensional FE models are constructed to calculate the value of the J-integral, as function of hygro-thermo-

mechanical loading. J-integral values are calculated at different interfaces within the package, see Figure 8.3. Besides this, a cohesive zone approach is used to examine the most likely delamination progression pathways in the package.

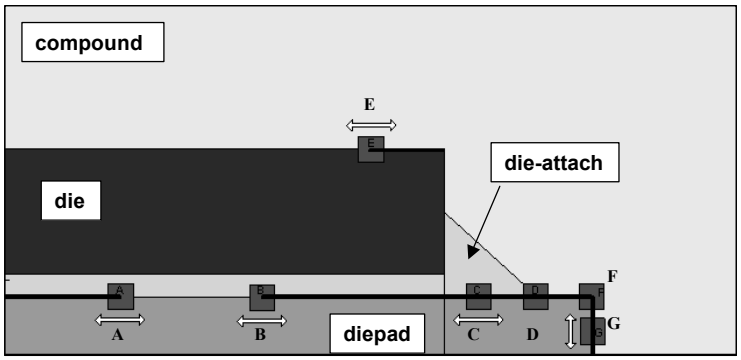


Figure 8.3: At locations A - G the J-integral values are predicted.

Figure 8.4 shows the fully parametric 2D FE model with some typical crack-tip meshes. Through a solid mesh sensitivity analysis the eventually used mesh size is fixed. Different integration-paths are analysed to fix the path to calculate the eventual J-integral value. As a nominal model, the HLQFP144 is selected with body size 20x20x1.4mm^3; diepad size 5.6x5.6x0.125mm^3; die size 4.5x4.5x0.38mm^3 and material combination DA1, MCC, Cu leadframe, Silicon IC and moisture level MSL3. Figure 8.5 shows the loading scheme, including the thermal, moisture and vapour pressure loading that is used in the FE model.

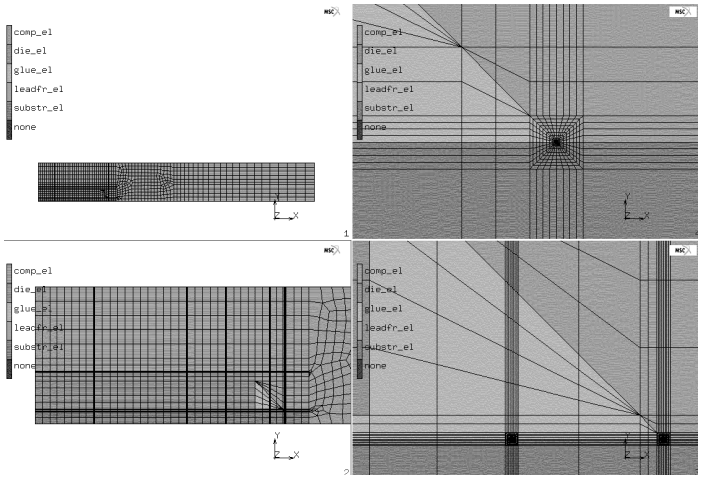


Figure 8.4: FE mesh for the exposed pad package (left) and typical crack-tip meshes to calculate J-integral values (right).

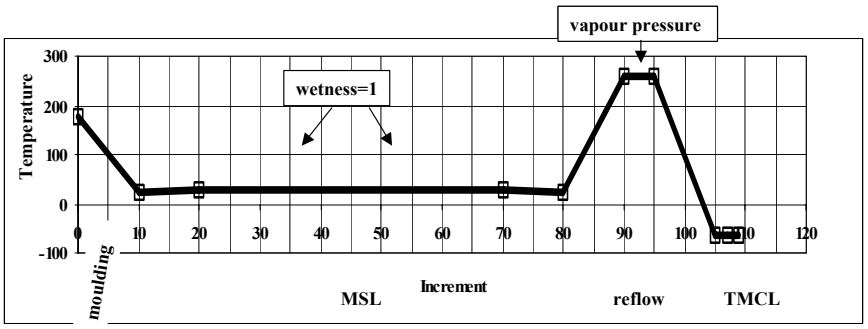


Figure 8.5: Loading scheme: thermal, moisture and vapour pressure are subsequently added.

8.4 Results

Figure 8.6 shows the locally deformed structure after moulding and MSL loading conditions. It is clear that the die-attach pulls at the exposed pad and high J-integral values are expected in this location. Due to the moisture loading, the swelling of the compound and die-attach decreased these local deformations, and thereby, closes any interface present.

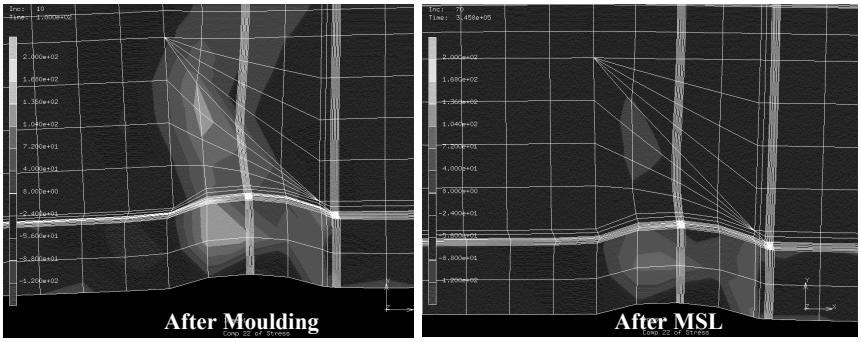


Figure 8.6: Deformed structure at the die edge in the exposed pad and die-attach area after moulding (left) and MSL (right) loading conditions.

Figure 8.7 shows the mode mixity along the diepad for the nominal model, 0% is the starting point at the side of the pad, 20% is the corner point, 40% is the point of the die-attach fillet, 60% is exactly below the die, 100% is at the symmetry line.

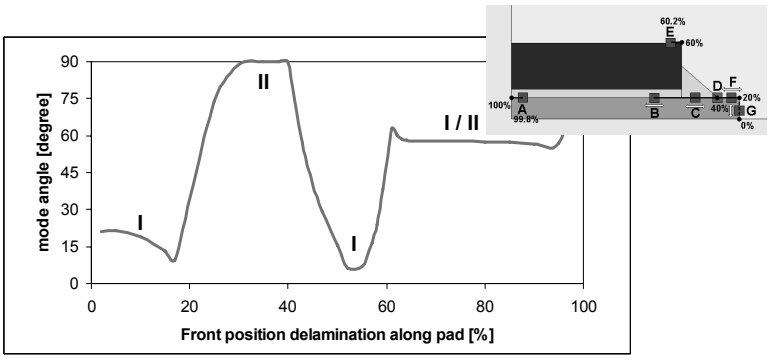


Figure 8.7: Mode mixity along the diepad interface.

Figure 8.7 shows that:

- At the diepad side (between 0-20%), the interface is loaded under a mode mixity of 20º. The interface toughness value for compound-leadframe at 20ºC is 6J/m^2. Remember that these values may drop with a factor 3 when the leadframe is contaminated and/or oxidized.
- At the top of the diepad (between 20-40%), the interface is loaded under a mode mixity of 90º (pure mode II, shear loading). The toughness value at 20ºC under this mode is >25J/m^2.
- Under the die-attach fillet (between 40-60%), the mode mixity drops to 10º (almost pure mode I, tensile loading) and rises to 60º when it reaches the die corner. The toughness values for this interface under this mode would be about 10-25J/m^2 at 10º and rising to 100-125J/m^2 at 60º.
- Under the die (between 60 to 100%), the mode mixity remains constant at 60º, where a toughness value of 100-125J/m^2 is expected (probably even higher but no data is available / measured at this mode).

These values can be compared with the calculated ones during manufacturing, processing and testing. Figure 8.8 shows the calculated J-integral values at the different locations as function of the loading conditions. In this case, J-integral values are calculated for the nominal package. The following can be concluded from this figure. At the side of the pad (location G and F), the J-integral values are below 5J/m2 during processing, indicating that this interface will not fail from a thermo-mechanical point of view. It will only fail when this interface is contaminated, since the toughness value will drop below 2J/m^2. During TMCL, the J-integral values increase to 10J/m^2 and are getting closer to the toughness values. During cool down from the moulding

temperature the J-integral values at the locations B and C (interface die-attach with leadframe) increased dramatically and seem to exceed the measured values. Especially at location C, directly below the die corner, the J-integral values rise until $50J/m^2$ after moulding and $150J/m^2$ during TMCL testing and are beyond the measured toughness values. During MSL testing, the J-integral values drop. This is due to the expansion of the compound as a result of moisture uptake. When swelling the compound closes the interface and J-integral values decrease. The effect of the moisture is purely degrading the interface toughness with 20-40%. The results indicate that delamination will occur at the die-attach border, have the tendency to progress until point B, but not until point A (lower J).

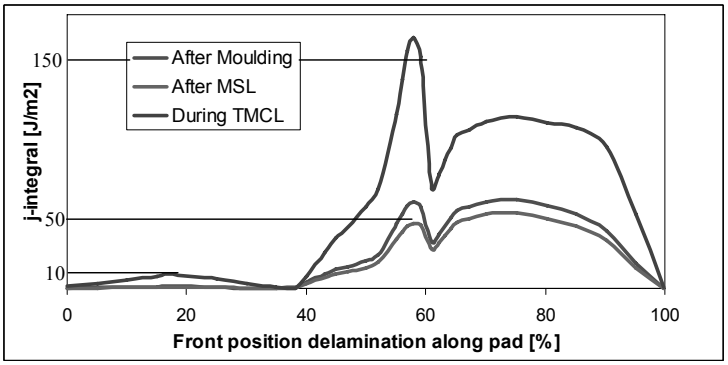


Figure 8.8: J-integral values at the different locations as function of the process conditions.

As shown above, the most likely place for the delamination to start is below the die corner in the die fillet region. A FE simulation is performed using cohesive zone elements (or interface elements) along the diepad interface. Cohesive zone techniques are different from J-integral techniques that it allows the calculation of progression of interface delamination. In the cohesive zone elements the interface toughness values in the different modes are given as an input. However, cohesive zone simulations may take much more computer CPU time. For the nominal model only, a cohesive zone simulation is performed to predict the most likely pathway for interface delamination in exposed pad packages during processing. Figure 8.9 shows the results of this simulation, where the interface delamination is highlighted. The cohesive zone simulation confirmed the J-integral simulations: the place where the delamination will start is below the die corner in the die fillet region. As the loading increases, by

thermo- or hygro-mechanics, the interface delamination progresses below the die. In a next stage, when the delamination below the die has reached a certain length, the forces at the side of the diepad are increased and exceed the toughness values. Almost instantly the complete side and top of the diepad delaminate in this stage. Finally, total dielift with total diepad delamination will occur, see the last picture in Figure 8.9. This is the thermo-hygro-mechanics based delamination pathway for exposed pad packages during processing and testing.

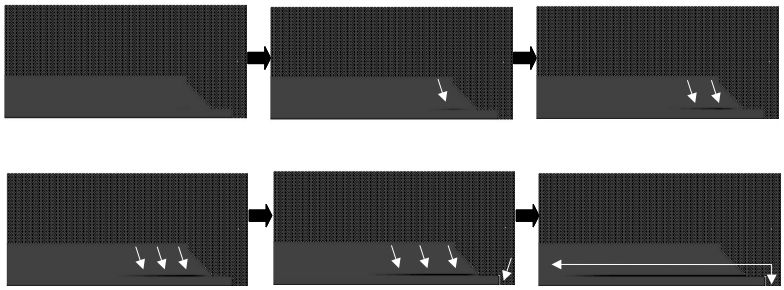


Figure 8.9: Results of the cohesive zone simulation showing the delamination pathway driven by the thermo-hygro-mechanical loadings.

- *Effect of MSL1*

Using the parametric FE model, different features can be explored. The first feature explored is the effect of the MSL level, 3 versus 1. Figure 8.10 shows the resulting J-integral along the diepad interface during TMCL testing. MSL1 moisture loading increases the moisture absorption and due to this also the maximum J-integral value (during TMCL) increases with a factor 20-30%. Notice that along the diepad (0-40%) the increased MSL level hardly increases the J-integral values.

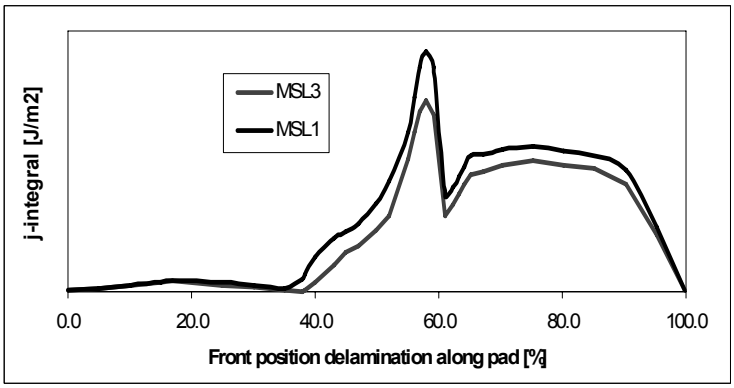


Figure 8.10: Effect of MSL level on the J-integral level.

- *Effect of dielift on ball-lift*

As mentioned before, total dielift may facilitate other failure modes, such as lifted ball bonds on top of the IC, during TMCL testing. Figure 8.11 shows J-integral values at the different locations C, D, G and E. The J-integral value for location E (on top of the IC) is calculated when the total diepad is delaminated (thus including total dielift). This J-integral value at location E is very low indicating that the relation between dielift and lifted ball bonds is not that significant.

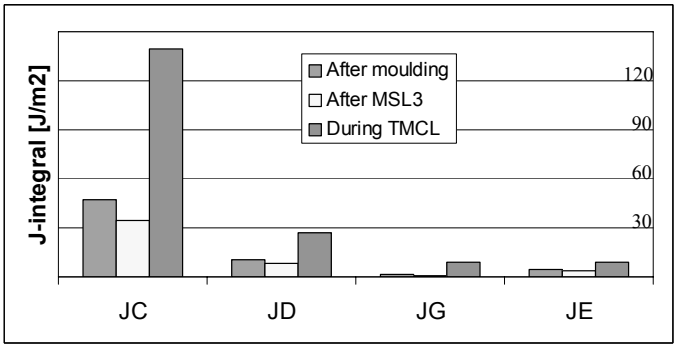


Figure 8.11: J-integral values at specific locations during processing and testing.

- *Effect of package type*

Exposed pad packages exist in different package types, all having a different body, leadframe and/or die thickness. Figure 8.12 shows the J-integral values for a comparison between QFN and HLQFP types. In QFN, the standard thickness equals 0.85mm for the body, 250µm for the IC, and 200µm for the leadframe. In HLQFP, these values are equal to 1.40mm, 380µm and 125µm.

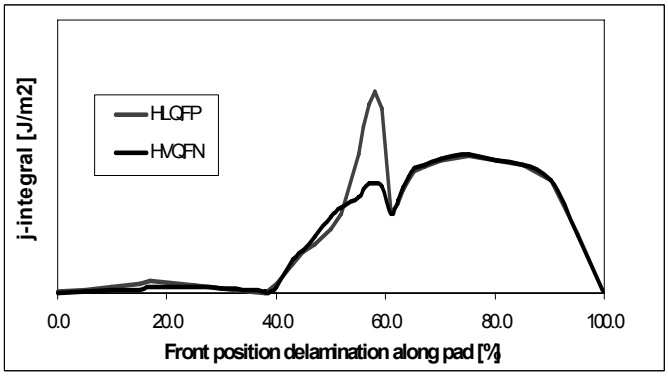


Figure 8.12: J-integral values along the diepad for HLQFP and QFN package type.

These results clearly show that the QFN package type causes lower J-integral values below the die, which is a combined effect of fillet height and vertical stiffness ratios.

- *Effect of moulding compound*

Figure 8.13 shows the calculated J-integral values when using compound MCA instead of MCC. Compound MCC slightly reduces the crack driving force, and even more, higher interface toughness values are found in the adhesion tests. Figure 8.13 explains why for MCA gaps are found rather around the diepad (and dielift), and even more, why these gaps tend to be larger.

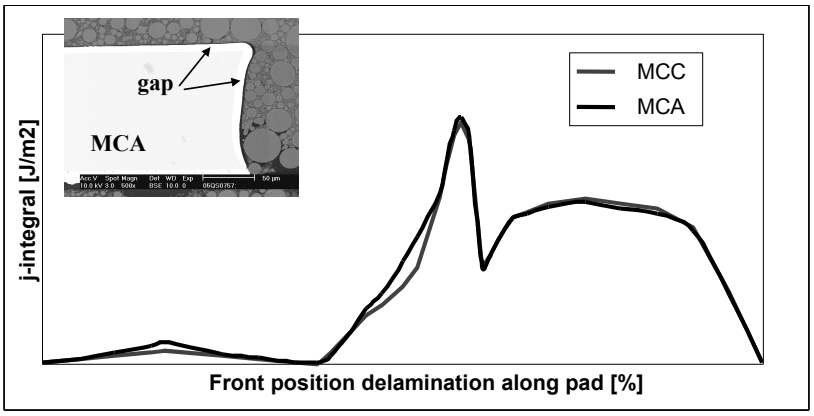


Figure 8.13: J-integral values along the diepad for MCC and MCA compound. SEM picture shows experimental qualification result for MCA.

- *Effect of die-attach fillet height*

Figure 8.14 shows the effect of the die-attach fillet height for the J-integral values at the locations G (side of the pad) and D (below the IC corner). At the side of the pad, the J-integral values more or less remain constant when increasing the die-attach fillet height but below the IC, the J-integral values strongly increase when increasing the die-attach fillet height. This is a result of the increasing pulling forces that the die-attach imposes to the leadframe in this location. From this result it can be deducted that a proper fillet height control is very crucial. It should be noted that the effect of die thickness is not dominant for location D since the fillet height overrules it.

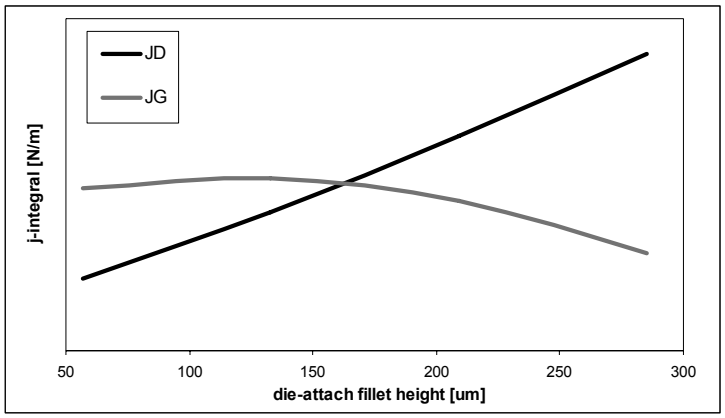


Figure 8.14: J-integral values as function of the die-attach fillet height for locations D and G.

8.5 RSM based Design Rules

A numerical DOE is performed using the following parameters:

1. Body size, increasing from 3x3mm^2 to 24x24mm^2
2. Pad-to-body ratio (length based) from 15% to 60%
3. Die-to-pad ratio (length based) from 10% to 85%.

A space-filling Latin-Hypercube design consisting of 30 variations is constructed. For the responses, the J-integral values at the locations C and G are chosen. Figure 8.15 shows the effect of body size and pad-to-body ratio on the calculated J-integral values on the G location (side of the pad). It is clear that both the body size and the pad-to-body size have no effect on the occurrence of pad side delamination. The same result is found for the die-to-pad ratio. Figure 8.16 shows the effect of J-integral values below the corner of the die (location C), in other words the occurrence of dielift, as function of the body size and the pad-to-body ratio. As the body size and the pad-to-body ratio increase, the J-integral value decrease from 190J/m^2 to 130J/m^2 (32% reduction) indicating that for larger packages the thermo-hygro-mechanical effects for dielift occurrence diminish. Note that for larger packages, the interface toughness may increase or decrease due to some processing effects. From these results it can be deducted that:

- Dielift is not related to package size and/or package internal ratios. There is no need to set-up a design rule for this feature. It is very important to secure interface

toughness in exposed packages by proper processing (curing time, no/limited leadframe oxidation and/or contamination).

Table 8.1 lists an overview of all the effects as simulated by the FE analysis. Indications are from +++ (large increasing impact) / ++ / + / 0 (no impact) / - / -- / -- (large decreasing impact).

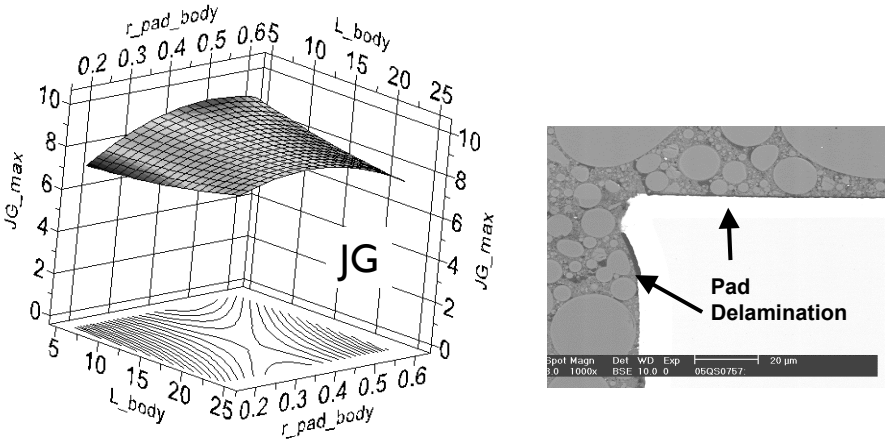


Figure 8.15: Effect of delamination on the side of the pad (location G) as function of body size and pad-to-body ratio.

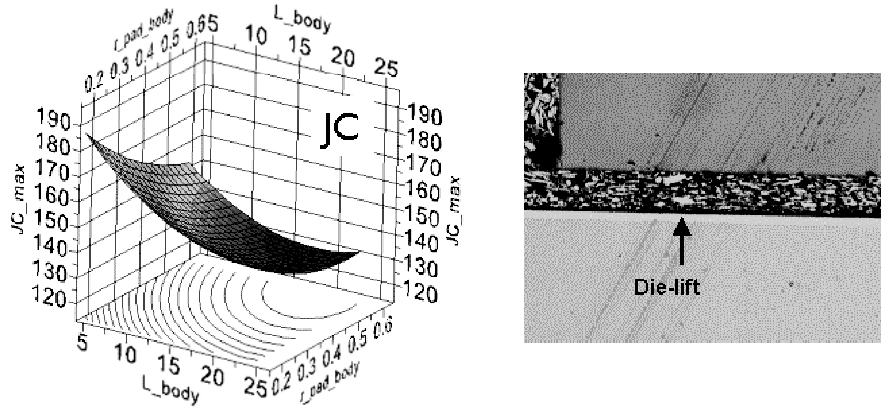


Figure 8.16: Dielift occurrence as function of body size and pad-to-body ratio.

Table 8.1: Effect overview (+++/++/+/0/-/- -/- - -).

Item / variation	Impact	Remarks
MSL1 vs. MSL3	++	Less at pad top and side
Vapour pressure	+	Becomes higher with large 'closed' delaminations
Effect of dielift on ball-lift	0	No correlation at all, at least for exposed pad packages
QFN vs. HLQFP	-	Especially below the die, lower J-integral values are calculated.
Effect Compound	+	MCC performs a bit better; has a higher interface toughness
Increased die-attach fillet height	+++	Very dominant effect of fillet height, predominantly on occurrence of dielift
Increased body size; pad-to-body ratio; die-to-pad ratio on pad delamination	0	No effect at all.
Increased body size; pad-to-body ratio; die-to-pad ratio on pad delamination	-	J-integral values below the die decrease when increasing these values

8.6 Conclusions

Despite the electrical and thermal advantages, the exposed pad packages experience a lot of thermo-hygro-mechanical related reliability problems during qualification and testing. In this chapter, interfacial adhesion test results are combined with non-linear FE models using fracture mechanics based J-integral calculations to assess the reliability problems of the exposed pad package family. Using the parametric FE models any geometrical and material effects can be explored to their impact on the occurrence delamination and/or dielift. For instance the impact of diepad size is much less as the impact of die thickness. Even more, the models can be used to find the starting location for the delamination from thermo-hygro-mechanical point of view. The results indicate that when diepad delamination is present, cracks are likely to grow beneath the die and dielift will occur. The interaction between dielift and other failure modes, such as lifted ball bonds, are not found to be very significant. Even

more, the modelling work combined with the strength measurements have shown that from thermo-hygro-mechanical point of view this interface should not delaminate, unless it's toughness is not secured by a proper material choice and/or processing. The degradation of the compound and die-attach to leadframe interfaces combined with the imposed thermo-hygro-mechanical forces will lead to the reliability problems. Therefore, it is vital to secure processing conditions of the exposed pad family by proper curing of moulding compound and/or die-attach materials to obtain sufficient interface toughness, secure leadframe storage under controlled environmental conditions to prevent oxidation and/or contamination and/or introduction of a cleaning step for those leadframes for which dielift is a known risk.

Delamination is a key trigger of mostly observed reliability problems in the microelectronics industry. As such, not only those materials having sufficient interface toughness should be selected but also design choices should be made able to withstand increased forces due to the occurrence of delamination. Prediction models may support these choices.

Chapter 9

Conclusions and Recommendations

9.1 Conclusions

The aim of this thesis is twofold. First, it aims to develop a general virtual thermo-mechanical prototyping framework that is able to predict the non-linear responses in microelectronics devices during manufacturing and testing. This includes the development of accurate and efficient methods for both DOE / RSM approaches and thermo-mechanical prediction models. Secondly, the developed framework is applied to four different reliability problems in microelectronics devices.

To meet the first objective, a general virtual thermo-mechanical prototyping framework has been developed. This framework is described in Chapters 3 and 4. From these chapters, it is concluded that:

- Simulation-based optimisation methods based on a space-filling Latin Hypercube design of experiments combined with quadratic and/or Kriging RSM methods are applicable to address virtual thermo-mechanical prototyping of microelectronics devices.
- Sequential methods like EGO that embeds the choice of the DOE points with the optimisation process decrease the simulation time without sacrificing the same accuracy for the eventual response surface. This may result in a substantial reduction of overall computational costs in case of problems involving non-linear FE models.
- In order to obtain accurate and reliable prediction models for IC structures, the intrinsic stress levels should be taken into account. Dedicated experiments are described in this thesis to measure the wafer warpage as function of temperature and to obtain intrinsic stress values of IC materials.
- Time- and temperature dependent properties of IC package constituents cannot simply be neglected if reliable virtual thermo-mechanical prototyping is desired. In this thesis it is shown that when assuming linear elastic, isotropic behaviour for packaging constituents such as die-attach and/or moulding compounds thermally induced deformations are under predicted.

- The total manufacturing process, in terms of thermal, mechanical and moisture history history, should be included in the FE models in order to correctly predict the stress and strain history. Element birth and death techniques to activate and/or deactivate constituents at the appropriate process temperature are strongly recommended. It is shown that thermal deformations from non-linear FE models match well with measured deformations for microelectronic packages by using interferometer techniques.
- To apply fracture mechanics, virtual prototyping techniques should be integrated with interface strength characterization experiments. In this thesis, the four point bending test is used to characterize the adhesion strength between leadframe and epoxy materials as function of temperature, moisture, storing conditions and mode mixity. Proper interface characterization methods should be used in conjunction with material selection procedures to further reduce the time and efforts spend on material qualification tests.
- To address moisture related reliability problems in microelectronics devices using virtual prototyping techniques, experiments are a needed to characterize the moisture diffusivity, absorption and swelling of the packaging constituents. In this thesis, a moisture diffusion model is presented using the thermal analogy. It is shown that by using this analogy, calculated moisture content of different packages match within 5% with measured values. High moisture concentrations in IC packages weaken interfacial adhesion, generate vapour pressures during reflow and induce hygro-thermo-mechanical stresses and strains in microelectronics devices.

The second objective concerns the application of the developed framework for different reliability topics in microelectronics devices. For all four case studies described in Chapters 5, 6, 7 and 8 a good correlation of the developed framework with experimental results is shown, thereby proving the predictability of the techniques. The results of both the strongly non-linear analytical cases and the real industrial applications clearly demonstrate that with sufficient knowledge and proper execution, the added value of virtual thermo-mechanical prototyping can be realized. In more details, it is concluded from the industrial applications that:

- In Chapter 5 the developed framework is used to optimise a real IC package case. The virtual thermo-mechanical prototyping results showed that a thinner leadframe

thickness could be well feasible. Next, a full qualification program is executed using the optimised leadframe thickness yielding no reliability issues. A significant cost reduction of 260k$ per year is obtained by the new package with no loss in reliability performance. More specific, this application clearly shows that virtual thermo-mechanical prototyping of microelectronics devices may lead to an optimised packaging geometry prior to any physical prototyping.

- In Chapter 6 it is demonstrated how *IC package stress design rules* can be generated using the developed framework. Several FE models are built to determine the mechanisms of passivation cracking and metal shift during wafer backend processes and package assembly. The numerical work is combined with a limited number of test samples to verify the simulation results and predict failures prior to prototyping of real IC metal structures. This combined approach revealed a significantly different picture than what is described by the current design rules. Although the simulations are performed for a given IC and packaging technology, based on the similarities, it is expected that many other will have the same/similar results with respect to the effects of all the variables investigated here. This means that there will be a great possibility to improve the current *IC package stress design rules* based on virtual thermo-mechanical prototyping.
- In Chapter 7 the developed framework is used to achieve advanced structural similarity rules for a given package family. A series of advanced structural similarity rules are deduced, which can be used to shorten design cycles. Even more, by combining the accurate 3D non-linear reliability prediction models an easy access tool is created that can be operated by package designers. By using this tool, the number of reliability qualification tests can be reduced. More importantly, possible failure mechanisms can be (better) understood and predicted.
- In Chapter 8 thermo-hygro-mechanical related reliability problems of exposed pad packages are the subject of study. Interfacial adhesion test results are combined with non-linear FE models using fracture mechanics based J-integral calculations to assess the known delamination problems of this package family. The virtual prototyping results combined with the strength measurements show that from thermo-hygro-mechanical point of view this interface should not delaminate, unless it's toughness is not secured by a proper material choice and/or processing. To prevent interface delamination, it is vital to secure the processing conditions of the exposed pad family

by proper curing of moulding compound and/or die-attach materials to obtain sufficient interface toughness, secure leadframe storage under controlled environmental conditions to prevent oxidation and/or contamination and/or introduction of a cleaning step for those leadframes for which interface delamination is a known risk. This application shows that prediction models can support design choices needed to withstand increased forces due to the occurrence of interface delamination.

The overall conclusion from the work presented in this thesis can be formulated as:

> *To cope with the development needs of microelectronics, virtual thermo-mechanical prototyping is an effective and efficient way to predict, qualify, optimise and design microelectronics against the actual requirements prior to major physical prototyping, manufacturing investments and reliability qualification tests. The success of virtual thermo-mechanical prototyping mainly depends on accurate and efficient prediction models, advanced simulation-based optimisation algorithms and methods and software tools being able to seamlessly and efficiently integrate prediction models with optimisation algorithms.*

9.2 Recommendations

The recommendations with respect to virtual thermo-mechanical prototyping for microelectronics devices are strongly related to its characteristics. In reality, these characteristics will inevitably interact with each other. First of all, microelectronics technologies and products are multi-scale in both geometric and time domains. In the geometric domain, the typical feature sizes range from nanometers to millimetres and will continue to shrink for at least another 15 years. From both application needs and academic challenges, there is an urgent need to understand the multi-scale phenomena and to develop theories, methods and tools to eventually predict the associated responses. It is recommended to spend effort on developing non-continuum mechanical theories capable of simulating the behaviour of microelectronics with micron, deep-submicron and nano dimensions. A bridge should be developed to close the gap between non-continuum theories, simulation tools and results of atomistic scale with the continuum theories, simulation tools and results on the macro-scale level.

Secondly, microelectronics corresponds to multi-technology, multi-loading and multi-discipline. From a technology aspect, the major manufacturing chain can even go beyond the traditional semiconductors technology as described in Chapter 2. Multi-technology results in multi-loading. Various loading types, such as thermal, mechanical, humidity, chemical, electrical and combinations hereof are commonly presented in different life cycles of various microelectronics products. Multi-physics simulation and verification capabilities to capture the strong interaction effects between different disciplines are essential for microelectronics. Commercially available FEM tools are all originated from the needs and knowledge of solving mechanical related problems. Therefore it is recommended that more effort should be spent on the development of sophisticated multi-physics and multi-scale models, efficient numerical algorithms and user interface code integration methods, as well as advanced computational techniques.

Thirdly, microelectronics contains multi-materials and multi-interfaces. Faster than ever, various types of new materials are being developed and introduced in microelectronics devices. Material development is becoming an indispensable and integrated part of new technology development. These materials exhibit strongly time and temperature dependent properties. Applications of these time and temperature dependent materials in microelectronics will make the final products in use also time and temperature dependent. Mainly because of this the microelectronics industry is confronted with the dilemma of unclear correlations between application profiles and reliability specifications and between application profiles with accelerated testing conditions. It is recommended that more effort is spend on finding these correlations by using combined experimental and virtual prototyping methods.

Fourth, reliability test results are showing multi-failure mechanisms, multi-failure modes and multi-failure locations. Typical failure modes confronted by other industries and applications, such as cracks, delamination, fatigue and corrosion are all observed in microelectronics devices. Strong interaction among these different failure mechanisms and failure modes in either simultaneous or sequential way, have also been observed. Although it is, even for single failure mode prediction, tough to describe the damage initiation, evolution and eventual failures there is no computational framework and algorithm available to deal with the simultaneously occurring failure modes. It is strongly recommended to spend a significant amount of effort to predict multi-failure modes.

Finally, delamination is probably the most prevalent and pervasive issue in the microelectronics industry. Driven by the rapid integration development, a dramatically increase in both the number and the type of interfaces is observed. Although interfacial adhesion is studied for decades, the vast majority focus on either the chemical, or the physical, or the mechanical aspect alone. Because of such compartmentalized approaches, no effective methodologies, models and tools are available for the prediction of interfacial strength in microelectronics, for given product, process and material characteristics. It is strongly recommended to develop a generic framework for prediction of interface strengths in microelectronics devices in order to upfront tailor and manipulate material and interface properties and behaviour for specific application needs.

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Summary

The era of microelectronics started in the early 1960's and since then grew with an enormous speed. Microelectronics have pervaded our lives for the past fifty years, with massive penetration into health, mobility, safety and security, communications, education, entertainment and virtually every aspect of human lives. The main technology drivers that enabled this expansion are miniaturization and integration. Moore's law is the driver for miniaturization with the ongoing trend of smaller feature sizes. Integration of different microelectronics technologies is captured by what is now called 'More than Moore'. However, the combination of these two has driven microelectronics technology into an unknown level of complexity and as a consequence, we are confronted with increasing difficulties to meet quality, robustness and reliability requirements. In this thesis, a general virtual thermo-mechanical prototyping framework is developed that is able to predict the non-linear responses in microelectronics devices prior to physical prototyping and/or reliability testing.

The framework developed in the present thesis relies on the development of accurate and efficient simulation-based optimisation methods, being Design Of Experiments (DOE) and Response Surface Models (RSM). Space-filling Latin Hypercube DOE's combined with quadratic and/or Kriging-based RSMs are found to be applicable. Using sequential methods like Efficient Global Optimisation (EGO) may result in a substantial reduction of overall computational costs in case of problems involving non-linear Finite Element Methods (FEM). These simulation-based optimisation methods are combined with accurate and efficient thermo-mechanical prediction models that are able to capture the non-linear responses of microelectronics devices. It is found that in order to do so, a series of requirements are needed. In the first place, this includes dedicated measurements of intrinsic stress levels in IC structures, the determination of the time, temperature and moisture dependent properties of microelectronics constituents and adhesion strength values using proper interface characterization methods. In the second place, the total manufacturing process in terms of thermal, mechanical and moisture history should be taken into account in the prediction models.

The uniqueness of the developed framework relies, for the first time, on the following three aspects:

- The development of advanced simulation-based optimisation algorithms and methods.
- The development of accurate and efficient thermo-mechanical prediction models able to capture the damage responses within microelectronics devices during manufacturing and reliability qualification tests.
- To seamlessly and efficiently integrate the prediction models with the optimisation algorithms.

The developed framework is applied to four case studies of reliability topics in microelectronics devices. The investigated topics include chip fractures in power packages, passivation cracks and metal shift in ICs, structural similarity rules for laminate-based packages and delamination in exposed pad packages. The results of these four case studies correlate well with experiments and/or field returns and prove the predictability of the developed techniques.

The first investigated reliability topic concerns the optimisation of a real IC package towards the prevention of die cracks. The developed framework predicted that a thinner leadframe is feasible; a full qualification program, which yielded no reliability issues, confirmed this. This application clearly shows that the developed framework may lead to an optimised packaging geometry, a significant cost reduction with no loss in reliability performance prior to any physical prototyping. The second topic concerns the interaction between IC and package towards the prevention of passivation cracking and metal shift. The numerical work is combined with a limited number of test samples to verify the simulation results and to predict failures prior to prototyping of real IC metal structures. This combined approach revealed a significantly different picture than what is described by the current design rules. This implies a major possibility to improve the current rules. The third topic concerns the development of structural similarity rules, which determine to what extend reliability test results from a specific device can be representative for other similar types. By using the developed framework, a series of similarity rules is deduced to reduce the number of reliability qualification tests. The fourth and last topic concerns exposed pad packages, which are quite vulnerable for interface delamination. Virtual prototyping is combined with interfacial strength measurements and show that from a

thermo-hygro-mechanical point of view interface delamination should not occur, unless its toughness is not secured by a proper material choice and/or assembly process. These real industrial applications demonstrate that with sufficient knowledge and proper execution, the added value of the virtual thermo-mechanical prototyping framework can be realized.

Willem van Driel, 2007

Samenvatting

De micro-elektronica, en de daarvan afgeleide eindproducten, heeft zich de afgelopen vijftig jaren een prominente positie in de huidige maatschappij veroverd. Micro-elektronische producten bevinden zich momenteel schijnbaar onzichtbaar om ons heen en nemen vitale functies waar, denk aan mobiele telefoons, televisies, geluidsapparatuur, veiligheidsinstallaties, maar ook in automobielen is een opgaande trend zichtbaar van het gebruik van elektronische producten. De micro-elektronische industrie wordt gedreven door twee factoren, te weten miniaturisatie en integratie. De zogenaamde wet van Moore is de drijvende factor achter het steeds kleiner worden van de lijnbreedte in een chip. Het integreren van verschillende chip technologieën in dezelfde verpakking noemt men tegenwoordig More than Moore. De combinatie van deze twee drijvende factoren brengt de micro-elektronica in een lastig parket: het wordt steeds moeilijker om te voldoen aan kwaliteitseisen, robuustheid, en betrouwbaarheid. In dit proefschrift is een structuur ontwikkeld waarmee de niet-lineaire responsie van micro-elektronische producten als gevolg van het thermo-mechanische krachtenspel a-priori kan worden voorspeld. Deze structuur is daarmee in staat om de betrouwbaarheid te voorspellen alvorens men overgaat tot het fysiek maken van het product.

De ontwikkelde structuur is opgebouwd uit twee fundamenten. Het eerste fundament betreft nauwkeurige en efficiënte optimalisatie methodieken bestaande uit Design of Experiments (DOE) en Response Surface Models (RSM). De zogenaamde Latin Hypercube DOE methode is gecombineerd met kwadratische en/of Kriging gebaseerde reponse surface benaderingen voor het uit voeren van de optimalisaties. Tevens is er een sequentiële techniek ontwikkeld, genaamd Efficient Global Optimisation (EGO), waarbij de keuze van de DOE rekenpunten is geïntegreerd met de nauwkeurigheid van het uiteindelijke response surface. Deze aanpak leidt tot een aanzienlijke reductie van de totaal benodigde rekentijd om tot een geoptimaliseerd product te komen. Het tweede fundament van de ontwikkelde structuur bestaat uit nauwkeurige en efficiënte thermo-mechanische voorspellingsmodellen die in staat zijn de niet-lineaire responsie van micro-elektronische producten te beschrijven. Zo'n voorspellingsmodel dient te voldoen aan verschillende voorwaarden. Ten eerste is het noodzakelijk dat de spanningsituatie in de chip lagen als gevolg van het maakproces

op voorhand wordt meegenomen. Zo ook dient men het tijd, temperatuur, en vocht afhankelijke gedrag van de verschillende materialen in het product, en hun onderling hechtbaarheid, op voorhand mee te nemen. Tevens is het noodzakelijk om belasting gedurende het totale maakproces in termen van temperatuursverandering(en), uitwendige mechanische krachten en het verloop van vocht dat het product in kan sijpelen in het voorspellingsmodel te beschouwen.

Het unieke van de ontwikkelde structuur is gebaseerd, voor de eerste keer, op de volgende drie aspecten:

- De ontwikkeling van geavanceerde optimalisatie methodieken.
- De ontwikkeling van nauwkeurige en efficiënte voorspellingsmodellen om het faalgedrag van micro-elektronische producten gedurende het maakproces en betrouwbaarheidstesten te beschrijven.
- Het integreren van de optimalisatie technieken en de voorspellingsmodellen.

De ontwikkelde voorspellingsstructuur is toegepast op een viertal industriële onderwerpen waarin de betrouwbaarheid van micro-elektronische producten van belang is. De bestudeerde betrouwbaarheden betreffen mogelijke breuk van chips, passivatie scheuren en de daarmee gepaard gaande metaal moeheid van chip lijnen, gelijksoortigheid regels voor substraatgebaseerde verpakkingen en hechtingsproblematiek in zogenaamde exposed pad verpakkingen. De resultaten van deze vier toepassing komen overeen met experimenten en waarnemingen uit het veld waarmee de voorspelbaarheid van de structuur kan worden aangetoond.

De eerste toepassing betreft de geometrische optimalisatie van een micro-elektronisch product waarbij mogelijke breuk van chips wordt voorkomen. Het voorspelde dunnere metalen frame blijkt ook na de betrouwbaarheidstesten geen breuk te vertonen. Het dunnere frame betekent een significante kostreductie. De tweede toepassing betreft onderzoek naar de interactie tussen een chip en de uiteindelijke verpakking. Door gebruik te maken van de ontwikkelde voorspellingsmodellen zijn de huidige regels verbeterd zodat men dure chip ruimte kan besparen. De derde toepassing betreft het opzetten van gelijksoortigheid regels, waarmee men kan bepalen of resultaten van eerdere (en geslaagde) betrouwbaarheidstesten voor product A kunnen worden gebruikt voor de vrijgave van een bijna identiek product B. Een serie regels is opgesteld en geïmplementeerd in huidige vrijgave procedures binnen de industrie. De vierde en laatste toepassing

betreft het aanpakken van de hechtingsproblematiek, welke een substantieel onderdeel is van de micro-elektronische industrie. De ontwikkelde structuur is gecombineerd met hechtingsterkte metingen en de resultaten tonen aan dat de sterkte voornamelijk wordt bepaald door de keuze van de materialen en het bijbehorende maakproces. De in dit proefschrift ontwikkelde voorspellingstructuur is met succes toegepast op het begrijpen en verbeteren van een viertal industriële toepassingen.

Willem van Driel, 2007

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Curriculum Vitae

Willem van Driel was born on July 19th 1970 in Dordrecht, The Netherlands. From 1982 to 1988 he passed through secondary school (Ongedeeld VWO). The first two years at 'Scholengemeenschap Willem de Zwijger' in Papendrecht, Zuid-Holland, and the remaining 4 years at 'Lorentz Scholengemeenschap' in Arnhem, Gelderland. He graduated from Mechanical Engineering at the Technical University of Eindhoven, the Netherlands. He has a broad R&D experience covering several multidisciplinary application fields. He is currently a principal engineer at NXP Semiconductors and also holds an adjunct position in Delft University of Technology, the Netherlands. His scientific interests are microelectronics and microsystems technologies, virtual prototyping, virtual reliability qualification and designing for reliability of microelectronics and microsystems. He is a member of the organizing committee of the IEEE conference EuroSimE, a member of the technical committee of the ICEPT and IMPACT conferences and Guest Editor for the IEEE Transactions on Components and Packaging Technologies. He is author and co-author of more than 80 scientific publications, including journal and conference papers, book or book chapters and invited keynote lectures.