Crystallographic Orientation- and Location-controlled Si Single Grains on an Amorphous Substrate for Large Area Electronics

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Chapter 1

Introduction

This thesis is the summary of investigations on single-crystalline location-controlled silicon grains aiming at the fabrication of thin-film transistors (TFTs) on large-area substrates. Two-dimensional (2D) location control can be achieved using the recently developed μ-Czochralski (grain filter) method [1]. Certain aspects of this new technique – such as defect reduction and crystallographic orientation control – need to be improved; these issues are addressed in this thesis. Thus, this thesis describes new methods in defect reduction and crystallographic orientation control, and introduces an ultra-low temperature ($T < 100^{\circ}$C) process in the μ-Czochralski method. TFTs fabricated inside location-controlled grains can be used for the fabrication of system circuits and three-dimensional (3D) integration, not only on glass substrates but also on flexible plastic substrates.

The first part of this chapter is a general introduction that presents various types of TFTs. Their comparison leads to the conclusion that single-grain TFTs (SG-TFTs) as active devices are essential for high-performance circuits. This discussion is followed by an overview of the μ-Czochralski process, a method used for the fabrication of single-crystalline location-controlled grains. The required improvements in single-crystalline silicon grains are discussed, and finally the chapter structure of the thesis is given.

1.1 TFT Characteristics

Conventionally, the term TFT refers to TFT-addressed liquid-crystal displays (LCDs), in which TFTs are used as switching devices turning individual pixels on and off [2]. However, TFTs can be used for the fabrication of peripheral drive circuits (e.g., decoders, drivers) or system circuits (memories, CPUs), opening the way to system-on-glass (SOG) integration [3] even on flexible plastic substrates [4]. Furthermore, three-dimensional integration can be achieved with stacked layers of TFTs, which increases the device density and functionality significantly [5].

However, for systems on glass and 3D ICs the electron field-effect mobility of the TFT needs to be of order 500 $cm^2/V{\cdot}sec$, as shown in Table 1.1. To fabricate high-

Table 1.1: The characteristics of TFTs

	α-Si TFT	poly-Si TFT	SG-TFT
Field-effect mobility [cm^2/V·sec]	0.1–1	50–300	500–600
Off-current [pA]	< 1	~ 0.1	~ 0.1
Type of TFT	NMOS	P-/N-MOS	P-/N-MOS
Uniformity	Good	Poor	Good

performance TFTs the active material for the TFT channels has to be crystalline Si on an insulator (SOI) or glass substrate.

Ideally, the silicon layer should be free of defects. It is almost impossible to prepare a macroscopic defect-free silicon layer on glass, however micrometer-sized (µm) silicon islands at predetermined positions may be produced with the µ-Czochralski process. TFTs fabricated inside location-controlled grains with this technology show a high performance, with an electron field-effect mobility of about 600 cm^2/V·sec [6].

1.1.1 α-Si TFTs

Hydrogenated amorphous silicon (α-Si:H) was one of the first active materials used for fabricating TFTs that meet the requirement of low process temperature for glass substrates [7]. α-Si:H has a crystal-like behavior because hydrogenation efficiently passivates the mid-gap states associated with dangling bonds in the silicon random network.

Using α-Si TFTs is a well-established approach for glass substrates nowadays. Due to the amorphous state of the active layer, off-state leakage currents in the sub-picoampere range and on-currents in the microampere range are typical for α-Si TFTs, therefore the requirement that TFTs in LCD pixels should have on/off current ratios greater than 10^6 is comfortably met [8].

Unfortunately, the threshold voltage of α-Si TFTs drifts rapidly during operation [9, 10]. Although the threshold-voltage shift can be compensated for by overdriving the gate at the expense of power dissipation, the shift makes it harder to implement peripheral analog circuits on glass [11]. The requirement for sufficiently high on-current – typically greater than 10^{-6} A – can be met by a large channel width to channel length (W/L) ratio, which implies a lower aperture ratio, and hence lower display resolution and brightness. Typical mobilities in the α-Si active layer are below 1 cm^2/V·sec (Table 1.1). This is one of the motivations for using polycrystalline silicon (poly-Si) as active material for TFTs (poly-Si TFTs), which also permits smaller transistor widths. Furthermore, the parasitic capacitance of the TFT can be reduced by a higher carrier mobility owing to the smaller transistor width.

1.1.2 Poly-Si TFTs

Poly-Si TFTs are fabricated with polycrystalline silicon (poly-Si) as active material for the channel. Poly-Si is a heterogeneous material made up of crystallites that are separated by grain boundaries. The primary motivation for the development of poly-Si TFTs is the double objective of higher integrated functionality on display panels and lower power consumption with high resolution.

One of the advantages of poly-Si TFT is the improved field-effect mobility – 50 to 150 $cm^2/V{\cdot}sec$ – compared to α-Si TFTs [12]. For the same on-current, the size of the poly-Si TFT is much smaller than that of the α-Si TFT, which allows a larger aperture ratio and higher display resolution [13]. Another advantage is that peripheral driver circuits can be made of poly-Si TFTs owing to its high mobility and the possibility of fabricating both n- and p-type TFTs [12, chapter 8]. Poly-Si TFTs are not subject to threshold-voltage shifts under electrical stress, therefore they show good stability over time, allowing the integration of peripheral circuits [12, chapter 11]. Mobility limits the range of applications for poly-Si TFT circuits to driver circuits: they cannot be used in system circuits.

However, the spatial uniformity of poly-Si TFTs is poor because of the random positions of grain boundaries. Atoms in the grain boundaries are either highly disordered, or the order of the lattice is discontinuous, therefore the density of defects is large [14]. This leads to the formation of trapping states, which influence carrier conduction. A free carrier (hole or electron) is immobilized by the trap, and creates a potential barrier that carriers have to overcome, hence it impedes the motion of the carrier [15, 16].

To improve mobility of poly-Si TFTs, lateral recrystallization of the silicon layer [17, 18] is currently used to produce large grains, stretching from the source to the drain of the TFT, thereby minimizing the probability of grain boundaries intersecting the current path. Various crystallization techniques have been proposed, including metal-induced lateral crystallization (MILC) [19, 20], sequential lateral solidification (SLS) [21, 22], selectively enlarging laser crystallization (SELAX) [23], comb-shaped beam in zone-melting recrystallization (ZMR)-excimer laser annealing (ELA) [24].

Although mobility is increased to 350 $cm^2/V{\cdot}sec$, uniformity could not be improved; it may become even worse. This is because the direction of and spacing between grain boundaries cannot be controlled, resulting in the variation of the number and direction of grain boundaries in the TFT channel.

To improve the uniformity of TFTs, the grain boundaries should be spatially controlled, leading to location-controlled grains [25–29]. Location control of the grain boundaries in poly-Si should improve performance and enhance uniformity in TFTs on account of the reduced number of random grain boundaries in the active channel [30,31]. In particular, if the grain is sufficiently large to build the entire TFT inside it (i.e., if there are no random grain boundaries in the channel) then a single-crystalline Si TFT (SG-TFT) is obtained. The performance of such devices is very close to that of SOI-FETs [32, 33].

1.1.3 SG-TFTs

SG-TFTs built in 2D location-controlled single-crystalline grains are prospective candidates for building blocks of future flat-panel displays, which can integrate system circuits in addition to driver circuits [30, 34].

The μ-Czochralski process is a promising technique to obtain location-controlled single-crystalline grains [1,35]. Another possibility is the location control of superlateral grain growth with microlight beam seeding [36]. Using a precision excimer-laser optical system, a seed can be formed with microbeam irradiation at a relatively low energy. Then the film, with a seed inside, is re-melted using uniform irradiation at a relatively high energy density. As a result, two-dimensional location-controlled grains can be produced. However, the yield and uniformity are much worse than for the μ-Czochralski process.

SG-TFTs fabricated with the μ-Czochralski process show superior performance: an electron field-effect mobility of 600 cm^2/V·sec, an off-current of 1.3×10^{-13} A, and a subthreshold swing of 0.21 V/dec. [33]. This high performance will allow developers to integrate peripheral driver circuits as well as system circuits with display, i.e., producing systems on panel (SOP).

The high performance of SG-TFTs permits the monolithic integration of analogue and digital driver circuits as well as other peripheral functions on an active matrix substrate. The resultant LCD modules have improved display functionality, performance and reliability. The next step in the development of this technology will be the integration of peripheral driver circuits and system circuits on a single substrate, leading to ultra-compact "system-on-panel" products.

This thesis focuses mainly on single-crystalline silicon grains used for SG-TFT fabrication. In the next section the method of fabricating single grains is discussed in detail.

1.2 Excimer-Laser Crystallization and the μ-Czochralski Process

1.2.1 Excimer-Laser Crystallization

Excimer-laser crystallization was first used for TFT fabrication in 1996 [37, chapter 1]. Compared to other crystallization methods, such as solid-phase crystallization, the intragrain defect density is lower and TFTs fabricated in such poly-Si grains have a much higher carrier mobility ($\sim$ 50–150 cm^2/V·sec) [38].

Excimer laser is a high-power ultraviolet (UV) light source. α-Si has such a high absorption rate ($\alpha =\sim 1.51 \times 10^6$ cm^{-1}) at this short wavelength ($\lambda = 308$ nm) that the absorption depth (or skin depth, $\delta = 1/\alpha \approx 6.6$ nm) of the α-Si film is only a few nanometers [39]. Hence, light power is absorbed only in the surface. The remaining α-Si film is heated up to the melting point, and the melt front advances vertically with laser irradiation.

During crystallization, α-Si undergoes two phase transformations:

Explosive crystallization: The melting point of α-Si, estimated to be 1420 K [40], is 200-300 K lower than that of crystalline silicon [41]. The rapid melting of α-Si results in a deeply supercooled liquid with respect to the melting point of crystalline silicon (~ 1685 K). Therefore the liquid immediately solidifies in fine poly-Si grains. Latent heat released during solidification moves the melt front deeper into the remaining α-Si layer. Therefore, there is a thin "underlying liquid layer" between the fine poly-Si grains and the remaining α-Si layer [42]. This procedure is called *explosive crystallization*. Since the released solidification enthalpy is higher than the melting enthalpy of α-Si, explosive crystallization is an energy self-sustaining transformation, which propagates through the α-Si layer and changes it into fine-grained poly-Si. The process continues until it is quenched by the energy required to raise the α-Si to its melting point. This picture of a propagating liquid layer was confirmed by transient reflectance and conductance measurements [42].

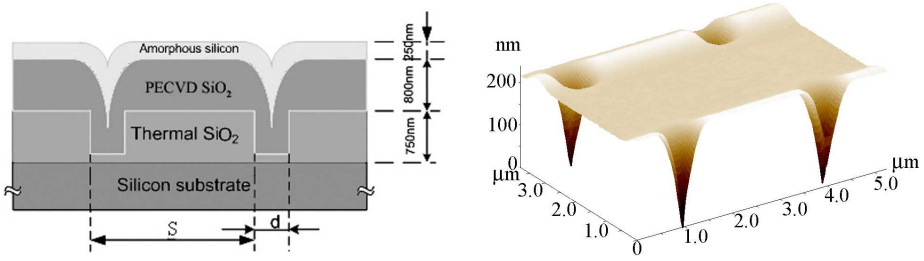
Melting and solidification: Above a threshold laser energy density the explosively crystallized polycrystalline silicon remelts. Molten Si is not so severely supercooled in this secondary step as in the primary one, so melting and solidification are much slower than explosive crystallization during explosive crystallization. The melt front propagates through the fine-grained poly-Si film with increasing laser energy density. If the laser energy is not high enough to melt the layer completely, then after laser irradiation has terminated solidification starts with heterogenous nucleation in the unmolten poly-Si, resulting in fine poly-Si grains. Otherwise, if the energy is high enough to melt the film completely, solidification starts from homogenous nucleation. Because of the absence of seeds in this case, solidification requires severe supercooling ($\sim$500 K) to overcome the critical energy barrier to form stable nuclei [43]. However, once solidification has started, nucleation and solidification rates are very high because of the severe supercooling [44]. With high nucleation and solidification rates, a film of fine pole-Si grains is obtained.

At a certain energy only few explosively crystallized fine grains survive secondary melting. This regime is called near-complete melting. At this laser energy density the grain size increases dramatically, and starts to exceed the film thickness. This phenomenon has been called superlateral growth (SLG) [45, 46]. Solidification starts with heterogenous nucleation from the few surviving seeds, and hence suppresses homogenous nucleation. The grain can therefore grow beyond the thickness of the layer.

SLG has a narrow energy density window [25], and the grain size is limited to a few hundred nanometers [47]. In order to enlarge the grain and widen the energy density window, various techniques have been introduced, including patterned capping layer [25, 48], phase-modulated excimer-laser annealing (PMELA) [48, 49], and dual-beam with oxide portion (DBTOP) [30, 31].

1.2.2 The μ-Czochralski (Grain Filter) Process

In this method grain filters are introduced to obtain large location-controlled grains [1, 35]. The location of grains can then be controlled in two dimensions, and there is a



(a) (b)

Figure 1.1: The structure of the grain filter. (a) Parameters of the grain filer: d is the diameter of the hole in the thermal SiO_2 layer, and S is the spacing of grain filters. (b) The cavity matrix of grain filters with a hole diameter of 1.0 μm before α-Si deposition.

wide energy density window up to the limit of agglomeration (see Appendix A). By controlling the location of grain boundaries, TFTs can be fabricated without random grain boundaries in the active channel. The obtained SG-TFTs are of high performance, almost as high as MOS field-effect transistors (MOSFETs) built on silicon-on-insulator (SOI) wafers.

Figure 1.1(a) shows the parameters and detailed structure of the grain filter, which is formed in two steps. First an approximately 750 nm thick oxide layer is grown by thermal oxidation of a silicon wafer, and it is subsequently patterned into grids of holes by reactive ion etching (RIE) in a CHF_3-C_2F_6 plasma. The diameters of the holes are $d = 0.8$, 1.0, 1.2, and 1.4 μm, while the grid spacing (S) varies from 3 to 15 μm. Next, an approximately 800 nm thick oxide layer is deposited by plasma-enhanced chemical vapor deposition (PECVD) using a tetraethylorthosilicate (TEOS) precursor to reduce the diameter of the holes to about 100 nm. Figure 1.1(b) shows the grids of the grain filter, measured by atomic force microscopy (AFM).

During excimer-laser irradiation, explosive crystallization occurs first, and propagates from the surface into the grain filter, producing fine poly-Si grains in the deep cavity. Then the secondary melt front advances from the surface into the grain filter. As the cavity is deep, some fine poly-Si grains (obtained in the explosive-crystallization phase) survive. These become the seeds during the solidification phase: they activate heterogeneous nucleation (or epitaxial growth) and initiate the vertical growth phase. In fact, the number of unmolten seeds and the amount of the successive vertical growth depends on the diameter, depth, and rim curvature of the grain filter. If the hole is sufficiently narrow and deep (Fig. 1.2), one single grain will be "selected" during the growth from the hole by the long vertical growth path – that is, other grains are occluded owing to the narrow growth passage. When the hole is wide or shallow, occlusion (the obstruction of the growth of poly-Si seeds) is less pronounced, and more than one grain survives after the selection by the hole. That explains why this cavity structure is called a grain filter.

The vertical growth phase is followed by lateral growth, starting from the surviving

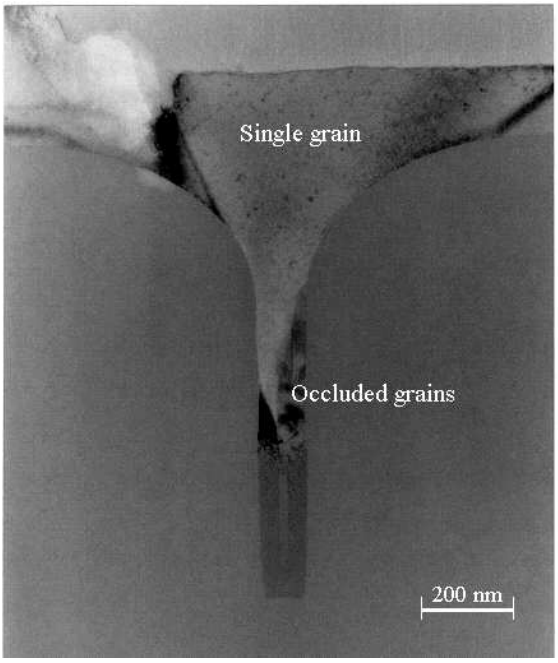


Figure 1.2: Cross-section transmission electron microscopic (TEM) image of the grain filter of diameter $d = 1.0$ μm, at an energy density of 1250 mJ/cm^2.

seeds in the grain filter. Lateral growth along the interface can last until the liquid in front of the solidification front reaches the critical supercooling temperature of heterogeneous nucleation.

The location of the grains can be controlled by the grain filters beneath. Because of the artificially selected seeds, there is a wide energy density window to prepare such grains.

Figure 1.3 shows the grain size as a function of the energy density of the laser pulse (E_l) for each diameter (d) of the grain filter. For the 1.0 μm grain filter, the grain size increases with the laser energy density. The maximum grain size, 7 μm, is obtained at 1300 mJ/cm^2. Above 1300 mJ/cm^2 the grain size even decreases, and at 1400 mJ/cm^2 complete melting occurs. Large two-dimensional location-controlled grains can be obtained with laser energy densities between 900 and 1400 mJ/cm^2.

The larger the diameter of the grain filter, the smaller the obtained grain. However, it is never smaller than 1.0 μm: grain growth does not occur from a 0.8 μm grain filter because it is either closed or the whole layer is completely molten (due to the shallow holes). For 1.2 and 1.4 μm grain filters the grain size is smaller than for 1.0 μm grain filters. The smaller the diameter of the grain filter, the fewer seeds survive secondary melting inside the cavity. If the number of unmolten solid grains (seeds) in the grain filter

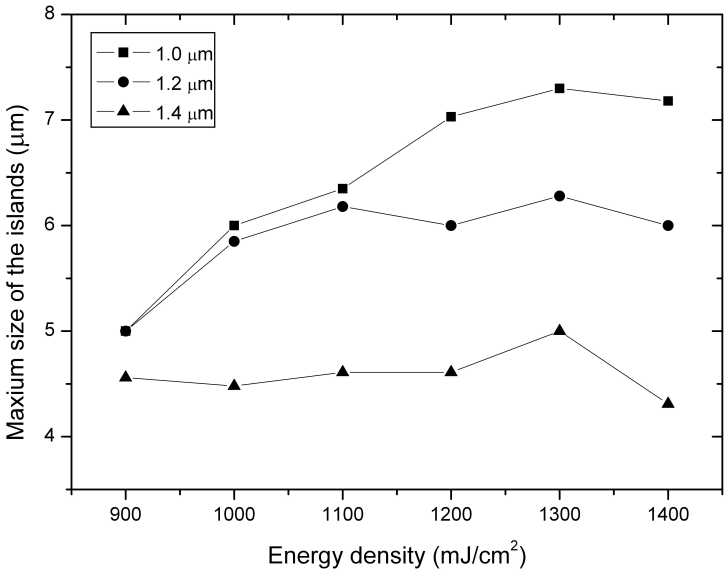


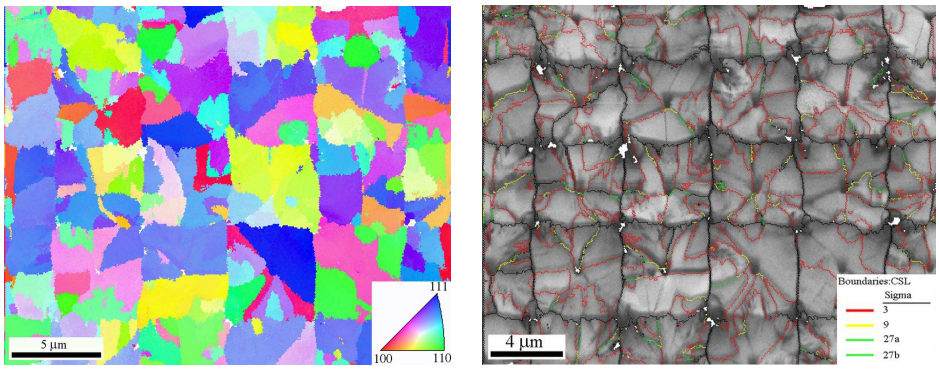
Figure 1.3: The maximum island size as a function of the laser energy density for different diameters d of the grain filter.

is large, they halt vertical and subsequent lateral growth, giving rise to small islands.

Figure 1.4 shows the inverse-pole-figure (or crystallographic direction) map and the grain-boundary-component map of the location-controlled grains, analyzed by electron backscatter diffraction (EBSD). The inverse-pole-figure map [Fig.1.4(a)] shows the surface orientation of the location-controlled grains. The inset in Fig. 1.4(a) is the color key for the orientation indices. Red, green, and blue are for grains with (001), (110), and (111) orientation aligned with the normal direction of the sample surface, respectively. Fig.1.4(a) indicates that there is no preferred orientation in the location-controlled grains, i.e., the crystallographic orientation of the grains is random.

The grain-boundary-component map [Fig. 1.4(b)] shows the subgrain boundaries inside a grain, based on the coincidence-site-lattice (CSL) model [50] and calculated from the misorientation between neighboring grains. Figure 1.4(b) shows that subgrain boundaries inside the island are mainly CSL types: most frequently $\Sigma 3$, followed by $\Sigma 9$ and $\Sigma 27$. Most CSL-type subgrain boundaries are microtwins; this is also confirmed by top-view TEM analysis [51, 52].

SG-TFTs fabricated in the location-controlled grains discussed above feature high performance [6, 53], with an average electron field-effect mobility of 600 $cm^2/V{\cdot}sec$. This is still lower than in single-crystalline silicon (700 $cm^2/V{\cdot}sec$). The lower value is due to defects inside the channels [32, 33]. The performance and uniformity can be improved further by controlling the crystallographic orientation of the grain and the reduction of planar defects. These are the main issues addressed in the present thesis.



(a) (b)

Figure 1.4: EBSD maps of location-controlled grains. (a) Inverse-pole-figure (IPF) map; the inset shows the orientation color key (the color gives an indication of the crystallographic direction aligned with the surface normal). (b) Grain-boundary-component map overlaid with image-quality (IQ) map; the inset gives the indices for the various types of grain boundaries in a coincident-site-lattice (CSL) model. Location-controlled grains are grown from 1.0 μm grain filters at an energy density of 1200 mJ/cm^2.

An important factor that affects the performance of SG-TFTs is the crystallographic orientation of the single-crystalline grains, on account of the anisotropy of mobility. Theoretically as well as experimentally, the dependence of the mobility of n- and p-type MOSFETs on the crystallographic orientation of the channel has been intensely investigated [54, 55]. So far, the single-crystalline grains have random crystallographic orientations with CSL boundaries (defects), leading to a poor uniformity (17% variations [33]) of the device performance. If the crystallographic orientation of the channel can be controlled and CSL boundaries (defects) can be removed in SG-TFTs, then their performance is expected to be improved further, therefore SG Si TFTs with the above features are ideal candidates for the fabrication of high-quality circuits.

Location-controlled grains are used for SG-TFTs on glass substrates with a process temperature below $450°$C [56]. The direct integration of circuits on large-area flexible plastic substrates has attracted a lot of attention recently. To fabricate circuits with location-controlled grains on plastic substrates it is essential to develop an ultra-low temperature process to prepare location-controlled grains. By implementing μ-Czochralski process in the ultra-low temperature range ($T < 100°$C), the scope of applications for SG-TFTs can be extended to smart e-papers, flexible displays, etc.

1.3 The Goal of this Thesis

As discussed in Section 1.2,various improvements are required for location-controlled grains to be suitable for the integration of system circuits. In this respect, the goals of the present research are:

1. ***Defect reduction:*** The main defects are CSL grain boundaries [Fig. 1.4(b)]. These grain boundaries in the TFT channels create potential barriers, impeding carrier mobility. In order to improve the performance of SG-TFTs, defects inside grains must be reduced.

2. ***Crystallographic orientation control:*** To improve the performance and uniformity of SG-TFTs, it would be ideal to have the crystallographic orientation of the single grain controlled in some preferred direction. By combining the μ-Czochralski process with crystallographic orientation control, orientation- and location-controlled grains can be prepared for the fabrication of SG-TFTs circuits.

3. ***Ultra-low temperature process for plastic microelectronics:*** The fabrication of low-temperature poly-silicon (LTPS)TFTs on plastic substrates has received a lot of attention recently because of its possible applications in flexible display technology and electronics. For the purposes of this thesis an ultra-low temperature ($T < 100°\mathrm{C}$) process has been developed for the application of SG-TFTs on flexible plastic substrates. Using this method SG-TFTs can be fabricated for microelectronics on plastic substrates.

1.4 Chapter Structure and Overview

This thesis addresses the problem of realizing crystallographic orientation- and location-controlled single-crystalline grains with defect reduction, with the aim of fabricating high-performance SG-TFTs inside them. The thesis is organized as follows:

Chapter 2, Fabrication, Characterization, and Heat-Transfer Simulations describes the fabrication process, materials analysis, device characteristics, and heat-transfer simulations used throughout the thesis. General concepts of materials and methods used during the thesis research are discussed.

Chapter 3, Defect Reduction investigates the methods of defect reduction. First a capping layer is introduced on top of the grain filter; this is found to be insufficient to reduce the defects. Next, a seeding layer is introduced at the bottom of the grain filter; this is found to reduce the number of defects significantly. (100)-oriented seeds are observed to be more efficient than non-(110)-oriented ones.

Chapter 4, $\langle 100 \rangle$-Oriented Seeding Layer describes the preparation of a $\langle 100 \rangle$-oriented seeding layer on top of an amorphous insulating SiO_2 layer. By multiple-shot excimer-laser crystallization, $\langle 100 \rangle$ orientation preference is observed in self-

assembled square-shaped poly-Si grains. Multiple-shot excimer-laser crystallization and the resulting laser-induced periodic surface structures (LIPSS) are discussed in detail. The mechanism of surface-orientation control is also presented.

Chapter 5, Crystallographic Orientation- and Location-Controlled Grains deals with the method to prepare crystallographic orientation- and location-controlled grains. Combined with the methods employed in Chapter 3, the $\langle 100 \rangle$-oriented poly-Si layer (described in Chapter 4) is now used as a seeding layer, to prepare crystallographic orientation- and location-controlled single silicon grains for SG-TFT fabrication.

Chapter 6, Ultra-Low Temperature Process introduces a promising method for applying location-controlled grains for integrated circuits on plastic substrates. By combining low-temperature sputtering and excimer-laser crystallization, location-controlled grains can be obtained at a process temperature of $100°$C. With an ultra-low-temperature SiO_2 ($T < 80°$C) obtained using inductively coupled plasma-enhanced chemical vapor deposition (ICPECVD), SG-TFTs can be fabricated at a process temperature of $100°$C.

Chapter 7, Conclusions and Recommendations concludes the thesis with a summary and discussion of the presented research topics, along with some suggestions for future research.

Appendix A, Effects of a Capping Layer describes additional effects of a capping layer on the μ-Czochralski process. Originally, the capping layer is introduced in the μ-Czochralski process in an attempt to reduce the number of defects inside grains. Experiments show that while it is ineffective in this respect, a sufficiently thin capping layer can enlarge the grain.

Chapter 2

Fabrication, Characterization, and Heat-Transfer Simulations

Based on the μ-Czochralski process, the problems of crystal-quality improvement, defect reduction, and orientation control are addressed in this thesis. Fabrication means are discussed in Section 2.1. The next section is a general treatment of the methods for crystal-quality analysis and device characterization. Finally, a description of the simulation of heat transfer during excimer-laser crystallization using finite-element methods is given.

2.1 Fabrication

All experimental procedures are performed in the cleanroom facilities of the Delft Institute of Microelectronics and Submicrotechnology (DIMES), at the Delft University of Technology.

2.1.1 Laser Systems

A large proportion of the investigations for this thesis are related to excimer-laser crystallization. In general, two laser systems were used: an XMR 7100 system – an old system that is not easy to operate because of the outdated computer control system –, and a new Exitech M8000V – which was installed at the DIMES facility in 2006.

The XMR 7100 System

The XMR 7100 system uses a mixture of Xe and Cl_2 as active gas, and Ne as buffer gas. When "excited dimer" (excimer) XeCl returns to the ground state, a pulse of ultraviolet (UV) light (wavelength: $\lambda = 308$ nm; full width at half maximum (FWHM): 50 ns) is emitted.

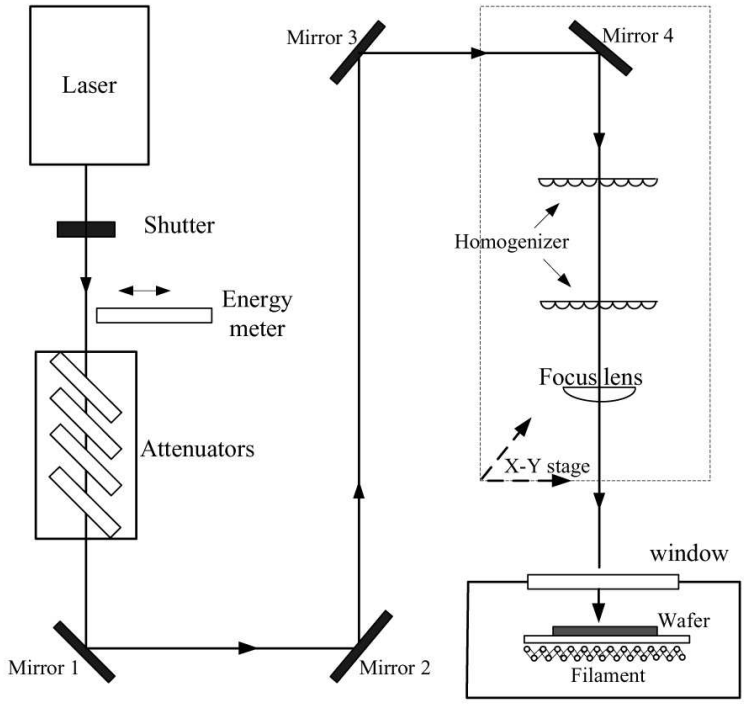


Figure 2.1: Schematic representation of the XMR 7100 system. The energy meter can be moved into the laser path to measure the energy density of the laser output. The energy density at the wafer surface is tuned by the laser spot size. The dotted rectangle indicates an X-Y stage, onto which mirror 4, the homogenizer, and the focus lens are mounted. During laser processing, the X-Y stage moves, whereas the wafer stays stationary.

Two pairs of crossed cylinder lens arrays with an output cylindrical condenser lens form a beam homogenizer. The first array splits the beam into separate parts, and each part is focused before passing through the corresponding lensin the secondary array. The output (condenser) lens deviates the diverging output beams so that they overlap at the wafer surface, leading to a rectangular beam profile with high spatial uniformity.

The energy density of the laser pulse can be tailored by tuning the final laser spot on the wafer. Adjustment of the laser spot size is achieved by changing the position of the upper lenses of the homogenizer. Typical spot sizes range from 0.3×0.5 cm^2 to 2×2 cm^2.

During laser processing, the wafer remains stationary on the chuck. The optics (homogenizer and focusing lens) are mounted on an X-Y stage, which moves in the X- and Y-directions to ensure scanning of each die on the wafer. Wafers are held under high vacuum ($\sim 1.33 \times 10^{-5}$ Pa), and can be heated up to 500°C by a tungsten filament.

Quartz beam splitters are used as attenuators in the light path to modify the energy before entering the homogenizer. The attenuator can also partially polarize the laser light; this issue will be discussed in Chapter 4.

The Exitech M8000V System

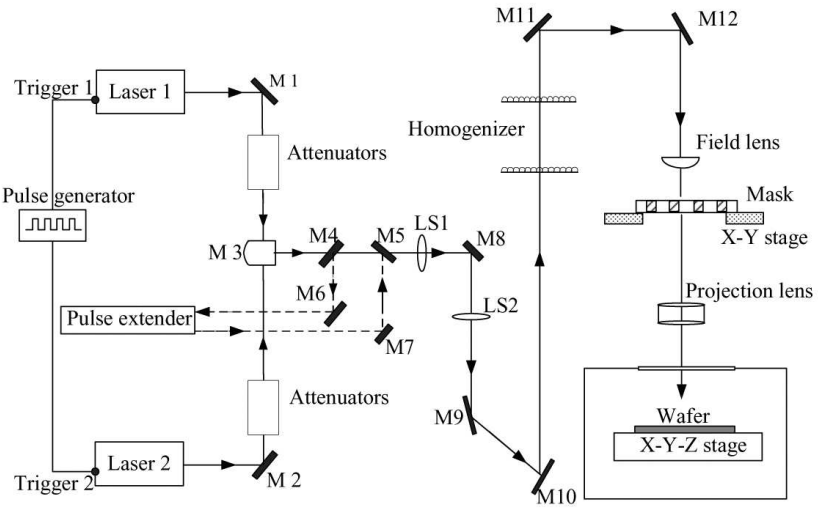


Figure 2.2: Schematic representation of the Exitech M8000V laser system. The removable mirrors M4 and M5 are used to direct the pair of beams into and out of the pulse-duration extender when required.

The schematic representation of the Exitech M8000V laser system is shown in Fig. 2.2. The system uses the same gases as the XMR 7100 laser system, and thus the same UV light (wavelength: 308 nm) is emitted.

The M8000V has two Lambda Physik LPX 210 laser sources. Their output beams travel through the optical chain, as indicated in Fig. 2.2, and mirror 3 (M3) combines them. Lenses LS1 and LS2 guide the combined beam from the exit of the laser sources to the entrance aperture of the beam homogenizer. The laser light leaving the homogenizer has a top-hat profile at the mask, and shows high spatial uniformity ($\sim 2.5\%$ variations in the X- and Y- directions).

The field lens located just before the mask guides the two beams toward the entrance pupil of the projection lens. The projection lens then produces an image of the mask at the wafer level. The mask can be designed with the desired pattern. With a suitable choice of the pattern the energy density of the laser light at the wafer level can be rearranged at will. The mask itself is mounted on an X-Y stage, which allows its alignment with the light path.

The pulse duration of the Exitech M8000V system is about 23 ns, which is shorter than that of the XMR 7100 system. Long pulse durations can be realized with a proper delay between the two lasers or by using a pulse-duration extender. The beam is deflected into the pulse extender by the removable mirror M4, and the long-pulse beam is introduced again into the light path by mirror M5. The maximum pulse duration of the output can exceed 300 ns.

Compared to the XMR 7100 system, the Exitech M8000V has a better control over operation accuracy, such as wafer handling and laser energy density. The position of the wafer can be controlled with a precision in the μm range by an accurately adjustable X-Y-Z stage. The energy density of the laser on the wafer is checked with an energy meter at the wafer level. When the X-Y-Z stage is moved to a safe position, the energy meter moves in and measures the energy density at the position where the wafer would be. The energy density at the wafer level is automatically tuned by turning the beam splitters of the attenuators. The energy density is determined separately for each laser source, and thus the attenuator for each laser source is tuned. The final energy density on the wafer is the sum of the two tuned energy densities.

2.1.2 Film Deposition and Patterning

To prepare single-crystalline grains for SG-TFT fabrication, various methods are used for layer deposition and subsequent patterning. These are discussed in detail in the following chapters; below only a short summary is given.

All investigations described in the following chapters are performed on oxidized c-Si wafers as carrier substrate – however, all the processes are compatible with glass substrates as well, and they can even be extended to plastic substrates (Chapter 6).

Layers

The fabrication of high-performance TFT devices requires high-quality active layers, electronic conductive layers, and insulating layers.

1. Active layers For high-performance SG-TFTs, single-crystalline Si material is used for the active channel for electron or hole transconduction. Excimer-laser crystallization is a promising method to prepare high-quality active materials from α-Si precursor layers. For α-Si precursor two deposition methods are used in the experiments of this thesis work.

(1) *Low-pressure chemical vapor deposition (LPCVD)* The α-Si film is deposited in a conventional horizontal hot-wall LPCVD furnace using pure silane as source gas at a pressure of 20 Pa and a temperature of $547°$C.

(2) *Pulsed DC magnetron sputtering (physical vapor deposition, PVD)* By using pulsed DC magnetron sputtering, α-Si is deposited directly from a pure silicon target.

Compared to LPCVD, Si deposition by sputtering offers certain advantages:

(i) Sputtering can produce high-quality films in a wide process-temperature range, down to room temperature, which ensures compatibility with a rich variety of substrates, especially with plastic substrates.

(ii) Sputtering can be realized with a batch process, as well as with the emerging roll-to-roll process; the latter is highly cost-effective, and also essential for large-area microelectronics on plastic substrates.

(iii) Sputtering of Si can eliminate the toxic and hazardous process gases (for example, SiH_4 used in LPCVD) and allow to control the amount of hydrogen incorporated in the deposited film. Pulsed DC magnetron sputtering will be discussed in detail in Chapter 6.

2. Conductive layers Aluminum is a good conductor, therefore, it is used for electron or hole conduction from device to device, or from layer to layer. Sputtering is the primary method for Al film deposition in microelectronics fabrication. Aluminum with 1% of Si is used as gate material and secondary metal for SG-TFT fabrication. In our experiments Al films were deposited by pulsed DC magnetron sputtering (Sigma sputter coater).

3. Insulating layers To prevent short circuits and to ensure the separation of active devices, various types of insulating layers are required. Oxide is widely used as an insulator both in active devices and the region between them.

(1) Buffer layer In this context *buffer layer* refers to the layer between active devices (TFTs) or circuits and the carrier wafer; it is typically of thermal oxide. Thermal oxidation is performed in ambient H_2-O_2 at $1100°$C. The thermal oxide is a high-quality electronic insulating and buffer layer for thermal processing (excimer-laser crystallization) and doping diffusion.

This high-temperature oxidation cannot be used with glass substrates – but in this case the layer can be easily substituted by a low-temperature oxide or by a nitride layer. In this thesis, thermal oxide is used as buffer layer for ease of application at the DIMES facility.

(2) Gate oxide The gate oxide is deposited using the decomposition of tetraethylorthosilicate (TEOS) precursor at a temperature of 300 or $350°$C in a plasma-enhanced chemical-vapor deposition (PECVD) reactor (Novellus concept one).

The possibility of using inductively coupled plasma-enhanced CVD (ICPECVD) for low-temperature gate-oxide deposition is analyzed in Chapter 6. Compared to conventional PECVD, ICPECVD opens the way to preparing high-quality oxides at an ultra-low temperature ($T < 80°$C) with less plasma damage on the oxide.

(3) Passivation oxide The passivation oxide is obtained from the decomposition of TEOS or silane (SiH_4) and O_2 mixture in a PECVD reactor. This low-temperature oxide passivates active TFT devices and provides an insulation between conductive metals.

Most of the investigations described in this thesis focus on the preparation of active materials for SG-TFT fabrication – however other layers are discussed as well.

Patterning

For SG-TFT fabrication layers need to be patterned to define active channels, dopedregions and open windows for connection between layers. All the necessary patterns are predefined by lithography.

1. Lithography Lithography is performed using an I-line ASML PAS 5000/50 wafer stepper. The minimum line width is 0.6 μm. The pattern is defined by exposing photoresist layers with predefined patterns on masks. The desired pattern is first formed on a photoresist film, and then transferred to the layers beneath by further etching or doping (ion implantation).

2. Etching

(a) Fluorine etcher: Oxide is patterned in a Drytek 384T fluorine etcher, with CF_4, CHF_3, C_2F_6 gases.

(b) Chlorine etcher: Si and Al are patterned in an Omega Trikon 201 electron cyclotron resonance (ECR) etcher. Aluminum is etched with HBr and Cl_2 gases, while Si is etched with Cl_2, CF_4, and CHF_3 gases.

3. Doping and laser annealing Source and drain regions are heavily doped so that ohmic contacts are formed with the Al films. This is achieved with ion implantation and subsequent activation of doping by excimer-laser annealing. Ion implantation is done with a Varian E500 HP implanter using PH_3, AsH_3, and BH_3 as source gases. Doping is activated by excimer laser at an energy density of 300 mJ/cm^2.

2.1.3 SG-TFT Fabrication

All the aforementioned layers – active layers, conductive layers, and insulating layers – are used in SG-TFT fabrication. Single grains are prepared with the μ-Czochralski process, described in Section 1.2.2.

Single grains are patterned into islands with chlorine etcher. Then the gate oxide is deposited on top of the islands, and the gate metal is deposited and RIE-patterned into a gate. In the next step the gate oxide is patterned to remove the oxide outside the channel. Ion implantation is then carried out in a self-aligned manner with the metal gate as mask. At this point doping is activated with the excimer laser.

After doping, source and drain regions are formed, and a passivation oxide is deposited. Finally contact openings are etched in the second metal to provide connections to outside circuits.

More details about SG-TFT fabrication can be found elsewhere [57].

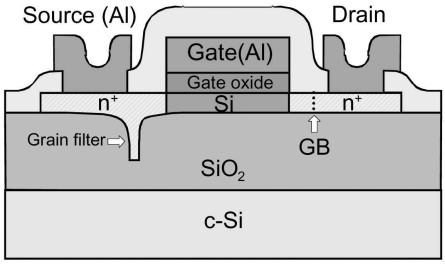


Figure 2.3: Schematic representation of the cross-sectional view of a SG-TFT inside a location-controlled grain, fabricated with the μ-Czochralski process. GB denotes the grain boundary. The channel region is free of grain boundaries.

2.2 Characterization

SG-TFT use single-crystalline silicon grains as active material for the channels. The microstructure of active channels is analyzed with SEM, EBSD, and TEM. SG-TFTs are characterized by electrical properties.

2.2.1 Material Characterization

SEM

After excimer-laser crystallization and Secco etching (a wet etching method to delineate planar defects), single grains resulting from the μ-Czochralski process are inspected with a scanning electron microscope (SEM). SEM produces high-resolution images of the morphology of the samples, allowing researchers to study the grain size of single grains and grain boundaries. We used two SEM systems in our investigations: an FEI XL 30 and an FEI XL 50 system.

EBSD

The microtexture of single grains and the nature of the grain boundaries are investigated using electron backscatter diffraction (EBSD). Since the early 1990s, EBSD has evolved to become a mature method for microtexture and microstructure analysis [58]. In this technique, backscattered electrons are detected and captured with a phosphor screen, producing an electron backscatter pattern (EBSP), which consists of Kikuchi bands from different crystal planes of the inspected spot. By indexing these Kikuchi bands, the three-dimensional crystallographic orientation is readily obtained.

EBSD analysis is carried out with an orientation imaging microscopy (OIM^{TM}) EBSD system, installed on the FEI XL 50 device. This system provides visual images of the microstructure of single-crystalline grains and the microtexture of films. In the EBSD

setup samples are tilted horizontally by 70°, and the accelerating voltage is 20 kV. EBSD mapping is performed with a step size of 100 nm.

The grain boundaries inside location-controlled grains are characterized using the coincidence-site-lattice (CSL) model [50]. The CSL concept describes misorientations between two neighboring grains – which means that by rotating the lattice of one grain around a specified axis, $\langle$UVW$\rangle$, through a specified angle (θ), *some* lattice sites (the "coincidence sites") of the second grain are repeated. These CSL boundaries are assigned a coincidence number (Σ) based on the reciprocal of the proportion of coincident lattice sites. Therefore low Σs indicate high coincidence. The identification of a grain boundary requires the specification of five independent parameters. When boundaries are classified according to their CSL type, two degrees of freedom that describe the interface plane (grain-boundary plane) remain unspecified.

The misorientation between the crystal lattices separated by grain boundaries and the existence of a particular relative crystallographic orientation between neighboring crystals are the criteria used to identify twin-grain boundaries [59] for CSL twins $\Sigma 3$, $60°@\langle 111\rangle$.

The microtexture (contour-pole figure or contour-inverse-pole figure) is calculated from a harmonic series expansion (series rank $L = 16$) of the discrete pole figures with a 5-degree Gaussian smooth. The texture component is denoted by $\{$ND$\}\langle$RD$\rangle$ [58]; the expression in curly brackets specifies the preferred crystallographic orientation for the normal direction (or surface normal), while that in the angle brackets gives the rolling direction in the sample reference.

TEM

SEM and EBSD provide information only about sample surfaces. A more detailed structural information is obtained by transmission electron microscopy (TEM).

Electron beams in TEM systems typically have energies between 100 keV and 1 MeV, which, according to the de Broglie relationship, correspond to wavelengths of less than 0.01 nm. Thus TEM provides high-resolution images. As electrons pass through the sample, elastic and inelastic scattering occur. These interactions disclose diverse information about the structure of the sample. For example, if the sample is crystalline, elastic interaction between electrons and lattice atoms give rise to Bragg diffraction, from which information about the orientation and structure of the sample can be extracted. If the sample has defects – such as dislocations, stacking faults, or grain boundaries – then the pattern of scattering between primary electrons and defects will be different from that in a perfect crystal.

Both top-view and cross-sectional samples are prepared. Electrons can penetrate through the sample only if its thickness is small.

Plane-view samples are prepared using normal ion milling methods. First the sample is mechanically thinned down to about 20 μm. Then it is glued to a 3 mm Cu grid, and the center part is treated by low-angle Ar ion milling to obtain an electron-transparent film. The ion mill used in our experiments is a dual-type Gatan device.

On account of their fine structure, cross-sectional samples are prepared using a focused ion beam (FIB). First a layer of Pt strips is deposited as protecting layer on the position of interest. Then the surrounding material is milled away by gallium ions at 30 kV, with a current of 5 nA in the beginning and 100 pA afterwards. Finally the obtained electron-transparent piece ($\sim 20 \times 10 \times 0.1$ µm^3) is transferred to a Cu grid.

In TEM studies a Philips CM30-T device is used with LaB_6 source operated at 300 kV. High resolution analysis is done using a Philips CM30-UT system, with the field-emission gun operated at 300 kV.

TEM patterns are analyzed at the Center for Electron Microscopy, Department of Applied Physics, at the Delft University of Technology.

2.2.2 Device Characterization

TFT characteristics are measured with an HP 4156A semiconductor parameter analyzer. Output characteristics (I_{DS} versus V_{DS}) and transfer characteristics (i.e., I_{DS} versus V_{GS}) are measured.

The drain current is written as

$$I_{\mathrm{DS}} = \begin{cases} \frac{\mu_{\mathrm{n}} W C_{\mathrm{ox}}}{L}[(V_{\mathrm{GS}} - V_{\mathrm{T}})V_{\mathrm{DS}} - \frac{1}{2}V_{\mathrm{DS}}^2], & V_{\mathrm{DS}} \leq V_{\mathrm{GS}}/V_{\mathrm{T}}, \\ \frac{\mu_{\mathrm{n}} W C_{\mathrm{ox}}}{2L}[V_{GS} - V_{\mathrm{T}}]^2, & V_{\mathrm{DS}} \geq V_{\mathrm{GS}}/V_{\mathrm{T}}, \end{cases} \tag{2.1}$$

where μ_{n}, C_{ox}, W, and L are the field-effect mobility, oxide capacitance, channel width, and channel length, respectively. The field-effect mobility, μ_{n}, is determined from the linear part of the I_{DS} vs. V_{DS} curve:

$$\mu_{\mathrm{n}} = \frac{\partial^2 I_{\mathrm{DS}}}{\partial V_{\mathrm{GS}} \partial V_{\mathrm{DS}}} \times \frac{L}{W C_{\mathrm{ox}}}. \tag{2.2}$$

The threshold voltage, V_{T} is defined as

$$V_{\mathrm{T}} = V_{\mathrm{FB}} + 2\psi_{\mathrm{F}} + \frac{\sqrt{4q\varepsilon_{\mathrm{Si}}\psi_{\mathrm{F}} N_{\mathrm{a}}}}{C_{\mathrm{ox}}}, \tag{2.3}$$

where V_{FB}, ψ_{F}, $\varepsilon_{\mathrm{Si}}$, and N_{a} are the flat-band voltage, the distance between the intrinsic level and the Fermi level, the dielectric constant of silicon, and the dopant density in the channel, respectively.

In the subthreshold regime the channel is in weak inversion, so the transconduction of carriers is controlled by the gate voltage. The subthreshold swing S is defined as the amount of gate voltage required to increase the drain current by one order of magnitude. Thus, S is the inverse of the slope of the $\ln I_{\mathrm{DS}}$ vs. V_{GS} curve:

$$S = \left[\frac{\partial \ln(I_{\mathrm{DS}})}{\partial V_{\mathrm{GS}}}\right]^{-1} = \frac{\partial V_{\mathrm{GS}}}{\partial \ln(I_{\mathrm{DS}})}. \tag{2.4}$$

The subthreshold swing S is an important parameter, a measure of the Si/SiO_2 interface trap density in MOSFETs. It can be shown that

$$S = \frac{kT}{q} \log_{10} \left(1 + \frac{C_{\text{depl}} + C_{\text{it}}}{C_{\text{ox}}} \right), \tag{2.5}$$

where k is Boltzmann's constant, T is the temperature,while C_{depl} and C_{it} are the capacitance of the depletion layer and of the interface states, connected in parallel. V_{T} and S can be determined from I_{DS} vs. V_{GS} curves.

2.3 Heat-Transfer Simulations

To evaluate heat transfer during excimer-laser crystallization, one-dimensional numerical simulations of transient heat transfer are performed using the finite-element method (FEM) based on the equations of heat conduction and solid/liquid phase transformation with the release or absorption of latent heat,

$$\rho c(T) \frac{\partial T}{\partial t} = \frac{\partial [K(T)(\partial T/\partial x)]}{\partial x} + S_{\text{L}}(x,t) + S_{\text{LH}}(x,t), \tag{2.6}$$

where ρ is the mass density, $c(T)$ is the specific heat capacity, $K(T)$ is the heat conductivity, and x and t are the space and time coordinates. To simplify simulations, the thermal radiation from α-Si to the vacuum chamber is ignored.

The heat from the laser pulse is given by

$$S_{\text{L}}(x,t) = \begin{cases} (1-R)AE_{\text{l}} \exp(-\alpha x), & 0 \le t \le 50\text{ns}, \\ 0, & t > 50\text{ns}, \end{cases} \tag{2.7}$$

where R is the reflectivity of the α-Si surface, A is the laser spot size, E_{l} is the energy density of the laser pulse,and α is the absorption coefficient of the α-Si film. $S_{\text{LH}}(x,t)$ is the latent heat released or absorbed in the phase transformation at the solid/liquid interface.

The physical properties used in this simulation are tabulated in Table 2.1. The temperature-dependent material properties [$c(T)$ and $K(T)$] are obtained from the literature [listed in Table 2.1]. The initial and ambient temperatures are assumed to be 450°C.

Heat-transfer simulations are carried out for epitaxial growth from seeding layers described in Chapters 3 and 5, while the effects of a capping layer are discussed in Appendix A.

Table 2.1: Physical parameters used in the numerical simulation

Mass density, ρ [g/cm^3]	
SiO_2	2.2
α-Si/l-Si	2.2
c-Si	2.33
Thermal conductivity, $K(T)$ [W/(cm·K)]	
SiO_2 [60]	$\begin{cases} 1.005 \times 10^{-3} + 1.3 \times 10^{-6} T, & T \leq 1170[\mathrm{K}], \\ 2.51 \times 10^{-2}, & T > 1170[\mathrm{K}]. \end{cases}$
α-Si [61]	$1.3 \times 10^{-11}(T-900)^3 + 1.3 \times 10^{-9}(T-900)^2 + 10^{-6}(T-900) + 10^{-2}$
c-Si [60]	$\begin{cases} 1523.9952\, T^{-1.22}, & T < 1200[\mathrm{K}], \\ 9.00162\, T^{-0.502}, & T \geq 1200[\mathrm{K}]. \end{cases}$
l-Si [60]	$0.502 + 2.99 \times 10^{-4}(T - 1687)$
Specific heat capacity, $c(T)$ [J/g·K]	
SiO_2 [60]	$0.708 + 2.99 \times 10^{-4} T$
c-Si [60]	$0.81 + 1.3 \times 10^{-4} T - 1.26 \times 10^4 T^{-2}$
α-Si [60]	$c_{\text{c-Si}} - 0.00799 + 1.016 \times 10^{-4} T$
l-Si [62]	$0.9098 - 2.274 \times 10^{-4} \times (T - 1687) + 4.871 \times 10^{-7}(T-1687)^2 - 7.208 \times 10^{-10}(T-1687)^3 + 9.950 \times 10^{-12}(T-1687)^4$
Reflectivity, R	
α-Si	0.7
Absorption coefficient, α [cm^{-1}]	
α-Si [60]	1.5×10^6
Melting point [62], [K]	
c-Si	1687
Latent heat (solid/liquid), [J/kg]	
Si	1.789×10^6

Chapter 3

Defect Reduction in Location-Controlled Grains

This chapter deals with the efforts to reduce defects inside single-crystalline location-controlled grains fabricated with the μ-Czochralski process. Defects are primarily CSL grain boundaries, some of which are electronic potential barriers for carriers (electrons or holes) conduction.

Two approaches are tested. In the first, a capping layer is introduced in the μ-Czochralski process; experiments show no significant reduction in the number of defects. In the second a seed produced with selective epitaxial growth from wafer substrates is introduced in the μ-Czochralski process; the number of CSL grain boundaries inside location-controlled grains is observed to be reduced significantly. This latter approach is discussed in detail in Section 3.2.

3.1 Effects of a Capping Layer

3.1.1 Introduction

Applying a SiO_2 capping layer on top of α-Si is an effective method for enlarging poly-Si grains during excimer-laser crystallization [63, 64]. The capping layer acts as a heat reservoir, returning the stored heat to the Si layer with some delay, and can therefore be used to obtain larger grains [49, 63]. Viatella et al. [38] reported that a capping layer can facilitate the growth of uniform poly-Si grains during excimer-laser crystallization.

In this section we shall investigate the effects of a SiO_2 capping layer in the μ-Czochralski (grain filter) process, and analyze its thermal effects on defect reduction. The capping layer acts as a heat reservoir during excimer-laser irradiation, and returns heat back to molten Si pool with a certain delay (Appendix A). The returned heat decreases the temperature gradient of the substrate underneath and extends the solidification period, hence enlarges the grains. A lower rate of solidification is expected to reduce the

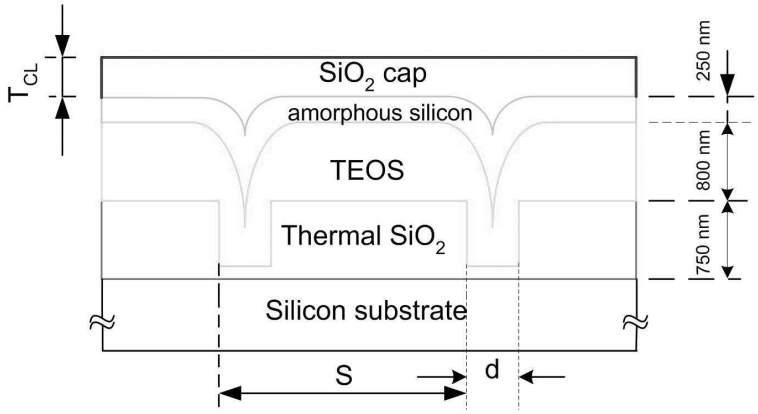


Figure 3.1: Schematic cross-sectional view of a grain filter with a capping layer: the thickness T_{CL} of the capping layer varies from 200 to 500 nm in 100 nm steps; the grid spacing (S) varies from 3 to 15 μm; the original diameter of the grain filter (d) is fixed at 1.0 μm.

number of generated defects.

3.1.2 Materials and Methods

The grain filter is fabricated using a routine process described in Section 1.2.

In the next step a 250 nm thick α-Si film is deposited on top of the grain filters in a conventional horizontal hot-wall LPCVD furnace, using pure silane as source gas. Then a SiO_2 capping layer, with a thickness (T_{CL}) between 200 and 500 nm is prepared via the decomposition of the TEOS precursor at $350°$C in a PECVD reactor.

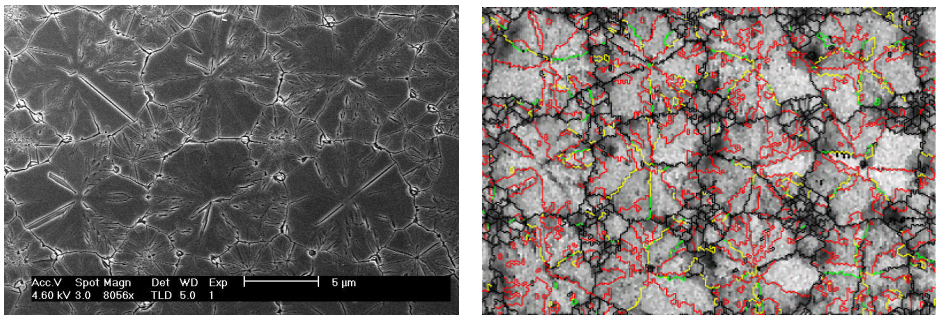
Figure 3.1 shows the schematic cross-sectional view of the entire structure with stacked layers. A similar structure with the same parameters but without the capping layer is prepared for reference purposes.

α-Si films are crystallized in a high-vacuum chamber (1.33×10^{-5} Pa) by a single shot (pulse duration = 50 ns) of XeCl excimer laser (XMR 7100 system) at a temperature of $450°$C and energy density (E_{l}) between 900 and 1600 mJ/cm^2, varied in 100 mJ/cm^2 steps.

The crystallized samples are checked by SEM and EBSD after Secco etching. The average grain size is calculated from the SEM images. The microstructure and grain boundary components are determined by EBSD analysis.

3.1.3 Experimental Results

Figure 3.2(a) shows a SEM image of grains after Secco etching. The thickness of the capping layer is $T_{\mathrm{CL}} = 200\,\mathrm{nm}$, while the energy density of laser pulse is $E_{\mathrm{l}} =$



(a) (b)

Figure 3.2: (a) SEM image of crystallized location-controlled silicon grains. The thickness of the capping layer (T_{CL}) is 200 nm, while the energy density of the laser pulse (E_{l}) is 1400 mJ/cm^2. (b) Grain-boundary-component map overlaid with an image quality map obtained from EBSD analysis. Black lines indicate random grain boundaries, while yellow and green lines show Σ3, Σ9, and Σ27 boundaries, respectively.

1400 mJ/cm^2. The microstructure shows the location-controlled grains grown superlaterally from grain filters in an equiaxial aspect. The spacing of grain filters (S) is 8 µm, and grains coalesce with their neighbors. Application of a capping layer increases the grain size to 9 µm; this will be discussed in Appendix A.

Figure 3.2(b) shows a map of the grain boundaries measured and investigated by EBSD analysis. The sub-boundaries inside the grains are mainly of CSL types [50], dominantly Σ3 boundaries, followed by Σ9 and Σ27 boundaries. It should be noted that random grain boundaries (indicated by black lines) occur very rarely inside location-controlled grains.

As expected on account of the low solidification rate, the application of the capping layer does not reduce the number of CSL grain boundaries inside grains – compare Fig. 1.4 (page 11) and Fig. 3.2(b). However, the grain size is increased by the application of a capping layer; this will be discussed in Appendix A.

The exact reason why a capping layer is inefficient at defect reduction is not understood yet. Probably, the low rate of solidification with a capping layer is still far from the solidification rate in thermal equilibrium, which suppresses defect generation considerably. Defects could be generated in earlier phases of solidification: the long subsequential phase due to the presence of the capping layer does not have a strong impact on defect generation.

3.1.4 Summary

Defect reduction cannot be achieved by the application of a capping layer in the µ-Czochralski process alone. The thermal effects of the capping layer are not sufficiently strong on the scales of ultra-fast melting and solidification due to excimer-laser crystal-

Table 3.1: Designation for seeds with different crystallographic orientation.

Designation	Description
(100)-oriented seed (or wafer)	Surface normal direction of $\langle 100 \rangle \pm 1^\circ$, with primary flat orientation of $\langle 110 \rangle \pm 1^\circ$
(111)-oriented seed (or wafer)	Surface normal direction of $\langle 111 \rangle \pm 1^\circ$, with primary flat orientation of $\langle 110 \rangle \pm 1^\circ$
(110)-oriented seed (or wafer)	Surface normal direction of $\langle 110 \rangle \pm 1^\circ$, with primary flat orientation of $\langle 111 \rangle \pm 1^\circ$

lization.

If defects could be generated principally at the beginning of solidification, introducing a seed at the bottom of the grain filter should have strong impact on defect generation as solidification would start from the seed. We shall investigate this possibility in the next section.

3.2 Effects of a Seed on Defect Reduction

3.2.1 Introduction

In this section we shall investigate the effects of a seed on defect generation during the μ-Czochralski process. In a standard grain filter seeds are randomly selected from fine poly-Si grains that resulted from explosive crystallization (Fig.1.2). It is hardly possible to put a desired seed directly into the bottom of a standard grain filter (Fig. 1.1) – and even if it were possible, it would be excessively difficult to prevent it from melting during excimer-laser irradiation.

Therefore the effects of a seed on defect generation are investigated using a modified grain filter with openings to a silicon substrate that functions as a seed at the onset of solidification. The processes that lead to the formation of openings at the bottom of the grain filters and subsequent selective epitaxial growth (SEG) through the openings are simulated on monocrystalline (100)-, (111)-, and (110)-oriented Si wafers and (100)-oriented SOI wafers as seeds. This experimental simulation of growth (or solidification) from a seed aims at the systematic investigation of the effects of seeds on defect generation.

The formation mechanism of CSL grain boundaries could be related to the crystallographic orientation of the seed. In this section, effects of crystallographic orientation on the CSL boundary formation are also studied for wafers with different orientations. The terms used in this section for wafers with different orientations are summarized in Table 3.1.

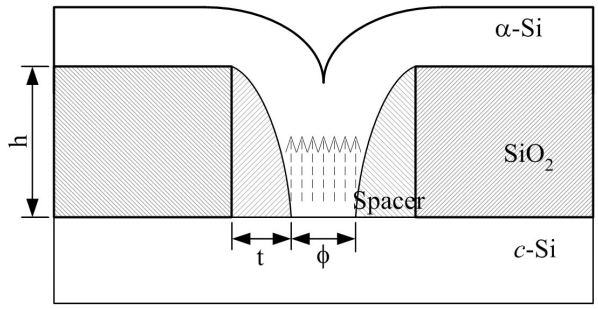


Figure 3.3: Schematic cross-sectional view of the selective epitaxial growth of single-crystalline grains through a SiO_2 window with silicon wafer as seed. The step height h is either 450, 600, or 750 nm; t is the spacer offset, and ϕ is the diameter of the opening to the seeds at the bottom of the grain filter. Dashed arrows indicate the vertical growth from the seed after excimer-laser irradiation.

3.2.2 Materials and Methods

Fabrication

To investigate the effects of seeds and their crystallographic orientation on defect generation, (100)-, (110)-, and (111)-oriented bulk-Si wafers and (100)-oriented SOI wafers (Si thickness: 200 nm) are used as seeds. The SiO_2 insulator is deposited on the substrates by PECVD using a TEOS precursor at a temperature of $350°C$. Windows for epitaxial seeds are opened by anisotropic RIE etching in a C_2F_6-CHF_3 plasma. Next, a second TEOS oxide layer is deposited by PECVD, and a second anisotropic etching is carried out to completely remove the second TEOS layer except for the oxide on the sidewalls of the first layer, forming an oxide sidewall spacer. Sidewall spacers are commonly used in lightly doped drains (LDD) in CMOS technology and applications of tiny geometry [12]. The spacer offset t is determined by the secondary TEOS deposition and RIE used in the fabrication of spacers. The spacer offset reduces the window opened to the silicon surface. To open the hole (both for 1st and 2nd oxide), two methods are used:

Method i: ***Dry etching combined with a wet soft-landing step*** To reduce plasma damage on the silicon surface [65, 66], RIE stops just before landing on the c-Si layer, and the rest of the TEOS in the holes is etched by 7:1 BHF (soft-landing step). The transition from RIE to wet etching is determined by the uniformity of the RIE etching rate (on the whole wafer).

Method ii: ***Dry etching combined with a dry soft-landing step*** To avoid isotropic wet etching of the spacer, wet soft-landing is replaced by a dry soft-landing step. Typically, the oxide layer is etched with 300 W RF power, while in the dry soft-landing step 50 W RF power is used.

The designed final thickness of the SiO_2 layer is either 450, 600, or 750 nm for each orientation. The final thickness of the SiO_2 layer is the same as the step height h of the grain filters, i.e., the vertical growth height during epitaxial growth.

To ensure a good contact for epitaxial growth, the native oxide of the exposed silicon is removed before the deposition of α-Si by dipping the whole wafer into a 0.55% HF solution for 4 minutes. A 250 nm thick α-Si layer is deposited on the SiO_2 layer with openings to the underlying seeds in an LPCVD furnace using silane as precursor gas.

The α-Si film is crystallized by a single pulse (duration: 50 ns) of XeCl excimer laser (wavelength: 308 nm) in a vacuum chamber at a pressure of 1.33×10^{-5} Pa. Laser fluence is varied from 700 to 1400 mJ/cm^2 in 100 mJ/cm^2 steps. The substrate is heated up to 450°C. To investigate the effects of substrate heating, three (100)-oriented wafers with different step heights are crystallized at room temperature and compared.

Numerical Simulations

Axisymmetric numerical simulations of transient heat transfer are carried out to investigate the melt depth during excimer-laser crystallization. The simulations are done using the finite-element method (FEM) based on the equations of heat conduction and solid/liquid phase transformation with the release or absorption of latent heat. The stacked layers along the symmetry axis feature an α-Si (250 nm)/c-Si (semi-infinite) structure for the bulk Si substrate, and an α-Si (250 nm)/c-Si (200 nm)/SiO_2 (semi-infinite) structure for the SOI substrate. More details about the simulations can be found in Section 2.3.

Characterization

After crystallization and Secco etching, the morphology of the grains and grain boundaries is investigated by SEM. Epitaxial regrowth is studied using cross-sectional TEM. The microstructure and microtexture are analyzed by EBSD.

3.2.3 Results and Discussion

In this subsection the effects of process parameters (laser fluence, substrate heating, methods used for opening holes) and crystallographic orientation on defect generation are investigated. To facilitate comparison, these effects are studied on grains grown from (100)-oriented seeds.

Effects of Laser Fluence (E_l)

Figure 3.4 shows the morphology of grains/islands at predetermined locations specified by the position of the grain filters. It indicates that location control can be achieved with openings at the bottom of grain filters. These grains/islands grow vertically from "seed" areas beneath the grain/island centers, and continue to grow laterally over the SiO_2 layer. The grain has an equiaxial aspect because of the equal lateral growth rates in all in-plane

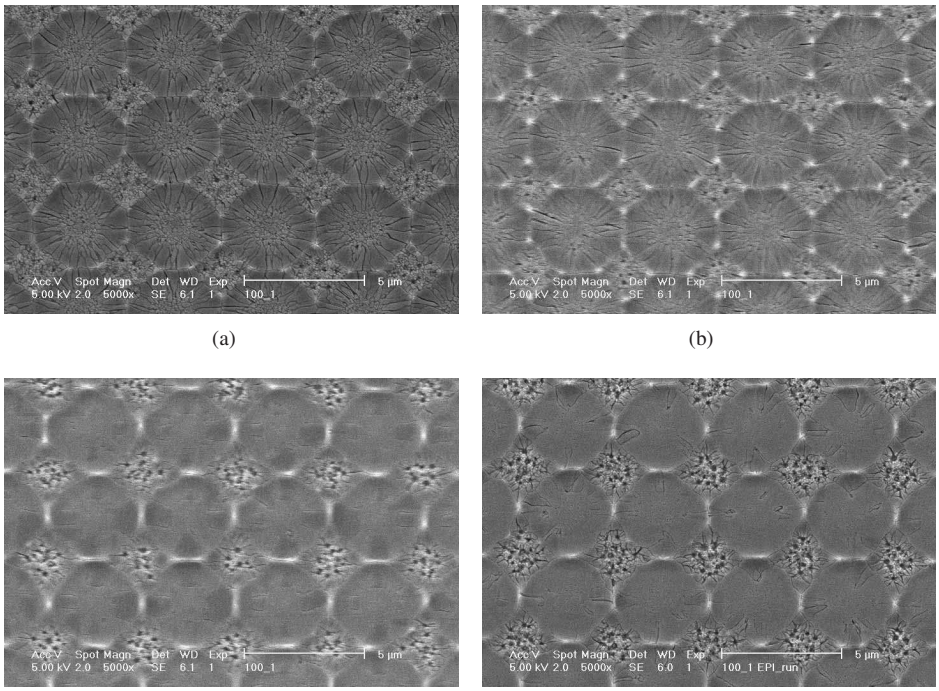


Figure 3.4: Grains grown from (100)-oriented wafers with wet soft-landing (method (i)); the step height is 450 nm and the substrate is heated up to 450°C with a laser fluence E_{l} of (a) 900 mJ/cm^2, (b) 1100 mJ/cm^2, (c) 1300 mJ/cm^2, (d) 1400 mJ/cm^2.

directions. At low laser fluence – Figs. 3.4(a) and 3.4(b) – fine petal-like multi-grains appear at the island centers. At higher energies – Fig. 3.4(c) – the fine grains in the central area disappear, and the island becomes a single grain. Finally at sufficiently high laser fluence – Fig. 3.4(d) – all islands become single-crystalline grains with some planar defects (grain boundaries) at the edge of grains.

Figure 3.4(d) shows single-crystalline location-controlled grains – more specifically, monocrystalline grains in the µm range without CSL grain boundaries. This indicates that defects can be completely eliminated by means of a seed. The diverse morphologies in Fig. 3.4 indicate that sufficient laser fluence is indispensable for defect reduction.

A plausible explanation for this change in morphology is that the melt front of silicon (in the vertical direction, i.e., perpendicularto the α-Si surface) increases with laser fluence, as shown schematically in Fig. 3.5. When the laser fluence is low – Fig. 3.5(c) –, the melt front of silicon stops before reaching the silicon seeds, resulting in multiple fine grains. On the other hand, with a sufficiently high laser fluence – Fig. 3.5(b) – the silicon melt front reaches the silicon substrate, hence a grain can grow epitaxially from

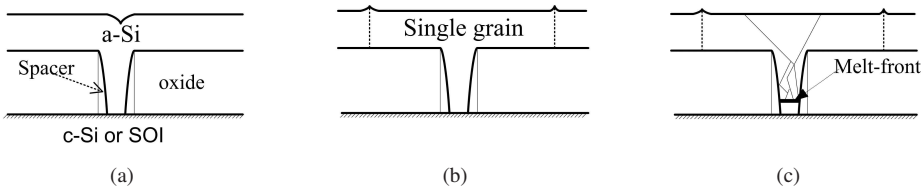


Figure 3.5: Schematic explanation of the effects of melt depth on the morphology of grains: (a) cross section of the experimental configuration; (b) melt front reaching the α-Si/c-Si interface, resulting in a single grain; (c) melt front not reaching the interface, resulting in multiple fine grains.

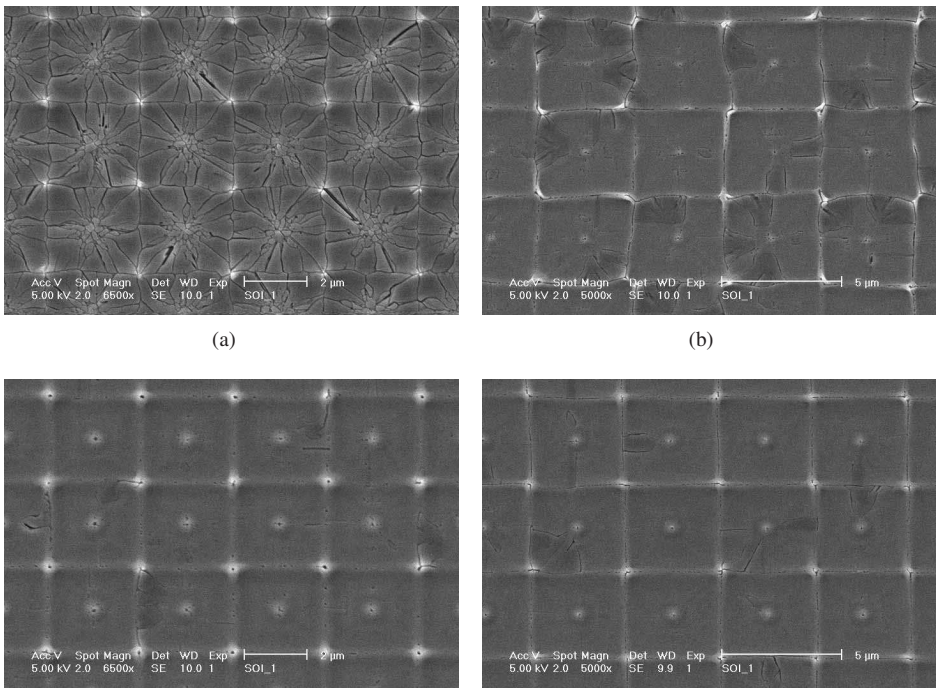
the seed, giving rise to a single-crystalline grain.

The morphology of grains grown from (100)-oriented SOI wafers (Fig. 3.6) shows similar dependence on laser fluence. However, single grains can be observed at much lower energy densities (900 mJ/cm^2) than for the bulk (100)-oriented seeds (1300 mJ/cm^2). Figure 3.6 shows that the grains grown epitaxially from neighboring seeds meet and coalesce, forming single-crystalline Si grains over the buried oxide layer. This is an alternative way to produce SOI structure.

Numerical simulation results (Fig. 3.7) show that the melt depth increases with laser fluence for bulk silicon wafers and SOI wafers alike – however, the increase is much faster for the latter than for the former. At 800 mJ/cm^2 [Fig. 3.6(a)] the melt depth is almost the same in the two cases but it increases much faster for SOI wafers, and reaches the seed ($>$ 250 nm) at 900 mJ/cm^2 (Fig. 3.6(b)). This occurs only at 1300 mJ/cm^2 [Fig. 3.6(d)] for bulk Si seeds. When the melt depth reaches the α-Si/c-Si interface, single-crystalline grains start to grow from the seed (inset images of grains in Fig. 3.7). The thermally insulating SiO_2 layer beneath the Si layer of the SOI wafer conducts less heat to the substrate than in a bulk wafer configuration, hence α-Si is heated up faster, the melt front can reach the α-Si/c-Si interface, and grow epitaxially into a single grain. The energy density window for obtaining single-crystalline Si grains on SOI wafers is open between 900 and 1400 mJ/cm^2, it is therefore much wider than for bulk Si wafers. Above 1400 mJ/cm^2, agglomeration occurs in silicon materials.

Effects of Substrate Heating

Figure 3.8 shows the morphology of grains crystallized at room temperature. These grains, produced without substrate heating, are multiple grains with radial grain boundaries. Even with laser fluence up to the threshold of agglomeration, 1400 mJ/cm^2, the islands are multi-grains [Fig. 3.8(b)]. However islands produced with substrate heating (450°C) at 1400 mJ/cm^2 are single grains without grain boundaries inside [Fig. 3.4(d)]. There is a shallow indentation at the center of grains crystallized at 900 mJ/cm^2. This disappears at 1400 mJ/cm^2 [Fig. 3.8(b)] or upon the application of substrate heating [Fig. 3.4(a)], which indicates that the surface roughness of crystalized Si is improved



(a) (b)

(c) (d)

Figure 3.6: Grains grown from (100)-oriented SOI wafers with a wet soft-landing step (method (i)); the step height is 450 nm and the substrate is heated up to $450°$C with a laser fluence of (a) 800 mJ/cm^2, (b) 900 mJ/cm^2, (c) 1000 mJ/cm^2, and (d) 1300 mJ/cm^2.

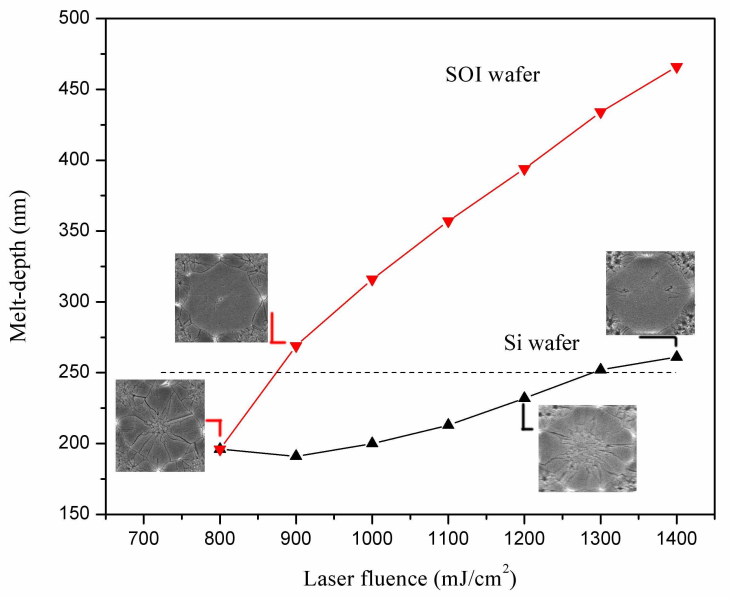


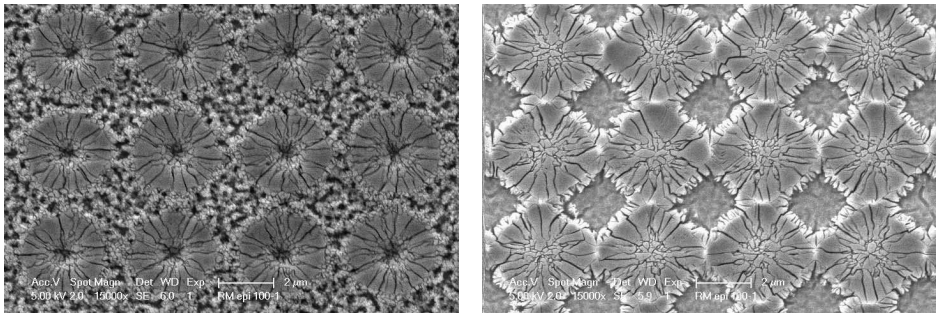
Figure 3.7: Simulated melt depth as a function of laser fluence. The insets show the corresponding grain morphologies observed experimentally.

due to a supply of sufficient energy – either by higher laser fluence or by substrate heating.

Figure 3.9 shows the simulated melt depths for both cases at room temperature and with substrate heating to $450°$C, indicating that the melt depth without substrate heating saturates at about 220 nm, leaving 30 nm Si unmolten. Without substrate heating the laser fluence is not sufficient to make the melt front reach the α-Si/c-Si interface, because the front is quenched by the cold bulk silicon underneath, which has a high thermal conductivity. This implies that for bulk silicon seeds it is impossible to obtain single grains – that is, to reduce defects by seeds – without substrate heating.

Effects of the Step Height

The step height h of the SiO_2 layer is either 450, 600, or 750 nm. The density of CSL grain boundaries is found to increase with increasing step height. Figure 3.10 shows a grain-boundary map of grains grown from (100)- and (110)-oriented seeds with step heights of 450 and 750 nm. The lines inside single-crystalline grains are CSL grain boundaries. For $h = 450$ nm the grains are single grains with some CSL boundaries at grain edges [Figs. 3.10(a) and 3.10(c)]. However, for $h = 750$ nm there are grain boundaries at the grain centers [Figs. 3.10(b) and 3.10(d)], i.e., the orientation changes with the step height, indicating that there is a higher probability of defect generation



(a) (b)

Figure 3.8: Grains grown from (100)-oriented bulk-Si wafers with a wet soft-landing step (method (i)); the step height is 450 nm and the laser fluence used in room-temperature excimer-laser crystallization is (a) 900 mJ/cm^2, (b) 1400 mJ/cm^2.

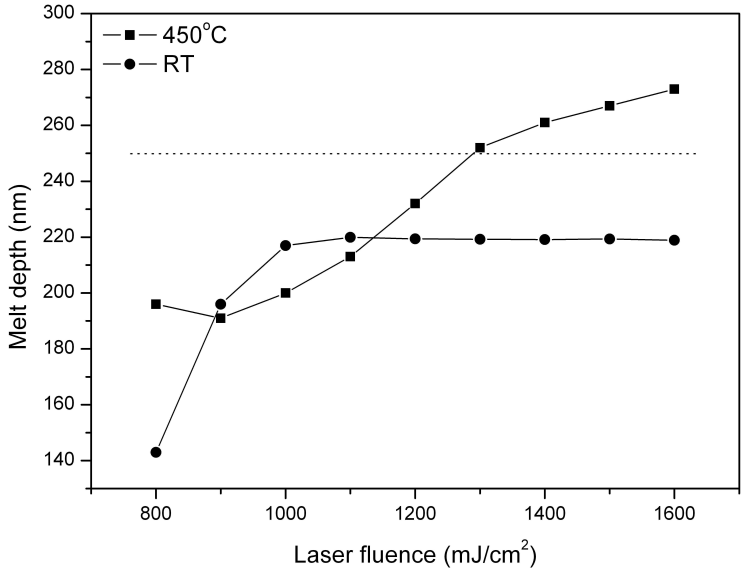


Figure 3.9: Simulated melt depth as a function of laser fluence for a bulk silicon seed crystallized at room temperature (RT), and with substrate heating to $450°$C. Without substrate heating the melt depth saturates before reaching the α-Si/c-Si interface.

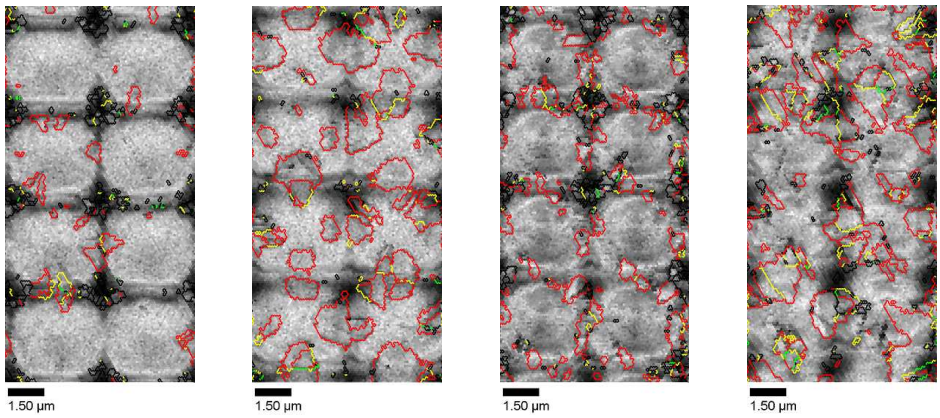


Figure 3.10: Grain-boundary maps of grains grown from (100)- [(a), (b)] and (110)- [(c), (d)] oriented wafers with method (ii). Samples are crystallized at 1200 mJ/cm^2 and 450°C; the step height is 450 nm [(a) and (c)] or 750 nm [(b) and (d)].

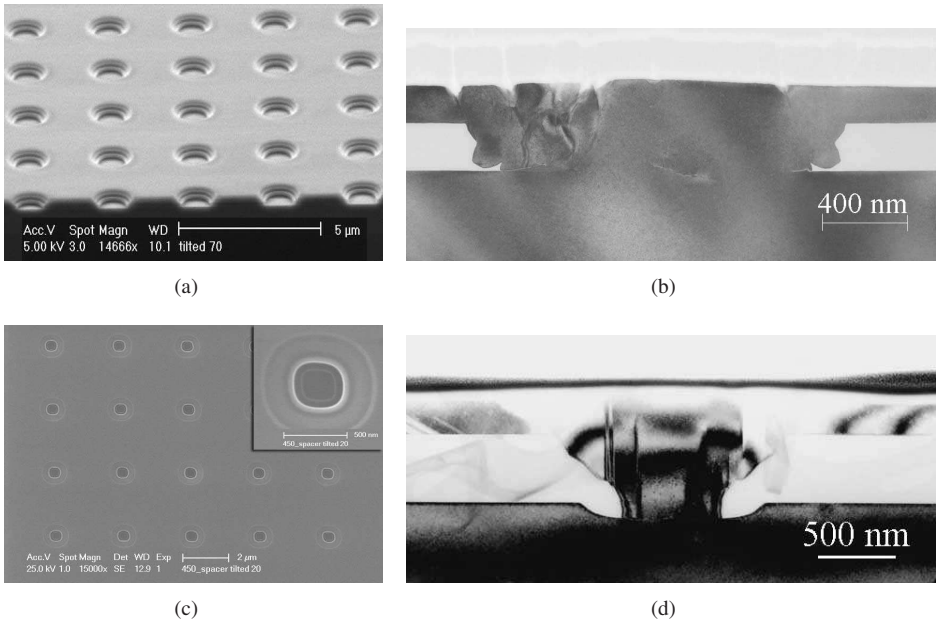
during vertical growth at larger step height.

Effects of the Landing Method

In method (i) dry etching is combined with a wet soft-landing step. This means that at a certain point the applied etching method changes from dry to wet etching. This transition depends on the uniformity of dry etching, since all the holes have to be opened. Figures 3.11(a) and 3.11(b) show cross-sectional holes produced by a wet soft-landing step. There are two possibilities to open the holes to the seed: by opening holes in the first TEOS layer, and by back-etching of the second TEOS film to form spacers inside the holes. In our investigations the uniformity of dry etching is poor, hence the wet soft-landing time is relatively long. Figure 3.11(a) shows that the sidewalls of the spacers are not smooth at all – instead, there are three under-etched rings. Under-etching resulting from wet etching is clearly seen in the cross-sectional TEM image [Fig. 3.11(b)]. It is difficult to control the hole diameter (ϕ) and the step height (h) in a long wet soft-landing step, thus the final hole diameter and step height are usually far from the designed values. For this reason, a dry rather than a wet soft-landing step is used for the anisotropic etching of holes, and the simultaneous reduction of plasma damage with low RF power.

Figure 3.11(c) shows the morphology of holes produced with a dry soft-landing step. The under-etching rings observed in Fig. 3.11(a) are absent now. Hole diameters are around 500 nm. The cross-sectional TEM images of the holes are shown in Figure 3.11(d). The slope of the spacer is much smoother and the step height is easily controlled.

Comparison of Figs. 3.11(b) and 3.11(d) shows that the dry soft-landing step gives



(a) (b)

(c) (d)

Figure 3.11: Cross-sectional SEM images of holes produced with (a) a wet soft-landing step; and (c) a dry soft-landing step. Sample (a) was tilted at 70°, while sample (c) at 20°. Cross-sectional TEM images of (b) grains grown from a (100)-oriented wafer with a wet soft-landing step; and (d) grains grown from a (110)-oriented wafer with a dry soft-landing step, crystallized at 1200 mJ/cm^2 with a step height of 450 nm.

rise to a large amount of over-etching. Since the etching rates for SiO_2 and Si are highly disparate for wet etching, hardly any over-etching is observed in Fig. 3.11(b).

In the ideal setup holes and spacers would be formed with sufficiently long dry etching followed by a very short wet soft-landing step. Then spacers would be smooth, without the under-etching rings in Fig. 3.11(a) and the marks of over-etching in Fig. 3.11(d). At the same time, the hole diameter (ϕ) and the step height (h) could be precisely controlled. This is essential since the geometry of the hole is important for a successful epitaxial growth from a seed.

Figure 3.12 shows the morphology of grains produced with a dry soft-landing method. The number of defects is obviously higher than in the grains shown in Fig. 3.4. For (100)-oriented seeds four small subgrains are observed near the center.

Defects inside grains result probably from the formation of facets on the slope of the grain filters. In wet etching no such orientation was observed because of the under-etching rings. Facet formation will be discussed in detail in Section 3.4.

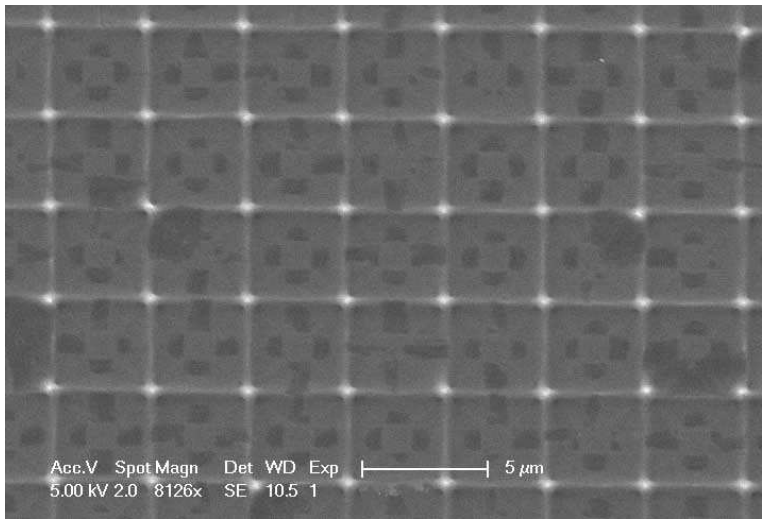


Figure 3.12: Grains produced from a (100)-oriented wafer with a dry soft-landing step (method ii) using excimer-laser crystallization and substrate heating to 450°C with a laser fluence of 1400 mJ/cm^2.

Effects of the Crystallographic Orientation of the Seed

Figure 3.13 shows the microstructure and microtexture of location-controlled Si grains produced from seeds of each orientation by means of a wet soft-landing step. The primary texture components of grains grown from (100)-, (110)-, and (111)-oriented wafers are $\{001\}\langle 1\bar{1}0\rangle$, $\{110\}\langle 1\bar{1}1\rangle$, and $\{111\}\langle 0\bar{1}1\rangle$, respectively. Note that in the pole figure (PF) not only the normal direction (ND) of the single grains is the same as in the underlying seed but also the in-plane orientation – i.e., the rolling direction (RD) and the transverse direction (TD). This indicates a successful epitaxial growth from the seeds – in other words, the crystallographic orientation of the grains is controlled by the seeds.

There is a grain boundary between the grain with the main orientation and sub-grains with different orientations. Figures 3.13(b), 3.13(d), and 3.13(f) show the grain-boundary-component maps of the Si islands obtained for seeds of various orientations. The map shows that the grain boundaries inside the islands are mainly of CSL types, and are normally at the edges of the islands. Grain boundaries inside the islands are mainly CSL $\Sigma 3$ grain boundaries, with a small proportion of higher-order – $\Sigma 9$ and $\Sigma 27$ – ones. The islands grown from (100) seeds have fewer grain boundaries than those grown from (110) and (111) seeds. It also shows that islands grown from (111)-oriented wafers have the highest number of CSL boundaries: this may be due to the pronounced facet formation on the growing solid-liquid interface in (111)-oriented seeds. Dense grain boundaries are observed at the edges of the islands grown from (110)-oriented seeds [Fig. 3.13(d)]. In islands grown from (111)-oriented seeds [Fig. 3.13(f)] the grain

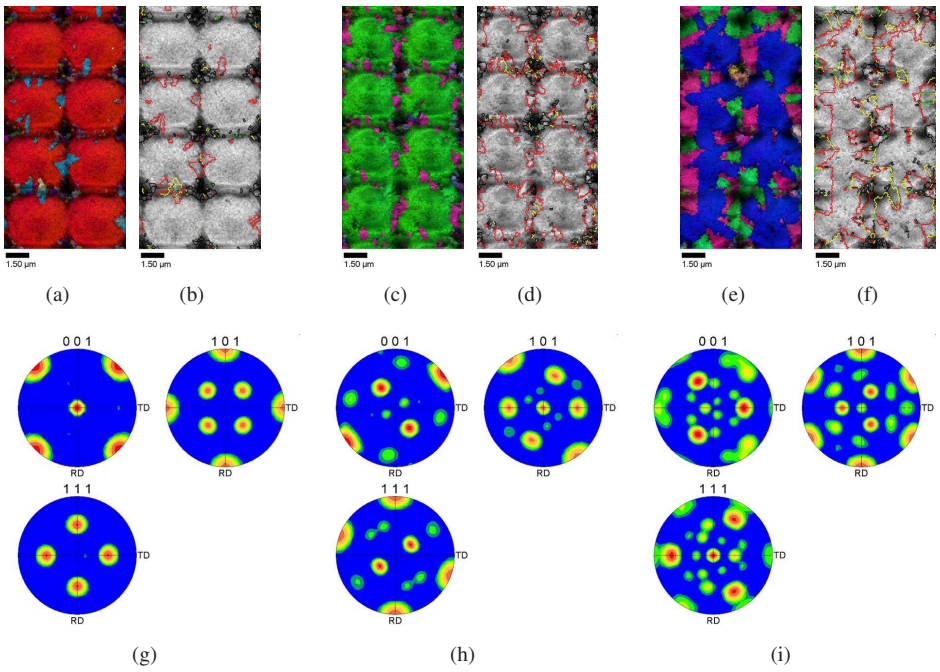


Figure 3.13: Inverse-pole-figure (IPF) maps [(a), (c), (e)], image-quality maps overlaid with grain-boundary-component maps [(b), (d), (f)], and pole figures [(g), (h), (i)] of grains grown from (100)- [(a), (b), (g)], (110)- [(b), (c), (h)], and (111)- [(e), (f), (i)] oriented seeds with a wet soft-landing step (method i) [step height: 450 nm, laser fluence: 1400 mJ/cm^2, substrate heating up to $450°$C]. The color code for CSL grain boundaries is: red – $\Sigma 3$; yellow – $\Sigma 9$; blue – $\Sigma 27$. Grain boundaries inside the islands are mainly $\Sigma 3$.

boundaries are near island centers, indicating that the seed orientation changes easily from (111) to some other direction.

Phases with secondary crystallographic orientation are observed at the edges of the grains grown from (100)- and (110)-oriented seeds, indicating that the change of crystallographic orientation occurs near the end of lateral growth. However, for grains grown from (111)-oriented seeds, the change of crystallographic orientation occurs at the grain centers, indicating that the $\langle 111 \rangle$ orientation changes easily to some other direction during vertical or lateral growth. Secondary textures are also observed in the pole figures of grains grown from (100)- and (111)-oriented seeds; they correspond to fine grains inside the single grains. However, no visible secondary texture components appear in grains grown from (100) wafers, which implies that orientation varies little between the main grain and the fine grains at the edges.

To summarize, using a wet soft-landing step, the epitaxial growth of (100)-oriented grains without defects is more easily achieved than that of (110)- and (111)-oriented grains. Thus, grains grown from (100)-oriented seeds have considerably fewer defects and show a stronger tendency to "inherit" the initial orientation than their (110)- and (111)-oriented counterparts. On the other hand, (111)-oriented seeds easily change their orientations.

Figure 3.14 shows the microtexture and microstructure of grains grown from wafers of different orientations using a dry soft-landing method.

EBSD analysis indicates that for grains grown from (100)-oriented seeds [Fig. 3.14(a)] the orientation is $\{001\}\langle 1\bar{1}0 \rangle$ over 92% of the EBSD scanned area [Fig. 3.14(g), in red]. The rest are CSL grain boundaries (or secondary twins) of the same orientation, as is shown in the grain-boundary-component map [Fig. 3.14(b)]. The boundaries are CSL boundaries: $\Sigma 3$ denotes $60^\circ @ \langle 111 \rangle$ twins with orientation changed to $\{212\}\langle 1\bar{4}1 \rangle$ or $\{122\}\langle 01\bar{1} \rangle$. Others are secondary boundaries, $38^\circ @ \langle 110 \rangle$ twins, with orientation changed to $\{\bar{3}16\}\langle 3\bar{1}\bar{5}4 \rangle$.

For grains grown from (110)-oriented seeds [Fig. 3.14(c)], the orientation in green is $(011)[\bar{1}\bar{1}1]$ or $(011)[1\bar{1}1]$. The orientation in purple is $(114)[1\bar{5}1]$ or $(\bar{1}41)[1\bar{1}5]$. Green regions are separated by $\Sigma 3$ boundaries. In Fig. 3.14(d) a $\Sigma 3$ boundary is seen between a green region – $(011)[\bar{1}\bar{1}1]$ – and a purple region. Purple regions are separated by $\Sigma 9$ boundaries. $\Sigma 9$ boundaries also appear between green – $(011)[1\bar{1}1]$ – and purple – $(\bar{1}41)[1\bar{1}5]$ – regions.

For grains grown from (111)-oriented wafers [Fig. 3.14(e)], the orientation is $\{110\}\langle 1\overline{11} \rangle$ (blue) over about 70% of the EBSD scanned area. This proportion is accounted for by the three main (110) orientation components and their CSL grain boundaries. More detailed analysis [Fig. 3.14(i)] shows a relatively even mix of three types of near-(110) grains: $(110)[001]$ makes up 15% of the scanned area, $(110)[1\bar{1}1]$ 14%, and $(110)[\bar{1}11]$ 14%. The rest is assumed to be due to CSL grain boundaries. The secondary orientation, shown in purple, is $(\bar{1}15)[1\bar{4}1]$ or $(115)[1\bar{1}0]$. Most grain boundaries between three blue regions, or between a blue region and a purple region are $\Sigma 3$, i.e., twins with $60^\circ @ \langle 111 \rangle$. Again, (111)-oriented seeds change their orientation easily to (110) or some direction.

Comparison of Figs. 3.13 and 3.14 shows that about 50% more defects are generated by dry soft-landing. No damage occurs on the surface when wet soft-landing is applied.

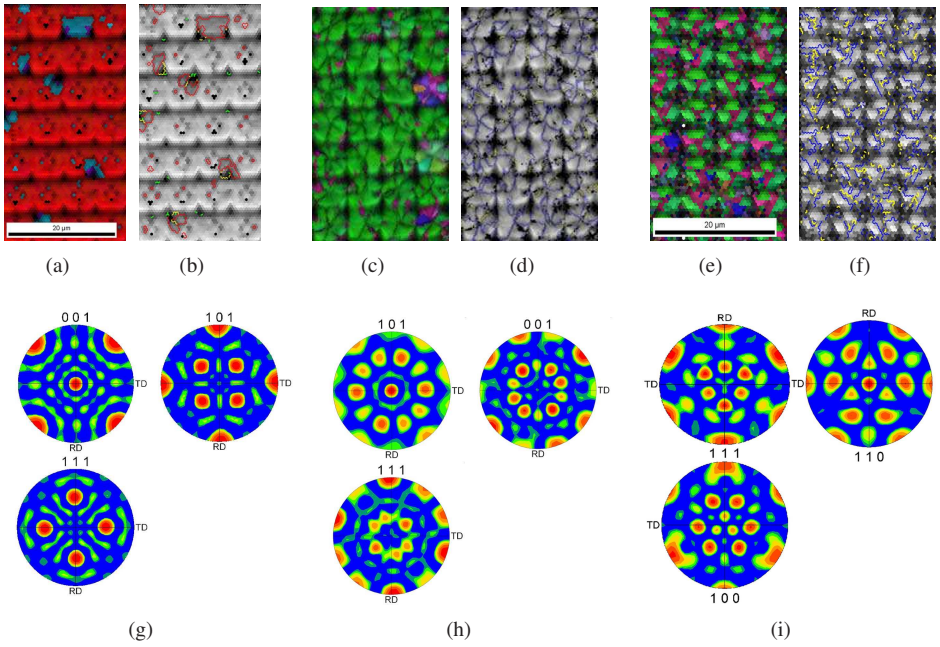


Figure 3.14: Inverse-pole-figure maps [(a), (c), e)], image-quality maps overlaid with grain-boundary-component maps [(b), (d), (f)], and pole figures [(g), (h), (i)] of grains grown from (100)- [(a), (b), (g)], (110)- [(b), (c), (h)], and (111)- [(e), (f), (i)] oriented wafers with a dry soft-landing step (method ii) [step height: 450 nm, laser fluence: 1400 mJ/cm^2, substrate heating up to $450°$C]. The color code for CSL grain boundaries is: red – Σ3; yellow – Σ9; blue – Σ27. Grain boundaries inside the islands are mainly Σ3.

However, the geometry of the holes produced by wet soft-landing is different from that obtained by dry soft-landing (Fig. 3.11), which may also be the reason for this difference. Defect generation could be related to facets generated at the solid/liquid interface when the interface satisfies some geometrical conditions [67]. This will be discussed in detail in the next section.

3.2.4 Summary

The number of defects can be significantly reduced by introducing a seed at the bottom of the grain filter. The efficiency of defect reduction depends both on internal factors, such as orientation and hole geometry (diameter of opening, step height, slope of sidewall, etc.), and external factors, such as laser fluence and substrate heating.

Melting of the α-Si layer down to the seeds is a prerequisite for successful epitaxial growth. This requirement imposes constraints on the external factors: sufficient laser fluence is essential, as indicated in Figs. 3.4 and 3.6. Substrate heating is also indispensable for the melt front to reach the seeds if the seeding layer is thick (Fig. 3.9).

The microtexture and microstructure of the oriented grains are predominantly determined by internal factors, such as seed orientation and hole geometry. Figures 3.14 and 3.13 show the effects of the seed orientation. The "inheritability" of orientation is much higher for the (100) orientation than for (110) or (111); the reason for this will be explained in detail in the next section.

The geometrical parameters of the holes – such as the step height h, the hole diameter ϕ, and the slope of the sidewall – are crucial for defect reduction. The geometry of a hole depends on the applied landing method (Fig. 3.11). In an optimized process, dry etching would last much longer, and it would be combined with a shorter wet soft-landing. This would provide anisotropic etching of the holes without plasma damage at the seed surfaces and would prevent over-etching of the seeds.

The number of defects can be significantly reduced by means of a seed and the application of substantial substrate heating as well as sufficient laser fluence. Using (100)-oriented seeds leads to much more efficient defect reduction than using seeds of other orientations.

3.3 Crystal Shape of Grains Grown from Seeds of Different Orientations

Grains grown from seeds of different orientations have specific crystal shapes (morphologies) when the spacing S of grain filters is much larger than the grain size.

The crystal shape is determined by the surface free energy (or surface tension). The surface free energies for $\{100\}$, $\{110\}$, and $\{111\}$ planes in bulk silicon are summarized in Table 3.2. The surface free energy is lower for the $\{111\}$ plane than for the $\{110\}$ and $\{100\}$ planes. Although surface-free-energy data are not available for each plane on the insulating surface (SiO_2) at higher temperatures (close to the melting point), the same trend is expected as in Table 3.2.

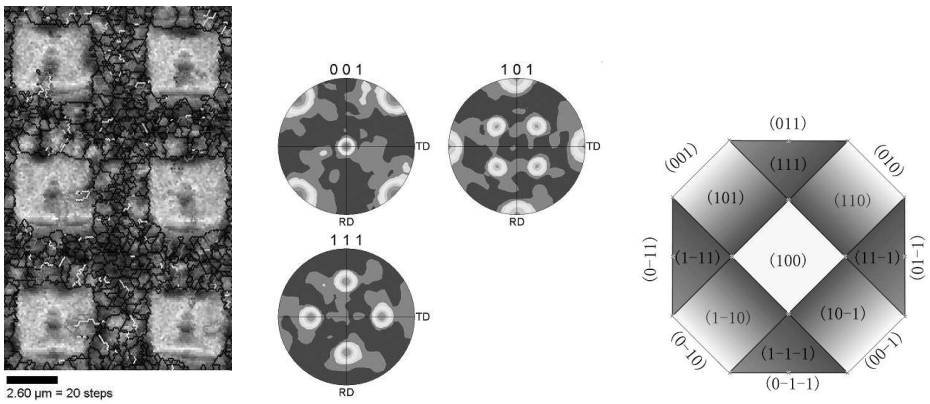
Table 3.2: Surface free energy of different crystallographic planes in bulk silicon [68].

Plane	{100}	{110}	{111}
Surface free energy [mJ/cm^2]	0.213	0.151	0.123

The grains in Figs. 3.13 and 3.14 coalesce because the spacing of grain filters (Fig. 1.1) is less than or equal to the diameter of the grains. When the spacing is much larger than the grain diameter, the grains are separated from each other by fine poly-Si grains. An individual grain has a specified crystal shape. Variations of the crystal shape with the spacing of grain filters is due to thermal interactions (or heat perturbations) in front of the solidification front.

In this section we shall discuss the crystal shape of individual grains, as opposed to the coalesced grains discussed in Section 3.2. Finally, the orientation dependence of the number of defects will be discussed, and related to crystal shapes.

3.3.1 Crystal Shape of Grains Grown from (100)-Oriented Seeds



(a) (b) (c)

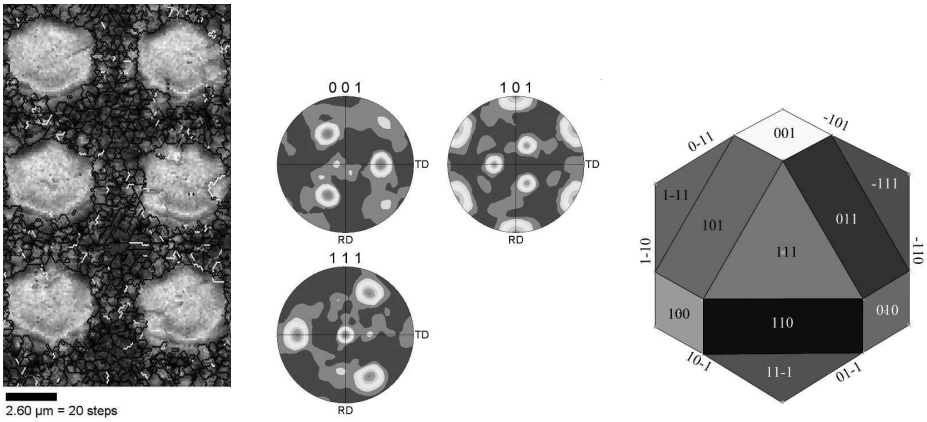
Figure 3.15: Individual grains grown from (100)-oriented seeds with a wet soft-landing step, substrate heating up to $450°$C, and a laser fluence of 1400 mJ/cm^2. (a) EBSD image-quality map overlaid with CSL grain-boundary-component map, clearly showing that grains are square-shaped. (b) Pole figure of the grains. (c) Schematic drawing of the crystal shape of grains grown with normal direction $\langle 100 \rangle$ and transmission direction $\langle 1\bar{1}0 \rangle$.

Figure 3.15 presents the microstructure and microtexture of separated grains grown

from (100)-oriented seeds. Figure 3.15(a) shows that there is a clear border between epitaxial grains and surrounding randomly oriented fine grains, and that (100)-oriented grains are square-shaped and aligned. Figure 3.15(b) shows that grains have the same orientation – $\{001\}\langle 1\bar{1}0\rangle$ – as the seeds. A grain grown from a (100)-oriented seed first undergoes vertical growth and then lateral growth. The diameter of grain is much larger than that of the openings. The crystal shape is therefore assumed to be the result of lateral growth. Figure 3.15(b) indicates that there are two possibilities for the crystal shape: (1) by connecting four $\langle 001\rangle$ poles (in the equatorial plane) the crystal shape has four $\{110\}$ outer surfaces; (2) by connecting four $\langle 101\rangle$ in-plane poles (in the equatorial plane) the crystal shape has four $\{001\}$ outer surfaces. The first square is tilted by 45 degrees with respect to the second. Figure 3.15(c) shows these two possibilities for the crystal shape: the outer surface is either $\{110\}$ or $\{100\}$.

However, due to the anisotropic surface free energy (Table 3.2), the surface tension of $\{100\}$ is much higher than that of $\{110\}$. Thus only one possibility remains: square-shaped grains have $\{110\}$ outer surfaces. This also implies that growth is faster along the $\langle 100\rangle$ direction than along $\langle 110\rangle$.

3.3.2 Crystal Shape of Grains Grown from (111)-Oriented Seeds



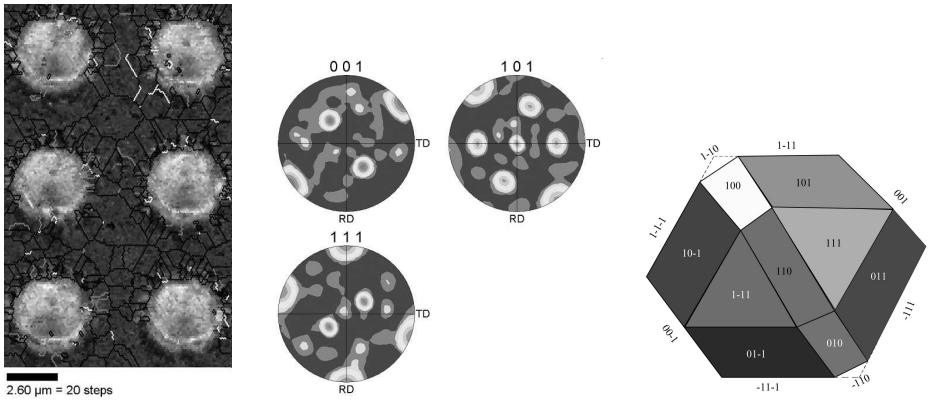
(a) (b) (c)

Figure 3.16: Individual grains grown from (111)-oriented seeds with a wet soft-landing step, substrate heating up to 450°C, and a laser fluence of 1400 mJ/cm^2. (a) EBSD image-quality map overlaid with CSL grain-boundary-component map, clearly showing that grains are hexagonal shaped. (b) Pole figure of the grains. (c) Schematic drawing of the crystal shape of grains grown with normal direction $\langle 111\rangle$ and transmission direction $\langle 2\bar{1}\bar{1}\rangle$.

Figure 3.16 presents the microstructure and microtexture of the grains grown from (111)-oriented seeds. Figure 3.16(a) shows that the crystal shape of $\langle 111\rangle$ grains is

hexagonal, and the grains are well aligned. Figure 3.16(b) shows the pole figures of such grains. The main texture is $\{111\}\langle 0\bar{1}1\rangle$. The only low in-plane index is $\langle 110\rangle$. By connecting six $\langle 110\rangle$ poles in a $\langle 110\rangle$ pole figure, a hexagonal shape is obtained. Figure 3.16(c) shows the hexagonal grain with normal direction (111) and rolling direction $(0\bar{1}1)$. The crystal of a $\langle 111\rangle$-oriented grain has six $\{110\}$ outer surfaces.

3.3.3 Crystal Shape of Grains Grown from (110)-Oriented Seeds



(a) (b) (c)

Figure 3.17: Individual grains grown from (110)-oriented seeds with a wet soft-landing step, substrate heating up to $450°$C, and a laser fluence of 1400 mJ/cm^2. (a) EBSD image-quality map overlaid with CSL grain-boundary-component map, clearly showing that the grains are hexagonal shaped. (b) Pole figure of the grains. (c) Schematic drawing of the grains grown with normal direction $\langle 110\rangle$ and transmission direction $\langle \bar{1}1\bar{2}\rangle$.

Figure 3.17 presents the microstructure and microtexture of grains grown from (110)-oriented seeds. The crystal shape is observed to be almost hexagonal [Fig. 3.17(a)]. The grains are also well aligned, and their in-plane orientation is different from that of (111)-oriented grains [Fig. 3.16(a)]. Each of $\langle 100\rangle$, $\langle 110\rangle$, and $\langle 111\rangle$ can be one of the in-plane orientations (i.e., orientations in the plane of RD and TD). By connecting the in-plane poles of two orientations (four $\langle 111\rangle$ and two $\langle 100\rangle$), a hexagonal shape can be obtained. Figure 3.17(c) shows the crystal with normal direction $\langle 110\rangle$. The hexagonal shape indicates that two $\langle 110\rangle$ orientations – $[\bar{1}10]$ and $[1\bar{1}0]$ in Fig. 3.17(c) – do not occur as outer surfaces. This is possibly because nearby $\{111\}$-oriented outer surfaces grow much more easily.

The in-plane orientations $\langle 110\rangle$ and $\langle 111\rangle$ are close to each other. Hence, the crystal shape of grains grown from $\{110\}$-oriented seeds is not so well pronounced as in Figs. 3.15 and 3.16.

The crystal shape of individual grains is determined by the normal direction of the

seeds. The orientation of individual grains (the in-plane alignment) is determined by the in-plane orientation of the seeds.

3.3.4 Defect Generation for Each Seed Orientation

Figure 3.15 shows individual grains grown from (100)-oriented seeds. There are four possible $\{111\}$ facet planes [Fig. 3.15(c)] from where defects can originate. These planes are facet planes during the vertical growth phase along the crystallographic orientation $\langle 100\rangle$; this might explain why there are four subgrains in Fig. 3.12. This will be discussed in detail in the next section.

In grains grown from (111)-oriented seeds vertical growth is very easily changed into growth along $\langle 110\rangle$ (Fig. 3.16); this may be the reason for the strong $\langle 110\rangle$ (rather than $\langle 111\rangle$) texture in the normal direction for (111)-oriented seeds (Fig. 3.14). There are three $\{110\}$ planes along the $\langle 111\rangle$ direction [Fig. 3.16(c)], leading to three evenly mixed $\langle 110\rangle$ orientations for grains grown from (111)-oriented seeds [Fig. 3.14(i)].

In grains grown from (110)-oriented seeds there are few possibilities for in-plane orientations – $\langle 111\rangle$, $\langle 100\rangle$, and $\langle 110\rangle$ –; the change from one to another gives rise to a CSL boundary. This might explain the large number of CSL boundaries generated in grains grown from (110)-oriented seeds.

Compared to (110)- and (111)-oriented seeds, there are fewer possibilities for (100)-oriented ones to change orientation (both in the normal and in-plane directions). This may be the underlying reason for the lower number of defects in (100)-oriented grains than in non-(100)-oriented ones.

3.4 Facet Formation in (100)-Oriented Grains

3.4.1 Defect Generation in (100)-Oriented Grains

In Fig. 3.12 four secondary subgrains are observed in each grain grown from a (100)-oriented seed, at identical positions in each grain. This feature can be traced back to facet formation during vertical growth [67] at the three-phase boundary (TPB) of molten Si, solidified Si, and insulating SiO_2, where a specific crystallographical plane satisfies an angle condition between the edge facet and the extension of crystal surface.

Figure 3.18 shows schematically the formation of facets near the TPB. These facets could be extended into large crystallographic planes during the subsequent growth phase, forming grain boundaries or stacking faults. This means that the facets are at the origins of these defects.

Figure 3.19 shows the top-view bright-field TEM image of a grain. One main grain – featuring four subgrains – is grown from each hole. By rotating one subgrain through 90° around the normal direction (namely, $\langle 001\rangle$), the subgrains can "repeat" the pattern, i.e., the positions of the four subgrains exhibit fourfold symmetry. Viewed from the top, these secondary grains are of triangular shape. The secondary subgrains are "attached" to the sidewalls of the hole. Sidewalls grow from bottom to top, and become larger, forming

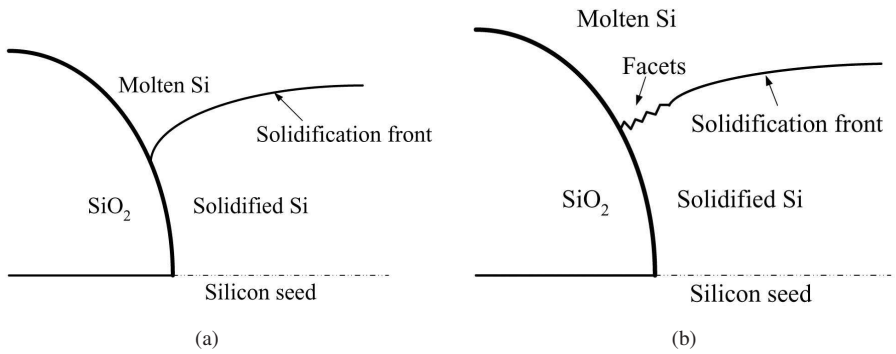


Figure 3.18: Schematic representation of facet formation at the three-phase boundary: (a) facets are absorbed at the boundary, and the l-Si/c-Si interface remains smooth; (b) facets are not absorbed, and the l-Si/c-Si interface near the three-phase boundary (TPB) features facets.

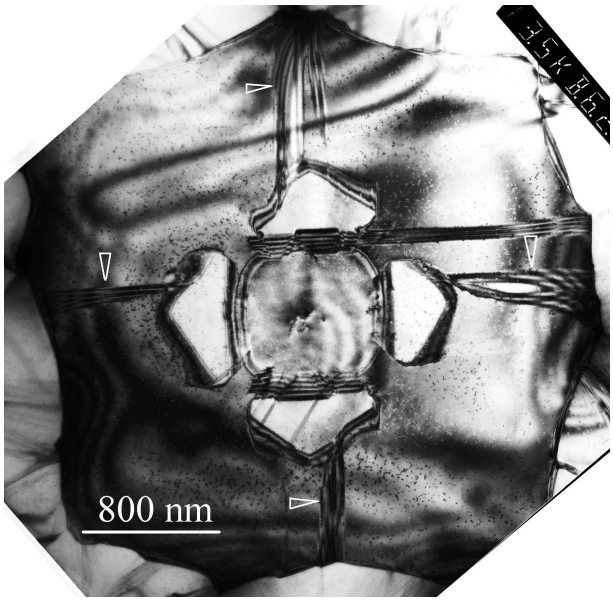
upside-down pyramids. Four secondary grains grow from the four sides of the square holes. The other defects (indicated by triangles) are twins, generated at the subgrain edges, forming twin lamellae.

The relative crystallographic orientation of the main grain and the subgrains is determined by selective-area diffraction. The grain boundaries between the main grain and the subgrains are of CSL $\Sigma 3$ type, i.e., by rotating the main grain through 180° around $\langle 111 \rangle$, certain lattice points of the main grain overlap with those of the subgrain. The surface orientation of the secondary subgrain is $\langle 221 \rangle$, and its lateral growth direction is $\langle 114 \rangle$. Secondary subgrains are grown aligned with $\langle 110 \rangle$ oxide sidewalls with respect to the main grain. These subgrains are grown from $\langle 111 \rangle$ facets.

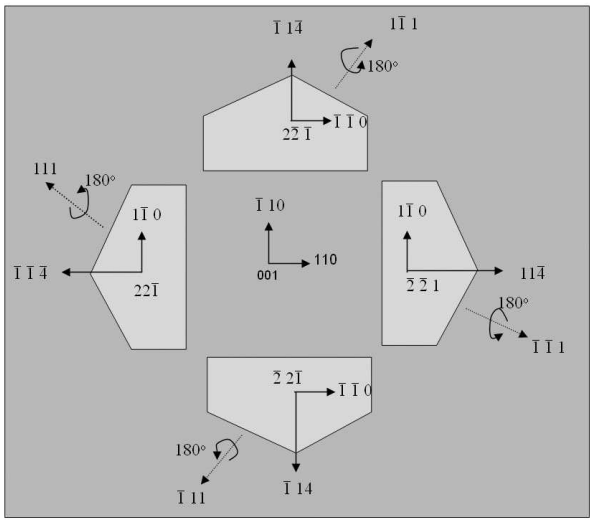
The evolution of the main grain consists of a first phase of vertical growth from the seed, followed by a lateral growth over the Si/SiO_2 interface. One of the most interesting features is that lateral growth may bypass the secondary subgrains and continue until the subgrains are surrounded. This may be due to the disparate growth rates along the $\langle 001 \rangle$ and $\langle 114 \rangle$ directions. The lower growth rate along the $\langle 114 \rangle$ direction imposes a limit on the growth of secondary subgrains, and allows growth along the $\langle 100 \rangle$ direction to the point when they are surrounded.

Figure 3.20 shows the cross-sectional TEM images $\langle 100 \rangle$-oriented grains grown epitaxially from the substrate. Some twins, dislocations, or stacking faults are generated near the epitaxial growth interface, however, all these defects are reduced during the vertical growth phase. The high density of defects near the α-Si/c-Si interface is due to the high speed of solidification, more specifically to the heat loss in the bulk silicon seed with high thermal conductivity.

As indicated in Fig. 3.20, the slope of the oxide sidewall of the holes is not ideally smooth. There are some corners and the slope of the sidewall also changes. This is

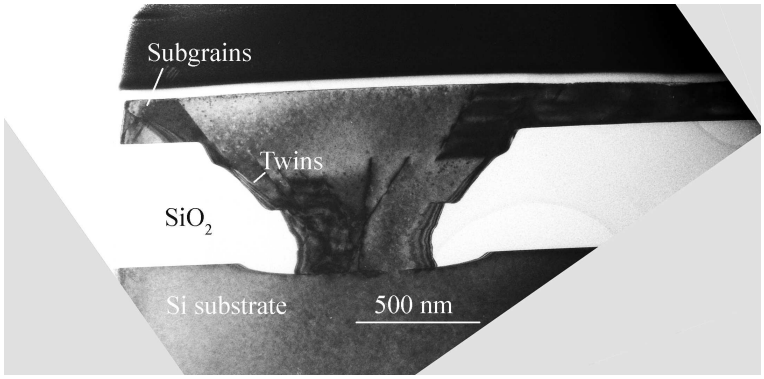


(a)

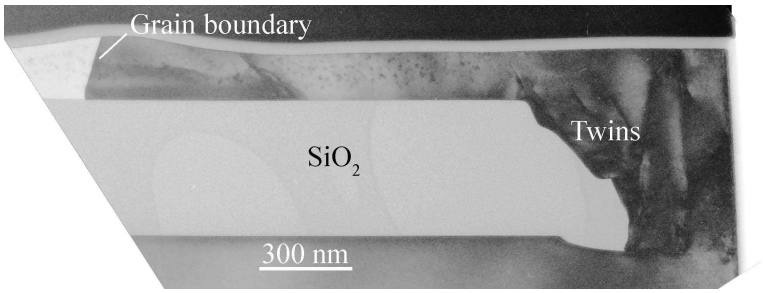


(b)

Figure 3.19: Four secondary subgrains in a large grain grown from (100)-oriented seeds using a dry soft-landing step (method ii), excimer-laser crystallization, and substrate heating up to $450°$C, with a laser fluence of 1400 mJ/cm^2. (a) Top-view image of grains with 4 subgrains: triangles indicate microtwins. The central square is the opening to the seed. (b) Crystallographic orientation relations between the secondary subgrains and the main grain.



(a)



(b)

Figure 3.20: Cross-sectional TEM images of grains grown from $\langle 100 \rangle$-oriented seeds with a dry soft-landing step (etching method (ii)), with substrate heating up to $450°$C. (a) Epitaxial growth and vertical growth from the seed. (b) Lateral growth along the Si/SiO_2 interface.

probably due to the change of etching rate or the change of the degree of anisotropic etching arising from the soft-landing steps.

Figure 3.20(b) shows the lateral growth along the Si/SiO_2 interface. The laterally grown silicon layer is free of planar defects. However, at the end of the lateral growth phase, some twins are generated. The grain boundary at the end of the lateral growth region is almost perpendicular to the Si/SiO_2 interface, which confirms the hypothesis (Section 3.3) that the crystal shape is determined in the lateral growth phase, and the grain boundary is perpendicular to the Si/SiO_2 interface.

The microtwins are generated at the corners of the sidewalls; these boundaries grow vertically and form a subgrain. However, the corners at the sidewalls form a circle, and there are only four subgrains generated.All the secondary subgrains are well aligned with $\langle 110 \rangle$ orientations in Fig. 3.19(b).

These microtwins and the succeeding subgrains are the results of facet formation during growth. Facet and sidewall defect formation during selective epitaxial growth from (001)-oriented silicon has received a great deal of attention [69, 70]. Films grown through oxide windows with $\langle 110 \rangle$-oriented sidewalls (with respect to the underlying (001) silicon layer) feature facets that are adjacent to the sidewall. This region has a high density of microtwins, too. Figure 3.19(a) shows that there are few segments of $\{111\}$ facets for each subgrain, which are aligned with $\{110\}$-oriented sidewalls. Segments of $\{111\}$ facets are not aligned, indicating that these facets are generated at different heights of the oxide sidewall.

Based on the experimental results mentioned above, an atomic model was proposed [71] for facet and sidewall defect formation. During the epitaxial growth phase, atoms that are far from the sidewall can readily bond to the underlying crystal, leading to rapid growth. At the sidewall, however, the lattice is interrupted by the SiO_2 layer. Atoms added at sites that close to the sidewall are singly bonded to their (100) layer. To ensure stability with the underlying lattice, additional atoms must be added. This results in new facets, which give microtwins. $\langle 110 \rangle$ sidewalls easily form $\{111\}$ planar defects, while keeping atomic growth along the $\langle 001 \rangle$ growth directions.

3.4.2 Facet Formation at $\langle 110 \rangle$ Oxide Sidewalls

In Fig. 3.19 four subgrains are seen to grow from the four sides of a square hole that are exactly parallel to the $\langle 110 \rangle$ oxide sidewalls. To confirm that the four secondary subgrains are indeed grown from the $\langle 110 \rangle$ oxide sidewalls, rather than the four sides of the squares, the holes are turned in-plane around the normal direction – [001] with respect to the orientation of the wafer underneath. Figure 3.21 shows the turned holes with different angles from the horizontal direction. [100]-, [210]-, [310]- and [510]-oriented holes are $45°$, $18.43°$, $26.57°$ and $33.69°$ rotated from the horizontal direction [110] along the normal direction [001].

SEM images (Fig. 3.22) indicate that the positions and density of secondary subgrains do not change with the orientation of the hole. The four secondary subgrains are always parallel to $\langle 110 \rangle$, regardless of the orientation of the holes. This indicates that facets and sequential defects are indeed generated at $\langle 110 \rangle$ oxide sidewalls.

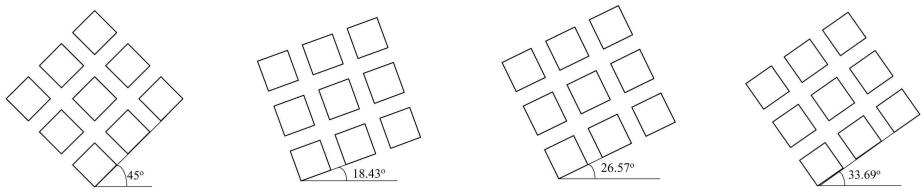


Figure 3.21: Schematic drawing of the orientation of holes opened in the first TEOS layer, with respect to the orientation of the underlying (100)-oriented wafer. (a) [100]-oriented holes; (b) [210]-oriented holes; (c) [310]-oriented holes; and (d) [510]-oriented holes. Holes are normally along the [110] orientation and the horizontal direction.

The hole opened in the oxide layer is circular, which means that there are always four positions on the circle with four $\{110\}$ planes satisfying the conditions for facet generation. By turning the holes in-plane, the length of the oxide sidewall parallel to $\langle 110 \rangle$ is changed – for example, a [110]-oriented hole has a maximum length and a [100]-oriented hole has a minimum length. However, the density of the subgrains does not significantly change with the orientation of the holes, indicating that the density is not sensitive to the length of the $\langle 110 \rangle$ oxide sidewall. On atomic scales, this variation of the length with hole orientation is not significant for facet generation. Once the facets are generated, defects appear during the vertical growth phase.

3.5 Conclusion

In this chapter we discussed the generation of defects in the μ-Czochralski process and investigated different approaches to eliminate them. Applying a capping layer on top of the α-Si film with a grain filter is not enough for reducing the number of defects – but the solidification rate is lowered.

Placing a seed at the bottom of the grain filter is an efficient method for suppressing defect generation in the μ-Czochralski process. With a sufficiently high energy density and substrate heating single-crystalline grains can be prepared at predetermined positions with the same orientation as the seed.

Structural properties of epitaxially grown grains depend strongly on the crystallographic orientation of the seed. The number of defects in (100)-oriented grains is significantly lower than in non-(100)-oriented ones. The generation of defects is related to facet formation during vertical growth through the holes and subsequent lateral growth. Grains of different orientations have specific crystal shapes (Figs. 3.15, 3.16, and 3.17) provided that the spacing of the grain filters is much larger than the grain diameter. (100)-oriented grains are much less likely to change orientation than (111)- and (110)-oriented ones: (111) orientation is easily transformed into $\langle 110 \rangle$ in the normal direction, and (110) orientation into other in-plane orientations.

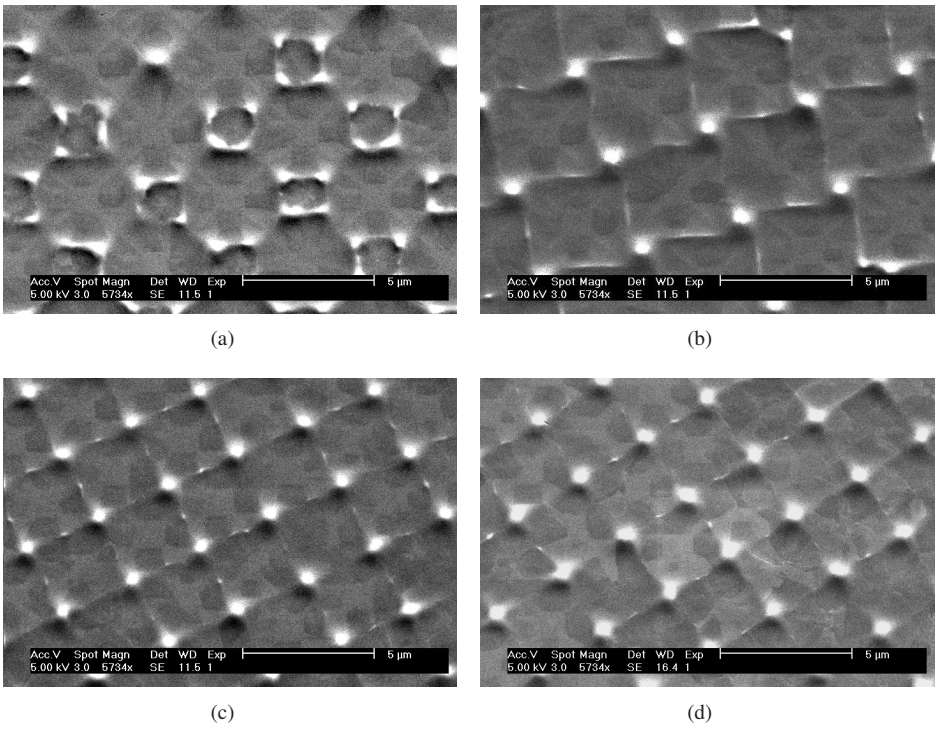


Figure 3.22: SEM images of grains grown from (100)-oriented seeds with a dry soft-landing step [crystallization at 1300 mJ/cm^2 and 450°C], with (a) [100]-, (b) [210]-, (c) [310]-, and (d) [510]-oriented holes. Secondary subgrains (dark regions inside the grains) are generated at identical positions for holes of different orientation.

Defects generated inside (100)-oriented grains were discussed in detail, with regard to the four secondary subgrains (Fig. 3.19). These subgrains are related to four $\{111\}$ facet planes [Fig. 3.15(c)] during the vertical growth phase along the $\langle 100 \rangle$ orientation. Defect generation during epitaxial growth depends on the relative orientation of the oxide sidewall and the seeds. $\langle 110 \rangle$ oxide sidewalls are at the origin of defect generation. By rotating the holes it is confirmed that defects (CSL grain boundaries, subgrains, etc.) are generated on $\langle 110 \rangle$ oxide sidewalls, regardless of the orientation of the holes.

Chapter 4

$\langle 100 \rangle$-Oriented Seeding Layers on Amorphous Insulating Substrates

Chapter 3 dealt with the effects of a seed on defect generation inside location-controlled grains. It was found that the number of defects can be significantly reduced by means of a seeding layer. In the present chapter we shall discuss the possibility of applying $\langle 100 \rangle$-oriented poly-Si layers on insulating SiO_2 films to substitute monocrystalline wafers as seeding layers. This opens the way to the preparation of crystallographic orientation- and location-controlled grains (to be discussed in Chapter 5).

Section 4.1 is concerned with a new method for preparing a seeding layer with a preferred orientation. Using multiple-shot excimer-laser irradiation, a clear preference for $\langle 100 \rangle$ orientation is observed in self-assembled square-shaped poly-Si grains.

In Section 4.2 this orientation preference is confirmed by experiments performed on the Exitech M8000V laser system.

The possible mechanisms leading to orientation preference in poly-Si grains on amorphous insulating SiO_2 layer are discussed in Section 4.3.

4.1 $\langle 100 \rangle$-Oriented Poly-Si Films

Kuriyama et al. [72] reported that poly-Si has a strong $<111>$ fiber texture after multiple-shot excimer-laser crystallization. Recently, Gosain et al. [73] observed a $\langle 100 \rangle$ fiber texture in square-shaped grains after multiple-shot excimer-laser crystallization. In this section we present the processes to obtain preferred $\langle 100 \rangle$ in-plane and $\langle 100 \rangle$ surface orientations in self-assembled square-shaped poly-Si grains by multiple-shot excimer-laser crystallization.

Laser-induced periodic surface structures (LIPSS) are observed; they coexists with

structures featuring crystallographic orientation preference, and could well be the reason for the formation of $\langle 100 \rangle$ texture in self-assembled square-shaped grains.

This poly-Si layer with $\langle 100 \rangle$ texture is used as seeding layer in the preparation of crystallographic orientation- and location-controlled grains.

4.1.1 Materials and Methods

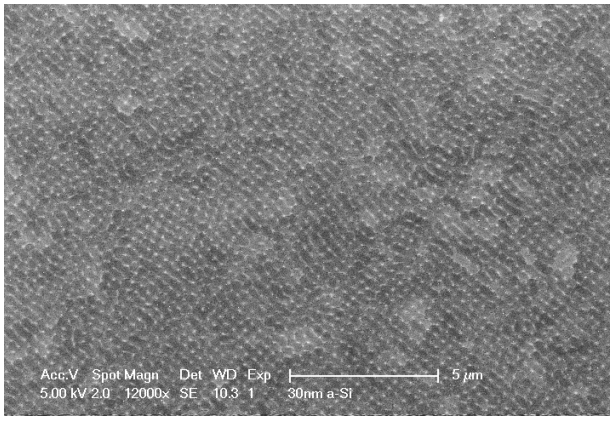
A 30 nm thick α-Si layer is deposited on a thermally oxidized Si wafer (SiO_2 thickness: 1 μm) in a conventional horizontal hot-wall LPCVD reactor using pure silane as source gas at a pressure of 20 Pa and a temperature of $547°C$. The α-Si layer is then irradiated with excimer laser in a vacuum chamber using the XMR 5121 laser system (XeCl laser, λ = 308 nm, FWHM = 50 ns), with an energy density varying from 250 to 280 mJ/cm^2 in 5 mJ/cm^2 steps. This laser energy density is slightly below the superlateral growth (SLG) threshold. The number of shots varies from 100 to 500, with a frequency of 5 Hz. The incident direction makes an angle of about $3°$ with the surface normal. No external heating of the substrate is applied during laser irradiation. A tilted quartz attenuator is placed in the light path to reduce the energy density of the laser and partially polarize the light.

4.1.2 Self-Assembled Square-Shaped Grains

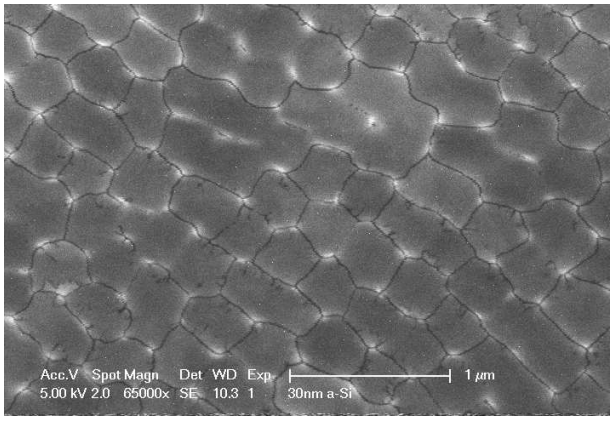
After excimer-laser crystallization and Secco etching, the morphology of grains is investigated by SEM. The images of poly-Si grains are shown in Figure 4.1. It is readily seen that grain boundaries are parallel and show spatial periodicity with a period of about 300 nm. The high-resolution image [Fig. 4.1(b)] clearly shows that grains are nearly square shaped, with a grain size of 300 nm, which is almost the same as the wavelength of the excimer laser. The periodicity is found to be independent of the number of shots. These characteristics indicate a very close connection to LIPSS. Kaki and Horita [74] reported the creation of periodic grain boundaries during multiple-shot solid-state laser crystallization of an α-Si layer with linearly polarized light. Although excimer laser light is known to have a minor degree of polarization, in our experimental setup the tilted quartz attenuator partially polarizes the light.

The LIPSS has been confirmed by AFM analysis. Figure 4.2 shows the AFM image of a 5×5 μm^2 area of poly-Si grains. Neighboring grains form hillocks and grain boundaries between them. Periodic grain boundaries are aligned along a line, with a uniform spacing of about 300 nm. Square-shaped grains are self-assembled, forming a hillock at each corner of the square. The root-mean-square (rms) roughness of the surface is 15 nm, which is of the same order as for poly-Si crystallized by nonpolarized laser light.

Periodic surface structure (hillock-valley-hillock-valley...) is observed not only in the direction perpendicular to the LIPSS direction but also parallel to it. Figure 4.2 shows that square-shaped grains are self-assembled and form a hillock at each corner of the square, i.e., four hillocks mark each square-shaped grain.



(a)



(b)

Figure 4.1: SEM images of poly-Si grains crystallized at 260 mJ/cm^2 after 500 shots. (a) Periodic grain boundaries; (b) self-assembled square-shaped grains.

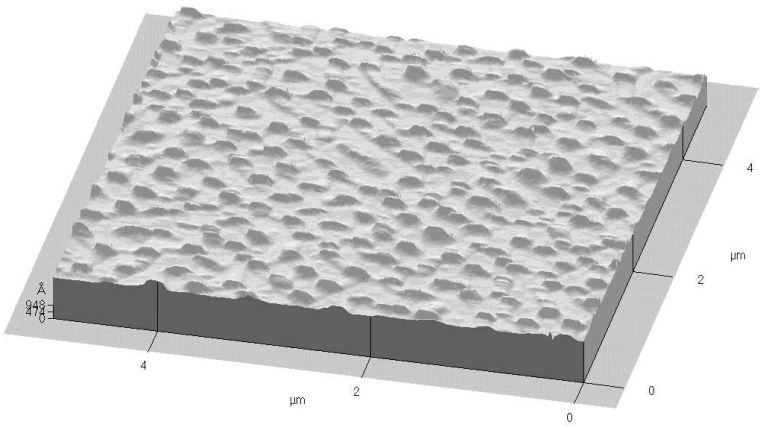
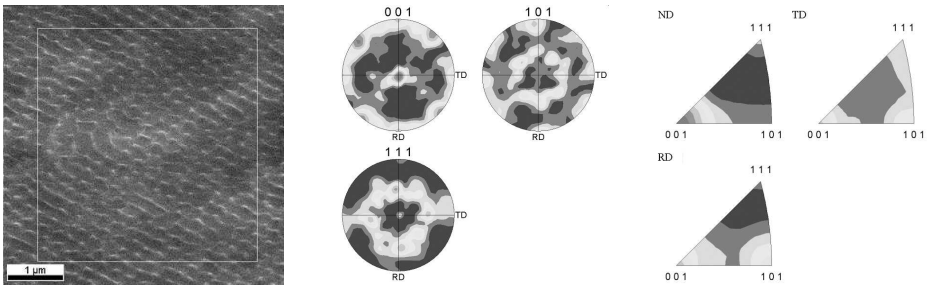


Figure 4.2: AFM image of poly-Si grains crystallized at 260 mJ/cm^2 after 500 shots.

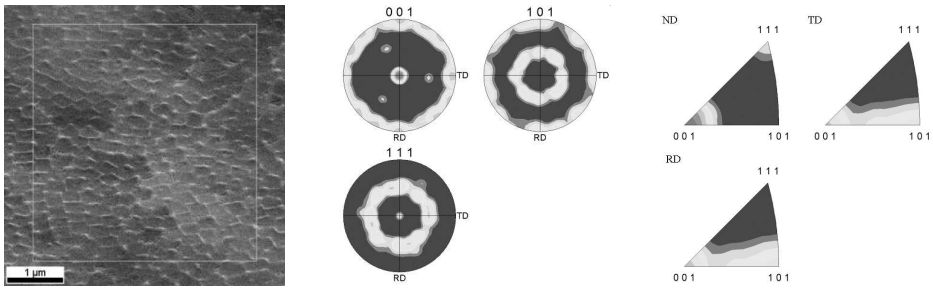
4.1.3 Surface Orientation and In-Plane Orientation

Figure 4.3 shows the pole figures and inverse-pole figures of poly-Si grains, analyzed by EBSD using an automatic mapping method. Figure 4.3(a) shows the EBSD-mapped area, where the square-shaped grains are well aligned. The clear preference for <100> texture is visible not only in the surface orientation [Fig. 4.3(c)] but also in the in-plane orientations [Fig. 4.3(b)]. It is the first time this preferred in-plane orientation has been achieved for the lateral growth of Si grains. Furthermore, the preferred in-plane <100> orientation is either parallel or perpendicular to the LIPSS direction, i.e., always perpendicular to the sides of the square. The prominent texture component is $\{001\}\langle 110\rangle$.



(a) (b) (c)

Figure 4.3: Texture of poly-Si grains, crystallized at 260 mJ/cm^2 after 500 shots. (a) SEM image of poly-Si; the rectangle shows the mapping area. (b) $\langle 100\rangle$, $\langle 111\rangle$ and $\langle 110\rangle$ pole figures of the mapped area. (c) Inverse-pole figures in the normal direction (ND), rolling direction (RD), and transverse direction (TD).



(a) (b) (c)

Figure 4.4: Texture of poly-Si grains, crystallized at 280 mJ/cm^2 after 500 shots. (a) SEM image of poly-Si; the rectangle shows the mapping area. The grain boundaries are facets, forming zigzag lines. (b) Pole figure of the mapped area. (c) Inverse pole figures in the ND, RD, and TD.

The well-aligned LIPSS is a result from the self-assembly process of square-shaped grains with well-aligned grain boundaries. These grain boundaries tend to be faceted, forming zigzag-shaped grain boundaries. When the periodic grain boundaries are faceted [Fig. 4.4(a)], a weak in-plane orientation preference is exhibited by these square-shaped grains [Figs. 4.4(b) and 4.4(c)]. However, there is a clear preference for ⟨100⟩ in the surface orientation.

The strongly textured and self-assembled square-shaped grains mentioned above are obtained in a relatively wide laser energy density window. This window is plotted in Fig. 4.5. For a fixed number of pulses its width is approximately 10 mJ/cm^2. At lower energy densities or shot numbers no LIPSS emerges. On the other hand, agglomeration or ablation of the film occurs above the window.

4.1.4 LIPSS Formation and Square-Shaped Grains

LIPSS formation on the surface of semiconductors (Si and Ge) and metals (Al and Cu) was thoroughly investigated in [75]. A spatially periodic temperature profile, arising from the interference of the incoming or refracted laser beam and the light scattered by the surface was proposed to be the cause of LIPSS formation [76]. Furthermore, at low fluence, LIPSS can be produced via the solidification of periodically and locally molten strips, as confirmed by time-resolved diffraction measurements [77]. The mechanisms of LIPSS formation are discussed in the literature [78, 79]. Below we shall focus on the formation of square-shaped grains, assuming that LIPSS has already formed.

The energy density applied in the experiment is slightly below the threshold for the uniform melting of the Si layer; therefore a periodic local melting could be at the origin of LIPSS formation. Figure 4.6 is a schematic sketch of the pulse-to-pulse alternation of the melting and solidification directions during the process leading to LIPSS. After the $(n-1)$th shot, periodic grain boundaries are formed at positions $m\lambda$ (m is an integer).

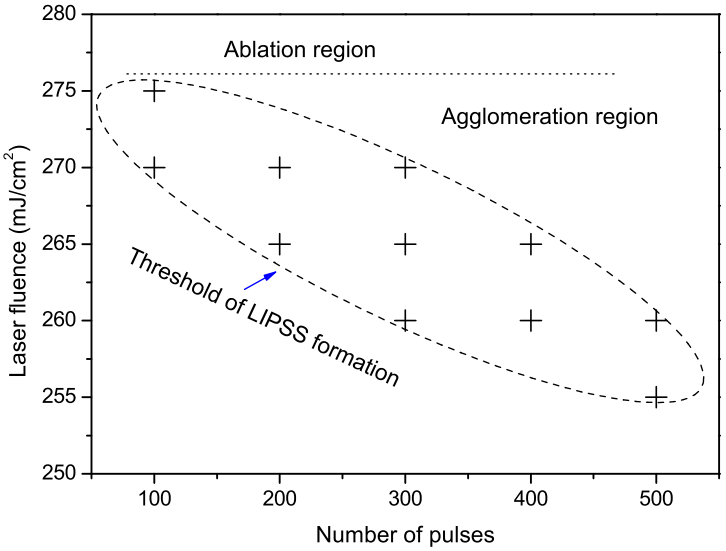


Figure 4.5: Energy density window for obtaining textured self-assembled poly-Si grains. Crosses indicate experimental points where textured self-assembled poly-Si grains were obtained. The dashed ellipse indicates the laser energy density window, taking into account the number of shots. The dotted line separates the ablation region from the agglomeration region.

In the nth shot, temperatures are higher in the valleys of the LIPSS than at the hillocks because of the preferential energy accumulation of laser light in valleys [80, 81] and the relatively thick Si layer at the hillocks. The modulated temperature profile is out of phase with the preformed LIPSS. Melting starts in the valley and advances toward the hillocks; it stops midway between the valleys leaving some Si unmolten. Solidification starts from these unmolten Si nuclei, and propagates in the opposite direction of melting. It then forms hillocks (grain boundaries) at positions $(m + 1/2)\lambda$ due to the collision of two solidification fronts. That is, the location of the grain boundary changes from shot to shot. Similarly, after the $(n + 1)$th shot grain boundaries return to the original positions $m\lambda$. Consequently, the grain boundary moves forward and backward in the directions normal to the LIPSS with successive shots. As a result, the poly-Si layer is a self-assembled structure of square-shaped grains arising from hundreds of melting-solidification cycles.

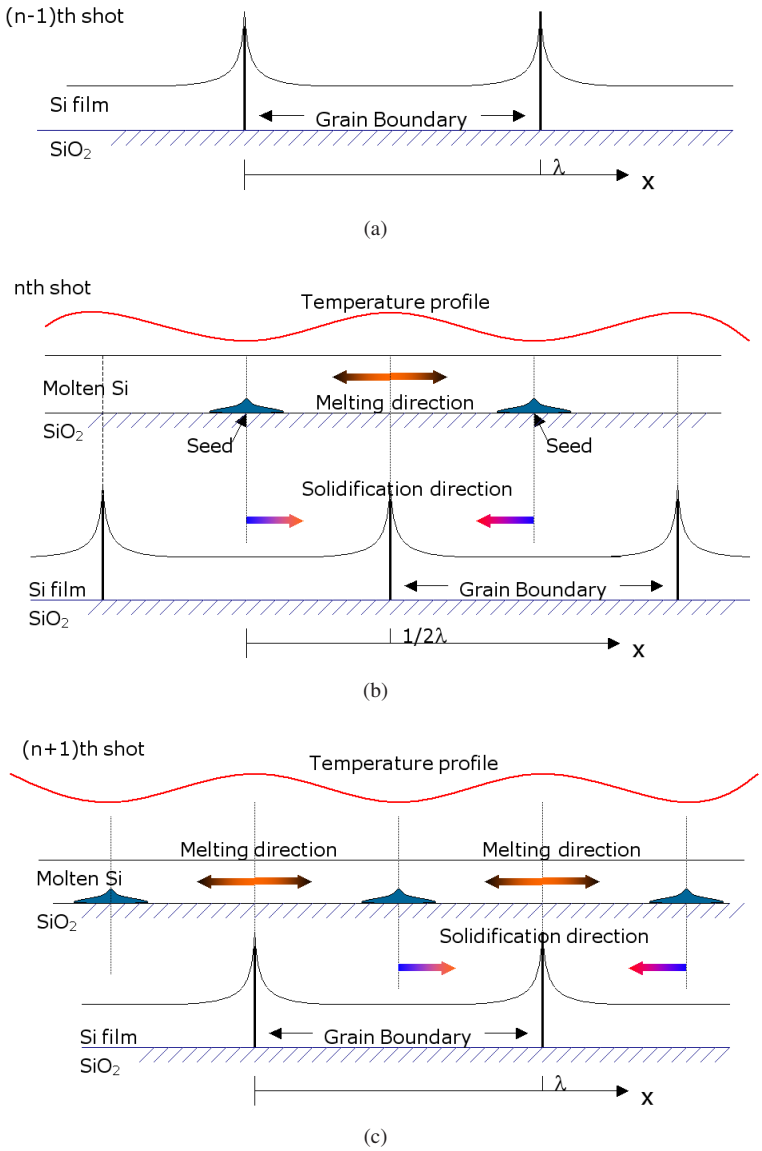
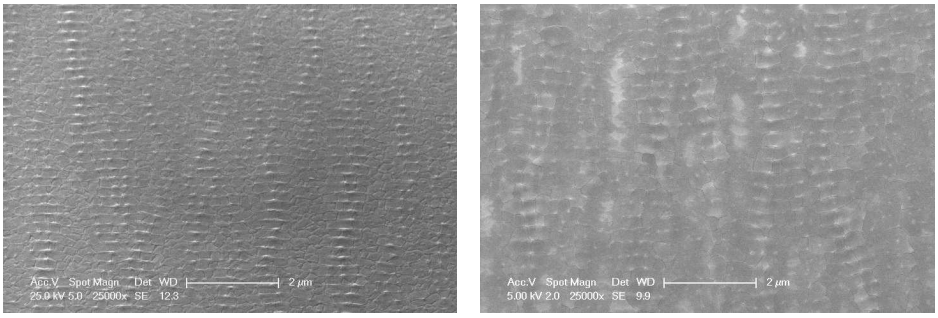


Figure 4.6: Schematic geometry of the periodic melting-solidification cycle, showing the alternation of the solidification direction and of the grain boundaries after the formation of the LIPSS. (a) After the $(n-1)$th shot the grain boundaries are at $m\lambda$ (m and n are integers). (b) After the nth shot the melting starts at $(m+1/2)\lambda$ due to the preferential accumulation of laser energy in the valleys, leaving some unmolten Si at $m\lambda$. The solidification of molten Si creates new grain boundaries at $(m+1/2)\lambda$. (c) After the $(n+1)$th shot the grain boundaries return to $m\lambda$.

4.2 $\langle 100 \rangle$-Oriented Seeding Layer with the Exitech Laser System

The experiments presented in Section 4.1 are repeated using another laser system (Exitech M8000V). The same materials and methods are used as in Section 4.1.1, only the parameters of the excimer-laser irradiation are different.

The periodic grain boundaries and square-shaped poly-Si grains, obtained after multiple-shot excimer-laser irradiation, are clearly seen on the SEM images in Fig. 4.7. The LIPSS has the same morphology as in Fig. 4.1 except for the orientation of the periodic grain boundaries. The LIPSS direction is determined by the polarization of the excimer-laser light. The relative orientation of the polarized light with respect to the sample reference is different for the two laser systems.



(a) (b)

Figure 4.7: SEM images of poly-Si grains crystallized at 280 mJ/cm^2 after 500 shots. (a) Periodic grain boundaries; (b) high-resolution image of the periodic grain boundaries.

The white stripes in Fig. 4.7(b) are caused by ablation during excimer-laser irradiation.

Figure 4.8 shows the microtexture of poly-Si grains obtained by EBSD analysis. The inverse-pole figures of the normal direction (ND) indicate a clear preference for $\langle 100 \rangle$ in poly-Si grains with LIPSS. A weak in-plane preference is observed in the $\langle 100 \rangle$ pole figure.

4.3 The Mechanisms Behind Orientation Preference

$\langle 100 \rangle$ fiber texture is observed in square-shaped poly-Si grains obtained from α-Si precursors with multiple-shot excimer-laser irradiation [73]. However, no in-plane orientation preference is seen in this case. The $\langle 100 \rangle$ fiber texture is explained in terms of the anisotropy of the melting temperature. It was argued that the melting temperature is higher for $<100>$-oriented grains than for other – for example, $\langle 111 \rangle$ – orientations, and

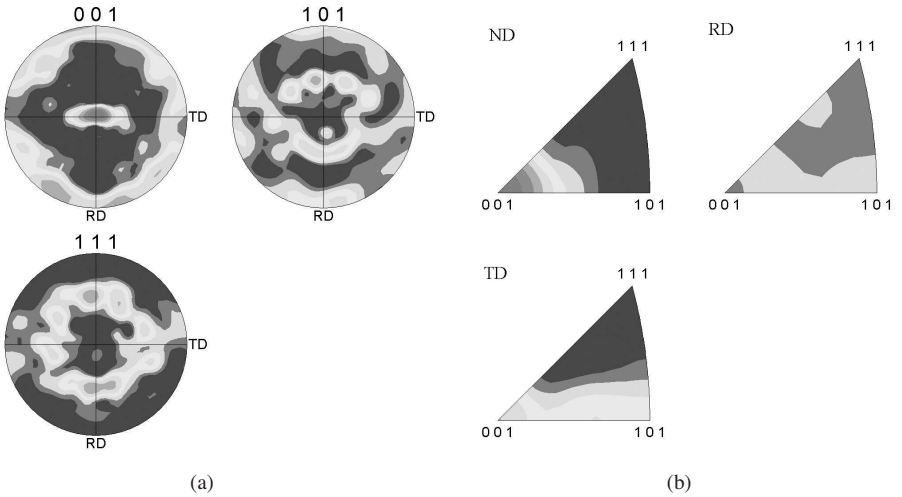


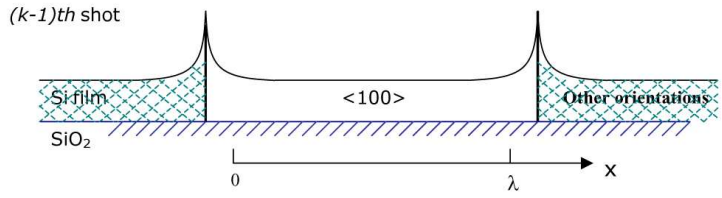
Figure 4.8: Microtexture of poly-Si grains, crystallized at 280 mJ/cm^2 after 500 shots. (a) Pole figures for $\langle 100 \rangle$, $\langle 110 \rangle$, and $\langle 111 \rangle$ orientations. (b) Inverse-pole figures of ND, RD and TD.

they can coexist with molten Si, which would explain why new solidified poly-Si grains show a preference for the $\langle 100 \rangle$ orientation. However, the difference of the melting temperatures is negligibly small: about 10^{-2} K for a 0.5 μm thick film. The heat conductivity of solid or molten Si is therefore sufficiently high to suppress the small difference at the melting temperature. In this study the $\langle 100 \rangle$ texture can be obtained in a relatively wide energy-density window. Furthermore, the coexistence of liquid and solid Si is reported to be stable only when the Si has contacts with oxide on both sides [82].

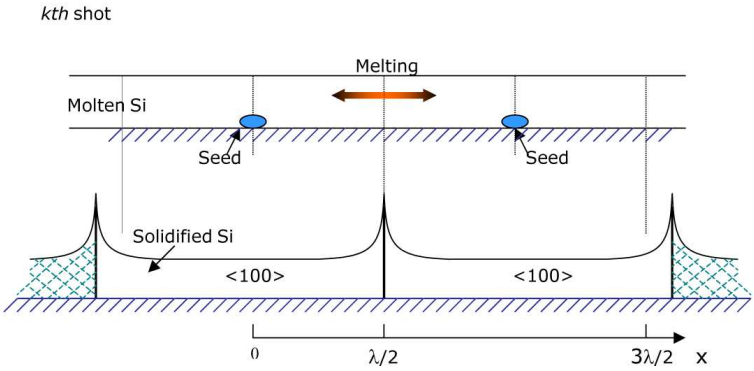
Another possible explanation for the orientation preference is the anisotropy of surface free energy [72] of the strong $\langle 111 \rangle$ texture obtained by multiple-shot excimer-laser crystallization. It was argued that the energy of the Si/SiO_2 interface is minimized by a $\langle 100 \rangle$ texture, while the free energy of the Si surface is minimized by a $\langle 111 \rangle$ texture. The free energy of the Si surface is larger than that of the Si/SiO_2 interface. Therefore, $\langle 111 \rangle$ texture is easily developed with multiple-shot excimer-laser crystallization.

However, this anisotropy of the melting temperature is caused by – and calculated from – the anisotropy of the surface free energy [73, 82]. Thus, by the same token, it could be possible to obtain either $\langle 111 \rangle$ or $\langle 100 \rangle$ texture after multiple-shot excimer-laser crystallization.

We propose that the strong preference for the $\langle 100 \rangle$ orientation may arise from the alternation of the solidification direction. The AFM image (Fig. 4.2) shows that there are hillocks at the four corners of each square-shaped grain. Figure 4.6 only indicates the alternation of the solidification direction perpendicular to the LIPSS. The same alternation may also occur parallel to the LIPSS due to periodic hill-valley structure in this



(a)



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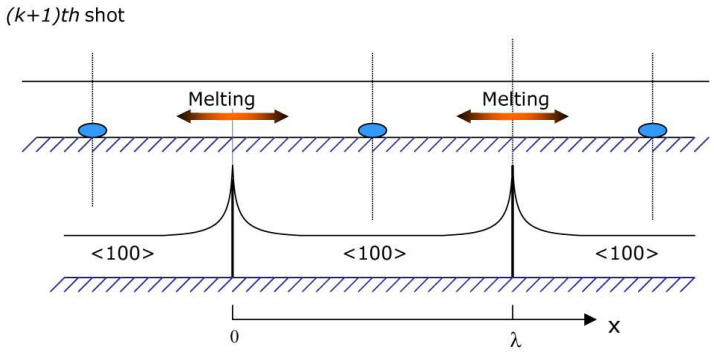


(c)

Figure 4.9: Schematic representation of the development of the <100> texture through three successive shots during LIPSS formation. After the $(k-1)$th shot a <100>-oriented grain grows largest. After the kth shot two seeds survive the melting phase, hence the length of the <100> direction is doubled. After the $(k+1)$th shot three seeds are present, so the length of the <100> direction is tripled.

direction. To satisfy this condition, the melting-solidification cycle requires the fourfold in-plane symmetry of the lateral growth direction, i.e, the bipolarity of the directions perpendicular and parallel to the LIPSS. Only the $\langle 100 \rangle$ orientation satisfies this symmetry condition.

We suggest that the growth rate for a fixed undercooling is the lagest along the $\langle 100 \rangle$ direction, in analogy with the dendrite growth direction for cubic metals [44]. As indicated in Fig. 4.5, the LIPSS is not well developed up to a certain number of shots for each proper energy level. The texture is developed in the course of LIPSS formation.

Figure 4.9 shows a schematic representation for the development of the $\langle 100 \rangle$ texture during LIPSS formation. After the $(k-1)$th shot the crystallographic orientation of grains is random. A grain with a $\langle 100 \rangle$ surface orientation and a $\langle 100 \rangle$ direction perpendicular to the LIPSS can grow largest because growth is fastest along these orientations. The grain boundary is formed beyond $\lambda/2$ as the $\langle 100 \rangle$-oriented grain grows fastest. Grains with other orientations cannot grow beyond $\lambda/2$. After the next, kth, shot melting starts in the valley ($\lambda/2$); then the hillocks also melt because they are located near the hot valleys. Melting stops about midway between the valleys, leaving the Si at 0 and λ unmolten. These two unmolten bits are single crystals, and act as $\langle 100 \rangle$-oriented seeds during solidification. During solidification two large grains are formed, and the length of $\langle 100 \rangle$ surface-oriented crystals is doubled. It should be noted that the length of the $\langle 100 \rangle$ orientation also increases in the direction parallel to the LIPSS. After the next, $(k+1)$th, shot, three $\langle 100 \rangle$-oriented seeds are formed at $\pm\lambda/2$ and $3\lambda/2$. While the seeds at $-\lambda/2$ and $3\lambda/2$ are single-crystalline, the one at $+\lambda/2$ may contain two grains. However, since these two grains originate from the same grain, they are crystallographically merged at a high temperature, and eventually form a single crystal. When the melting-solidification cycle is repeated, the preference for the $\langle 100 \rangle$ orientation propagates to the outside, while other orientations are occluded by the growth of $\langle 100 \rangle$-oriented grains. With hundreds of the melting-solidification cycles, the preferred in-plane $\langle 100 \rangle$ directions are perpendicular and parallel to the LIPSS direction.

The model presented in Fig. 4.9 can explain not only the preferred surface orientation but also the preferred in-plane orientation. LIPSS coexists with the 3D texture, and could be the origin of 3D orientation preference.

Figure 4.9 shows the texture development along the vertical direction, which is perpendicular to the LIPSS direction. Figure 4.10 shows a top view of the texture developing in 2 dimensions – i.e., including the direction parallel to the LIPSS. The $\langle 100 \rangle$-oriented grain with the in-plane arrangement shown in the Fig. 4.10(a) can become the largest because of its fast growth rate. $\langle 100 \rangle$ grains are multiplied, and other grains are occluded for the same reason as in the one-dimensional case (Fig. 4.9). In the end all $\langle 100 \rangle$-oriented grains have the same growth rate. When two solidification fronts meet in the LIPSS direction or perpendicular to it, solidification continues in the perpendicular direction to fill the area with square-shaped grains.

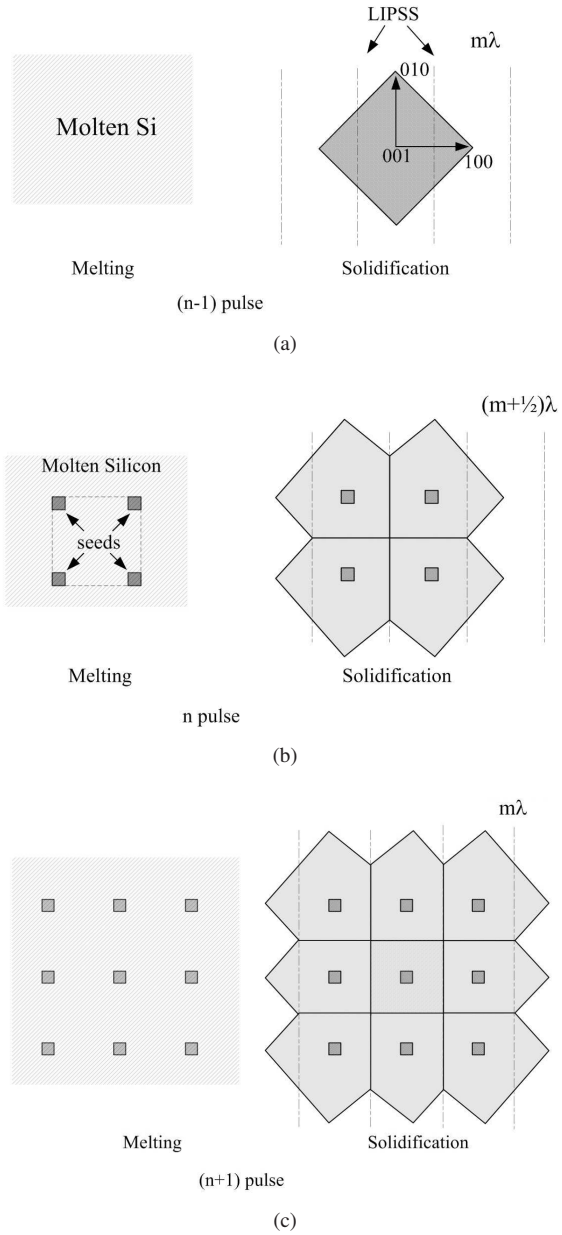


Figure 4.10: Schematic representation of the 2D development of the $\langle 100 \rangle$ texture through three successive shots. After the $(n-1)$th shot there is one grain with $\langle 100 \rangle$ orientation. After the nth shot four seeds at the four corners survive the melting phase, hence after solidification the number of $\langle 100 \rangle$-oriented grains is multiplied by four. After the $(n+1)$th shot even more seeds are formed, raising the number of $\langle 100 \rangle$-oriented grains to nine.

4.4 Conclusion

In this chapter we proposed a new method for the preparation of poly-Si films with $\langle 100 \rangle$ orientation preference. By multiple-shot excimer-laser crystallization, strongly $\langle 100 \rangle$-textured self-assembled square-shaped poly-Si grains can be prepared from 30 nm thick α-Si precursors.

The strong texture coexists with the LIPSS, and can be obtained in a relatively wide energy density window. The $\langle 100 \rangle$ orientation is speculated to have the largest growth rate. During LIPSS formation, in-plane directions of solidification (perpendicular and parallel to the LIPSS) require fourfold in-plane symmetry. This requirement is met by the $\langle 100 \rangle$ orientation, which is therefore selected while others are occluded.

Owing to the smallest effective mass and lowest number of interface electronic trap states, $\langle 100 \rangle$ is the most desirable crystallographic orientation on insulating SiO_2 layers for manufacturing CMOS integrated circuits (ICs).

It was demonstrated in Chapter 3 that structural and electronic properties of epitaxially grown films depend strongly on the crystallographic orientation of the Si substrate. The number of extended defects – i.e., CSL grain boundaries, dislocations, and stacking faults – is significantly lower in $\langle 100 \rangle$-oriented films than in non-$\langle 100 \rangle$-oriented ones.

In Chapter 5 we shall discuss the application of the $\langle 100 \rangle$-textured film (presented above) as seeding layer, combined with location control, to prepare orientation- and location-controlled grains for the fabrication of TFTs and 3D ICs. The $\langle 100 \rangle$-textured poly-Si film can be directly used for TFT fabrication, leading to improved TFT characteristics.

Chapter 5

Crystallographic Orientation- and Location-Controlled Grains

This chapter deals with a new method for preparing orientation- and location-controlled grains.

Control over the crystallographic orientation of single grains – i.e., fabrication of grains with some preferred orientation, e.g., $\langle 100 \rangle$ – would lead to an improvement of the performance and uniformity of SG-TFTs.

In this approach, poly-Si films with square-shaped grains of $\langle 100 \rangle$ orientation preference are used as seeding layers. The methods for preparing the seeding layer is discussed in Chapter 4.

Localization control is achieved through selective epitaxial growth from a seeding layer – a method that was discussed and optimized in Chapter 3.

To understand heat transfer during excimer-laser crystallization and to find a suitable process window, thermal effects and phase transformations during excimer-laser irradiation are simulated using the axisymmetric finite-element method.

5.1 Conceptual Ideas of Orientation- and Location-Controlled Grains with a Seeding Layer

Apart from the details of the seeding layer, the preparation of orientation- and location-controlled grains is based on the ideas of Chapter 3 (Fig. 3.3). In Chapter 3 a bulk silicon wafer (or SOI wafer) was used as seeding layer. In the present chapter a poly-Si film with a preferred orientation on top of an insulating SiO_2 layer is used instead. Figure 5.1 shows the general concept of the configuration to prepare crystallographic orientation- and location-controlled grains.

Using excimer-laser irradiation, the melt front of α-Si reaches the seeding layer. The subsequent solidification of liquid silicon (epitaxial growth) starts from the seeding layer.

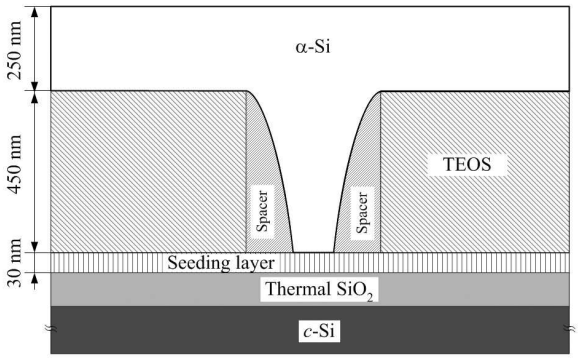


Figure 5.1: Schematic cross-sectional view of stacked layers for crystallographic orientation and location control. The α-Si layer is applied directly on a TEOS oxide layer, with an opening to the seeding layer that has a $\langle 100 \rangle$ texture.

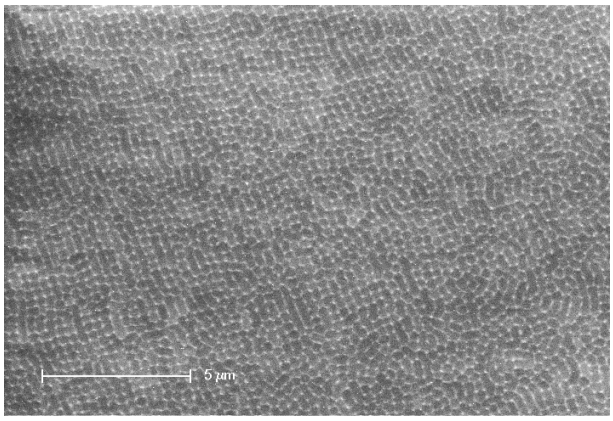
The preparation of crystallographic orientation- and location-controlled grains can be based on this configuration.

The seeding layer used in this chapter is a poly-Si film with a preferred $\langle 100 \rangle$ orientation (for details, see Chapter 4). The seeding layer is checked with SEM and EBSD. Figure 5.2 shows the morphology of poly-Si grains.

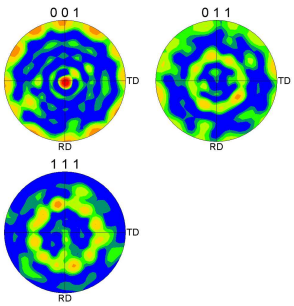
Figure 5.2(b) shows the $\langle 100 \rangle$, $\langle 110 \rangle$, and $\langle 111 \rangle$ pole figures. The (100) pole figure indicates a clear $\langle 100 \rangle$ preference in the normal direction and a $\langle 100 \rangle$ preference in the equatorial plane (i.e., for in-plane orientations). Inverse-pole figures [Fig. 5.2(c)] indicate a clear orientation preference in the normal direction.

92% of grains feature $\langle 100 \rangle$ texture within 10 degree to the exact surface normal.

Note that the location of the grain boundaries of poly-Si grains (or of the grains themselves) is not controlled by the seeding layer. The grain size is about 300 nm, while the window (opening to the seeding layer) is about 600 nm. This means that there is always some probability to have random grain boundaries in the window area. Multiple grains in the window either merge (on account of their small relative misorientation), or occlude each other during vertical growth. To avoid grain boundaries in the final grains, the opening to the seeding layer should be sufficiently small.



(a)



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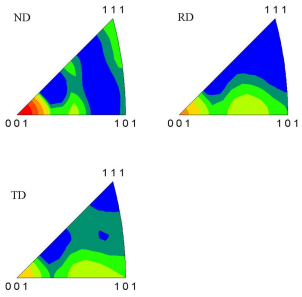


(c)

Figure 5.2: The seeding layer used in the preparation of orientation- and location-controlled grains: (a) self-assembled square-shaped grains, crystallized from 30 nm thick α-Si film at 265 mJ/cm^2 with 500 shots; (b) contour-pole figures; (c) contour-inverse-pole figures calculated from EBSD mapping, indicating a clear $\langle 100 \rangle$ preference.

5.2 Transient Heat-Transfer Simulations for Epitaxial Growth from the Seeding Layer

5.2.1 Configuration for Simulation

Since the seeding layer (SL) is thin, the melt front should reach the α-Si/SL interface, and should not melt the entire SL. For a 30 nm thick SL, the process window, which is critical for orientation control, should be very narrow.

To investigate epitaxial growth and to find a suitable process window, transient heat transfer and phase transformation during excimer-laser irradiation and subsequential solidification are simulated using the finite-element method (FEM) (see page 24).

Simulations are carried out on a three-dimensional mesh using axisymmetric configurations (Fig. 5.3). The elements of the mesh are axisymmetric triangles and quadrilaterals. The bottom of the thermal SiO_2 layer is simulated by semi-infinite axisymmetric elements. The configuration of the stacked layers along the symmetry axis is: α-Si (250 nm), SL (30 nm), thermal SiO_2 layer (semi-infinite). The excimer laser specifies the boundary condition at the surface of the α-Si film. The second boundary condition is the fixed temperature at the bottom of the thermal oxide layer ($450°$C). The initial temperature is $450°$C everywhere.

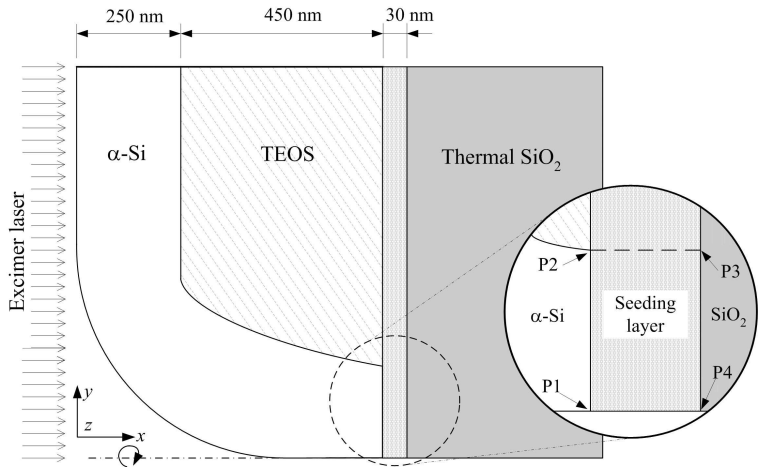


Figure 5.3: Schematic diagram of the axisymmetric configuration for simulating epitaxial growth from the seeding layer. The symmetry axis is along the x-direction. Points of special importance, P1, P2, P3, and P4, are marked in the inset image.

To ensure epitaxial growth from the seeding layer, the melt front must reach the seeding layer; at the same time, the entire seeding layer should not become molten. The four points (P1, P2, P3, P4) marked in the inset image of Fig. 5.3 play an important role in determining the suitable energy density window for excimer-laser irradiation. P3 is the

projection of P2 on the bottom of the seeding layer along the x-direction. The process window therefore ranges between the melting-energy densities of P1 and P3.

Even if melting continues beyond P3 in Figs. 5.1 and Fig. 5.3, epitaxial growth from the side (i.e., lateral growth from the seeding layer) is still possible. For convenience, P3 is defined as the limit of the seeding layer in this simulation. In future investigations, the seeding layer could be patterned into, for example, seeding islands in the window to reduce electrical capacitance between the two silicon layers.

5.2.2 Process Window and Melt Front

Finding a suitable process window requires the simulation of how the process depends on the energy density of the excimer laser. The lower limit for the onset of epitaxial growth is defined as the laser fluence at which α-Si melts down to the seeding layer (α-Si/SL interface), while the upper limit is the energy density at which the entire seeding layer (the SL/SiO_2 interface) in the window melts. The process window is the difference between the upper limit and the lower limit.

At a pulse duration of 25 ns, the lower limit of laser fluence where the melt front reaches point P1 is found to be at 855 mJ/cm^2, while the upper limit is at 935 mJ/cm^2. The process window is thus 80 mJ/cm^2. Figure 5.4 shows the history plots for the 4 points (P1, P2, P3, P4). Figure 5.4 also shows that the melt front first reaches P1, then P4, and then advances laterally to P2 and P3.

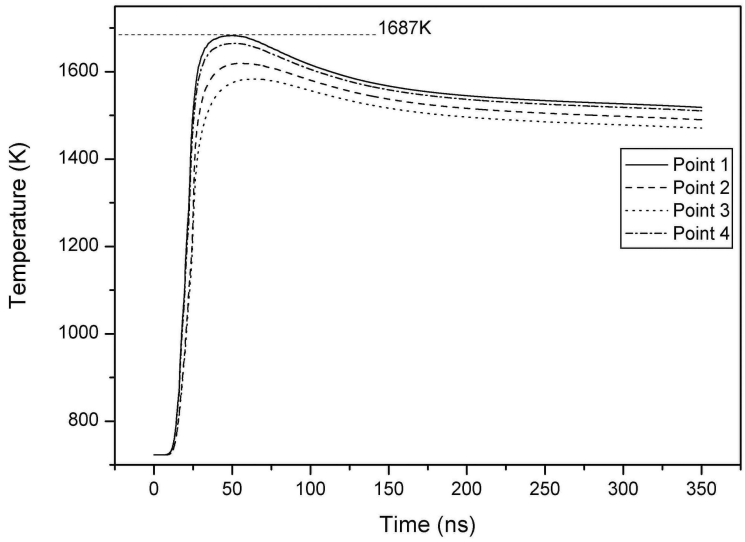
As Fig. 5.4 shows, the time required for each point to reach its maximum temperature is larger than the pulse duration of the excimer laser ($t_{\text{max. temp.}} > 25$ ns), where t is the time measured from the start of the laser irradiation. In other words, the melt front reaches the seeding layer only after excimer-laser irradiation. Figure 5.5 shows the path plot along the symmetry axis (x-direction). By the end of laser irradiation ($t = 25$ ns), the melt front reaches a depth of 163 nm. After laser irradiation, the heat stored in the molten pool and in the α-Si layer is transferred to the silicon layer underneath, heating up the silicon to its melting point. The seeding layer then melts because of the absorbed heat.

5.2.3 Effects of Pulse Duration on the Process Window

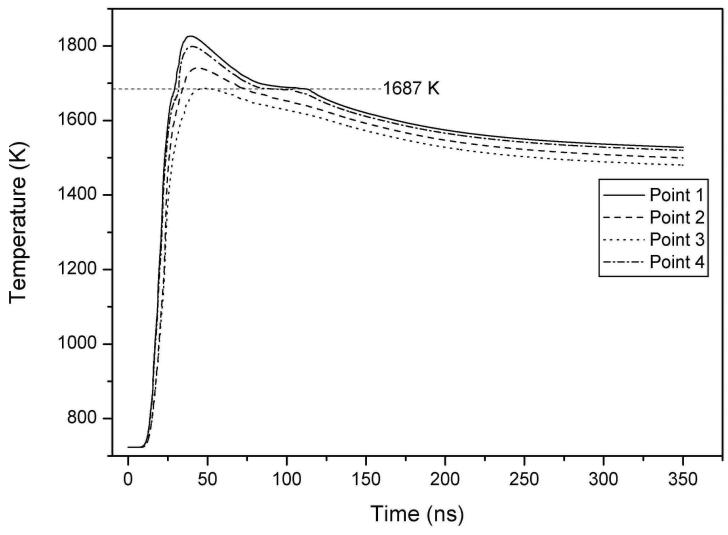
The duration of the laser pulse of the Exitech M8000V system (page 17) can be extended by means of a pulse extender. In the present simulations different pulse durations are used in order to identify the effects of pulse duration on the process window.

In addition to the system's native pulse duration of 25 ns, 50, 100, 200 and 500 ns pulses are also used. Table 5.1 summarizes the simulation results for the lower/upper limit of laser fluence and the process window.

With a long pulse duration, higher laser fluence is required to melt the α-Si down to the seeding layer (the α-Si/SL interface) [83], as the amount of heat transferred to the substrate is larger on account of the longer pulse duration. To melt α-Si down to the seeding layer, higher laser fluence is then required [83].



(a)



(b)

Figure 5.4: History plots of the temperature profiles at P1, P2, P3, and P4. The laser fluence is (a) 855 mJ/cm^2, and (b) 935 mJ/cm^2; the pulse duration is 25 ns. The origin is at the start of excimer-laser irradiation.

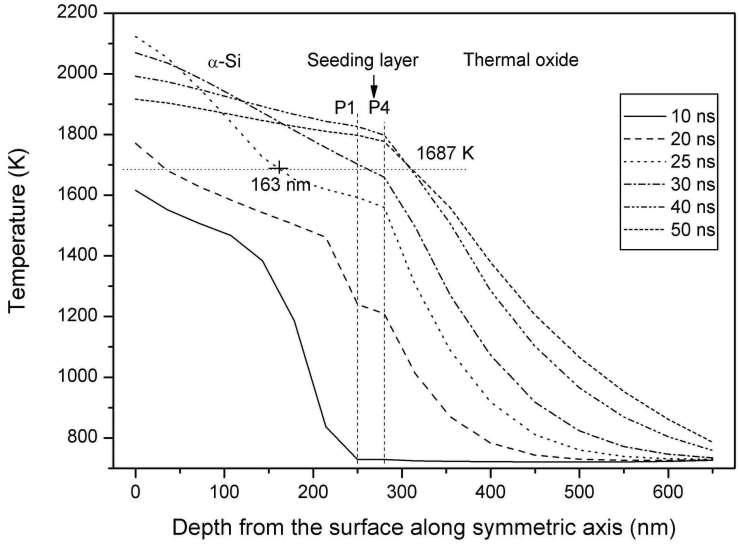


Figure 5.5: Path plots along the symmetry axis through the α-Si layer, seeding layer, and thermal oxide layer. The origin is at the surface of α-Si. The region between P1 and P4 (denoted by two dashed lines) is the seeding layer.

For long pulse durations the process window is very narrow. The temperature difference between points P1 and P3 is small due to the long heating time of the substrate (thermal oxide). For a 500 ns pulse, the process window is 35 mJ/cm^2. Since temporal variations in the output of the laser system are approximately 10%, the process window is extremely narrow for long pulses. This indicates that it would be hardly possible to control the melt depth by changing the laser fluence.

To summarize, selective epitaxial growth from a thin seeding layer requires short rather than long pulses.

5.3 Crystallographic Orientation- and Location-Controlled Grains

5.3.1 Materials and Methods

After the preparation of the seeding layer (Section 4.1), TEOS oxide is deposited on top of it by the decomposition of the TEOS precursor at a temperature of 350°C in a PECVD reactor.

Contact holes to the seeding layer are opened in the TEOS oxide layer by RIE dry etching in a C_2F_6-CHF_3 plasma with a wet soft-landing step. Then a second TEOS oxide layer is deposited by PECVD, and a second anisotropic etching step is carried out

Table 5.1: Effects of pulse duration of the process window

Pulse Duration [ns]	Lower limit of laser fluence [mJ/cm^2]	Upper limit of laser fluence [mJ/cm^2]	Process window [mJ/cm^2]
25	855	935	80
50	890	950	60
100	930	985	55
200	1020	1065	55
500	1280	1315	35

to remove the second TEOS layer completely – except for the oxide on the sidewalls of the first layer in order to form an oxide sidewall spacer. The second back-etching phase also ends in a wet soft-landing step. The purpose of this last step is to avoid over-etching of the seeding layer by RIE dry etching. This procedure for opening a window to the seeding layer is the same as discussed in Chapter 3.2.

The wafer is then dipped into 0.5% HF solution for 4 minutes to remove its native oxide, and immediately afterwards a 250 nm thick α-Si film is deposited in a conventional horizontal hot-wall LPCVD furnace using pure silane as source gas.

Fig. 5.1 shows the final configuration used for preparing crystallographic orientation- and location-controlled grains.

The α-Si film is crystallized with a single pulse of excimer-laser light (Exitech M8000V system) at a substrate temperature of 450°C. For reference purposes the α-Si film is also crystalized without substrate heating. To ensure a better process control, the pulse-duration extender is not used (i.e., the pulse duration remains 23 ns) (Fig. 5.6). The energy density varies from 900 to 1200 mJ/cm^2.

Excimer-laser crystallization is followed by Secco etching, and the crystallized films are then observed by SEM. The microtexture and grain-boundary components are analyzed by EBSD.

5.3.2 Grains Crystallized at Room Temperature

Grains grown from the seeding layer and crystallized at room temperature (without substrate heating) have similar morphology to grains grown from bulk wafers and crystallized at room temperature (Fig. 3.8). Grains produced using a low laser fluence [Fig. 5.7(a)] have cavities at their centers. They are absent when high laser fluence is used on account of the higher mobility of molten silicon. The critical energy density, where cavities disappear, is 1080 mJ/cm^2.

Clear cracks are observed in grains crystallized without substrate heating (Fig. 5.7). The length of these cracks is much larger than the grain diameter. This can be traced back to the huge temperature difference between the cold SiO_2 seeding layer and the

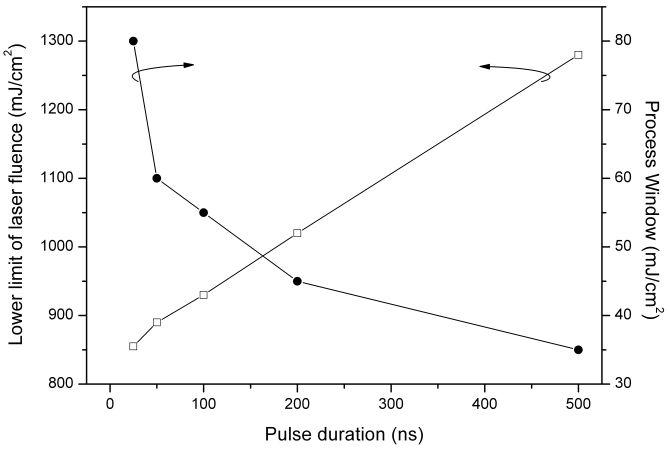


Figure 5.6: Effects of laser-pulse duration on the process windows for orientation- and location-controlled grains.

freshly solidified grain: the difference in thermal expansion between the two can cause huge mechanical stresses, giving rise to cracks.

5.3.3 Grains Crystallized with Substrate Heating

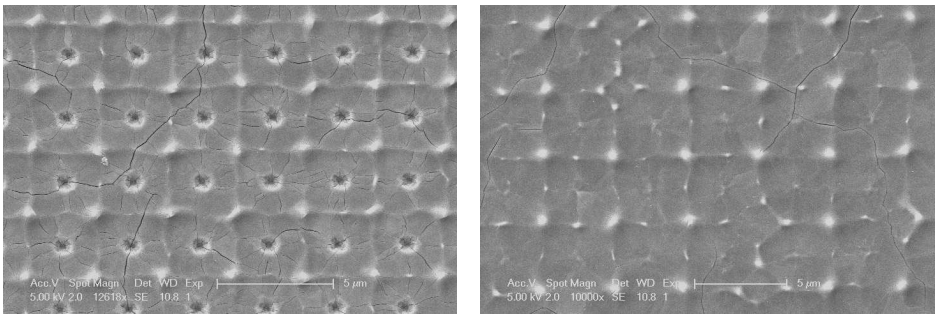
Grains crystallized with substrate heating show similar morphological variations as in Fig. 5.7 with increasing laser fluence. The critical energy density for the disappearance of cavities is now 980 mJ/cm^2. The absence of cracks in Fig. 5.7 indicates the necessity of using substrate heating to produce samples free of large cracks.

Figures 5.7 and 5.8 indicate that the location of the grains can be successfully controlled by the location of the holes underneath.

5.3.4 Orientation Control in Location-Controlled Grains

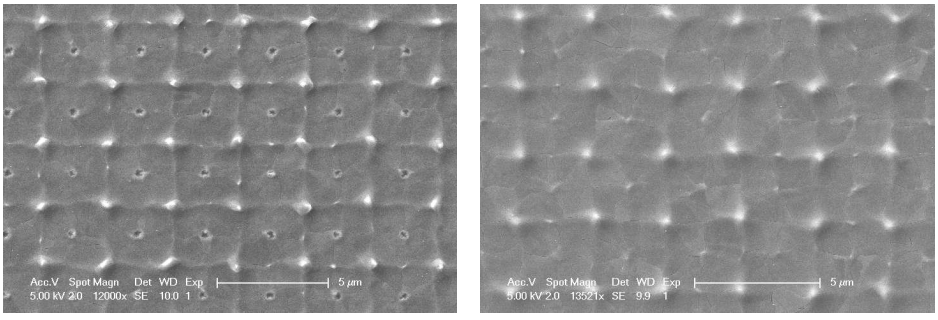
The crystallographic orientation of location-controlled grains is analyzed with EBSD. The results are shown in Fig. 5.9. For statistical analysis, a large area of location-controlled grains is analyzed by EBSD mapping. The grain size and the spacing of cavities are both 4 μm. Figure 5.9(a) shows the area mapped by EBSD. Within 10 degrees of misorientation tolerance, 19.8% of the area has $\langle 100 \rangle$ orientation. Figure 5.9(b) shows the areas that have $\langle 100 \rangle$ orientation parallel to the surface normal.

No preference of crystallographic orientation has ever been noticed in location-controlled grains grown from normal grain filters. The random crystallographic orientation of such grains is shown in Fig. 1.4. Setting the tolerance for misorientation at 10 degrees,



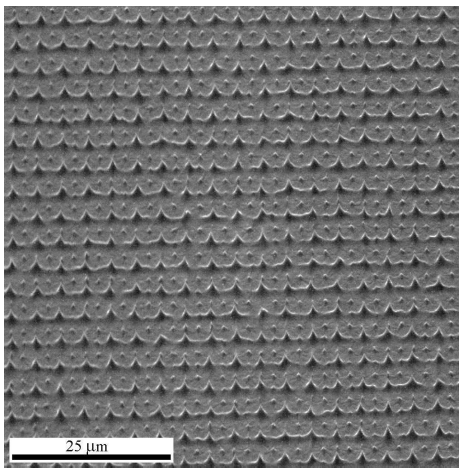
(a) (b)

Figure 5.7: SEM images of location-controlled grains crystallized at room temperature with a laser fluence of (a) 700 mJ/cm^2, and (b) 1140 mJ/cm^2. Cracks are clearly visible in both images.

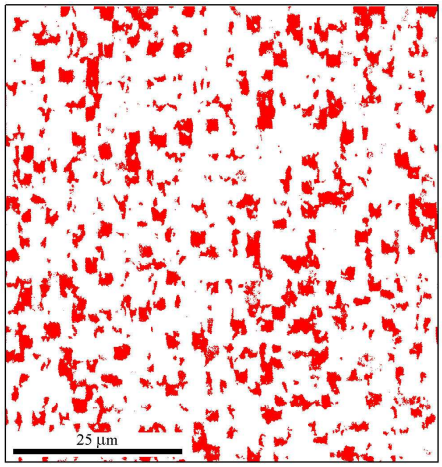


(a) (b)

Figure 5.8: SEM images of location-controlled grains crystallized with substrate heating up to $450°$C, with a laser fluence of (a) 960 mJ/cm^2, and (b) 1020 mJ/cm^2.



(a)



(b)

Figure 5.9: EBSD analysis of location-controlled grains crystallized with substrate heating up to $450°C$, with a laser fluence of 1060 mJ/cm^2: (a) area mapped for EBSD analysis; (b) area fraction of $\langle 100 \rangle$-oriented grains.

the area fraction of the ⟨100⟩-oriented grains is about 2.3% provided that the crystallographic orientation is completely random.

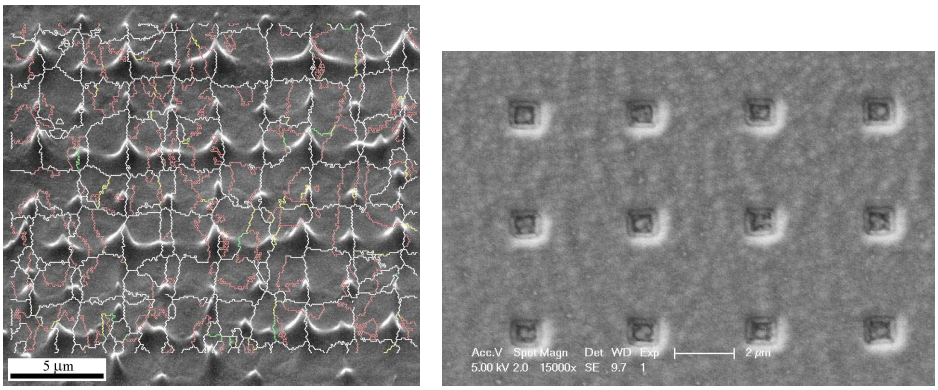
Application of a seeding layer increases the preference for crystallographic orientation significantly. The originally random crystallographic orientation of location-controlled grains can therefore be controlled, at least in principle, by the seeding layer.

However, the area fraction of location-controlled grains is not yet as high as 90%, obtained the value in the seeding layer. To fabricate highly uniform SG-TFTs, orientation control needs to be improved further.

The weak orientation preference during epitaxial growth from the seeding layer may be due to the following reasons: (1) the crystallographic orientation of the seeding layer is not so good as for monocrystalline silicon wafers (Section 3.2); (2) processes for opening a hole to the thin seeding layer are critical for epitaxial growth; (3) during the vertical growth phase, ⟨100⟩ orientation does not easily change into other orientations (Section 3.2). However, the possibility is still not entirely suppressed.

5.3.5 Defects Inside Crystallographic Orientation- and Location-Controlled Grains

The crystallographic orientation preference is weaker inside location-controlled grains than in the seeding layer. This could be traced back to defect generation during epitaxial growth from the seeding layer.



(a) (b)

Figure 5.10: Defects generated during epitaxial growth from the seeding layer. (a) SEM image overlaid with a grain-boundary-component map, indicating large grain boundaries inside one island and normally four grains per hole. (b) Top view of square-shaped holes, where grains start to grow from the seeding layer.

Figure 5.10 shows the defects generated during epitaxial growth from the seeding layer. In addition to CSL twin boundaries (Σ3, Σ9, Σ27a, and Σ27b) large grain bound-

aries (white lines) are also observed inside one island originating from each hole. Random boundaries divide each island into four grains.

Figure 5.10(b) shows the holes from which epitaxial growth starts after excimer-laser irradiation. The holes are revealed by Secco etching, which removes the α-Si film completely before excimer-laser irradiation in order to check the morphology of the holes. The holes are found to be square-shaped, with an opening of about 500 nm in diameter. Each sharp corner of the rectangle is a preferred site for the onset of solidification as it is the coldest location due to thermal conduction to the sidewalls. Epitaxial growth (solidification) initiates from the 4 corners and ends at the center of the holes. This explains why there are four grains per hole.

The location of large grain boundaries can still be controlled, although there are four grains from each hole. The grain at each quadrant of the island is large enough to fabricate a SG-TFT.

The large-angle grain boundaries in one island from each hole could be reduced with a rounder or smaller-diameter hole (comparable to normal grain filters).

5.4 Conclusions

In this chapter methods and processes to prepare orientation- and location-controlled grains were discussed.

The crystallographic orientation inside location-controlled grains can be controlled by the seeding layer that has a preferred $\langle 100 \rangle$ orientation and an opening beneath. The efficiency of orientation control is about 20% with this method. The orientation preference is significantly increased by the application of a seeding layer. In principle, orientation- and location-controlled grains can be prepared with this method. The area fraction of crystallographic orientation control could be improved by using a seeding layer with a perfect orientation control by employing an optimized processes.

With a 30 nm thick seeding layer the process to open the holes to the seeding layer is critical, as over-etching must be avoided. The geometry of the holes has a serious impact on defect reduction. Considerable reduction is expected for round-shaped holes whose diameter is similar to that of the the grain filter.

The seeding layer does not need to be a poly-Si film with orientation preference. For example, metal-lateral-induced crystallized (MILC) poly-Si films were observed to show orientation preference (along $\langle 100 \rangle$) [84].

Crystallographic orientation- and location-controlled grains are ideal candidates for SG-TFT fabrication. The methods discussed in this chapter could be a first step in this direction.

Chapter 6

SG-TFTs on Plastic Substrates

Chapters 3 and 5 dealt with a low-temperature process for producing SG-TFTs on glass substrates. We shall now turn to the efforts put in the development of an ultra-low temperature (100°C) process for producing SG-TFTs on plastic substrates, using a combination of excimer-laser crystallization and physical vapor deposition (PVD) techniques. The motivation behind this endeavor is to realize large-area microelectronics on cheap plastic substrates.

6.1 Introduction

Flexible electronics is an emerging and highly promising field in which remarkable progress has been made to build electronic circuits on flexible, large-area substrates [85]. Microelectronic devices are distributed and integrated over much larger substrates than what traditional microelectronics fabs can handle.

One of the prime objectives of flexible electronics is the realization of system circuits (memories, CPUs) on flexible plastic substrates that can be built directly on or into devices to enable them to sense, control, compute, communicate, etc. [86]. Research in this field is expected to yield new applications – large-area, flexible, light-weight products, such as direct-view large-area displays, electronic paper (e-paper), rollable displays, intelligent textures, artificial retinas, etc. – that will reshape the global market of large-area microelectronics.

Circuits on plastic substrates may be built using organic TFTs (OTFTs) [87]. Such circuits on polymer substrates are called *plastic electronics*; they can be realized with ink-jet printers with solution-processable materials and emerging roll-to-roll manufactures. However, as of now, the performance of OTFTs is not comparable to that of LTPS TFTs.

Since LTPS-based TFTs and high-quality c-Si TFTs would provide the best solution for IC-quality devices on plastic substrates at present, considerable effort has been put in the fabrication of LTPS-based TFT circuits on plastic substrates [88, 89].

There are two main approaches to deposit high-quality Si materials on plastic sub-

strates. The first is substrate transfer. A TFT circuit layer is first fabricated in a routine LTPS TFT process on a glass substrate, and then transferred onto a plastic substrate. Using this method, an 8-bit microprocessor was produced on a plastic substrate [4] by surface-free technology by laser annealing (SUFTLA) [90].

In the second approach integrated TFT circuits are fabricated directly on a plastic substrate. The most challenging part is the preparation of high-quality Si and gate oxide at a low process temperature. In this chapter we shall discuss the direct fabrication of TFTs for circuits on plastic substrates.

The process temperature has to be even lower for plastic substrates – typically, $100°$C for polyethylene terephthalate (PET) and $220°$C for polyethersulphone (PES) [91] – than for glass substrates ($400°$C) [92].

The requirement of low process temperature can be met by a combination of sputtering and excimer-laser crystallization [89]. In the sputtering step an α-Si film is prepared with low hydrogen content at a deposition temperature below the deformation temperature of the plastic substrate [93]. Excimer-laser crystallization of the α-Si film causes no thermal damage to the plastic substrate if the two are separated by a thin (< 0.5 μm thick) buffer layer – such as SiO_2, which can be deposited at an ultra-low temperature (see Section 6.4.1). This is because a short but intense pulse of laser energy is absorbed by the α-Si surface, and the heat diffusion length in such a short time is not more than 300 nm in SiO_2 [94].

Unfortunately, sputtered α-Si is easily ablated by the explosive evolution of the trapped ambient gas (such as Ar) during excimer-laser crystallization [95], resulting in a grain size smaller than 300 nm [93]. Ablation can be avoided by thermal annealing at $500°$C before laser crystallization [96]. However, high-temperature annealing is clearly not suitable for plastic substrates. Thus the suppression of ablation without high-temperature post-annealing poses a big challenge for the direct preparation of high-quality Si on plastic substrates.

Below, we shall first investigate the effects of sputtering conditions on subsequent excimer-laser crystallization in respect of ablation and the direct preparation of low-temperature poly-Si at $100°$C. Then we turn to the application of the μ-Czochralski process in the preparation of location-controlled grains. Finally, we discuss TFTs are fabricated inside location-controlled grains with gate-oxide deposition at a low temperature.

6.2 Low-Temperature Poly-Si

In this section we shall deal with the effects of sputtering parameters on subsequent excimer-laser crystallization and their optimization. LTPS is achieved at a maximum process temperature of $100°$C without any post-annealing.

6.2.1 Experimental Details

Sputtering

Prior to sputtering, monocrystalline Si wafers are thermally oxidized (at $1100°C$) to form a 100 nm thick SiO_2 film. An α-Si film – prepared by DC pulsed magnetron sputtering from a circular 12 inch intrinsic Si target (99.9999%) – is directly deposited on the SiO_2 layer. The sputtering system is set up in a sputter-down configuration, and the target to substrate distance is about 3 inches. The sputtering system is evacuated to a base pressure of around 5.3×10^{-5} Pa before sputtering. Deposition is performed in a pure argon atmosphere at 0.16 Pa. The frequency f of DC pulses is 150 kHz and the pulse width t_{on} (excitation period) is 2.6 µs, hence, the duty cycle $f \times t_{on}$ is held constant at 0.4. Deposition conditions (substrate temperature, substrate bias, plasma power, and Ar-flow rate) are summarized in Table 6.1. These four parameters are varied to investigate their effects on subsequent laser crystallization.

Table 6.1: Deposition conditions for pulsed DC magnetron sputtering

Wafer No.	Power [W]	Bias [W]	Temperature [°C]	Ar flow rate [sccm]	Deposition rate [nm/s]
A1	10	250	100	25	12.40
A2	10	250	40	25	12.31
A3	10	250	200	25	12.58
A4	10	250	400	25	12.36
B5	10	0	100	25	12.25
B6	10	50	100	25	12.33
B7	10	150	100	25	12.44
C8	6	250	100	25	8.33
C9	4	250	100	25	5.56
C10	0.5	250	100	25	0.71
D11	10	250	100	20	16.35
D12	10	250	100	40	12.40
D13	10	250	100	55	12.11
D14	10	250	100	85	11.68
E15	6	0	100	25	7.33
E16	3	0	100	30	7.03
E17	6	0	100	100	3.18

Residual Stress

The residual stress of sputtered α-Si films is measured by the curvature technique using a Tencor FLEX laser system. By measuring the curvature of the substrates prior to and after sputtering the stress is calculated using the Stoney formula [97]:

$$\sigma = \frac{Eh^2}{6(1-\nu)Rt}, \tag{6.1}$$

where $E/(1-\nu)$ is the biaxial elastic modulus of the substrate [MPa/m], h is the substrate thickness [m], and t is the thickness of the film thickness [m]. The curvature radius R of the substrate can be calculated from

$$R = \frac{R_1 \cdot R_2}{R_1 + R_2}, \tag{6.2}$$

where R_1 and R_2 are the curvature radii prior to and after the deposition of the α-Si film.

Thickness Measurement

After stress measurements, several square holes are opened in the α-Si layer by reactive ion etching (RIE); the thickness of α-Si is then measured by a surface profiler (Dektak 8, Veeco).

Argon Analysis

The argon content of the sputtered α-Si film is measured by Rutherford backscattering (RBS) channeling analysis. Samples are irradiated with a 2.3 MeV He ion beam. Experimental data are collected by a normal detector mounted at 170° and a grazing exit detector mounted at 115°.

Excimer-Laser Crystallization

The α-Si films are crystallized by a single shot of XeCl excimer laser (pulse duration: 50 ns; wavelength: 308 nm). The energy density of the laser pulse varies in 100 mJ/cm^2 increments from 100 mJ/cm^2 to the ablation threshold. During crystallization, the wafer is held in a high-vacuum chamber (1.33×10^{-5} Pa). No external substrate heating is applied during excimer-laser crystallization.

6.2.2 Results and Discussion

Effects of the Sputtering Parameters

Figure 6.1 shows the effects of the sputtering parameters on the residual stress of the sputtered α-Si layer.

To establish a common range for all data, the numerical values of the argon-flow rate and the plasma power are multiplied by 4 and 40, respectively. The negative sign

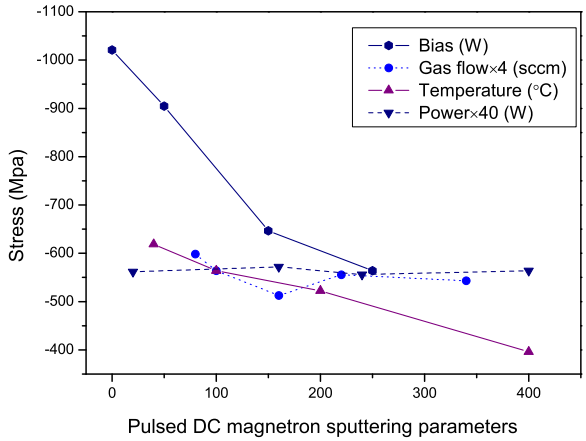


Figure 6.1: Effect of the parameters of pulsed DC magnetron sputtering on the residual stress in the α-Si film.

indicates that the sputtered α-Si films are under compressive stress in all cases. Of all parameters substrate bias has the largest impact.

As a reference, the residual stress of a 250 nm thick α-Si film deposited by LPCVD at $547°$C on a thermally grown 1.0 µm thick SiO_2 layer is measured. The layer is found to be under -23.5 MPa of compressive stress, which is negligible compared with that of the sputtered α-Si layer.

The residual stress of the sputtered α-Si film is related to its intrinsic structure (the mismatch of the interface between the Si film and the SiO_2 substrate) and the thermal stress during sputtering. Hence the residual stress σ of the film is the sum of thermal stress (σ_T), growth-induced stress (σ_g), and structural-mismatch-induced stress (σ_m) [98]:

$$\sigma = \sigma_T + \sigma_g + \sigma_m. \tag{6.3}$$

σ_T is an extrinsic stress, whereas σ_g and σ_m are intrinsic stresses. σ_g is caused by high-energy ion bombardment during sputtering, while σ_m is the result of lattice mismatch between the film and the substrate, or between various phases in the film. The sputtered α-Si film is amorphous on an amorphous SiO_2 substrate, therefore, $\sigma_m \approx 0$, so

$$\sigma = \sigma_T + \sigma_g. \tag{6.4}$$

σ_T results from the difference of the coefficients of thermal expansion (CTEs) of the Si film and the SiO_2 substrate [99]:

$$\sigma_T = \frac{E_{\text{Si}}}{1-\nu} \int_{T_{\text{room}}}^{T_{\text{dep}}} \left[\alpha_{\text{Si}}(T) - \alpha_{\text{SiO}_2}(T)\right] \, dT, \tag{6.5}$$

where T_{dep} is the sputtering temperature and T_{room} is the room temperature, E_{Si} is the elastic modulus and ν is Poisson's ratio for the sputtered α-Si film. $\alpha_{\text{Si}}(T)$ and $\alpha_{\text{SiO}_2}(T)$

are the CTEs of the film and substrate. As a rough estimate, σ_T is proportional to the product of Δ(CTE) and ΔT, where $\Delta(\text{CTE}) = \alpha_{\text{Si}}(T) - \alpha_{\text{SiO}_2}(T)$ and $\Delta T = T_{\text{dep}} - T_{\text{room}}$.

During the post-cooling phase after sputtering, the shrinkage of the Si film would be larger than that of the SiO_2 substrate – i.e., the CTE of the Si film is larger than that of the $1100°$C thermally grown SiO_2 substrate. Therefore σ_T is positive and tensile. In Fig. 6.1 the sum of stresses is compressive in the sputtered α-Si film, indicating that the contribution of σ_T to σ is minor. σ_T increases with sputtering temperature, leading to a more tensile stress (positive sign). This can explain the observation in Fig. 6.1 that the sum of the stresses decreases with increasing substrate temperature.

Since σ_T is positive and tensile, σ_g is the main contribution to the compressive stress [Eq. (6.4)] in the sputtered α-Si film. During deposition, particle bombardment of the film surface can lead to the displacement of atoms, defects, and implantation of inert gas, inducing residual stress in the sputtered Si film. These high-energy ions transfer not only energy but also momentum to the growing film. If momentum transfer dominates, residual-induced stress is compressive, much like for cold-working. On the other hand, if energy transfer dominates, the film is in a tensile state. High energy increases the mobility of atoms, resulting in thermal annealing of the film [100]. At a certain threshold energy the film obtains sufficient energy to initiate annealing. Silicon has a high melting temperature, so this threshold is difficult to reach. Consequently, the sputtering of Si is dominated by momentum transfer.

Theoretically, higher substrate bias implies larger momentum of the high-energy ions, and so higher compressive stress. However, as shown in Fig. 6.1, stress decreases with increasing substrate bias. This cannot be explained in terms of the domination of momentum transfer.

The variations of residual stress with substrate bias may be due to the trapped Ar of the α-Si layer.

RBS analysis (Fig. 6.2) shows that trapped Ar content increases with substrate bias. The same observation was made in [101]. This trapped Ar gives rise to pores and a weakly bonded matrix of Si atoms. The stress around the trapped Ar is tensile. The higher the substrate bias, the higher the trapped Ar content in the α-Si layer. Thus, at high substrate biases the compressive stress is released at a high content of trapped Ar. This is a plausible explanation for the stress introduced during sputtering, which decreases with increasing substrate bias. For decreasing substrate bias film porosity decreases, while film density increases.

Figure 6.3 summarizes the effects of substrate bias on the ablation threshold: a sputtered α-Si film with a high compressive stress contains less trapped Ar, and hence has a higher mass density, which is advantageous for the suppression of ablation during subsequent excimer-laser crystallization.

In summary, residual stress can be used as a figure of merit to monitor the Ar content in an α-Si film. High compressive stress, which indicates low Ar content, is advantageous for subsequent excimer-laser crystallization.

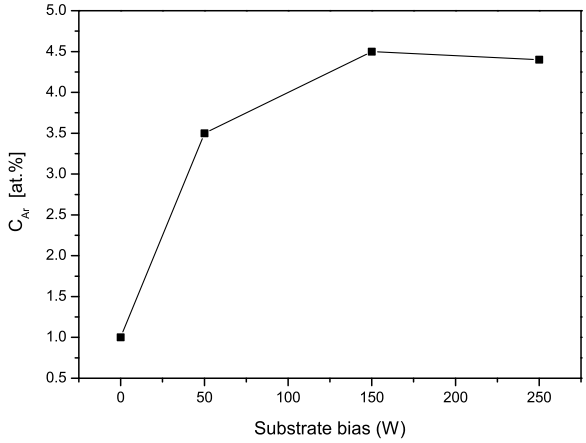


Figure 6.2: Content of trapped Ar in an α-Si film as a function of the substrate bias (wafers No. A1, B5, B6, B7). C_{Ar} is analyzed by RBS.

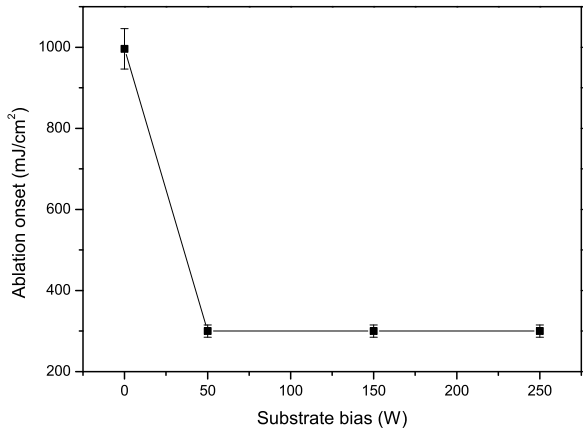


Figure 6.3: Influence of the substrate bias on ablation during excimer-laser crystallization (wafers No. A1, B5, B6, B7).

Optimization of the Sputtering Parameters

To optimize sputtering parameters, the effects of frequency (f) and pulse width (t_{on}) of pulsed DC magnetron sputtering are investigated. Residual stress is now used for monitoring the Ar content in α-Si films. Table 6.2 summarizes the parameters used for optimization. The substrate bias, substrate temperature, and plasma power are keep constant at 0 W, 100°C, and 6 kW, respectively.

Table 6.2: Sputtering parameters used for optimization

Wafer No.	Frequency [kHz]	Pulse width [ns]	Ar flow rate [sccm]
F1	50	2016	100
F2	100	2016	100
F3	150	2016	100
F4	200	2016	100
G5	150	976	100
G6	150	496	100

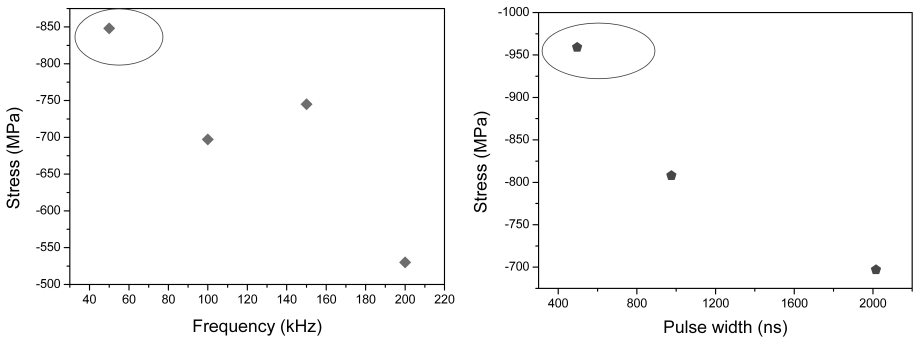


Figure 6.4: Residual stress as a function of (a) frequency and (b) pulse width. Ellipses indicate the selected parameters.

Figure 6.4 shows stress as function of frequency (f) and pulse width (t_{on}). Parameters with a high stress are selected, indicated by ellipses.

The sputtering parameters to be optimized are low frequency, low pulse width, and zero substrate bias. For example, for the pulsed DC magnetron sputtering system used in this study, the optimized parameters are: $f = 50$ kHz, $t_{\text{on}} = 496$ ns, zero substrate bias, substrate temperature $T_{\text{substrate}} = 100°\text{C}$.

With these parameters the ablation threshold is as high as 1100 mJ/cm^2 for a 250 nm thick α-Si film. The suppression of ablation in the sputtered α-Si film is realized without any high-temperature post-annealing.

Poly-Si Grains

After the laser crystallization and Secco etching of the α-Si films deposited using the optimized sputtering parameters described above, the microstructure of polycrystalline grains is investigated by SEM. Figure 6.5 shows the SEM images of the grains crystallized from a 122 nm thick α-Si film. At a low energy density of 200 mJ/cm^2 [Fig. 6.5(a)] fine grains (diameter: a few times ten nanometers) are observed. This energy density is not sufficiently high to crystallize the entire layer. Therefore, the crystallized fine poly-Si grains form a network, encompassing the inner α-Si phase. At 300 and 400 mJ/cm^2 the α-Si layer is completely crystallized and the grain size ranges from 1 to 1.8 μm. At even higher laser energy densities (500 and 600 mJ/cm^2) large grains are surrounded by very fine poly-Si grains. The density of large grains decreases with increasing laser energy density. At 700 mJ/cm^2 [Fig. 6.5(f)] fine grains are formed everywhere, and large grains disappear on account of lateral growth.

To describe variations of microstructural with laser energy density, the diameter and density of grains are plotted in Fig. 6.6 against laser energy density. The density of large grains is calculated roughly from the large-grain area coverage. As indicated in Fig. 6.6, the laterally grown grains can be obtained in a wide energy density range in this case, for a 122 nm thick α-Si layer. The energy density window ranges from 300 to 600 mJ/cm^2, which is 60% of the total energy density window (from 200 to 700 mJ/cm^2). This high proportion cannot be explained in terms of the near-complete melting theory developed by Im and Kim [17]. In this theory, grain size increases markedly in a very narrow energy density window. These superlaterally grown (SLG) grains nucleate and grow from unmolten seeds in a near-complete melting range. As shown in Fig. 6.6, above 400 mJ/cm^2 the density of the large grains decreases with increasing laser energy density, which indicates that the source (nucleus) – where lateral growth starts – melts at a higher energy density. When the energy density is sufficiently high (in this case, 700 mJ/cm^2), nuclei are completely molten. Hence no lateral growth occurs, resulting in fine grains everywhere [Fig. 6.5(f)].

Figure 6.7 shows the morphology of grains grown laterally from the sputtered α-Si film. The morphology of these grains is different from that of the grains grown from the α-Si:H film prepared by LPCVD [102]. Figure 6.7(a) shows that large poly-Si grains are petal-shaped, with radial subgrain boundaries originating from a central nucleus. These nuclei are probably fine crystallites with a high density of defects, either nucleated from amorphous Si with high-energy ion bombardment during sputtering, or conglomerated from crystalline Si particles deposited from the Si target. These nuclei feature a very high density of defects. They can be etched away in a long process of Secco etching, as shown in Fig. 6.7(b).

The wide energy density window and petal-like morphology of grains cannot be explained in terms of the SLG theory. According to speculations, the sputtered α-Si film

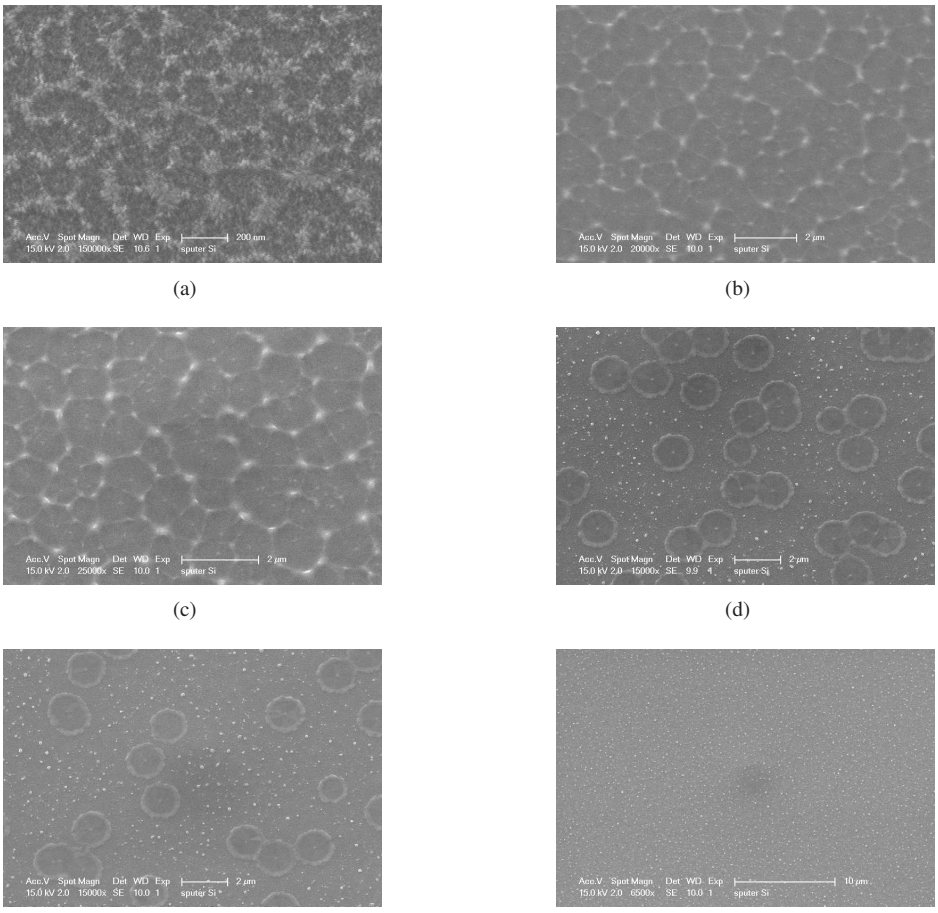


Figure 6.5: SEM images of grains grown from a 122 nm thick α-Si film (wafer No. E15) crystallized at: (a) 200 mJ/cm^2; (b) 300 mJ/cm^2; (c) 400 mJ/cm^2; (d) 500 mJ/cm^2; (e) 600 mJ/cm^2; and (f) 700 mJ/cm^2.

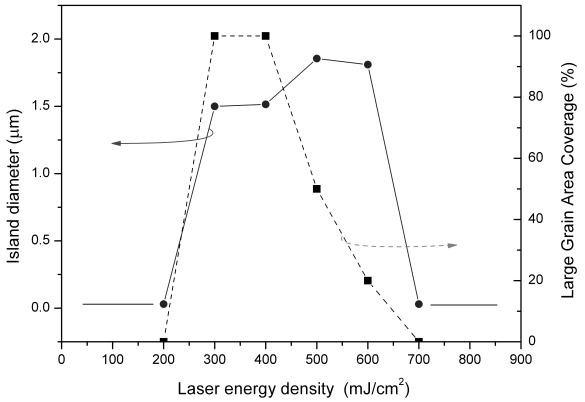


Figure 6.6: Diameter of laterally grown grains and large-grain area coverage for a 122 nm α-Si layer (wafer No. E15) as a function of the energy density of the laser pulse.

is an α-Si matrix, made up of fine crystals. Since these crystals have a higher melting point than the surrounding α-Si, they do not melt at the same time as the surrounding α-Si during laser irradiation. Consequently lateral growth starts from these unmolten fine crystalline seeds after laser irradiation, during solidification. The number of nuclei decreases with increasing in laser energy density as crystallites melt. At a sufficiently high laser-energy density they all melt, and thus no lateral growth occurs. The crystallites in the α-Si matrix give rise to a wide energy-density window and a petal-like morphology.

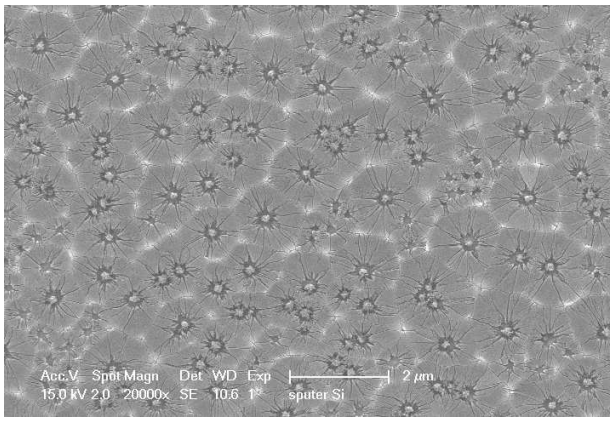
6.2.3 Summary

Spurred by the motivation of preparing large grains at a low process temperature for flexible substrates, excimer-laser crystallization of sputtered α-Si films was investigated in the foregoing.

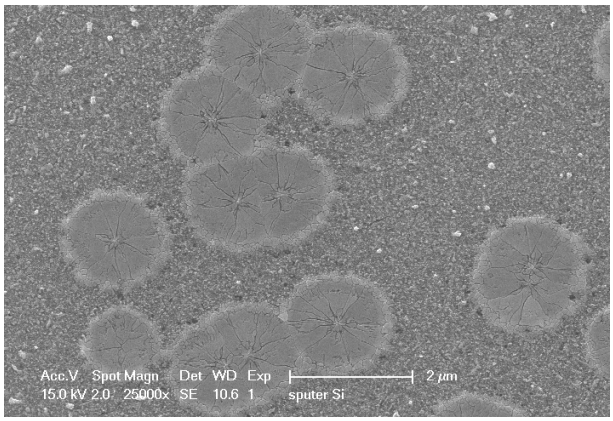
Sputtered α-Si is successfully crystallized at room temperature without any high-temperature thermal annealing. The obtained grains are 1.8 µm in diameter, i.e., much larger than those produced with LPCVD. The maximum process temperature to prepare the poly-Si film is $100°$C; this is highly promising for the fabrication of large poly-Si grains on plastic foils for large-area flexible microelectronics applications.

It was found that high compressive stress – arising from non-bias sputtering – is advantageous for the suppression of ablation during subsequent excimer-laser crystallization. This high residual stress is due to the low content of trapped Ar and the high density of the film. In other words, compressive residual stress is released at a high content of trapped Ar.

The growth mechanism of sputtered α-Si after excimer-laser crystallization was discussed and compared with that of α-Si:H from LPCVD. The former one has a wider energy density window and larger grain size with a petal-shaped morphology.

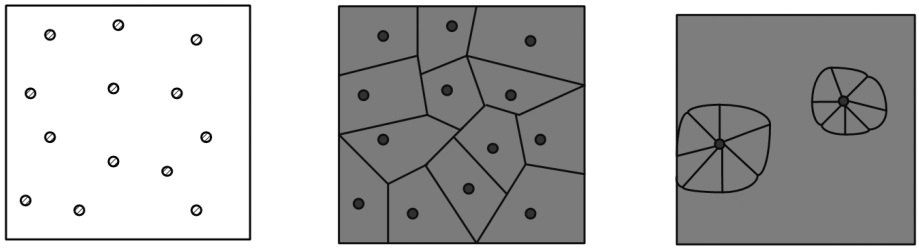


(a)



(b)

Figure 6.7: Morphology of laterally grown grains after excimer-laser crystallization of the sputtered α-Si film (wafer No. E15) at (a) 400 mJ/cm^2 and (b) 500 mJ/cm^2.



(a) (b) (c)

Figure 6.8: Schematic representation of the growth mechanism of an α-Si precursor after laser irradiation. (a) As-deposited α-Si; round dots are randomly distributed fine crystals. (b) Collided grains at a low energy density of laser pulse. (c) Large grains at a higher energy density of laser pulse.

Although the buffer SiO_2 layer was thermally grown at $1100°C$, it is not necessary to form a buffer layer at such a high temperature: the SiO_2 layer can just as well be formed at $80°C$ by inductively coupled plasma enhanced CVD (ICPECVD), as discussed in Section 6.4.1.

6.3 Location-Controlled Grains

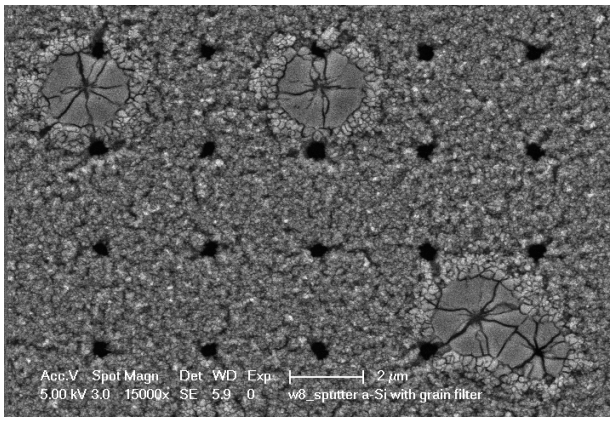
The preparation of high-quality Si active materials on plastic substrates for TFT fabrication requires the control of the location of the grains. Hence the μ-Czochralski method is employed in the low-temperature process.

To improve the step coverage of sputtering, which is inferior to that of LPCVD, the grain filter is modified. This section is devoted to all those improvements that opened the way to preparing location-controlled Si islands at a maximum process temperature of $100°C$.

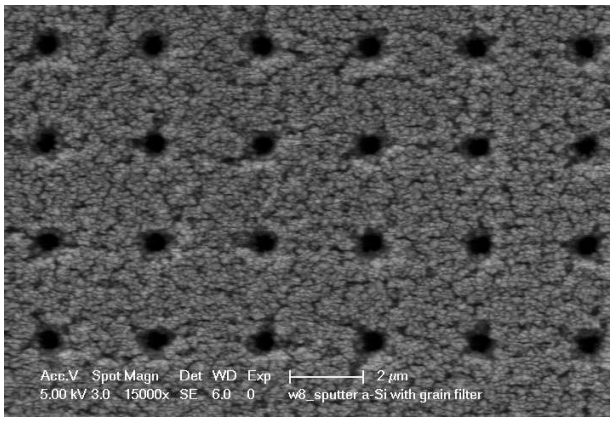
6.3.1 With Normal Grain Filter

First, sputtered α-Si is deposited directly on top of the SiO_2 layer with grain filters. Then the α-Si film is crystallized with a single shot of excimer laser. Figure 6.9 shows SEM images of the crystallized film on top of the grain filter. Unlike for α-Si deposited by LPCVD, no location-controlled grain is seen to have grown from the grain filter. There are some large grains at 700 mJ/cm^2, however these are not grown from the grain filter but are the large grains described in the previous section [Fig. 6.9(a)]. Only small grains are observed at 1100 mJ/cm^2.

Figure 6.9 indicates that it is impossible to prepare location-controlled grains with direct deposition of sputtered α-Si on grain filters. The high aspect ratio of the grain filter causes a poor step coverage during sputtering, which could account for the lack of



(a)



(b)

Figure 6.9: Microstructure of a 250 nm thick sputtered α-Si layer crystallized at an energy density of (a) 700 mJ/cm^2; (b) 1100 mJ/cm^2.

location-controlled grains. The narrow (∼100 nm) and deep (1 μm) grain filter is not filled with α-Si; its interior may be void. The bottom of the grain filter contains no seeds during laser crystallization.

6.3.2 With Modified Grain Filter

To improve step coverage, the grain filter is modified by back-etching the 2nd TEOS layer (Fig. 1.1). The schematic diagram of back-etching is shown in Figure 6.10. Back-etching renders the slope of the sidewall smooth and the hole wider than a normal grain filter.

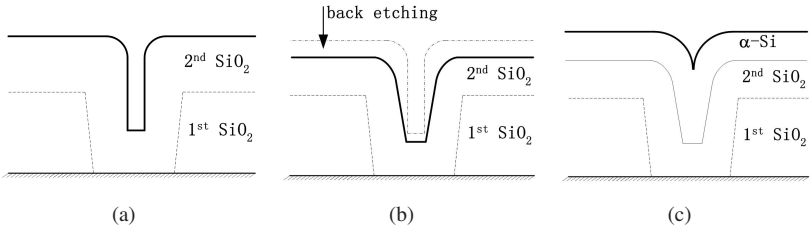


Figure 6.10: Modified grain filter obtained by back-etching the 2nd TEOS layer. (a) Normal grain filter; (b) back-etching of the 2nd TEOS layer; (c) sputtering α-Si on the modified grain filter.

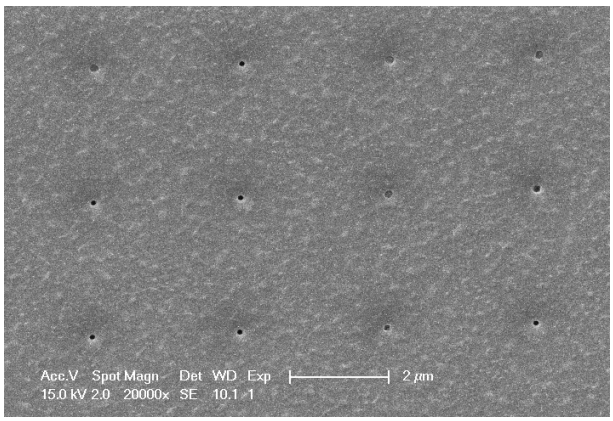
The thickness of the 2nd TEOS layer is about 800 nm for a normal grain filter. To determine the optimum time for back-etching, a 4-inch wafer is divided into four quarters, and different back etching times are used on each (0 s, 28 s, 56 s, and 84 s). The etching rate is about 9 nm/s in each case. After 84 seconds of back-etching, the 2nd TEOS layer is almost completely etched away, except for the sidewall of the holes. Then a 125 nm thick α-Si layer is sputtered on top of the modified grain filter. Subsequently, the α-Si layer is crystallized with a single shot of excimer laser.

Figure 6.11 shows the microstructure after laser crystallization. The probability of obtaining location-controlled grains increases with increasing back-etching time: at 56 seconds there are grains around the grain filter, while at 84 seconds there are several single grains grown from grain filters. Although the grains are small (probably because of the thickness of the α-Si layer), their location is controlled by the grain filter.

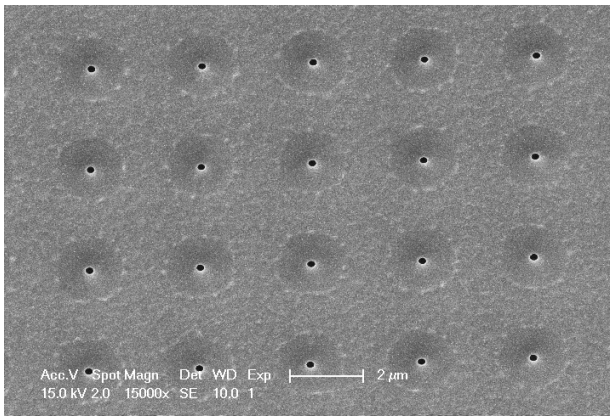
Orientation- and location-controlled grains were prepared using this modified grain filter, in combination with nickel-induced lateral growth, leading to a preferred $\langle 110 \rangle$ orientation [103]. Due to its larger diameter, the modified grain filter induces a higher number of defects and a low selectivity of single-crystalline seeds [104].

6.3.3 Location-Controlled Grains

Using the modified grain filter described in the previous subsection, location-controlled grains can be fabricated at a low process temperature.

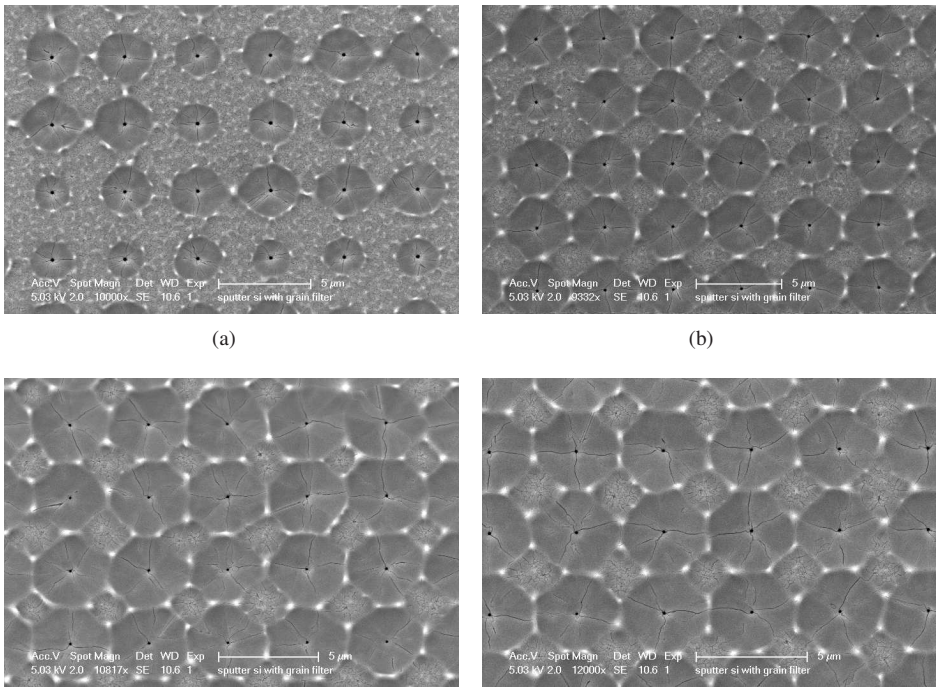


(a)



(b)

Figure 6.11: Microstructure of a 125 nm thick sputtered α-Si film crystallized at an energy density of 620 mJ/cm^2 with the modified grain filters. The back-etching time is (a) 56 seconds; (b) 84 seconds.



(a) (b)

(c) (d)

Figure 6.12: SEM images of grains grown from a 250 nm thick α-Si film crystallized at (a) 775 mJ/cm^2; (b) 825 mJ/cm^2; (c) 875 mJ/cm^2; (d) 900 mJ/cm^2.

Figure 6.12 shows SEM images of location-controlled grains grown from modified grain filters with a 250 nm thick sputtered α-Si layer, crystallized at room temperature. Square-shaped grains with a diameter of 3 µm can be successfully obtained as shown in Fig. 6.12(a); here the spacing between grain filters is 3 µm and the energy density is 775 mJ/cm^2. The maximum grain size is 4 µm, as shown in Fig. 6.12(d), where the spacing is increased to 4 µm and the laser fluence to 900 mJ/cm^2. Now the diagonal direction is not filled with the large grains, and eventually octagonal-shaped grains are obtained. The center of each grain features a pinhole; this is caused by insufficient filling of α-Si due to the poor step coverage. The pinholes can be removed by further improvement of the step coverage.

Location-controlled grains with a diameter of 4 µm can be obtained in a relatively wide energy-density window. These grains can used for the fabrication of single-grain thin-film transistors (SG-TFTs) on plastic substrates for flexible electronics.

6.4 Fabrication of SG-TFTs

The fabrication of high-performance TFTs is a crucial step for building integrated circuits (ICs) directly on plastic substrates – and at the same time quite a challenge at low process temperatures. This section will be concerned with the fabrication of TFTs inside location-controlled grains at a low process temperature. Electric performance data show that high-performance TFTs can be fabricated on plastic substrates.

Preparing high-quality gate insulators for active devices at a low process temperature is another difficulty that has to be overcome in order to form high-quality circuits directly on plastic.

In this section we shall first discuss the general aspects of gate-oxide deposition at low temperatures. Then we shall turn to the fabrication of TFTs in location-controlled grains using a low-temperature gate oxide.

6.4.1 Low-Temperature Oxide

ICPECVD

PECVD is widely used for the low-temperature deposition of gate insulators in poly-Si TFTs [105]. It should be noted that intense ion bombardment in conventional PECVD may cause considerable inherent plasma damage at the interface between the gate insulator and the poly-Si film.

The recent development of inductively coupled plasma-enhanced CVD (ICPECVD) for low-temperature gate-oxide deposition [106] has attracted a lot of attention because the ion energy and the ion current density of the plasma can be controlled independently. ICPECVD can ensure low plasma damage even for high plasma densities. Compared to conventional PECVD, ICPECVD minimizes film contamination, promotes film stoichiometry, and reduces plasma damage caused by direct ion-surface interactions.

MOS Capacitors

The electronic properties of low-temperature ICPECVD SiO_2 are investigated by C-V and I-V measurements of MOS capacitors.

The MOS capacitors used in this study are fabricated with p-type (100) silicon wafers of resistivity between 2 and 5 Ω·cm. Right after dipping the wafer into 0.55% HF for 2 minutes to remove native oxides, a 100 nm thick SiO_2 gate is deposited at $80°C$ by ICPECVD (at Sentech Instruments GmbH). The ICP source has a frequency of 13.56 MHz and a power of 500 W; SiH_4 and O_2 are used as precursor gases. Aluminum (Al) is sputtered onto the oxide surface and patterned by photolithography into islands (area: 0.0064 cm^2). The backside of the wafer is coated also with a thin layer of Al to serve as an ohmic contact.

I-V Measurement

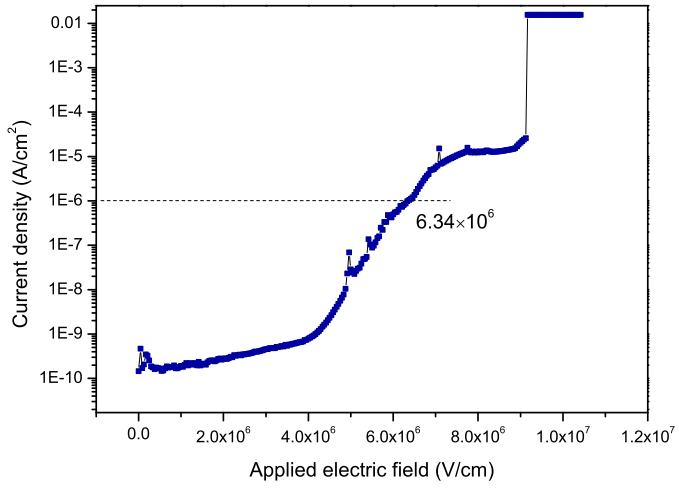


Figure 6.13: Current density (I) vs. applied electric field (E) characteristics for Al/SiO_2/p-type Si MOS capacitors. The breakdown field is 6.34×10^6 V/cm; the resistivity is 5.20×10^{15} Ω·cm.

The analysis of the resistivity and breakdown voltage of the ICPECVD SiO_2 layer is based on I-V measurements. A high-resistivity gate oxide leads to a low leakage current during TFT operation. A higher breakdown voltage ensures more tolerance for a maximum electric field across the gate oxide.

Figure 6.13 shows the current density (I) as a function of the applied electric field (E) for ICPECVD SiO_2. The breakdown field – defined as the field at which the leakage current density reaches 1 μA/cm^2 – is 6.34×10^6 V/cm. Resistivity (ρ) – defined at $E = 1$ MV/cm – is 5.20×10^{15} Ω·cm. These properties are comparable to those of thermally grown SiO_2 (Table 6.3).

C-V Measurement

Interface characteristics are investigated by C-V measurements of MOS structures using an LCR meter (Agilent 4282A).

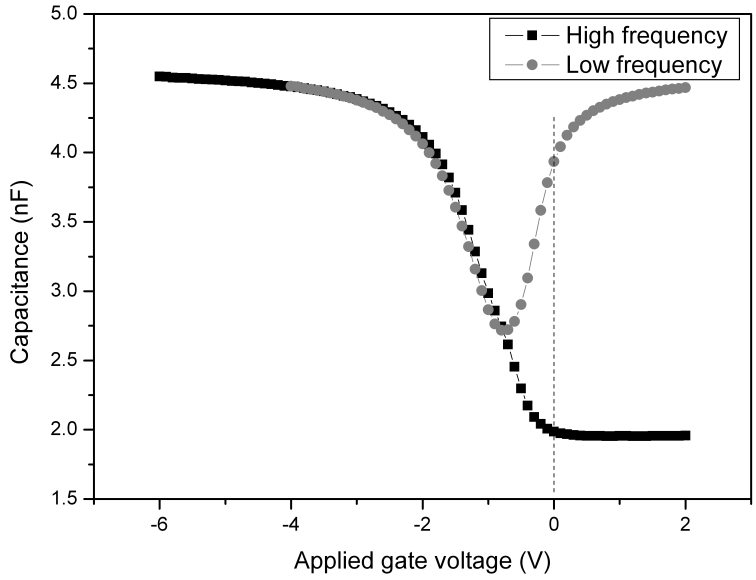


Figure 6.14: Capacitance vs. applied gate voltage curves for Al/SiO_2/p-type Si MOS capacitors; SiO_2 is deposited at $80°$C.

The interface trap density (D_{it}) at mid-gap is calculated from quasi-static and high frequency C-V measurements [107]. The dependence of the interface trap density on applied gate voltage, $D_{\text{it}}(V_{\text{g}})$, can be extracted from the difference of high- and low-frequency C-V curves:

$$D_{\text{it}}(V_{\text{g}}) = \frac{1}{A}\frac{C_{\text{ox}}}{q}\left(\frac{C_{\text{QS}}/C_{\text{ox}}}{1 - C_{\text{QS}}/C_{\text{ox}}} - \frac{C_{\text{HF}}/C_{\text{ox}}}{1 - C_{\text{HF}}/C_{\text{ox}}}\right), \tag{6.6}$$

where C_{ox} is the oxide capacitance, C_{QS} and C_{HF} are the quasi-static (QS) and high frequency (HF) capacitance from accumulation to strong inversion, q the electronic charge [eV^{-1}cm^{-2}], and A is the gate area.

The density of interface trap states (D_{it}) is evaluated from the high- and low-frequency C-V characteristics of MOS capacitors (Fig. 6.14). For the used frequencies, 100 Hz and 100 kHz, D_{it} is estimated to be as low as 3.21×10^{10} cm^{-2}eV^{-1}. This is comparable to that of thermally grown SiO_2.

Table 6.3 compares the electric performance of the low-temperature ICPECVD oxide, and thermally grown oxide.

Table 6.3: Summary of electric characteristics for two kinds of oxide

	Low-temperature ($80°$C) ICPECVD SiO_2	Thermally grown SiO_2
Breakdown field [MV/cm]	6.34	8.1 [108]
Resistivity [Ω·cm]	5.20×10^{15}	8.7×10^{15} [108]
D_{it} [cm^{-2}eV^{-1}]	3.21×10^{10}	3.2×10^{10} [57]

6.4.2 SG-TFTs

TFT Fabrication

Top-gate n-channel TFTs are fabricated in location-controlled single grains. These single grains are patterned so that an active channel, positioned outside the grain filter, is established inside the grain. The channel length and width are both 1 µm. Since the grain is smaller than normal grains fabricated at high temperatures (Section 3.1), the smaller features of the devices are exploited.

A 100 nm thick SiO_2 layer is deposited with ICPECVD technique at $80°$C. Then Al is sputtered at room temperature, and patterned into a gate. After this step the gate oxide is patterned in a low-power fluorine-based plasma with Al gate as a mask.

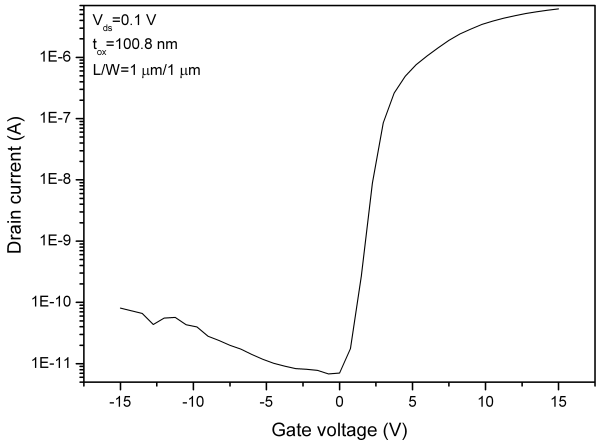
Source and drain regions are doped with phosphorus, using ion implantation at 30 keV and a concentration of 10^{16} ions/cm^2. Implantation is performed in a self-aligned manner with the Al-gate-oxide stack as a mask. The source and drain implantations are activated with excimer-laser annealing at room temperature. The energy density of activation is 300 mJ/cm^2, with 80% overlap scanning mode.

Finally, source and drain electrodes are made by Al sputtering at room temperature.

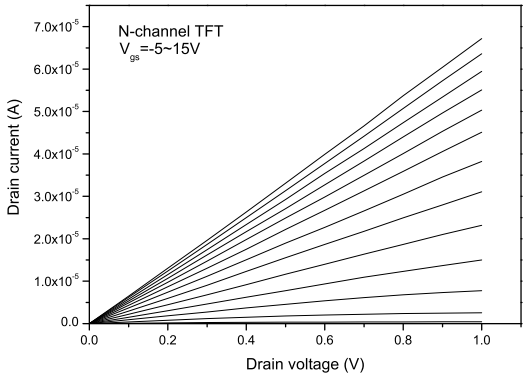
TFT Performances

Transfer and output characteristics for SG-TFTs with a SiO_2 gate deposited at $80°$C are shown in Fig. 6.15. The field-effect mobility of electrons, defined at a low-drain voltage, is 290 cm^2/V·sec, while the subthreshold slope is 0.49 V/dec.

Such high-performance TFTs fabricated at such a low temperature are very promising ingredients for electronic circuits on plastic substrates.



(a)



(b)

Figure 6.15: Transfer characteristics (a) and output characteristics (b) of single-grain TFTs fabricated with gate-oxide deposition at 80°C. The subthreshold slope is 0.49 V/dec., while the maximum electron field-effect mobility is 290 $cm^2/V{\cdot}sec$.

Mobility is not much higher in SG-TFTs fabricated at this low temperature than in SG-TFTs fabricated at higher temperatures [6, 33]. Because of the modification to the grain filter (Chapter 6.3.2), the location-controlled grains (Fig. 6.12) have a high surface topography. The large surface roughness is assumed to be a major reason for the reduction of mobility due to surface scattering of electrons, which implies that mobility can be improved by the reduction of surface roughness.

6.5 Conclusion

In this chapter we demonstrated that high-performance SG-TFTs can be fabricated at a process temperature of $100°$C. Such a low process temperature opens the way to using SG-TFTs as active devices for microelectronics on plastic substrates.

By combining sputtering and excimer-laser crystallization, sputtered α-Si is successfully crystallized at room temperature without ablation. Poly-Si grains with a diameter of 1.8 μm can be prepared with a maximum process temperature of $100°$C.

Using modified grain filters, location-controlled grains can be prepared for SG-TFT fabrication. Location-controlled grains with a diameter of 4 μm can be obtained in a relatively wide energy density window.

N-type TFTs are fabricated inside location-controlled grains, by low-temperature oxide deposition via inductively coupled plasma-enhanced chemical vapor deposition (ICPECVD). The electric performance of gate oxide deposited at $80°$C is comparable to that of thermally grown oxide.

TFTs fabricated in location-controlled grains with low-temperature gate oxide feature a field-effect mobility of 290 $cm^2/V{\cdot}sec$ and a subthreshold slope of 0.49 V/dec.

In this chapter we only demonstrated that n-type TFTs can be fabricated at low temperatures. Nonetheless p-type TFTs, TFT-based CMOS circuits, or more complicated circuits may also be fabricated in location-controlled grains at low process temperatures.

This method of producing IC-quality TFTs at a low process temperature is a promising step toward the fabrication of large-area microelectronics on plastic substrates. New applications are expected to appear in the near future, such as flexible displays, sensor arrays for structural health monitoring (for aircraft and armament), multi-functional foldable blankets (displays, antenna and solar cell arrays), etc.

Chapter 7

Conclusions and Recommendations

The μ-Czochralski (grain filter) process is a highly promising technology for preparing two-dimensional location-controlled grains that can be used for SG-TFT fabrication on large-area substrates. This thesis is concerned with possible improvements of this technology in three main aspects: defect reduction, crystallographic orientation control, and low-temperature process. The results are briefly summarized in this chapter.

In addition to these conclusions, this chapter also contains some recommendations for further research.

7.1 Conclusions

The conclusions of this research are summarized separately for each part of the thesis:

General

- Two-dimensional single-crystalline location-controlled grains can be prepared with the μ-Czochralski process. The maximum grain size of the location-controlled grains is 7 μm. SG-TFTs fabricated inside location-controlled grains show a high performance, an electron field-effect mobility of 600 $cm^2/V{\cdot}sec$, an off-current of $1.3{\times}10^{-13}$ A, and a subthreshold swing of 0.21 V/dec.

- There are a large number of planar defects (microtwins) inside the location-controlled grains, while the crystallographic orientation of location-controlled grains is random. To improve the performance and uniformity of SG-TFTs, planar defects should be reduced and crystallographic orientation should be controlled in some preferred orientation.

- In view of the emerging field of microelectronics on large-area flexible plastic substrates, an ultra-low temperature process should be developed in conjunction with the μ-Czochralski process.

Defect Reduction

- A capping layer is deposited on top of the α-Si film using the μ-Czochralski process, and its thermal effects on defect reduction are examined. These are found to be insufficient, i.e. a capping layer cannot considerably reduce the number of planar defects. It does, however, enlarge the size of location-controlled grains.

- By introducing a seed at the bottom of the grain filter, planar defects can be significantly reduced. It is found that at sufficient energy density and substrate heating, single-crystalline grains can be prepared at predetermined positions with the same orientation as the substrate.

- Structural properties of epitaxial grains depend strongly on the orientation of the substrate. The number of defects in (100)-oriented grains is much lower than in non-(100) oriented grains.

- When prepared with a low-power dry soft-landing step, epitaxially grown grains from (100)-oriented wafers feature 4 secondary subgrains in each grain. TEM analysis shows that secondary subgrains originate from twin lamellas at the corners of spacers. These secondary subgrains develop when facets are formed at the three-phase boundary among SiO_2, liquid Si, and solid Si in the presence of $\langle 110 \rangle$ oxide sidewalls.

Crystallographic Orientation Control

- Poly-Si films on amorphous insulating substrates with $\langle 100 \rangle$ surface orientation and $\langle 100 \rangle$ in-plane orientation are prepared by multiple-shot excimer-laser irradiation. A laser-induced periodic surface structure (LIPSS) coexists with crystallographic orientation preference, and a self-assembly process organizes poly-Si into square-shaped grains. This LIPSS formation may be the underlying reason for orientation preference. Poly-Si films showing $\langle 100 \rangle$ preference can be used for TFT fabrication or – with a seeding layer – for the preparation of orientation- and location-controlled grains.

- Orientation- and location-controlled grains can be prepared with a seeding layer that shows orientation preference. Specifically, the crystallographic orientation of 20% (areal fraction) of location-controlled grains can be controlled by a seeding layer with $\langle 100 \rangle$ orientation preference.

Ultra-Low Temperature Process

- Large poly-Si grains are successfully prepared with excimer-laser crystallization of a sputtered α-Si film at a maximum process temperature of $100°$C. The sputtering parameters are optimized to suppress ablation during excimer-laser crystallization. Residual stress can be used as a figure of merit for structure verification. High compressive stress, which indicates a low Ar content, is advantageous for subsequent excimer-laser crystallization.

- Location-controlled grains with a diameter of 4 μm are prepared by excimer-laser crystallization of sputtered α-Si with the μ-Czochralski process at a maximum process temperature of $100°$C. The step coverage of the sputtered α-Si is improved by back-etching of the grain filter.

- SG-TFTs are fabricated within location-controlled grains at a maximum process temperature of $100°$C. Gate oxides deposited at $80°$C (by ICPECVD) are comparable to thermally grown oxides. TFTs fabricated in location-controlled grains are high-performance devices with an electron field-effect mobility of 290 $cm^2/V{\cdot}sec$ and a subthreshold slope of 0.49 V/dec.

7.2 Recommendations

Based on the above conclusions, some recommendations are given for further research:

- The seeding layer, produced by multiple-shot excimer-laser crystallization, shows a clear $\langle 100 \rangle$ surface and a weak $\langle 100 \rangle$ in-plane orientation preference. The $\langle 100 \rangle$ in-plane orientations are in the directions that are perpendicular and parallel to LIPSS direction. It may be more advantageous if the crystallographic orientation of the poly-Si grains can have much clearer (stronger) three-dimensional preference, not only in the surface orientation (ND), but also in the in-plane orientations (RD and TD).

  This could be realized by better control of the LIPSS formation, and would lead to a $\langle 100 \rangle$ SOI-like poly-Si wafer.

- In the present work orientation preference was investigated only in 30 nm thick α-Si films prepared with multiple-shot excimer-laser crystallization. Layers with other thicknesses should also be tested. The dependence of crystallographic orientation preference on thickness should be investigated. A thicker seeding layer would be better for the preparation of orientation- and location-controlled grains by selective epitaxial growth.

- Using a seeding layer, the orientation of location-controlled grains can be controlled with a 20% efficiency (areal fraction). This proportion should be improved either with a better seeding layer or by using an optimized process.

- SG-TFTs should be fabricated inside orientation- (with improved areal fraction) and location-controlled grains, and the performance and uniformity of SG-TFTs should be tested to confirm the importance of orientation control.
- Back-etching of the grain filter in location-controlled grains produced in an ultra-low temperature process gives rise to extra-rough surfaces. New methods should be considered to improve the step coverage of the grain filter and to reduce the surface roughness.

Appendix A

Effects of a Capping Layer on the μ-Czochralski Process

A.1 Introduction

In this Appendix, we shall analyze the effects of a capping layer on the μ-Czochralski process. The original motivation for applying a capping layer in the μ-Czochralski process was to study its thermal effects on defect reduction (Chapter 3). It was found that the capping layer does not significantly reduce the number of defects (Section 3.1). Below we shall examine the effects of a capping layer on the grain size and on the suppression of agglomeration.

The location of large grains (diameter: 7 μm, see Fig. 1.3) is successfully controlled in the μ-Czochralski process. A further increase in grain size and an improvement in crystal quality are expected to open the way to more flexible circuit design and higher device uniformity, respectively.

The grain size increases when a capping layer of optimum thickness is applied, whereas it decreases when the applied capping layer is too thick or too thin. The mechanism of grain enlargement is discussed in the next section, in terms of the heat-reservoir effect of a capping layer during the solidification of molten Si after excimer-laser irradiation.

The analysis of grain enlargement reveals that the capping layer effectively suppresses agglomeration/ablation induced by high-energy excimer-laser irradiation. This is discussed in detail in Section A.3.

The enlargement of grains is due to the heat-reservoir effect – the capping layer stores heat during laser irradiation, and returns it to the Si layer with a delay –, and not to the suppression of agglomeration. The latter only provides a wider energy density window, enabling the irradiation of the CL/α-Si stack at a higher energy density. Increasing the energy density can compensate for some of the heat lost in the capping layer during laser irradiation. However, high energy density does not directly give rise to larger grains

(Fig. 1.3).

A.2 Grain Enlargement

A.2.1 Introduction

How large should location-controlled grains be? The answer is simple: the bigger, the better. A large grain provides more freedom for circuit design – for example, TFT-based CMOS can be designed in one large grain, which can improve the uniformity and reliability of integrated circuits. Furthermore, large grains may feature low defect density because of the low solidification rate that is necessary for grain enlargement.

Location-controlled grains can be enlarged by substrate heating or by increasing the laser fluence [104]. Substrate heating and high laser fluence prolong solidification after laser irradiation. However, substrate heating is limited by the resistance temperature of the glass or plastic substrate. Grain size increases with laser fluence, however, it saturates at a certain level (Fig. 1.3). Laser fluence is also limited by agglomeration of the Si layer.

A SiO_2 capping layer on top of α-Si was reported to effectively enlarge poly-Si grains during excimer-laser crystallization [63, 64]. The capping layer acts as a heat reservoir, returning the stored heat to the Si layer with some delay [49, 63]. Viatella et al. [38] reported that the capping layer can promote uniform grain growth during excimer-laser crystallization.

In this section, we discuss the experiments and numerical simulations performed to study the effects of a SiO_2 capping layer on excimer-laser crystallization of α-Si films in the μ-Czochralski process. The capping layer acts as a heat reservoir during excimer-laser irradiation, and returns the stored heat to the molten Si pool. The returned heat decreases the temperature gradient and extends the solidification phase, and hence enlarges the grains.

Grain enlargement by a capping layer is a simple method that is not limited by substrate materials. However, the capping layer needs an extra deposition step – unless it is used as gate oxide.

A.2.2 Materials and Methods

Experimental details are discussed in Section 3.1.2. The experimental configuration is shown in Fig. 3.1.

A.2.3 Experimental Results

Figure A. 1 shows the average grain diameter (D) as a function of laser fluence (E_l) for each capping layer thickness (T_{CL}). This figure also indicates that a CL prevents ablation of the α-Si layer, that is, the threshold energy density of ablation is increased by the application of a capping layer. The ablation of α-Si occurs at about 1400 mJ/cm^2 for

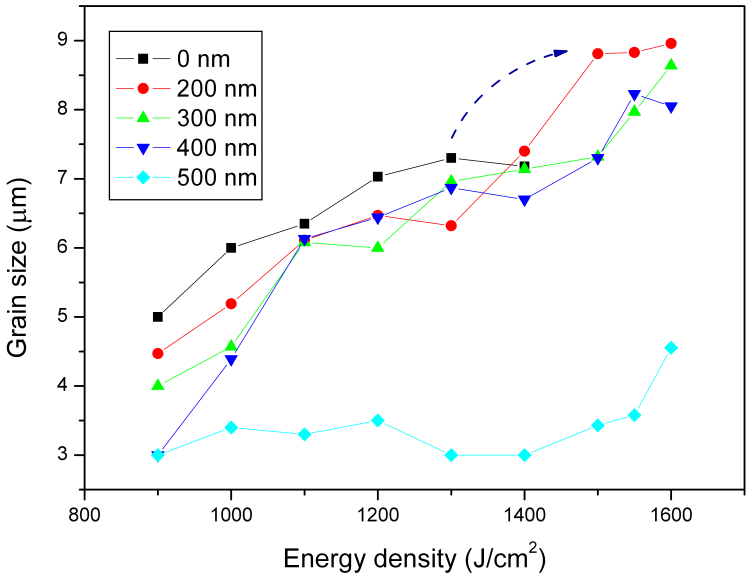


Figure A. 1: Variations of the grain size with the energy density (E_l) for several values of T_{CL}. Because of ablation, an α-Si film without a CL cannot withstand an energy density in excess of 1400 mJ/cm^2 – however, E_l can be higher, up to 1600 mJ/cm^2 for capped samples.

samples without and at about 1600 mJ/cm^2 with a capping layer. Effects of a capping layer on ablation or agglomeration will be discussed in detail in the next section.

Owing to the suppression of ablation by a capping layer, α-Si can be crystallized at a higher energy density, and larger grains can be grown from grain filters than for uncapped samples. Without a capping layer D has its maximum at 7 µm for a laser energy density of 1300 mJ/cm^2; the latter cannot exceed 1400 mJ/cm^2 because of ablation. With a 200 nm thick capping layer, D increases to a maximum of 9 µm at 1600 mJ/cm^2, while for a 300 nm thick capping layer it occurs at 1600 mJ/cm^2 – before the grain size reaches a maximum. For a 500 nm thick capping layer the grain size is substantially smaller. A capping layer that is thinner than 400 nm acts as a heat reservoir, favoring larger grains, whereas a capping layer thicker than 500 nm acts as a heat sink, and thus decreases the average grain size.

A.2.4 Numerical Simulations

One-dimensional numerical simulations of transient heat transfer are performed using the finite-element method (FEM) based on the equations of heat conduction and phase transformation (solid/liquid) with the emission or absorption of latent heat; for details see Section 2.3.

The heat of the laser pulse, $S_{\mathrm{L}}(x,t)$, is incident on the surface of the SiO_2 capping layer. Since the capping layer is assumed to be transparent for excimer laser light due to its negligible absorption, it is effectively the α-Si surface that is irradiated from $t = 0$ to 50 ns [Eq.(2.7)].

T_{CL} used in the simulation is an even multiple of the thickness of the quarter-wave film,

$$T_{\mathrm{CL}} = 2k\frac{\lambda}{4n}, \tag{A. I}$$

where λ is the wavelength of the excimer laser light, n is the refractive index of the capping layer, and k is a positive integer. The reflectivity R of the capping layer is assumed to be the same as for α-Si [109]:

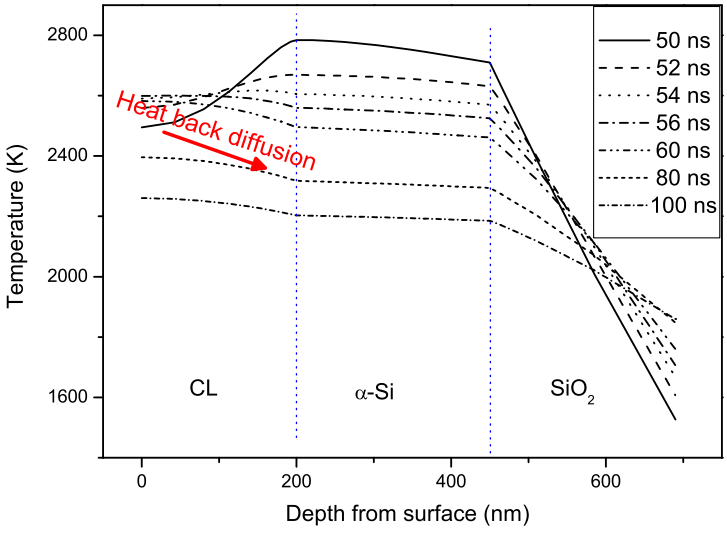
$$R_{\mathrm{CL}} = R_{\alpha\text{-Si}}. \tag{A. II}$$

Anti-reflection effects of the capping layer are neglected in this simulation. The dependence of the reflectivity of the capping layer on its thickness is also ignored, i.e., only thermal effects of the capping layer are discussed. More details about the model can be found elsewhere [110]. Anti-reflection effects of the capping layer are discussed in [53].

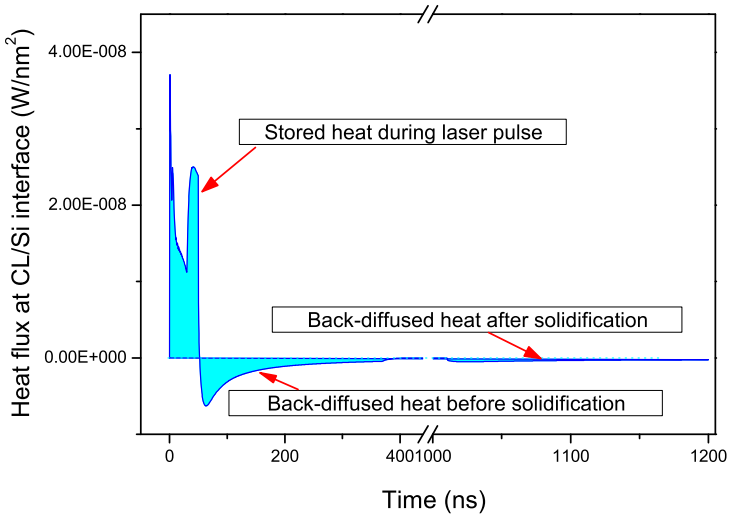
Heat Transfer in the Capping Layer

Figure A. 2(a) shows the time-dependent temperature profiles of the capping layer, α-Si film, and underlying SiO_2 layer after laser irradiation. Although the SiO_2 capping layer does not absorb a considerable amount of energy from the laser light optically, it absorbs thermal energy by conduction from the underlying molten pool. Heat diffusion to the capping layer can be observed in Figure A. 2(b), where the heat flux at the CL/α-Si interface is shown.

The surface of α-Si reaches its maximum temperature at the end of the laser pulse ($t = 50$ ns). The temperature of the liquid Si decreases during cooling due to heat transfer to the substrate and the capping layer. At $t = 54$ ns the temperature of the liquid Si surface becomes lower than that of the surface of the SiO_2 capping layer; the heat stored in the capping layer starts to diffuse heat back to the molten pool of Si; see the part $t > 54$ ns in Figure A. 2(b). However, the back-diffusion of heat stops between $t = 369$ ns and $t = 1010$ ns: during this period, the heat loss in the substrate is exactly balanced by the release of latent heat in the film. This is due to solidification, which keeps the temperature of Si almost constant. After solidification the heat stored in the capping layer diffuses back again to the Si layer. Thus, the back-diffusion of heat from the capping layer can be divided into two phases: before and after solidification. The former is useful for the enlargement of grains, while the latter has negligible impact on the growth process. Therefore, the effectiveness of a capping layer depends not only on the amount of heat that diffuses back to the molten pool but also on the time evolution of heat diffusion.



(a)



(b)

Figure A. 2: Heat transfer of a 200 nm thick capping layer at 1400 mJ/cm^2: (a) time-dependent temperature profiles of the CL, α-Si, and underlying SiO_2 layer; (b) heat flux at the bottom surface of the CL (CL/α-Si interface).

Effects of the Capping Layer Thickness (T_{CL})

As described above, the heat loss in the capping layer ($E_{\text{Loss-CL}}$) before solidification has no influence on the solidification of the molten Si. $E_{\text{Loss-CL}}$ is determined by the difference between the amount of stored heat in the capping layer during the laser pulse (in the period from 0 to 50 ns) and the amount of back-diffused heat before solidification (in the period from 50 to 369 ns), as shown in Fig. A. 2(b). To compare capped and uncapped samples, $E_{\text{Loss-CL}}$ has to be subtracted from E_{l} to maintain equal net energy inputs to the α-Si layer. The effective energy density E_{eff} for α-Si is then defined as

$$E_{\text{eff}} = E_{\text{l}} - E_{\text{Loss-CL}}/(1-R) \qquad \text{(A. III)}$$

where $E_{\text{Loss-CL}}/(1-R)$ is the normalized energy density of the laser pulse before reflection.

Figure A. 3 shows the temperature profiles of a sample with a 200 nm thick capping for $E_{\text{l}} = 1400\text{mJ/cm}^2$; E_{eff} corresponds to $E_{\text{l}} = 1067\text{mJ/cm}^2$ for a sample without a capping layer. In Fig. A. 3 the temperature profiles of a sample without a capping layer are shifted to a depth of 200 nm for comparison. For the same E_{eff} the maximum temperature in the uncapped sample is about 60 K higher than in the sample with a capping layer however the temperature gradient (∇T) of SiO_2 at the bottom interface (Si/SiO_2) is almost the same in the two samples at the end of the laser pulse ($t = 50$ ns). During cooling, ∇T decreases in both cases, however ∇T is lower with the capping layer than without it. This is because the heat diffusing from the capping layer to the molten Si propagates further into the underlying SiO_2 layer and eventually decreases ∇T in the underlayers [Fig. A. 2(b)]. The solidification rate of the liquid is proportional to the rate at which latent heat is removed. This indicates that growth from the liquid phase is determined by the thermal flux to the substrate, which depends on ∇T in the underlayers. The larger the temperature gradient the shorter the solidification period, and eventually, the smaller the grain. Thus, the capping layer suppresses the quenching rate in this case.

As shown in Fig. A. 2(b), the SiO_2 capping layer returns only part of the stored heat to the molten Si before solidification, and releases the rest well afterwards ($t > 1010$ ns). The effects of the capping layer therefore depend on the involved time scale, which in turn depends the thickness T_{CL}. To discuss the effects of T_{CL} on solidification, E_{l} is considered constant (1400 mJ/cm^2). As shown in Fig. A. 4(a), for larger values of T_{CL} more energy is stored in the capping layer. However, the amount of heat that diffuses back from the capping layer to the molten pool before solidification decreases.

Figure A. 4(b) shows the solidification duration and the temperature gradient ∇T for SiO_2 at the bottom interface of the molten Si (Si/SiO_2) as functions of T_{CL}. For T_{CL} increasing from 0 to 200 nm ∇T decreases – that is, the solidification period is prolonged. It is longest for a 200 nm thick capping layer – in good agreement with the experimental finding that the grain size is largest for a 200 nm thick capping layer.

In the T_{CL} range from 200 to 500 nm ∇T increases – hence, the solidification duration decreases. This is again in agreement with experiments that record a decrease in the grain size beyond $T_{\mathrm{CL}} = 200$ nm. For $T_{\mathrm{CL}} = 500$ nm, the solidification duration is

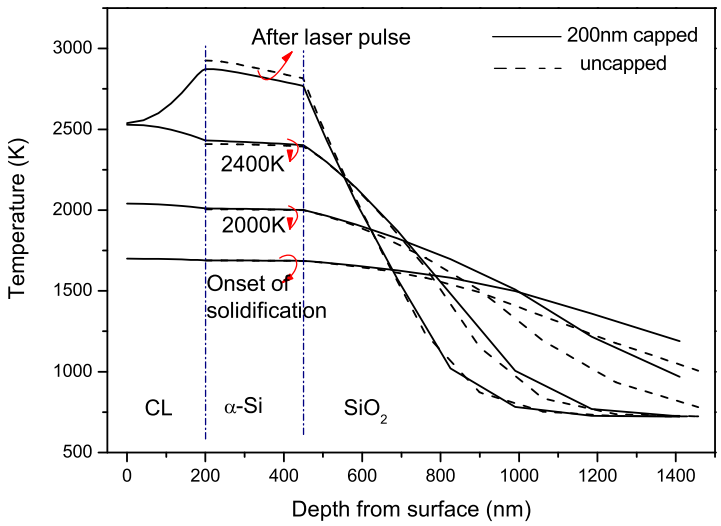


Figure A. 3: Temperature profiles of α-Si films with and without a capping layer for the same input E_{eff}. Dotted line: without capping layer at 1067 mJ/cm^2; straight lines: 200 nm thick capping layer at 1400 mJ/cm^2.

shorter than for samples without a capping layer, and the grain is also smaller. That is, for $T_{\text{CL}} \geq 500$ nm, the capping layer acts as a heat sink rather than a heat reservoir.

A.2.5 Summary

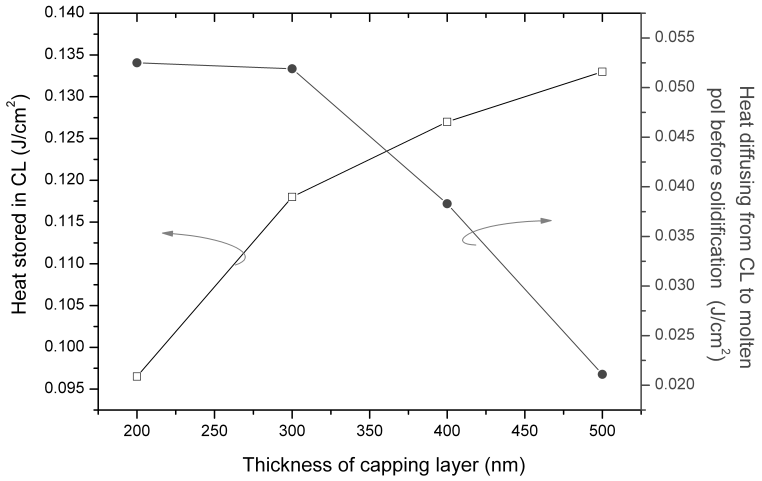
In this section effects of the capping layer on grain growth in the μ-Czochralski process were investigated in experiments and numerical simulations.

Experimentally, grains are enlarged by the introduction of a capping layer in the μ-Czochralski process. With a 200 nm thick capping layer, grains are enlarged to 9 μm, however the grain size decreases for thicker capping layers ($T_{\text{CL}} > 400$ nm).

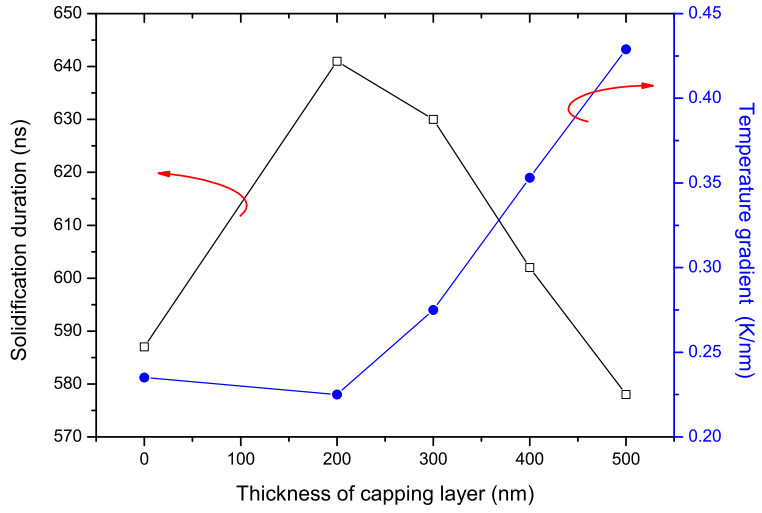
Numerical simulations support experimental results. Effects of the capping layer and their dependence on the thickness are explained in terms of an effective energy density (E_{eff}) defined for the α-Si film. For the same E_{eff}, the capped sample has a longer solidification duration because of its lower heat extraction rate. This is due to the low temperature gradient (∇T) of the underlayers, which in turn is the consequence of the diffusion of heat from the capping layer to the molten pool and the underlying SiO_2 layer.

The application of a capping layer in the μ-Czochralski process is an attractive method for enlarging location-controlled grains, even though the capping layer does not significantly reduce the number of defects (Chapter 2).

Observations also show that the capping layer suppresses ablation/agglomeration



(a)



(b)

Figure A. 4: Variations of the thermal parameter with T_{CL} at 1400 mJ/cm^2. (a) Heat stored in the CL during laser irradiation and back-diffused heat before solidification. (b) Solidification duration of the molten pool and temperature gradient (∇T) of the Si/SiO_2 interface at the onset of solidification. E_{eff} is the same for uncapped ($T_{\mathrm{CL}} = 0$ nm; 1067 mJ/cm^2) and capped ($T_{\mathrm{CL}} = 200$; 1400 mJ/cm^2) samples.

(Fig. A. 1). Suppression of agglomeration grants a wider energy density window, enabling the irradiation of the CL/α-Si stack at a higher energy density, and compensating for the heat lost in the capping layer. The suppression of ablation/agglomeration will be discussed in detail in the following section.

A.3 Agglomeration and Ablation

A.3.1 Introduction

Agglomeration is an important phenomenon in excimer-laser crystallization but the driving mechanisms are far from well understood. In this section we shall investigate agglomeration in detail, and discuss the effects of a capping layer on agglomeration.

The upper limit of the energy density for conventional excimer-laser crystallization is the threshold of complete melting, which initiates superlateral growth, and yields poor uniformity of the grain size [45]. The upper limit for location-controlled methods, such as the grain filter method, is agglomeration; up to this point (in the near-agglomeration region) large grains can be obtained [111]. This threshold is higher than for conventional excimer-laser crystallization. However, the mechanism of agglomeration is not well understood, and the energy density for the onset of agglomeration is still not clearly defined.

Agglomeration is a type of serious damage because it creates holes in the active film or breaks the film into droplets or stripes, making it discontinuous. The diameter of the holes varies from a few micrometers to a few tens of micrometers – i.e., it is much larger than the scale of TFTs. Furthermore the holes are randomly distributed. Layers in which agglomeration occurs are no longer suitable for TFT fabrication. To prevent agglomeration and to optimize the process it is imperative to understand the underlying mechanisms and to identify its onset.

Ablation is a similar damage to the Si layer: an excessive agglomeration that occurs at a much higher energy density, stripping off parts of the film and leaving nothing behind. It was first thought that ablation was the highest limit of energy density, however, according to experiments, it is agglomeration. It is well understood [112,113] that ablation is caused by the explosive boiling or explosive transformation of the superheated liquid into a mix of particles or droplets and vapor that are subsequently ejected from the film.

Agglomeration was also observed in zone-melting techniques [114] used for recrystallizing encapsulated silicon films; in such cases, molten silicon tends to bead up. A SiO_2 capping layer can efficiently prevent agglomeration during zone-melting recrystallization [115]. Recently, SiO_2 CLs have been used to suppress agglomeration in thin metallic films during pulsed laser melting [116]. In this section we shall investigate how the agglomeration of α-Si films during excimer-laser crystallization is affected by the application and thickness of a capping layer.

We shall also determine phenomenologically how agglomeration depends on the energy density of the laser pulse. First, α-Si films are studied using an optical microscope and SEM. The agglomeration threshold is defined by extrapolating the hole density vs.

laser energy density function. Then the effects of the capping layers on agglomeration are discussed. Finally, some agglomeration mechanisms are presented and a consistent model is proposed.

A.3.2 Materials and Methods

A 750 nm thick oxide layer is formed by wet oxidation of a silicon wafer at $1100°C$. Then a 250 nm thick α-Si film is deposited on the SiO_2 layer by decomposition of pure silane gas in a horizontal hot-wall LPCVD furnace. Finally a SiO_2 capping layer is deposited on the α-Si film by decomposition of the TEOS at a temperature of $350°C$ in a PECVD reactor. The thickness of the SiO_2 capping layer (T_{CL}) varies from 0 to 500 nm in 100 nm steps.

These stacked layers are irradiated with a single pulse of XeCl excimer laser (XMR 7100 laser system). The energy density (E_l) ranges from 1200 mJ/cm^2 to the ablation threshold of α. The wafer is heated up to $450°C$.

The morphology of the agglomerated or ablated films is analyzed by an optical microscope (Axiotron 2). Photos of the films are taken with a confocal scan module. The holes created by agglomeration are counted and then the hole density (I) is calculated for each value of E_l. The onset of agglomeration is determined by extrapolating the I vs. E_l function. Further investigation is performed by SEM (Philips FEI XL50) after the removal of the capping layers by immersing the wafer into 7:1 buffered HF (BHF) solution.

A.3.3 Results

Agglomeration of the α-Si Film

Figure A. 5 shows optical images of agglomeration and ablation in a 250 nm thick α-Si film without a capping layer. In an initial stage of agglomeration, round and widely spaced isolated holes appear in the Si layer at $E_l = 1385$ mJ/cm^2 [Fig. A. 5(a)]. The hole density increases with increasing E_l, and at 1511 mJ/cm^2 holes cluster together; neighbors are separated by a straight wall [Fig. A. 5(b)]. At 1793 mJ/cm^2 [Fig. A. 5(c)] the walls between the holes break into the beads, and the vestiges of the walls become visible. At 1893 mJ/cm^2 [Fig. A. 5(d)] the silicon beads disappear in the bare area, and eventually no silicon remains on the surface of the underlying SiO_2 layer. This is the point where ablation occurs. These observations confirm that agglomeration continuously evolves into ablation when the energy density of the laser pulse is increased.

The agglomeration process described above is investigated by SEM. Figure A. 6 shows SEM images of agglomeration and ablation in α-Si films. At 1511 mJ/cm^2 [Fig. A. 6(a)] high ridges at the hole edges indicate a boiling process that expands the Si vapor and drives molten Si to the edge of the bubble, giving rise to a thicker rim. The wall between two neighboring holes is almost perpendicular to the SiO_2 substrate. At 1793 mJ/cm^2 [Fig. A. 6(b)] a part of the film is ablated, and ablated regions are surrounded by agglomeration margins. Figure A. 6(c) shows individual beads that are solidified from

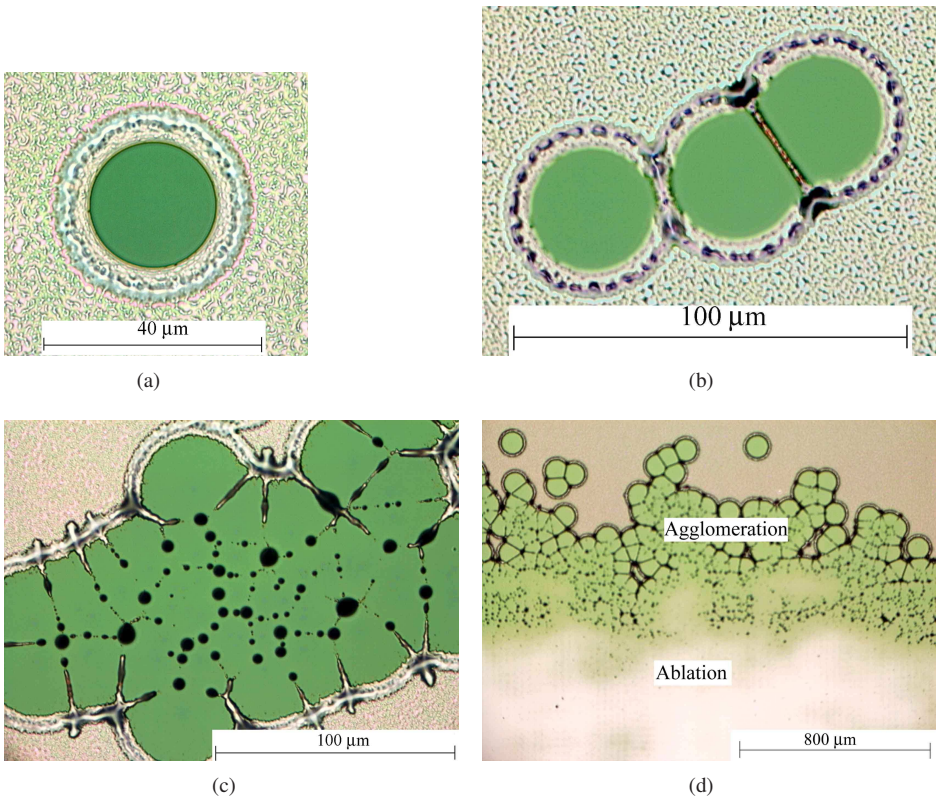


Figure A. 5: Optical images of agglomeration in α-Si films irradiated with an energy density of (a) 1385 mJ/cm^2; (b) 1549 mJ/cm^2; (c) 1793 mJ/cm^2; (d) 1893 mJ/cm^2.

the droplets of molten Si. The diameter of the beads (about 2 μm) is much larger than the thickness of the α-Si film. Spherical beads [Fig. A. 6(c)] and vertical walls [Fig. A. 6(a)] indicate that the contact angle between molten Si and the underlying SiO_2 surface is larger than 90°, which implies poor wetting. The large ratio of the bead diameter to the thickness of the α-Si layer indicates that a high energy is required to overcome the energy barrier of the formation of large beads. Wall and bead formation may be thermodynamically related to the poor wetting property of molten silicon on the SiO_2 surface.

Figure A. 7 shows optical images of irradiated α-Si films with a 100 nm thick capping layer. At low energy densities ($E_l = 1441$ mJ/cm^2) agglomeration of the α-Si film occurs [Fig. A. 7(a)], and cracks or punctures appear in the capping layers. These seem to be channels through which inflated vapor can escape. At larger energy densities [Fig. A. 7(b)] the α-Si film undergoes ablation, and the capping layer is broken and splashed away.

As is well known, material is expelled in ablation. This expulsion is confirmed by experiments performed on an α-Si film with a thick capping layer (Figure A. 8). The ablation of the α-Si film is relatively weak at 1941 mJ/cm^2 [Fig. A. 8(a)]: the capping layer is not yet broken just tumefied due to the volume expansion of vapor bubbles. The droplets, ejected from the molten pool, are projected to the bottom surface of the tumefied CL. At 2046 mJ/cm^2 [Fig. A. 8(b)] the capping layer breaks and Si is splashed away in a violent ejection of droplets, leaving radial cracks in the capping layer at the edges of the ablated region.

Agglomeration Threshold

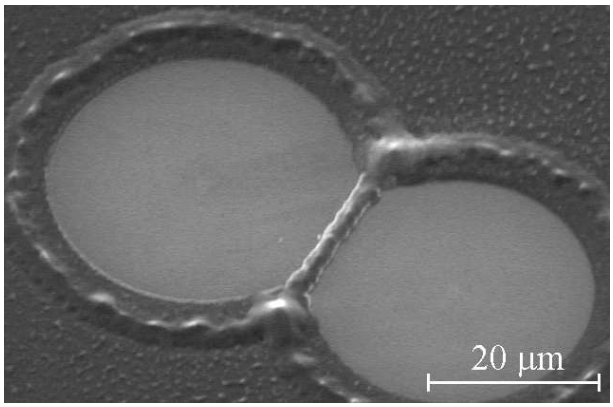
Figure A. 9(a) is a semi-logarithmic plot of the I against E_l, for each value of T_{CL} used in the experiments. The straight lines indicate that the hole density increases exponentially with E_l. With respect to the uncapped sample, curves for 100, 200, and 300 nm thick capping layers are shifted to higher energy densities and their slope are almost equal. However, for 400 and 500 nm thick capping layers the slope decreases, which indicates that the hole density is less sensitive to E_l. Thus, thin ($T_{CL} \leq 300$ nm) and thick ($T_{CL} > 300$ nm) capping layers affect the agglomeration of the Si films differently.

Assuming that each vapor bubble nucleus at the interface between the molten Si and the underlying SiO_2 (L_{Si}/S_{SiO_2}) grows into a hole (see under point 3 in Section A.3.4), the hole density must be equal to the density of vapor bubble nuclei, which is a function of the excess free energy (ΔG) of molten Si [44] (hence approximately the energy absorbed during laser irradiation, E_l). Therefore, the number of holes on a unit area (I)is given by

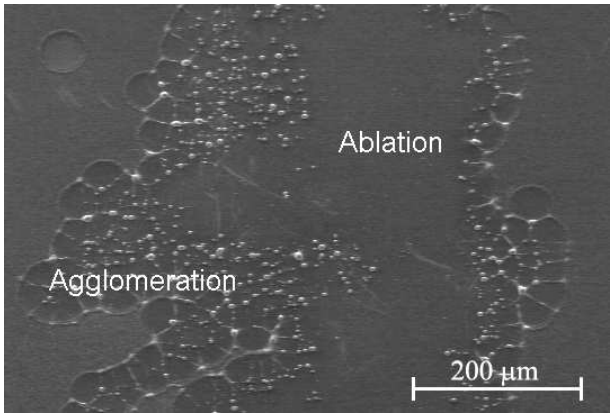
$$I = \mu_0 \exp\left(\frac{-\Delta G}{kT}\right) = \nu_0 \exp\left(\frac{E_l}{kT}\right), \qquad \text{(A. IV)}$$

where μ_0 and ν_0 are constants, k is Boltzmann's constant, and T is the temperature of molten Si.

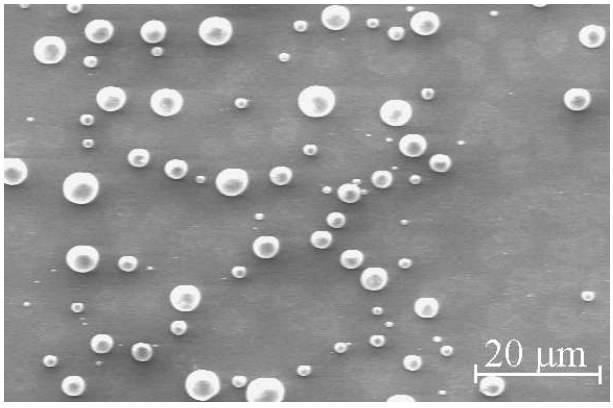
The agglomeration threshold E_{agg} is crucial for the optimization of excimer-laser crystallization. E_{agg} is defined as the energy density where the first hole in a laser spot



(a)

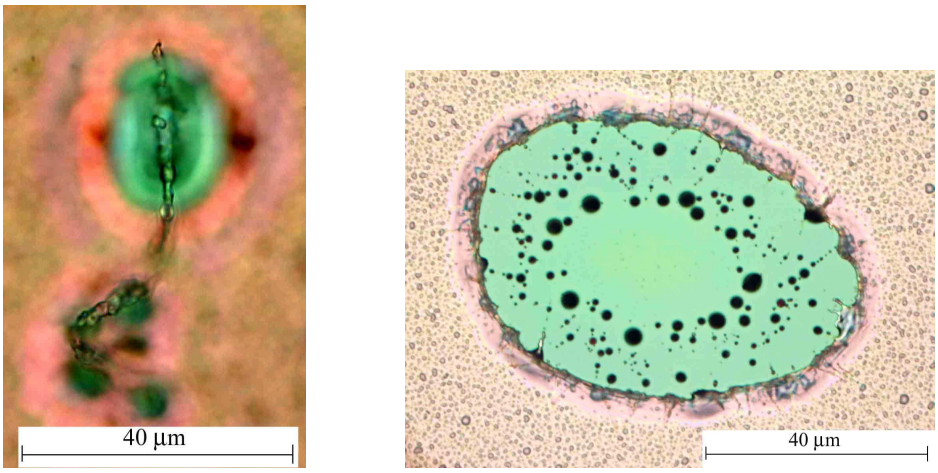


(b)



(c)

Figure A. 6: SEM images of the agglomeration in α-Si films irradiated with an energy density of (a) 1511 mJ/cm^2 and (b) 1793 mJ/cm^2. Part (c) shows the high-resolution image of the round silicon beads in (b). The sample is tilted by 30°.



(a) (b)

Figure A. 7: Agglomeration of α-Si films with a 100 nm thick CL at an irradiation energy density of (a) 1441 mJ/cm ^{2}, (b) 1793 mJ/cm^2.

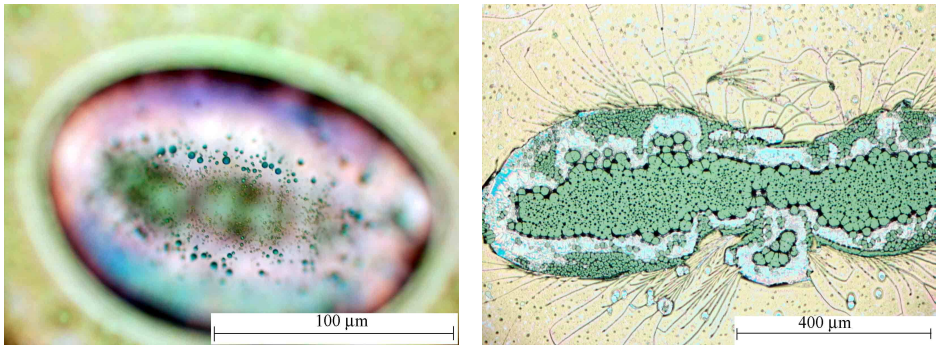
(5.5 mm $\times$ 6 mm) appears; it is determined by extrapolating the I vs. E_l function:

$$\ln I = \ln \frac{1}{5.5 \times 6} = -3.5, \qquad \text{(A. V)}$$

shown by the horizontal dashed line in Fig. A. 9(a).

Figure A. 9(b) shows the strong dependence of E_agg on CL thickness for 250 nm thick α-Si films. Experimentally, the hole density increases with T_CL up to 300 nm. For thicker CLs the hole density decreases significantly, and the initial agglomeration occurs at a very low E_l. Due to heat conduction from the Si layer to the CL during laser irradiation, thick capping layers require more energy than thinner ones to reach the same temperature [117]. To investigate the suppression of agglomeration by a thin capping layer ($T_\mathrm{CL} \leq 300$ nm), heat loss in the capping layer is calculated in one-dimensional numerical simulations of the transient heat transfer. The heat loss is then deduced from the agglomeration threshold (E_agg) obtained above, and is used to compare the calculated energy density with the experimental value.

Further details of the simulation are given on page 24. Simulated data are also shown in Figure A. 9(b). The heat loss in the capping layer is the difference between experimental and simulated data, which becomes larger for thicker capping layers. However, fitted simulation data still indicate the suppression effects of thin capping layers. Consequently, E_agg is reached at higher values of E_l when a thin capping layer is applied, which widens the process window.



(a) (b)

Figure A. 8: Agglomeration of α-Si films with a 400 nm thick capping layer at (a) $E_l = 1941$ mJ/cm^2; (b) $E_l = 2046$ mJ/cm^2.

A.3.4 Discussion

Preventing the agglomeration of molten Si is important for excimer-laser crystallization at high energy density. However, the mechanism of agglomeration is still far from well understood. Below we present three possible explanations, and then propose a more rational alternative.

1. **Surface fluctuation**

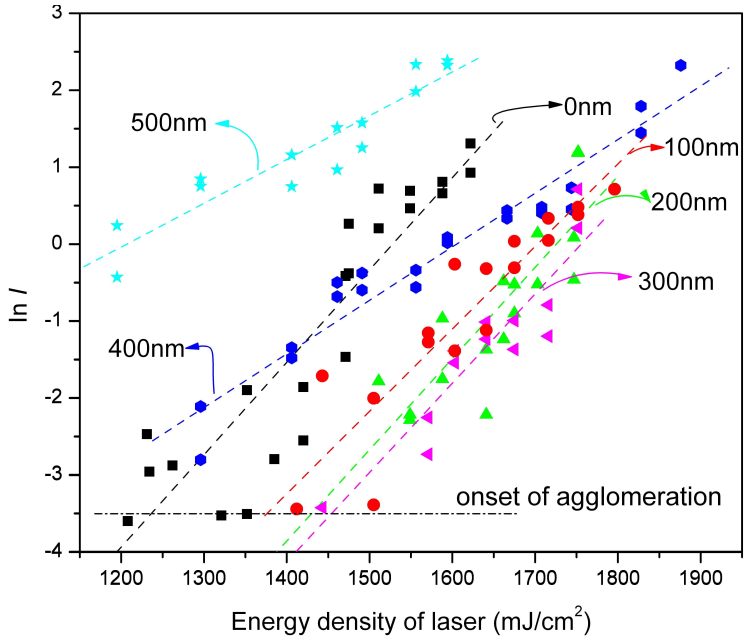
   Agglomeration occurs at a higher energy density than the formation of surface ripples. It was assumed [104, 118] that fluctuations in the surface properties lead to thickness variations of the liquid film, and agglomeration starts when the film is thin enough to break. However, surface ripples are always aligned, and there are no signs for the alignment of the holes: observations show that they are randomly distributed.

2. **Normal boiling**

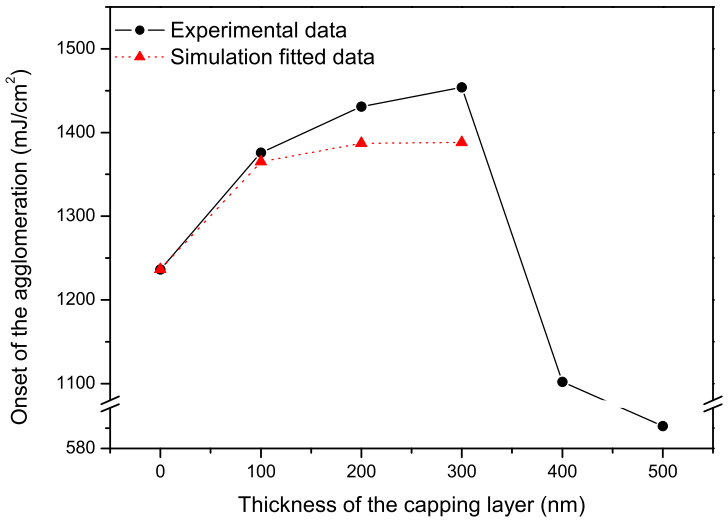
   Since ablation is excessive agglomeration and occurs through explosive boiling, it is logical to conclude that agglomeration is caused by normal boiling. In this process [119], vapor bubbles nucleate *heterogeneously* from a variety of disturbances – such as gaseous or solid impurities, defects, or interfaces. The bubbles diffuse toward the outer surface and burst. However, it was proposed [120] that normal boiling is never dominant on the short (µs) timescale of the laser pulse because of the prohibitive kinetics of the slow diffusion of bubbles.

3. **Boiling, Thermodynamically Promoted by Dewetting**

   The "normal boiling" theory neglects the wetting properties of molten silicon on a SiO_2 surface. However, the L_{Si}/S_{SiO_2} interfacial energy is important for the



(a)



(b)

Figure A. 9: (a) The number of hole on a unit area (I) as a function of the laser energy density E_l, for each value of T_{CL} used in the experiments. (b) Agglomeration threshold, E_{agg}, as a function of T_{CL}. Dashed lines in (b) show mark data for $T_{CL} \leq 300$ nm as per [117].

nucleation of the vapor bubble and its subsequent mobility. Figure A. 10 shows schematically the course of nucleation, growth, and burst of a single vapor bubble. The dewetting property tends to pull a molten silicon film apart, expand the vapor bubbles, uncover the substrate, and promote the nucleation and diffusion of vapor bubbles. In other words, a vapor bubble arising from heterogeneous nucleation at the interface (L_{Si}/S_{SiO_2}) expands easily. When it grows beyond the outer surface of molten Si, it bursts, leaving holes in the film.

Agglomeration does not occur in completely molten Si for $E_l < E_{agg}$, which indicates that poor wetting is not a sufficient driving force in itself for agglomeration. The nucleation of vapor bubbles initiates dewetting, and is therefore the ultimate cause of agglomeration. Nucleation starts when molten Si has sufficient excess free energy – that is, when $E_l > E_{agg}$. The density of nucleated vapor bubbles is a function of E_l, quantitatively shown in Fig. A. 9(a).

Agglomeration is therefore due to bursting vapor bubbles. The process – including the nucleation of vapor bubbles and their growth till burst – is thermodynamically promoted by the poor wetting properties of molten Si on the SiO_2 film. This could explain why interfacial nitrogen can decrease surface tension and suppress agglomeration [121], and why the presence of hydrogen can induce it [114, 119].

The enveloped vapor bubble bursts [Fig. A. 10(c)] when the interior pressure exceeds the ambient pressure. The capping layer acts as a confining layer for the vapor bubble. The bubble does not burst easily, as its interior pressure has to exceed that of the free surface. Higher vapor pressure inside the bubble tends to favor a liquid phase (molten Si) with a smaller specific volume. Therefore, the energy barrier for bubble expansion and for the subsequent nucleation of a new bubble increases, hence for thin capping layers the agglomeration threshold (E_{agg}) increases with the thickness of the capping layer T_{CL} [Fig. A. 9(b)].

However, for thick capping layers E_{agg} decreases with T_{CL} [Fig. A. 9(b)]. The exact reason is not understood yet. It may be due to an extremely high stress stemming from the large disparity in the coefficients of thermal expansion related to the formation of vapor bubbles. Because of the high stress, the capping layer cracks easily, and holes are generated at a low energy density. When an initial hole is formed and a vapor bubble penetrates through the capping layer, the high stress is released by cracks around the hole [Fig. A. 8(b)]. The generation of further holes is less sensitive to the increase in energy density, as indicated in Fig. A. 9(a): the slope is more gentle for thick capping layers than for thin ones.

To recap, agglomeration is an evaporation phenomenon in which vapor bubbles nucleate heterogeneously at the L_{Si}/S_{SiO_2} interface, and are thermodynamically promoted to burst by the poor wetting property of molten Si on the underlying SiO_2. On the other hand, ablation is an explosive process of boiling, in which vapor bubbles nucleate homogenously in a dramatic way, and explode upon the application of a laser pulse of high energy density.

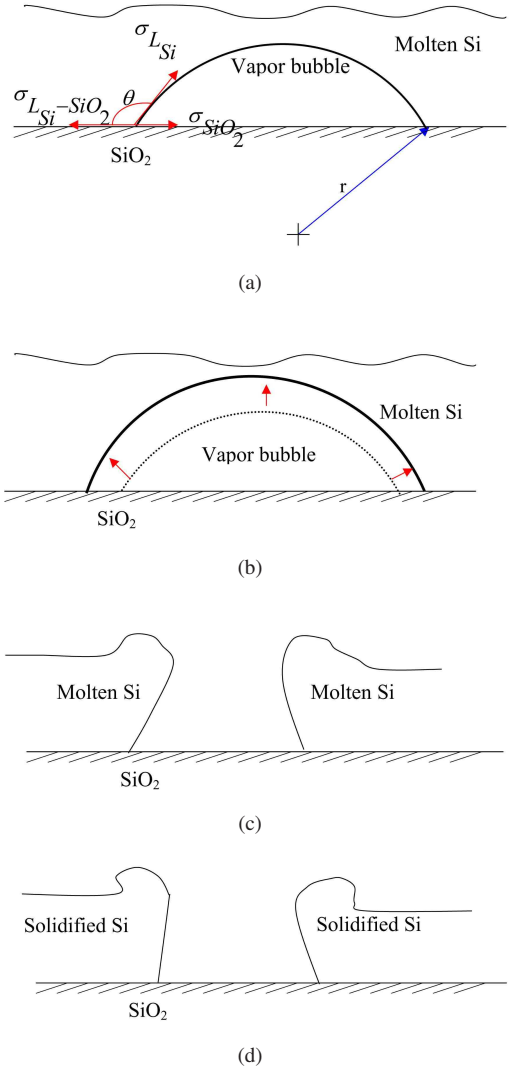


Figure A. 10: Schematic representation of the process of hole formation. (a) Heterogeneous nucleation of the vapor bubble at the L_{Si}/S_{SiO_2} interface. The contact angle between L_{Si} and S_{SiO_2} is larger than $90°$. (b) Growth of the vapor bubble. (c) Burst of the vapor bubble. (d) Solidification of the molten Si.

A.3.5 Summary

In this section we investigated the agglomeration of α-Si films upon excimer-laser irradiation at high energy densities, and discussed how it is affected by the application of a CL.

Agglomeration during excimer-laser crystallization at high energy density causes serious damage to the sample. It first creates holes, which then cluster, forming straight walls. Subsequently, the walls are broken into beads, and finally even the beads are ejected away, and ablation occurs. It is proposed that agglomeration is a process of boiling. Heterogeneously nucleated vapor bubbles burst at the surface of molten Si, and create holes. This process is thermodynamically promoted by the poor wetting property of molten Si on the underlying SiO_2 layer.

The agglomeration threshold (E_{agg}) is defined by extrapolating the hole density (I) vs. laser energy density (E_{l}) function for each thickness of the capping layer (T_{CL}). For thin ($T_{\text{CL}} \leq 300$ nm) capping layers agglomeration occurs at a higher value of E_{l}. A thin capping layer confines bursting vapor bubbles, thus it suppresses agglomeration.

Understanding the mechanism of agglomeration is an important step toward preventing the damage in high-energy-density excimer-laser crystallization. By suppressing agglomeration, thin capping layers widen the energy density window for excimer-laser crystallization, enabling CL/α-Si stacks to be irradiated at higher energy densities. This can compensate for some of the heat lost in the capping layer during laser irradiation.

A.4 Conclusion

The application of a capping layer helps to enlarge location-controlled grains in the μ-Czochralski process.

The precise effects of a capping layer depend on its thickness. For thin capping layers the grain size increases because the layer acts as a heat reservoir; for thick ones the grain size decreases because it acts as a heat sink.

The quality of grains (regarding defects, such as dislocations, faults, twins, grain boundaries, etc.) grown from a grain filter is not considerably improved by the application of a capping layer (Section 3.1).

The applied capping layer could be directly used as gate oxide. Because of the melting of Si, the capping layer is annealed at a high temperature, hence the interface of Si/SiO_2 should be improved. TFTs fabricated with a capping layer have shown much better performance than those without a capping layer [53].

Suppression of agglomeration with a thin capping layer widens the energy density window for excimer-laser crystallization. Using a higher energy density can compensate for some of the heat lost in the capping layer during laser irradiation, and thus the grain size can be increased by the application of a thin capping layer.

By introducing a capping layer in the μ-Czochralski process and optimizing its thickness, location-controlled grain can be enlarged. TFTs fabricated in such grains show considerably improved performance.

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Summary

Title: **Crystallographic Orientation- and Location-Controlled Single Silicon Grains on Amorphous Substrates for Large-Area Electronics**

This thesis is the summary of investigations on single-crystalline location-controlled silicon grains aiming at the fabrication of thin-film transistors (TFTs) on large-area substrates. The goal of the research is to obtain SG-TFTs with electrical characteristics comparable to SOIFETs to realize the entire systems on panel.

Three main issues of single-crystalline location-controlled grains are addressed in this thesis: 1) defect reduction; 2) orientation control; 3) ultra-low temperature process for the fabrication of location-controlled grains. The aim is to improve the quality of single-crystalline location-controlled grains, and at the same time to widen the range of applications for these grains on a plastic substrate.

First, a method for producing location-controlled grains – the μ-Czochralski (grain filter) process – is discussed as a promising technology for future SG-TFT fabrication. Single-crystalline grains can be prepared at predetermined positions with CSL subgrain boundaries inside the grains. The maximum grain size can reach 7 μm. SG-TFTs fabricated in the grains show superior performance (electron field effect mobility: 600 $cm^2/V{\cdot}sec$, off-current: $1.3{\times}10^{-13}$ A, subthreshold swing: 0.21 V/dec.). Certain aspects of this new method – such as defect reduction and crystallographic orientation control – need to be improved; these are addressed in this thesis.

Two approaches are used for defect reduction. In the first one a capping layer is applied on top of the α-Si layer with the grain filter underneath. It is found that the capping layer does not reduce the defects efficiently inside the grains, although it does increase the grain size owing to thermal influence of a capping layer.

In the second approach a seed is introduced at the bottom of grain filter. This reduces the number of defects significantly. With sufficient energy density and substrate heating, single-crystalline grains can be prepared at predetermined positions with the same orientation as the seed. The number of defects generated from $\langle 100 \rangle$-oriented seeds is significantly lower than in the situation of non-$\langle 100 \rangle$-oriented seed.

The crystallographic orientation of grains is the same as that of the seed, which means that the crystallographic orientation of the grains can be controlled by a seeding layer. Controlling the crystallographic orientation of single grains along some preferred direc-

tion would be the ideal solution to improve the performance and uniformity of SG-TFTs.

Using multiple-shot excimer-laser crystallization, the preferred $\langle 100 \rangle$ orientation is observed in self-assembled square-shaped poly-Si grains. The areal fraction of $\langle 100 \rangle$-oriented grains – within 10 degrees of misorientation – exceeds 92%.

This predominantly $\langle 100 \rangle$-oriented poly-Si layer is used as a seeding layer to prepare crystallographic orientation- and location-controlled grains. About 20% of the crystallographic orientation can be controlled by the seeding layer. This is an important improvement that opens the way to preparing orientation- and location-controlled grains. Further improvement can be realized by improving the orientation control of the seeding layer or by optimizing the process.

The recent development of TFTs on plastic substrates requires an ultra-low temperature process for SG-TFTs. By combining excimer-laser crystallization and sputtering, large poly-Si grains can be successfully prepared at a maximum process temperature of $100°$C. In conjunction with the μ-Czochralski process, location-controlled grains with a diameter of 4 μm are prepared. SG-TFTs are fabricated within location-controlled grains at a maximum process temperature of $100°$C. Using ICPECVD, gate oxide can be deposited at $80°$C. TFTs fabricated in these location-controlled grains show high performance, with a field-effect mobility of 290 $cm^2/V{\cdot}s$. This development of IC-quality TFTs at a low process temperature is a promising step toward the fabrication of large-area microelectronics on plastic substrates.

In conclusion, the research and development presented in this thesis lead to the fabrication of crystallographic orientation- and location-controlled single-crystalline grains, which can be used for fabricating high-performance SG-TFTs for large-area microelectronic applications. As a result, peripheral driver circuits as well as system circuits can be integrated on a single substrate, leading to ultra-compact "system-on-panel products" not only on glass but also plastic substrates.

Samenvatting

Titel: **Kristallografische oriëntatie- en locatiegecontroleerde Si éénkristallen op een amorf substraat voor Large Area elektronica**.

Dit proefschrift is een samenvatting van onderzoek naar éénkristal locatie-gecontroleerde silicium granules, die zullen worden gebruikt voor dunne laag transistoren (Thin Film Transistors: TFTs) fabricage op een groot oppervlak substraat. De doelstelling van dit onderzoek is het verkrijgen van SG-TFTs met elektrische eigenschappen vergelijkbaar met die van SOI FETs, die een realisatie van het hele systeem 'on panel' mogelijk maken.

In dit promotiewerk worden drie kernvraagstukken voor éénkristal locatiegecontroleerde granules behandeld: 1) reductie van defecten; 2) oriëntatie beheersing en 3) één ultra-laag temperatuur proces voor de fabricage van locatie gecontroleerde granules. Het doel van dit werk is het verbeteren van de kwaliteit van één-kristallijne locatie gecontroleerde granules en tegelijkertijd het verbreden van het toepassingsgebied van deze granules op een plastic substraat.

Allereerst wordt een methode voor locatie-gecontroleerde granules, μ-Czochralski (grain filter) proces, geïntroduceerd als een van de veelbelovende technologieën voor toekomstige SG-TFTs fabricage. De enkelkristallijne granules kunnen worden vervaardigd op van te voren bepaalde posities met CSL sub-granule boundaries binnen de granules. De maximale granule grootte kan 7 μm zijn. SG-TFTs die in de granules werden gemaakt vertoonden superieure prestaties: elektron veldeffect mobiliteit van 600 cm^2/V·sec, off-current van 1.3×10^{-13} A en subthreshold swing van 0.21 V/dec. Deze nieuwe methode heeft een klein aantal verbeterpunten, zoals defect reductie en kristallografische oriëntatie beheersing, welke behandeld worden in dit werk. Twee benaderingen worden gebruikt voor defectreductie. Eerst een 'capping' laag bovenop een α-Si laag met daaronder de grainfilters. Het blijkt dat een capping-laag niet efficiënt is in het reduceren van defecten in granules, hoewel het wel een toename in granule grootte teweegbrengt ten gevolge van de thermische invloed van deze laag. Een andere benadering is de introductie van een entkristal op de bodem van het grainfilter. Met het entkristal kunnen defecten significant verminderd worden. Met voldoende energiedichtheid en substraat verhitting kunnen éénkristallijne granules vervaardigd worden op een van te voren bepaalde locatie met dezelfde oriöntatie als het entkristal. Het aantal defecten dat wordt gegenereerd van een $\langle 100\rangle$-georiënteerd entkristal is beduidend kleiner dan in de situatie van een niet-$\langle 100\rangle$-

georiënteerde seed. De kristallografische oriëntatie van de granules is dezelfde als die van de seeds, wat betekent dat de kristallografische oriëntatie van de granules geregeld kan worden door de entlaag. Om de SG-TFT prestaties en uniformiteit te verbeteren zou het ideaal zijn dat de kristallografische oriëntatie van een enkele granule geregeld kan worden naar een gewenste oriëntatie.

Na multi-shot excimer laser kristalisatie wordt de $\langle 100 \rangle$ voorkeursoriëntatie waargenomen in zelfgeassembleerde vierkante poly-Si granules. Meer dan 92 procent oppervlakte fractie van de granules heeft de $\langle 100 \rangle$ voorkeursoriëntatie, binnen 10 graden misoriëntatie. Bovengenoemde $\langle 100 \rangle$-voorkeursgeoriënteerde poly-Si laag wordt gebruikt als een entlaag om kristallografisch georiënteerde en gelokaliseerde granules te vervaardigen. Ongeveer 20 procent van de kristallografische oriëntatie kan door de entlaag worden bepaald. Er is een betekenisvolle toename in de kristallografische oriëntatie-voorkeur met een entlaag. In principe kunnen oriëntatie- en locatie gecontroleerde granules vervaardigd worden via deze methode. Verdere verbetering kan gerealiseerd worden met hetzij een perfectere oriëntatie gecontroleerde entlaag hetzij door een meer geoptimaliseerd proces.

Met de recente ontwikkeling van TFTs op een plastic substraat is een ultra-laag temperatuur proces voor SG-TFTs ontwikkeld voor toepassing op een plastic substraat. Door combinatie van excimer laser kristallisatie met sputtering van silicium kunnen grote poly-Si granules met succes worden vervaardigd bij een maximale procestemperatuur van 100^oC. In combinatie met het μ-Czochralski (grainfilter) proces worden locatie gecontroleerde granules vervaardigd met een diameter van 4 μm. SG-TFTs worden gemaakt binnen locatie gecontroleerde granules bij een maximale procestemperatuur van 100^oC. Dankzij ICPECVD kan gate-oxide gedeponeerd worden bij 80^oC. TFTs die in deze locatie gecontroleerde granules zijn vervaardigd vertoonden hoge prestaties met een veldeffect mobiliteit van 290 cm^2/V·sec. Deze ontwikkeling van IC kwaliteit TFTs onder lage procestemperatuur is veelbelovend voor fabricage van groot-oppervlak micro-elektronica op plastic substraten. Ten slotte heeft het onderzoek en de ontwikkeling in dit werk geresulteerd in de fabricage van éénkristallijne kristallografische oriëntatie- en locatiegecontroleerde granules die gebruikt kunnen worden voor high-performance SG-TFTs fabricage van groot-oppervlak micro-elektronische toepassingen. Als gevolg hiervan kunnen perifere driver circuits alsmede systeem circuits geïntegreerd worden op één enkel substraat, hetgeen resulteert in ultra-compacte 'system on panel' producten, niet alleen op glazen, maar ook op plastic sustraten.

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List of Publications

PhD Period

Journal Papers

- M. He, R. Ishihara, J. W. Metselaar and C. I. M. Beenakker, $\langle 100 \rangle$-textured self-assembled square-shaped poly-Si grains by multiple shots excimer-laser crystallization, *J. Appl. Phys.* 100 (2006), p: 83103-1∼5.

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- M. He, E. J. J. Neihof, Y. van Andel, T. Chen, H. Schellevis, R. Ishihara, J. W. Metselaar and C. I. M. Beenakker, Single grain Si TFTs fabricated at $100°$C for microelectronics on a plastic substrate, Mater. Res. Soc. Spring meeting (San Francisco, USA, Apr.2007).

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Patents

- Fabrication method of semiconductor devices, electro-optic devices, integrated circuits and electronic devices. Inventors: Yasushi Hiroshima, Ryoichi Ishihara, Ming He. Japanese Patent No: JP2005353939.
- Fabrication method of semiconductor devices, electro-optic devices and electronic devices. Inventors: Yasushi Hiroshima, Ryoichi Ishihara, Ming He. Application No: JP012141201 (applied by Seiko Epson Corporation in Japan), 2005.