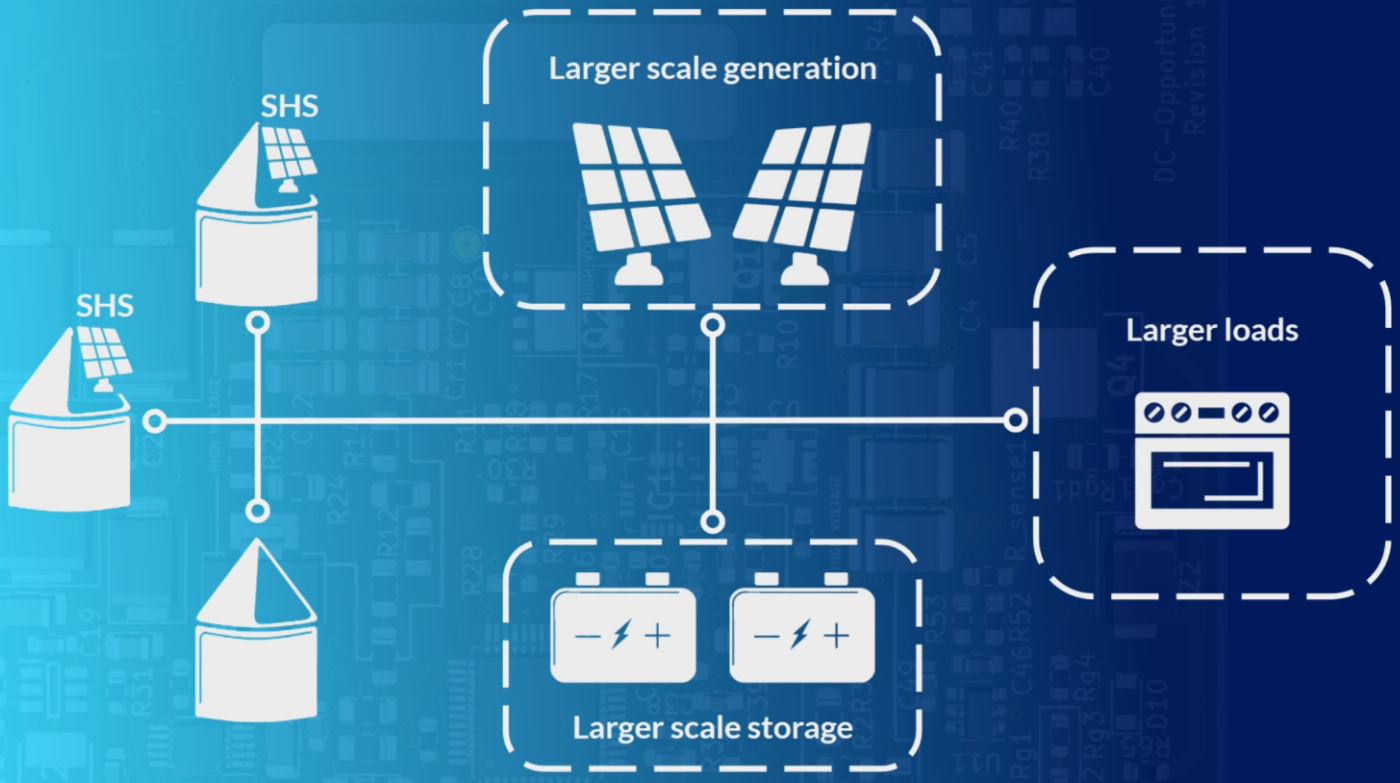
Isolated DC/DC Converters for DC Distribution Grids in Rural Electrification

Jesse Echeverry



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Challenge the future

Isolated DC/DC Converters for DC Distribution Grids in Rural Electrification

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to obtain the degree of Master of Science
in Electrical Power Engineering (EPE)
at the Delft University of Technology.

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An electronic version of this thesis is available at `http://repository.tudelft.nl/`.

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DC pportunities

Acknowledgment

Writing a master's thesis can be described as a difficult task that demands time, dedication, and skill. If one sets ambitious research goals and rises up to meet the challenges, it can be a catalyst for personal growth. I have found, in my experience, that this has been the case. Over the past nine months, I have experienced many things; I have worked on my thesis, observed the effects of the coronavirus pandemic on society, worked with talented individuals, and developed new inspirations for my future work. These recent experiences have convinced me that unification, understanding, and working together to help the Earth and our immediate environments should be my focus moving forward. My personal development and completion of the thesis were only possible because of the unwavering support of my advisors, family, and friends. And to them, I dedicate this work.

This work is dedicated to the following people:

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Jesse Edward Echeverry
Delft, Netherlands
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Abstract

Roughly 840 million people, predominately from rural communities in sub-Sahara Africa, still lack access to electricity. The direct current (DC) microgrid is an emerging grid infrastructure that meshes efficiently with DC based technology such as photovoltaics, batteries, consumer electronics, and electric vehicles. This characteristic of DC microgrids designates them as a preferred solution for new grid infrastructures in rural electrification applications. In order to establish a DC microgrid, power electronic interfaces (PEI) are required for regulating power flow and interconnecting different grid components of the microgrid. In this thesis, the PEI (operating at 200-900 W) connecting a 350 V DC-microgrid to a solar home system (compatible with USB-C) is investigated. A unidirectional half-bridge LLC converter and a bidirectional dual active half-bridge (DAHB) converter (both utilizing gallium-nitride (GaN) transistors and planar transformers (PT)) are designed and tested. A working prototype of the half-bridge LLC converter with a center-tapped secondary is presented and the waveforms at maximum load and no-load conditions are analyzed. A complete design and efficiency approximation for a DAHB converter with a center-tapped secondary and active snubber circuits is included. In addition, simulations (in PLECS) of the designed DAHB converter provide waveform results for both the forward and reverse power flow direction. The results of the work discuss how high frequency operated, half-bridge isolated DC/DC topologies with GaN transistors and planar transformers are an excellent composition of technology for these rural electrification applications. The GaN transistor is most effective in a low voltage (up to 650 V), high performance scheme, and offers inherent benefits which allow for high frequency operation and thus, smaller passive components. Moreover, the effect of current collapse (an adverse effect in GaN transistors) is discussed and analyzed from a design standpoint. The benefits of planar transformers in low-medium power (up to 900 W) rural electrification applications and an in-depth PT design process are presented. Additionally, rural electrification safe extra-low voltage (SELV) standards require that PT designs must have reinforced (or double) isolation between primary and secondary windings. Taking this into consideration, two proposed PT configurations using a U-core and planar E-core, respectively, are compared. The main conclusions of this work aim to bridge the gap for the design and implementation of efficient **DC microgrid variable power output converters** for use in rural electrification applications.

Keywords: Rural Electrification, DC Microgrid, Half-bridge LLC, Dual Active Half-bridge (DAHB), GaN Switching, Current Collapse, Planar Transformers, Safe Extra-low Voltage (SELV)

Contents

Nomenclature

η	Efficiency
μ	Total permeability of a material
μ_o	Permeability of free space
μ_r	Relative permeability of a material
Φ	Phase shift
ϕ	Flux
ρ	Resistivity
τ_{dt}	Dead time
τ_{rr}	Reverse recovery time
a	Voltage gain characteristic of the transformer
A_c	Core cross-sectional area
A_L	Inductance factor
A_w	Trace cross-sectional area
B	Flux density
B_s	Flux density saturation point
C_{DS}	Drain to source capacitance
C_{GD}	Gate to drain capacitance
C_{GS}	Gate to source capacitance
C_{HB}	Parasitic capacitance summation
C_r	Resonant capacitor
C_{WW}	Winding-to-winding capacitance
d	Relationship between input and output for DAHB
D_{pen}	Penetration depth
dc	Duty cycle 50%
F_{FF}	Fringing flux factor
f_{R1}	Resonant frequency of the tank
f_{R2}	Lower resonance frequency
f_{SR}	Self-resonant frequency

f_s	Switching frequency
H	Magnetizing force
H_s	Magnetizing force saturation point
i_2	Leakage inductance current
I_{cc}	Gate driver supply current
I_d	Drain current
i_L	Tank inductor current
K_f	Waveform coeffficient
l_g	Length of the air gap
L_k	Leakage inductance
L_m	Magnetizing inductance
L_p	Parallel component of inductance
L_r	Resonant inductor
L_s	Series component of inductance
l_w	Length of a trace
mmf	Magnetomotive force
MPL	Mean path length
N	Turns ratio of a Transformer
Q	Quality factor
Q_{rr}	Reverse recovery charge
R_{ac}	AC loss component
R_{dc}	DC loss component
$R_{ds(on)}$	Drain to source (on) resistance
R_l	Load resistance
T_s	Switching period
V_{cr}	Voltage across resonant capacitors
V_F	Forward voltage drop of a diode
V_{HB}	Voltage across the half-bridge
V_H	High voltage
V_L	Low voltage
W	Length of the core window
W_a	Area of the core window

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Chapter 1

Introduction

In this chapter, the relevant background for rural electrification and the DC microgrid (a smaller variant of a direct current (DC) distribution grid) is presented. Furthermore, the motivation for the work is elaborated.

1.1 Problem Definition: Rural Electrification, Solar Home Systems, and the DC Microgrid

The large-scale emergence of decentralized renewable energy generation alongside the modern ”green energy” ideologies permeating throughout the political and societal spectrum are setting a new standard for the future of power and the modernized power grid. When considering the future of power, the 840 million people who have no access to electricity and an additional one billion more who still have an unreliable electricity connection [1, 2] remain as one of the major concerns moving forward. A stable electrical connection provides rural communities with the ability to utilize their natural energy sources, such as solar or wind. As an example, in sub-Sahara Africa, 573 million out of 840 million people lack electricity [1]. Individuals in these communities typically work as farmers and in hard labor conditions. Moreover, this group is poverty-stricken and lacks sufficient medical care, education, and other social welfare. In order for these communities to grow in a positive manner, especially in regard to education, access to electricity is vital. However, it is still unclear what is the most effective way to achieve rural electrification and studies are currently being conducted on methods which are based on new available technology. In order to discuss the pathways towards electrification, it is necessary to identify the different tiers or steps that are needed in the electrification process. This process takes into consideration the trend that the power demand required by a user increases over time. This growth in the electrification process can be visualized by the electrification ladder (presented in [3, 4]) shown in figure 1.1. Each rung of the ladder represents a different power level that has unique loads and appliances associated with it. Higher levels represent the increase in the number of appliances, and therefore, the overall electricity demand.

Three different rural electrification pathways— grid extension, stand-alone solar-based solutions, such as solar home systems (SHS), and centralized microgrids —are critically examined in [5]. The results of the study in [5] are developed based the on circumstances seen by the communities with no access to electricity. Additionally, the study considers current developing technology when proposing the conclusions. Grid extensions (expanding the national grid’s network to provide electricity access [6]) are a costly endeavor and this results in an infeasible method for providing electricity to these communities. However, SHSs are a less expensive and more viable solution. The pathway employing SHSs can achieve the 5 W, 40 W, and sometimes 100 W tier of electrification but it is only a stepping stone along the path and is not the ultimate solution.

A DC microgrid has unique characteristics such as energy sharing, inherent plug and play capability, and its ability to grow over time. In figure 1.2, the architecture of a typical DC microgrid used in rural electrification is shown. The microgrids are usually centralized with central power generation and storage. It is important to distinguish that although smaller SHS based forms of these grids do have a decentralized way of delivering electricity, the most robust and higher power forms of these off-grid

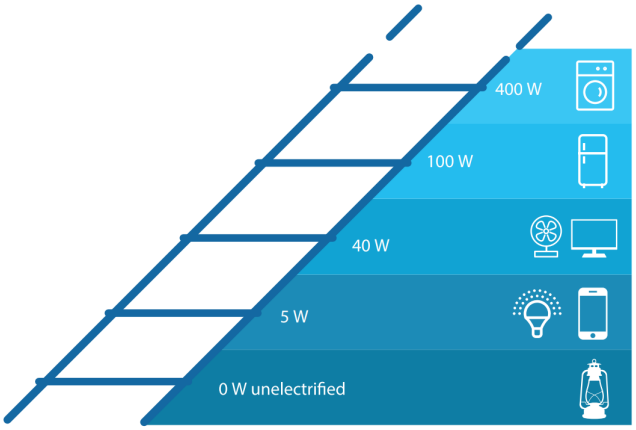


Figure 1.1: Conceptual illustration of the electrification ladder. As a household scales up the ladder, the electricity demand- in Watts (W) -increases through the addition of higher power (or greater number of) appliances [5]

microgrids generally have centralized large-scale PV and battery storage architecture. Centralized microgrids are a vital part of the electrification process but directly implementing a full grid into a rural community has many downsides. Most significantly, the cost is high compared to starting with individual SHSs. Furthermore, an overall demand estimation is needed in the design of a microgrid. This estimation relies on many assumptions and it is difficult to predict the changes in electricity demand over time. In order to perfect this process and find the best pathway to electrification, the implementation of a bottom-up DC microgrid is proposed as the key ”missing link” between all of the possible electrification pathways [5]. The bottom-up characteristic refers to building up in a logical or modular manner in order to properly account for the overall demand of the community. Additionally, it is more economically suitable for these communities to have an implementation process that requires multiple smaller investments versus a single large investment.

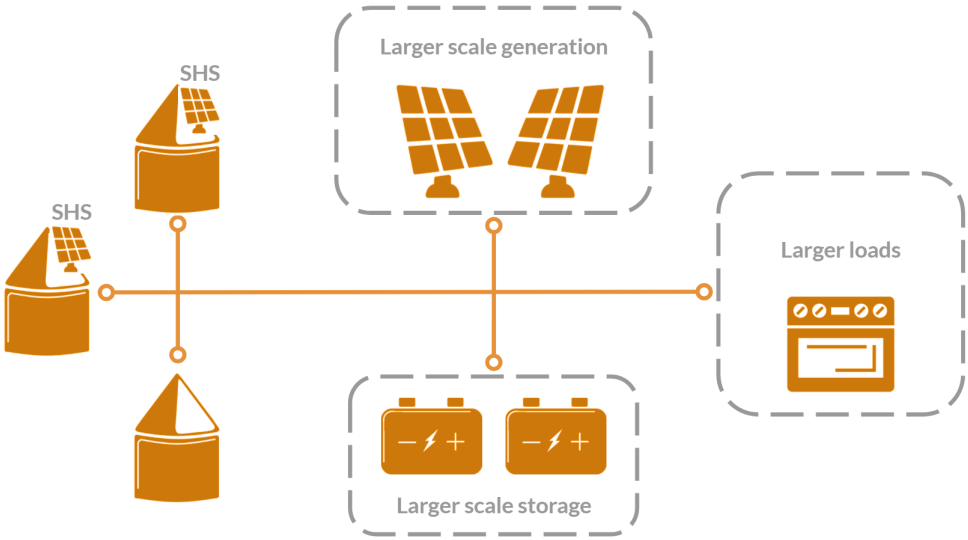


Figure 1.2: Diagram of an interconnected SHS-based meshed DC microgrid with additional centralized generation and storage. The bottom house is shown without an SHS, revealing that purely consumptive houses can join the microgrid.

The modular process begins with an individual SHS for each home. The evolved form of a single SHS is an interconnected SHS meshed DC microgrid which can be established by the interconnection of existing SHSs. This form of a DC microgrid is decentralized (represented by the homes and interconnections on the left side of figure 1.2). These decentralized solutions, can provide on demand

electricity for lower levels of power as well as enable energy sharing between homes. Conversely, a centralized grid (with larger photovoltaic (PV) panels and energy storage systems (ESSs)) can grant consistent higher levels of power proportionate to the 100 W and 400 W load level. In time, when the national grid arrives, a previously established DC microgrid can readily serve as a ready distribution grid for communities naturally requiring more power demand as they develop. Additionally, the process of implementing grid extensions reduces to a simplified electrical connection at the perimeter of villages because the interior is already interconnected by a DC microgrid.

1.2 Problem Definition: Power Electronics

Power electronics serve as the interface between different components of a DC microgrid. In figure 1.2, each node represents a power electronic interface (PEI). Therefore, it is essential to successfully implement many DC/DC conversions (occasionally a DC/AC conversion for some loads), with both unidirectional and bidirectional power flow, to each part of the DC microgrid. These microgrids for rural electrification work at a 300 - 400 Volt (V) range, typically at a nominal 350 V. Solar home systems provide power to low power loads in tiers 1 to 2 of the electrification ladder with 12 V battery and 12 V distribution [7]. This SHS operating voltage can vary up to but not exceeding a voltage of 48 V [8]. There are also new emerging connectivity methods like the USB type C load connection. Its inherent power delivery characteristics allows for the DC/DC power electronic converter to have an adjustable voltage that can vary from 5 - 20 V.

The PEIs at the PV panel, ESS or battery bank, and high power load are quite similar to the SHS connections of the DC microgrid. However, the nominal values for the voltage differ from the standard DC voltage at the SHS-to-DC microgrid connection. In order to facilitate greater tiers of consumption, these nodes of the microgrid require a higher voltage level because it minimizes the distribution losses. Furthermore, the voltage level at these nodes often varies depending on series/parallel configurations (for PV and batteries) and, for the high power loads, it is dependent on the operation voltage of the appliance which generally is either at 110 V or 240 V.

At the heart of many power electronic devices, there is a transformer. The transformer is responsible for the stepping-up (or stepping-down) of the voltage. A transformer and its windings of wires naturally have a unique characteristic called the turns ratio. This ratio is responsible for the gain in the voltage and current from its input to output (regarded as primary and secondary sides in practice). Transformers also grant electric isolation between the primary and secondary sides of a switching converter. A planar transformer (PT) is a contemporary and innovative design of a traditional transformer. Most notably, it can be recognized by its lack of wires which are replaced by traces on a printed circuit board (PCB). It is described as planar because these transformers are typically very flat and use specific core types that are horizontal and flat. The core (generally an iron or ferrite material) makes up the overall shape of the transformer and is a vital component that allows for the transmission of power from one side of the transformer to other through electromagnetic induction. It so happens that planar transformers have unique attributes that mesh well with the type of converters found at PEIs in DC microgrids used in rural electrification.

1.3 Motivation

Historically, DC/DC converters for high power applications, such as wind turbines and electric vehicle (EV) charging, are rated at 1 kW or greater due to the nature of the loads and the high societal demand for power. Moreover, alternating current (AC) has dominated as the main form of electricity in power transmission. This AC infrastructure usually pushes the DC/DC conversions to happen externally via a converter attached to the load itself. These converters are usually referred to as point of load converters. Therefore, DC/DC conversion typically finds its main applications in low power, such as power supplies, and household loads. These applications are typically limited to less than 100 W. Converters designed for the 200 W to 1 kW range do exist, such as server power supply used in telecommunications [9], but are usually only used in definitive specialized applications. This category of converter is more uncommon and less explored in literature compared to the other power ranges of converters previously discussed.

However, due to the emergence of the DC microgrid and the movement to provide stable electricity access to all, a new niche of converters has been brought to light. This class of converter operates in the 200 W to 900 W range and are specifically designed to work in a decentralized DC microgrid environment. These converters must also have voltage regulation at the output in order to provide the correct voltage level to different loads, thereby one converter is used to satisfy all household load requirements and the grid connection. It is important to mention that converters in rural electrification fall in this power range but also similar PEI applications at this power level could be utilized in the modernized hybrid AC/DC grid of the future, presented in [10], to provide the needed DC/DC conversion in the DC part of the grid.

The motivation for this thesis is to find the best topologies, switching technology, and to create successful designs for a unidirectional and bidirectional version of a **DC microgrid variable power output converter**. The research specifically focuses on the DC/DC converters that connect a SHS to the DC microgrid (the connection point is shown in detail in figure 1.3). The Gallium nitride (GaN) transistor is the preferred switch technology for this application due to its effectiveness in the low voltage (up to 650 V), high performance scenario. GaN transistors have inherent benefits such as zero reverse recovery, low switch resistance, and low parasitic capacitance which allows for high frequency operation with low switching losses resulting in smaller passive components. The work also takes into consideration the unique possibilities available to the design due to the lower power (200 - 900 W) characteristic of these converters. In addition, the advantages and design of the planar transformer will be explored for these applications. This research aims to bridge the gap from the standard DC/DC converter of this power level to a more effective and efficient converter custom-fit for a DC microgrid, especially those used in rural electrification.

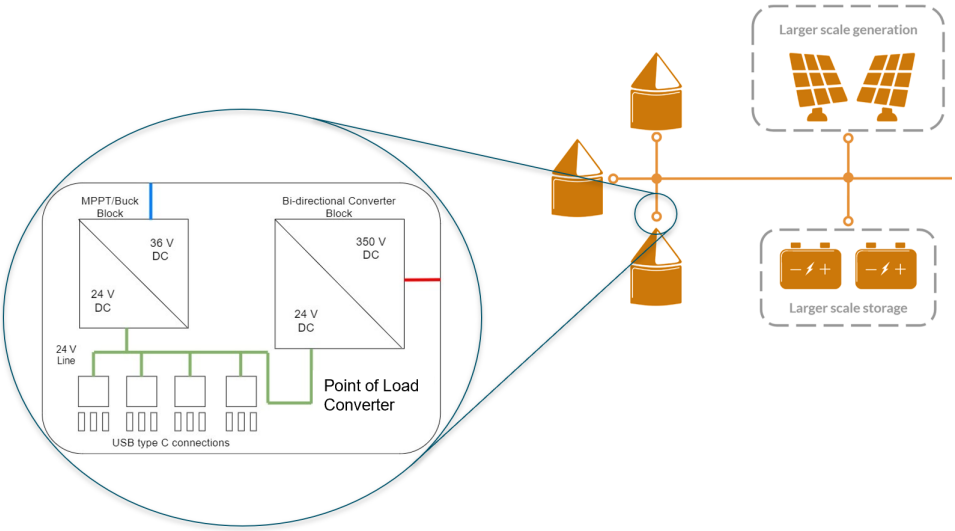


Figure 1.3: A diagram highlighting the node where a point of load converter (a specific type of PEI) connects to the DC microgrid. This node is comprised of not only the bi-directional DC/DC converter (most relevant for this research) but also to a maximum power point tracking (MPPT) converter for the solar connection and USB type C compatible connections for the SHS

1.4 Research Questions

1. How can a unidirectional DC/DC converter be designed for the interconnection of a 350V DC microgrid to individual households for rural electrification that includes high switching frequency GaN technology?
2. How can a bidirectional DC/DC converter be designed to achieve the same purpose but also with a higher power rating?
3. How to design a PCB based planar transformer for these two converters and why is a planar transformer preferred for these applications ?

1.5 Outline

The report is divided into 7 chapters and is followed by an appendices which contains supporting information for additional reference. The following list provides the title and a small summary for each chapter:

Chapter 1: Introduction

- Provides the relevant background for rural electrification and the DC microgrid (a smaller variant of a direct current (DC) distribution grid) is presented. Furthermore, the motivation for the work is elaborated.

Chapter 2: Literature Review and Background Information

- Provides the design theory for the main converters used in this research. Alongside the review, an analytical topology selection process (comparing multiple topologies) is presented. The section ends with a theoretical overview and analysis of Gallium nitride (GaN) switching.

Chapter 3: Planar Transformers

- Describes the theory and design process for creating a planar transformer. It will conclude by presenting the benefits of these transformers, especially for the power levels typically found in rural electrification.

Chapter 4: Unidirectional Half-bridge LLC Prototype Modeling, Design, and Construction

- Provides the complete design process for the unidirectional Half-bridge LLC DC/DC converter. The process includes simulations, transformer design, thermal considerations, and PCB layouting.

Chapter 5: Bidirectional DAHB Prototype Modeling and Design

- Provides the complete design process for the bidirectional DAHB converter. The process includes simulations, transformer design, and thermal considerations.

Chapter 6: Results and Analysis

- Provides a summary of the testing results for the unidirectional half-bridge LLC converter and the simulation results for the bidirectional DAHB converter. Moreover, it will analyze findings, provide explanations, and give recommendations based on the results.

Chapter 7: Conclusion

- Provides answers to the research questions and the conclusions of the work. Additional recommendations for future work are also included.

Chapter 2

Literature Review and Background Information

Chapter 2 provides the design theory for the main converters used in this research. Alongside the review, an analytical topology selection process (comparing multiple topologies) is presented. The section ends with a theoretical overview and analysis of Gallium nitride (GaN) switching.

2.1 Topology Comparison

The following review is comprised of the more prominent single-stage topologies which permit bidirectional power flow, galvanic isolation, and efficient DC/DC conversion. Two separate converters were designed for this work; a unidirectional and a bidirectional version.

2.1.1 Buck, Boost, and Buck-Boost Converters

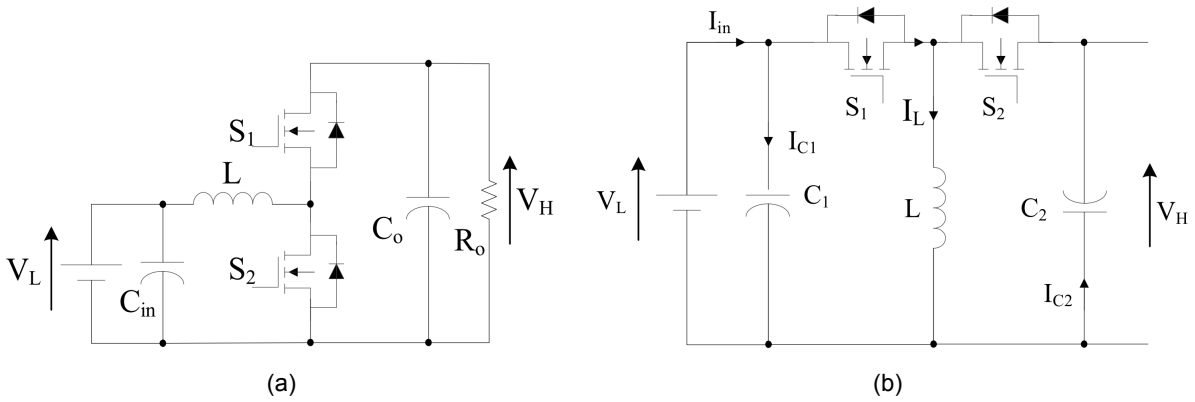


Figure 2.1: (a) Schematic of a bidirectional (non-isolated) Buck and Boost (b) Schematic of a bidirectional (non-isolated) Buck-Boost [13]

A boost/buck converter steps up/down a DC voltage from input to output. The circuit operation is dependent on the conduction state of the switches. During the on state, current within the inductor increases and the anti-parallel diode in the other switch blocks current flow. In the off state, energy is transferred from the inductor to the capacitor resulting in a decreasing inductor current. Since current through the inductor can not instantaneously change, the diode of the switch conducts current [11]. Steady state operation can be characterized as discontinuous conduction mode (DCM) or continuous conduction mode (CCM). In DCM, the inductor current reaches zero in each cycle however, in CCM, the inductor current never reaches zero. Duty cycle control is used to adjust and regulate the voltage output.

A conventional boost/buck converter (seen in figure 2.1a) is typically non-isolated and can be transformed to operate bidirectionally with the use of switches in place of diodes. Parallel combination of an inductor and capacitor, typically seen at the outputs of both types of converters, acts as a second order low pass filter to reduce output voltage ripple. The only variant of these converters that fits the application niche would be a version that includes coupled inductors in the design in order to provide isolation. Coupled inductors can be normally coupled or inverse coupled. Inverse coupling allows for a larger inductance given an inductor of the same size that is normally coupled. The flux adds together to result in a higher flux with a smaller ripple. Inverse coupling can reduce core losses in the coupled inductor and allow for a smaller component to achieve the same level of inductance. There are trade-offs in the design to consider but this section is limited to an overview of different configurations that can be implemented into boost/buck converters to allow for a more feasible design.

An interleaved version of these converters, in essence, is an exact replica of the converter in parallel with the original. The benefit of this is to half the current in each inductor while also decreasing the value of output voltage ripple. An interleaved configuration reduces the size of the passive components and, in certain scenarios, can reduce price, adverse thermal effects, and surface area of the system. More information can be found in [12]. The cascading of multiple of converters can also be implemented in order to increase the overall voltage boost (or reduction) ability of the converter and reduce current stress [13]. This is when two or more converters are connected in a series-like cascaded formation.

It is rare to find an example of a bidirectional isolated converter that uses the standard boost/buck set up. One example is the primary parallel isolated boost converter (PPIBC) introduced in [14]. It is possible that by using one or more of the aforementioned adjustments alongside coupled inductors, a converter could be designed for a rural electrification application. However, due to limited literature coverage of a bidirectional version with isolation and the tendency for an increasing number of components as more functionalities are added, these topologies are limited in this regard.

As for the buck-boost converter (non-isolated version shown in figure 2.1b), this topology is mostly used in its non-isolated form as a cascaded addition to a more conventional dual active full bridge switch converter. There are cases such as the buck-boost used in [15] with a coupled inductor. It uses three active switches along with three diodes. The converter uses both zero-current switching (ZCS) and zero-voltage switching (ZVS) to reduce losses. A buck-boost converter can operate in the kilo-watt power range but has multiple passive components because of the need for snubber circuits. There are some favorable options such as the converter presented in [15] but it remains a less popular topology choice in literature for bidirectional isolated converters.

2.1.2 Flyback Converter

The flyback converter is one of the most common topologies utilized in low power applications. The flyback is known for its limitations at medium and high power ranges. This is a result of large ripple current in Boundary Conduction Mode (BCM) and DCM operation, the increased size of the coupled inductor, and high voltage stress of the switch. A flyback converter stores energy in the magnetic field of an air gap in a coupled inductor while the converter switch is conducting. When the transistor turns off, the magnetic field deteriorates and the energy stored in the air gap is drawn by the output load of the flyback converter. The flyback converter can be described as two inductors sharing a common core, in which the widings have opposite polarities.

However, because of the recent advancements in switching technology, there are switch options that have lower drain to source resistance and higher break down voltages. This has allowed for the emergence of flyback in the medium voltage range, realistically up to 300 W. A bidirectional DC-DC isolated version is shown in figure 2.2. It only requires two switches, where one is for active power flow in one direction and the other works as a diode for rectifying the output. The flyback converter should be operated in DCM or BCM mode so that soft switching can be implemented. This reduces the voltage ringing, the EMI, and losses in the switch.

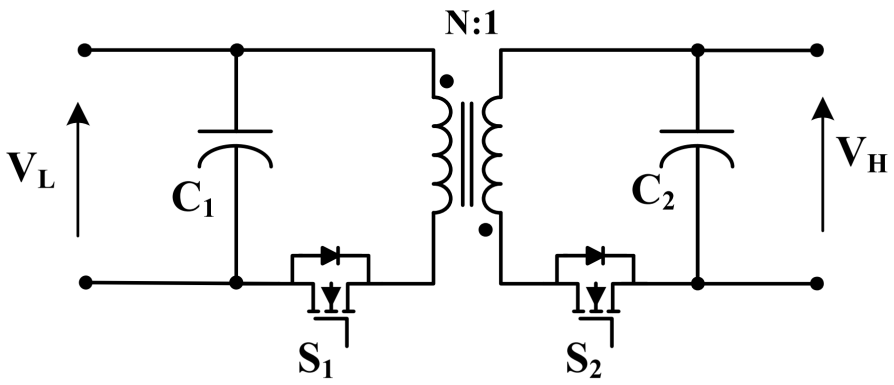


Figure 2.2: Schematic of a bidirectional flyback converter [13]

The voltage stress on the switch in a flyback is high because it is composed of the input voltage, the reflected voltage of the output and the voltage spike due to the leakage inductance of the coupled inductor. Therefore, the switch voltage rating can be derived as $V_{in} + N * (V_{out} + V_{fwd}) + L_k di/dt$ where V_{fwd} is the forward voltage drop of the diode and $L_k di/dt$ is equal to the voltage due to the leakage inductance multiplied by the rise in current over time [16].

2.1.3 Forward Converter

The forward converter is a DC/DC conversion topology that uses a transformer and its turn ratio to increase or decrease the output voltage. It provides galvanic isolation for the load and has multiple output windings which can be used to simultaneously produce both higher and lower voltage outputs [17]. The output voltage is determined by the input voltage, transformer turns ratio and duty cycle. The transformer has same-polarity windings, higher magnetizing inductance, and no air gap which also signifies that it does not store energy in the transformer [17]. A forward converter passes energy directly to the output through transformer during the conduction phase of the switch.

The bidirectional version of the forward converter, shown in figure 2.3, utilizes a clamped circuit to achieve ZVS. There have been hybrid configurations mentioned in literature within the 300 W to 900 W power range. These hybrid configurations are referred to as Forward-Flyback, Push-pull Forward, and Flyback-Push-pull. In these converters, the primary side of the transformer is derived from one of the mentioned isolated topologies and the secondary is derived from another, either current-fed or voltage-fed [13].

The multiple-switch forward converter is an effective topology for applications that require high efficiency and effective power handling capability for up to 500 W of power. The forward converter is often compared to flyback because they have similar efficiencies at relatively the same power levels. The forward converter has a disadvantage due to the presence of an extra inductor on the output and, additionally, is not well suited for high voltage outputs. The forward converter has an advantage over the flyback converter when high output currents are needed for the load. Since the output current is non-pulsating, it is well-suited for applications with currents that exceed 15 A [18].

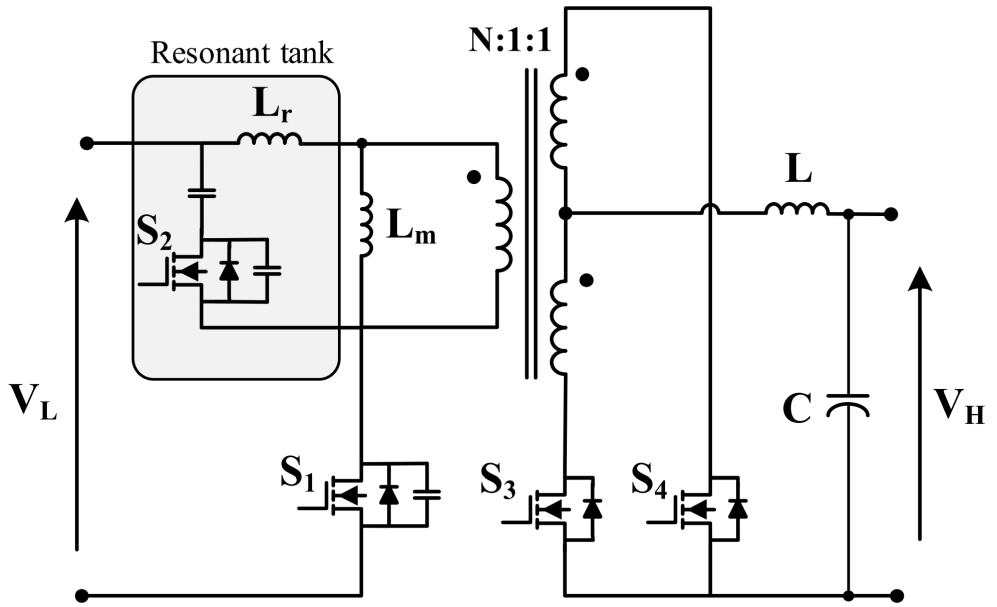


Figure 2.3: Schematic of a bidirectional forward converter [13]

2.1.4 Push-pull Converter

In a bidirectional push-pull converter (shown in figure 2.4), current flowing in the transformer primary is supplied from a pair of switches in a symmetrical push-pull circuit configuration. The switches are controlled with an alternating on and off signal which results in a transformer current that is periodically reversed. Consequently, current is drawn from the input line in both halves of the switching cycle. Push–pull converters have steadier input current, create less noise on the input line, and are more efficient in higher power applications.

A push-pull topology uses two primary windings to create a dual drive winding. This will utilize the core of the transformer in a significantly more efficient manner than the flyback or the forward converters. Moreover, push-pull converters will have smaller filters compared to the forward converters at the same power level [18]. On the downside, only half of the copper winding is conducting current at a time, hence increasing the resistance and copper losses compared to a transformer of a similar size.

The leading problems recorded in literature with push-pull converters are unbalanced flux in the windings and large voltage stress on the switches. Flux in the primary and secondary windings of the center-tapped transformer (discussed more in chapter 3) can become unbalanced and cause heating/loss. As for switch stress issues, each transistor must block more than twice the amount of voltage. There is also the added stress of the voltage spike at the beginning of the cycle due to energy caught in the leakage inductance of each winding in the center-tapped configuration. Stress on the switch makes the push-pull an undesirable topology choice for power factor correction (PFC) applications.

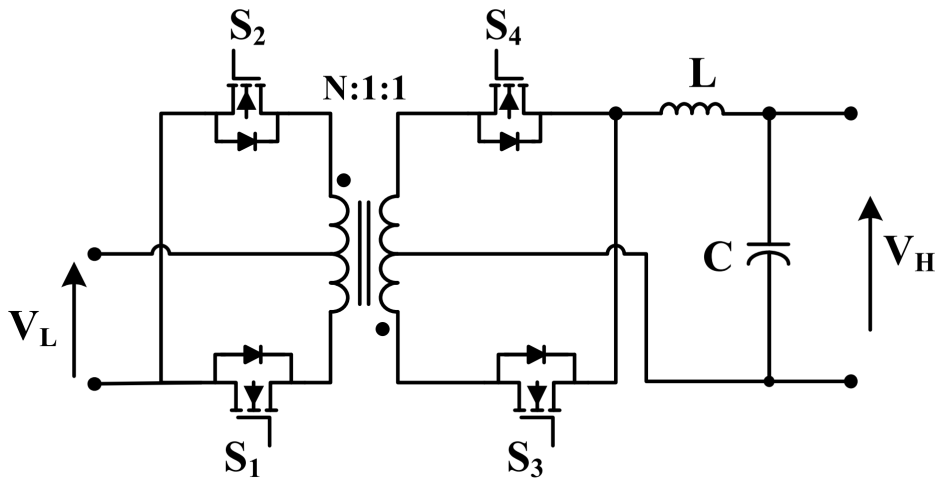


Figure 2.4: Schematic of a bidirectional push-pull converter [13]

2.1.5 Isolated Resonant Converters

Resonant conversion is a longstanding topic known for providing converters with high efficiency, high power density, and smooth waveforms. Resonant converters are based on a ”resonant inverter”, which is a system that converts a DC voltage into a sinusoidal voltage [19]. It then provides this AC signal or power to a load. A network of switches creates a square-wave voltage that is applied to a resonant tank which is tuned to the fundamental component of the square wave [19]. The resonant tank will interact with the fundamental component and react in a negligible way with higher order harmonics, so that its voltage and current will be predominantly sinusoidal. The tank circuit is characterized by two reactive elements; the resonant capacitor (C_r) and resonant inductor (L_r) which can also be denoted as L_s as the series inductance component of an integrated magnetic structure. Different configurations of C_r and L_r define the power transfer behavior and classify the type of resonant converter. However, only a few of the different possible combinations are able to be used in an actual converter. The two basic structures are the series resonant converter and parallel resonant converter, comprised of one tank inductor and one capacitor. Multiple resonant elements can be combined to form multi-resonant converters, such as LCC, LLC, and CLLC converters, to name a few. The main difference between these converters is the frequency and output voltage gain relationship. In the case of multi-resonant converters, there are multiple resonant frequency points because of the different interactions between reactive elements of the tank at specific operating conditions. Another beneficial quality of resonant converters is the inherent zero-voltage switching capability for the primary side power switches and (in some cases) soft commutation for the output rectifier [20]. For the context of this thesis, the LLC converter will be the main resonant topology discussed. A more in-depth comparison of LLC, LCC, and CLLC converters can be seen in Appendix A.

2.1.6 LLC Converter

The LLC converter is a favored topology for bidirectional power converters. It is known for its high efficiency, allowing for high switching frequencies, and high power density. The converter has smooth waveforms for the current and voltage in the tank and EMI emissions are considerably low which results in loose or flexible filtering requirements. This topology can operate bidirectionally and naturally offers galvanic isolation which makes it an ideal fit for power electronics in rural electrification. However, it should be noted that in LLC resonant converters, the output current form factor is generally worse which signifies that the output capacitor bank is stressed more. Albeit, the stress level is considerably lower than the output of a flyback converter, but it still remains one of the few real drawbacks of the LLC topology [19].The typical DC/DC LLC converter is comprised of a switching network (full or half bridge), then, a tank with two inductors and one capacitor, with the load connected in parallel to one L (generating the LLC inverter), and followed by rectification. An example of a bidirectional LLC converter

is shown in figure 2.5. The following information will describe the half-bridge implementation of an LLC but the transition to a full bridge primary side switching is straightforward with similar behavior.

The rectifier block of the converter can be configured as a center tapped secondary (followed by a full-wave rectifier) or a normal secondary windings (followed by a full-bridge rectifier). The secondary configuration of the LLC should be chosen in order to maximize the usage of energy handled by the inverter stage [19]. The center tapped is the ideal configuration when the secondary side is low voltage and high current. The conventional version (single-winding) secondary winding is the more efficient option in a high voltage and low current scenario.

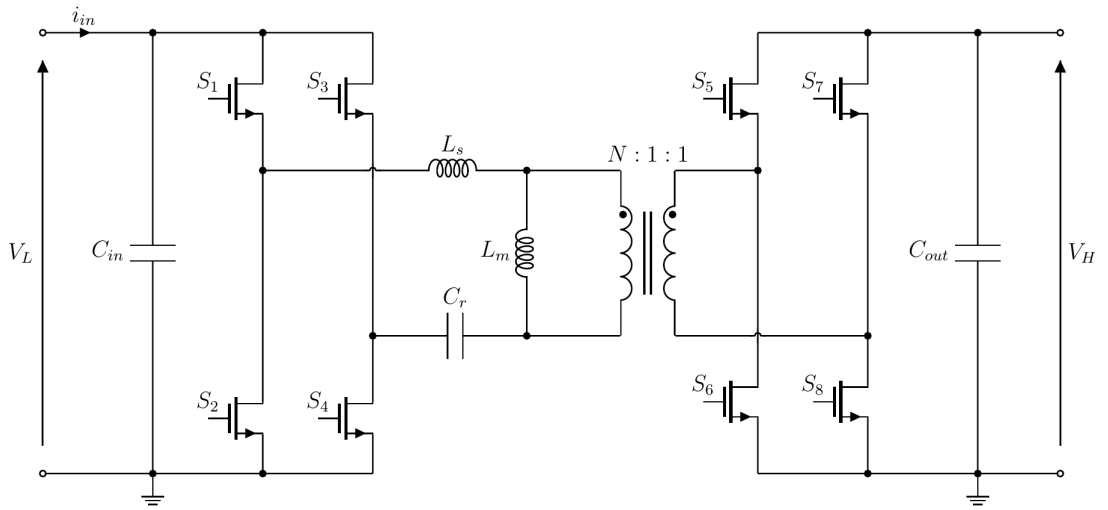


Figure 2.5: Schematic of a bidirectional LLC converter, where the magnetizing inductance L_m can also be denoted as L_p which represents the parallel component of inductance in the resonant tank

The input square wave from the half bridge has a DC component that is equal to $V_{in}/2$. The following equation shows the relationship between input and output voltage of the half-bridge LLC (assuming the standard 50 % duty cycle of the LLC converter)

$$V_{out} = N\frac{V_{in}}{2} \tag{2.1}$$

where N is the turns ratio of the transformer. The resonant capacitor C_r of the resonant tank appears in series to the voltage source. Moreover, under steady-state conditions, the average voltage of the resonant inductor must be zero. Consequently, the input voltage $V_{in}/2$ is applied across Cr which functions as both a DC blocking capacitor and resonant capacitor.

LLC Converter Resonant Characteristics

The half bridge LLC is defined as a multi-resonant converter and, due to the three reactive elements in the tank, there are two resonant frequencies related to the circuit. The first resonant frequency is associated to the operation condition when the secondary windings are conducting. This causes the inductance L_p to be negligible because it is actively shorted out by the low-pass filter and load (when there is a constant output voltage applied across the load) [19].

$$f_{R1} = \frac{1}{2\pi\sqrt{L_s * C_r}} \tag{2.2}$$

The second resonant frequency is associated to the condition when the secondary winding(s) is an open circuit. The resonant tank transforms from a LLC to LC because both L_p and L_s, in this situation, combine into a single inductor:

$$f_{R2} = \frac{1}{2\pi\sqrt{(L_s + L_p) * C_r}} \tag{2.3}$$

f_{R1} is known as the resonant frequency of the tank where as f_{R2} is generally referred to as the lower resonance frequency. The ratio between L_p to L_s determines the degree of separation between f_{R1} and f_{R2}. A typical LLC gain curve can be seen in figure 2.6. A larger ratio results in a larger distance between the two frequencies and vice versa. This affects the frequency modulation and controls of the converter, thus making L_p/L_s a critical design parameter.

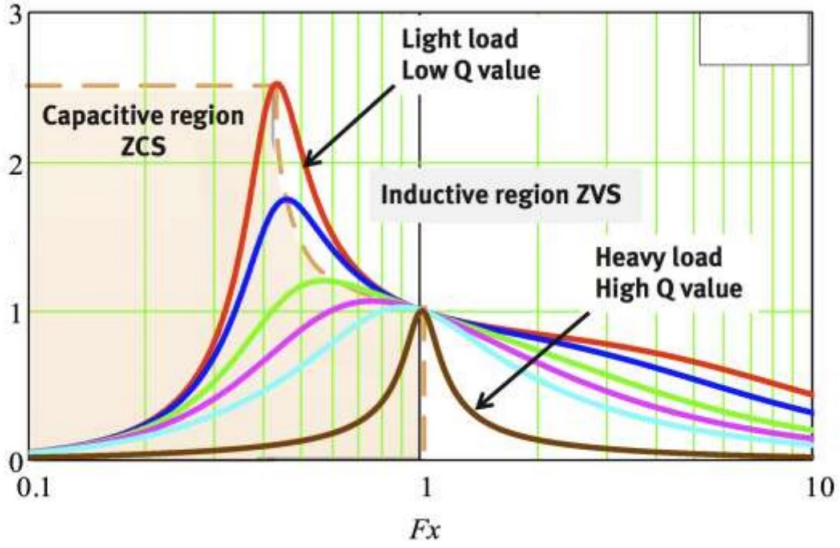


Figure 2.6: Gain curve for a LLC converter, where F_x = f_{R1}

The converter must function in the inductive region. This is the frequency range where input impedance is inductive. The inductive range is where $f_{R2} < f_s < f_{R1}$ and $f_s > f_{R1}$. Operation in the inductive region permits that the primary side switches can achieve ZVS, which is integral for efficient operation of the LLC converter. In the half-bridge LLC converter, the driver circuit powers both MOSFETs in the switching leg on and off with symmetrically alternating signals (for the exact same time and at 50% duty cycle). However, the duty cycle is slightly less than 50% due to a small dead time (τ_{dt}) which is inserted between the turn-off and the turn-on of both switches (also for the complementary case). The dead time interval is quite important in order to achieve ZVS on the primary side (more information on ZVS can be found in appendix A). Soft switching operation is dependent on the magnitude of the magnetizing inductance. Therefore, an air gap in the magnetic core of the transformer is necessary to reduce the effective permeability of the core which results in a smaller magnetizing inductance [21].

Parasitic Elements and Dead Time

The first parasitic element considered is the equivalent capacitance that is seen at the center point between the switches of a switching leg. Its presence means that transitions between switches will take some time to complete and require energy. These transitions are linked to the dead time. The time it takes for this parasitic switch capacitance to completely charge and discharge determines the dead time duration. Equation 2.4 shows the method for determining the dead time in a half-bridge LLC converter (derived in [22]) , where C_{oss} is the equivalent parasitic capacitance found on a switch data sheet.

$$\tau_{dt} = 16\frac{L_m * C_{HB}}{T_s} \tag{2.4}$$

This equation is slightly modified to include C_{HB} which is a combination of all parasitic elements that appear at the half-bridge node between the switches. C_{HB} is defined in the following equation:

$$C_{HB} = C_{oss1} + C_{oss2} + C_{stray} \tag{2.5}$$

C_{stray} is representative of the capacitance that forms between the MOSFET and heatsink, the inter-winding capacitance of the resonant inductor, and any other capacitance that appears at the node. C_{oss1} and C_{oss2} are parasitic capacitances associated to each half bridge switch, respectively.

The second parasitic element that is considered is the winding capacitance of transformer windings. This capacitance, which has a component on both the primary and the secondary sides, is combined with the inductance of the winding, producing the ”self-resonance” of the transformer. In the case of the half-bridge LLC (where there are secondary rectifiers), the junction capacitance of the diodes adds up with the winding capacitance producing a slightly lower self-resonant frequency (f_{SR}) [19]. The winding capacitance can be added to the equivalent circuit model with a single capacitor in parallel to the magnetizing inductance (elaborated upon in later sections). Consequently, the presence of this parasitic capacitance modifies the tank from an LLC to an LLCC. The multi-resonant behavior then results in 3 distinctive resonance frequencies where f_{SR} is greater than f_{R1}. Generally, the operating frequency is substantially lower than f_{SR} and, when this is the case, the effect of the parasitic capacitance is negligible on the power transfer in the tank. However, this may not always be the case and understanding the power versus frequency relationship when this capacitance is not negligible is important for troubleshooting LLC converters if f_{SR} is close to f_{R1}.

Transformer and Leakage Considerations in the LLC Converter

The LLC converter is a topology that collaborates well with magnetic integration. Magnetic integration is when inductors and transformers are combined into a single magnetic component (usually a transformer). This results in a smaller number of components in the system and can enhance the operation of the converter by reducing the path length/resistances between magnetically integrated components.

The LLC topology requires a magnetic structure with significant leakage which is usually avoided in conventional transformer design. Various winding configurations can be used to manipulate the value of leakage inductance such as increasing the space between the windings (a topic which will be evaluated more in chapter 3). Moreover, integrated magnetic structures have a leakage component on both the primary and secondary sides, and in the case where there are multiple output windings or a center tapped configuration, there is a leakage inductance associated to each individual output winding. Leakage inductance at the secondary carries a current,i_2, which produces a voltage drop of the leakage inductance multiplied by di_2/dt. This decreases the expected voltage available on the secondary winding for a given impressed voltage from the primary side. Additionally, in multi-output converters, cross-regulation between the outputs will be negativity affected because of the decoupling effect caused by a component of leakage inductance on each output winding [19].

A voltage drop, caused by leakage inductance, can also be seen in the center-tapped output configuration. During the period where one half-winding is conducting, the voltage seen across the half-winding is equal to $V_{out} + V_F$ (in the ideal case) where V_F is the forward voltage drop of the conducting rectifier diode. Continuing with an ideal case, the half-winding will be coupled one-to-one to the non-conducting half-winding and the reverse voltage across the reversed biased rectifier diode will be equal to $2(V_{out} + V_F)$ [19]. Now, if the leakage inductance of the nonconducting half winding is considered, a $L_k * di_2/dt$ voltage drop adds to $V_{out} + V_F$. This is reflected to the other half-winding and causes the reverse voltage across the nonconducting rectifier diode to be increased by $L_k * di_2/dt$. This can also be referred to as the voltage spike caused by leakage inductance.

Lastly, it can be noted that for a single-winding secondary with a diode rectifier bridge, the voltage applied to reverse-biased diodes of the bridge is not affected by leakage inductance of the winding. The reason is that the negative voltage of the secondary winding is fixed at -VF externally and is not determined by internal coupling which is the case in the center-tapped secondary [19].

LLC (Half-bridge): No Load Operation

The capability to operate at no-load is another unique characteristic of the LLC half-bridge converter. No-load operation is also referred to as ”cutoff” mode and it can occur at frequencies above, below, and at the f_{R1} resonant frequency [19]. In cuttoff mode, the tank current is equal to the current following in the magnetizing inductance and the current through both output diodes is equal to 0.

In order for no-load operation to occur, the voltage produced across the parallel component of inductance in the tank (L_p) and reflected to the secondary side must be less than the output voltage

throughout the whole switching cycle. This condition ensures that neither secondary rectifier can be forward-biased and is mathematically represented in the following equation:

$$\frac{L_p}{L_s + L_p} \leq 2\frac{a * V_{out}}{V_{in}} \tag{2.6}$$

where a is the voltage gain characteristic of the transformer, full or half bridge configuration, etc. L_p is an critical parameter to consider for no load operation as well as soft switching ability in the LLC. The tank current circulating in the circuit will be considerably large and this circulation of current will result in losses. These losses due to circulating current prevent the LLC converter from efficiently operating at extremely low input power levels. There are proposed methods for effectively reducing the losses in cutoff mode such as implementing a burst mode or pulse-skipping mode [19]. The average switching frequency f_s will be substantially lowered which will reduce the switching losses and the current in the tank will be diminished to a negligible level.

LLC Control

Referring to equation 2.1, the essential quantities that characterize the input/output relationship of the converter are the input/output voltages and turn ratio of the transformer N. There is a second-order relation to the value of the load current due to the presence of parasitic elements (winding resistance, forward voltage of didoe, etc...) which causes a voltage drop in the output.

The LLC converter should be operated in the region where the input impedance of the resonant tank has an inductive nature. The tank tends to have more of an inductive nature as the frequency increases. This relationship signifies how the control of power flow can be realized by changing the operating frequency of the converter. The focus for this work will be on power flow control by frequency modulation. This modulation scheme changes the frequency of the square wave with respect to the tank circuit resonant frequency while maintaining a fixed 50 % duty cycle. To properly control the converter, an increased power demand for the load results in a frequency reduction, whereas a reduced power demand yields a frequency rise.

The preferred operation point (at normal conditions) is at the f_{R1} resonant frequency point where tank current is maximally sinusoidal (no impedance), has reduced circulating current, and where operation in CCM minimizes the peak tank current. Operation points in between the f_{R1} and f_{R2} resonance frequencies should be used to handle mains voltage dips and above f_{R1} operation for situations where there is a light load or overshoot transients in the input voltage [19].

2.1.7 DAB Converter

A dual active bridge (DAB) is a bidirectional, isolated, DC-DC converter with symmetrical primary and secondary side full bridge (or half bridges) circuits, a high frequency (HF) transformer, DC-link capacitors, and an energy transfer inductor. Figure 2.7 shows an example of both a full bridge in (a) and a half bridge in (b). Other configurations are possible such as the implementation of push-pull circuits [23]. The reactive network contains an auxiliary inductor (occasionally magnetically integrated into the transformer) which is connected in series to the high frequency transformer. The DAB converter directly incorporates the transformer leakage inductance in series with the auxiliary inductance. Furthermore, the DAB efficiently allows bidirectional power transfer to occur because of the symmetrical structure of the topology[24]. Other benefits of the topology include inherent ZVS turn-on of switches in forward and reverse power flow directions and voltage clamping for the switches, hence removing the need for a turn-off snubber circuit.

The dual Active half-bridge (DAHB) (presented in figure 2.7b) grants the added benefits of a lower amount of transistors, reduced complexity and number of components for gate driver circuits, and operation with zero steady-state DC offset of transformer magnetizing current [25]. Another characteristic of a half bridge LLC is that the magnitude of the half bridge AC voltage is half of the magnitude compared to a full bridge AC voltage. That is to say, that double the RMS current ratings for each switch on the secondary side would be needed in order to provide the same power to the output as the full bridge. Therefore, the DAHB generally is only suitable for usage in lower power applications under 750 W [25].

The half bridge is useful when significant voltage step down is needed. This configuration allows for potentially half of the turns on the transformer which can be beneficial for certain designs. Moreover, a

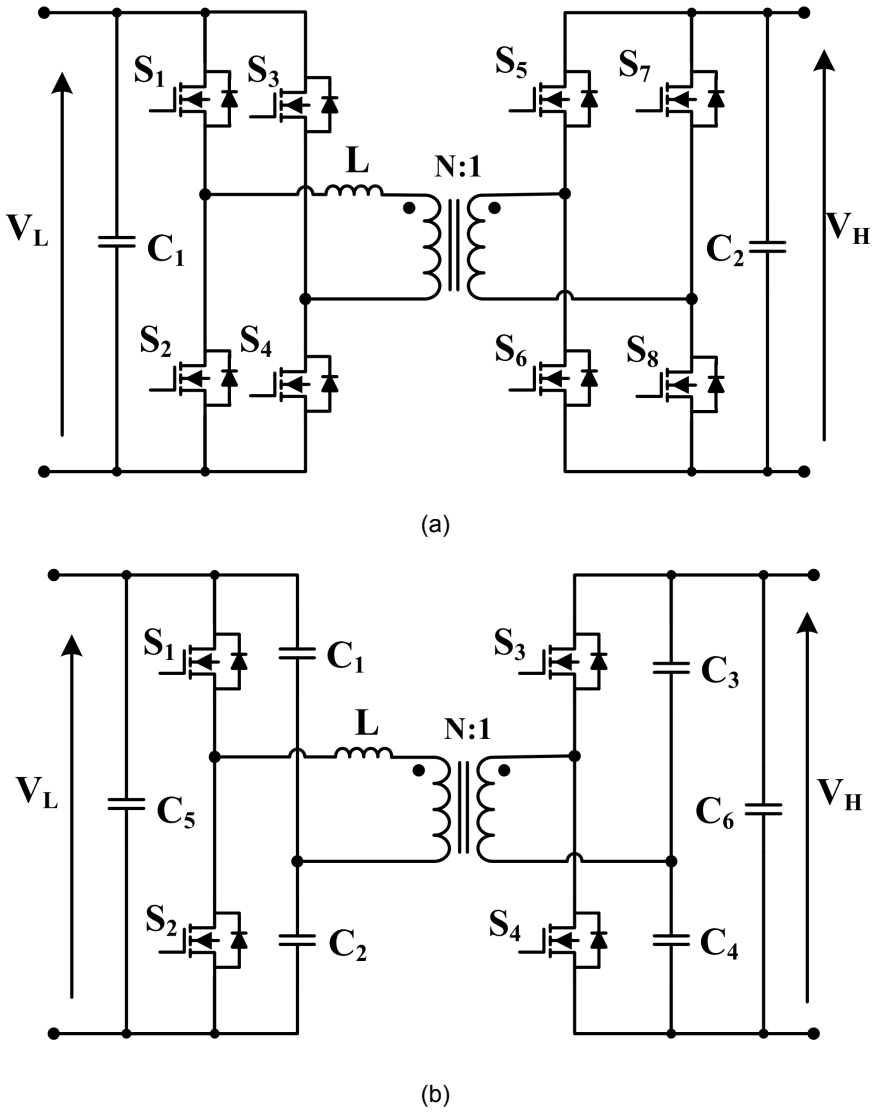


Figure 2.7: (a) Schematic of a bidirectional dual active bridge (DAB) converter (b) Schematic of a bidirectional dual Active half-bridge (DAHB) converter [13]

DAHB invites collaboration with the push-pull circuit for the secondary side because it is useful for current handling on the low voltage side with high current characteristics. The push-pull circuitry attaches to a center-tapped transformer which has two windings that connect at a center point. These windings only handle current for half of the switching period. Therefore, the transformer is utilized less efficiently and greater power handling is required. The push-pull configuration has two low side switches (connected to ground) and each switch requires double the voltage rating compared to that of a normal half-bridge configuration.

The primary advantages of the DAB converter are a low number of passive components, evenly distributed currents through the switches, and its soft switching capabilities (which vary depending on the control modulation strategy). It should be noted that the DAB current waveform depends greatly on the operating point of the converter. The operating point is defined by the input and output voltage alongside the desired total output power. The individual modulation strategies, or method of controlling the converter, have different characteristics and, in some cases, have larger/smaller ranges of ZVS and high circulating current behavior. For certain operating points, higher magnitude transformers RMS (DC) currents can result [24].

DAB Control

There are many modulation strategies for controlling a DAB converter. Those methods with multiple degrees of freedom and a more complex modulation can yield much higher efficiencies and with a wider ZVS operation range including lighter load conditions [24], [26], [25]. In the context of this research single phase-shift control (SPC) is the modulation strategy of interest due to its ease of implementation compared to other modulation strategies.

In SPC for DAB and DAHB converters, the primary and secondary side bridges are driven with complimentary square-wave PWM pulses at a 50% duty cycle with a small dead time inserted in between pulses. The ”phase-overlap” or phase shift between the primary and secondary side resulting square waves is used to vary the output power and determine the direction of power flow (in bi-directional applications). The direction of power transfer is delivered from leading bridge to lagging bridge. The square pulses delivered to the bridges create a differential voltage applied across the series inductance responsible for energy transfer. More energy is stored in the inductor for a larger phase overlap up to $\pi/2$. The power transfer equation for a DAB operating in SPC, derived in [27], can be seen below:

$$P = \frac{V_1 V_2}{2\pi L}\left(\Phi - \frac{\Phi^2}{\pi}\right) \tag{2.7}$$

where Φ is the phase shift and the transfer ratio is 1:1. The power transfer equation is also dependent on the turns ratio of the transformer. This ratio is chosen based on the analytical model for power transfer (shown in equation 2.7). The dynamic model describes the power transfer through the switching node and passive components (capacitances, energy transfer inductor etc...) in the tank which is presented in [24]. Achieving ZVS is dependent on the resonance between the output capacitance of each switch and series (auxiliary), leakage, and magnetizing inductances of the tank circuit during different switching intervals and output load conditions. This behavior can be analyzed by using dynamic equivalent circuit models with harmonic considerations which can be seen in [24]. Further information regarding the effects of magnetizing inductance and parasitic capacitance on ZVS range can be seen in Appendix A. ZVS can be realized when the current through one of the complimentary switches is interrupted during a switching moment. This current (regulated by the energy transfer characteristic of the auxiliary inductance) then flows through the output capacitor of the switch and is subsequently forced into the anti-parallel diode of the device. The power transfer behavior in the DAB based on equation 2.7 is shown in figure 2.8.

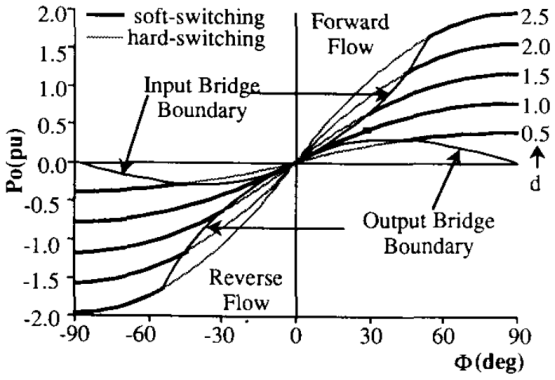


Figure 2.8: Bidirectional power flow characteristics portrayed by a power output versus phase shift relation. d is the power relationship between input and output [27]

where Φ is the phase shift and d is defined for a full bridge in the following equation (factor of $1/2$ input voltage for half bridge):

$$d = \frac{V_{out}}{N * V_{in}} \tag{2.8}$$

PI control serves as an effective method for implementing single phase-shift control (SPC). Feedback measurements must be incorporated into the design such as the output voltage and current. An

output voltage error signal is produced based on a reference point selected by the designer. This feedback differential measurement is delivered into the PI control algorithm in order to generate the proper phase shift in between the PWM signals. The goal of the controller is to regulate constant power while also achieving zero steady state error.

The drawbacks of SPC, gathered from various literature, are quite consistent. SPC results in high circulating current in the circuit, which leads to increased i^2R conduction losses and higher current ratings for the components. An additional limitation is that ZVS operation over the entire power range is possible only when the effective voltage conversion ratio is unity [26], [27]. Otherwise, ZVS is only available in certain operation modes as can be seen by the soft-switching regions depicted in figure 2.8.

2.2 Topology Selection

The main criteria considered for the selection of the topology is listed below, in order of importance:

- Transition from Unidirectional (240 W) to Bidirectional (500 W)
- Compatibility with High Frequency Switching
- Cost (Number of Components, Size of Passive Components, etc...)
- Efficiency at 500 W Level
- Surface Area

Table 2.1 presents the design parameters for the prospective converters. The information in this table primarily considers efficiency at 500 W level. Certain topologies work better with certain output characteristics, such as low voltage and higher currents like the forward converter. Also, some converters see more losses at higher power levels, such as the flyback topology.

Table 2.1: Overview of the parameters used in the preliminary design of the converters for rural electrification

	Power (P)	**Input Voltage (V_{in})**	**Max Input Current (I_{in})**	**Output Voltage (V_{out})**	**Max Output Current (I_{out})**
Unidirectional Version	240 W	300-400 V	800 mA	20-30 V	10 A
Bidirectional Version	500 W	300-400 V	1.67 A	20-30 V	20 A

The topology must be flexible to feasibly transition from a unidirectional to a bidirectional version with minimal changes. In addition, the integration of Gallium Nitride (GaN) transitors is required in order to actualize high frequency operation and investigate deeper into the benefits of GaN. GaN power transistors have significantly lower input and output capacitances as compared to silicon transistors of the same on-state resistance and voltage rating. GaN switching collaborates well with many of the inherent attributes of the LLC converter. While resonant LLC converters do not suffer from switching loss, the reduced output capacitance enables higher efficiencies and switching frequencies by reducing the dead-time soft-switching duration, and reducing converter RMS currents [28].

The flyback has higher losses at the 500 W level and does not function as well at high frequencies compared to other topologies because it uses the core less efficiently (cost increase due to increased size and weight for a core as power levels go up). The boost, buck, and buck-boost topologies were also ruled out of the selection process because they rely on the operating frequency and value of the inductor to limit the current ripple. If a large step up or step down is needed, the value of the inductance for a coupled inductor significantly increases. The only solution is to cascade multiple converters to

reduce the magnitude of the voltage change or to raise the frequency. Raising the frequency results in more core losses in the coupled inductor which stores energy and is overall less efficient than a transformer.

Forward and push-pull converters are both legitimate bidirectional options with potential to operate in both power levels. The push pull seems to take the edge because it utilizes the core more efficiently and needs smaller passive components than the forward converter. The switch stresses in the push-pull are also double of V_{in} which increases the cost significantly on the high voltage side. Most importantly, the main concern comes from the transformer and the number of windings needed in order to step up or down the voltage. Half bridge topologies such as the LLC resonant converter and DAB produce V_{in}/2 at the transformer input which significantly reduces the number of turns needed by the transformer. This not only reduces leakage but the size of the core, costs, and issues at higher frequency operation. It should be noted that high output current handling is an advantage of the push-pull topology and this attribute was taken into consideration for the final design

The half-bridge LLC resonant topology was chosen as the unidirectional version because of its potential to achieve high switching frequencies, lower switching losses, and for its relationship to transformer leakage and magnetizing inductances in the resonant tank. The use of an integrated transformer reduces the weight and size of passive components in the circuit. A half-bridge configuration was selected in order to utilize the $V_{in}/2$ characteristic of the half-bridge so that the turns ratio and number for turns on the transformer could be reduced. Moreover, the secondary side of the converter was configured as a center-tapped winding configuration with a full wave rectifier, which is the exact same as the secondary of a unidirectional push pull converter.

The DAHB converter was the chosen topology for the bidirectional version. The LLC was originally planned as the topology for the bidirectional version for the above reasons. However, the catalyst for changing to the DAB topology when transitioning to a 500 W bidirectional version was the complications in designing the resonant tank for the LLC. Because of the need for reinforced isolation (a requirement in rural electrification), there will be a higher leakage inductance value in general. This, in combination with the possibility of having two different tank characteristics in the forward and reverse direction (a result of a needed turns ratio of around 10), introduced some complications into the design of the tank that could be avoided with the DAB. The main downside to the DAB is that it needs larger passive components (DC blocking capacitors and auxiliary inductance) compared to the LLC. The DAB converter, similarly to the unidirectional LLC, employed a secondary side modeled after the push pull secondary, in order to have better current handling capabilities at the output.

2.3 Gallium Nitride (GaN) Switching

Gallium nitride is a material used in the manufacturing of semiconductor power devices. It is the material used in GaN high electron mobility transistors (HEMT) which is the transistor explored in this research. GaN is a wide band gap semiconductor (3.4 electron Volts) which results in an intrinsic carrier concentration which is several times lower than the concentration in silicon. Therefore, GaN devices produce a lower leakage current and can function at higher temperatures. Other attributes of the GaN HEMT are the high critical electric field and the maximum reachable breakdown of the material which allows for GaN technology to be effective for high voltage applications. The likelihood of obtaining a specific breakdown voltage with thinner current drift layers yields a considerable reduction of the on-resistance ($R_{ds(on)}$) of the GaN HEMT compared to a silicon transistor. As a result, more compact GaN tech can be manufactured, thereby reducing both the dynamic and static losses of the device [29]. The smaller parasitic capacitances and their locations between the layers in a GaN device can be seen in figure 2.9.

GaN HEMT's naturally lower output and gate capacitance alongside the GaN material's high saturation electron velocity allows for high switching frequencies in the megahertz range. The lower capacitances associated to the GaN transistor minimize gate and switching losses to increase efficiency. Another characteristic of GaN that increases efficiency, reduces ringing in the switch node, and EMI is the inherent lacking of a body diode, thereby eliminating the presence of reverse recovery loss. Lastly, operation at higher frequencies is achievable because of the two-dimensional electron gas (2-DEG) present in AlGaN and GaN heterostructures [30]. The charge carrier mobility values in 2DEG normally exceed 1000 $cm^2V^{-1}s^{-1}$.

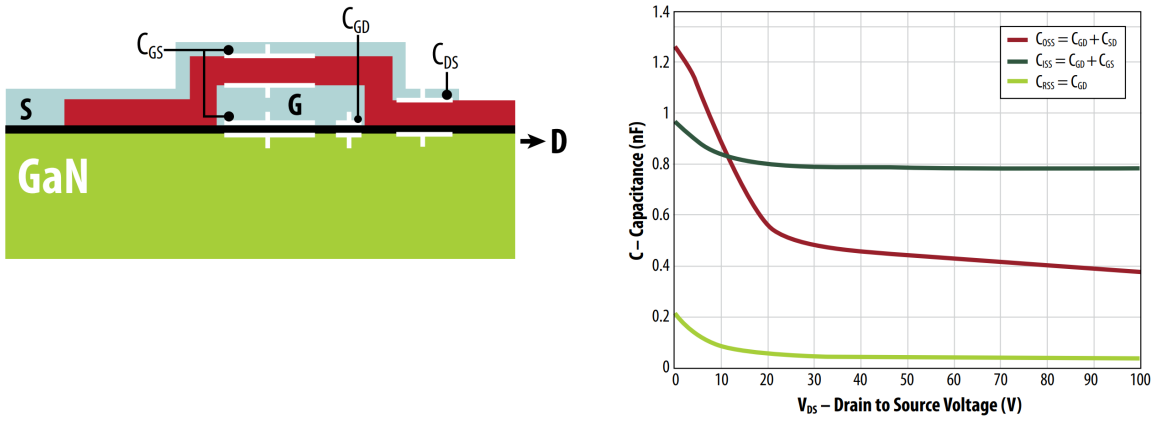


Figure 2.9: Locations of parasitic capacitance within the cross section of the GaN transistor junction. The graph shows the magnitude of each of the individual parasitic capacitances [31]

High electron mobility transistors are novel devices and its operation is based on the 2DEG gas previously mentioned. GaN HEMTs are inherently normally-on devices, meaning, current conducts between the source and drain electrodes at a zero gate bias voltage (V_g= 0) [30]. This normally-on or depletion mode trait is due to the presence of 2-DEG which forms a conduction channel for current to flow. In the normally-on case, current flow is controlled by applying a negative bias to a Schottky gate electrode. New GaN techonology has emerged for reliable normally-off (enhancement mode) HEMTs [29]. Enhancement mode (E-mode) GaN HEMTs have become widely available and the GaN device of choice in most applications. More can be read in Appendix B about the techniques used to create enhancement mode GaN transistors.

2.3.1 Reverse Conduction in E-mode GaN HEMT

The reverse conduction path (formed in an E-mode GaN device) is created when current is forced into the source of an off transistor. A voltage drop (similar to the voltage drop across a diode) is generated from source to drain when the drain voltage is lower than the gate voltage by the value of the turn-on threshold voltage. When this condition is met, the 2-DEG is restored under the gate electrode which creates a channel for current to flow from source to drain. It should be noted that if a negative voltage is applied to the gate the forward voltage drop of the GaN device will increase by the same amount of the negative bias gate voltage. There is no reverse recovery (Q_{rr}) because there are no minority carriers forming the channel. The device turns off instantaneously as the 2-DEG dissipates.

2.3.2 Layout Considerations for GaN HEMT

Parasitic elements introduced in the layouting become more concerning as the switching frequency increases. For GaN devices, the common-source inductance L_{cs} limits the slew rate of the device's drain current. A higher L_{cs} will lead to more losses and possibly catastrophic damage to the transistor at high frequency operation or at high drain currents. The reduction of the gate-to-ground loop has a great impact on switching performance, especially during turn-off when the GaN gate is pulled down with a resistor. The resistance value needs to be low enough so that the device does not turn back on when the drain is pulled high during switching. In addition, reducing the current loops of the switching nodes will reduce the magnitude of stray inductance and the overall impedance seen by the GaN devices.

A gate driver can be integrated into the package of a GaN transistor which minimizes the L_{cs}, thereby reducing limitation on the slew rate. Package integration also reduces gate stress during turn-off and improves the ability to eliminate a false turn-on scenario. Driver integration gives the designers freedom to design and implement effective thermal and current-protection circuits into the GaN FETs [29]. However, this is not always the case because many GaN HEMTs do not come with an internally integrated gate driver. When an external gate driver is implemented it is important that the gate driver

is designed to minimize the gate power loop stray inductance between the VDD supply capacitor and the power devices. This will reduce the gate driver rise time and enhance the driver's ability to change current over time (di/dt) [32]. Moreover, the micro-controller (MC) should be on the same ground as the gate driver and not grounded at the source of the switch where the stray inductance is substantially larger. This topic will be revisited in the design section of chapter 4.

2.3.3 Current Collapse

In a GaN HEMT, a natural phenomenon called current collapse occurs when the GaN on-resistance $R_{ds(on)}$ increases during the application of high voltage to the device. The effects of current collapse on the current voltage (IV) relationship of a GaN HEMT can be seen in figure 2.10. The cause of this anomaly is due to some of the electrons accelerating under voltage stress and getting trapped in the crystal or a dielectric film, and/or at the interface between dielectric and semiconductor layer. The location and density of these traps depend on the device structure and manufacturing process. When electrons are trapped, negative charges cause depletion of the channel of 2-DEG, resulting in an increase in $R_{ds(on)}$ and a decrease in drain current I_d [33]. During this piling up of electrons, on-resistance increases continuously as the power device keeps on switching ON and OFF as shown in figure 2.10.

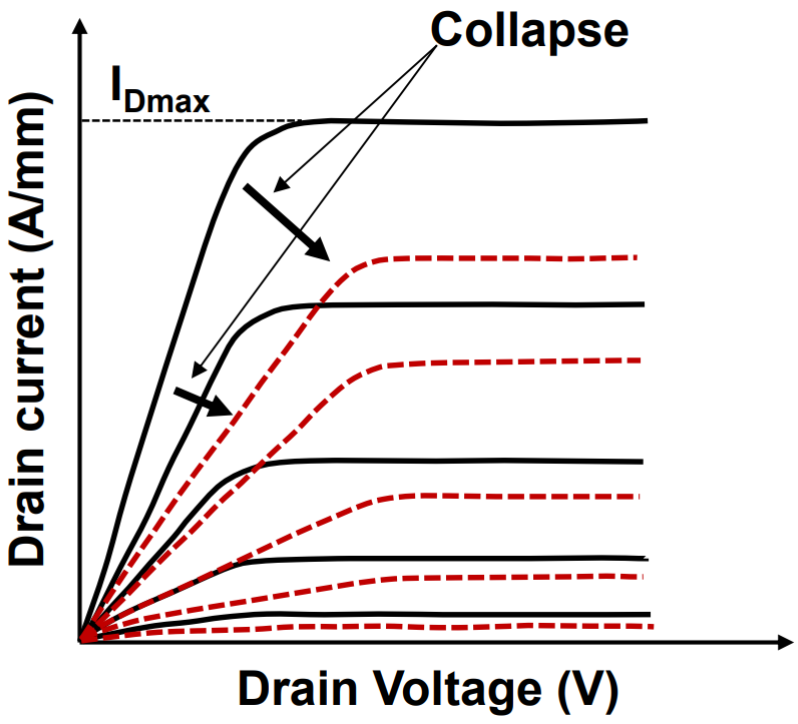


Figure 2.10: IV curve for a GaN transistor where the effects of current collapse can be seen alongside normal IV characteristics [34]

The effect of current collapse contrives the terminology of dynamic $R_{ds(on)}$ or transient $R_{ds(on)}$ and should be taken into consideration when choosing a GaN device. The increase of $R_{ds(on)}$ at higher voltages can degrade the efficiency of the GaN device, heat up the device, and, eventually, overheat and destroy the device [35].

2.3.4 GaN vs. Silicon Carbide (SiC) Vs. Silicon MOSFET

The literature review on GaN switching concludes with a brief comparison of the three leading semiconductor switches used in DC/DC conversion. Compared to the conventional silicon (Si) technology,

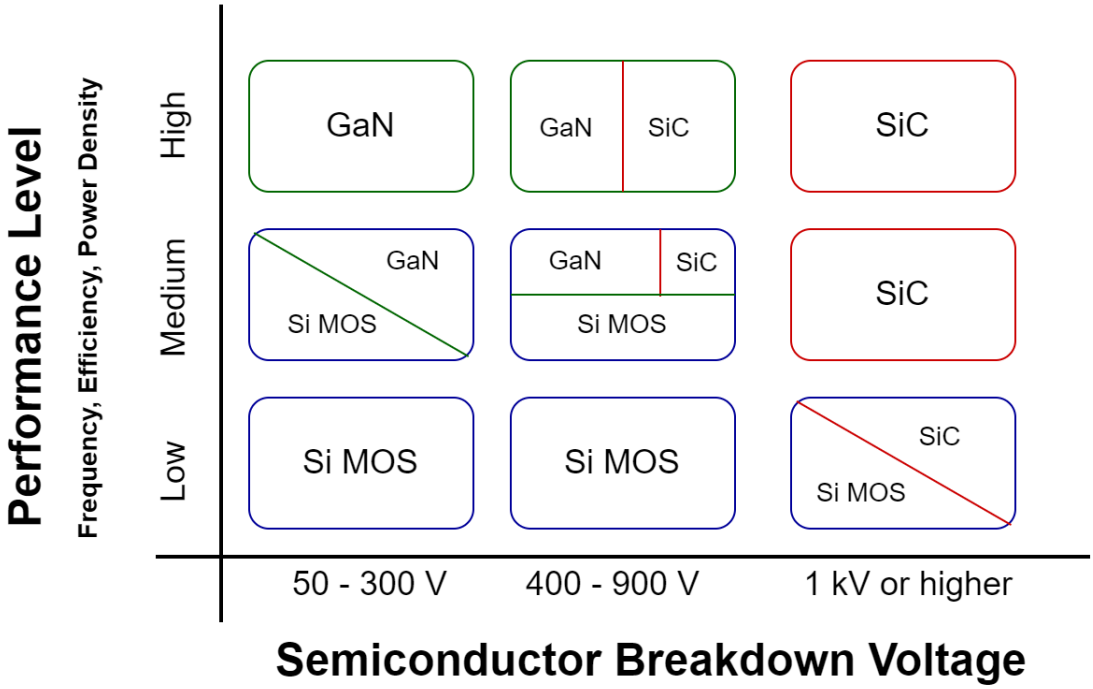


Figure 2.11: Graph which portrays the comparison between the breakdown voltage and on-resistance of Si, SiC, and GaN

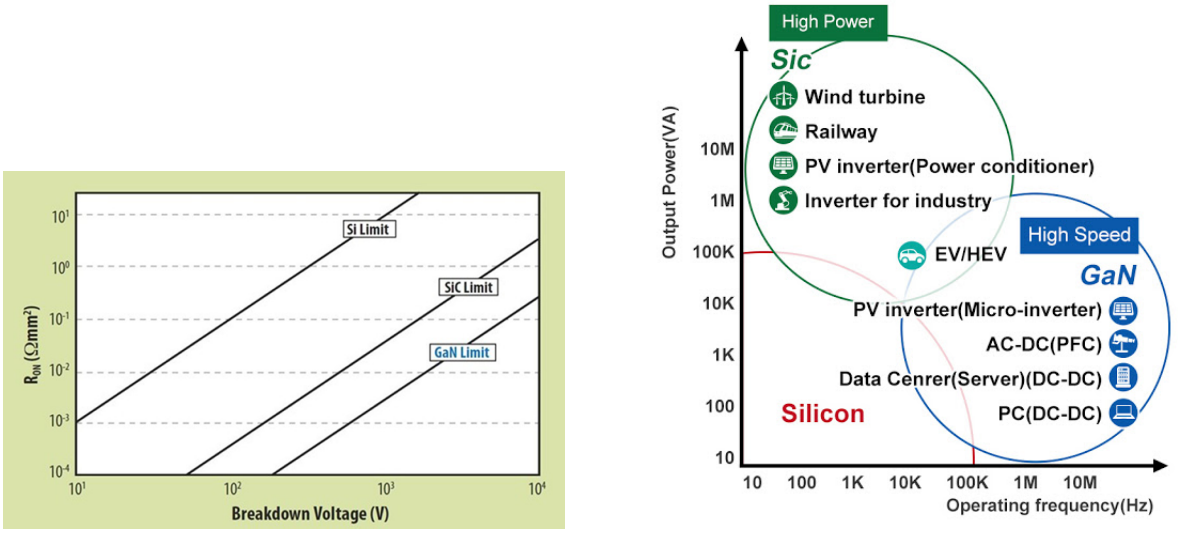
wide-band gap materials such as Silicon Carbide (SiC) and GaN are promising due to their superior material properties such as high temperature operation, high breakdown voltage and high frequency operation. Figure 2.11 can be referenced in order to find the best semiconductor for a given application. This figure is based on a general consensus composed of many academic sources. The figure shows that Si MOSFET is still dominant in lower, medium and, in some cases, high voltage applications when operating lower frequency range up to 100 kHz (sometimes 200-300kHz). The low cost, plethora of different transistor options, alongside efficient operation at these voltage levels make it the obvious choice for these applications. The silicon technology also includes insulated-gate bipolar transistors (IGBTs) which can be used in some areas (lower switching frequencies) of the Si application region.

SiC transistors preform better and are more stable at higher temperatures compared to conventional Si devices. Typically, a silicon carbide transistor has the same performance as a silicon IGBT with double the current rating. In addition, SiC reverse recovery losses are a mere fraction, around 1%, of energy losses in silicon due to Q_{rr} losses [36]. The small Q_{rr} in SiC permits faster turn-off capability and, therefore, more efficient operation at higher frequencies. Compared to silicon FETs of the same rating, SiC transistors have a smaller size and close to half the cooling requirements which reduce the surface area of a design. However, the cost of SiC is significantly higher than Si and the SiC device benefits are only a worthwhile investment in higher voltage applications. SiC and GaN technology need specially designed packaging and gate drivers in order to maximize their advanced operation potential.

The GaN switch is the preferred choice in medium-high frequency and low-medium voltage ranges which is depicted in figure 2.11. Similarly to SiC, it has special gate drive requirements which result in higher costs and additional complexities, thereby making it unable to compete with Si in the lower frequency range. When comparing GaN and SiC, the current collapse phenomenon impedes the effectivity of GaN at higher voltages (greater than 900 V). In the high voltage and high frequency regime, the SiC is the better choice.

Figure 2.12a offers an additional comparison between the three semiconductor materials by displaying the relationship between the breakdown voltage of the transistor and the on-state resistance of Si, SiC, and GaN. Figure 2.12b supports the findings presented in the literature review graphical overview in figure 2.11. It also provides a brief overview of the different real-life applications that can be implemented when incorporating the selected wide-bandgap semiconductor into the design.

In conclusion, the GaN transistor is better suited for low-medium voltage range (200–600 V), higher



(a) (b)

Figure 2.12: (a) Comparison between the breakdown voltage and on-resistance of Si, SiC, and GaN [37] (b) Application map for semiconductor devices based on output power and frequency [38]

frequency and performance applications. In these applications, the transistors manufactured from GaN material are predicted to be the best replacement for conventional Si based technology. As prices for GaN HEMTs decrease over time [39], as is projected by EPC (a company specializing ins GaN tech), investing in GaN switching is currently advantageous because the 600–900 V range covers the converters for electric vehicles (EVs) charging, DC/DC converters in rural electrification, and photovoltaic inverters (among other renewable energy applications). In the 600 to 900 V range, GaN devices are expected to overtake Si devices and be in competition or coexist with SiC transistors.

A summary of the benefits of GaN HEMTs for the two converters presented in this research is listed below:

- Lower on-state resistances yielding lower conduction losses
- Faster devices resulting in less switching losses at a given frequency
- Reduced parasitic capacitance giving less losses when charging and discharging energy
- Less gate charge needed to drive the switch (less losses)
- Smaller devices (compared to Si Fet of same level) using less space on the PCB
- Lower cost (due to HF operation and smaller passive circuit elements)

Chapter 3

Planar Transformers

The following section will describe the theory and design process for creating a planar transformer. It will conclude by presenting the benefits of these transformers, especially for the power levels typically found in rural electrification.

3.1 Isolated Transformer Characteristics

Operation at the maximum possible efficiency is one of the fundamental goals of a switched-mode power converter. Components with loss, such as resistors, are typically avoided in the power stage of any switching converter. Lossless elements, such as magnetic components (transformer and inductors), switches, and capacitors, are preferred for use in the power stage of these circuits [40]. For the context of this research, the typical isolation transformer will be the main transformer defined. Isolation transformers provide galvanic isolation between the AC power lines (mains) and the powered device [41]. This signifies that there is not a DC connection between the two windings. These transformers have three main attributes. Firstly, they isolate the secondary from ground (earth). Secondly, they serve as a voltage and current step up or step down of the line voltages, thirdly, they scale down the line noise being transmitted from primary to secondary or vice versa. Additionally, the presence of an air gap in the ferromagnetic core of a transformer allows for the storage of energy in the gap. However, isolated transformers have non-idealities, such as winding resistance, inter-winding capacitance, and leakage inductance, which can be depicted in an equivalent circuit model, such as figure 3.1(a). These parasitic effects can introduce unwanted resistances or behaviors to the power stage of the converter. Nonetheless, a transformer's characteristics, even the non-ideal effects such as leakage inductance (L_k), can be utilized through different configurations in order to fulfill the needs of the design.

There are different set-ups that can be used when designing the windings. There can be multiple (or auxiliary) windings, series wired windings, and parallel winded windings. In addition, the center-tapped secondary (seen in figure 3.1(b)) is one of many configurations that can be integrated into a transformer. Two separate output voltages, V_2 and V_3, appear with reference to the center point. However, the peak voltage is twice compared to a single winding output. A single winding output is typically followed by a full bridge rectifier with 4 didoes in order to achieve AC to DC conversion. However, a center-tapped secondary only requires half of the diodes (2 in total) to rectify the output. The center-tapped secondary is advantageous in applications where there is a low voltage and high current characteristic on the output. The low voltage lessens the magnitude of the double voltage component and the conduction losses through the diodes (due to the current) are half of what they would be in a full bridge rectifier.

3.1.1 Integrated Magnetic Structures

An integrated magnetic structure can reduce the number of components in the design, therby reducing the cost, and allowing for the implementation of additional functionalities into a single transformer. In resonant converter topologies, a resonant tank, which is composed of a resonant capacitor and inductor, must be designed. In some situations, the effect of leakage can be used to replace the resonant inductor in these converters. This is done by using an integrated magnetic structure. Figure 3.1(b)

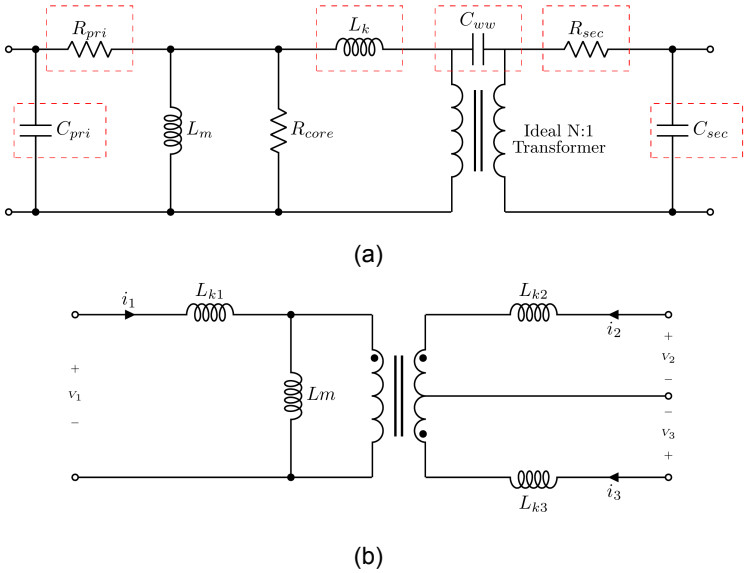


Figure 3.1: (a) Circuit model portraying the parasitic elements of a transformer. (b) Equivalent circuit model for a N:1:1 winding center-tapped secondary transformer for the case where $L_m >> L_k$

shows an equivalent circuit model of the magnetic elements in a single transformer that has primary and secondary side leakage components and a center-tapped configuration on the output. All of these separate magnetic elements, including the leakage and magnetizing inductance, can be integrated into a single isolated transformer. This equivalent circuit model is also used in the design process to properly calculate the transfer function and the voltages and currents flowing in the power stage of the transformer. When transferring parasitic elements in the equivalent circuit across the transformer, a factor of N^2 (or $1/N^2$) is needed to properly convert the value. The magnetizing inductance (L_m) represents the inductance value associated to the primary side winding of a transformer. The theory behind both leakage and magnetizing inductance will be explained in detail in a later section. As previously mentioned, there is the option to integrate an auxiliary winding into a transformer. This is an additional winding (isolated from both the primary and secondary windings) which functions similarly to a supplementary secondary winding. Generally, this type of winding is used in order to establish a voltage power source for low voltage components in the circuit.

3.1.2 Isolation

In order to ensure sufficient protection from electric shock by eliminating a conductive path between the primary and secondary, certain standards and regulations are defined by the International Electrotechnical Commission (IEC). These standards vary based on the voltage level and area of application in which the transformer is used. For instance, in rural electrification, there are standards put in place that require for a transformer to adhere to the Safe Extra Low Voltage (SELV) standard defined in IEC 60364 [8]. The SELV systems must have protective separation such as reinforced insulation, double insulation or protective screening from all circuits carrying higher voltages [42]. Moreover, the transformer cannot be earthed. SELV cables need to be double insulated or wired through plastic conduits when it is possible that they could come into contact with other circuits. The performance and structure of the reinforced insulation assures that the system is still safe even if the basic insulation fails. Reinforced insulation and double insulation provide the same degree of protection against electrical shock and guarantee that even if one of dielectric layer fails, the additional layer will sustain the required level of insulation so that the system or device remains safe.

In order to determine how much insulation is needed to achieve a desired blocking voltage, testing can be done by applying the maximum DC voltage across the transformer and monitoring the circuit to see if there is any leakage current drifting across the transformer. The barrier or insulation can be composed of dielectric materials and air. Each dielectric material (including air) provides voltage blocking capabilities for a given thickness, depending on the individual properties of the medium. Therefore,

when designing an insulation barrier, the designer bases the thickness of the dielectric layer on the magnitude of blocking voltage required. There are two parameters, clearance and creepage, shown in figure 3.2, that indicate the needed distances for constructing the transformer when insulated by air. The clearance is the shortest path between the primary and secondary sides of the transformer (measured through air), whereas the creepage is the shortest path between the primary and secondary sides of the transformer (measured along the surface of the insulation).

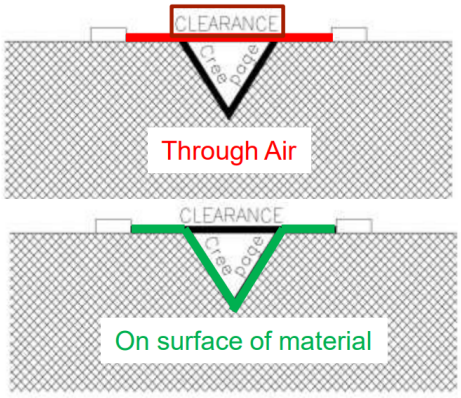
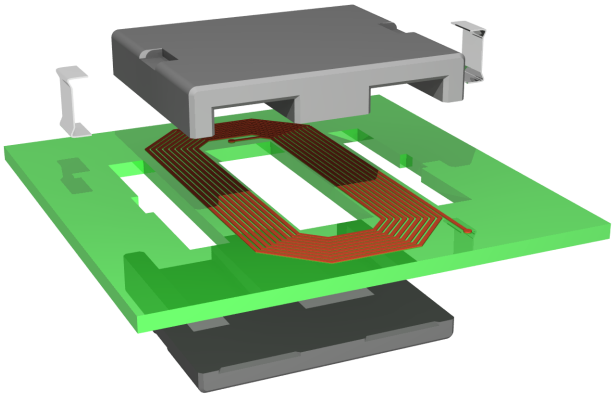


Figure 3.2: An illustration which presents a visual representation of clearance and creepage in a transformer [43]

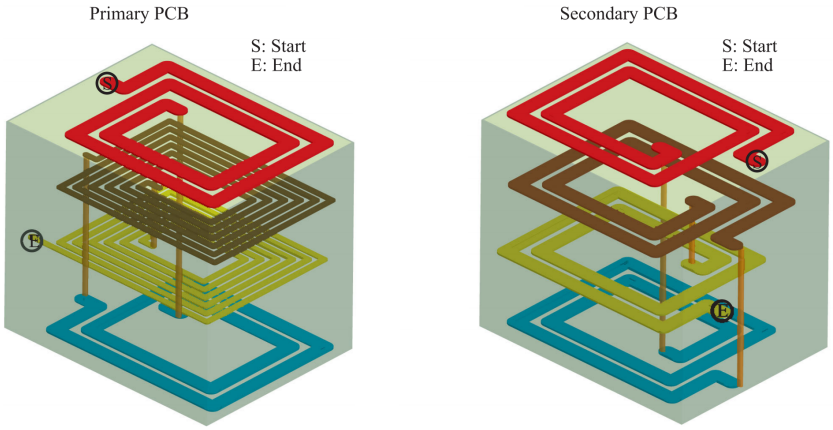
3.1.3 Planar Transformer Overview

The windings in a planar transformer are tracks or traces of copper on a multilayered printed circuit board. This copper trace is visible in figure 3.3(a). Each individual layer is separated by an insulating material, commonly FR4, which is the industry standard insulation material used in PCBs. Unlike the spiral or helical windings of a conventional transformer, those in a planar transformer are printed on a flat surface and extend outwards from the center of the core. In figure 3.3(b), the internal make up of two PCBs, one for the primary and the other for the secondary, are shown in a 3D image. This representation also depicts how there are different winding configurations per layer, and how they interconnect through the use of vias (holes filled with copper to interconnect different layers). Figure 3.3 is a typical planar transformer where the core halves can be joined together with tape, glue, or clamps. There is also a hybrid planar transformer (not shown) that is composed of both integrated PCB windings and traditional helical windings connected to the surface of the PCB.

Apart from the winding, the core is the other main component of a PT. There are different core types (soft magnetic materials), such as ferrites, nanocrystalline, and iron based, each with unique properties that are suited for different applications. Generally, for PTs, the operating frequency is much higher and ferrites are the preferred core type. This is due to the naturally high resistivity in ferrite cores which results in insignificant eddy current losses and reduced core losses compared to other materials at high frequency [46].



(a)



(b)

Figure 3.3: (a) Planar transformer made of multilayer circuit boards. The PCB is located around the smaller-sized ferrite E core. [44] (b) 3D representation of a primary side PCB (left) and secondary side PCB (right) where the start and end of the winding is shown as well as the different winding configuration of each layer. [45]

3.2 Electromagnetic Theory

In this section, the relevant electromagnetic background theory, pertaining to planar transformer design, will be explained. The permeability (μ), the capability of a material to conduct flux, is a key design parameter when selecting the transformer core. The permeability is influenced by frequency and temperature. The permeability of a material drastically drops off at the curie temperature, a material parameter. It is formulated by the ratio of the flux density (B) to the magnetizing force (H).

$$B = \mu H \ \ [gauss] \tag{3.1}$$

The magnetic flux density is the flux divided by the core cross-sectional area, therefore the flux density can also be formulated as equation 3.2.

$$B = \frac{\phi}{A_c} \ \ [gauss] \tag{3.2}$$

H can be defined as a force per unit length and this force is directly proportional to the magnetomotive force (mmf). However, the mmf should not be confused with the magnetizing force, H, because they have a cause and effect relationship. Both are defined in equations 3.3 and 3.4, respectively, and are derived from Ampere's law.

$$H = \frac{mmf}{MPL} \left[\frac{gilberts}{cm} = oersteds\right] \tag{3.3}$$

$$mmf = 0.4 * \pi NI \ [gilberts] \tag{3.4}$$

Therefore,

$$H = \frac{0.4 * \pi NI}{MPL} \ [oersteds] \tag{3.5}$$

MPL is the mean path length in centimeters, N is the number of turns, and I is the current in Amperes. Generally, the magnetic circuit (composed of reluctance, flux, and mmf) is used to analyze the circuit and define the effects from occurrences such as air gaps in the magnetic core. The magnetic circuit is quite similar to its electrical circuit counter part where the reluctance, flux, and mmf function similarly to the electrical circuit's resistance, current, and voltage, respectively. Figure 3.4 provides a visual representation of the different core parameters including the addition of an air gap. An air gap can be used to handle the DC flux in the core. It is represented by a large reluctance in the magnetic circuit and is the main contributor to the change in the permeability of the core. Therefore, when designing a transformer, it is imperative to consider the effects that the air gap causes to the value of permeability. μ_r is the relative permeability which is used to define the conductivity of flux in magnetic materials. The total permeability is a composition of the materials relative permeability and the permeability of free space (μ_o) which can be seen in equation 3.6.

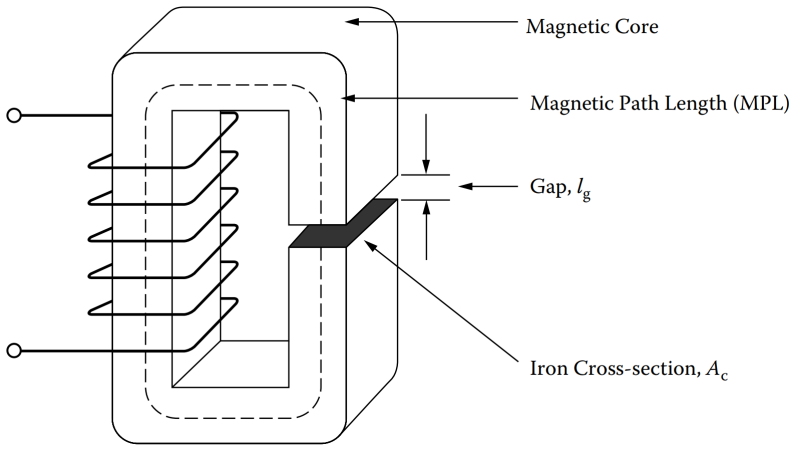


Figure 3.4: A basic magnetic core with an air gap [47]

$$\mu = \mu_r \mu_o \tag{3.6}$$

where μ_o is equal to $4\pi * 10^{-7} \frac{H}{m}$. Now considering the air gap l_g we obtain equation 3.7,

$$\mu_r = \frac{\mu_r}{1 + \mu \frac{l_g}{MPL}} \tag{3.7}$$

The magnetic flux density depends on the current, number of turns, and core parameters. When designing a transformer, the maximum magnetic flux density B_{max} must be determined in order to select a core which can handle the calculated value. Often the parameters for current and N are fixed based on the design requirements of the application, therefore, the magnetic flux density is controlled by the air gap. This conclusion is also described in [47] where it is stated that the flux density is controlled by the gap, for a given magnetomotive force (which is dependent on the magnitude of the current). Moreover, by using the above equations, we can generate an expression to show the main design equation for B and the air gap.

$$B_{max} = \mu_r \frac{0.4\pi NI_{max}}{MPL} \ [gauss] \tag{3.8}$$

if combined with equation 3.7, then,

$$B_{max} = \frac{0.4\pi N I_{max}}{l_g + \frac{MPL}{\mu}} \ [gauss] \tag{3.9}$$

Another equation can be formulated for magnetic flux density. The previous equations are displayed in units of gauss which is equivalent to one ten thousandths of a Tesla. The unit of Tesla can be expressed as volts seconds per meters squared and the following equation comes in this form and is useful in the design process.

$$B_{max} = \frac{V_{in,max}}{f_s A_c K_f N} \ [tesla] \tag{3.10}$$

The variable f_s is the switching frequency and the constant K_f is the waveform coefficient of the AC signal at the input of the magnetic structure. In switching converters this signal is typically a square wave and the value of the constant is taken to be 4.44. Equations 3.9 and 3.10 can be compared to see which situation produces a higher magnetizing flux. The core should be able to account for the maximum B_{max}. Each transformer winding has a magnetic inductance associated to it. The value for magnetic inductance is an important design parameter and its effects on the circuit vary with respect to the topology or application. The fundamental equation to describe inductance is defined as,

$$v(t) = L * \frac{di}{dt} \tag{3.11}$$

from this equation we can deduct that, for a given voltage, the inductance will limit the change in current over time. Furthermore, the inductance of a transformer is also affected by an air gap or change in permeability. Current carrying coils generate magnetic flux which is transmitted throughout the core. The magnetizing inductance L_m is representative of the flux that actually links to the core of the transformer.

$$L_m = \frac{\mu_o \mu_r N^2 A_c}{MPL} \ [henrys] \tag{3.12}$$

The value of L_m will have an effect on the rate of change in the current flowing through the transformer. In addition, similarly to the magnetic flux density, the implementation of an air gap will affect inductance.

$$L_m = \frac{\mu_o N^2 A_c}{l_g + \frac{MPL}{\mu}} \ [henrys] \tag{3.13}$$

Many core manufactures also provide an inductance factor abbreviated as A_L. This parameter usually comes in the units of nano-henry per number of turns squared (nH/N^2). The designer simply multiplies A_L by the number of turns squared to receive a value of L_m (not considering air gap). The method for designing magnetizing inductance depends on the required L_m for the application and the size of the air gap. Furthermore, the leakage inductance will always be a smaller fraction of magnetizing inductance. This should be kept in mind if a specific leakage is needed in the design.

3.2.1 Leakage Inductance

Operation of transformers at high frequencies presents unique design problems due to the increased effects of core loss, leakage inductance, and winding capacitance [47]. Unlike the magnetizing inductance, the leakage inductance is distributed throughout the windings of a transformer and it represents the flux that does not link to the core. Each winding has its own degree of leakage inductance which can be represented as a single parasitic L_k, as was seen in figure 3.1.

Turn-on voltage spikes are one of the main negative effects due to the presence of leakage. The energy stored in the leakage inductance can result in a spike that will always appear on the leading edge of the voltage switching waveform [47]. The energy stored in the leakage can be calculated by the following equation, note that it will increase with the load.

$$Energy = \frac{L_k(I_{pk})^2}{2} \ [watt - seconds] \tag{3.14}$$

The value of leakage inductance often becomes a design parameter in the transformer design process. This is the case when the leakage is used as the resonant inductance of the tank in a resonate converter or if the designer wants to limit the leakage inductance to reduce the unwanted parasitic effects. There is a general estimation that is used to approximate the value of leakage based on the magnetizing inductance of the core. However, this can be highly inaccurate and better estimations can be made based on the core geometry which has a large influence on the value of leakage inductance. A unique formula must be derived based on the core and the winding configuration and, although the calculation is fairly accurate, it is not a precise result. The following equation shows a possible leakage calculation where a, b, and c are winding length, window length, and insulation thickness, respectively, in cm.

$$L_k = \frac{\pi(MLT)N^2}{b}\left(\sum c + \frac{\sum a}{3}\right)(10^{-9}) \ [henrys] \tag{3.15}$$

This formula also shows that the magnitude of leakage is affected by the number of turns on the primary. Furthermore, thicker insulation (resulting in fewer flux lines to couple the two windings together) will increase the value of leakage inductance and is one of the negative effects when the user is required to implement higher levels of insulation. A larger window length can reduce the magnitude of the leakage and for that reason planar cores with long, wide, flat geometry have large window length and naturally reduce the value of leakage in this respect. In general, the leakage can be minimized by placing the winding of the primary, as close as possible to the secondary winding, using the minimum amount of insulation. This decreases the average distance between the windings and yields a fraction of the original magnitude of the leakage. In the case of a planar transformer, where printed circuit board layers are used, the only way to reduce the leakage inductance is to divide the primary winding into sections, and then sandwich the secondary winding between them. This process is also referred to as interleaved windings which can been seen in figure 3.5.

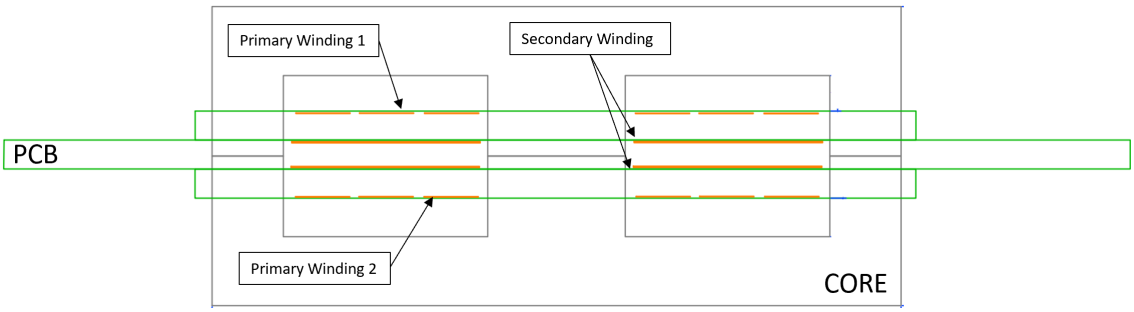


Figure 3.5: Cross sectional image of a planar transformer with 3 PCBs, a 6:1 turns ratio, and an interleaved winding configuration where the secondary is sandwiched by the primary

Interleaving reduces the AC losses because it reduces eddy currents in the traces, thereby increasing flux linkage to the core. Interleaving specifically targets eddy currents produced by the proximity effect (discussed more in detail in section 3.2.4). One last consideration should be given to maintaining a balanced DC resistance between the windings which becomes more of a concern when trying to interleave the windings. If the distance between the two windings is minimal this can result in unbalanced interwinding capacitance potentially leading to EMI issues. This imbalance can be minimized by increasing the insulation between the primary and secondary windings as much as possible, e.g. dielectric shield, tape, or auxiliary winding.

In summary, core and winding configurations, formulas, and general approximations can be used to pinpoint a general value of leakage inductance, but proper measurements should be taken in a lab setting to determine the leakage inductance and get the exact value. Actual measurement is one of two best ways to verify the value of leakage and should be done after the transformer or inductor is manufactured and is physically available for testing. The preferred method to measure the leakage

inductance will be discussed later in the results (chapter 6). The other method for obtaining a precise leakage inductance measurement is to use finite element matching (FEM) simulation with an accurate core and winding model. However, this is beyond the scope of this research. There are always design trade-offs between the distance separating the primary and secondary, core parameters, winding configuration, leakage inductance, and parasitic capacitance.

3.2.2 Winding Capacitance

Operating at high frequency presents unique problems in the design of transformers to minimize the effect of winding capacitance. Transformer winding capacitance has three main negative attributes. Firstly, it can introduce a premature resonance into the transformer. Secondly, the winding capacitance can produce primary current spikes when operating from a square wave source (which is typical in converters) and lastly, this parasitic capacitance can permit electrostatic coupling to other circuits. As can be seen in figure 3.1(a), there are multiple elements of capacitance that constitute the total parasitic capacitance of the circuit. The capacitance elements C_{pri} and C_{sec} are comprised of the capacitance between turns, between layers and stray capacitance while the winding-to-winding capacitance is represented separately as C_{WW}.

Keeping turns to a minimum and increasing the insulation spacing between the primary and secondary will keep the capacitance to a minimum. In the case where interleaving the primary and secondary windings is actualized, this minimizes the winding capacitance but it increases the winding-to-winding capacitance. In general, for design considerations, transformer parasitic inductance and capacitance have an inversely proportional relation; if the leakage inductance is increased, the capacitance will decrease, and vice versa, if the designer increases the parasitic capacitance, the leakage inductance decreases. The exception is the number of turns. A low number of turns will reduce the effect of both leakage inductance and winding capacitance.

3.2.3 Fringing Flux

When designing a transformer with an air gap, the designer should take into consideration the fringing flux factor, which can be seen in equation 3.16.

$$F_{FF} = 1 + \frac{l_g}{\sqrt{A_c}}\, ln\left(\frac{2W}{l_g}\right) \tag{3.16}$$

where l_g is the air gap and W is the length of the core window. If the fringing flux is not handled correctly, there could be premature core saturation. The fringing effect lowers the reluctance seen in the magnetic path and therefore increases the inductance of the winding. Furthermore, high frequency operation enhances the effects of fringing flux and its parasitic eddy currents. Fringing flux can reduce the overall efficiency of the converter, by generating eddy currents that cause localized heating in the windings and/or the brackets and due to this concentration of the flux in the magnetic core there are increased copper losses [48].

The presence of fringing flux can be utilized by the designer to reduce the value of leakage inductance in the windings closest to the air gap. The effect of fringing flux helps bind more flux to the core around the air gap. Placing transformer windings in this area can reduce the magnitude of the flux that leaks out of the windings [40]. Therefore, there is a connection to the size of the air gap and the value of the leakage inductance. This is more-so the case in planar transformers which are known for a low profile, fewer windings, and a closer proximity between the windings and the air gap.

3.3 Losses

3.3.1 Copper and Conduction Losses

Skin Effect and Proximity Effect

The AC copper losses in a transformer are composed of skin effect loss and proximity effect loss. They are similar because both effects generate unwanted eddy currents (a result of Farady's law) in the wire

or conductor. High frequency operation can increase the magnitude of these effects because of the natural tendency of current flow. Current flows in the path that yields the smallest expenditure of energy. At lower frequency, this pertains to the path of least resistance with respect to i^2R losses (uniformly distributed). At higher frequencies, current flows in the path that minimizes inductive energy or energy transfer to and from the magnetic field generated by the current flow (from [49]). The result of this behavior is that high frequency current concentrates close to the surface of a thick conductor resulting in a higher net resistance (higher i^2R loss) but minimizes the transfer of energy to the net inductance. This phenomenon is known as the skin effect. The numerical significance of this effect can be defined as skin depth (or penetration depth D_{pen}). D_{pen} is defined as the distance from the conductor surface to where the current density (and the field, which terminates on the current flow) is 1/e (Euler's number) times the surface current density and is defined as,

$$D_{pen} = \sqrt{\frac{\rho}{\pi \mu_o \mu_r f_s}} \ [meters] \tag{3.17}$$

where ρ , for copper, is equal to $2.3x10^{-8}\Omega m$ and μ_r = 1.

The proximity effect is caused by induced eddy currents due to the presence of an alternating magnetic field of other wires in close vicinity [47]. The existence of eddy currents cause a distortion of the current density (described above) and this "distortion" is the consequence of magnetic flux lines that generate eddy currents in the magnet wire which cancel out the main current on one side of the conductor while simultaneously enhancing the main current on the opposite side. In appendix C, there are figures that depict this situation in detail.

In summary, regarding the AC copper losses, it is an accumulation of both the skin and proximity effects. The skin effect is the result of the frequency, trace thickness, and thermal design of the magnetic component, while the proximity effect is the result of the winding configuration and number of layers. When calculating the total AC copper loss, the Dowell graph is used (shown in figure 3.6). The graph produces a value for R_{AC} and the total AC copper power loss can be calculated with respect to the current level.

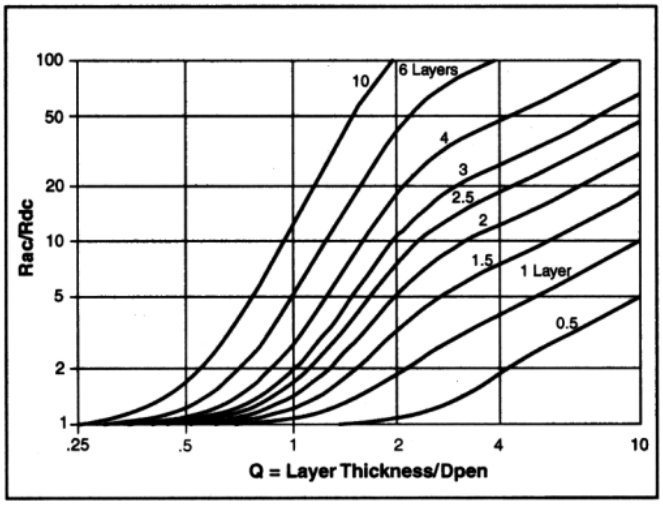


Figure 3.6: Dowell Graph where the x-axis is Q = layer thickness / D_{pen} and the y-axis is the ratio between R_{AC} and R_{DC}

For planar transformers, there are generally less layers and there is one standard copper trace (compared to multiple wire options e.g. litz, massive, etc...). Therefore, the main factors contributing to AC loss are the frequency and the parameters of the Dowell graph. There is also a consideration or trade-off between layer thickness and number of layers. Additionally, interleaving the windings, a natural characteristic available to PTs, reduces the AC resistance (by reducing the proximity effect) but increases the level of common mode noise [45].

Conduction Losses

The DC loss component, or conduction loss, of the copper traces is proportional to the magnitude of current and resistance. The electrical resistance of a conductor is associated to its total length l_w, cross-sectional area of the trace A_w, and resistivity ρ. This relation can be seen in the following equation,

$$R_{DC} = \rho \frac{l_w}{A_w} \ [ohms] \tag{3.18}$$

Often in planar transformers, each layer can have a different value for thickness, A_w, and lw (shown in figure 3.3(b)). However, as mentioned previously, there should be a balanced DC resistance in all the windings. This is not the case for the relationship between the primary and secondary windings and appropriate resistance calculation should be done for each side, respectively, according to the different winding resistance and current ratings for each side.

The total copper losses can be calculated as follows

$$P_{cu} = i_{pri}^2 R_{AC,pri} + i_{pri}^2 R_{DC,pri} + i_{sec}^2 R_{AC,sec} + i_{sec}^2 R_{DC,sec} \ [watts] \tag{3.19}$$

where R_{AC}, R_{DC}, and the current are considered separately for both the primary and secondary side.

3.3.2 Core Losses

Core losses are composed of hysteresis loss and eddy current loss. When a transformer is completely magnetized and then afterward demagnetized, the results can be seen in a hysteresis curve. The hysteresis diagram, based on DC current, describes the relationship between B and H but it also illustrates the energy lost in the core. The area inside the curve represents the total loss during one cycle which also signifies that the loss increases with frequency. As H increases, the flux density B increases along the curve until the saturation point (B_s) is reached. Core saturation causes the losses in the PT to intensify, possibly to a catastrophic degree, if thermal runaway occurs. The hystersis effect can be seen in figure 3.7.

The other component of core loss are eddy currents which were previously defined when describing the AC loss component due to the skin effect in the windings. If the core has a lower resistivity this loss mechanism will be of greater magnitude. It is the result of induced electromagnetic forces (EMF) on the core which cause circulating currents to flow. The eddy current losses are greater at higher frequencies.

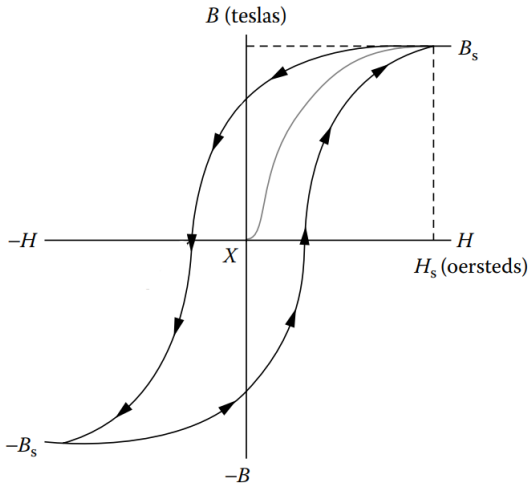


Figure 3.7: A typical hysteresis curve [47]

In practice, the core loss can be described in different ways. It can be displayed in a graph of power loss versus frequency and magnetic flux density or as a constant or variable that is provided by the

manufacturer (based on a set of testing conditions). In addition, the core loss can be approximated using FEM simulation. In summary, when it comes to core loss, a designer must be flexible and consider the method used by the core manufacturer as well as being aware of the constant reliant formulas derived in literature such as the Steinmetz equation below,

$$P_{hys} = k_h \, f_s^{\alpha} \, B_{max}^{\beta} * V_{core} \;\; [watts] \tag{3.20}$$

$$P_{ec} = k_e \, f_s^2 \, B_{max}^2 * V_{core} \;\; [watts] \tag{3.21}$$

where k_h, k_e α, and β are the Steinmetz coefficients which are material parameters and α / β are generally derived from the B-H hysteresis curve of a material. B_{max} is preferred in the design process in order to consider the worst case loss scenario. Furthermore, the core losses could be lower or higher depending on the waveform type (sin ,triangle, etc...) therefore adjustments can be made to the Steinmetz constants to account for changes in the form factor (harmonic distortion) of the waveform [50].

3.4 Planar Transformer Design and Construction

3.4.1 Design Process

The design process for a planar transformer varies on the application and requirements of the design. In order to account for this variability, figure 3.8 illustrates the process in a step-by-step generalized approach that can applied to a wide variety of different applications, specifically for PTs in power electronic converters. The flow diagram follows a sequential pattern until the blue highlighted stages. The early stages of the diagram are comprised of straight-forward calculations based on topology design equations (such as those presented in chapter 2) and the equations previously defined in the electromagnetic theory section. Moreover, a ”general plan” for the windings are presented as part of the early process. This is a good practice to ideate geometric requirements for the core. This pre-design visualization not only assists in the decision for core size but also for the shape of the core (E, U, EQ, R, etc..). The blue section indicates where the design process embraces a trial and error concept where there is a loop of steps that repeat until the loss due to B_{max} (from loss curve of core material) is less than or equal to the desired core loss condition is met. This reiterative process is not always focused on obtaining the B_{max} loss condition. The designer must be focused on the values and adjustments of N, L_m, l_g, and L_k as much as B_{max}. Consequently, this is the most lengthy part of the design process and computational scripts can assist in running multiple scenarios. The final stages of the diagram are related to finalizing the winding configuration as well as producing the information to implement FEM and thermal (loss) modeling. The following list is included to present some of the methods and trade-offs which can aid in the PT design process:

Methods

- Increasing ratio of turns, e.g. 7:1 to 14:2
  - Increases total L_m, L_k, flux saturation level, and resistance of the traces
- Placing multiple cores in series
  - Increases the A_c, flux saturation level, lenght of MLT, and resistance of the traces
- Configuring parallel traces on different layers
  - Enhanced current handling capability and reduction in losses (balanced DC resistances of traces must be maintained)

Trade-offs

- Reduce the number of turns
  - Higher core loss, lower saturation level, and lower L_m and L_k

- Reduce the thickness of conductors and insulators
  - Higher winding resistance, inter-winding capacitance and less L_k
- Increase the window width
  - Higher inter-winding capacitance, number of turns, and increased losses due to proximity effect

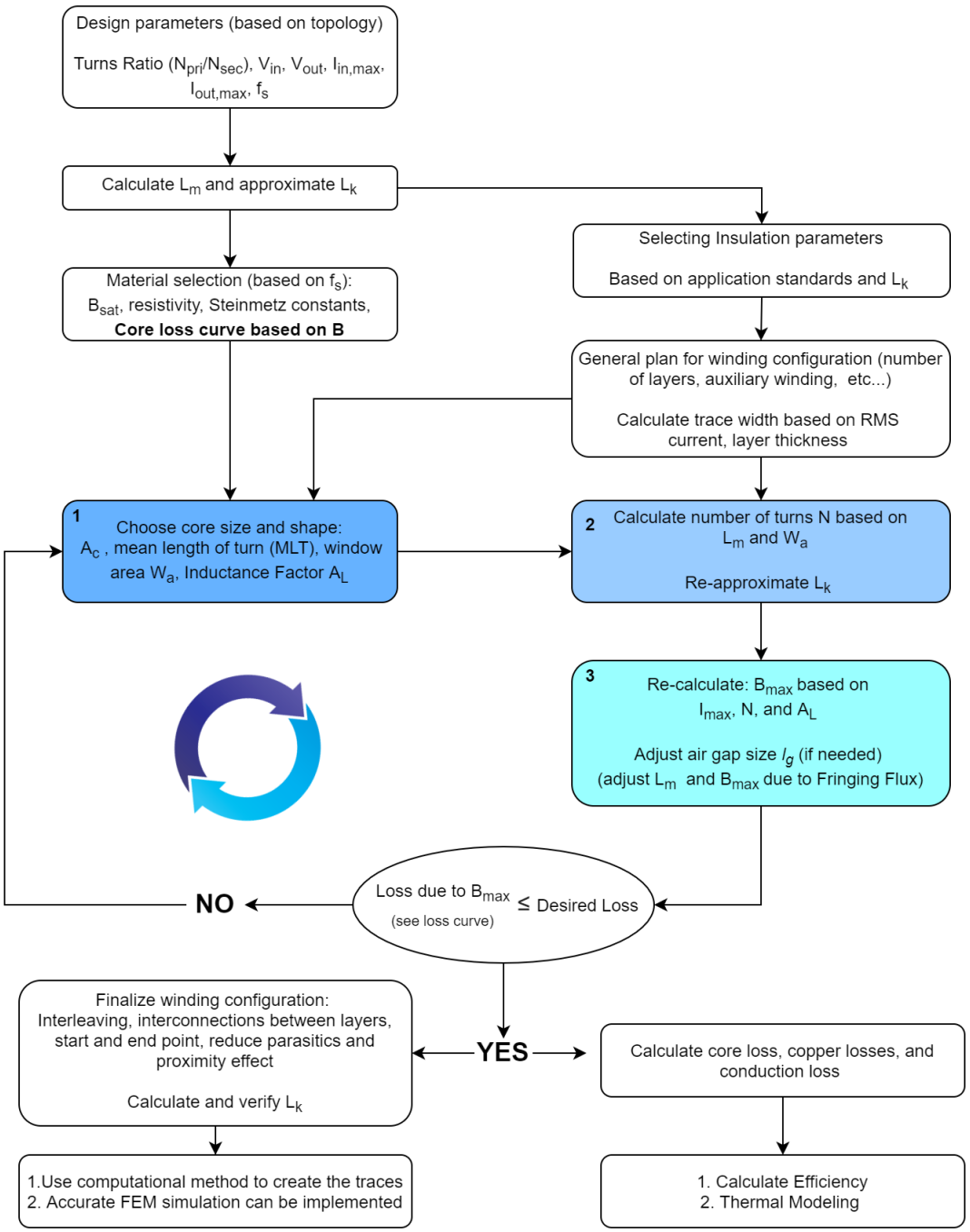


Figure 3.8: A flow diagram that illustrates the design process for a planar transformer

3.5 Coding Traces and Layout in Python

Once the design process is complete, the PCBs need to be constructed in order to fit effectively into the design. A Python script was created to make an algorithm for the traces and KiCAD software is used for PCB routing. A Python script can be activated through the use of KiCAD's scripting console. The process of properly constructing the winding becomes more complex as the number of turns and layers increases. It is more efficient and reduces the chance of user error (when routing by hand) to use code to generate the winding.

In order to compensate for a wide variety of different core types and winding configurations, multiple code blocks were written where each actualizes a different functionality. The final script is a composition of different blocks which are chosen based on the designer needs. The coding blocks and the variables associated to each block are defined in the following table:

Table 3.1: Table which outlines the individual components or blocks of the Python script. The inner rows share the same variables, apart from two unique cases which are depicted as such

	Block	**Associated Variables**
1	Core	Core Type (E or U) Core Dimensions (length, width, window length(s), length of leg, width of leg) Layer (edge cut)
2	Clockwise Winding (Arc)	Leg specification (primary or secondary side) Layer (4 possible layers) Thickness of trace Number of turns Clearance (between first trace and core- left and right sides) Scaling Clearance (between subsequent traces for N turns) Vertical Clearance (between first trace and core on top and bottom side) *** Unique Variables Arc: angle or degree (a constant fixed at 90) Octaganal: Diagonal length (length of top and bottom side diagonal in trace)
3	Clockwise Winding (Octagonal)	
4	Counter-Clockwise Winding (Arc)	
5	Counter-Clockwise Winding (Octagonal)	
6	Start/End Adjustments	Trace related variables to adjust position of start and end points

In order to connect individual layers, vias must be used. The number of vias used to make a connection is based on the current through the trace. Furthermore, the vias must not break clearance standards and cannot intersect with other traces on different layers. Therefore, the designer must consider layer connections and the start/end point for both the primary and secondary sides before starting the code. These connections must be planned before determining the orientation and placement of the windings. In the case where the planar transformer is designed externally from the main circuit board, mounting or castellated holes are placed on the edges to make connections between layers and to connect from the planar transformer to the main board. The paths after the start and end point should be as short as possible to reduce EMI and the overall DC resistance. An example of an output of the code is shown in figure 3.9 where the vias were placed by hand.

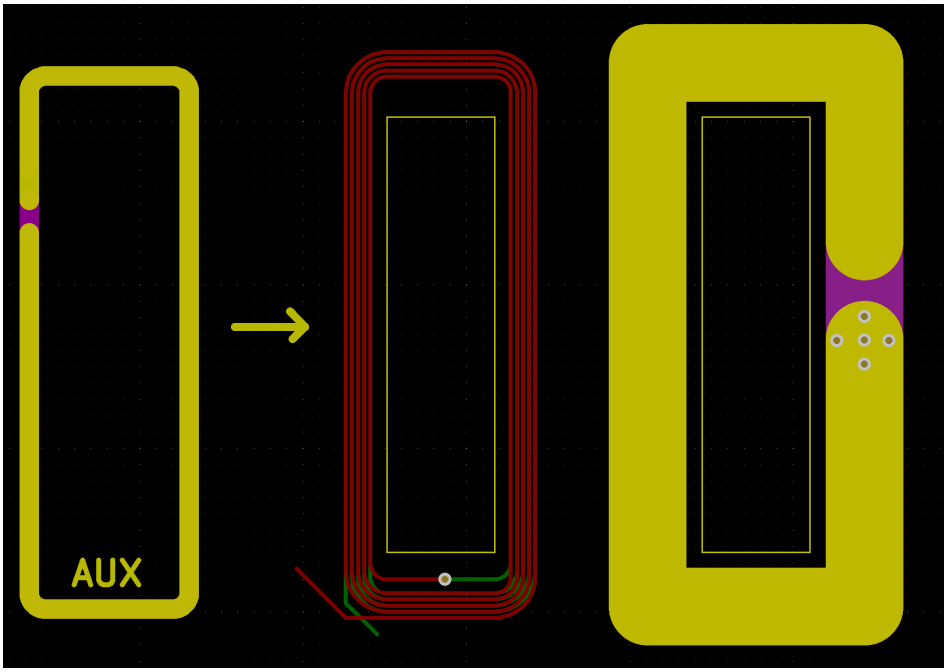


Figure 3.9: Traces generated by a python script. An auxiliary winding created with two layers in parallel was extracted from the primary side and shown on the left

As a last remark, this code can be improved upon with a consolidated, method-based, algorithm, less reliance on user inputs for adjustments and via connections, and the addition of a graphic user interface (GUI). The code was developed specifically for this thesis and its main purpose is for drawing the windings and outlining the core parameters to assist in the overall design process.

3.6 Conclusions and Findings

Due to the decreasing cost of multi-layer PCBs, planar transformers are gradually replacing conventional transformers, especially when smaller sized magnetic components are required (high frequency and lower power applications) [51]. Therefore, PTs are quite useful for power electronics utilized in rural electrification because these converters typically fall into this lower power category. The cores' reduced height (low profile) and greater surface area, when compared to a conventional magnetic core of equal volume, have improved heat dissipation capabilities [52]. The low profile also is useful when constructing rack-mount, or portable sized equipment. Alongside these benefits, the cores typically have a greater magnetic cross-sectional area which enables fewer turns and a reduces the magnetic flux density for a given current. Thick traces with a reduced path length replace wire wound windings of the conventional transformer which results in a smaller winding resistance (depends on application). The winding structure and inclusion of muli-layer PCBs naturally facilitates interleaving and simple interconnections (using vias) between layers. Interleaved winding lowers the magnitude of the leakage inductance L_k. Furthermore, interleaving can reduce the proximity effect in the copper traces lowering the AC winding resistance. However, in inductors and flyback transformers using air gapped center-legs, certain winding configurations can often result in greater AC winding loss [52].

The windings for planar transformers are manufactured by machines that are both precise and consistent. This results in winding structures with highly controllable and predictable parasitic parameters and low tolerance cuts. These PTs have superb reproducibility due to the precision of the manufacturing process. Furthermore, with low cost PCB manufacturing, the overall price compared to a conventional transformer of the same size is lower and a bobbin is generally not needed for PTs. The final advantage discussed is the flexibility and capability to adjust the design as needed. The design of the windings as well as core selection can be easily changed in order to tweak the design parameters. This is a very useful trait during prototyping or in modular systems that require increasing power handling capabilities

at each stage. In order to complete the analysis, some of the main limitations of planar transformers, discovered over the course of the thesis, are listed below:

- Increased footprint area
  - larger surface area, for a given volume, when compared to conventional transformer
- Reduced window area
  - the window area of planar core is much smaller than the cores used in conventional transformers
- Limited selection of planar cores for shapes other than E-planar
- Low copper fill
  - PCB trace windings have lower copper fill factor about 0.25 where as conventional windings have around 0.4. This is due to the fact that the windings in PCBs has higher spacing between turns and dielectric thickness [53]

Chapter 4

Unidirectional LLC Prototype Modeling, Design, and Construction

This chapter presents the complete design process for the unidirectional Half-bridge LLC DC/DC converter. The process includes simulations, transformer design, thermal considerations, and the PCB layout.

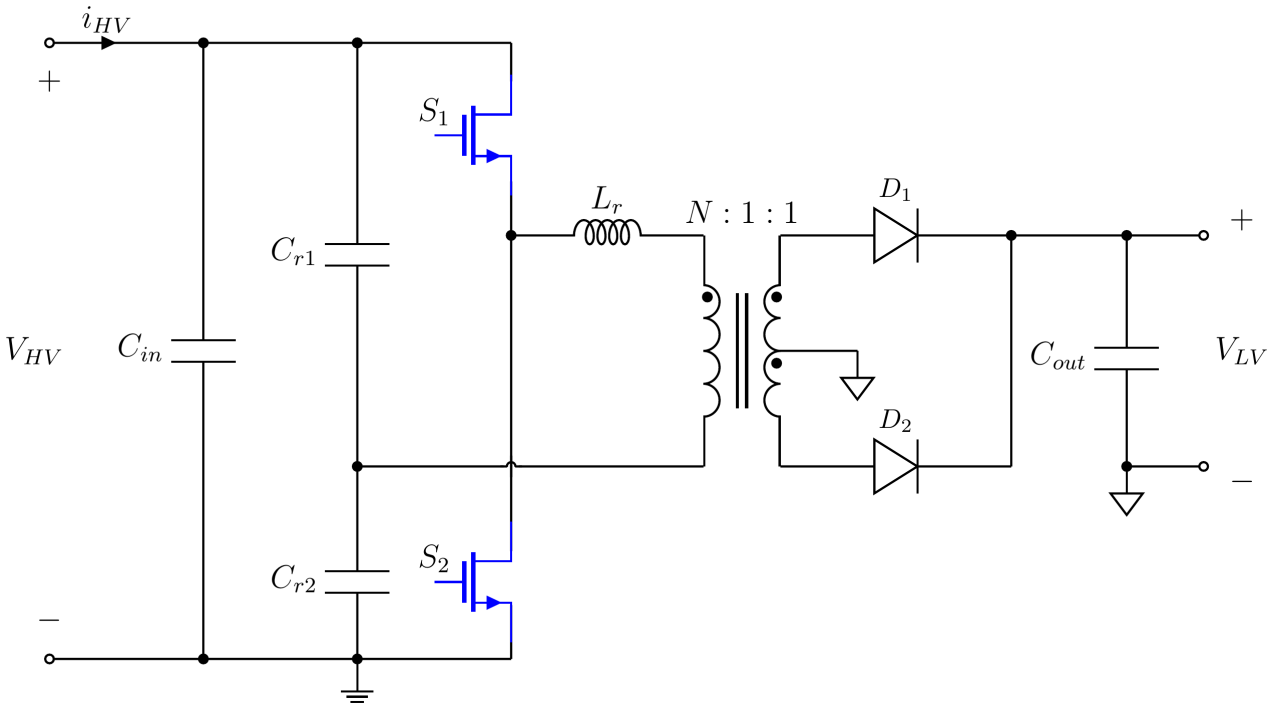


Figure 4.1: Basic Schematic for the unidirectional LLC converter where L_r = L_k

4.1 Preliminary Design

The half-bridge LLC was chosen as the converter topology for the rural electrification DC microgrid to household unidirectional power electronic interface. The basic schematic of the design can be seen in figure 4.1. The center-tapped secondary side includes rectifying didoes and therefore, there is no active synchronous rectification. The converter was designed for a resonant frequency f_{R1} of 1 MHz. The input voltage range is 300-400V, settling at a nominal value of 350 V. The output voltage range

is 20-30 V, which is an uncommon output voltage range that is specifically for this rural electrification application. This converter is part of a modular solar home system (containing USB-C connections for loads). The maximum operation voltage of USB type C power delivery is 20V which signifies that the converter output should never drop below 20 V. This converter is the component of the modular system that interconnects a SHS to a DC microgrid. The batteries in the solar home system, depending on the state of charge (SoC), have a voltage that can range from 21 (when batteries are empty) to 28.5 V (fully charged).

The schematic in figure 4.1 depicts a split resonance capacitor on the primary side. This is a slight variation of the typical half bridge LLC where the two capacitors are connected in parallel to the switches. If each capacitor has a value of $C_r/2$, they add together so that the capacitance of the resonant tank is equal to C_r. This is implemented in order to mitigate the current stress into two equal capacitors and reduce the initial imbalance in the rise volts-seconds applied to the transformer during the start up. The currents through the switches remain unchanged and the configuration will decrease the stress of the input capacitor and the input differential mode noise [19].

The main half-bridge LLC design equations are adapted from [19], [22], and [54]. The turns ratio of the transformer is determined based on the desired input to output ratio. It should be noted that the turns ratio is different than the number of turns on the primary and secondary sides, respectively. Generally, N is defined as N_1/N_2.

$$V_{out} = \frac{1}{2} N * V_{in} \tag{4.1}$$

Next, the desired total power is determined to be 240 W, as defined in the design parameters of table 2.1. After determining the total power, the output load range can be determined. Figure 4.2 shows the equivalent circuit model used as a reference in the design of the half bridge LLC converter.

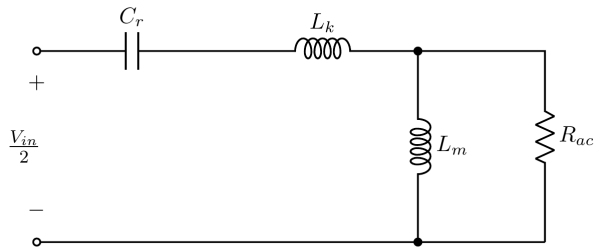


Figure 4.2: Equivalent circuit model for an LLC resoanct tank where $L_m >> L_k$

The values of C_r and L_k were selected based on obtaining f_{R1} while meeting the requirements of equation 2.2. Moreover, the value of L_k depends on the transformer design. The approximations for L_k presented in chapter 3 were used to pinpoint a leakage value. The value for C_r was adjusted based on the predicted leakage and its total stored energy. L_m is determined from the f_{R2} (equation 2.3), the desired L_{ratio} (L_p/L_k), the number of turns, and dead time (time needed for ZVS to occur) based on equation 2.4. The magnitude of the air gap (required in a HF LLC converter) also factors into the value of L_m. The value of L_{ratio} should be determined to meet the requirements of the application and the desired frequency range of operation. A higher L_{ratio} separates the two resonant frequencies over a wider frequency range and has small conduction losses due to smaller circulating currents. A smaller L_{ratio} yields a narrow range for frequency modulation and the output gain will rapidly change with a small frequency adjustment. Additionally, the smaller ratio will have higher circulating currents and more losses.

R_{ac} is the load impedance reflected over the transformer to the primary side. There is a square wave waveform coefficient of $8/\pi^2$ to produce a more accurate approximation of the impedance.

$$R_{ac} = \frac{8}{\pi^2} * \frac{R_{load}}{N^2} \tag{4.2}$$

Where R_{load} varies depending on output load requirement. With a completed equivalent circuit model, the quality factor (Q) at different loads and the transfer function of the resonant tank can be

derived. The following equation defines the quality factor which is representative of the magnitude of reactive power in the tank.

$$Q = \frac{1}{R_{ac}} * \sqrt{\frac{L_k}{C_r}} \tag{4.3}$$

A high Q means that there is significant current circulating (the reactive power is high) resulting in a large phase shift between waveforms in the power transfer. At a smaller Q, the waveform overlap duration (the phase of external energy re-circulation) is smaller which means there is less reactive energy and an improved energy transfer process (less losses). This value is important when diagnosing the operation points where the designer can expect higher circulating currents. The size of the air gap, and therefore magnitude of L_m, will effect the magnitude of circulating current. If the magnetizing inductance decreases, the circulating current will climb to higher peak values.

The transfer function, derived using Kirchhoff's current law in the circuit of figure 4.2, is presented below:

$$\frac{V_{out}}{V_{in}} = \frac{Z_m * R_{ac}}{(Z_k + Z_{cr}) * (Z_m + R_{ac}) + (Z_m * R_{ac})} \tag{4.4}$$

where Z_m, Z_{cr}, and Z_k are the Laplace transforms of the impedance L_m, C_r, and L_k, respectively. This transfer function is used to plot figure 4.3 which portrays the gain versus frequency curve used in both the control and design process.

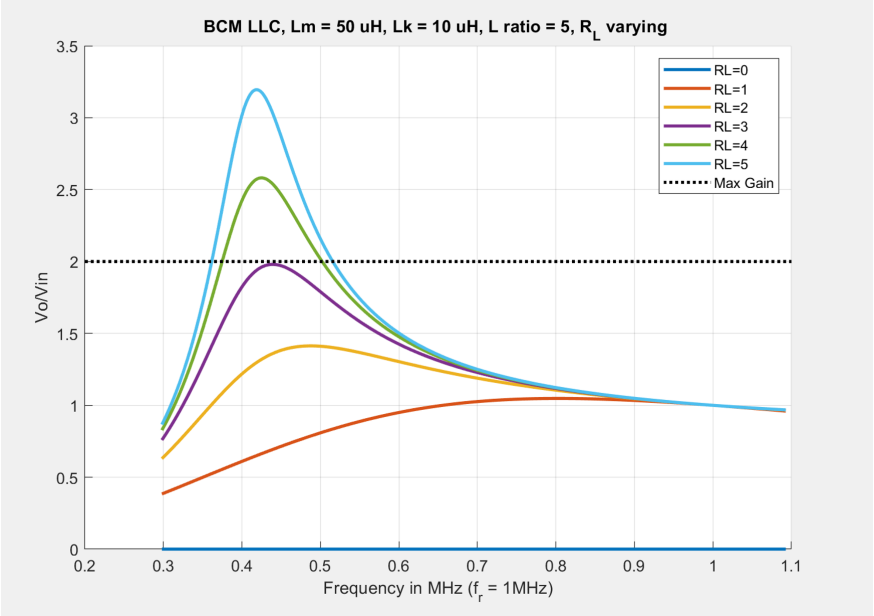


Figure 4.3: Gain curve for the designed LLC converter, where f_{R1} = 1 MHz and the black dotted line represents the maximum gain of the system which would be the worst-case-scenario if V_{in} was 300 and $Vout$ needed to be 30 V

The input and output capacitances of the half-bridge LLC converter are determined based on the amplitude of the ripple voltage seen at the input and output, respectively. The duty cycle, load current, and switching frequency (f_s) are the main factors that affect the magnitude of the input voltage ripple [55]. The value for capacitance must be designed to tolerate the maximum energy that is received from the power transfer. Ceramic capacitors are selected because of the low equivalent series resistance (ESR). The design considers the maximum limits as well as transients seen which can boost the output ripple. The document presented in [55] provides an in-depth explanation for the input and output capacitor selection process referenced for this design. The following formulas were used to determine the minimum value for input/output capacitances in order to produce an output voltage ripple (V_{pk-pk}) of 1% of the nominal 24 V output voltage.

$$C_{in(min)} = \frac{i_{L(pk-pk)}}{8 f_s V_{pk-pk}} \tag{4.5}$$

$$C_{out(min)} = \frac{I_{out} * dc(1-dc)}{f_s * V_{pk-pk}} \tag{4.6}$$

Where $i_{L(pk-pk)}$ is the current ripple in the series inductance component of the tank and dc is a 50% duty cycle. The remaining parameters needed to complete the design are the value for the currents seen in the primary tank and at the output of the center-tapped transformer. Mathematical approximations for DC current can be obtained from the P=VI relation for the input and output but it does not account for the value of circulating current that can increase the overall current flowing in the tank. The following two equations, referenced from [54], provide an additional estimation for the RMS current value of the primary and secondary side currents in the tank for a half bridge LLC converter.

$$I_{rms(tank)} = \frac{0.25 * V_{out}}{(\sqrt{2}N * R_{load})\sqrt{(N^4 R_{load}^2 T_s^2 / L_m^2) + 4\pi^2}} \tag{4.7}$$

$$I_{rms(sec)} = \frac{\sqrt{3} V_{out}}{24\pi * R_{load}} \sqrt{12\pi^4 + ((5\pi^2 - 48) N^4 R_{load}^2 T_s^2 / L_m^2)} \tag{4.8}$$

Where N = N_{pri}/N_{sec} and T_s is the switching period. A MATLAB script was created for the calculations in the design. A complete summary of the numerical results are presented in table 4.1. All of the values are based on the design process described above and in the LLC section of Chapter 2.

Table 4.1: All of the parameters used in the preliminary design phase and for simulating the converter

Preliminary Design		Resonant Tank		Control	
Parameter	**Value**	**Parameter**	**Value**	**Parameter**	**Value**
V_{in} (range)	300-400 V	L_k	10 μH	τ_{dt} (min dead time)	17 ns
V_{in}(nominal)	350 V	L_m	70 μH	*Duty Cycle*	*50 %*
I_{in} (max)	800 mA	L_{ratio}	7	f_s gain of 2	425 kHz
V_{out} (range)	20-30 V	C_r	2.5 nF		
V_{out}(nominal)	24 V	$I_{rms(tank)}$	1.46 A_{rms}	**Input/Output Capacitance**	
I_{out} (max)	10 A	$I_{rms(sec)}$	9.47 A_{rms}	**Parameter**	**Value**
N Primary	10 turns	f_{R1}	1 *MHz*	C_{in}	2.2 μF
N Secondary	1 turn	f_{R2}	355 *kHz*	C_{out}	22 μF
R_l(nominal)	2 Ω	R_{ac}	162 Ω		

4.2 Transformer Design

The planar transformer was designed based on the process outlined in-depth in the flowchart presented in figure 3.8. The methods and formulas used to determine many of the important design parameters for the PT are highlighted in chapter 2 but the choice of the core and winding configuration due to safe extra-low voltage SELV requirements will be discussed thoroughly in this section.

The SELV regulations required for applications in rural electrification denote that there must be sufficient isolation between primary and secondary side windings. In the IEC 60364 [8] SELV standardization document, in order for a transformer to have sufficient isolation (through air) at a primary side operation voltage of 420 V with up to 2500 V of mains transient voltage, 4 millimeters of clearance and 5 millimeters of creepage are needed to obtain reinforced isolation. These isolation related parameters are considered when determining the appropriate size for the core, specifically, a large

enough window area to allow for sufficient clearance. The recommended trace widths for the primary and secondary side were also considered to select the core. The transformer required 10 primary side turns each of which can handle up to 1 A of current. The secondary side required 2 windings, 1 for each center-tapped winding, with maximum of 10 A of current. The KiCAD software has a built-in trace width calculator based on the layer, temperature rise, and current level expected.

The final aspect that was considered for the core selection was the expected leakage inductance. The overall goal was to design a PT that had 10 μH of leakage using a common winding configuration (not interleaving). The winding configuration, 10 turns in total, split over 4 layers (1 on top, 3 on each of the remaining 4 layers), is shown in figure 4.4.

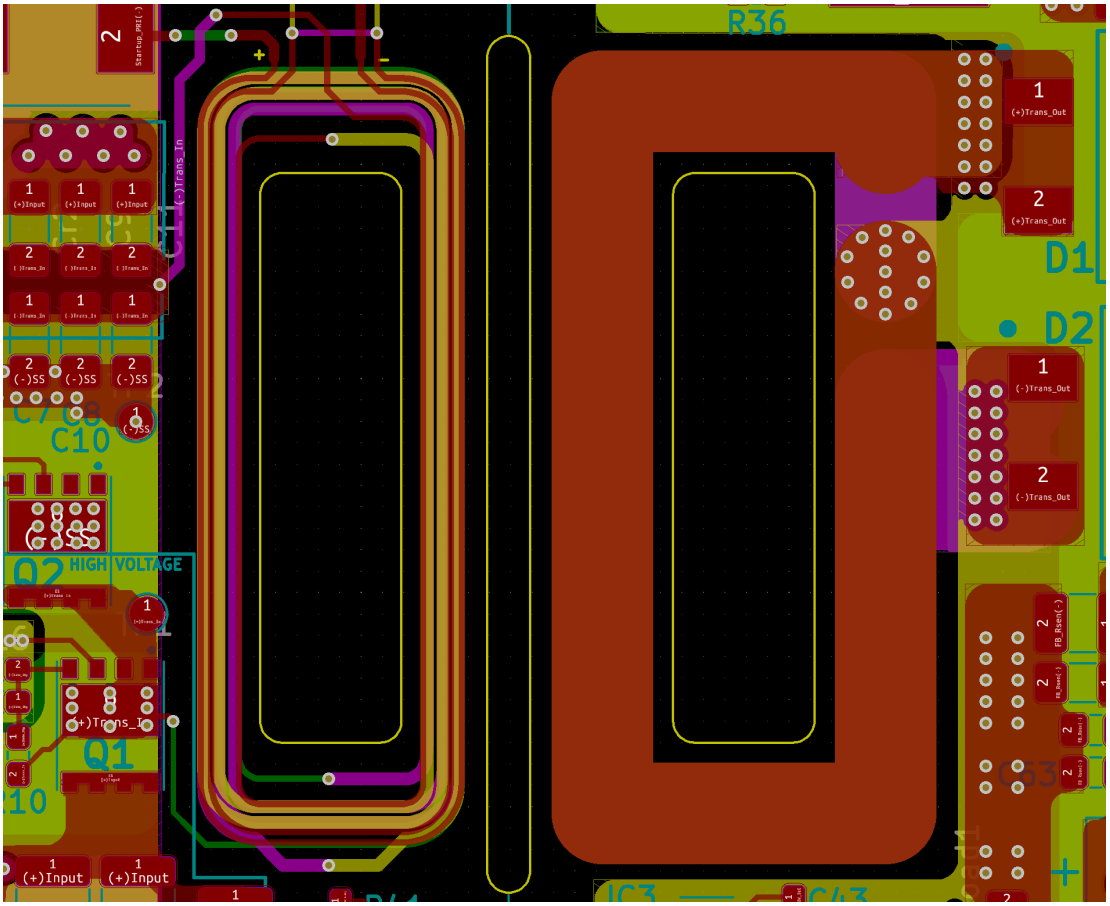


Figure 4.4: Layout of the planar transformer for the unidirectional half-bridge LLC converter. The top layer (red), primary side (left), includes 2 parallel traces creating an auxiliary winding and one primary turn (out of the 10 required turns). The secondary side is a center-tapped configuration with 2 turns, each containing one inner layer in parallel in order to increase current handling.

Journal article [56], a well referenced guide which compares core types and magnitude of leakage, describes the well-known planar E-core as the best core for minimizing leakage only when interleaving is implemented. If the windings are wound in a conventional manner (as seen in figure 4.4 where primary and secondary are not interleaved), the leakage inductance is less in core types, such as the U-core, where the leakage is 2.4 times lower compared to planar E. This numerical ratio is only valid for a certain testing scenario but the reason for this, in general terms, is that there are thinner windings and shorter length of a turn in the U core compared to the planar E-core. The planar E-core is known for its low profile with a large surface area compared to a U-core of the same volume. In conclusion, the U-core was selected as the core type for this PT because it allowed for a conventional winding configuration where the primary and secondary can be adequately isolated. Furthermore, a high number of turns would produce significant leakage for the resonant tank inductance, but it would be a leakage of lesser magnitude compared to that of a planar E-core. The U-core also has a greater height and the air gap location (with respect to the windings) can be used to manipulate the value of leakage inductance. Due to the presence of the fringing effect, the primary side leakage inductance

can be minimized by placing the primary windings (or PCB) near the air gap. This gave the design a bit of leeway for adjusting the value of leakage by utilizing the ample space available in the vertical window when changing the PCB location with respect to the air gap.

The transformer core in the LLC converter, especially for high frequency applications, has an air gap to reduce the value of L_m. ZVS is dependent on a relatively large magnetizing current. This current must flow into the anti-parallel diode of the switch during the dead time to allow for ZVS. Equation 3.13 was used to determine the length of the air gap. The following table includes the relevant design parameters for the planar transformer:

Table 4.2: The relevant design parameters for the half-bridge LLC planar transformer. The PCB layer thicknesses are 0.035 mm and 0.0175 mm for the outer and inner layers, respectively.

Core Parameters			Winding Parameters	
Parameter	**Value**		**Parameter**	**Value**
l_g (air gap)	0.5 *mm*		$l_{w(primary)}$	880 *mm*
A_{core}	4*40.6 μm^2		$l_{w(secondary)}$	180 *mm*
MPL	83.4 *mm*		$Width_{\,inner(primary)}$	0.6 *mm*
A_L	3180 nH/T^2		$Width_{\,outer(primary)}$	0.3 *mm*
Clearance	4 *mm*		$Width_{(secondary)}$	4.75 *mm*
Creepage	5 *mm*			

4.3 Simulation

Simulations were done in LT Spice for the unidirectional half-bridge LLC converter. The simulation was modeled with reference to the schematic shown in figure 4.1 and the values defined in table 4.1. A proper model for the GaN switch was downloaded from the GaN Systems website and other considerations such as, input impedance from cables, leakage inductance on the secondary side, and input and output capacitance are taken into account. An overview of the LT Spice simulation can be seen in appendix D. Lastly, a start-up circuit (designed to handle the powering of the micro-controller for the first few moments of operation) was simulated and designed in LT Spice.

4.4 Losses and Efficiency

An efficiency calculation was completed based on the design for the unidirectional half-bridge LLC converter. In order to produce a useful approximation, the following calculation is based on a steady-state 200 W operating condition at f_s equal to 1 MHz which is close to the maximum projected load of 240 W. The first loss component considered was the switching loss. It was assumed that ZVS turn-on would be achieved in steady state and that the main switching loss components would be conduction losses through $R_{DS(on)}$, dead time losses (P_{dt}) (more so at lower frequencies), gate charge loss (P_{gate}), and loss from the gate driver IC (P_{driver}). Apart from the gate driver loss, each loss mechanism is multiplied by two for each switch in the half-bridge. The following formulas were used for calculating the switching loss and the conduction loss formula is generalized for all cases.

$$P_{cond} = I_{RMS}^2 * R \tag{4.9}$$

Where I_{RMS} is the current flowing through the conductor and R is the resistance

$$P_{dt} = V_{diode} * I_{RMS} * \tau_{dt} * 2 \tag{4.10}$$

and where V_{diode} is the forward voltage drop of the diode in the switch.

$$P_{gate} = Q_{gate} * V_{gate} * f_s \tag{4.11}$$

$$P_{driver} = V_{in(driver)} * I_{cc} \tag{4.12}$$

Where I_{cc} is the supply current for the gate driver. Transformer losses are discussed in-depth in chapter 3. There are conduction losses in the windings (one component based on DC resistance and the other on AC resistance) and a core loss component. The losses due to AC resistance account for the proximity and skin effect in the copper. Independent conduction loss calculations are done for the primary and secondary windings, using equation 4.9, and they are added together. The core loss is derived from graphs provided by the manufacturer. Further information on these loss mechanisms can be obtained in chapter 3.

There are two Schottky diodes on the output and the losses for these components are comprised of conduction, reverse recovery (P_{rr}), and reverse leakage current $P_{Lk(rjev)}$ losses. Similarly to the parameters used to calculate switching losses, the parameters used for diode losses can be taken from the datasheet of the component in question. Furthermore, it is important to mention that the 50 % duty cycle control of the half-bridge LLC equally splits the stress on secondary rectifiers with respect to both reverse voltage and forward conduction current. Therefore, there is equal loss on each diode and the loss calculation can be done for a single diode and then multiplied by 2 for the total loss. The following formulas were implemented in order to calculate the diode losses:

$$P_{rr} = I_{pk} * \tau_{rr} * V_{fwd} * f_s \tag{4.13}$$

where τ_{rr} is the length of time for the reverse recovery to finish and V_{fwd} is the forward voltage drop of the diode.

$$P_{Lk(rev)} = dc * V_{out(max)} * I_{Lk(rev)} \tag{4.14}$$

Where dc is the duty cycle and $I_{Lk(rev)}$ is the reverse leakage current in the diode. The conduction losses in the diode are significant and can be calculated with equation 4.9. There are also conduction losses associated to the two shunt resistors included in the design of the half-bridge LLC converter. The final loss component in the analysis are losses in the power circuitry and this can be calculated from datasheet parameters and the rated current expected to be flowing through components (in steady-state). A 1 W approximation was taken for this loss component and it also compensates for any additional non-ideal losses that can occur in real life. Table 4.3 includes all of the values for each source of loss in the design.

Table 4.3: The individual loss components for all of the major sources of loss in the design. These values are calculated for the 200 W power operation condition where the input and output current are 0.8 A_{RMS} and 8 A_{RMS}, respectively.

Transformer Losses		**Switching Losses**		**Diode Losses**		**Power Circuity and Shunt Resistor Loss**	
Parameter	**Value**	**Parameter**	**Value**	**Parameter**	**Value**	**Parameter**	**Value**
Core	2.25 W	Conduction	0.212 W	Conduction	6.4 W	Shunt (primary)	0.047 W
Conduction (primary)	1.43 W	τ_{dt} (dead time loss)	0.64 μW	Q_{rr} (reverse recovery loss)	0.01 W	Shunt (secondary)	0.224 W
Conduction (secondary)	1.75 W	Gate Driver	0.144 W	Reverse Leakage Current	0.3 W	Power Circuitry	1 W
		Gate Charge	0.03 W				
Total Loss:	5.43 W	**Total Loss:**	0.386 W	**Total Loss:**	6.71 W	**Total Loss:**	1.271 W

Diode rectification conduction loss makes up the majority of the system losses. Transformer losses also contribute a significant amount to the total losses. $P_{loss(total)}$ can be calculated by summing all of the column loss totals (of table 4.3) together. The final efficiency calculation based on design parameters was completed using the following equation:

$$\eta_{HB-LLC} = \frac{200W - P_{loss(total)}}{200W} * 100 \tag{4.15}$$

Equation 4.15 yields an efficiency approximation of **93.1%** at 200 W power and a 1 MHz switching frequency.

4.5 Thermal Considerations

The results from the efficiency approximation show that the most significant component of power loss are the output rectifier diodes. A thermal calculation shows that the package temperature of the diode could get up to 100 degrees Celsius at 10 A of current, especially in a steady state situation. This calculation takes into account a large thermal copper pad that was integrated into the bottom layer on the secondary side. Its purpose is to help dissipate some of the heat of the rectifying didoes in high load conditions. The design has adequate space for a 10 x 8 mm heat sink in case the thermal pad is not sufficient to dissipate the heat.

Assuming ZVS and accounting for the small parasitics and no reverse recovery in the GaN HEMT, the switching losses do not need any additional consideration. Losses in the power, measurement, and other sub-module circuity should be minimal because of the low current level in these circuits. In the power circuitry, efficiency integrated circuit (IC) or chip technology is used such that losses are minimized. The remaining loss components are the windings and core of the planar transformer. The core losses shown in table 4.3 suggest the losses will not yield a high level of heating. As for the windings, they are designed to effectively handle the rated current levels; 1A for the primary and 10 A for the secondary.

4.6 Gate Driver and Layout Considerations

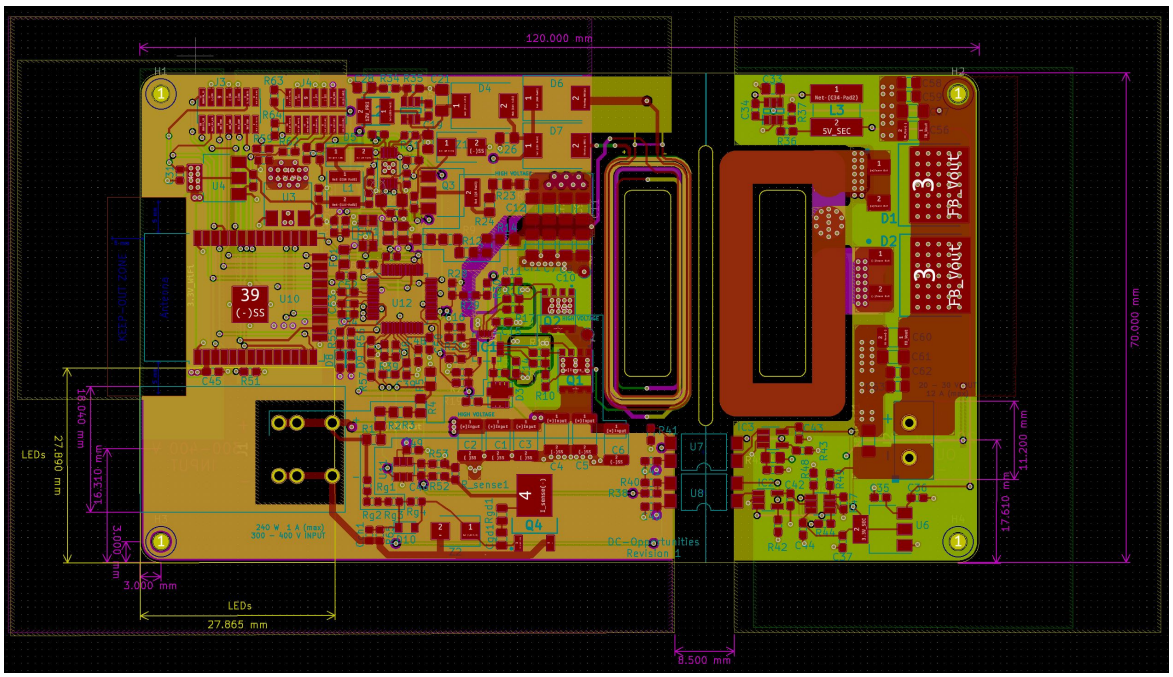


Figure 4.5: PCB layout for the unidirectional half-bridge LLC converter where the traces and footprints are shown. The red, yellow, pink, and green coloration depicts which layer the trace or footprint is on and they refer to the top, first inner, second inner, and bottom layers, respectively.

The placement of components on a PCB depends on the common mode noise, differential mode noise, and circulating current paths while simultaneously minimizing the total surface area of the PCB. Every application has unique configurations and present different current loops within the circuit. It is important to minimize these current loops because a longer path adds additional impedance to each connection. Stray inductance is a leading issue because this creates electromagnetic interference (EMI)

and it delays the current by introducing a di/dt relation to the path. Another cause of EMI is insufficient clearance between components. Figure 4.5 shows the PCB layout for the unidirectional half-bridge LLC converter. The common mode and differential mode noise paths are shown in appendix D. These loops were minimized as much as possible (seen in figure 4.5) to reduce adverse effects.

The routing of traces primarily depends on thermal characteristics (current handling), avoiding EMI, and limiting overall impedance when interconnecting different components. For this design, each of the 4 copper layers are responsible for a different type of trace (with occasional exceptions). The top layer (red) is the signal layer and where the components connect to the PCB. The second layer (yellow) contains the ground plane(s) and is where the ground exists for the whole PCB. The circuit has a primary side ground and an isolated secondary side ground where the split between the two grounds is centered through the clearance between the primary and secondary windings of the transformer. The third layer (magenta) is the power layer. Similarly to the ground layer, large copper planes are implemented in order to carry the required power, generally 3.3 V, to different parts of the PCB. The bottom layer (green) is mostly used for thermal planes (to dissipate heat) and to help create paths (connected by vias) that are not possible in the signal layer.

When choosing the width of the trace, the total current flowing between the two components of interest must be considered. Signal traces have low current but are sensitive to noise and should be routed, with appropriate clearance, from noisy components. Power circuitry can have larger currents and may need thicker traces. Datasheet referencing is a good way to check the maximum current that the IC or component will conduct. Power traces are responsible for conducting high, system-level, currents through the circuit and care should be given that these traces or planes do not cross-over or receive additional EMI from other sources.

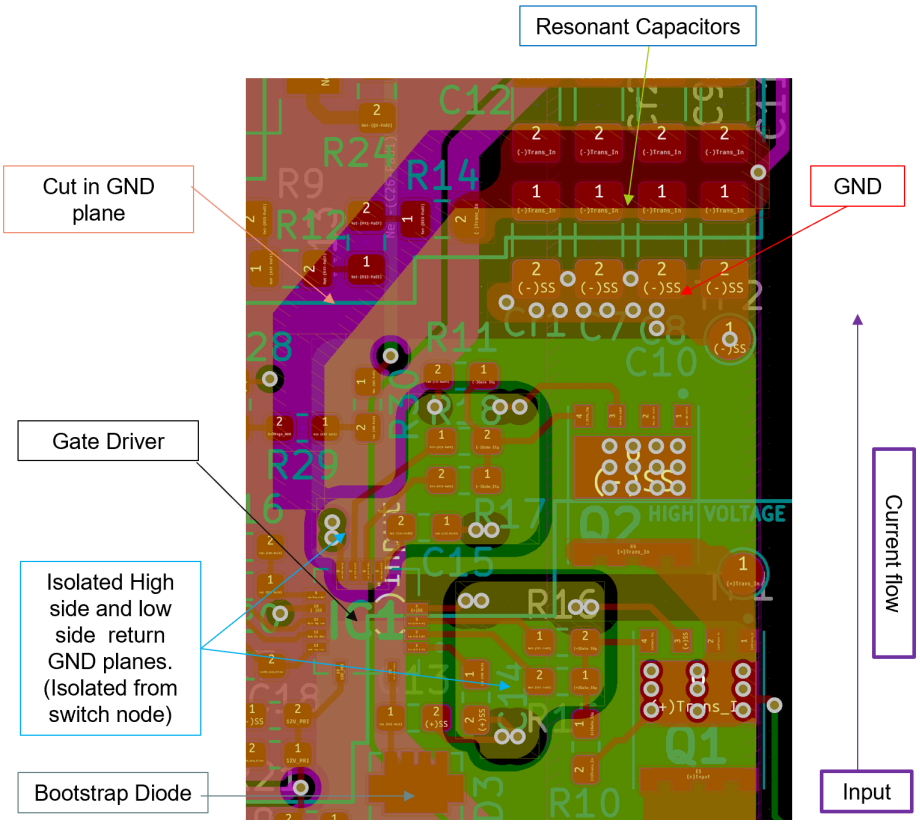


Figure 4.6: Layout of the GaN switches and gate driver designed to avoid any additional stray inductance from ground loops of current.

In chapter 2, the GaN HEMT was presented as well as the strict requirements that must be acknowledged when designing the gate driver circuit and its supplementary components. GaN switches can operate at high frequencies making them extremely susceptible to noise. This also applies to the gate driver circuitry. The component placement and routing for the power loop, switch−node, and the

current loops within the gate driver IC are critical design requirements for GaN. Moreover, components that are most sensitive to noise must be placed as close as possible to the driver IC.

For the given application, the power dissipation of the driver and the resulting junction temperature was verified to be within the operational temperature range. Secondly, a multi-layer PCB must be used for GaN applications because the application of isolated ground/return planes must be included. In the half-bridge GaN, there are two gate output signals; high and low. The design requires that they must be electronically isolated from one another, the high side must be isolated from the switching node, and the low side isolated from the system ground. Therefore, two dedicated copper return planes are needed (for the high and low side gate driver outputs) to properly configure a HF compatible circuit. Figure 4.6 presents a cut-out image of the gate driver, GaN switches, and the resonant capacitors. Additionally, the isolated return planes, component placement with respect to the gate driver IC, and traces connecting components can be seen. A cut in the primary side ground plane was included in order to direct current flow in a specific pathway from the input to the ground of the switching node.

4.7 Additional Modules and Controls

The half-bridge LLC converter contains multiple sub-circuits that support its operation. Powering circuitry, measurement circuitry, and a WiFi module, with supporting components, are included in the design. The input voltage V_{in}, output voltage V_{out}, voltage of the resonant tank V_{tank}, and voltage of the auxiliary winding V_{aux} are the voltage measurements collected. Furthermore, the input current I_{in} and the output current I_{out} are also measured with analog-to-digital (ADC) pins of the microcontroller. These measurements function as inputs to a proportional-integral (PI) feedback control responsible for the converters operation. The control algorithm produces the correct V_{out} based on V_{in} using measurements provided by a feedback line (composed of optocouplers and op-amps circuits).

The power circuity is comprised of 3 buck converters (a 12 V and two 5 V step-down conversions from a 25 V source), two LDOs to provide 3.3 V, a start-up circuit using a depletion mode MOSFET, and an auxiliary winding in the planar transformer. The design for each individual sub-module followed the same process of limiting current loops and reducing EMI. Furthermore, the datasheets for many of the IC's provide sufficient information to successfully design the circuits. Lastly, an input current limiting circuit was included in-between the line input and the input capacitors. This circuit was designed at DC-Opportunites R&D and its design is outside the context of this thesis. It was implemented in order to provide protection from an inrush of current during the start-up of the converter.

The controls for the half-bridge LLC converter require a PI controller but also overcurrent protection must be provided. This is to ensure that the converter never enters a capacitive mode of operation. Overcurrent protection also protects the circuit from excessive currents flowing in the transformer, resonant tank, switching node, and through the rectifier didoes at the output. Soft-start is another attribute added to the controls. Potentially destructive currents can flow into the circuit during start up and the soft-start control uses a high switching frequency (1.5 times f_{R1}) for a limited time interval to limit the current rise in each cycle.

Chapter 5

Bidirectional DAHB Prototype Modeling and Design

Chapter 5 presents the complete design process for the bidirectional DAHB converter. The process includes simulations, transformer design, and thermal considerations.

5.1 Preliminary Design

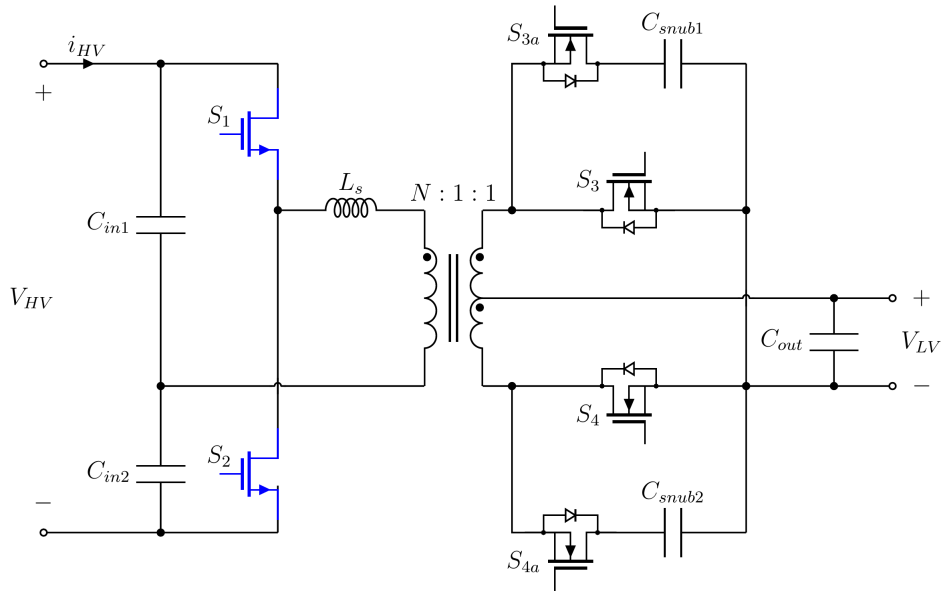


Figure 5.1: Basic Schematic for the bidirectional MDAHB converter

The dual active half-bridge converter was selected as the converter topology for the DC microgrid to SHS bidirectional power electronic interface. A schematic of the design is presented in figure 5.1. This converter is designed for the same application as the unidirectional half-bridge LLC converter described in chapter 4. Therefore, it is designed for the same input (300-400 V) and output voltage (20-30 V) ranges. However, the bidirectional DAHB converter is rated for 500 W and requires twice the current handling capability compared to the unidirectional version of chapter 4. The secondary side of this converter is a version of the push-pull or center-tapped secondary. In place of rectifier diodes, there are two MOSFET switches to preform active synchronous rectification in the forward direction and form a switching node for DC to AC conversion in the reverse direction. There are additional snubber circuits positioned in parallel to each secondary side switch. The main purpose of these snubber

circuits is to safely dissipate any energy stored in the leakage inductance of each center-tapped winding. Voltage spikes on the output waveform of the transformer can put unwanted stress on the output and reduce efficiency. Thus, it is critical to limit the value of leakage inductance on the secondary side to keep the value of the snubber capacitor smaller and reduce the magnitude of voltage spikes. The capacitors C_{snub1} and C_{snub2} were selected based on the amount of energy stored in the leakage inductance which is determined in the transformer design section. The secondary MOSFET switches were chosen to have 100 V drain to source voltage. The values of the leakage, snubber capacitance, and parasitic capacitance of the MOSFET can form a resonance. The design of the snubber leg takes into consideration its resonance in order to reduces its effects on the output waveform.

Equation 4.1 defines the input/output voltage relationship of a typical isolated half-bridge converter. This relationship applies to the DAHB primary which is the same as the primary side of the unidirectional half-bridge LLC converter. The only difference between the primary side of the two converters, is that a higher quality GaN HEMT (GS66504B by GaN Systems) with a 15 A drain current is used for both switches in the half-bridge. This switch was selected because of its superb hard-switching performance, low parasitics, and to compensate for the current collapse effect.

The design of a DAB converter depends on the modulation or control strategy. For the DAHB converter in this design, single phase shift control was selected as the modulation strategy. A modulation strategy with more degrees of freedom (duty cycle of primary, secondary, etc...) can allow for a wider operation range of soft switching. Single phase-shift control (SPC) is most efficient at larger loads and for a limited voltage range. The soft switching area of operation can be widened by reducing the parasitic capacitance of the switch (shown in figure A.2 of Appendix A). Low parasitic capacitances and less losses during hard switching are additional benefits of the GaN HEMT in a DAHB. The magnitude of magnetizing inductance, L_m, also affects the ZVS range. A smaller magnetizing inductance results in a increasingly lagging load which is a needed condition for ZVS. The downside for decreasing L_m is less efficient utilization of the transformer. If the application requires efficient switching at lightly loaded conditions, lowering L_m can be useful. However, a large L_m with no air gap in transformer of the DAHB is preferred. A larger L_m allows for the main energy transfer element in the tank to be the series inductance component, L_s, which is comprised of the auxiliary inductance, L_{aux}, and equivalent inductance, L_k, of the transformer. The following equation is a modified half-bridge version of equation 2.7 which characterizes the power transfer of a DAHB modulated with single phase shift control.

$$P_{DAHB} = \frac{V_{HB} V_{out} N}{2\pi f_s L_s} * (\Phi - \frac{\Phi^2}{\pi}) \tag{5.1}$$

Where P_{DAHB} is the total power of the DAHB, $V_{HB} = V_{in}/2$, Φ is the phase shift in radians, f_s is the switching frequency, and N is the turns ratio. This equation, the load requirements, and desired ZVS range determine the value of L_m. The value of f_s is also based on equation 5.1 and should be lower in order to reduce the magnitude of hard switching losses. It has a direct relationship to the energy transfer time and can limit the total power of the system. The number of turns and corresponding turns ratio is derived from equation 5.1. The process for selecting N becomes more complex depending on the modulation scheme and the tank configuration. Furthermore, the value for N is determined from the needed voltage step down/up from the transformer to achieve the desired output voltage. In general, the design for a single phase shift control DAB converter is a trial and error process with equation 5.1. The following two equations (adapted from [27]) define the maximum and minimum currents that occur in the primary side tank.

$$i_{L(max)} = \frac{V_{HB} * (2\Phi - \pi) + (N\pi V_{out})}{4\pi f_s L_s} \tag{5.2}$$

$$i_{L(min)} = \frac{-\pi V_{HB} + N(\pi - 2\Phi) V_{out}}{4\pi f_s L_s} \tag{5.3}$$

Current limits are considered in order to select the value of series inductance, design the windings, and select the core of the planar transformer. Figure 5.2 presents the phase versus power relationship based on equation 5.1. The d parameter represents the different input and output relationships that can happen due to the input and output voltage ranges. The power transfer in the DAHB occurs from leading bridge to lagging bridge. The control for the bidirectionally can be seen in the figure. The

first quadrant represents power transfer in the forward direction, whereas the third quadrant shows the power transfer characteristic in the reverse direction.

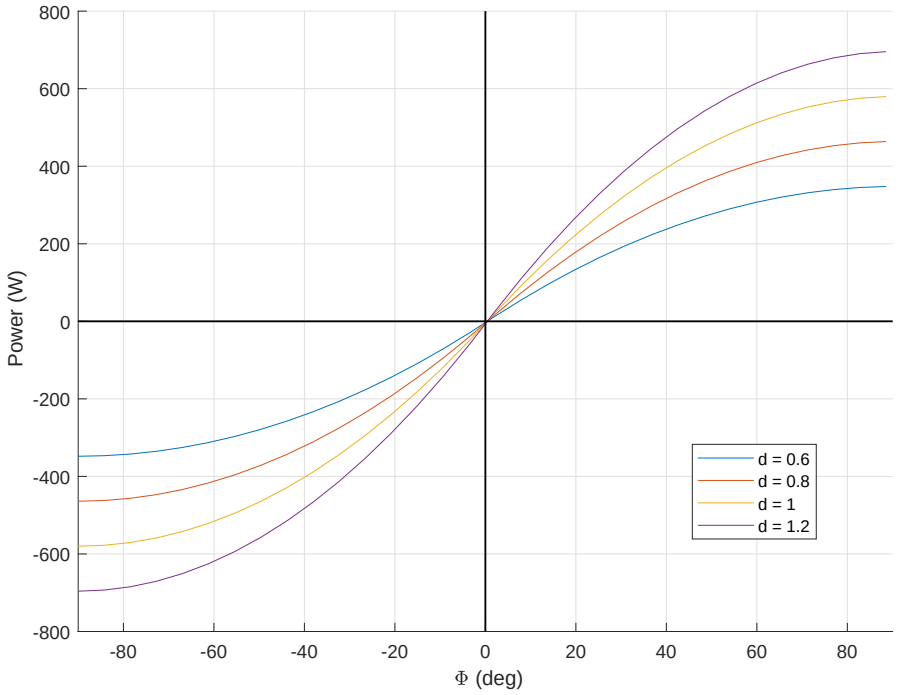


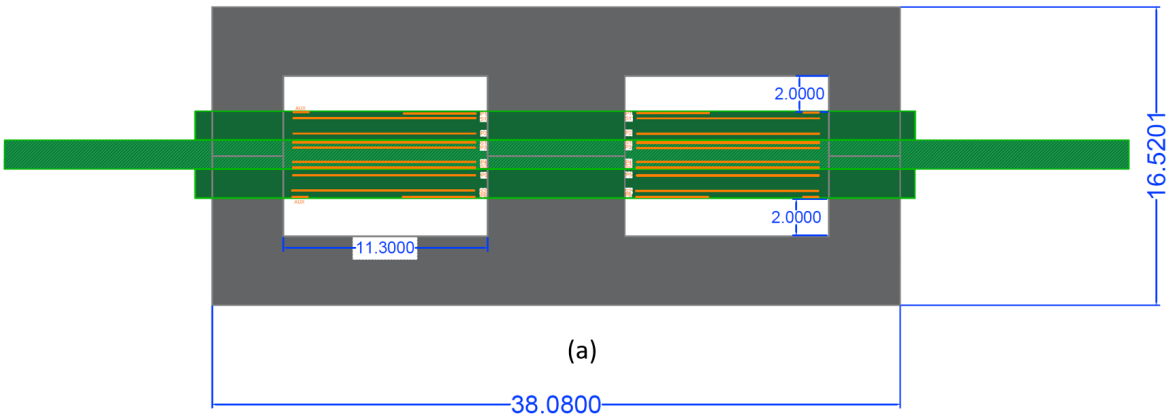
Figure 5.2: Phase versus power relationship based on equation 5.1. d is the input to output relationship $N * Vout/V_{HB}$ where $VHB = V_{in}/2$. d = 0.85 is the nominal 350 V input and 25 V output relationship

Additionally, figure 5.2 portrays the phase and output voltage relationship for a PI controller. The phase change will effect the output power and, consequently, the magnitude of output voltage and current. If a 20-25 V output voltage range is desired, the converter operates at a lower power level in order to drop the voltage. The value for input and output capacitance is the last consideration in the preliminary design. A characteristic of DAHB converters is to maintain a stable voltage at the input capacitor midpoint. Input capacitors C_{in1} and C_{in2} of figure 5.1 function as both input and DC blocking capacitors. A series blocking capacitor reduces the effect of voltage bias (when primary and secondary side are unbalanced). The input and output capacitances were calculated using equations 4.5 and 4.6, respectively. A MATLAB script was created for all of the calculations in the design. A complete summary of the numerical results are presented in table 5.1. All of the values are based on the design process described above and in the DAB section of chapter 2.

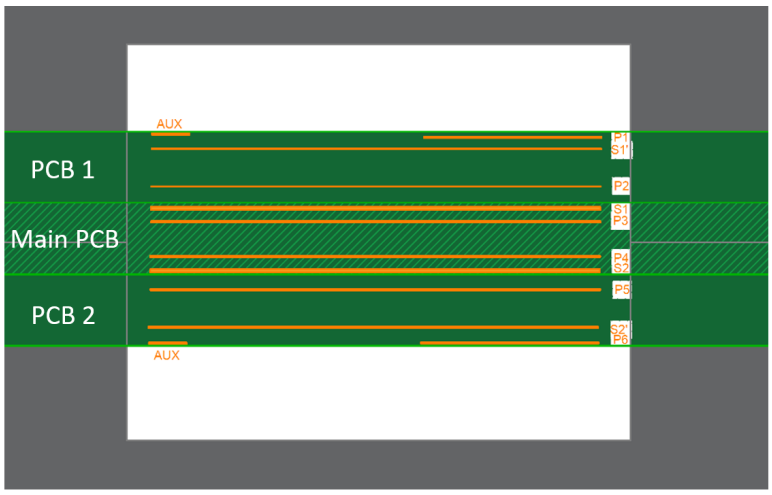
Table 5.1: The parameters used in the preliminary design phase and for simulating the DAHB converter

General Design		Power Transfer		Phase Shift	
Parameter	**Value**	**Parameter**	**Value**	**Phase**	**Power**
V_{in} (range)	300-400 V	L_k	*5 µH*	π/2 (90°)	511 W
V_{in}(nominal)	350 V	L_{aux}	30 *µH*	π/4 (45°)	377 W
i_L (max)	6.62 A	f_s	200 k*Hz*	π/8 (22.5°)	220 W
i_L (min)	-6.62 A				
V_{out} (range)	20-30 V	**Input/Output Capacitance**		**Control**	
V_{out}(nominal)	25 V	**Parameter**	**Value**	**Parameter**	**Value**
I_{out} (max)	25 A	C_{in}	30 *µF*	τ_{dt} (dead time)	100 ns
I_{out} (min)	16.7 A	C_{out}	150 *µF*	*Duty Cycle*	*50 %*
N (turns ratio)	6				

5.2 Transformer Design



(a)



(b)

Layer	Winding Configuration
1 (PCB1)	Primary 1 (P1) & Auxiliary winding
2 (PCB1)	Parallel secondary 1 (S1')
3 (PCB1)	Primary 2 (P2)
4 (PCB1)	(Empty)
1 (Main PCB)	Secondary 1 (S1)
2 (Main PCB)	Primary 3 (P3)
3 (Main PCB)	Primary 4 (P4)
4 (Main PCB)	Secondary 2 (S2)
1 (PCB2)	(Empty)
2 (PCB2)	Primary 5 (P5)
3 (PCB2)	Parallel secondary 2 (S2')
4 (PCB2)	Primary 6 (P6) & Auxiliary winding

(c)

Figure 5.3: (a) Complete cross-sectional area of the DAHB PT (including relevant core dimensions in mm) (b) Zoom-in of the cross sectional area of the left most window of the planar E-Core (in order to view the winding configuration) (c) Explanatory table for the layers and winding configurations

The planar transformer was designed based on the flowchart presented in figure 3.8 and the formulas provided in chapter 2. The design for the PT follows the same aforementioned SELV standards that were used when designing the PT of the unidirectional converter. However, instead of a U-core, a planar E-core is used in the bidirectional converter design. It is projected that using a planar E-core with interleaved primary and secondary windings (which meet reinforced isolation clearance requirements between layers) will yield a lower leakage inductance than a U-core with a conventional winding configuration. Moreover, the limited selection of U-cores further hinders its usage because often the needed core size is not available. Therefore, a new planar transformer design, with reduced leakage, is proposed.

A cross-sectional image of the planar transformer is shown in figure 5.3. The design will have 6 primary side turns interleaved with 2 secondary side turns, one for each center-tapped winding. Three multilayered (4 layers) PCBs are used in the design. The main PCB has a 2 oz copper weight for the top and bottom layers in order to handle the maximum 25 A of current that could flow on the secondary side in the worst-case scenario. The primary side windings must handle a peak current of 6.5 A (seen in table 5.1). A primary winding on an inner layer (0.5 oz) needs a width of 11 mm to meet the current handling requirement. The 2 external PCBs have conventional layer thicknesses (1 oz for top and bottom and 0.5 oz for inner layers).

The medium between all primary and secondary windings is the FR4 printed circuit board insulation material (not air). Therefore, in order to achieve reinforced isolation at a primary side operation voltage of 400 V with up to 2500 V of mains transient voltage, 0.12 millimeters of clearance and 5 millimeters of creepage are needed. The solder mask (0.01 mm thick) on the top and bottom layers does not provide sufficient clearance between adjacent PCBs. Therefore, the layer on the external PCB that is adjacent to the main PCB is empty to provide the correct clearance. The electric strength in kV/mm and the inner composition for a conventional market PCB can be seen in Appendix D.

The winding configuration allows for a single turn per layer which reduces the leakage and the proximity effect in the windings. In addition, there is only one case where a path on the PCB's surface links a primary and secondary winding. This exception is the auxiliary winding, which is located on the the top and bottom most layers of the three PCB configuration. This is the only point where the creepage must be considered. The following table includes the relevant design parameters for the planar transformer.

Table 5.2: The relevant design parameters for the bidirectional DAHB planar transformer where the core is ELP 38/8/25 core with I-core and 3C95 material

Core Parameters		Winding Parameters	
Parameter	**Value**	**Parameter**	**Value**
l_g (air gap)	0 mm	$l_{w(primary)}$	574.8 *mm*
A_{core}	2*194 µm^2	$l_{w(secondary)}$	185.6 *mm*
MPL	43.6 *mm*	$Width_{\,inner(primary)}$	11.1 *mm*
A_L	9600 nH/T^2	$Width_{\,outer(primary)}$	3 *mm*
L_m, L_k	400 µH, 5µH	$Min\ Width_{(secondary)}$	6.9 *mm*
B_{max}	170 mT		

5.3 Simulation

Two PLECS simulations were created for the bidirectional DAHB converter. One to simulate forward conduction of the converter and the other for the reverse conduction case. The simulations were modeled in reference to the schematic shown in figure 5.1 where the component values are defined in table 5.1. Models for the GaN switch and secondary side MOSFETs were downloaded from the GaN Systems and Infinion websites, respectively. In Appendix D, the forward condition simulation can be viewed.

5.4 Losses and Efficiency

Multiple loss mechanisms are considered in the bidirectional DAHB efficiency analysis. The efficiency approximation is based on a methodology presented in [57].

HV Primary Side GaN HEMT Losses

The high voltage side GaN switches are assumed to be operating in ZVS steady-state operation with a medium to high load. The same assumption is taken for the final efficiency approximation, but thermal consideration is given for the case where the primary side high voltage (HV) switches are hard switching. A double pulse simulation test was used to model the turn-on and turn-off switching loss (at different currents and voltages). The results of this simulation (based on the GS66508P PSpice model by GaN Systems) can be seen in [57]. A concrete trend is visible; the turn-on energy is much higher (around 5 times more on average) than the turn-off energy. An approximation is done for the switching loss on the HV side ($P_{sw(HV)}$) due to turn-off loss ($P_{off(HV)}$) using the following equation:

$$P_{sw(HV)} = P_{off(HV)} = f_s * (E_{off(measured)} - E_{oss}) \tag{5.4}$$

where E_{oss} is the energy stored in GaN parasitic capacitance and $E_{off(measured)}$ is based on the results of the double pulse simulation test presented in [57]. The turn-on losses are assumed to be 5 times the turn-off losses in order to see if hard-switching (at lower loads) would cause a high level of heating and thus, need for additional thermal handling capability. The conduction losses and gate driver losses are calculated using equations 4.9 and 4.11, respectively.

LV Secondary Side Si MOSFET Losses

Low voltage (LV) side switching losses in the Si MOSFETs are analyzed with the same methodology used above. A double pulse simulation test was done in order to obtain an approximation for the turn off energy at a given drain current. The switches are assumed to be operating under ZVS conditions in steady state conduction. Equations 4.9, 4.11, and another form of equation 5.4 (used for determining the turn-off losses ($P_{off(LV)}$)) where the drain current I_d is used to calculate the total switch loss of the LV secondary side Si MOSFETs.

$$P_{sw(LV)} = P_{off(LV)} = f_s * E_{off(measured)} * I_d \tag{5.5}$$

Active Snubber Losses

The active snubber has yet to be discussed from a control standpoint. This will be elaborated on in section 5.6. In short, the snubber switch is turned on to release energy stored in the snubber capacitor. When this occurs, the current will resonate from zero, thus resulting in a snubber switch which has soft turn-on. The turn-off switching loss ($P_{sw(snub)}$) (presented in equation 5.6), conduction loss, and gate driver loss are the loss mechanisms considered in loss calculation for the active snubber.

$$P_{sw(snub)} = P_{off(snub)} = (V_{LV} + V_{HV}/n) * Q_{oss} * f_s \tag{5.6}$$

Transformer and Inductor Losses

The losses in the planar transformer windings and core are calculated using the same methodology defined in chapter 3. The losses of the auxiliary inductor, similarly to the planar transformer, are winding loss and core loss. The DC resistance of the inductor is based on its geometry provided by the datasheet.

Results of Efficiency Analysis

The efficiency estimation is based on a 500 W steady state condition where the input voltage is 350 V and the output voltage is 25 V. The individual loss components can be seen in table 5.3. Dead time losses (based on equation 4.10) are negligible in most cases but included to show that the small dead time will not be a factor for the efficiency. Moreover, losses due to the gate driver, powering circuitry (including LDOs), sense resistors, and other components of the system (not included in table 5.3) are estimated to be 3 W.

Table 5.3: The individual loss components for all major sources of loss in the DAHB design. These values are calculated for the 500 W system power where the input and output current are 1.42 A_{RMS} and 20 A_{RMS}, respectively. The losses are multipled by 2 to represent the total loss for both switches

Transformer Losses & Inductor Losses		**HV Switching Losses (Primary side GaN)**		**LV Switching Losses (Secondary side Si)**		**Active Snubber Losses**	
Parameter	**Value**	**Parameter**	**Value**	**Parameter**	**Value**	**Parameter**	**Value**
Core	4.9 W	Conduction	0.42 W	Conduction	3.8 W	Conduction	3.1 W
Conduction (primary)	0.51 W	τ_{dt} (dead time loss)	8 μW	τ_{dt} (dead time loss)	4.4 μW	τ_{dt} (dead time loss)	3.2 μW
Conduction (secondary)	2.96 W	Gate Charge	0.02 W	Gate Charge	0.05 W	Gate Charge	0.01 W
Inductor (core + winding)	1.01 W	Turn-off	0.06 W	Turn-off	0.8 W	Turn-off	0.83 W
Total Loss:	9.38 W	**Total Loss:**	0.51 W	**Total Loss:**	4.65 W	**Total Loss:**	3.94 W

The transformer losses make up the majority of the system losses. LV side Si MOSFET and snubber switching losses also contribute a significant amount to the total losses. $P_{loss(total)}$ can be calculated by summing all of the column loss totals (of table 5.3) and the 3 W of supporting circuitry losses together. The final efficiency calculation based on design parameters was completed using the following equation:

$$\eta_{DAHB} = \frac{500W - P_{loss(total)}}{500W} * 100 \tag{5.7}$$

Equation 5.7 yields an efficiency approximation of **95.6%** at 500 W power and a 200 kHz switching frequency.

5.5 Thermal Considerations

The results from the efficiency approximation show that the most significant components of power loss are the low voltage secondary side switches (due to the high conduction losses) and the transformer. Furthermore, the HV primary side switches, when hard switching, will have higher loss and heating in the switching node. A more accurate load analysis needs to be conducted in order to determine if a heat sink is needed for these 2 primary switches, but it will likely not require a heat sink. The secondary side (low voltage and high current characteristic) will have a heat sink but the primary side may only require the presence of thermal pads because of the GaN transitor's ability to have low switching losses even in hard switching operation. Ultimately, the process for the thermal design can only be completed in the PCB layout phase. Information such as, available space, thermal pad area, and component placement factor into the decision for a secondary side heat sink.

The transformer is the highest loss mechanism in the design. The core loss approximation is a worst case value based on the maximum flux density that the core can allow. The core will also be exposed to air and this will help with heat dissipation. In addition, the secondary side windings have significant heating, where up to 3 W of power dissipation will be required. The presence of a secondary side heat sink should remove any issues surrounding heating in the secondary side windings.

5.6 Additional Modules and Controls

Powering circuitry, measurement circuitry (with a feedback line), a WiFi module (with supporting components), two gate drivers, a digital isolator, an in-rush current limiting circuit, and a start-up circuit are included in the design. These modules are designed in the same manner and based on the verified working sub-modules of the unidirectional half-bridge LLC converter.

The control of the primary HV side GaN HEMTs and secondary LV side Si MOSFETs have already been explained in-depth. SPC, for a dual active half-bridge, requires two sets of two complementary PWM signals that have a phase shift between each pair. The leading and lagging relationship between the two sets of signals determines the forward or reverse operation direction for the bidirectional control. The control of the active snubber has three goals; to switch on the snubber in order to discharge the snubber capacitor, suppress the voltage spike from the leakage inductance by providing a path for the energy in the leakage to flow during dead time, and reduce the turn-off current by injecting reverse current into the main Si MOSFET. All three of these goals can be achieved by using a single complementary pulse, which is long enough to successfully discharge the snubber capacitor every cycle. A complementary pulse means that the snubber switch is turned on when the adjacent main LV side switch is turned off. This can be seen in figure 5.4, as the non-dead-time pulses for S_{4a} and S_{3a}. The anti-parallel diode of the Si MOSFET provides a path for the leakage current to flow when the switch is off. Therefore, the control of the snubber does not require a dead-time pulse to switch on. As a last remark, a single pulse is not a complex addition to the overall control scheme thus, the STM32-G0 series 48 pin microcontroller by ST (rather than the G4 with enhanced resolution and timer peripherals) is used in this application.

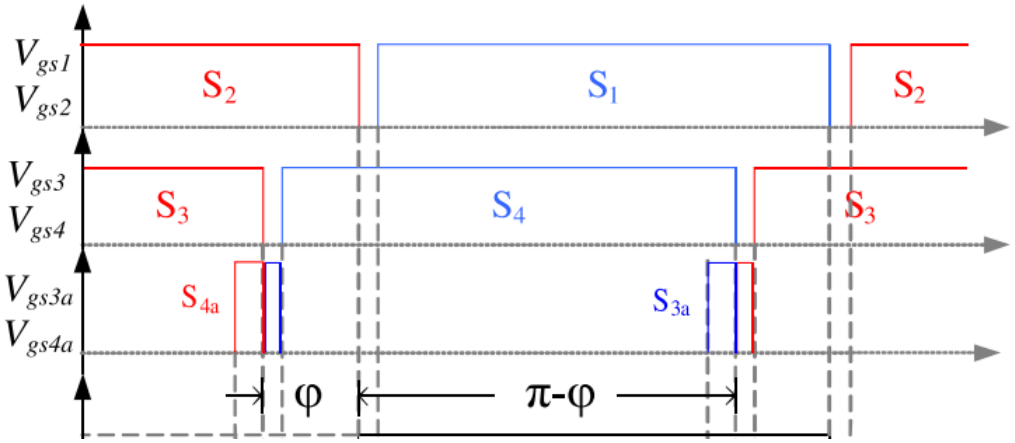


Figure 5.4: Steady-state gate pulse waveforms of the 6 switches (defined in 5.1) of the DAHB in reverse conduction mode [57]

5.7 Schematic

The complete design of the DAHB bidirectional converter, including all sub-circuits, can be seen in figure 5.5. The completed schematic with all components associated to footprints is presented. The next step is to begin the PCB layout for the converter however this was not completed for this thesis.

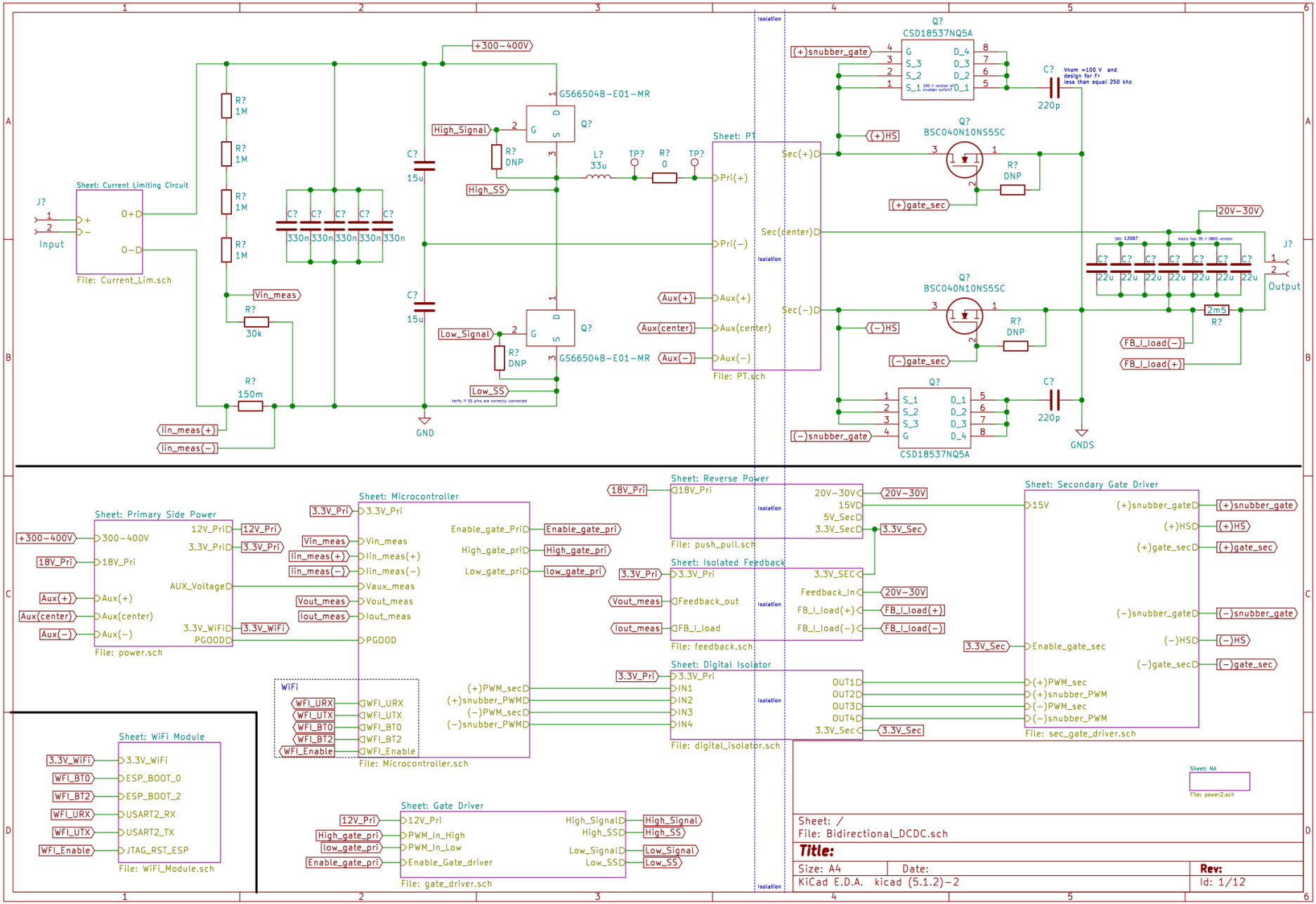


Figure 5.5: KiCAD schematic including sub-circuits for the bidirectional MDAHB converter

Chapter 6

Results and Analysis

This chapter will summarize the testing results for the unidirectional half-bridge LLC converter and the simulation results for the bidirectional DAHB converter. Moreover, it will analyze findings, provide explanations, and give recommendations based on the results.

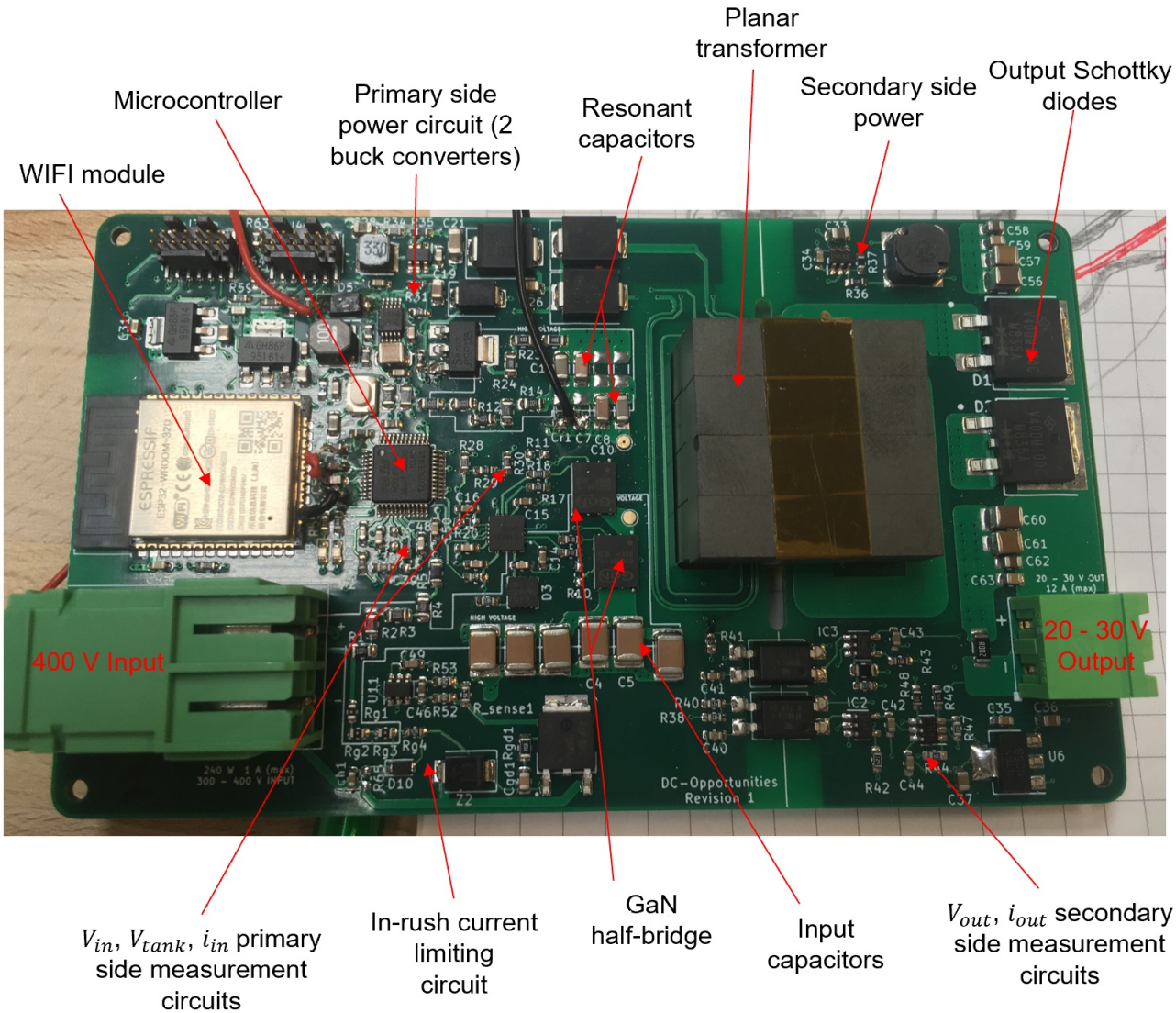


Figure 6.1: Hardware Overview of the Unidirectional LLC converter. Dimensions 120 mm x 70 mm

6.1 Unidirectional Half-bridge LLC Converter

A hardware overview can be seen in figure 6.1. The figure highlights the important circuit components in the final working design. It should be noted that some adjustments and component changes have been made to the final product after testing the device.

6.1.1 Measuring the Leakage Inductance

The values for leakage and magnetizing inductance are integral in order to finalize the design and configure the controls. These values should be verified when the designer makes their own magnetic components. This is often the case for planar magnetics. The following three distinctive configurations were used in the testing process: both diode outputs short-circuited, only one diode output short-circuited to ground, and the no load condition (secondary side component of leakage disappears). Each configuration produces a different resonant tank equivalent circuit. This produces three equations, one for each configuration, and allows for the solving of three unknown variables (leakage inductance of the primary L_{pri}, magnetizing inductance L_m, and leakage inductance of the secondary L_{sec}). The entire process is done assuming that C_r is known (based on designer choice) and that the parasitic capacitance (diode junction capacitance, switch parasitic capacitance, etc...) components are negligible.

To find the resonant frequency, the converter is operated with a 25 V input testing voltage and the resonant capacitor voltage is closely monitored. By carefully adjusting the switching frequency, a resonant frequency becomes visible within the voltage waveform of the resonant capacitor. An oscilloscope measurement of the resonance in the C_r waveform gives the resonant frequency. The last step is using equation 2.2 for f_{R1} to find the total value of the inductive component for each of the three configuration. The resonant frequencies (f_{R1} and f_{R2}) and the gain versus frequency relationship for the controls can be determined after obtaining the value of L_k. The following table shows the final tank configuration and relevant parameters.

Table 6.1: Measured component values (and relevant parameters) of the resonant tank after solving for leakage inductance components

Parameter	Value		Parameter	Value
L_{pri}	22 μH		C_r	8 nF
L_{sec}	6.1 μH		f_{R1}	336 kHz
L_m	62 μH		f_{R2}	187 kHz
L_{ratio}	2.2			

This result is notable because leakage inductance is much higher and L_{ratio} is much smaller than the values calculated in the design phase. There will be limitations in the system due to forced operation at frequencies lower than 1 MHz (see value for f_r) in order to operate around the resonance. A larger value for leakage inductance forces the resonant frequency to drop. It also sets a limit to the value of the resonant capacitor. As the value of C_r increases, the resonant frequency will decrease. Furthermore, a lower switching frequency corresponds to a greater time period for current conduction in each cycle resulting in a larger average value of current on the primary side windings.

6.1.2 Accurate Equivalent Circuit Model of the Tank

The approximations for the equivalent circuit model used during the design phase were found to be no longer valid, due to the small ratio between leakage and magnetizing inductance. The reduced ratio between the inductances does not allow for the series component of leakage to slide out in front of the magnetizing inductance. Figure 6.2 shows the actual equivalent circuit model which represents the tank behavior seen in the final version of the converter.

Testing yielded an additional discovery; effects on the output voltage gain due to the presence of the winding resistance (both an AC and DC component) from the primary and secondary windings of the transformer. The components of resistance are depicted as R_{pri} and R_{sec} shown in figure 6.2. These resistance components are often overlooked in the typical gain curves provided throughout literature. In

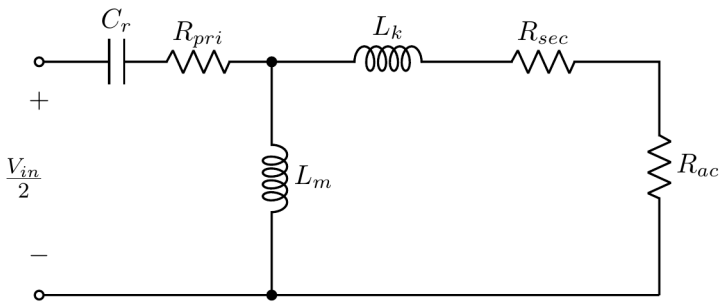
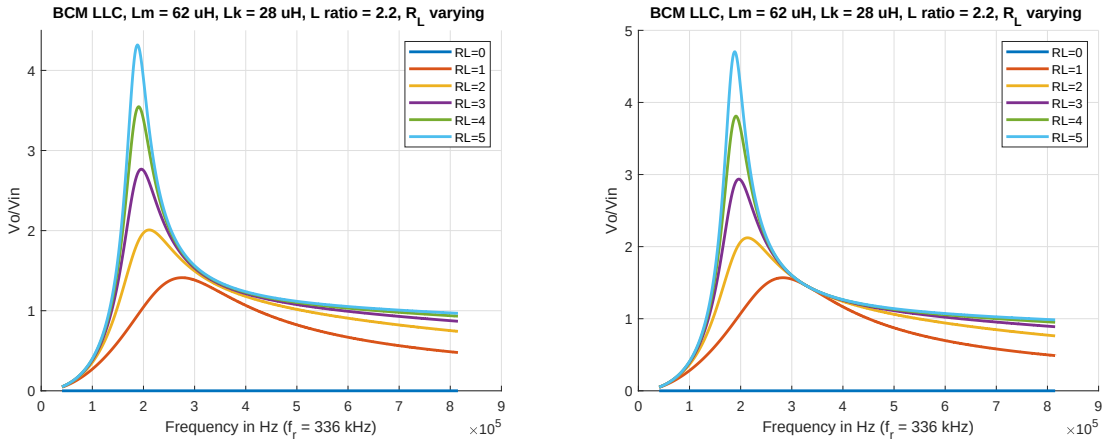


Figure 6.2: Actual equivalent circuit model for the unidirectional LLC converter where L_k is the equivalent leakage of the primary and secondary added in series

real applications, the effect of this resistance can reduce the expected output gain at a given frequency. Furthermore, this effect will be more noticeable as R_{ac}, representative of the proximity effect and skin effect, changes with frequency.

The final gain versus frequency curve based on the transfer function calculated from the equivalent circuit model is presented in figure 6.2. The effect of the series resistance is included in (a) but not in (b) to show the significance of the drop in voltage gain for a given frequency. The frequency versus maximum primary current relationship is shown in figure 6.4 for perspective on the current value in the tank (on the primary side). This figure shows the relationship between the value of L_m and the magnitude of the primary tank current and how the current increases as the f_{R2} is approached. These graphical results specifically characterize the power transfer behavior of the final version of the converter.



(a) (b)

Figure 6.3: (a) Actual gain versus frequency curve for the unidirectional LLC converter (b) Ideal gain versus frequency curve (not considering series resistance components) for the unidirectional LLC converter

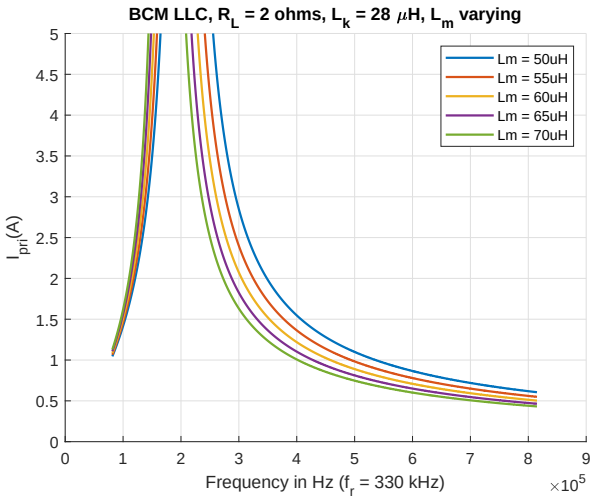


Figure 6.4: This graph shows the primary side current vs frequency for increasing values of L_m. The load resistance is fixed to 2 Ω, which is the value of the load resistance in full load operation. The input and output voltage (taken at their nominal values based on V_{in} = 350 V) were used in the calculation

6.1.3 Current Collapse in GaN HEMT

The GaN transistor selected for the LLC converter was the GS-065-004-1-L from GaN Systems. This is the lowest tier version of the 650 V enhancement-HEMT series with the capability for conducting up to 4 A of drain current. In the early testing of the converter there was often catastrophic damage to the GaN switches at high voltages. Figure 6.5 is an oscilloscope capture of a moment leading to catastrophic breakdown where the V_{ds} across the bottom switch begins to fall off, in this case, around 25 V from 300 to 275 V.

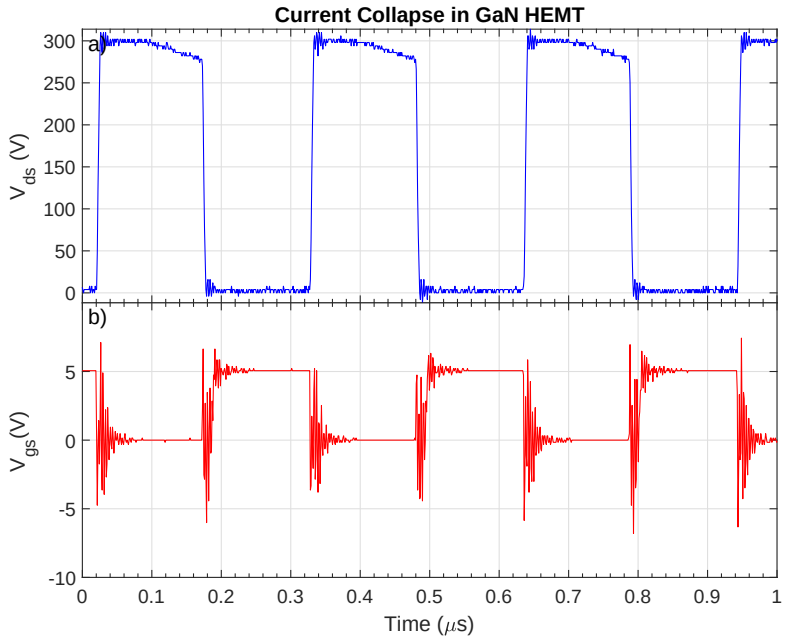


Figure 6.5: Waveforms taken from the results which show the effect of current collapse in a GaN HEMT before catastrophic breakdown occurs

Figure 6.5 shows how the value of $R_{ds(on)}$ is dynamically changing within each cycle. The capacitor of the bottom switch starts discharging prematurely because not enough current can flow through the

top switch towards the end of the on time. Electrons accelerating under high voltage stress are trapped in the interface between the dielectric and semiconductor layers and in other impurities in the device structure, building up over time. This effect decreases the electron mobility and creates a larger resistance for the current flow. The effect worsens as the voltage increases, and eventually V_{ds} drops all the way to 0 prematurely in the cycle resulting in catastrophic breakdown. In order to solve this issue, so that operation at 350-400 V is possible, an 8 A version of the switch with a higher current rating and lower $R_{ds(on)}$ is used. This solves the issue and the effect of increased temperature and premature voltage drop off disappears. It should be noted that current collapse is present in all GaN e-HEMTs and to avoid adverse effects at high voltages the designer must compensate for this effect and choose a transistor with current handling that is significantly greater than the maximum current through the switch calculated in the design phase. A higher system voltage signifies that the gap between the currents should be greater.

6.1.4 Experimental Waveforms

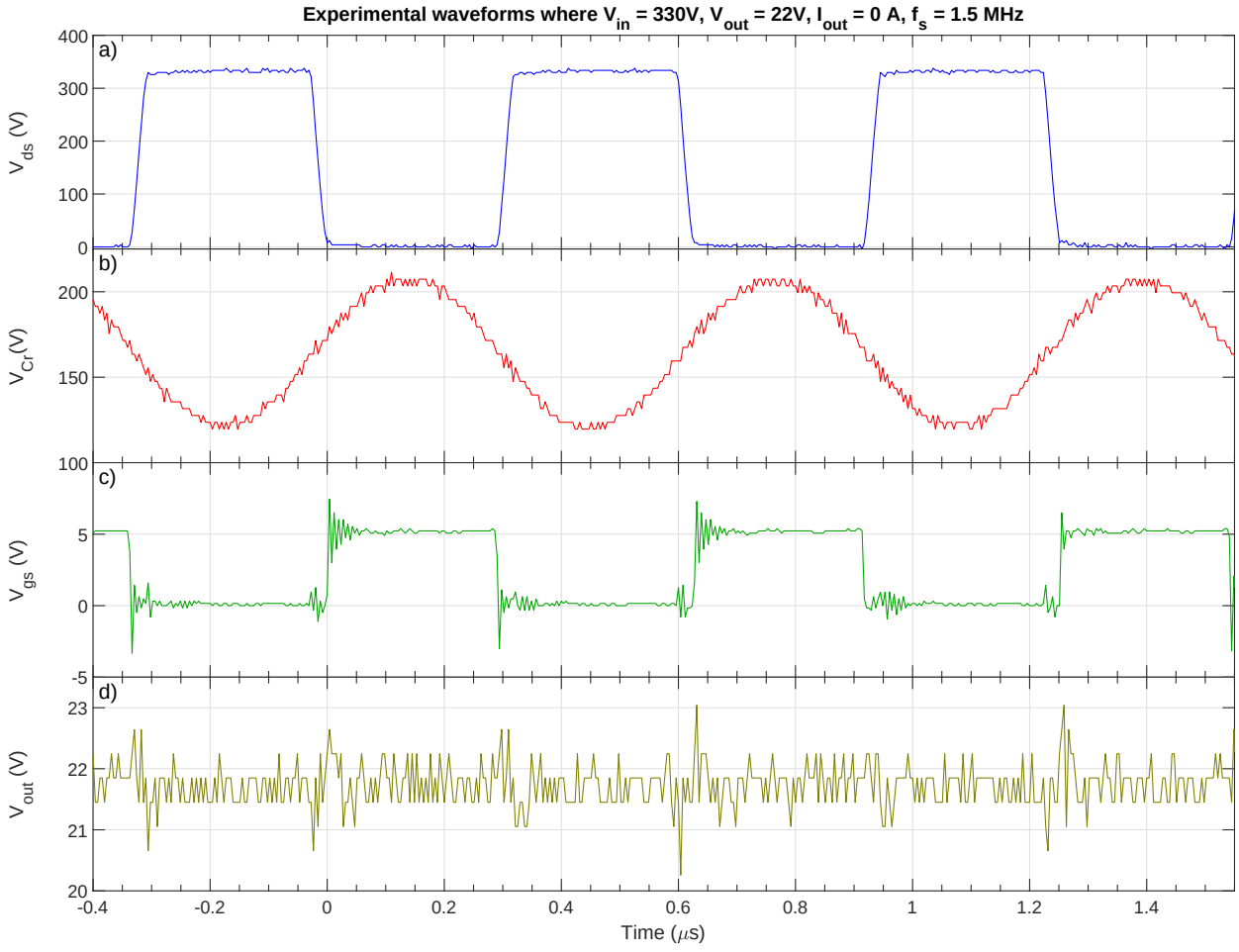


Figure 6.6: Experimental waveforms at no load where V_{ds} and V_{gs} are the voltages of the bottom side switch in the half-bridge and V_{cr} is the voltage across the resonant capacitors. The output voltage V_{out} is approximately 22 V at V_{in} equal to 330 V

The waveforms for the half-bridge LLC operating at no load are shown in figure 6.6. The results showcase the high (1.5 MHz) switching frequency enabled by GaN HEMTs, and present clear waveforms typically associated with LLC converters. High switching frequencies are preferred for small and no

load demands, in order to limit the circulating current in the tank. Moreover, ZVS turn-on for the primary switches is verified because the V_{gs} waveform goes high after the V_{ds} voltage of the bottom side switch falls towards 0. This is also confirmation that the LLC tank is properly designed. No-load operation is not an intrinsic property of the LLC resonant converter (like ZCS for the secondary rectifiers) [19]. It can only be realized with the correct design of the tank circuit (based on equation 2.6) and is an important test to verify the design and planar transformer.

In figure 6.7, the results at full load (150 W) can be seen. In waveform (d), the peak current value in the tank is higher than 1 A. This is a higher peak current than was expected in the design phase. The voltage waveforms (a) and (c), V_{ds} and V_{gs} respectively, of the bottom switch are demonstrating soft switching. The resonant capacitor voltage waveform (b) is phase shifted due to a high load demand. The sinusoidal behavior of V_{cr} is distorted because, as the load increases, the voltage in the capacitor at the beginning of the conduction cycle becomes more and more negative (due to increasing negative charge). The resonant capacitor waveform in steady-state operation is half of V_{in} which is the expected voltage across a half-bridge LLC resonant tank.

Additionally, the converter is operating at 375 kHz (slightly above the resonant point depicted in figure 6.3a) and the output voltage gain is around the expected value of 18 V. The output voltage will be smaller than the ideal case due to the voltage drop caused by resistance of the winding and the voltage drop due to the presence of leakage inductance on each center-tapped winding.

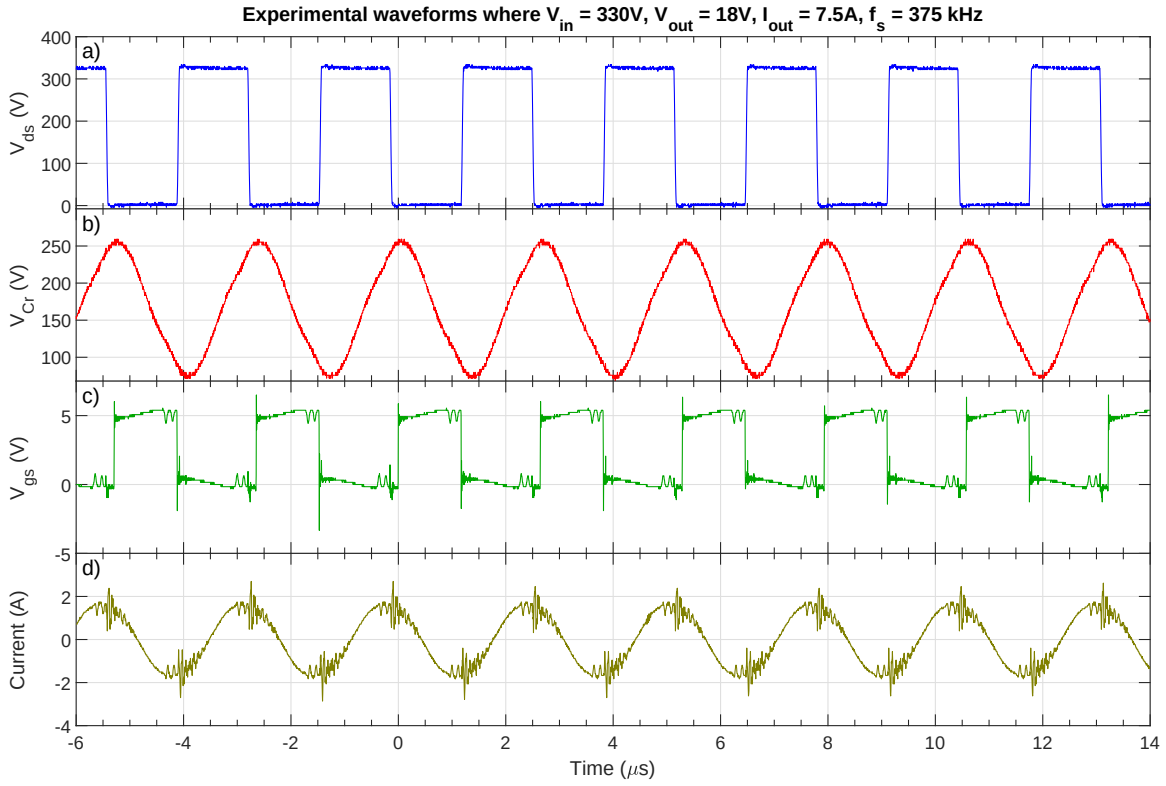


Figure 6.7: Experimental waveforms at full load (7.5 A) where V_{ds} and V_{gs} are the voltages of the bottom side switch in the half bridge and V_{cr} is the voltage across the resonant capacitors

The thermal behavior of the LLC converter at a 150 W load can be seen in figure 6.8. The converter was designed for 240 W, however due to high temperatures in primary side windings, the maximum load current that the converter can safely handle in steady-state operation is 7.5 A. The temperature of the primary side windings can been seen climbing up to 90-100 degrees Celsius. The rectifier diodes on the output also heat up (as expected) to around 80 degrees Celsius in steady state operation. The switches, due to lower frequency operation and ZVS, stay around 40 degrees Celsius. The gate driver temperature (seen as the small temperature peak on the left side of figure 6.8) settles at around 55

degrees Celsius.

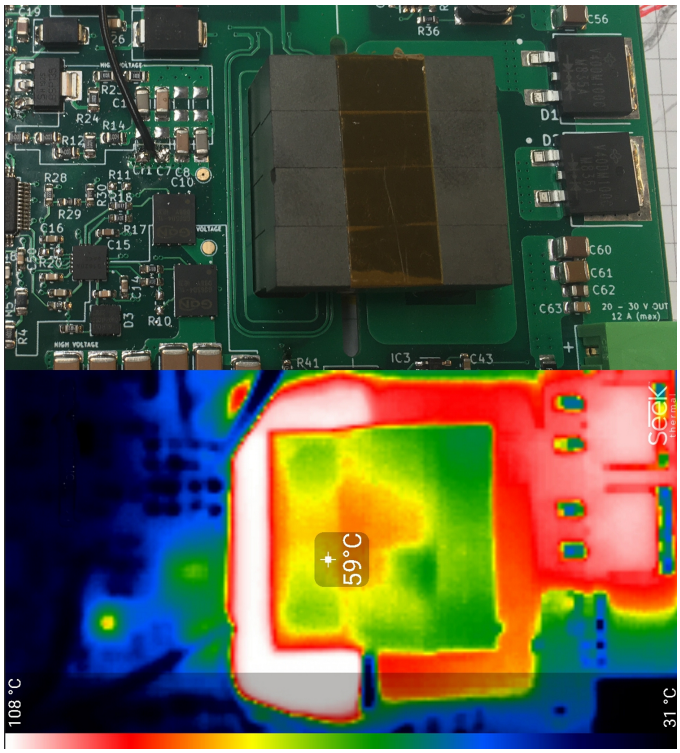


Figure 6.8: Thermal Behavior at a 150 W load $I_{out} = 7.5A$

6.1.5 Testing Setup

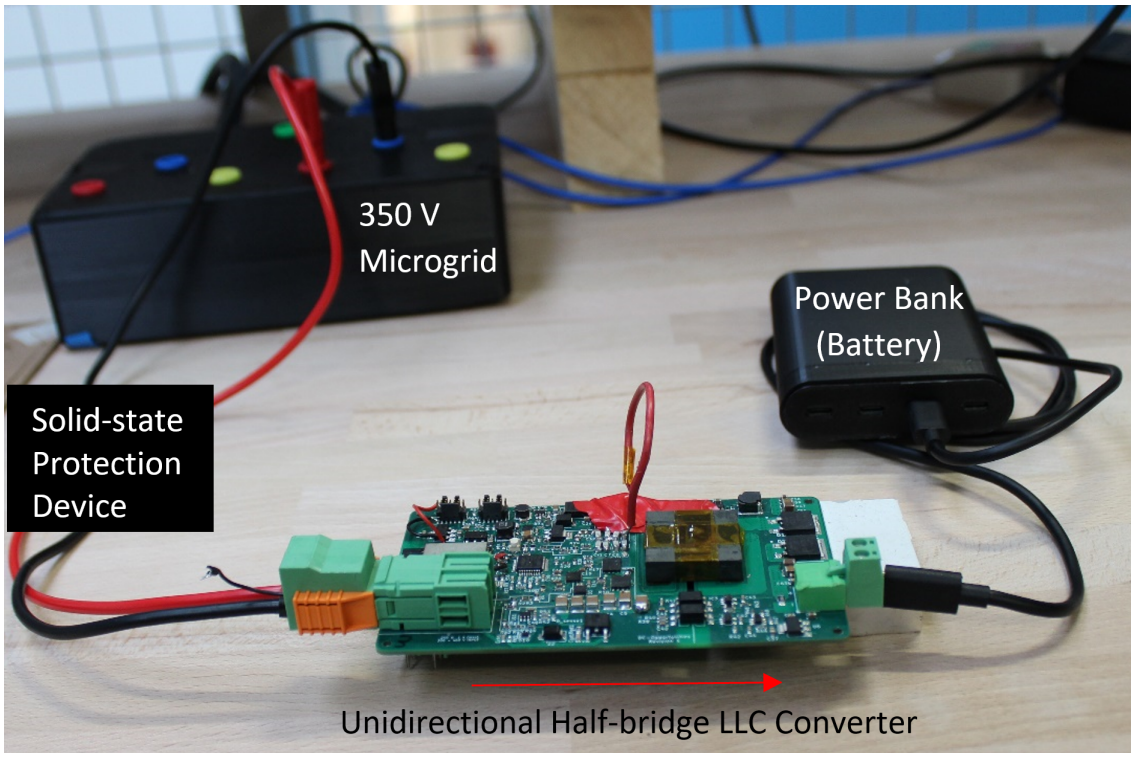


Figure 6.9: Picture of the verified working test set up for the half bridge LLC converter: 350V input and 24 V output to a SHS

Figure 6.9 is an actual DC microgrid to solar home system setup that would be seen in a rural electrification application. The figure depicts how an input from the DC microgrid (350 V) connects to a solid state protection device before connecting to the unidirectional LLC converter. The 350 V line runs through the protection device and the output of the circuit breaker will provide power as long as no faults are detected. The converter, when provided with 350 V, starts up on its own (without an external power supply for the supplementary circuitry) and the converter successfully provides 22 V to a small output SHS load.

6.1.6 Discussion of Limitations

At a 150 W load, the measured efficiency of the converter (based on input and output IV measurements) is 90.2%. This is three percent less than the efficiency calculated for a 200 W load case in the design phase. In the experimental setup for the 150 W load test, the converter conducts a load current of 7.5 A which is only 500 mA less than the average current of the system (8 A) for a 200 W load at a nominal 25 V output voltage. The lower efficiency is a result of the relationship between the primary side current and both the 335 kHz resonant frequency and output voltage gain requirement.

The 25 μH of leakage inductance forces the resonance in the tank to have a frequency much lower than 1 MHz. In order to compensate for this, the converter operation needs to be at a lower frequency (close to the 335 KHz resonance) which results in a higher tank current. By referring to figure 6.4, the primary side current increases as the frequency decreases (in the inductive region) thus putting more stress on the primary side windings. When considering a small or no load condition, the negative effects resulting from higher reactive power and circulating current in the tank will be worse at lower frequencies.

The magnitude of the output voltage is dependent on the input voltage and frequency of operation. In addition, achieving a certain output voltage gain requires that the frequency modulation can, in some cases, go lower than the resonant frequency (as can be seen in figure 6.3). In other words, in order to have an output voltage in the 25-30 V range, the frequency of operation would need to decrease below the resonance, thus further increasing the heating in the primary side windings. The impedance parameters of the planar transformer, winding resistances and leakage inductance, further decrease the expected output voltage and additional compensation from voltage gain is required .

An effective way to alleviate the stress on the primary windings is to reduce the air gap in the transformer such that it limits the rise in current over time at lower frequencies. Furthermore, depending on the desired output voltage of the system, the frequency and value of load will change. If a 25-30 V output voltage is required the converter can only operate at a limited load (less than 150 W). If a 20 V output is required, the load can increase up to 150 W. These are the operating conditions that must be upheld for the unidirectional half-bridge LLC converter to properly and safely function. The main limitations of this converter are due to the design of the planar transformer. All of the issues stemmed from the significantly large leakage inductance (25 μH) that appeared in the actual transformer which significantly deviated from the predicted value in the design phase.

6.1.7 Recommendations

A re-designed planar transformer with a smaller leakage component will allow for operation at higher frequencies, eliminate issues regarding high currents in the primary side, and support a widespread operation frequency range for controlling the output voltage. Secondly, if GaN switches are used, the design and GaN HEMT selection should account for the effect of current collapse. A GaN switch with a larger drain current rating (8 A or greater) should be used for this converter. Lastly, in order to drastically improve the efficiency, active synchronous rectification should be implemented into the secondary side by replacing the Schottky diodes with switches.

6.2 Bidirectional DAHB Converter

The results for the DAHB converter consist of the simulation results and the discoveries made during the design of the planar transformer.

6.2.1 Simulation Waveforms

The forward mode simulation (which can be seen in figure D.5 of Appendix D) functions as expected based on the design parameters. Figure 6.10 shows the waveforms for V_{gs} and V_{ds} of the primary side HV bottom switch. Moreover, the inductor current i_L and output voltage are shown. Operation at a power of close to 490 W is shown in the yellow waveform and the ripple is large because the value of output capacitance was lowered to speed up the simulation.

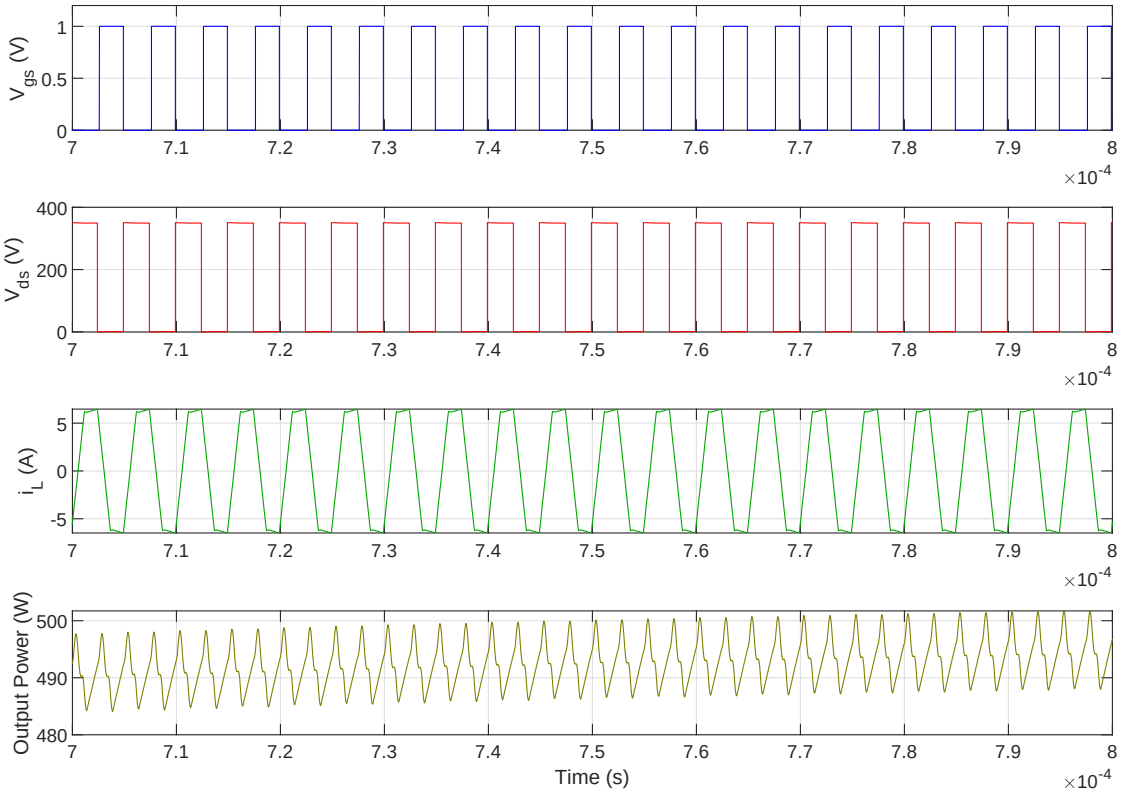


Figure 6.10: Simulation results for forward operation at steady-state where V_{in} = 350 V, V_{out} = 27 V, I_{out} = 18 A, f_s = 200 kHz, and $\Phi = \pi/2$

The simulation uncovered a resonance which appeared between the leakage inductance of the center-tapped winding and the snubber capacitor. The value of the snubber capacitor was raised in order to reduce the effect of this resonance on the voltage and current of the secondary side transformer output. A larger snubber capacitance can handle more energy which gives the approximation for the leakage on the secondary side some ”room for forgiveness” such that if the leakage is higher than expected the capacitor will be large enough to store the extra energy. An additional test, regarding the dead time turn-on pulse for the snubber circuit, was conducted using the simulation. It was concluded that the pulse is not needed because the energy stored in the leakage can flow through the anti-parallel diode of the snubber switch into the capacitor.

The simulation for the reverse operation case (presented in figure 6.11) also functions as expected. For reverse operation mode, the waveforms for V_{gs} and V_{ds} refer to the secondary side LV bottom Si MOSFET voltages. The resonance between the leakage and snubber capacitance can been seen in the V_{ds} waveform. This can result in an applied voltage of up to $2V_{out}$ when the switch turns-off. The inductor current remains the same in both situations where the peak value is at 5.8 A. Lastly, the power is slightly lower in the reverse operation case, around 475 V on average. The capacitance of the DC blocking capacitors was reduced in order to speed up the simulation resulting in a ripple. The output power is slightly lower than the forward operation case because the input to output voltage relationship is slightly different (e.g. V_{out} = 27 vs V_{in} = 25 V in the reverse scenario). The small variations in the output power due to the IV relationship can be seen in figure 5.2.

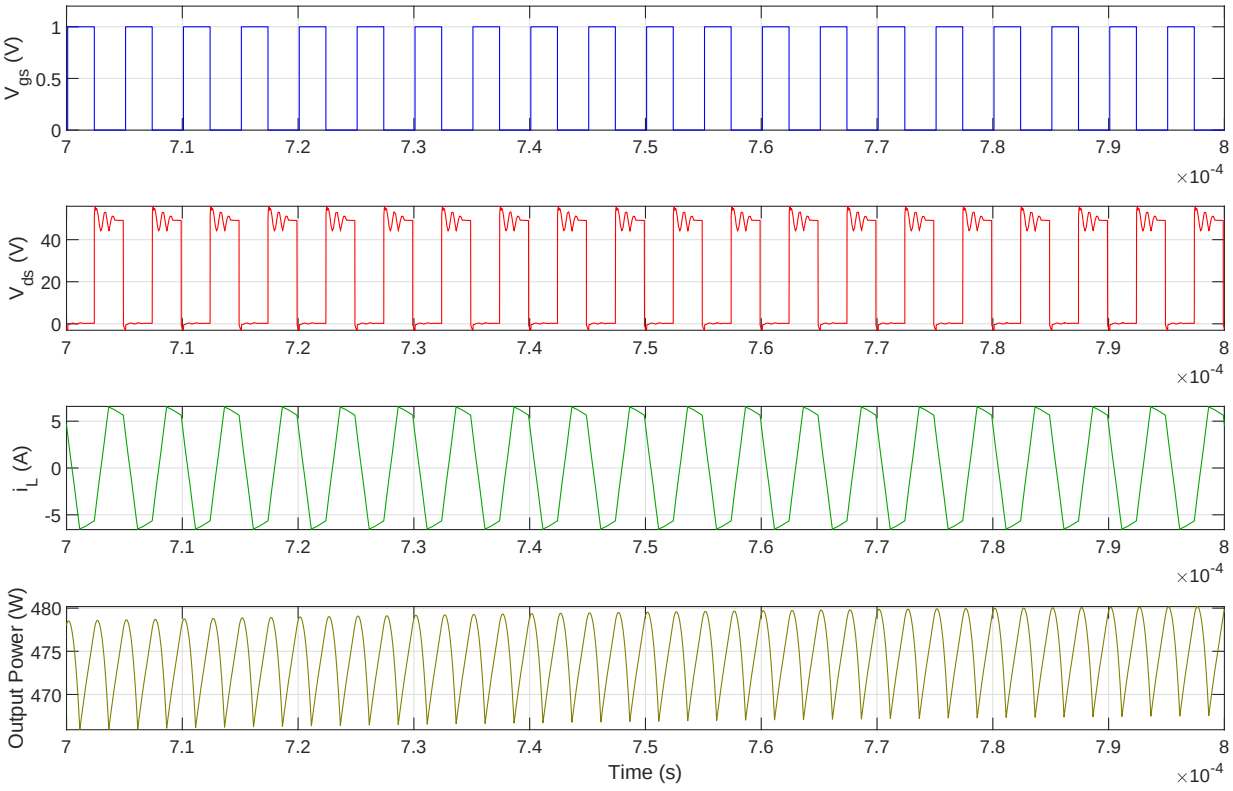


Figure 6.11: Simulation results for reverse operation at steady-state where V_{in} = 25 V, V_{out} = 345 V, I_{out} = 1.4 A, f_s = 200 kHz, and $\Phi = \pi/2$

6.2.2 Planar Transformer Design

A new design for a planar transformer was proposed; one that considers the SELV standards for rural electrification as well as a small value for leakage inductance. It is proposed that a planar E-core with interleaved windings (which have sufficient clearance between primary and secondary) will yield a smaller leakage and less proximity effect losses than a U-core with a conventional winding structure. However, the reinforced insulation planar E-core PT design presented in figure 5.3 can only be used for applications where the HV side is 400 V or smaller. If a bipolar DC micro-grid is used, the transformer could see up to 800 V. This would require a different design with a new winding configuration and possibly a larger core. For higher voltage clearance applications, only some layers could be used because of the limited 0.18 mm width of pre-preg layer in between inner and outer layers. In conclusion, the PT shown in figure 5.3 presents a SELV design (with minimize value of leakage compared to other configurations) that can be effectively used in rural electrification applications with a DC micro-gird

operating up to 400 V.

6.2.3 Recommendations

This is a complete design up to the PCB layout phase. However, an accurate approximation for the ZVS range in both the forward and reverse operation cases is needed. Additionally, if operation in light load is required for a long period, the stress on the primary side and secondary switches should be re-evaluated for the duration of this period. Single phase shift control, although the easiest DAB control algorithm to implement, does have a smaller ZVS range and high circulating currents. As it is currently, it is assumed that the converter will primarily operate at medium to heavy loads at 300-400 V input. Additional thermal consideration should be given to the light load operation scenario with hard switching for both the primary and secondary sides. If soft-switching is necessary at light load conditions a more advanced modulation scheme should be investigated.

Chapter 7

Conclusion

The final chapter, presents answers to the research questions and the conclusions of the work. Additional recommendations for future work are also included.

7.1 Answering Research Questions

How can a unidirectional DC/DC converter be designed for the interconnection of a 350V DC microgrid to individual households for rural electrification that includes high switching frequency GaN technology?

A 240 W unidirectional half-bridge LLC converter with a push-pull center-tapped secondary was successfully designed, manufactured, and tested. The GaN HEMT was observed under different operation conditions. The presence of GaN transistors allowed for an effective half-bridge LLC design that has small passive components (due to HF operation) and low switching losses (due to low parasitics, low $R_{ds(on)}$, and no reverse recovery). The resonant inductance was magnetically integrated into the design by using the leakage of the transformer. The half-bridge is a useful switch configuration for the converter in order to halve the output voltage, thereby reducing the needed turns ratio of the transformer to achieve a low output voltage range (20-30 V). Additionally, the LLC's small size, wide ZVS range of operation, inherent ZCS on the secondary side, ability to conduct no-load operation, and flexible frequency modulation for voltage adjustment designate it as an efficient and cost effective topology for the interface between a DC microgrid and solar home system.

How can a bidirectional DC/DC converter be designed to achieve the same purpose but also with a higher power rating?

A 500 W bidirectional dual active half-bridge converter with a push-pull center-tapped secondary side (including additional active clamping circuitry) was successfully designed and simulated. The GaN HEMT is selected as the primary side switch in order to reduce losses in hard switching conditions. Moreover, the low parasitics of the GaN transistor increase the ZVS range which is somewhat limited due to the single phase shift control modulation (which has ZVS operation at medium to high loads but hard switching at lower loads). An auxiliary series inductance was externally implemented into the design to function as the energy transfer mechanism of the DAHB. The low voltage, high current, characteristic of the secondary side meshes well with the push-pull center-tapped secondary. This configuration reduces the stress on the secondary side switches and there are also active snubber circuits to protect the main secondary Si MOSFET switches from voltage spikes caused by the leakage inductance of the center-tapped winding. The DAHB was selected instead of the half-bridge LLC due to the complications that arise when controlling a bidirectional LLC and its dependence on the leakage of the transformer. The DAHB has larger passive components and requires an external inductor making it a bit more costly, however, unlike the LLC, the control is not as sensitive to the planar transformer leakage and other parasitics. The transition into the DAHB yields a converter which has high efficiency, flexible/easy-to-implement

single phase shift modulation, ZVS on primary and secondary sides, and low component count. The DAHB is as an efficient topology for the bidirectional 500 W interface between a DC microgrid and solar home system.

How to design a PCB based planar transformer for these two converters and why is a planar transformer preferred for these applications?

An in-depth process for designing a planar transformer (PT), based on both literature review and past design experience, is a result of this work. Two planar transformers, which meet the safe extra-low voltage (SELV) requirements for rural electrification, were designed for the unidirectional and bidirectional converters, respectively. The unidirectional version PT consists of a U-core, a conventional winding configuration with an auxiliary winding, and an adequately isolated primary and secondary. The bidirectional version PT is composed of a planar E-core, an interleaved (single turn per layer) winding configuration with an auxiliary, and uses the FR4 material between layers to provide sufficient isolation between the primary and secondary windings. The value of leakage, voltage insulation limits, and performance for both SELV compliant PTs were investigated.

Planar transformers are preferred for this rural electrification (200-900 W) application because they can achieve low leakage values, which is a necessity in high frequency applications. Additionally, these PTs have flexibility for design changes, low cost (only core needed), improved heat dissipation capabilities, a low profile and less proximity effect losses due to less turns per layer (crucial for HF applications).

7.2 Conclusion

The main conclusions of this work aim to bridge the gap for the design and implementation of efficient **DC microgrid variable power output converters** for use in rural electrification applications in the low-medium power (200-900 W) regime. It is concluded that high frequency operated, half-bridge isolated topologies with GaN HEMTs and planar transformers are an excellent composition of technology for these applications. The GaN HEMT is clearly the best switch in the low voltage high frequency range, providing less losses, smaller passive components, and a smaller device size. The planar transformer, allows for flexible designs with predictable integrated leakage inductance, improved heat dissipation, and can be a less expensive alternative to conventional transformers available for purchase.

Converters

The two converters designed in this thesis are fitted for a unique application niche; SELV compliant 200-900 W isolated converters for rural electrification. This is a relatively unexplored area for power electronic converters. Moreover, the unconventional output voltage range (20-30 V) is tailored to always provide sufficient power for USB-C connections (20 V) while also providing up to 30 V for battery charging requirements unique to the design.

The half-bridge LLC with a push-pull (diode rectification) secondary is an effective topology choice for a unidirectional PEI between a DC microgrid and solar home system. The half-bridge LLC with GaN HEMT successfully operates at a high switching frequency thus yielding smaller values (less size and cost) for the passive components. The unidirectional converter presented in chapter 4 works at no load and up to 150 W simply by providing 300-400 V to the input of the converter. In addition, the converter has been successfully tested in a verified DC microgrid real-life application scenario where the input to the converter comes from a solid state protection device and it provides output to a SHS load. The bidirectional DAHB converter with a center-tapped secondary and active snubbers is a favorable topology choice for a bidirectional version of the PEI between a DC microgrid and SHS. GaN transistors are used to raise the efficiency and to allow for hard switching operation. The converter presented in chapter 5 has been successfully simulated in both forward and reverse conduction modes. Furthermore, a worst-case calculation was completed for an approximated efficiency of 95%.

Planar Transformers

Two unique planar transformers were designed; a PT with a U-core and conventional windings for the unidirectional (10 A max) converter and a PT with a planar E-core with interleaved windings for the bidirectional (20 A max) version. The SELV standards for rural electrification, specifically the double isolation requirement between primary and secondary traces, limit the possible configurations typically used in planar transformers. After extensive literature review and testing of the U-core version of the PT, it was concluded that the U-core has higher leakage and primary side losses, due to the proximity effect, in comparison to the planar E-core with interleaving (reduces leakage) and only a single turn per layer (reducing proximity effect). The preferred planar transformer design for a 400 V maximum DC microgrid with up to 2500 V of transient blocking is the planar E-core with interleaved windings. However, if the voltage were to increase, for example in a bipolar DC microgrid which can reach up to 800 V, the clearance between layers in an industry-standard multi-layer PCB would not be sufficient to meet SELV standards. If the maximum voltage level increases, the U-core would be the preferred PT for the application and the designer needs to give extra considerations for a higher leakage inductance and proximity effect loss (especially in HF applications).

GaN Switching

GaN transistors are the favored switch for low voltage and high frequency applications which corresponds to the operation characteristics of the rural electrification application in this thesis. The inherent characteristics, such as zero reverse recovery, low $R_{ds(on)}$, and low parasitic capacitance allow for high frequency operation with low switching losses. In all GaN HEMT applications, careful consideration must be given to the parasitics introduced in the layout of the gate driver and switching node. The GaN switch is sensitive to parasitics (especially source stray inductance) and this sensitivity increases as the frequency of operation increases. In this thesis, the effect of current collapse, which results in a dynamic $R_{ds(on)}$ that increases as the voltage increases, limits the current handling capability of the transistor. The conclusions made during the testing of the GaN transistors used in the unidirectional converter convey that the maximum rated drain current of a GaN HEMT will be lower at higher voltages. Therefore, extra compensation for drain current must be given when implementing GaN HEMTs to a design. Moreover, the quality (often proportional to price) and generation of the GaN HEMT also affects the degree of the current collapse. Newer models with reduced parasitics and created with better crystal epitaxy technique will see reduced effects from current collapse. In general, the GaN switch should allow for roughly double the maximum current expected in the design and the higher the voltage the more prominent the effects of current collapse will be. Another solution to current collapse is to configure GaN transistors in parallel so that the current is mitigated equally among the switches. This will not reduce the effect of current coallpse but it will reduce the current stress on each switch, especially as the dynamic $R_{ds(on)}$ increases.

7.3 Recommendations

The following recommendations are provide for future work:

1. Active rectification should be included in the unidirectional half-bridge LLC converter to significantly raise the overall efficiency and reduce heating on the secondary side. Moreover, a planar transformer with a smaller leakage is needed to allow the converter to operate at high frequency and full (240 W) power.

2. A single phase shift modulation scheme has a limited ZVS range in DAHB which invites the use of GaN switching to reduce the effects of hard switching. If a different modulation method is used, with multiple degrees-of-freedom, the ZVS range many extend for most of the operation scenario. In this case, the presence of GaN would not be worth the cost because a Si MOSFET would be just as effective at 200 kHz in a soft switching condition. A more in-depth investigation should be done on the ideal modulation scheme (complexity vs. efficiency), the effect that the selected scheme will have on ZVS operation, and the choice for using GaN HEMTs or conventional Si.

3. Throughout the work, the implementation of GaN switching and investigation of the most effective planar transformer design were prioritized over the total cost of the converter. Moreover, some of the supporting circuitry (micro-controller, buck converters, LDOs, etc..) may be more costly than is required for a working design. In rural electrification, and when placing a product on the market, cost becomes a priority in the design. More consideration should be given to the cost of the final products and careful evaluation should be done on the effectiveness (efficiency vs. cost) of GaN transistors in both designs as they are one of the more costly components, especially in comparison to conventional silicon switches.

4. A rural electrification case study could be organized in order to verify the optimal power (300-900 W) that is needed for these converters. If a household climbs the electrification ladder up to the point where connection to a DC microgrid becomes feasible, what loads do these households typically use and when is a unidirectional preferred over the bidirectional? More information regarding the application would help the design and research to progress towards the optimal solutions.

Appendix A

Soft Switching

A.1 ZVS in LLC

ZVS is beneficial for GaN switching because there is a reduced energy needed to drive the half-bridge because of the absence of Miller effect at turn-on. Furthermore there is a reduction in, needed gate charge, noise, and EMI, thus minimizes filtering requirements. In order to achieve ZVS in the switches of a half-bridge LLC converter in all operation scenarios, two conditions must be met:

1. In a high load scenario, the tank current needs to have the same sign as the impressed voltage at the switching moment. Secondly, the current must be high enough so that the C_r capacitor energy transition at the half-bridge node is finished. Additionally, the current direction cannot reverse before the end of the dead-time (important to choose an appropriate dead-time).
2. In a no-load condition, the tank current at the instance of switching (same sign as the impressed voltage) needs to be high enough to complete the half-bridge node energy transition within the dead-time period.

In conclusion, a minimum current will always be needed in order to achieve ZVS. The minimum current in the worst-case load scenario can be fixed for the primary side but it will be at a cost to the efficiency. When considering lighter or no load conditions, current needs to circulate in the tank to active ZVS. This means that reactive energy is required in this scenario even if no current or active energy is being delivered to the output. Furthermore, when considering a larger load, the value of the current determines the turn-off and conduction losses of the half-bridge switches. This relationship usually sets the power limit for the converter and which switch the designer will implement. More in-depth information on ZVS in the half-bridge LLC can be found in [19].

ZCS in secondary switches

An inherent attribute or property of an LLC resonant converter is zero current switching (ZCS) in the secondary side rectifiers. ZCS occurs at both turn-on and turn-off of the switch (if active rectification is done). During a turn-on moment, the initial current always starts at zero and ramps up slowly over time (presence of inductor di/dt). This results in a negligible forward recovery loss. Lastly, during a turn-off moment, the rectifiers become instantly reverse biased (because the forward current is zero) and the reverse recovery process never occurs.

A.2 ZVS in DAB

Figures A.1 and A.2 show the effects of magnetizing inductance and parasitic capacitance, respectively, on the ZVS range in a DAB converter. The variable K in figure A.1 is directly proportional to magnetizing inductance L_m.

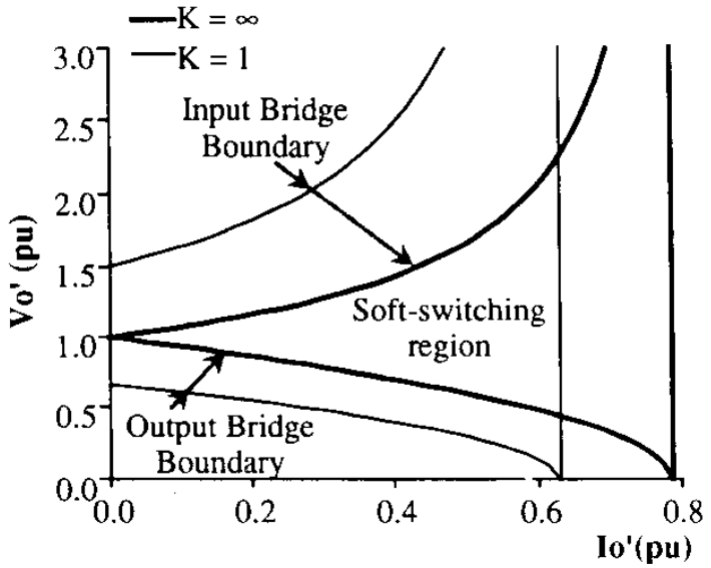


Figure A.1: Effect of magnetizing inductance on the ZVS range in a DAB converter [27]

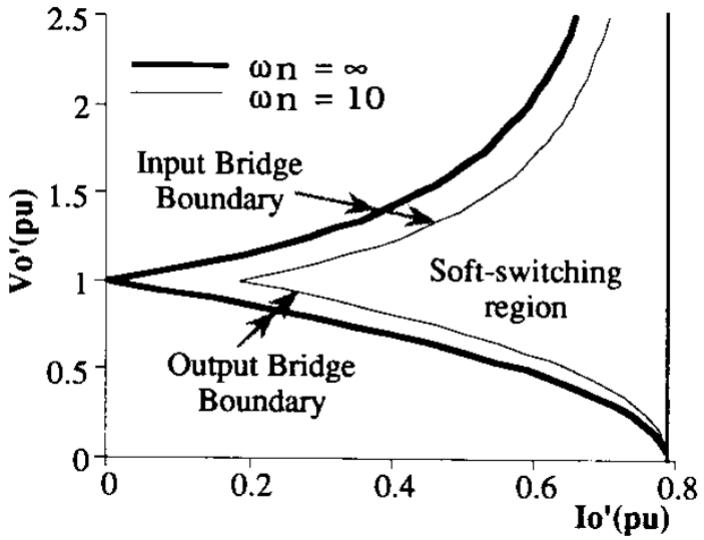


Figure A.2: Effect of parasitic capacitance on the ZVS range in a DAB converter [27]

Figure A.3 is an additional DAB power transfer characteristic graph (similar to figure 2.8) which also includes the distinctive IV relationships at different load resistances.

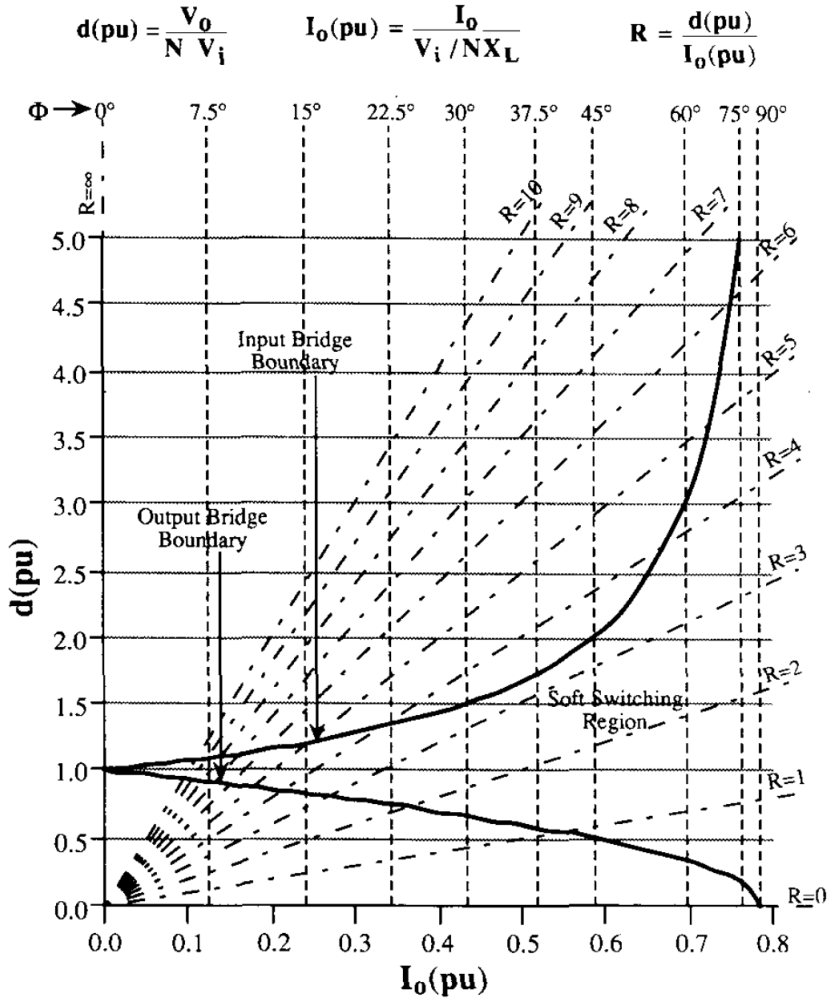


Figure A.3: Effect of parasitic capacitance on the ZVS range in a DAB converter [27]

Appendix B

Supplementary Information for GaN Switching

B.1 GaN Normally ”off” Transitors

Figure B.1 shows the cross-section of an enhancement mode GaN HEMT. The enhancement mode fabrication process begins using silicon wafers. Aluminum Nitride (AlN) is grown on the silicon to provide a thin layer such that a gallium nitride hetero-structure can be grown on top of this layer. Lastly an AlGaN thin layer is grown which forms a permeable interface between the AlGaN and GaN layers. This interface generates the 2DEG which is filled with electrons with a high mobility. To turn-on the GaN HEMT, a positive voltage is applied to the gate just as is done in an enhancement mode N-MOSFET.[58]

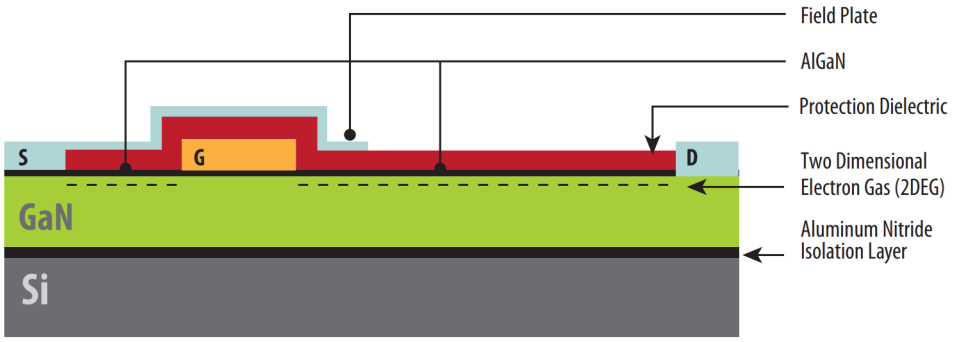


Figure B.1: Structure of an enhancement-mode GaN HEMT [58]

B.2 Paralleling GaN Transistors

When high current handling is required by a GaN HEMT paralleling GaN Transistors can be done in order to reduce current stress on the switch, help with the current collapse effect, and raise the efficiency (i^2R losses). The goal for placing GaN transistors in parallel is to merge the multiple $R_{ds(on)}$ parameters for each switch together so that it appears as a single, lower resistance,switch that can handle more current. In order to successfully parallel devices, careful consideration should be given such that each switch shares equal current and equally share losses. Furthermore, if there is unbalanced parasitics within the switches this can cause issues, especially at higher frequencies. As is discussed in the gate driver layout section of chapter 4, common source inductance and all current loop inductances should be minimized. Additionally, if source inductance is introduced to the GaN switch, each switch must have the same amount of source inductance in order to be balanced and conduct current equally. [59]

Appendix C

Supplementary Information for the Magnetics Section

Figure C.1 is an excerpt from [47] of two figures that depict eddy currents in a copper wire. This phenomenon offers an explanation for the current behavior caused by the skin and proximity effects.

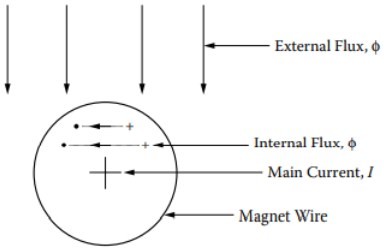


Figure 4-26. Flux Distribution in a Magnet Wire.

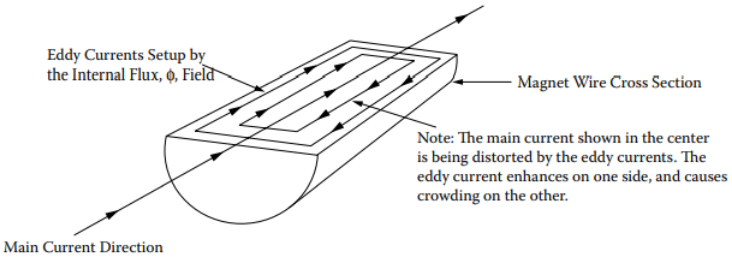


Figure 4-27. Eddy Currents Generated in a Magnet Wire.

Figure C.1: Diagram presenting a visual representation of eddy currents in a copper wire [47]

Appendix D

Supplementary Information for the Design Chapters

Chapter 4 Design

Figure D.1 presents the schematic/simulation created in the LT spice for the half-bridge LLC unidirectional converter

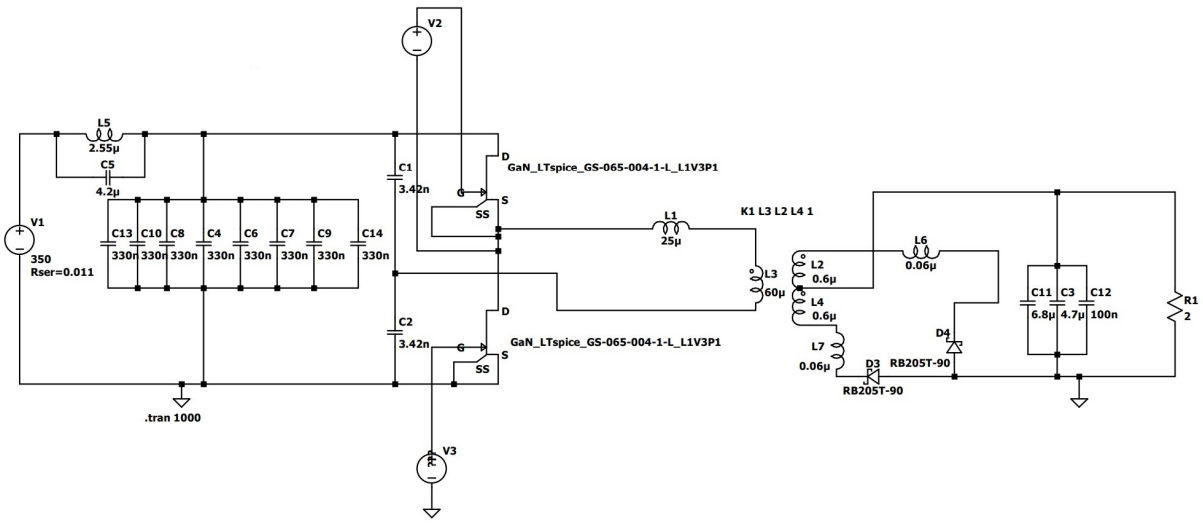
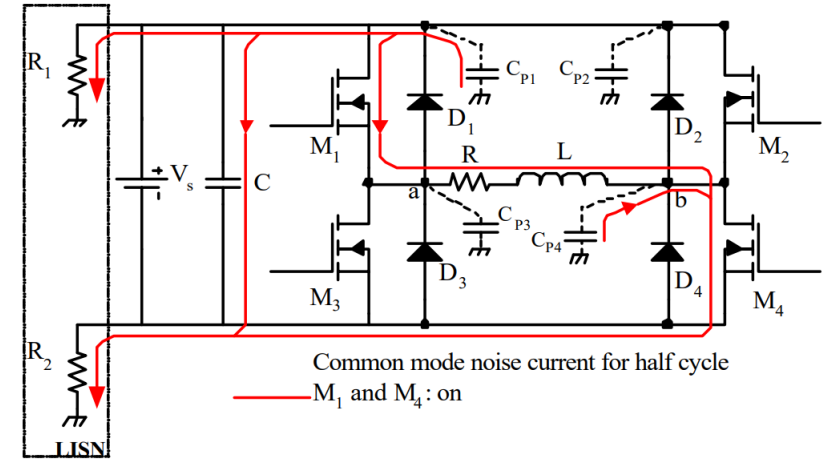


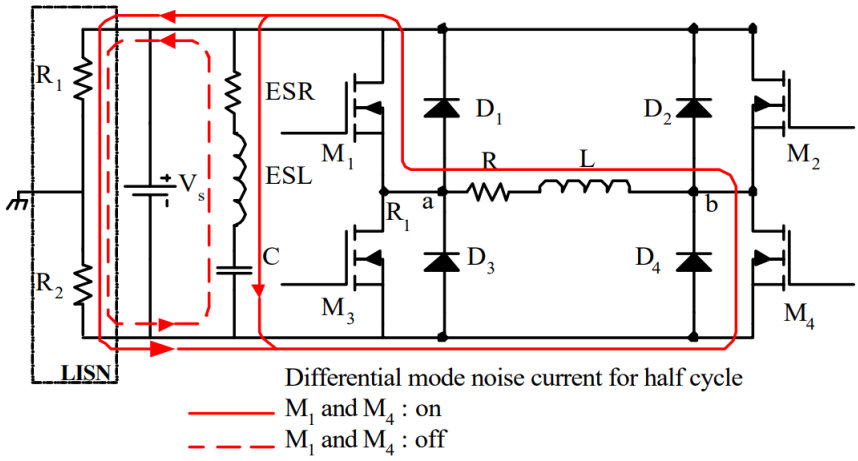
Figure D.1: LT Spice simulation for the half-bridge LLC unidirectional converter

Full-bridge vs Half-bridge

Figures D.2 and D.3 from [60] show the paths for differential and common mode noise currents in the full bridge and half bridge, respectively. These loops were carefully considered during the PCB lout phase in the unidirectional half-bridge LLC version of the converter. A full bridge is preferred in higher power applications. The maximum output voltage of the full-bridge converter is double that of a half-bridge converter. In order to achive the same power on the input and ouput, double the current is needed on the secondary side of the half-bridge [60].

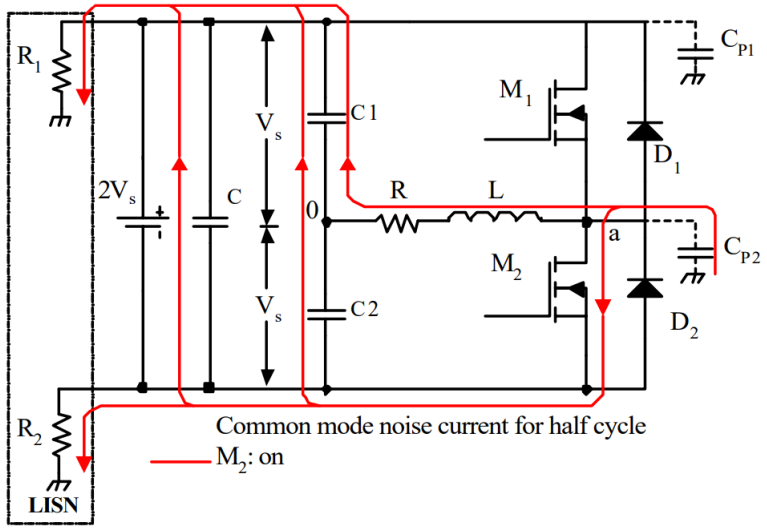


(a) Shows the route of common mode current

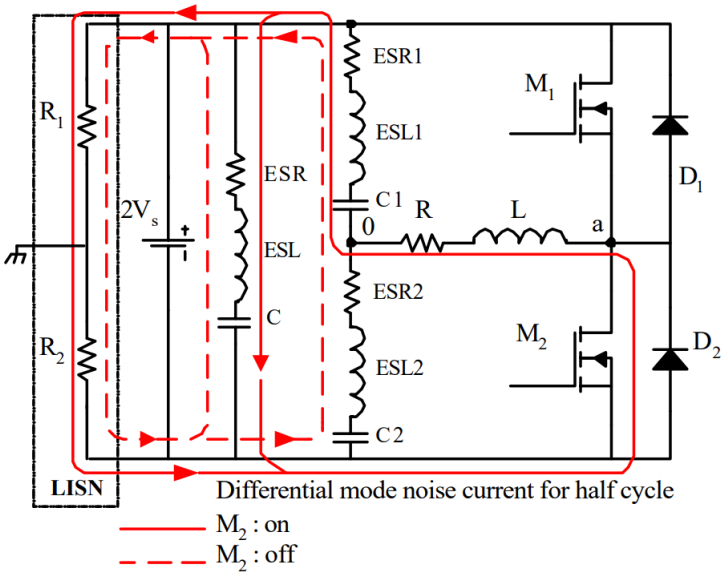


(b) Shows the route of differential mode current

Figure D.2: Differential and common-mode currents in full bridge circuit [60]



(a) Shows the route of common mode current



(b) Shows the route of differential mode current

Figure D.3: Differential and common-mode currents in half-bridge circuit [60]

Chapter 5 Design

The typical multi-layer PCB configuration and the properties of the FR4 insulation material were critical in the design of the planar transformer for the bidirectional DAHB converter. The electric strength of FR4 PCB material is 30-39 kV/mm and the industry standard pre-preg (pre-impregnated) epoxy is 32 kV/mm [61], [62]. The inner composition for a conventional market PCB can be seen in figure D.4.

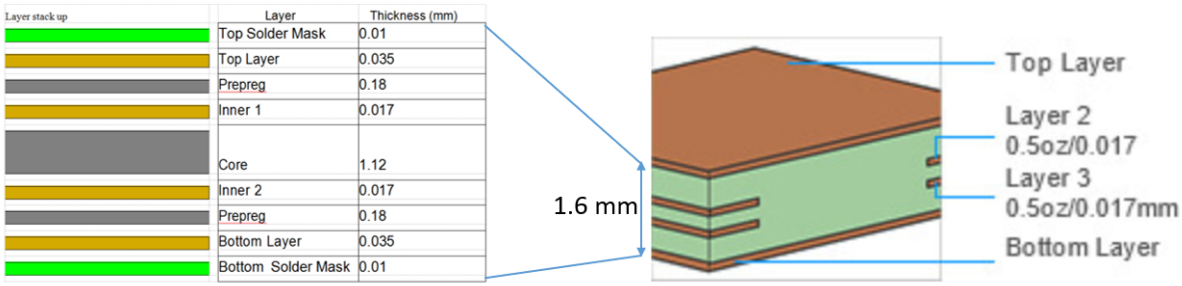


Figure D.4: Inner composition for a conventional market PCB with measured values. Where the core is FR4 material and prepeg (pre-impregnated) is fiberglass impregnated with resin [61], [62]

Figure D.5 presents the schematic/simulation created in the PLECS for the bidirectional DAHB converter.

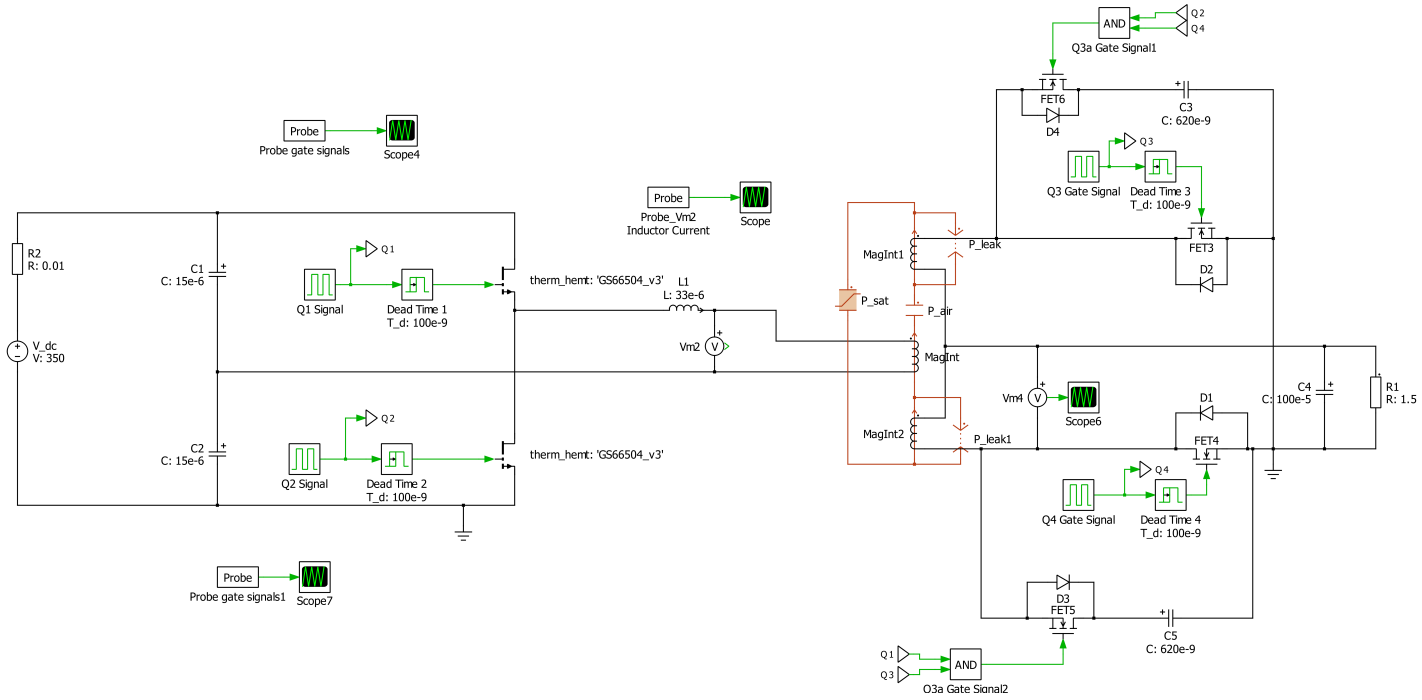


Figure D.5: PLECS simulation for the forward conduction bidirectional DAHB converter

Bibliography

[1] United Nations. Affordable and clean energy: Ensure access to affordable, reliable, sustainable and modern energy for all. [Online]. Available: https://unstats.un.org/sdgs/report/2019/goal-07/

[2] International Energy Agency, “World energy outlook 2018,” *Paris, France*, 2018.

[3] T. Den Heeten, N. Narayan, J.-C. Diehl, J. Verschelling, S. Silvester, J. Popovic-Gerber, P. Bauer, and M. Zeman, “Understanding the present and the future electricity needs: Consequences for design of future solar home systems for off-grid rural electrification,” pp. 8–15, 2017.

[4] B. Tenenbaum, C. Greacen, T. Siyambalapitiya, and J. Knuckles, *From the bottom up: how small power producers and mini-grids can deliver electrification and renewable energy in Africa*. The World Bank, 2014.

[5] Nishant Narayan, Victor Vega-Garita, Zian Qin, “The Long Road to Universal Electrification: A Critical Look at Present Pathways and Challenges,” *Energies*, vol. 13, 508, pp. 1–20, 2020.

[6] H. Louie, *Off-grid electrical systems in developing countries*. Springer, 2018.

[7] N. Narayan, A. Chamseddine, V. Vega-Garita, Z. Qin, J. Popovic-Gerber, P. Bauer, and M. Zeman, “Quantifying the benefits of a solar home system-based dc microgrid for rural electrification,” *Energies*, vol. 12, no. 5, p. 938, 2019.

[8] International Electrotechnical Commission, “Electricity access requirements with selv dc for tier ii and tier iii of esmap multi-tier framework for house hold electricity supply” as international standard,” *IEC, Geneva, Switzerland*, 2020.

[9] U. Badstübner, “Ultra-high performance telecom dc-dc converter,” Ph.D. dissertation, ETH Zurich, 2012.

[10] J. R. Aguero, E. Takayesu, D. Novosel, and R. Masiello, “Modernizing the grid: Challenges and opportunities for a sustainable future,” *IEEE Power and Energy Magazine*, vol. 15, no. 3, pp. 74–83, 2017.

[11] PLEXIM: Electrical Engineering Software. Buck converter. [Online]. Available: https://www.plexim.com/academy/power-electronics/buck-conv#:~:text=A%20Buck%20converter%20steps%20down,increases%20and%20the%20diode%20blocks.&text=Energy%20is%20transferred%20from%20the,in%20a%20decreasing%20inductor%20current.

[12] Miftakhutdinov, Rais, “Optimal design for an interleaved synchronous buck converter under high-slew-rate, load-current transient conditions,” *Analog Applications*, 2001.

[13] Gorji, Saman A and Sahebi, Hosein G and Ektesabi, Mehran and Rad, Ahmad B, “Topologies and control schemes of bidirectional dc–dc power converters: an overview,” *IEEE Access*, vol. 7, pp. 117 997–118 019, 2019.

[14] Botella, Juan Carlos Hernandez and Albert, Maria del Carmen Mira and Sen, Gökhan and Thomsen, Ole Cornelius and Andersen, Michael AE, “Isolated boost converter with bidirectional operation for supercapacitor applications,” *Journal of power electronics*, vol. 13, no. 4, pp. 507–515, 2013.

[15] Wai, R-J and Duan, R-Y and Jheng, K-H, “High-efficiency bidirectional dc–dc converter with high-voltage gain,” *IET Power Electronics*, vol. 5, no. 2, pp. 173–184, 2012.

[16] Picard, Jean, “Under the hood of flyback smps designs,” in *Texas Instruments Power Supply Design Seminar*, 2010, pp. 245–250.

[17] ST. Forward converter. [Online]. Available: https://www.st.com/en/applications/power-supplies-and-converters/forward-converter.html

[18] Würth Electronik. Switch mode power supply topologies compared. [Online]. Available: https://www.we-online.com/web/en/electronic_components/news_pbs/blog_pbcm/blog_detail-worldofelectronics_45887.php

[19] S. Microelectronics, “Application note an2644,”,” *An introduction to LLC resonant half-bridge converter*, 2008.

[20] Jung, Jee-Hoon and Kim, Ho-Sung and Ryu, Myung-Hyo and Baek, Ju-Won, “Design methodology of bidirectional cllc resonant converter for high-frequency isolation of dc distribution systems,” *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1741–1755, 2012.

[21] Noah, Mostafa and Shirakawa, Tomohide and Umetani, Kazuhiro and Imaoka, Jun and Yamamoto, Masayoshi and Hiraki, Eiji, “Effects of secondary leakage inductance on the llc resonant converter—part i: Transformer voltage gain and efficiency,” in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2019, pp. 780–786.

[22] Park, Hwa-Pyeong and Ryu, Younggon and Han, Ki Jin and Jung, Jee-Hoon, “Design considerations of resonant network and transformer magnetics for high frequency llc resonant converter,” *Journal of Electrical Engineering & Technology*, vol. 11, no. 2, pp. 383–392, 2016.

[23] Hofsajer, IW and Ferreira, Jan Abraham and Van Wyk, Jacobus D, “A new manufacturing and packaging technology for the integration of power electronics,” in *IAS’95. Conference Record of the 1995 IEEE Industry Applications Conference Thirtieth IAS Annual Meeting*, vol. 1. IEEE, 1995, pp. 891–897.

[24] Krismer, Florian, “Modeling and optimization of bidirectional dual active bridge dc-dc converter topologies,” Ph.D. dissertation, ETH Zurich, 2010.

[25] Chakraborty, Shiladri and Chattopadhyay, Souvik, “Fully zvs, minimum rms current operation of the dual-active half-bridge converter using closed-loop three-degree-of-freedom control,” *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10 188–10 199, 2018.

[26] ——, “Minimum-rms-current operation of asymmetric dual active half-bridge converters with and without zvs,” *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5132–5145, 2016.

[27] Kheraluwala, MN and Gascoigne, Randal W and Divan, Deepakraj M and Baumann, Eric D, “Performance characterization of a high-power dual active bridge dc-to-dc converter,” *IEEE Transactions on industry applications*, vol. 28, no. 6, pp. 1294–1301, 1992.

[28] Seeman, Michael D and Bahl, Sandeep R and Anderson, David I and Shah, Gaurang A, “Advantages of gan in a high-voltage resonant llc converter,” in *2014 IEEE Applied Power Electronics Conference and Exposition-APEC 2014*. IEEE, 2014, pp. 476–483.

[29] Roccaforte, Fabrizio and Greco, Giuseppe and Fiorenza, Patrick and Iucolano, Ferdinando, “An overview of normally-off gan-based high electron mobility transistors,” *Materials*, vol. 12, no. 10, p. 1599, 2019.

[30] Asif Khan, M and Kuznia, JN and Bhattarai, AR and Olson, DT, “Metal semiconductor field effect transistor based on single crystal gan,” *Applied Physics Letters*, vol. 62, no. 15, pp. 1786–1787, 1993.

[31] Colino, Stephen L and Beach, Robert A, “Fundamentals of gallium nitride power transistors,” *Industry Report from Efficient Power Conversion*, pp. 1–4, 2011.

[32] Johan Strydom, David Reusch, Steve Colino, Alana Nakata, “Using enhancement mode gan-on-silicon power fets (egan® fets).”

[33] Sugiyama, Toru and Oasa, Kohei and Saito, Yasunobu and Yoshioka, Akira and Kikuchi, Takuo and Shindome, Aya and Ohguro, Tatsuya and Hamamoto, Takeshi, “Evaluation methodology for current collapse phenomenon of gan hemts,” in *2018 IEEE International Reliability Physics Symposium (IRPS)*. IEEE, 2018, pp. 3B–4.

[34] Hasan, Md Tanvir, “Mechanism and suppression of current collapse in algan/gan high electron mobility transistors,” *Dissertation, University of Fukui*, 2013.

[35] H. Sin, “Normally-off and current collapse free gan transistor,” *Application note of Panasonic*.

[36] Efthymiou, Loizos and Camuso, Gianluca and Longobardi, Giorgia and Udrea, Florin and Lin, Evelyn and Chien, Terry and Chen, Max, “Zero reverse recovery in sic and gan schottky diodes: A comparison,” in *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*. IEEE, 2016, pp. 71–74.

[37] Davis, Sam. The great semi debate: Sic or gan? [Online]. Available: https://www.powerelectronics.com/technologies/power-management/article/21864289/the-great-semi-debate-sic-or-gan

[38] Bruckewell Group. Potential application of wide gap semiconductors. [Online]. Available: http://www.bruckewell-semi.com/in_SIC_Products.html

[39] Arlt, Bodo, “The future of gan: An interview with alex lidow of epc,” *EE Power*, 2019.

[40] Dauhajre, Abraham and Middlebrook, RD, “Modelling and estimation of leakage phenomena in magnetic circuits,” in *1986 17th Annual IEEE Power Electronics Specialists Conference*. IEEE, 1986, pp. 213–226.

[41] Art Pini. The basics of isolation transformers and how to select and use them. [Online]. Available: https://www.digikey.com/en/articles/the-basics-of-isolation-transformers-and-how-to-select-and-use-them

[42] Schneider Electric. What is significance of separated or safety extra-low voltage (selv). [Online]. Available: https://www.se.com/in/en/faqs/FA253330/

[43] Wurth Elektronic. Transformer design considerations. [Online]. Available: https://www.st.com/content/ccc/resource/sales_and_marketing/promotional_material/newsletter/group0/6b/10/c1/aa/ba/76/41/cf/Wurth_Design_Considerations_Munich/files/Wurth_Design_Considerations_Munich.pdf/jcr:content/translations/en.Wurth_Design_Considerations_Munich.pdf

[44] cet. What is a planar transformer? [Online]. Available: https://www.cettechnology.com/what-is-a-planar-transformer/

[45] Saket, Mohammad Ali and Ordonez, Martin and Craciun, Marian and Botting, Chris, “Improving planar transformers for llc resonant converters: Paired layers interleaving,” *IEEE Transactions on Power Electronics*, vol. 34, no. 12, pp. 11 813–11 832, 2019.

[46] Nikolov, Georgi T and Valchev, Vencislav C, “Nanocrystalline magnetic materials versus ferrites in power electronics,” *Procedia Earth and Planetary Science*, vol. 1, no. 1, pp. 1357–1361, 2009.

[47] C. W. T. McLyman, *Transformer and inductor design handbook*. CRC press, 2017.

[48] Zurek, Stan. Flux fringing. [Online]. Available: http://www.encyclopedia-magnetica.com/doku.php/flux_fringing

[49] Dixon, Lloyd H, “Magnetics design for switching power supplies,” in *Unitrode Seminar*, 2001.

[50] Daut, Ismail and Syafruddin, HS and Ali, Rosnazri and Samila, M and Haziah, H, “The effects of harmonic components on transformer losses of sinusoidal source supplying non-linear loads,” *American Journal of Applied Sciences*, vol. 3, no. 12, pp. 2131–2133, 2006.

[51] Terratel. Advantages of planar transformers: Design features and benefits of using planar transformers. [Online]. Available: https://www.terratel.eu/advantages-planar-transformers.html

[52] L. Dixon, “Designing planar magnetics,” in *Power Supply Design Seminar*, 2006, pp. 2006–2007.

[53] Quinn, Conor and Rinne, Karl and O’Donnell, Terence and Duffy, Maeve and Mathuna, CO, “A review of planar magnetic techniques and technologies,” in *APEC 2001. Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No. 01CH37181)*, vol. 2. IEEE, 2001, pp. 1175–1183.

[54] Y.-C. Liu, C. Chen, K.-D. Chen, Y.-L. Syu, and M.-C. Tsai, “High-frequency llc resonant converter with gan devices and integrated magnetics,” *Energies*, vol. 12, no. 9, p. 1781, 2019.

[55] Arrigo, Jason, “Input and output capacitor selection,” *SLTA055*, 2006.

[56] Carsten, Bruce W, “The low leakage inductance of planar transformers; fact or myth?” in *APEC 2001. Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No. 01CH37181)*, vol. 2. IEEE, 2001, pp. 1184–1188.

[57] F. Xue, R. Yu, and A. Q. Huang, “A 98.3% efficient gan isolated bidirectional dc–dc converter for dc microgrid energy storage system applications,” *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9094–9103, 2017.

[58] Lidow, Alex and De Rooij, Michael and Strydom, Johan and Reusch, David and Glaser, John, *GaN transistors for efficient power conversion*. John Wiley & Sons, 2019.

[59] Reusch, David and Strydom, Johan, “Improving performance of high speed gan transistors operating in parallel for high current applications,” in *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. VDE, 2014, pp. 1–8.

[60] Srisawang, A and Panaudomsup, S and Prempraneerach, Y, “Comparison of emi performance of full-bridge and half-bridge power converter,” in *International Conference on NOLTA*, 2002, pp. 203–306.

[61] Candor Circuit Boards. What exactly is prepreg in a pcb? [Online]. Available: https://www.candorind.com/what-is-a-prepreg-pcb/

[62] Euro Technologies. Thermally conductive pre-preg dielectric. [Online]. Available: https://www.euro-technologies.eu/en/product/thermally-conductive-pre-preg-dielectric/