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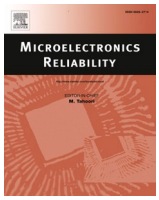

Effect of microstructural variability on fatigue simulations of solder joints

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ABSTRACT

The objective of this work is to develop a microstructure-based simulation approach to assess the fatigue life of solder joints that are used by the microelectronics industry. The developed approach can generate solder joints with random grain morphologies by means of 3D Voronoi tessellation. The anisotropic material behavior of each grain is described by the Garofalo creep equation combined with Hill's definition of the equivalent stress for anisotropic materials. Grain boundaries are implemented as interface elements, with an isotropic creep constitutive model. The stochastic variability in the creep response of solder joints was qualitatively estimated by generating 100 unique solder joints containing 5 to 9 grains, each having a random material orientation. These joints were independently loaded with a realistic stress level for microelectronic products during thermal cycling. The volume-averaged creep strain energy density in the solder joints was used to predict the fatigue life of the solder joints. The results showed a factor of ~4 difference in expected lifetime of the individual solder joints. Next, nine randomly picked solder joints from the above-mentioned pool of 100 were sandwiched between a silicon die and a printed circuit board to form a simulation model of a Wafer-Level Chip-Scale package (WLCSP). The creep strain energy density in the joints was computed for 34 unique cases of the WLCSP. A factor of ~2.5 between the highest and lowest estimate for the solder joint life was found. The slope of the corresponding Weibull distribution equals ~6, which falls within the slopes typical reported for solder joint reliability of WLCSPs.

1. Introduction

Microelectronic packages are used to protect the sophisticated microelectronic circuity from environmental hazards, such as moisture, whereas it provides electrical connectivity to the environment [1]. The package is usually connected to a Printed Circuit Board (PCB) by solder joints, which are typically of the size of 10s to 100s of micrometers. Repeated high temperatures, originating from the environment, as well as from (high) power densities generated by the microcircuit itself, give rise to cyclic mechanical stress throughout the operational lifetime of a product. This stress can result in reliability issues such as warpage of the package and delamination of internal interfaces [2,3], or solder joint fatigue [4]. The solder joints are often critical for the reliability of the assembly; a single solder joint failure can cause failure of the whole semiconductor device [4]. Consequently, it is understandable why research on solder joints has been a major topic in the semiconductor industry ever since its inception. An accurate simulation model of solder joints, including their stochastic variability, will accelerate this research, and will have practical application by reducing empiricism during product development.

The commonly used SnAgCu (SAC) solder joints are composed of a few grains, each consisting of ~95 % body centered tetragonal $\beta - Sn$ [5] which aggregate to form oligocrystalline solder joints, such as shown in Fig. 1. The few $\beta - Sn$ grains have a dominating effect on the thermomechanical (creep) response of the joints because of their strong anisotropy, and high atomic percentage [6–8]. The processes currently used to manufacture solder joints result in grains with near-random orientations [8,9]. Typical joints are composed of 1 to 12 independent grains, with an estimated average of 8 grains per joint [8]. Given the low number of grains, microstructural effects on the creep response become non-negligible [10]. Creep in solder joints is a complex phenomenon that combines diffusion and dislocation climb both within the grains and near the boundaries [11,12] The creep behavior of grain boundaries, however, is not nearly as well-researched as that of grains. The

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composition of grain boundaries tends to be more variable than that of the grains since alloying additives tend to segregate there [13]. Grain boundaries also play a critical role in the nucleation and propagation of fatigue cracks in the solder joints [14–16] and are therefore of high interest to solder joint reliability. When subjected to cyclic thermo-mechanical deformation, the grains dynamically recrystallize in the regions of high inelastic deformation [8]. The new grain boundaries generated from this grain fragmentation process are sites of fatigue crack growth due to grain boundary sliding. Another important characteristic of the microstructure of SAC solder joints are the intermetallic compounds (IMC) that form at the top and bottom interfaces of the joint. The composition of these IMCs is determined by the surface plating material of the adjacent metallic pads [17]. This surface plating then reacts with the solder bulk to form compounds, such as Ag_3Sn or Cu_6Sn_5 [8,18,19]. The differences in IMC composition can lead to changes in mechanical properties, affecting the creep behavior of the solder joint [20,21].

Although a considerable part of the reported research on solder joints has focused on techniques that allow for more accurate Finite Element (FE) simulations of their fatigue life, the current best practice in the industry still uses homogenized isotropic constitutive models. In this work the focus is on a microstructure-based simulation approach. First, the key 'building blocks' of the microstructural modeling strategy are explained; (i) the constitutive equations used for the grains, (ii) the interface element approach used to model the grain boundaries, and (iii) the Voronoi tessellation algorithm used to generate solder joint geometries containing unique grain morphologies. Next, it is shown how these building blocks are used to generate a stochastic pool of unique FE models for single solder joints. This pool is then used to generate several models for complete packages, each fitted with a random combination of solder joints. The results of these models are used to estimate the effect of microstructural anisotropy on a realistic simulation of a microelectronic product.

2. Microstructural finite element modeling strategy

2.1. Constitutive equations for β − Sn grains

The Garofalo-Hill constitutive combines the Garofalo creep law for the steady-state creep rate with the equivalent Hill stress formulation for anisotropic materials. The hyperbolic sine Garofalo relation is often used in the literature to compute steady-state creep at high temperatures and stress magnitudes since power law formulations usually 'break down' at these regimes [22]. The Garofalo constitutive equation writes [23],

$$\dot{\bar{\varepsilon}} = C_1[sinh(C_2\bar{\sigma})]^{C_3}\ exp(-C_4/T), \tag{1}$$

where $\dot{\bar{\varepsilon}}$ is the equivalent creep strain rate, $\bar{\sigma}$ the equivalent stress, T the temperature in Kelvin, and C_1, C_2, C_3, and C_4 are material parameters. The equivalent stress follows from the Hill yield criterion, defined as,

$$\bar{\sigma}_{Hill} = \sqrt{F(\sigma_{22}-\sigma_{33})^2 + G(\sigma_{33}-\sigma_{11})^2 + H(\sigma_{11}-\sigma_{22})^2 + 2L\sigma_{23}{}^2 + 2M\sigma_{13}{}^2 + 2N\sigma_{12}{}^2}, \tag{2}$$

where F, G, H, L, M and N are constants, defining the state of anisotropy within the material [24]. Note that one obtains the isotropic von Mises yield criterion for $F = G = H = 1/2$, and $L = M = N = 3/2$. The components of the creep strain tensor follow from the flow rule,

$$\dot{\varepsilon}_{ij} = \dot{\bar{\varepsilon}}\frac{\partial\bar{\sigma}_{Hill}}{\partial\sigma_{ij}}. \tag{3}$$

Finally, the Garofalo-Hill model is coupled with corresponding description for the anisotropic linear elastic behavior, $\sigma = C\,\varepsilon_e$, where σ gives the components of the stress tensor (in Voigt notation), C is the stiffness matrix, and ε_e denotes the components of the elastic strain tensor (in Voigt notation).

2.2. Interface element for the grain boundaries

As in previous work [11,24], grain boundaries are modeled as very thin layers of isotropic material. Consequently, the equivalent stress and equivalent strain in the grain boundary are represented by a von Mises' formulation rather than Hill's formulation. In this work we use infinitesimally thin interface elements instead of modeling the interface as explicit thin layers. Interface elements were recently used to successfully model intergranular fracture in polycrystalline solids [26,27]. The interface elements in this work, however, are used to model the undamaged behavior of the grain boundaries.

Previous research on creep of pure Sn and Sn-based polycrystalline alloys has found a linear dependence of the equivalent creep strain rate on the equivalent stress within the grain boundary, at a given temperature [28] [29],

$$\dot{\bar{\varepsilon}} = A_{GB}\bar{\sigma}, \tag{4}$$

where A_{GB} is a constant that represents the influence of multiple factors such as the thickness, diffusivity and temperature.

In order to use Eq. (4) in commercial FE software, the stress and strain components will be converted to *tractions* and *displacements*. Consequently, the interface elements will become consistent with standard cohesive zone elements (see Fig. 2), which are readily available in most FE codes. Note that the displacements are the separations of the node pairs that are initially collocated at the boundaries of adjacent

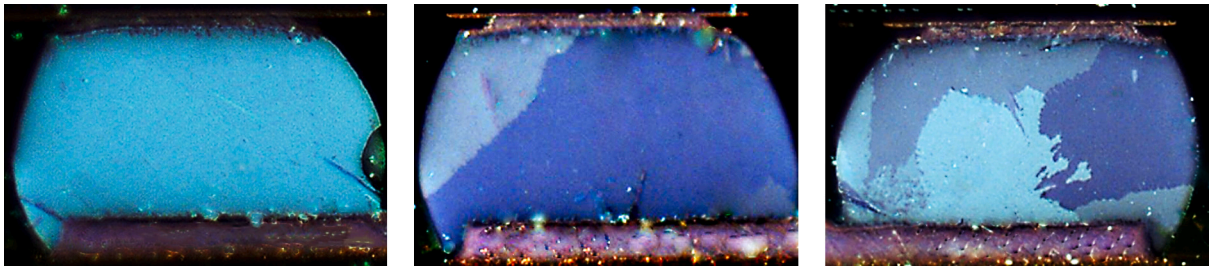

Fig. 1. Cross-polarized images of cross-sections of three oligocrystalline solder joints from a single product showing their grain morphology; single crystal (left), bi-crystal (center), and four grains (right).

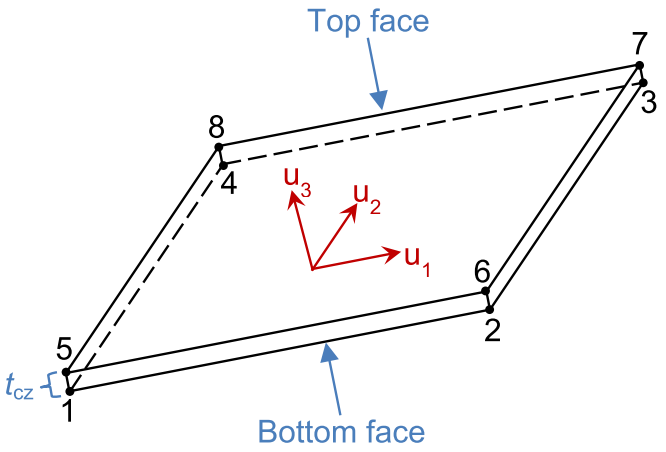

Fig. 2. Schematics of an interface element; initially the bottom and top face lie on top of each other, the relative displacements of the nodes (1–8) are given by a normal and two shear components.

elements. As the interface elements have no actual (initial) thickness, only three stress components are defined: one in the normal direction and two shear components. Instead of using a conventional stiffness matrix connecting the collocated node-pairs, cohesive zone elements use a traction-separation law of the form,

$$\sigma_i^{coh} = D\, u_i^{coh}, \tag{5}$$

where σ_i^{coh}, and u_i^{coh} are the three stress components (a.k.a. the traction components) described above and their corresponding separations, and D are the linear stiffness coefficients of the traction-separation law. There is a disconnect between the constitutive models described by Eq. (4) and the relation given by Eq. (5), since the former uses strains, whereas the latter uses displacements. The strain components are equal to the corresponding displacement components divided by the initial grain boundary thickness. However, since the interface elements have no initial thickness, common practice is to define a constitutive thickness, t_{cz}, which is simply a reference value used for convenience of calculations. Methods in the literature recommend using a constitutive thickness of 1 μm rather than the real thickness of the grain boundary in order to facilitate computations [28]. The elasticity and creep constitutive relations must therefore be modified accordingly before they can be used in the separation tracking scheme of an interface element. Substituting $\dot{\bar{e}} = \dot{\bar{u}}/t_{cz}$ in Eq. (4) yields

$$\dot{\bar{u}} = A_{GB} t_{cz} \bar{\sigma}, \tag{6}$$

for the equivalent separation rate due to creep. According to Hooke's law the stress on the interface element is given by,

$$\sigma_{ij} = \frac{G}{t_{cz}} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 2\langle 1+\upsilon \rangle \end{bmatrix} \begin{Bmatrix} u_1^{el} \\ u_2^{el} \\ u_3^{el} \end{Bmatrix}, \tag{7}$$

where G is the shear modulus, ν the Poisson's ratio, superscript *el* indicates the elastic part of the displacement, and the subscript 1, 2, and 3 are the two in-plane and out-of-plane directions, respectively. Note that the elastic displacement equals the total displacement minus the displacement due to creep. The original constitutive model deals in terms of equivalent tractions and displacements, to convert them into directional components it is necessary to multiply the equivalent stress in Eq. (6) by the stress gradient, $\partial\bar{\sigma}/\partial\sigma_{ij}$, (likewise the flow rule of Eq. (3)) where the equivalent stress is given by

$$\bar{\sigma} = \sqrt{\sigma_n{}^2 + 3(\tau_1 + \tau_2)^2}, \tag{8}$$

where σ_n, τ_1, and τ_2 refer to the out-of-plane normal stress and the two in-plane shear stress components, respectively. The equivalent stress is simply a modified version of the isotropic von Mises stress in which the stress components in the directions that are not considered by the interface element are set to zero. To solve the set of ordinary differential equation, an implicit Runge–Kutta method based on the trapezoidal rule is used where the assumption is made that the strain rate is constant over the time interval. When under compression, the stiffness of the interface element is multiplied by a penalty factor (10^6) to prevent penetration of elements, and the creep rate in compression is accordingly set to zero.

2.3. Voronoi tessellation to generate the microstructure

In our simulation model, the variability in solder joint microstructure must be accounted for in terms of number, size, and crystallographic orientation of the solder grains. To this purpose, a 3D space partitioning method capable of representing the random grain distributions in different solder joints is developed. This method is based on Voronoi tessellation, which divides a space into regions so that each region is made up of all the points that are the closest to a so-called seed (Fig. 3). These regions are called cells, which in this work represent the grains. Voronoi tessellation has been used extensively in computational material science to model random polygonal grains [30,31].

A script has been developed in Python for tessellating an arbitrarily-shaped 3D object using the *scipy.spatial* library, which features a function capable of generating a Voronoi object starting from given seed coordinates. This function bases its outputs on the Voronoi vertices, i.e. the vertices of each cell polygon. The segments (in 2D) or planes (in 3D) connecting these vertices are known as ridges. Generating a Voronoi tessellation starting from completely random seeds may result in some cells having shapes that would be unrealistic for grains in a solder joint microstructure. One way to remedy this is by using centroidal Voronoi tessellation, in which every seed is also the centroid of its cell. A centroidal tessellation can only be achieved by having appropriate starting seeds. The *CVTSampling* function from the *idaes.surrogate.pysmo.sampling* library is capable of generating a random combination of such"centroidal seeds".

The diagrams generated by *scipy.spatial.voronoi* are unbounded; the dashed lines in Fig. 3 are unbounded ridges. It is necessary to clip the unbounded ridges in the 3D Voronoi diagram into a shape that is typical

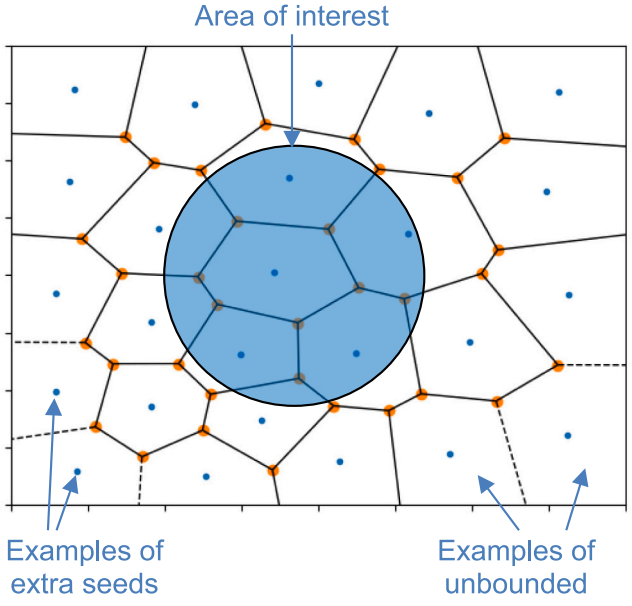

Fig. 3. Illustration of extra seeds method for bounding of Voronoi region to prevent unbounded regions to intersect with the region of interest.

for solder joints. The starting input of the tessellation is the number of grains to be generated, which is chosen with the Python function *random.random*. The Python script takes the number of seeds and generates a centroidal Voronoi diagram. The problem of unbounded ridges is solved by applying extra seeds at a significant distance from the area where the solder joint is supposed to be. By doing so, the joint area (e.g. the blue part of Fig. 3) is filled only with finite ridges. The last step to obtain the microstructure geometry consists of intersecting the imported ridges with a solder joint-shaped solid.

3. Simulation model of a microelectronics package

The modeling strategy as outlined in the previous section has been implemented in the commercial Marc Mentat software from Hexagon. This section provides details on how this implementation was achieved. The solder alloy considered in this work is SAC305, i.e., an alloy containing 96.5 % Sn, 3 % Ag, and 0.5 % Cu. SAC305 is a common soldering alloy for semiconductor packages. In addition to the anisotropic creep properties described by the Garofalo-Hill equations, the solder material exhibits anisotropic elasticity as well. To be accurate, SAC305 is orthotropic, with two out of the three principal directions having the same properties both for the elastic and the creep behavior. An approximation is made where the elastic constitutive matrix is constant with temperature, as the orthotropic elastic properties of the SAC grains have not yet been well quantified over a range of temperatures [32]. The same applies to the Garofalo creep constants and the Hill coefficients. Thermal expansion is orthotropic in nature as well, with the Coefficients of Thermal Expansion (CTEs) linearly temperature dependent. Furthermore, the properties used for the isotropic grain boundaries (i.e. G, A_{GB} and ν) are all taken to be temperature independent, since sufficient characterization is missing. Consequently, the results in this work will qualitatively illustrate the microstructural dependence on the mechanical behavior of solder joints. For a full temperature dependent, and quantitative, analysis further experimental characterization of the properties of both the grains and the interfaces is required. An overview of properties used in the simulations is given in Table 1.

The meshing process for grain morphology in solder joints has been fully automated. A surface mesh is first generated on the 3D solids produced by the Voronoi tessellation algorithm. The complete steps in the meshing process are: (i) *Seeding of surfaces*: the solid surfaces are seeded according to the preferred seed size, (ii) *Surface Meshing:* a triangular surface mesh is generated on the seeded solids, (iii) *Conversion of surface mesh to faceted surfaces:* the benefit of using faceted surfaces is that they are orientation-independent, thus it is not necessary for them to have normal vectors oriented in the same direction, (iv) *Removal of the 3D solids:* these geometric entities are not necessary anymore and are discarded, (v) *3D Meshing:* a tetrahedron-based 3D mesh is generated from the faceted surfaces. Tetrahedrons are used instead of hexahedron elements since they are better capable of reconstructing rounded shapes [33]. The mesh is conformal across the complete joint. An example of the final mesh for a solder joint containing randomly generated polycrystalline morphology is given in Fig. 4. An appropriate element size was determined via a mesh convergence study. An average edge length of 35 μm is used for the elements in the solder joints.

A pool of 100 unique solder joints was generated according to the methodology described above. The joints are sandwiched between two copper pads. The copper is assumed linear elastic with a Young's modulus (E) equal to 110 GPa, $\nu = 0.33$, and a CTE of16.5 ppm/K. The size of all solder joints in the pool is constant. The dimensions are chosen to be consistent with solder joints typically used for Wafer-Level Chip-Scale Packages (WLCSP). The dimensions are:

- Height (without copper pads): 175 μm.
- maximum radius of the joint: 150 μm.
- Top pad thickness: 8.75 μm.
- Bottom pad thickness: 17.5 μm.
- Pad radius: 125 μm.

Five to nine grains were generated per joint using the Python function *random.random*. The same function was used to randomly rotate the internal material axis of the grains.

The final step is to combine multiple solder joints from the pool of 100 joints, into a simulation model of a WLCSP (see Fig. 5) with overall dimensions of 1.2 × 1.2 × 0.4 mm. The model is simplified but believed to be still sufficiently realistic to represent the general trends of a possible real product. The model consists of solid block of silicon (1200x1200x225 μm) that are connected to a PCB (3.6 × 3.6 × 1 mm) using nine solder joints (3 × 3 array at 400 μm pitch). The silicon is modeled as an isotropic material with $E = 169$ GPa and $\nu = 0.23$ [34], with a temperature-dependent CTE (2.35 ppm/K at room temperature) [35]. The PCB is also treated as an isotropic material, but in this case, E is temperature dependent (17.4 GPa at room temperature) while the CTE is constant at 19.6 ppm/K. Quadratic interpolation functions are used for all elements in the model. The meshes of the silicon block, copper pads, and PCB are all made by an extrusion method. The result is a mixed mesh containing both tetrahedral and hexahedral elements. The mesh

Table 1
overview of the constants used for the numerical analysis of solder crystals (for the selected microstructural state, as determined from crystal viscoplasticity analysis) [11,12,25,32].

Elastic constants for the grains					
$C_{11} = C_{22}$	C_{33}	$C_{23} = C_{13}$	C_{12}	$C_{44} = C_{55}$	C_{66}
73.4 GPa	89.3 GPa	36.4 GPa	59.6 GPa	22.3 GPa	24.2 GPa
Hill constants					
$F = G$	H	$L = M$	N		
1.0	4.56	4.15	1.49		
Creep constants of the grains					
C_1	C_2	C_3	C_4		
22.75	0.095 1/MPa	2.5	55.8 kJ/mol		
Coefficient of thermal expansion					
	x and y direction		z direction		
233 K	16.6 ppm/K		32.1 ppm/K		
398 K	19.8 ppm/K		36.8 ppm/K		
Elastic and creep constants interfaces					
G	ν	A_{GB}			
26.3 GPa	0.33	$1.05{\cdot}10^{-6}$ 1/MPa			

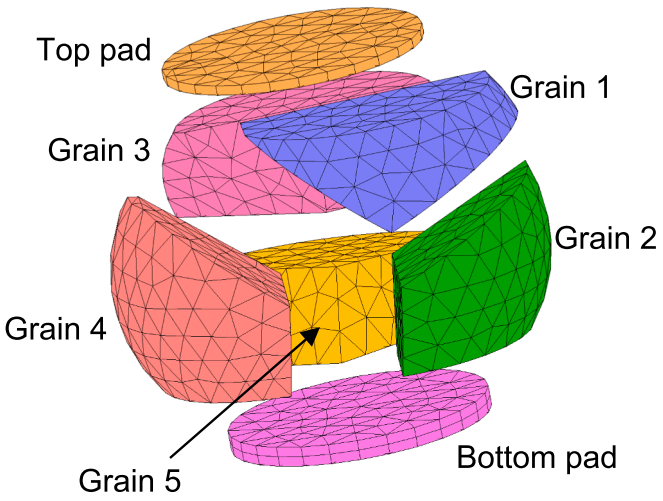

Fig. 4. Exploded view of the mesh of a randomly generated solder joint.

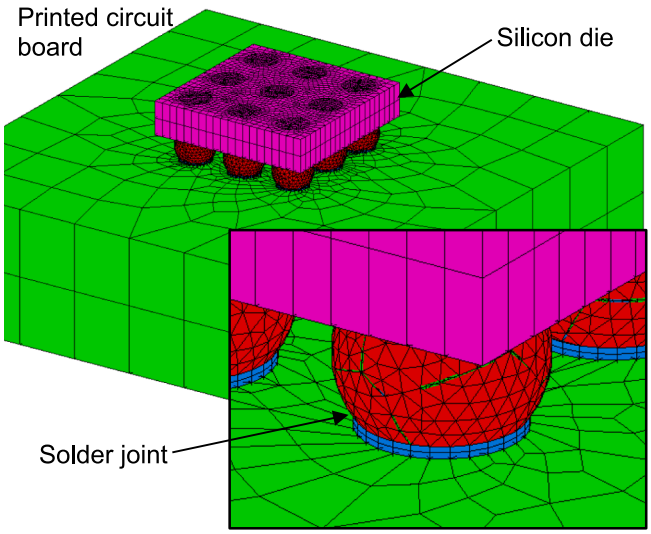

Fig. 5. FEM model of sample WLCSP product.

across the complete model is conformal, which circumvents numerical problems with tying equations at the interfaces. The boundary conditions for the model are set for the PCB to freely expand/contract and warp by constraining one corner point in x-,y- and z-direction, another corner in y- and z-direction, and a final corner point in z-direction. These constraints serve to prevent rigid body motions. The only applied loading is the temperature cycling by applying a uniform temperature with a cyclic profile between −40 °C and 125 °C, with 15-min dwell and ramp times. In total 3 thermal cycles are simulated. These thermal cycling conditions are according to JEDEC specification [40].

4. Results & discussion

The main output variable of the FE simulations is the Creep Strain Energy Density (CSED) accumulated over the thermal cycles as it is a metric often correlated to fatigue damage in solder joints [22 [36] [37] [38]. The CSED has been averaged over different volume domains in order to provide more insight on the behavior of individual grains and of solder joints as a whole. In accordance to literature, a postulate is made that the fatigue life of a solder joint or grain is inversely proportional to the volume-averaged accumulated CSED [22].

4.1. Single solder joints

The first series of results have the objective of analyzing a single solder joint with a fixed-grain microstructure and constant boundary conditions, but with varying orientation of the grains. The boundary conditions compose of a compressive stress of 0.1 MPa on the top pad, with the bottom pad fully constrained in all directions. The cyclic temperature profile of Section 3 is used, whereas a corresponding cyclic horizontal shear load between 0 and 15 MPa is applied on the top pad of the solder joint. The considered joint contains 5 grains (as shown in Fig. 4), which is the minimum among the solder joints used in this work. The averaged CSED over the whole solder joint is analyzed for 100 different combinations of grain orientations. The distribution of CSED values is shown in Fig. 6. The solder joint with the most creep-sensitive grain orientations experiences approximately 2.5 times as much accumulated CSED than the least sensitive one.

The second series of results expands the first one, now each solder joint has a unique microstructural geometry, whereas the orientation of each grain is randomized as well. Again, 100 unique solder joints were simulated. The boundary conditions are the same as for the previous study. The CSED is extracted and averaged over the whole solder joint

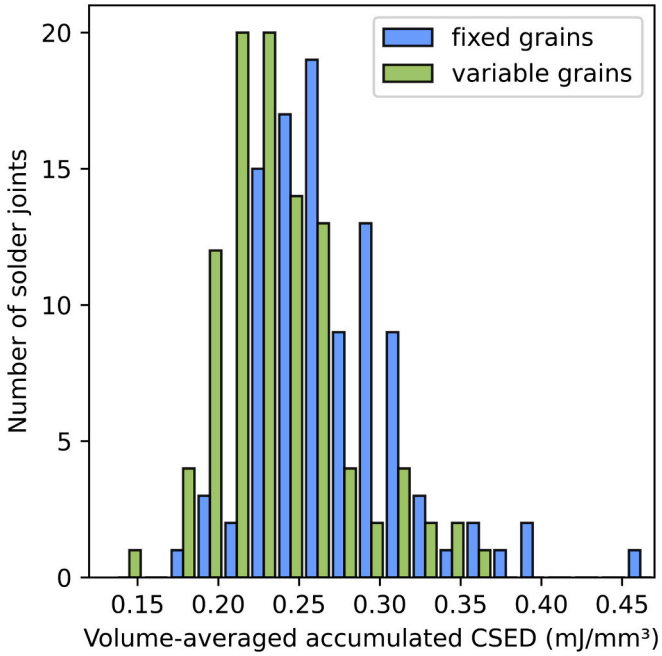

Fig. 6. CSED histogram of joints with fixed-grain structure (blue) and variable microstructural geometry (green). For both cases the orientation of the grains was varied randomly.

volume; the resulting distribution is shown in Fig. 6. With respect to the previous results, the difference between the lowest and highest accumulated CSED values is similar at ~0.20 mJ/mm3. This suggests that the material orientations of the grains have a significant contribution on the resulting variability compared to the shape and amount of grains. While the variability seems to be unaffected, the magnitude of the accumulated CSED is influenced by the grain geometry. The mean for the CSED in case of a fixed grain structure is higher than for the full variable microstructure (0.270 vs 0.238 mJ/mm3, respectively).

An additional analysis was performed on the results of the full

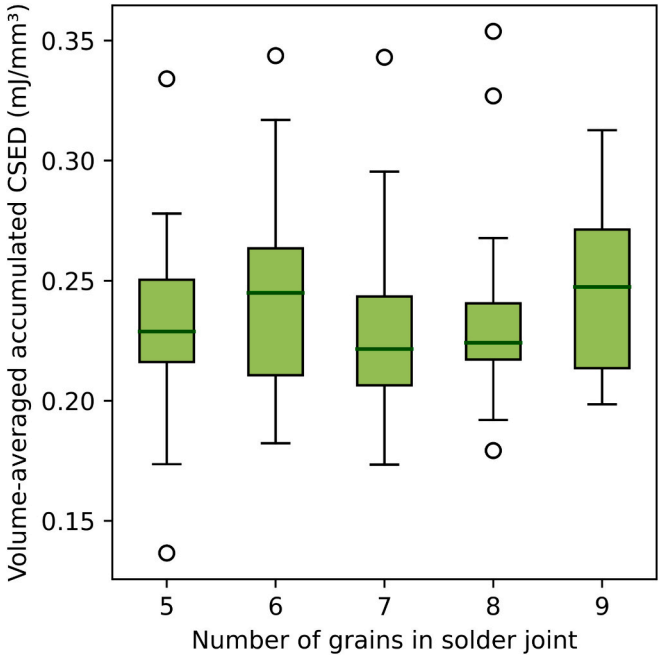

Fig. 7. Box plot of CSED in single solder joints sorted by number of grains in the joint.

variable microstructure to investigate whether the number of grains in a solder joint is correlated to the overall creep response of the whole joint. To this end, this CSED data has been sorted by number of grains in the joint as shown in Fig. 7. It seems that the number of grains in a joint (within the range studied) does not have a significant effect on either the magnitude or the variance of the CSED that developed within the solder joints.

4.2. Package level

Next the general behavior of solder joints within the WLCSP model will be discussed. Fig. 8 depicts the CSED in the solder joints after three thermal cycles. By tracking its evolution, it was found that the CSED accumulates initially at the corners and later spreads along the interfaces with the copper pads. As the CSED is correlated with fatigue damage, it may be inferred that an eventual crack would begin at the corners and then propagate adjacent to the interface. This behavior is in accordance with numerous studies on the thermomechanical response of SAC solder joints [39–41]. Furthermore, the joints at the corners experience higher CSED magnitudes than the edge joints (Fig. 8). The explanation for this is their increased distance from the assembly's neutral point. With the silicon and PCB expanding and contracting radially to the neutral point during temperature cycling, the central solder joint will experience the smallest mismatch in displacement while the furthest solder joints will experience the highest mismatch. This is also in line with typical experimental observations, where the corners joints virtually always fail first.

For a stochastic analysis of the solder joints, 34 sample products were simulated, each fitted with a unique combination of random grain morphologies in the solder joints. The accumulated CSED has been averaged over the volume of the entire solder joint. The results are plotted in Fig. 9 for the corner and edge joints in all the products, where"edge" refers to all solder joints at the edge of the solder joint array minus the corner ones (see Fig. 8). The distributions for the edge and corner datasets are qualitatively similar. Note that the highest CSED value in the edge joint dataset is higher than the lowest value from the corner dataset. This does not necessarily mean that a sample product may have its most critical location with respect to solder fatigue outside of a corner joint, as the maximum edge joint CSED and the minimum corner joint CSED are coming from two different simulation models.

A special case was tested to verify whether an edge joint could accumulate more CSED than the corner joints due to having a particular grain microstructure. Bieler et al. [5] stated that the most critical $\beta - Sn$ orientation with respect to fatigue fracture is the one in which the material z-axis is parallel to the PCB. It is then hypothesized that the most creep-resistant orientation is that in which the material z-axis is

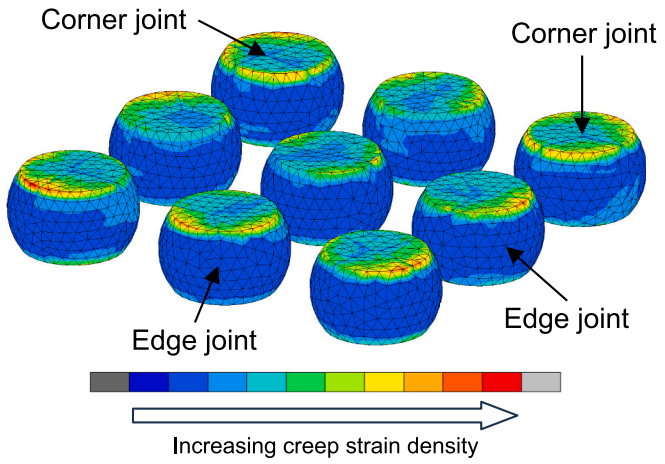

Fig. 8. Overview of CSED in solder joints from sample product.

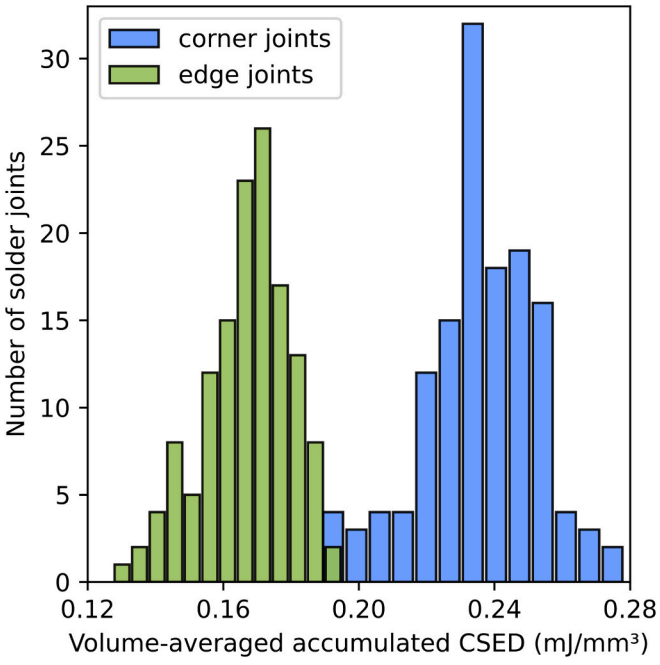

Fig. 9. Histogram of CSED of corner and edge joints from sample products.

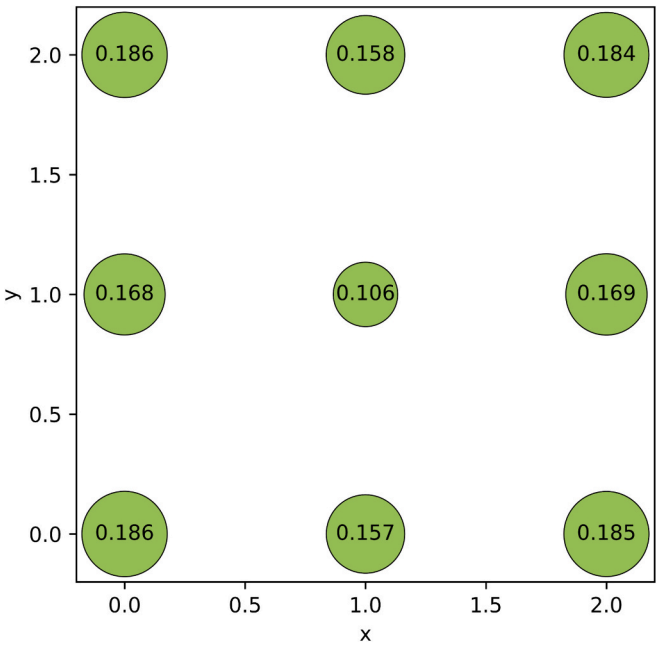

Fig. 10. Bubble plot representing the accumulated CSED in each joint of the WLCSP model.

perpendicular to the PCB. In a separate simulation run, the edge joints were fitted with the most critical orientation while the corner joints had the least critical orientation. The extracted CSED for each solder joint in this sample product is visualized as a bubble plot (in which each bubble represents a solder joint) in Fig. 10. It can be noted that the CSED values for the edge joints do not exceed those of the corner joints. Thus, a solder joint's location within the package has a higher influence than its grain morphology, on its creep response. This observation might however not hold up for larger solder joint arrays. In the current 3×3 setup, the difference in relative distance from the neutral point between adjacent joints is significant. WLSCP packages typically feature solder joint arrays with between 2 and 12 solder joints per side. For a larger array, the

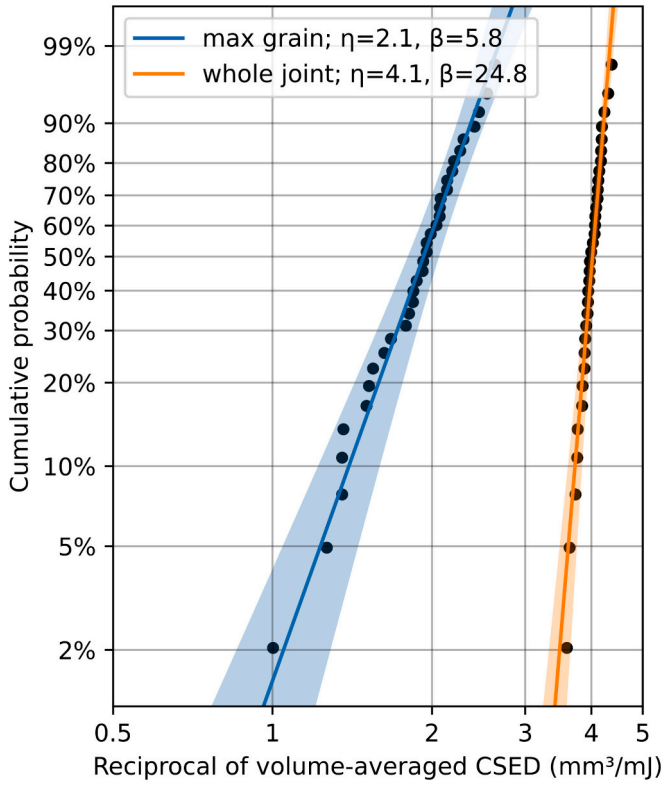

Fig. 11. Weibull probability plot of grains with maximum CSED in each sample product. The shaded region represents the 95 % confidence interval.

difference in distance to the neutral point will become smaller for adjacent joints. Therefore, the effect of the solder joint's location within the array should diminish. As a consequence, the effect of the grain morphology on the creep response might become dominant over the effect of location.

The statistical distribution of the volume-averaged CSED within the 34 simulated products is an important aspect in comparing the results with experimental data. The fatigue life of the solder joints is assumed to be inversely related to accumulated CSED, $N_f = C/\Delta W$, where C is an empirical constant, and ΔW is the volume-averaged CSED per thermal cycle. The computed data for ΔW is used in a Weibull analysis, which is the de facto standard in reliability engineering to model lifetime distributions [42]. In a Weibull analysis the cumulative density function ('unreliability') is defined as,

$$F(N_f) = 1 - exp\left[-(N_f/\eta)^{\beta}\right], \tag{9}$$

where β is the shape parameter, and η is the scale parameter. The scale parameter, also known as the characteristic life, is the number of cycles at which 63.2 % of the samples have failed [43]. The shape parameter is a measure of the uniformity of the distribution, and corresponds to the slope of the fit. The computed data points are converted into cumulative probability using, $(i\text{-}0.3)/(n + 0.4)$, where i is the rank of the data points and n is the total number of observations (34 in this case). Fig. 11 shows the Weibull plots of both the maximum volume-averaged CSED across the whole solder joint as well as across the grains with highest CSED for each of the 34 products. The Weibull slope for the volume-averaged CSED across the whole solder joint equal 24.8, revealing only a limited spread in the computed results. The factor between the computed value for the worst and best performing case is approximately 1.5, which is much lower than found in experiment. This factor is also lower than for the single joint simulations because the performance on a product level is a combination of all its solder joints. The Weibull slope for the volume-averaged CSED across the grains reveals a slope of 5.8, which does align with the reported experimental values of ~3.4–6.7 for similar thermal cycling experiments [44]. A higher Weibull slope means there is a lower spread in the distribution. Therefore, it is logical that a real-life reliability test results in a lower β than for the simulated distribution, since a real-life test has a higher number of factors influencing the possible outcome and thus increasing the spread in results. This indicates that an eventual fatigue crack is expected to nucleate in proximity of this most critical grain. Consequently, the volume-averaged CSED per grain might be a better metric than the volume-averaged CSED per solder joint to statistically analyze the computed results. A full analysis including a damage model for the material is required to draw a definite conclusion.

5. Conclusions

In conclusion, this study aimed to develop a microstructure-based Finite Element (FE) modeling technique to evaluate the fatigue life of solder joints in microelectronics. The developed technique employed 3D Voronoi tessellation to generate solder joints with random microstructures featuring β − Sn grains and grain boundaries. The anisotropic behavior of the β − Sn grains was described by the Garofalo-Hill creep model, while the grain boundaries were implemented as interface elements with an isotropic creep constitutive model. The qualitative estimation of stochastic variability introduced by microstructural differences in the creep response of solder joints was conducted. The study involved the generation of approximately 100 unique solder joints with 5 to 9 grains each, subjected to realistic stress levels during thermal cycling. The volume-averaged creep strain energy density was used to assess the fatigue life of the solder joints, revealing a factor of ~4 difference in expected lifetimes. Further investigations included the generation of 32 sample products mimicking a Wafer-Level Chip-Scale package (WLCSP), incorporating nine randomly chosen solder joints from the pool. The computed creep strain energy density indicated a factor ~ 2.5 between the highest and lowest estimates for solder joint life. A Weibull plot generated from the results of all 34 products showed a slope of 5.8, falling within the typical range reported for thermal cycling experiments. The study emphasized the importance of considering the microstructural variability of solder joints in predicting their fatigue life, departing from the industry's common use of homogenized isotropic constitutive models. The developed modeling technique allowed for a statistical analysis of the impact of grain anisotropy on solder joint reliability. Overall, this work contributes valuable insights into the complexity of solder joint behavior under cyclic mechanical stresses, paving the way for more accurate and reliable simulations in microelectronics reliability assessments.

Declaration of competing interest

The authors whose names are listed immediately below report the following details of affiliation or involvement in an organization or entity with a financial or non-financial interest in the subject matter or materials discussed in this manuscript.

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Data availability

No data was used for the research described in the article.

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