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Application of 1.7-kV 700-A SiC LinPak to Optimize LCL Grid-Tied Converters

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***Abstract*—The current rating of SiC MOSFETs has been increased ever since its introduction. Yet, high current modules for 690-V and beyond grid applications, which would enable the realization of megawatt range converters, are not readily commercially available. Recently, a new high current 1.7-kV SiC MOSFET module suitable for hard-parallel connection to increase the current rating has been introduced. This paper investigates the system-level benefit of this module for a 2-level 690-V 1-MW grid-tied converter regarding achievable efficiency and power density and benchmarks the results against the achievable performance with conventional Si IGBTs. The study analyzes in detail the impact of the number of paralleled modules, the choice of the cooling system and the filter design.**

***Index Terms*—Grid-tied converter, paralleling, cooling, SiC MOSFET.**

I. Introduction

In power electronic systems, as the power rating increases, the power density of the total system typically increases while the cost per watt is reduced. For example, the cost per watt of megawatt range central solar inverters is about twice lower when compared with string inverters with power capability below 100 kW [1]. To increase the power rating of the system above certain levels, paralleling of components is essential [2]. Paralleling concepts can be employed on different levels of the power circuit, i.e. from paralleling of individual modules up to paralleling of entire power electronic building blocks (PEBBs).

The low switching losses are the most attractive feature of SiC-based semiconductor devices among others. This feature is particularly beneficial for grid-tied converters where a harmonic filter is often the bulkiest and heaviest component [3]-[6]. With higher switching frequency operation enabled by the SiC device technology, the power density of a grid-tied converter can be significantly improved by reducing filter requirements. However, the application of SiC devices is so far restricted to low power applications because of the poor availability of high current rated power modules. Typically, a three-phase voltage source converter (VSC) can be built up to 200 ~ 300 kW by using a single 300-A half-bridge module per phase in the range of 900-V ~ 1.7-kV. When it comes to high power megawatt converters, paralleling of the modules becomes inevitable. However, currently available SiC modules are often not dedicated for hard-paralleling. There, the design of the terminals and the mechanical structure often results in non-matched parasitic impedances from the dc busbar and ac terminals which results in noticeable static and dynamic current imbalance.

Recently, a new high current SiC MOSFET module has been introduced [7] that is suitable for hard-parallel operation to increase the current rating. This paper investigates the potential of this power module towards the implementation of a 690-V 1-MW grid-tied 2-level converter. The achievable efficiency and power density is investigated and benchmarked against the same converter using conventional Si IGBTs. The study takes into account different numbers of hard-paralleled modules, the cooling system performance and the degrees of freedom related to the LCL filter design.

II. Paralleling of 1.7-kV SiC LinPak

A. ABB SiC LinPak

The high current SiC MOSFET half-bridge module investigated in this paper has been reported in 2016 [7]. It is based on the 140×100 mm^2 new open standard module, also known as LinPak from ABB [8],[9], nHPD2 from Hitachi [10] and XHP™ from Infineon [11]. The mechanical configuration and the terminals of the LinPak are optimized for the paralleling of modules for easy

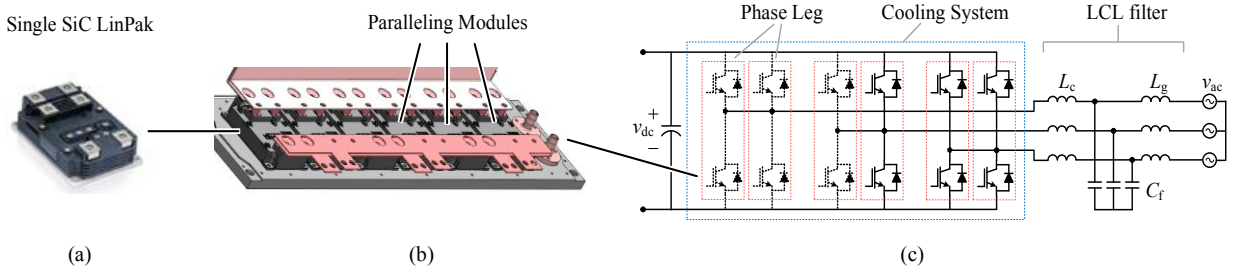
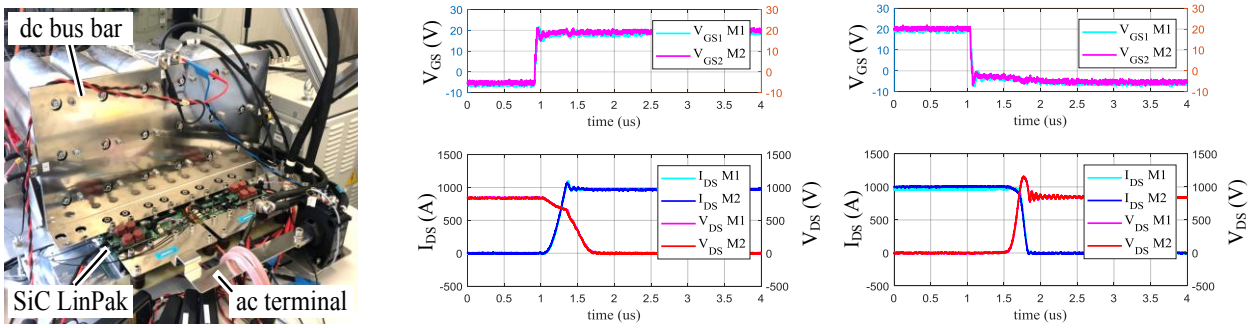
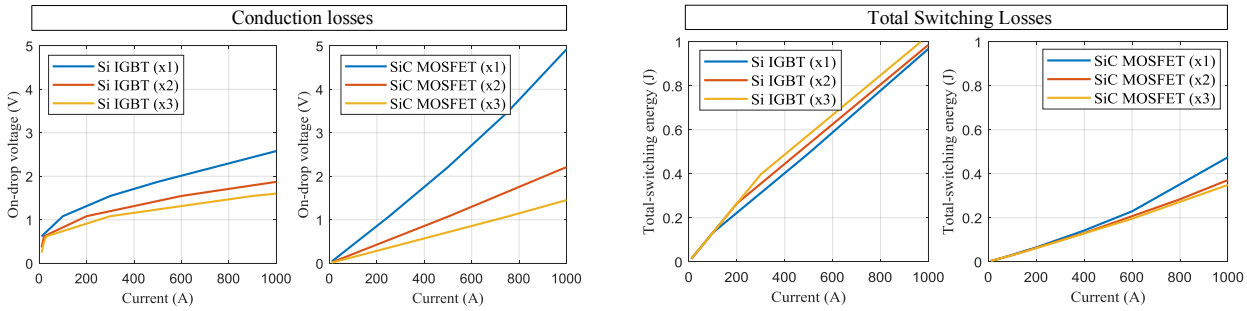


Fig. 1. Application of 1.7-kV 700-A SiC MOSFET-based LinPak module on a 690-V 1-MW grid-tied converter. (a) LinPak module. (b) Power electronics building block with two hard-parallel-connected LinPaks. (c) Grid-tied converter with LCL filter.



(a) (b) (c)

Fig. 2. Experimental results with parallel-connected SiC LinPak. (a) 1-MW power electronic building block. (b) Turn-ON and (c) turn-OFF waveforms with two LinPaks in parallel.



(a) (b)

Fig. 3. Power loss comparison between Si and SiC 1.7-kV LinPaks as a function of the number of paralleled modules. (a) Conduction losses with junction temperature T_j = 125°C. (b) Total switching losses including turn-ON, turn-OFF, and reverse recovery losses with 900-V dc link.

scaling up of the power ratings as shown in **Fig. 1**. Furthermore, it has a low stray inductance of about 10 nH [7] which enables a fast switching switching transient without high turn-off over-voltages [7]. In addition, the same package is already available with conventional Si IGBTs which allows for a low cost production and easy snap-in installation of the SiC LinPak version with only small modification in the existing PEBB.

B. Paralleling of LinPak

Fig. 2(a) shows the a 1-MW PEBB based on parallel-connected 1.7-kV SiC LinPaks. The switching waveforms for 2×1000 A and 900 V are given in **Figs. 2(b)** and **2(c)**. To keep the parameter variations within tolerable limits, modules with chips from the same manufacturing lot were used. Here, a passive balancing scheme which has been widely used for paralleling of IGBTs is adopted: a common-mode choke and a resistor in the gate return path is included in the gate driver amplification stage, which render the gate signals more robust towards differences in the individual switching transitions [12], [13]. A current imbalance below 10% was achieved, thereby both switching losses and conduction losses imbalances are also below 10% on average. This allows paralleling of LinPak without significant current derating. For the remainder of the paper, ideal sharing is assumed for the sake of the analysis.

Fig. 3(a) shows the impact of the number of paralleled modules, $N_{parallel}$, on the on-state voltage drop of the Si IGBT-based and the SiC MOSFET-based LinPak. Because of the ohmic characteristic of the MOSFET, the on-state voltage drop of the SiC LinPak is inversely proportional to $N_{parallel}$. In contrast, this effect is much less pronounced for the Si IGBT due to the constant voltage drop of the pn junction. The crossover point where the voltage drop of SiC becomes higher than that of IGBT is 400 A with $N_{parallel}$ = 1 and 800 A with $N_{parallel}$ = 2. In other words, the SiC enables lower conduction losses when the total current is lower than 800 A and $N_{parallel}$ = 2. As shown in **Fig. 3(b)**, the total switching losses of the SiC LinPak is reduced by a factor of ~3 compared to the Si LinPak. This finding is largely independent from $N_{parallel}$.

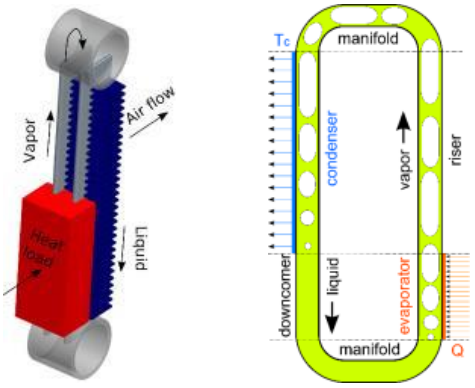
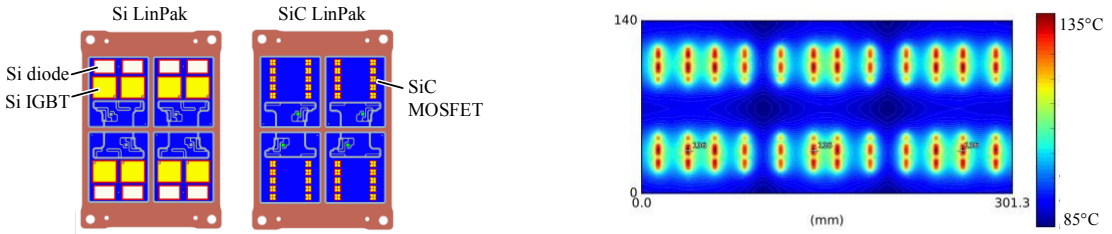


Fig. 4. Working principle of ABB two-phase thermosiphon [15].



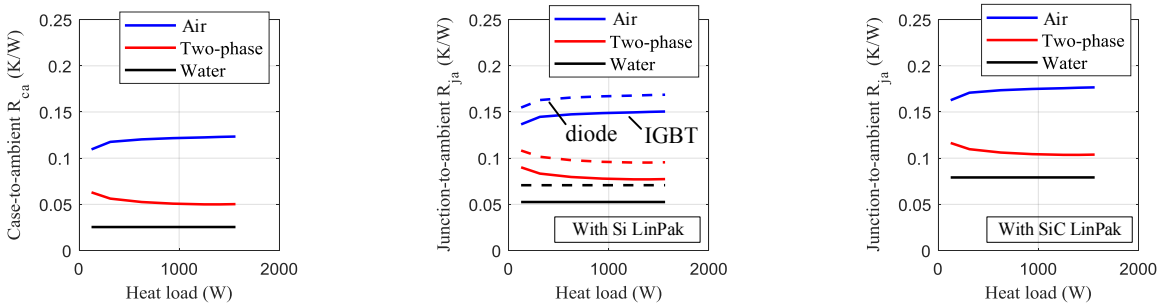
(a) (b)

Fig. 5. (a) Comparison of the chip size between the Si and SiC LinPak. (b) Cooling system simulation with 3 SiC LinPaks in parallel assuming a two-phase thermosiphon with 6200-W heat load. The thermal cross-coupling between two adjacent switches is negligible. (ambient temperature T_a = 50°C)

TABLE I

COOLING SYSTEM PERFORMANCE FOR A SINGLE MODULE WITH 2.5 KW HEAT LOAD; LINEARLY SCALABLE WITH $N_{PARALLEL}$

Cooling system type	Size (mm^3)	Convection type	Mass flow (m^3/hr)	Weight (kg)	Junction-to-ambient R_{th} (K/W)
Air (aluminum heat sink)	100 × 140 × 125	Air-forced convection	408	3.3 (without fan)	0.176
Two-phase thermosiphon	100 × 450 × 30	Air-forced convection	408	1.4 (without fan)	0.104
Water (copper cold plate)	100 × 140 × 4	Water-forced convection	0.525	1 (without pump)	0.080



(a) (b) (c)

Fig. 6. Simulated cooling system performance for a single module. (a) Case-to-ambient thermal resistance of the cooling system. Junction-to-ambient thermal resistance (b) with Si LinPak and (c) with SiC LinPak. In (b), the smaller diode chip size explains its higher thermal resistance when compared to the IGBT .

III. COOLING SYSTEM FOR THE LINPAK

A. Cooling System for High Power Converter

Heatsink cooling with natural or forced air convection is the most popular choice in low power systems. However, heatsink cooling is limited by two factors: the heat conduction from the base to the top of the fins (up to 10 cm for high aspect ratio heatsinks), and the heat transfer coefficient to the air (typically 50 W/m^{2}K). Water cooling overcomes these limitations by using low aspect ratio fins (a few millimetres) and having a very high transfer coefficient (typically 5000 W/m^{2}K). Two-phase cooling is another way of overcoming these limitations: the phase-change inside the thermosiphon yields an equivalent thermal conductivity 100 times that of pure aluminium while the use of louvered folded fins on the air side produces a heat transfer coefficient of up to 150 W/m^{2}K, three times that of the standard heat sink [14].

The presented study aims at investigating the system level impact of using a standard air cooling heatsink, a water cooling plate or a passive two-phase cooling system such as a thermosiphon shown in **Fig. 4**.

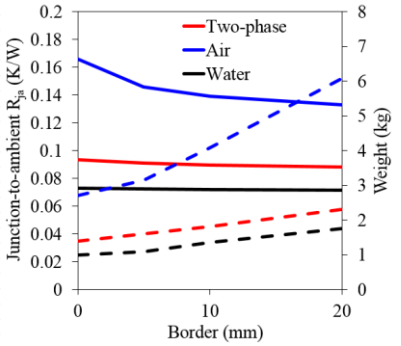


Fig 7. Evolution of the thermal resistance (solid lines) and weight (dashed lines) as the cooler base plate size is increased beyond the footprint of module borders.

B. Design of ABB Two-Phase Thermosiphon

ABB has developed an in-house Python solver to predict the performances of such two-phase coolers [16]. The basic problem in power electronics cooling is to predict the temperature rise from the coolant to the die. From the die

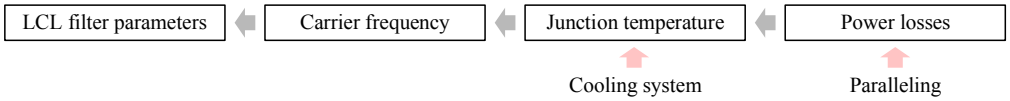


Fig. 8. Impact of the cooling system and the paralleling of semiconductors on the LCL filter parameters.

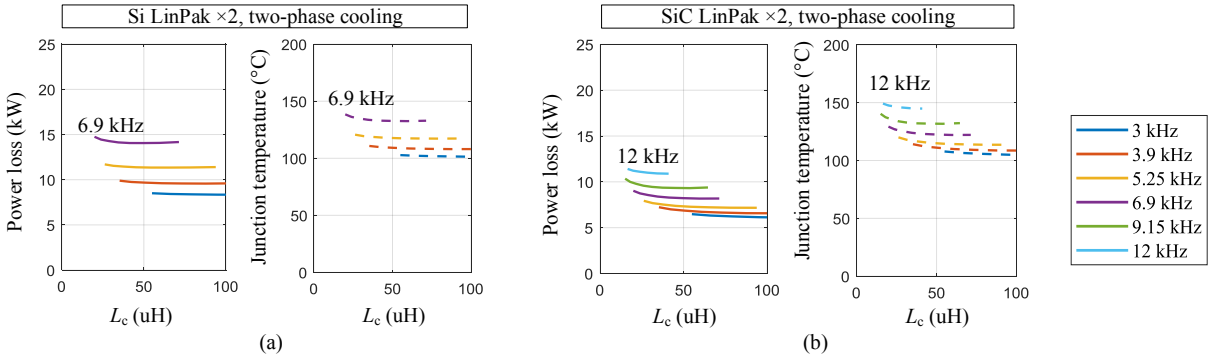


Fig. 9. Comparison of the maximum achievable f_{ca} between Si and SiC LinPak for the 1-MW system shown in **Fig. 1(c)** with T_a = 50°C and $T_{j,max}$ = 150°C; the x-axis represents the converter-side inductance of the LCL filter which was obtained based on [3].

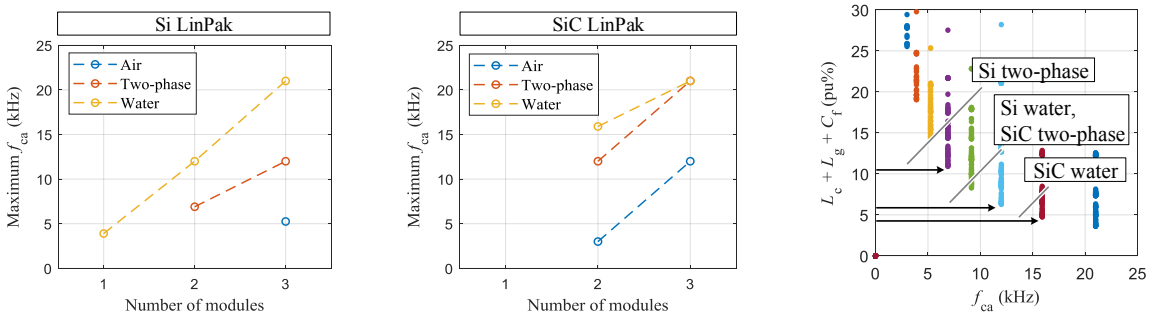


Fig. 10. Maximum achievable f_{ca} as a function of the number of paralleled modules and the choice of the cooling system for (a) Si and (b) SiC LinPak; f_{ca} sweep range = 3…21 kHz. The maximum f_{ca} of SiC is limited by the sweep range for $N_{parallel}$ = 3. (c) Minimum LCL filter requirements for Si and SiC, varying cooling systems and $N_{parallel}$ = 2.

to the coolant, multiple layers of more or less thermally conductive materials are present to ensure sufficient heat spreading in addition to electrical functions (metallization, substrate, solder, baseplate). This heat spreading is usually predicted with numerical simulations. Such a method was implemented using FiPy [17], an object oriented, partial differential equation (PDE) solver, written in Python, which has been developed at the National Institute of Standards and Technology (NIST). It becomes particularly handy when one needs to couple the output of a first python simulation yielding boundary conditions to a PDE solver to execute automated sweep simulations and post-processing.

The motivation to couple a 3D heat spreading simulation to ABB in-house two-phase flow solver is that the boiling heat transfer coefficient is strongly dependent on the local heat flux, vapor quality and fluid velocity in the evaporator channels. These dependences will affect the heat spreading and in turn change the local boiling heat transfer coefficient, so that this problem can be solely solved iteratively.

C. Impact of the Cooling System Choice

Fig 5 (a) shows the different chip layouts for the Si and SiC LinPak. The SiC chips are much smaller so that the total chip area is 2.5 times smaller and the heat flux density is proportionally larger. If the allowed maximum junction temperature of the SiC is kept at the same value as Si, this means that a better cooling system or heat spreading are needed for the SiC module at constant heat losses. **Fig. 5(b)** shows the simulated temperature map at the die level for 3 modules with two-phase cooling. There is thermal cross-coupling between the chips of the same switch position, i.e. high-side or low-side switch, but not significant one in between the switch positions nor in between modules.

Table I shows the characteristics of the three different cooling systems considered in the simulations. **Fig. 6(a)** shows the case-to-ambient thermal resistance as a function of the heat load. **Figs. 6(b)** and **6(c)** show the junction-to-ambient thermal resistance as a function of the heat load for Si- and SiC-based LinPaks, respectively. While traditional air cooling with a heatsink is restricted to high

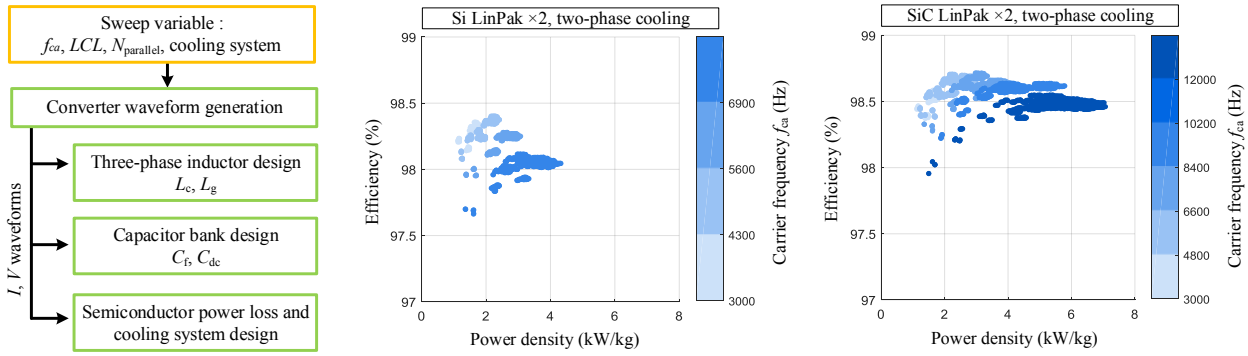


Fig. 11. (a) Total system design routine. Achievable efficiency-power density performance space of the 1-MW grid-tied converter with (b) Si LinPak and (c) SiC LinPak where two-phase cooling and $N_{parallel} = 2$ was assumed.

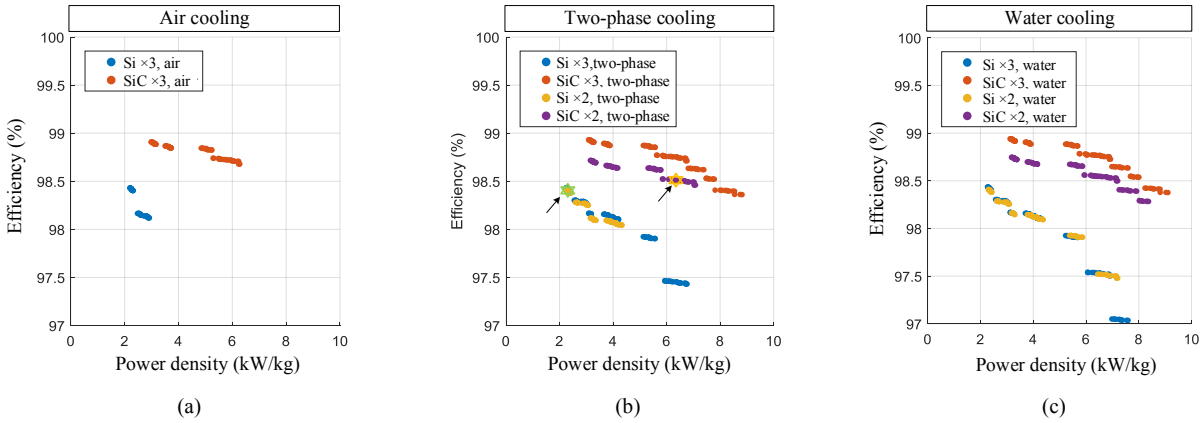


Fig. 12. Impact of the number of modules, the cooling system, and the selection of either Si or SiC on the efficiency-power density Pareto front. (a) Air cooling. (b) Two-phase cooling. (c) Water cooling. The arrows indicate the systems shown in Table II and Fig. 13.

thermal resistances, the two-phase thermosiphon allows to still use air cooling but yields a thermal resistance and weight close to that of water cooling.

Fig. 7 shows the evolution of the thermal resistance and weight as the cooler base plate size is increased beyond the module borders. Increasing the size of the heat sink significantly decreases its thermal resistance due to better heat spreading, but at the cost of an exponential weight increase, while for the two-phase and water coolers the weight increase is linear, but the thermal resistance gain is modest because of negligible additional heat spreading. For the remeinder of the paper, therefore, the same size of the cooler base plate size with the module border is used.

IV. Maximum Achievable Carrier Frequency

The power density of a grid-tied converter is typically dominated by the LCL filter size which in turn is highly affected by the carrier frequency f_{ca} of the pulse width modulation (PWM). As shown in **Fig. 8**, for the same power rating, the maximum achievable f_{ca} is limited by the maximum allowed semiconductor junction temperature which is determined by its power loss. Then, the power loss of the semiconductor and the junction temperature is determined by the cooling system and the number of parallel-connected modules, respectively. The following sections will quantitatively analyze the above described set of dependencies for the system at hand.

A. LCL Filter Parameters

When PWM is used for the grid-tied converter, the voltage harmonics appear at multiples of the carrier frequency f_{ca} which in turn causes harmonics in the grid-side current i_g. The LCL filter parameters (L_c, L_g, C_f) must be designed to comply with relevant harmonics standards, e.g. IEEE519 (0.3% of the rated current for harmonic orders > 35). The LCL filter attenuation Att_{req} [5]

$$Att_{req} \approx \frac{1}{L_c L_g C_f \omega_{h.sw}^{\ 3}} = \frac{1}{\left(\frac{L_c}{k}\right)\left(\frac{L_g}{k}\right)\left(\frac{C_f}{k}\right)\left(k\omega_{h.sw}\right)^3} \quad (1)$$

must be designed so as to sufficiently suppress the first group of voltage harmonics located at the harmonic angular frequency $\omega_{h,sw}$ ($\approx 2\pi f_{ca}$). It is noted that when the $\omega_{h.sw}$ increases k times, the LCL parameters decreases roughly by the factor of k.

B. Maximum Achievable Carrier Frequency

Although the filter requirement can be reduced with higher f_{ca} as described in (1), the maximum allowed f_{ca} is

TABLE II
COMPARISON OF SI AND SIC-BASED GRID-TIED CONVERTER WITH SAME EFFICIENCY

	Si	SiC
Carrier frequency f_{ca} (kHz)	3.9	12
Converter-side inductor L_c (uH)	105	20
Filter capacitor C_f (uF)	780	445
Grid-side inductor L_g (uH)	42	14
Total weight of system (kg)	425	141
Efficiency (%)	98.4	98.5

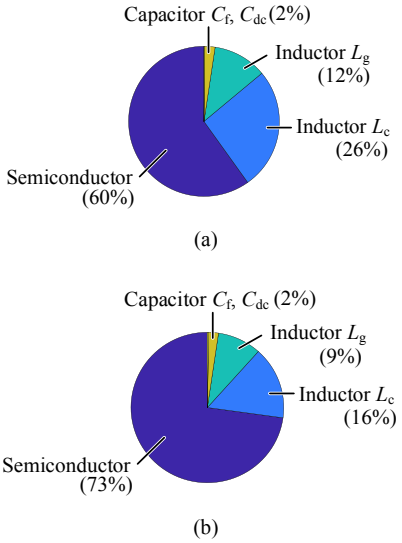


Fig. 13. Power loss breakdown for the two candidate systems highlighted in **Fig. 12(b)** with same efficiency of ~98.5% (a) 3.9-kHz Si-based and (b) 12-kHz SiC-based system.

restricted by the maximum power loss capability of the module which is determined by the cooling performance. In order to find the maximum f_{ca}, the power losses and the corresponding junction temperatures T_j are calculated as a function of f_{ca} and the cooling system from Section III as shown in **Fig. 9**. If two-phase cooling and two paralleled LinPaks is considered, the maximum achievable f_{ca} for Si and SiC with a maximum permissible junction temperature of $T_{j,max}$=150°C, is 6.9 kHz and 12 kHz, respectively. The maximum power loss dissipation of the Si LinPak is about 25% higher than the value for the SiC LinPak.

Figs. 10(a) and **10(b)** show a comparison between the maximum achievable f_{ca} for Si and SiC LinPak as a function of $N_{parallel}$ and the cooling system. Generally, the higher $N_{parallel}$, the higher the maximum f_{ca}. Note that for the target power of 1MW, the minimum $N_{parallel}$ for SiC LinPak is 2 while it is 1 for Si. **Fig. 10(c)** shows the minimum LCL parameter requirement between Si and SiC LinPak according to the cooling system. It is remarkable that the maximum f_{ca} for Si LinPak with the water cooling is similar to SiC LinPak with the two-phase cooling when $N_{parallel}$ = 2.

V. SYSTEM-LEVEL PARETO OPTIMIZATION

A. Optimization Routine

The system-level optimization routine shown in **Fig. 11(a)** is carried out with the following specifications: $v_{ac,line\text{-}to\text{-}line}$ = 690 V_{rms}, v_{dc} = 1100 V, rated power = 1 MW, f_{ca} = 3…21 kHz, $N_{parallel}$ = 1…3, maximum junction temperature = 150°C. The analysis includes the semiconductors, the cooling system, the LCL filter and the dc link capacitors. The generated LCL filter parameter values satisfy IEEE519. First, the waveforms are calculated. Then, the semiconductor power loss calculation in association with a cooling system and designs of all passive components are carried out [4],[5].

Three-phase inductors are considered for the implementation of the LCL filter. The winding losses are calculated based on 2D field approximations considering the fringing field of the air gap. The core losses are calculated using the improved Steinmetz equation (iGSE). Once the power losses of the inductors are calculated, a detailed thermal model is used to estimate the temperature distribution. The optimization algorithm searches the 5-D parameter space and calculates the inductances, flux density, power losses, and temperature of each design candidate. Then the minimum weight design is selected amongst those satisfying the maximum temperature constraint [5].

The capacitor bank optimization selects weight-optimal series-parallel connections of different capacitors so as to satisfy the target capacitance and lifetime (> 200 khrs) [4].

B. Analysis

Figs. 11(b) and **11(c)** shows the achievable efficiency vs. power density performance space for the Si- and SiC-based grid-tied 2-level converter of **Fig. 1(c)** with two-phase cooling and $N_{parallel}$ = 2. Even though the cooling performance of the SiC LinPak is lower when compared to the Si-based counterpart as discussed in Section IV, the higher achievable f_{ca} of SiC allows for a higher power density. The maximum power density of the Si- and SiC-based converters is 4.3 kW/kg and 7.2 kW/kg, respectively, while 20% lower total losses can be achieved with the SiC-based design.

Fig. 12 shows the impact of $N_{parallel}$ and the cooling system on the Pareto-front of the target system. If air cooling is used, the minimum $N_{parallel}$ for 1-MW system is 3 in accordance with **Fig. 10**. Two-phase cooling or water cooling is required to build the system by using 2 LinPaks in parallel. When $N_{parallel}$ is increased to 3, the efficiency of SiC-based converter is increased because of the ohmic characteristic of MOSFET, while the IGBT-based system improves only marginally.

Table II provides detailed information on two candidate designs for the Si- and SiC-based grid-tied converter with two-phase cooling and $N_{parallel}$ = 2. Both systems achieve a similar efficiency of ~98.5% as indicated in **Fig 12(b)**. For the selection of candidate systems at hand, a 3 times higher f_{ca} can be employed with the SiC LinPak, resulting in a 3 times higher power density**.** It is noted that the calculated power density only considers the weight of the analyzed components while neglecting additional weight from other

parts such as the mechanical housing, circuitry for protection, startup, and auxiliaries. **Fig. 13** shows the power loss breakdown of the selected designs in **Table II**. It is worth noting that the semiconductor loss of the SiC-based converter is higher compared to that of the Si-based counterpart under the same total power loss. That is, the selection of the cooling system becomes more important with SiC when the optimization target is to maximize power density.

VI. Concluding Remarks

The 1.7-kV 700-A SiC LinPak can reduce the switching losses over Si-counterpart by factor 3 and good dynamic current balancing can be achieved based on passive balancing scheme. Owing to the smaller total installed chip size, the SiC LinPak has a higher thermal resistance compared with Si LinPak which renders the cooling more challenging.

The optimization of a 1-MW grid-tied 2-level converter shows that for a similar efficiency of ~98.5%, about 3 times higher f_{ca} can be used with SiC-LinPak. When considering only the weight of the main power electronic components, 3 times higher power density can be achieved with the SiC LinPak for a maximum T_j of 150°C.

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