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5-Level Packed U-Cell (PUC5) Active Front-End Rectifier

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ABSTRACT This article presents the 5-level Packed U-Cell (PUC5) converter as an active front-end (AFE) rectifier designed to achieve high power quality and power factor correction (PFC) in grid-connected applications. Operating in boost mode, the proposed topology significantly mitigates input current harmonics and enables precise regulation of the DC output voltage, making it well-suited for bidirectional DC systems such as electric vehicle (EV) charging infrastructure with Vehicle-to-Grid (V2G) capability. A detailed analysis of the converter's switching states is conducted, with a focus on identifying redundant states that can be strategically utilized to balance the voltage of the auxiliary capacitor. This balancing is essential to sustain the five-level voltage waveform at the rectifier input, which in turn minimizes voltage distortion and directly reduces current harmonic content. The output voltage is tightly regulated to supply downstream DC loads with high stability. Experimental validation confirms the effectiveness of the proposed PUC5 rectifier, demonstrating its ability to operate with a near-unity power factor while drawing low-distortion current from the AC grid and maintaining robust dynamic performance under varying load conditions.

INDEX TERMS Active front-end rectifier, PUC5, electric vehicle, battery charger, power quality.

I. INTRODUCTION

A significant development in the electric vehicle (EV) industry led to many green cars on the roads. The more EVs are driven, the more battery chargers are needed [1], [2]. Nowadays, multilevel power converters are seen in the product list of electrical manufacturing companies, which assures their acceptable performance in power system applications [3], [4]. A basic example of a multilevel rectifier could be the full bridge that generates a 3-level voltage waveform using the unidirectional PWM technique. With some modification to the full bridge rectifier, such as adding a path between legs or creating a neutral point by splitting the DC capacitors, some 5-level topologies have been reported in the literature [5], [6], [7]. The main limitation in those configurations is the middle point of the DC capacitors, which is a neutral point that should be balanced accurately to divide the voltage between two capacitors identically. The same issue is still an essential matter of research in Neutral Point Clamped (NPC) rectifier [8]. However, space vector modulation is a practical solution in balancing the neutral point voltage of 3-phase NPC converters using redundant switching states [9].

Researchers have also introduced different multilevel topologies, which are mainly inverters with too many isolated DC supplies. Such topologies are complex to employ in rectifier mode due to having multiple output terminals, bringing further problems.

Cascaded H-bridge (CHB) rectifier is the most popular one which many researchers study to develop effective voltage regulation techniques in order to balance each cell voltage acceptably [10], [11], [12]. Moreover, another limitation of such multiple output configuration is the power-sharing between individual cells, as illustrated and investigated in details [13].

The PUC5 topology has been introduced as a single-dc-source inverter in 2016 [14]. As illustrated in Fig. 1, it employs only 6 active switches to synthesize a five-level output voltage waveform. A key advantage of this structure lies in the presence of redundant switching states, which are exploited to achieve effective voltage-balancing of the DC-link capacitor voltages. The PUC5 rectifier is designed to operate in boost mode, enabling unity power factor operation while significantly mitigating input current harmonics. This capability is primarily attributed to the high-quality multi-level voltage waveform generated at the AC side, which leads to a

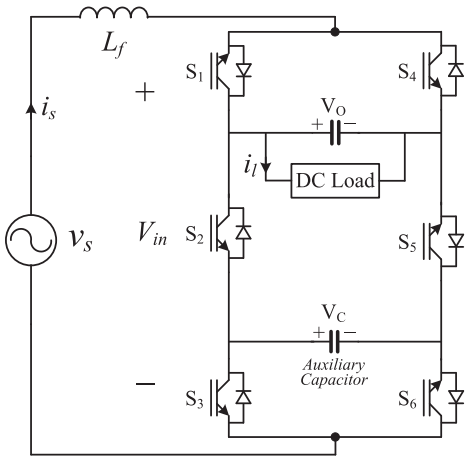

FIGURE 1. PUC5 rectifier.

lower Total Harmonic Distortion (THD) in the input current. Consequently, the required size of the input inductive filter is substantially reduced compared to conventional two-level rectifiers, contributing to a more compact overall system design. An important feature of the PUC5 rectifier is that its control structure remains equivalent to that of a conventional full-bridge rectifier with a single DC output, owing to the voltage balancing of the auxiliary capacitor through appropriate redundant state selection. Therefore, the current and voltage regulation can be achieved using a standard cascaded PI controller architecture, eliminating the need for complex balancing control algorithms [15].

PUC5 rectifier topology, switching states, and voltage balancing algorithm are analyzed in Section II. A standard cascaded controller is implemented and discussed in Section III. Finally, experimental tests and verifications are done, and results are shown and discussed in Section IV.

II. PUC5 RECTIFIER

A. CONFIGURATION AND SWITCHING STATES

As illustrated in Fig. 1, the PUC5 rectifier has two DC links. The upper capacitor is the main DC link that should be voltage-regulated to supply the DC load. The lower one is an auxiliary capacitor with half the voltage amplitude of the main terminal (V_O). It aims to form the rectifier input voltage (V_{in}) as a 5-level quasi-sine wave. Therefore, $V_C = E$, $V_O = 2E$, and the 5 voltage levels include 0, $\pm E$, $\pm 2E$. It should be mentioned that it differs from the modified PUC rectifier discussed in [13], where both DC links should have equal voltages and be connected to two isolated loads.

The output DC voltage should be more than the input AC peak value to have a boost rectifier.

$$V_{S-rms} = 120\ V \ \rightarrow \ V_{S-peak} = 120\sqrt{2} = \ 170V$$

Based on the peak value of the AC grid, the DC voltage is selected at 200 V so:

$$V_O = 200\ V \ \rightarrow \ V_C = 100\ V$$

TABLE 1. PUC5 Rectifier Switching States

Switching State	S_1	S_2	S_3	V_{in}	V_{in} voltage levels
1	1	0	0	V_O	+200V
2	1	0	1	V_O-V_C	+100V
3	1	1	0	V_C	+100V
4	1	1	1	0	0V
5	0	0	0	0	0V
6	0	0	1	-V_C	–100V
7	0	1	0	-V_O+V_C	–100V
8	0	1	1	-V_O	–200V

That means the output terminal voltage V_O should be regulated at 200 V to feed the DC load, which could be a battery or a DC bus in a hybrid energy hub. Moreover, the auxiliary capacitor voltage V_C must be balanced at 100 V to properly generate a 5-level voltage waveform of V_{in}.

Based on the above-selected voltages, the two upper switches, S_1&S_4 withstand 200 V. The other 4 switches, S_2, S_3, S_5, and S_6, see only half level, which is 100 V.

All switching states of the PUC5 rectifier have been listed in Table 1. Note that each pair of S_1-S_4, S_2-S_5, and S_3-S_6 is complimentary.

It is seen that based on each combination of switches, a path is provided to flow the current through the rectifier, and consequently, the corresponding voltage level appears at the input that together forms the 5-level voltage waveform. Such smooth waveform has lower THD and directly affects the AC current harmonic contents. The naturally reduced amount of THD results in a smaller filter in the AC line with acceptable performance compared to the larger ones in 2-level converters.

B. VOLTAGE BALANCING DESIGN

Table 1 reveals several redundant switching states. Those states and their effect on capacitor voltage balancing have been meticulously studied in [16]. Given that an external PI controller regulates the primary output voltage V_O, these redundancies serve two key purposes: (1) they assist in minimizing the regulation error of V_O, thereby alleviating the control effort required from the external controller, and (2) they facilitate balancing the auxiliary capacitor voltage V_C, which is essential to maintain five uniform voltage levels at the input. To illustrate their role in voltage balancing, switching states 2 and 3 are highlighted with red lines in Fig. 2. The polarities of the DC links are defined as shown. Depending on the direction of the current, these states either charge or discharge the capacitors. For instance, in state 2 with positive current flow, the upper capacitor charges while the lower one discharges due to its reversed polarity. Consequently, V_O increases, and V_C decreases. In contrast, in state 3 under the same current condition, the lower capacitor charges. Reversing the current direction inverts these effects. Additionally, it should be noted that when the load is disconnected from the AC source, V_O naturally decreases due to discharging.

Analyzing all switching states in a similar manner provides critical insights for designing an effective voltage balancing

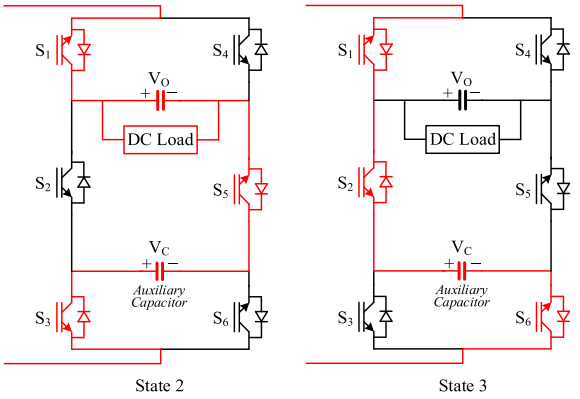

FIGURE 2. Connected path through switching states 2 and 3 to study the voltage balancing effects.

TABLE 2. Effects of Switching States on DC Capacitors

Switching State	Line Current Sign	V_{in}	Effect on V_O	Effect on V_C
1	$i_s > 0$	V_O	Charging	Discharging
2	$i_s > 0$	V_O-V_C	Charging	Discharging
2	$i_s < 0$	V_O-V_C	Discharging	Charging
3	$i_s > 0$	V_C	Discharging	Charging
3	$i_s < 0$	V_C	Discharging	Discharging
4	$i_s \geq 0$	0	Discharging	Discharging
5	$i_s \leq 0$	0	Discharging	Discharging
6	$i_s > 0$	-V_C	Discharging	Discharging
6	$i_s < 0$	-V_C	Discharging	Charging
7	$i_s > 0$	-V_O+V_C	Discharging	Charging
7	$i_s < 0$	-V_O+V_C	Charging	Discharging
8	$i_s < 0$	-V_O	Charging	Discharging

algorithm. The detailed impact of each switching state on the DC link voltages is summarized in Table 2.

Given that the proposed PUC5 rectifier operates in a grid-connected configuration, the system inherently includes a current sensing mechanism as part of the grid current control loop. Leveraging this existing sensor infrastructure, the voltage balancing strategy is designed to avoid the addition of extra current sensors, thereby minimizing cost and system complexity. Specifically, the same line current sensor used for grid current control is repurposed to support the voltage balancing algorithm, eliminating the need for redundant sensing hardware. The voltage balancing method utilizes feedback from two DC voltage sensors, which measure the voltages across the upper and lower DC-link capacitors. These measurements provide real-time information about the capacitor voltage deviations from their nominal values. Based on this feedback, a modified multi-carrier pulse width modulation (PWM) scheme is employed [14]. The modulation strategy is augmented with a redundancy-based switching algorithm that actively selects among the available redundant switching states of the PUC5 topology. The selection criterion is driven by the goal of minimizing voltage imbalance, where the switching state is dynamically chosen according to the instantaneous capacitor voltage deviations and the direction and magnitude of the line current.

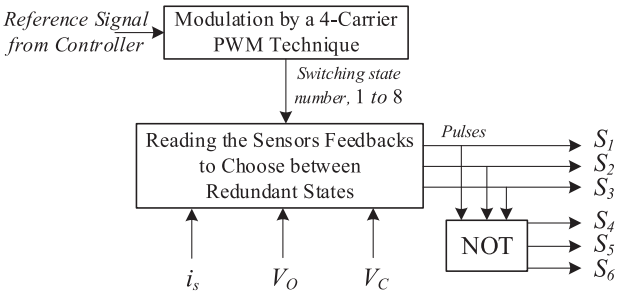

FIGURE 3. Voltage balancing technique integrated into the switching method.

Table 2 outlines the influence of various redundant switching states on the capacitor voltages, serving as a lookup reference for optimal switching decision-making within each sampling period. The implementation of the balancing algorithm within the PWM modulation block, as illustrated in Fig. 3, enables fast correction of voltage imbalances. This integrated approach facilitates real-time balancing without needing an external balancing loop or additional control layers. Due to the effectiveness of the embedded voltage balancing mechanism, the design allows for the use of relatively small capacitance values on the lower DC bus. This reduction in required capacitance not only contributes to improved power density but also enhances system reliability by reducing the stress and aging effects typically associated with large electrolytic capacitors.

III. CASCADED PI CONTROLLER

As mentioned, the PUC5 configuration was introduced as a single-DC-source inverter since the auxiliary capacitor voltage is balanced through the switching states. Although the proposed topology has two DC capacitors in rectifier mode, the auxiliary one is voltage-controlled by the designed switching technique and requires no additional voltage regulator. Hence, in this work, only one external voltage controller is needed to fix the output DC terminal at the desired level of 200 V. That means a simple cascaded PI Controller can be used to regulate the output DC voltage as well as to control the input current and synchronize it with the grid voltage to ensure the PFC operation of the rectifier. That type of controller is widely used by industries in market products [17]. A detailed design process of cascaded PI controller is discussed in [7], and the implemented schematic is shown in Fig. 4.

To regulate the output voltage V_O and ensure power factor correction, a cascaded control structure is implemented for the PUC5 rectifier. The outer voltage control loop regulates the DC-link voltage by dynamically adjusting the amplitude of the reference current $i_s{}^*$. This loop operates in conjunction with a phase-locked loop (PLL) that extracts the phase angle of the input AC voltage v_s. The PLL output is used to synchronize the reference current waveform with the input voltage, thereby enabling unity power factor operation.

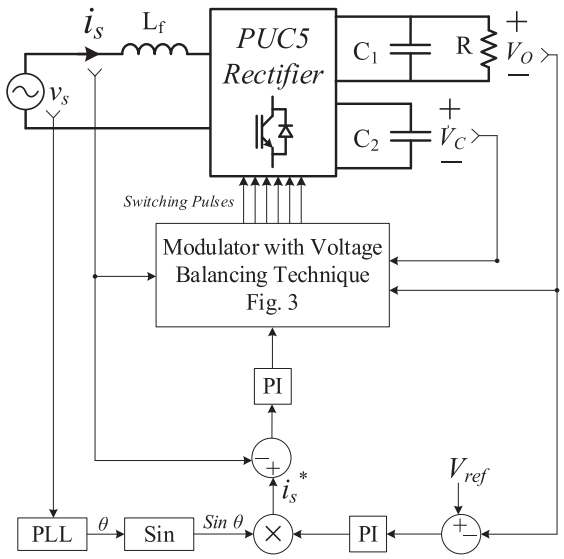

FIGURE 4. Cascaded PI controller applied on the PUC5 rectifier.

For stable and responsive operation, the control bandwidths of the cascaded loops are carefully selected. The outer voltage loop is designed with a bandwidth in the range of 30–50 Hz. This ensures adequate voltage regulation while maintaining sufficient decoupling from the dynamics of the inner current loop. The inner current loop, which is responsible for tracking the sinusoidal current reference, must possess a significantly higher bandwidth—typically in the range of 200–400 Hz. This range allows precise tracking of the 60 Hz fundamental component with minimal phase delay and ensures compliance with low THD requirements. Importantly, the selected bandwidth is kept well below the switching frequency (2 kHz) to prevent the controller from responding to high-frequency switching harmonics or PWM-induced ripple, which could otherwise compromise system stability and performance. The final current reference generated by the control loops is modulated using a standard four-carrier PWM strategy. This modulation technique is inherently compatible with the PUC5 topology and facilitates the integration of the voltage balancing algorithm, as shown in Fig. 3. The complete control process is illustrated in Fig. 4.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

Practical tests have been carried out on a prototype of the PUC5 rectifier. The proposed voltage balancing approach integrated into the switching technique and the cascaded controller has been implemented on dSpace 1103, and consequently, switching pulses are sent to the PUC5 switches. The tested system parameters are listed in Table 3.

The steady-state results at 1 kW have been captured, as seen in Fig. 5. Both Fig. 5(a) and (b) demonstrate that the output DC terminal voltage is regulated at 200 V with an acceptable voltage ripple of less than 10%. Moreover, the PFC operation of the PUC5 converter can be observed through the input voltage and current waveforms (v_s and i_s). As shown in

TABLE 3. Practical Tests Parameters

Grid Voltage Frequency	60 Hz
Grid Voltage (vs)	120 V RMS
Output DC Voltage (Vdc)	200 V
DC Load (R)	38 Ω
Switching Frequency	2 kHz
Inductive filter (Lf)	2.5 mH
C1 Capacitor	2000 µF
C2 Capacitor	50 µF

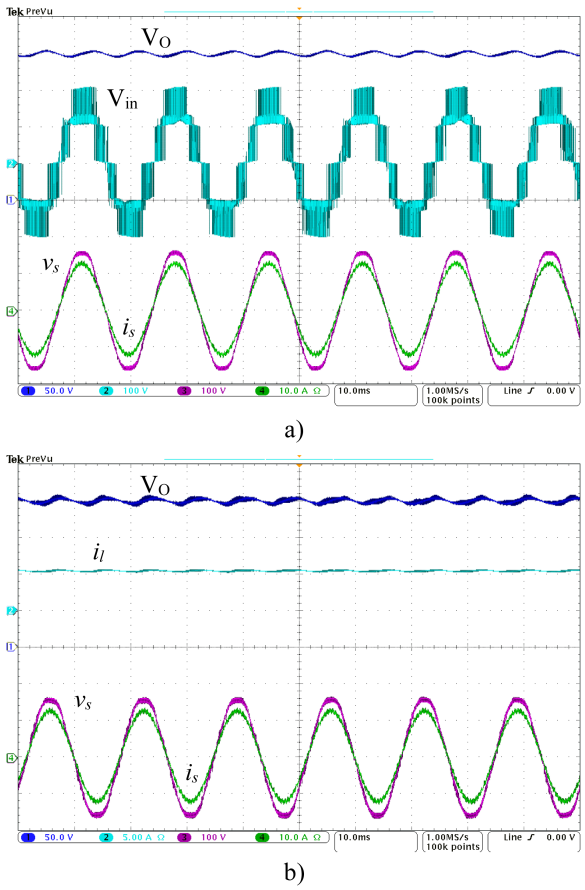

FIGURE 5. Steady-state results of 1 kW PUC5 rectifier.

Fig. 5(a), the V_{in} has been formed by 5 identical voltage levels of 0, ±100, ±200 V. Although the ±100 V levels show some voltage ripples inside, it should be noted that the auxiliary capacitor has been selected as 50 μF, which is small enough to be attractive for design aspects and also large enough to have less than 10% voltage ripple thanks to the effective voltage balancing of V_C, which resulted in lower harmonic distortion than existing rectifiers in the market (e.g., full-bridge configuration). The THD results are shown in Fig. 6. Such smooth quasi-sine wave requires less filtering effort compared to 2-level conventional rectifiers to comply with acceptable harmonic levels recommended in standards like IEEE STD 519 [18]. The lower the harmonics, the smaller the filters, the lower the losses, and the smaller the size of the rectifier.

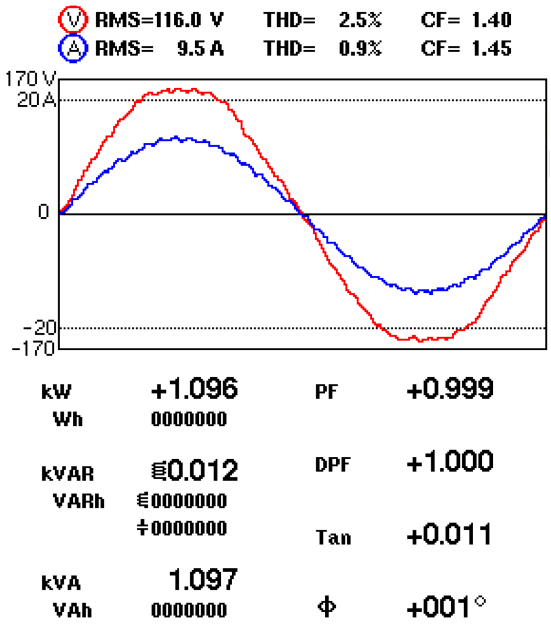

FIGURE 6. Power analyzer measurements of the AC side voltage/current in the PUC5 rectifier.

Eventually, as depicted in Fig. 5(b), the load current (i_l) is measured at almost 5A, demonstrating the 1 kW operating system at 200 V DC.

Fig. 6 depicts some other parameters measured by the AEMC power analyzer. The PUC5 rectifier has been tested at 1 kW with the highest possible power factor, significantly reducing the amount of reactive power and promising the controller a good performance in synchronizing the line current with the grid voltage. Moreover, the current THD is too low, thanks to the low harmonic pollution of the multilevel voltage waveform generated by the PUC5 rectifier.

Eventually, a 50% load change has been made intentionally from 38 Ω to 75 Ω to examine the dynamic performance of the controller. As shown in Fig. 7(a), the load current is reduced to almost half of the initial amplitude. Consequently, due to changes in the amount of energy delivered to the load, the VO varies yet is well stabilized by the controller and voltage balancing technique without unexpected over or undershooting. Moreover, the input AC current is kept synchronized with the grid voltage while its amplitude changes to reach the steady state mode. It is clear that the current harmonic is also controlled during the transition. As shown in this figure, other measurements have been done through a power analyzer. It is obvious that the PUC5 rectifier and implemented controller are working correctly even at half-load conditions by synchronizing the grid voltage and current as the PFC mode of operation. As well, the THD of the AC current is still smaller than the standard of 5%.

The experimental validation of the PUC5 rectifier demonstrates the effectiveness of the proposed configuration, control strategy, and integrated voltage balancing mechanism. The controller exhibits excellent dynamic response, ensuring rapid

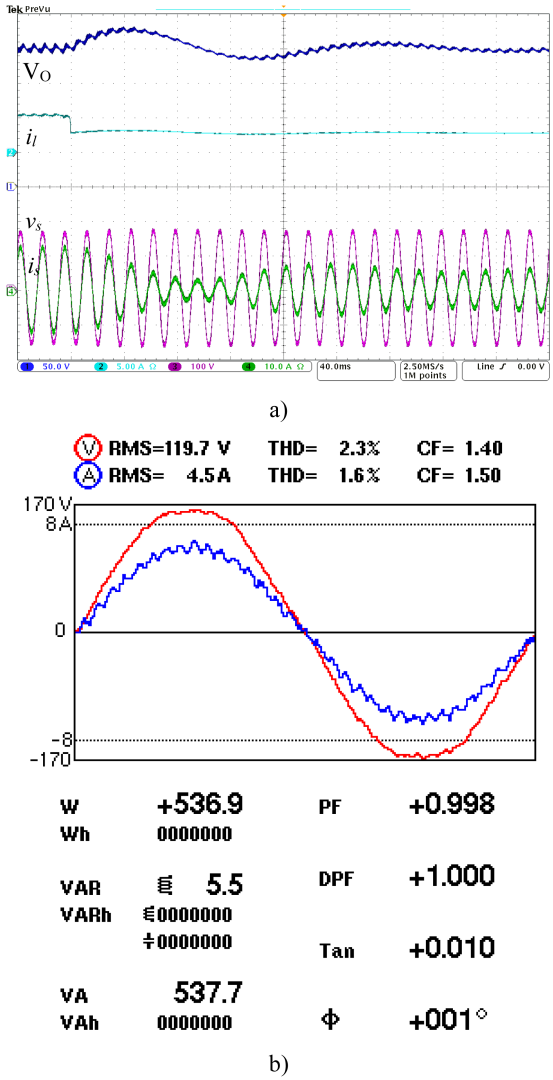

FIGURE 7. PUC5 rectifier test results during a 50% change in the DC load.

adaptation to transient conditions, while the embedded voltage balancing technique, incorporated within the modulation algorithm, maintains the auxiliary capacitor voltage at the desired reference with minimal voltage ripple. This results in the generation of a high-quality five-level quasi-sinusoidal voltage waveform at the AC input terminal of the rectifier. The multilevel waveform significantly reduces the THD, enabling compact passive filters to meet stringent grid current harmonic standards. Such a feature is particularly advantageous in high-power density applications where size and efficiency are critical design parameters.

The PUC5 topology's inherent ability to synthesize multilevel waveforms using a reduced number of active switches and DC capacitors makes it a strong candidate for industrial rectifier applications, particularly in electric traction systems and electric vehicle (EV) charging infrastructure. Furthermore, the commercial deployment of the PUC5-based converter by dcbel Inc., marketed under the product name *Ara*^{TM}, marks a significant milestone. *Ara*^{TM} is recognized

as the world's first bidirectional EV charger and photovoltaic (PV) inverter capable of operating in all vehicle-to-everything (V2X) modes, including V2G and V2H, with high operational efficiency and system-level reliability. This commercial adoption underscores the practical viability and market readiness of the PUC5 architecture in modern power conversion systems [16].

V. CONCLUSION

In this work, the PUC5 rectifier topology has been introduced, analyzed, and experimentally validated. A novel voltage balancing technique was developed and seamlessly integrated into the modulation scheme to effectively regulate the auxiliary capacitor voltage. This integration enables the synthesis of five voltage levels at the AC input, producing a smooth, low-distortion multilevel voltage waveform with significantly reduced harmonic content. The single DC-link structure simplifies the controller design, which eliminates the need for split capacitors, allowing the use of a conventional cascaded PI controller for current regulation and DC-link voltage control. Experimental results confirm the strong dynamic performance of the proposed system under both steady-state and transient load conditions. The voltage balancing method maintains capacitor voltage stability with minimal ripple, ensuring reliable multilevel operation even during abrupt load changes. The compact design, efficient voltage regulation, and reduced filter requirements position the PUC5 rectifier as a promising solution for bidirectional AC–DC conversion in hybrid energy systems, such as electric vehicle charging stations, smart grids, and renewable energy hubs. Its practical viability is further reinforced by ongoing commercial deployment in real-world applications.

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