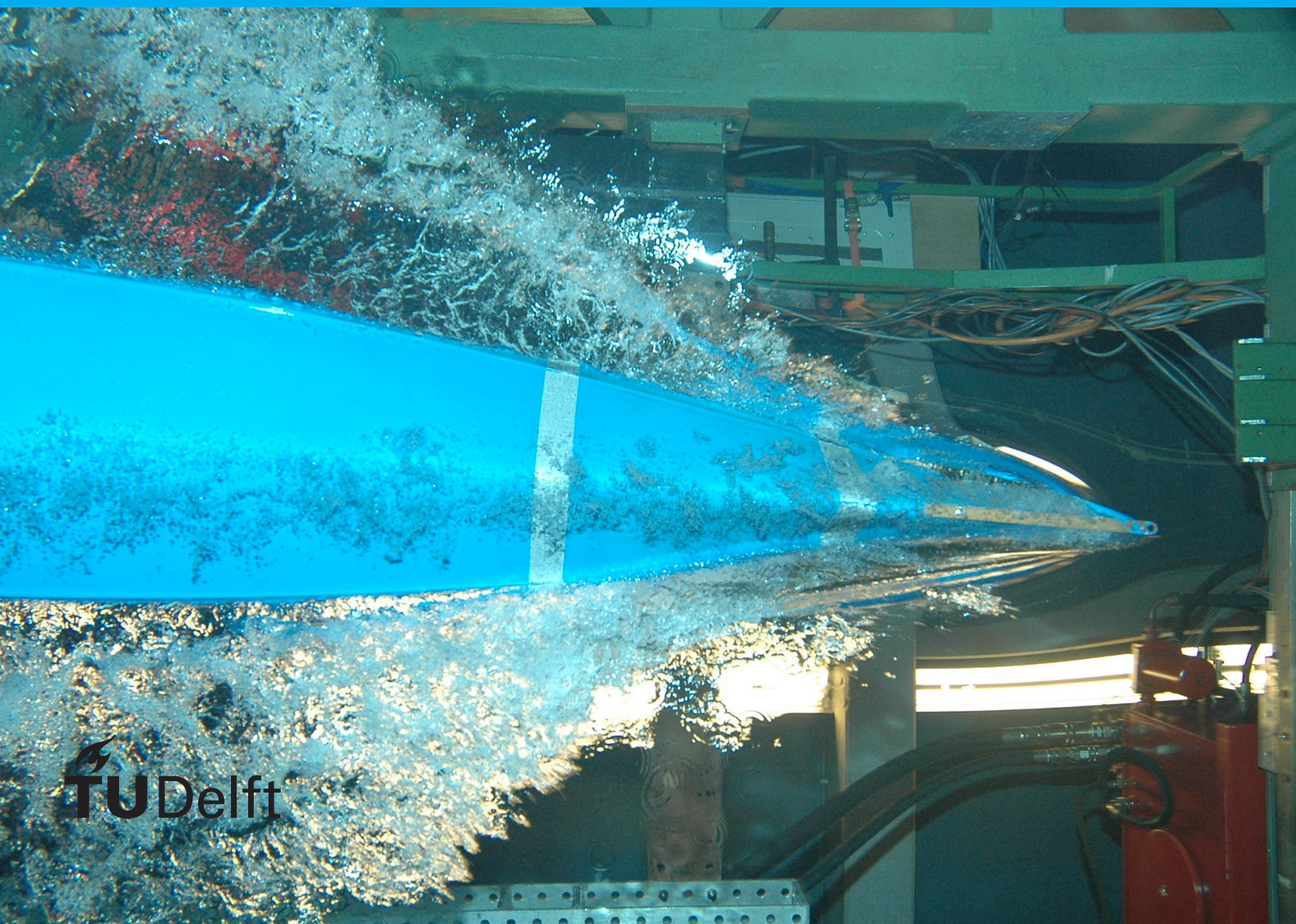
# Diagnosis Methodology for STT-MRAM

## Defect Identification and Classification

A. Aouichi



# Diagnosis Methodology for STT-MRAM

## Defect Identification and Classification

by

A. Aouichi

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at the Delft University of Technology,
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# List of Abbreviations

AI Artificial Intelligence

API Application Programming Interface

ATE Automatic Test Equipment

ATS Asian Test Symposium

BER Bit Error Rate

BH Back-Hopping

CD Critical Diameter

CUT Chip Under Test

DAT Device-Aware Test

DDR4 Double Data Rate 4

DFT Design For Testability

DRAM Dynamic Random-Access Memory

FF Flip-Flop

FIB Focused Ion Beam

FL Free Layer

FN False Negative

FP False Positive

HL Hard-Layer

IC Integrated Circuit

IM Intermediate State

IMEC Interuniversity Microelectronics Centre

KNN K-Nearest Neighbor

LVI Laser Voltage Imaging

ML Machine Learning

MTJ Magnetic Tunnel Junction

NN Neural Network

PEM Photon Emission Microscopy

PFA Physical Failure Analysis

PH Pinhole

PL Pinned Layer

RH Resistance-Magnetic Field

RL Reference Layer

RTL Register-Transfer Level

RER Read Error Rate

SA Sense Amplifier

SAFF Synthetic Anti-Ferromagnetic Flip

SAF Synthetic Anti-Ferromagnet

SEM Scanning Electron Microscopy

SRAM Static Random-Access Memory

STT Spin-Transfer Torque

STT-MRAM Spin-Transfer Torque Magnetic Random-Access Memory

TB Tunnel Barrier

TEM Transmission Electron Microscopy

TMR Tunnel Magnetoresistance

TN True Negative

TP True Positive

TSV Trough-Silicon Via

VLSI Very-Large Scale Integration

WER Write Error Rate

# Abstract

This thesis focuses on identifying and classifying defects in STT-MRAM technology using novel and machine learning approaches. The thesis discusses the basic principles of STT-MRAM and the semiconductor chip manufacturing process and test stages. The research aims to develop novel methods and explore machine-learning approaches to diagnose defects in STT-MRAM devices. The current defect identification methodologies have shown certain cost, speed, and scalability limitations. The thesis presents DAT-based and ML-based Diagnosis methodologies to identify and classify STT-MRAM unique defects to address these challenges. The methods are evaluated and validated on experimental wafers performed at IMEC in Leuven, Belgium.

DAT-based Diagnosis involves automated defect identification in STT-MRAM based on identifying features automatically extracted from specialized measurements targeting the unique defects, Pinhole, Intermediate State, SAF Flip, and Back-Hopping. ML-based Diagnosis uses machine learning techniques to classify defects using MTJ features extracted from low-cost measurements. Data collected from electrical measurements on experimental STT-MRAM devices serve as the basis for evaluating the developed methodologies. The thesis also discusses data analysis, including data visualization, feature correlations, and outlier analysis for future research. Furthermore, a machine learning training process is performed, including hyperparameter optimization and evaluation using F-score and B-accuracy metrics to assess the model's performance and the ability to generalize on unseen data.

DAT-based Diagnosis aims to maximize the defect detection accuracy at the expense of measurement costs. In contrast, ML-based Diagnosis minimizes the measurement cost while maximizing the detection accuracy for robust and balanced classification. However, the DAT-based Diagnosis is not verified using PFA to validate the defect types identified by the developed methodology. Furthermore, the ML-based Diagnosis uses training data labeled by the unverified DAT-based Diagnosis approach to train machine learning models. Despite these limitations, the results have shown valuable insights into defect identification and classification, proving a robust framework for diagnosing STT-MRAM devices. Additionally, a scientific paper is submitted on march-based diagnosis, adapting the DAT-based Diagnosis method to industrial chips that are limited in extracting the identifying features; see appendix A.

A. Aouichi
Delft, August 2023

# Contents

# 1 Introduction

This chapter introduces the motivation, the challenges this thesis addresses, the state-of-the-art, and the main contributions. Section 1.1 motivates the need for defect identification and classification of STT-MRAM devices. Section 1.2 shows the state-of-the-art methods for defect identification and classification of memory devices. Section 1.3 summarizes the contribution of the research project. To conclude, section 1.4 illustrates the outline of the thesis.

## 1.1. Motivation

Spin-Transfer Torque Magnetic Random-Access Memory (STT-MRAM) is considered a promising technology memory due to its non-volatility, scalability, and fast write and read operations Garzon et al., 2020. Compared to conventional memory devices such as Dynamic Random-Access Memory (DRAM), Static Random-Access Memory (SRAM), and Flash, STT-MRAM combines several advantages of these memories Apalkov, 2013. STT-MRAM is a promising memory solution to the evolving demands for efficient memory in terms of speed and cost Nam, 2006; Yoda, 2015. However, like any electronic device, STT-MRAMs are susceptible to manufacturing defects affecting their performance and reliability. The limited diagnosis methodologies for STT-MRAM defect identification limit its commercialization. The manufacturing processes still need to be fully optimized to reduce the occurrence of defects, leading to low yield. Unlike traditional memory technologies, the unique magnetic properties of STT-MRAM present additional challenges in understanding and identifying these defects Zhang, 2016; Zhao, 2012.

Defects in STT-MRAM devices can occur during various stages of the process, such as material deposition, engraving, etching, and annealing Moreau, 2012. These defects can manifest themselves as changes in magnetic properties, resistivity, or structural integrity Fieback et al., 2019a. The presence of defects can cause increased power consumption, write and read errors, and even device breakdowns Zhang, 2016. Therefore, identifying and classifying these defects is important to ensure the quality and productivity of STT-MRAM devices efficiently.

Traditional methods for defect identification in STT-MRAM devices often rely on costly, destructive, and time-consuming techniques during Physical Failure Analysis (PFA) M. Wu, 2012. PFA aims to find the root cause of the failing chips after the localization of the defective part by diagnosis tools L. Wagner, 2001. These approaches are not only resource-intensive but also limit the scalability and cost-effectiveness of defect identification. Furthermore, the manual intervention required for analyzing the measurement data makes the process vulnerable to human error and subjectivity. Due to the unique electrical and magnetic properties of STT-MRAM, it is more challenging to identify and classify defects with conventional methods.

There is a need for developing smart and low-cost diagnosis solutions that can accurately identify and classify defects in STT-MRAM devices while minimizing the complexity and the costs involved. By leveraging advanced techniques such as electrical and magnetic measurements for defect identification, fitting for feature extraction, and machine learning algorithms for defect classification, it is possible

to develop an automated defect identification and classification system that is both accurate and cost-efficient.

This thesis addresses the challenges of defect identification and classification in STT-MRAM devices. By proposing a novel approach that combines electrical measurements, fitting techniques, and machine learning algorithms, our aim is to develop a smart and low-cost solution that improves the accuracy, scalability, and costs used for diagnosis to guide or even replace PFA. Automated defect identification and classification are critical in STT-MRAM technology for increasing yield and producing high-quality STT-MRAM memory chips.

## 1.2. State-of-the-art

Conventional diagnosis and defect identification methodologies for memory devices have made significant progress in ensuring product quality and improving yield learning. These methods typically involve pattern generation, electrical testing, and physical failure analysis L. C. Wagner, 1999a; L. Wagner, 2001. These methods face certain limitations regarding scalability, cost, and efficiency D. P. Vallett, 1997; Venkataraman, 2004.

Pattern generation techniques in high-volume production environments label the device as defective or defect-free, where the test time is considered an important metric. Therefore, the test patterns generated by the test algorithms are used to identify faults instead of defects Wang et al., 2006a. Faults refer to the defect's impact on the logical behavior of the targeted chip module. A fault can cover multiple physical defects since different defects can have similar logical impacts. Therefore, these testing methods are not optimal for defect identification and learning J.-F. Li et al., 2001; Wang et al., 2006b.

Electrical testing is a commonly used method to detect and characterize defects in memory devices. Techniques such as current-voltage (I-V) measurements, pulse testing, and frequency response analysis provide insights into the device's behavior and performance Zschech et al., 2002. Deviations from expected electrical behavior can be detected, indicating the presence of defects. However, these methods require specialized equipment, measurement setup, and time-consuming test procedures.

Physical failure analysis techniques are commonly used techniques that offer high-resolution imaging of the device and material structure and properties and the root cause and the underlying defects of the failed devices, such as Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM), fault isolation, Photon Emission Microscopy (PEM), and Laser Voltage Imaging (LVI) Nokuo, 2007; L. Wagner, 2001. These techniques provide detailed information about the defects present in the memory devices and identify the defects responsible for the device failure. However, these methods are time-consuming and require special equipment and expertise. In addition, these methods are used for small samples, making it challenging to analyze many devices for defect identification.

While these conventional methodologies have proven effective in defect identification and classification, there are certain limitations regarding scalability, cost, and speed. As the demand for more complex devices increases, smarter, more efficient, and cost-effective defect identification and classification are required. Several researchers are exploring alternative approaches to address these challenges using machine learning to make it possible to develop automated, scalable, and cost-effective solutions for defect identification and classification. The integration of machine learning has shown potential in automating defect classification by extracting key features from large data sets such as test responses generated during production tests, parameters from electrical measurements and simulations, images from physical characterization results, and other types of data leading to more efficient defect classification.

More efficient and intelligent methods for defect identification and classification in memory devices will lead to improved yield, reduced costs, and enhanced reliability. As a result, high-quality memory devices can be developed due to the optimized manufacturing process by smarter diagnosis methodologies. Machine learning has great potential to revolutionize the diagnosis process and the production test of memory devices.

## 1.3. Contribution

This thesis aims to develop smart and efficient diagnosis methodologies for identifying and classifying STT-MRAM unique defects, Pinhole (PH), Intermediate State (IM), Synthetic Anti-Ferromagnetic Flip (SAFF), and Back-Hopping (BH) defects by addressing the challenges discussed above.

The key contributions of this research can be summarized as follows:

1. Device-Aware Test (DAT)-based Diagnosis: The thesis proposes a novel methodology for STT-MRAM defect identification using specialized electrical measurements and fitting functions to automatically identify the known defect type. The methodology is based on the defects' physical behavior and its impact on the device parameters, and the method aims to identify the defects as accurately and efficiently as possible.

2. Accepted Paper: For many industrial chips, DAT-based Diagnosis methodologies do not apply to measure the device parameters. Therefore, this thesis proposes a diagnosis method to identify the defects based on digital patterns applicable to industrial design. We are pleased to announce the acceptance of a research paper on March-Based Diagnosis, which derives from the principles and findings outlined in this thesis, see appendix A.

3. Machine Learning (ML)-based Diagnosis: The thesis also explores the machine learning potential to classify the defects identified by the DAT-based Diagnosis method using features from low-cost measurements. The goal is to speed up the diagnosis process by utilizing the correlations and patterns of the low-cost features and the defect types.

4. Framework: This thesis demonstrates a framework to diagnose emerging technologies that go beyond the traditional approaches targeting conventional defects. The framework consists of a systematic approach to developing a diagnostic methodology for unique defects.

5. Software: Extracting parameters and features required for the proposed diagnosis methodologies is performed using dedicated written software. The software consists of several modules to handle and process STT-MRAM raw data, automatically extract relevant features, and identify and classify the defect types.

6. Data analysis: Lastly, the data and results acquired from measurements are analyzed to identify outlying defective behavior and study the correlations between relevant features. The purpose of the analysis is to pinpoint defective outliers for future research.

Overall, this thesis makes relevant contributions to STT-MRAM defect identification and classification using the proposed diagnosis methodology, integration of machine learning, and outlying behavioral analysis of the measured data. The thesis emphasizes researching potential diagnosis methods of STT-MRAM devices for yield learning and optimizing the manufacturing process by intelligent and efficient defect identification and classification.

## 1.4. Outline

This research explores the potential of machine learning in diagnosing and testing STT-MRAM devices. Several steps are involved in addressing the research question, as illustrated in figure 1.1. First, a comprehensive background study was conducted to fully understand the technology of STT-MRAM, the principles of the test and diagnosis of Integrated Circuit (IC), and machine learning techniques. Following the background study, a review of the literature focused on conventional methods for testing and diagnosing STT-MRAM is conducted. This literature study provided valuable insights into the existing methodologies and highlighted the need for efficient and effective diagnostic techniques for emerging technologies like STT-MRAM. Based on the problem statement and the findings from the literature review on machine learning applications in IC test and diagnosis, the research proposal was defined as developing a robust and efficient defect identification and classification methodology for STT-MRAM. The proposed methodology aims to use machine learning techniques and novel approaches to identify and classify STT-MRAM manufacturing defects.

Chapter 2 explains the STT-MRAM principles and operations, including the fundamental physics and

the key parameters. Chapter 3 provides an overview of the test and diagnosis phases of integrated circuits and their current machine learning applications. Furthermore, the chapter also discusses the manufacturing defects targeted in this thesis. Lastly, the conventional test and diagnosis methodologies for emerging technologies such as STT-MRAM are explained. This overview lays the foundation for developing machine learning solutions and novel approaches for STT-MRAM diagnosis used in this project.

Chapter 4 proposes the two methodologies for defect identification and classification of STT-MRAM manufacturing defects, DAT-based Diagnosis and ML-based Diagnosis. Chapter 5 discussed the implementation of the proposed methodologies on real STT-MRAM devices at Interuniversity Microelectronics Centre (IMEC) in Leuven, Belgium. Additionally, the measured data will be analyzed to identify new potential defects and outlying defective behavior of the STT-MRAM devices. Lastly, Chapter 6 concludes the thesis and presents recommendations for future research in defect identification and classification of emerging devices such as STT-MRAM.

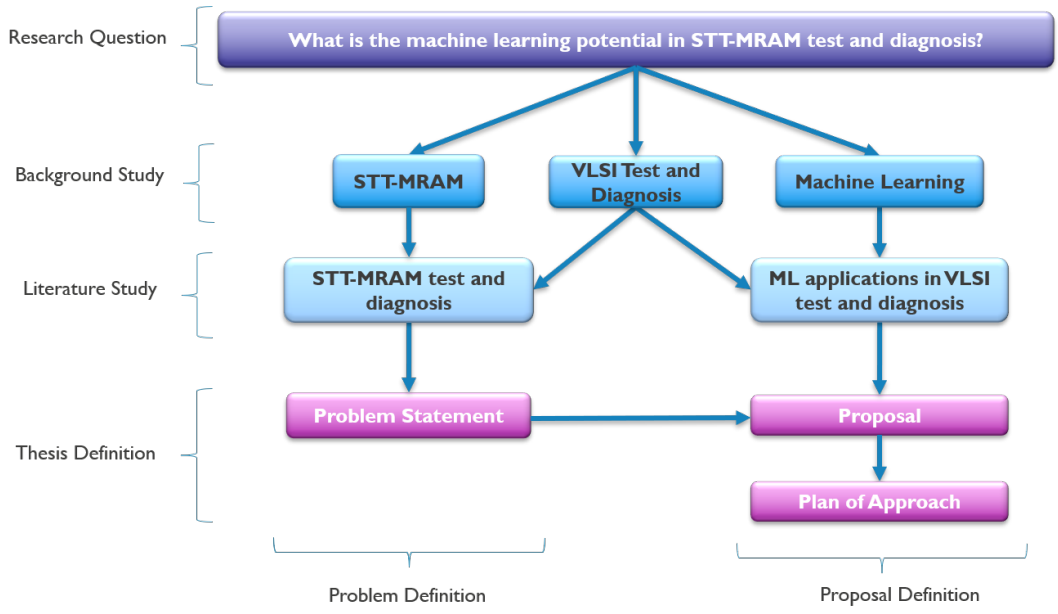



Figure 1.1: Thesis Workflow for Proposal and Problem Definition

# 2

# Background on STT-MRAM Principles and Manufacturing Defects

This chapter provides a comprehensive background on STT-MRAM basics and the targeted defects for identification and classification. The fundamental concepts of STT-MRAM serve as a foundation for feature engineering in machine learning. It is essential to understand the underlying physical faulty behavior of the memory cell in order to develop diagnostic solutions. Section 2.1 and section 2.2 explain the STT-MRAM basic principles and operations and the internal manufacturing defects. The chapter concludes in section 2.4 with an overview of the key parameters affected by the defects used as the baseline for this research.

## 2.1. STT-MRAM

STT-MRAM offers several benefits due to its high performance, endurance, low power consumption, and non-volatility. Therefore, STT-MRAM shows potential for various applications such as cache applications, solid-state drives, mobile devices, automotive electronics, and the Internet of Things. Additionally, it can replace part of the memories in computing systems and enable neuromorphic computing. However, several challenges exist, such as reducing costs, minimizing process variations, and diagnosing and understanding manufacturing defects, which is the goal of this thesis. Researchers aim to improve the performance, reliability, and commercial availability of STT-MRAM to overcome these challenges.

### 2.1.1. Magnetic Tunnel Junction

STT-MRAM is a non-volatile memory with a Magnetic Tunnel Junction Magnetic Tunnel Junction (MTJ) storage element and a transistor to select the memory cell. An MTJ consists of two magnetic layers separated by a thin insulating layer. The top magnetic layer is a ferromagnetic material called the Free Layer (FL). The bottom magnetic layer consists of two ferromagnetic layers: the Reference Layer (RL) and Hard-Layer (HL) and referred to as the Pinned Layer (PL), see figure 2.1. $RL$ and $HL$ are anti-ferromagnetically coupled and separated by a thin layer of ruthenium. Ferromagnetic materials have permanent magnetization in the absence of an external magnetic field. Anti-ferromagnetic materials have zero net magnetization due to the opposite orientation of the magnetization domains within the material. However, both $RL$ and $HL$ are ferromagnetic materials and are anti-ferromagnetically coupled due to the opposite magnetization of the two layers, resulting in a fixed magnetization direction of the $RL$.

### 2.1.2. STT-MRAM Array

The STT-MRAM memory array is organized in the form of a matrix with $N$ rows and $M$ columns of STT-MRAM cells. Each STT-MRAM cell typically stores 1 bit of data in an MTJ and contains a transistor to select the cell through row and column decoders. The data are stored by applying a relatively high current and read by applying a small current through write drivers. The value of the data written to an STT-MRAM cell is determined by the direction of the applied current. Each column consists of a

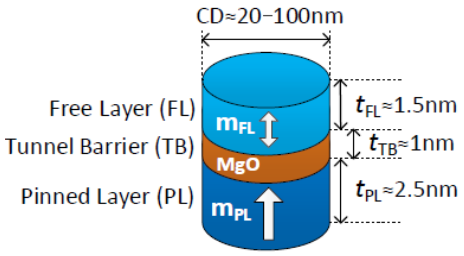



Figure 2.1: Magnetic Tunneling Junction L. Wu, 2021

sense amplifier to read the stored data as logical values, 0 or 1, making the memory array compatible with the conventional memory interfaces such Double Data Rate 4 (DDR4) L. Wu, 2021, see figure 2.2.

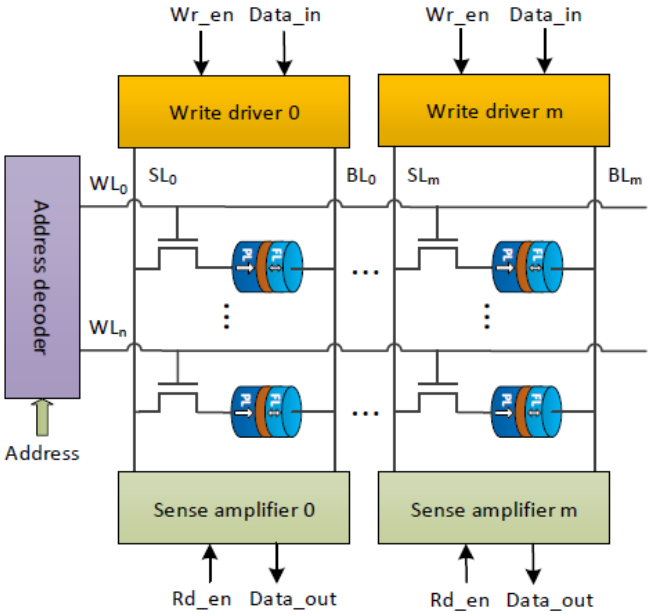
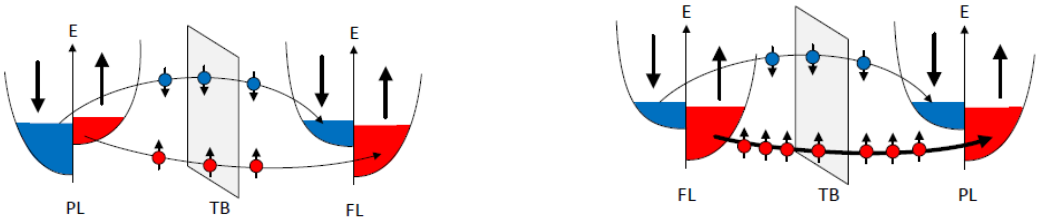



Figure 2.2: STT-MRAM circuit organization L. Wu, 2021

### 2.1.3. Tunnel Magneto-Resistance Effect

This basic layered structure of the MTJ allows the storage element to be in a high or low resistance state depending on the relative magnetization of the $FL$ and the PL. A low resistance is obtained when the magnetization of the two layers is in parallel, $R_P$, and a high resistance is obtained when the magnetization of the two layers is anti-parallel, $R_{AP}$. The electrons of a specific spin orientation can tunnel from one electrode to the other electrode. Therefore, the MTJ acts as a storage element with parallel and anti-parallel states representing 0 and 1, respectively. The change of the tunneling current in MTJ when the relative magnetization of $FL$ and $RL$ is changed is called the Tunnel Magnetoresistance (TMR) effect; see figure 2.3. TMR allows the data to be read from the MTJ by applying a current small enough not to change the magnetization direction of $FL$ and strong enough to read the resistance state of the MTJ. TMR effect can be modeled by equation 2.1, also known as the TMR ratio Khvalkovskiy et al., 2013; L. Wu, 2021.

$$TMR = \frac{R_{\mathrm{AP}} - R_{\mathrm{P}}}{R_{\mathrm{P}}} = \frac{2P_{\mathrm{FL}}P_{\mathrm{PL}}}{1 - P_{\mathrm{FL}}P_{\mathrm{PL}}} \text{ with } P = \frac{n\uparrow - n\downarrow}{n\uparrow + n\downarrow} \tag{2.1}$$




(a) Anti-Parallel state

(b) Parallel state

Figure 2.3: Band diagram representing the Tunnel Magneto-Resistance effect

### 2.1.4. Thermal Stability

Data storage is characterized by the thermal stability factor Δ, representing the ability of the memory cell to hold the stored data over time under different temperature conditions. The magnetization orientation of the $FL$ can be flipped due to thermal fluctuations over time. The thermal stability is the ratio of the energy barrier, $E_B$, divided by the operation temperature in $k_B$ units; see equation 2.2. $E_B$ is the energy that has to be overcome by the $FL$ to flip its magnetization, see figure 2.4. The retention time is when the memory cell can hold its data over a certain period; see equation 2.3. $\tau_0$ is the time constant assumed to be 1ns. Therefore, the data storage ability of an MTJ can be improved by increasing the thermal stability factor Khvalkovskiy et al., 2013; L. Wu, 2021.

$$\Delta = \frac{E_{\mathrm{B}}}{k_{\mathrm{B}}T} = \frac{\mu_0 M_{\mathrm{s}} V H_{\mathrm{k}}}{2k_{\mathrm{B}}T} \tag{2.2}$$

$$RT = \tau_0 e^{\Delta} \tag{2.3}$$

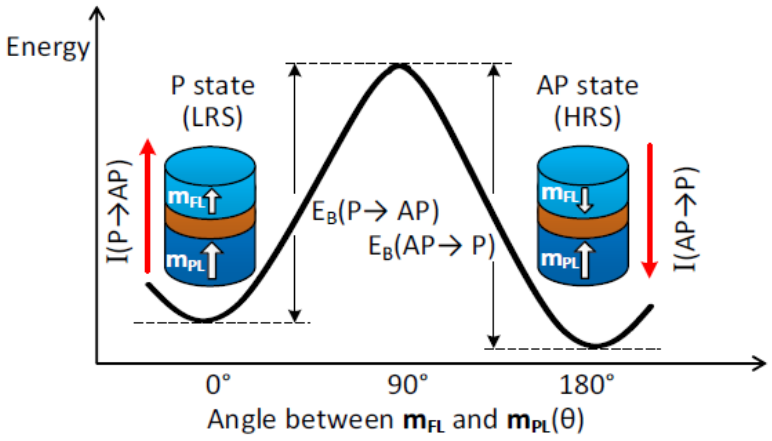



Figure 2.4: Energy barrier between parallel and anti-parallel states L. Wu, 2021

### 2.1.5. Spin-Transfer Torque Effect

Writing data to an MTJ is done through the Spin-Transfer Torque (STT) effect, where spin angular momentum is transferred between the $FL$ and the PL. When a current flows through the MTJ, the electrons are either attracted or repelled by the FL, depending on the spin orientation of the electrons. The two states of the electron, spin-up and spin-down, describe the magnetic state of the applied spin-polarized electrons. As a result of the $FL$ drawing electrons with the opposite spin orientation, a net transfer of spin angular momentum occurs between the two layers. This transfer results in a torque on the $FL$ magnetization, which flips its direction; see figure 2.5. The STT effect can be described by the critical current $I_C$ needed to switch the $FL$ from one state to another; see equation 2.4. $\alpha$ denotes the

rate at which the magnetization relaxes to its equilibrium magnetic state, referred to as the damping factor. The damping factor contributes to the switching time of an MTJ, where a current is applied over a certain period. $\eta$ denotes the STT efficiency describing the polarization of the injected current. Additionally, data can be written to the MTJ by applying an external magnetic field with the required magnetization orientation Khvalkovskiy et al., 2013; L. Wu, 2021.

$$I_{\mathrm{c}} = \left[\frac{4ek_{\mathrm{B}}T}{\hbar}\right]\frac{\alpha}{\eta}\Delta. \tag{2.4}$$

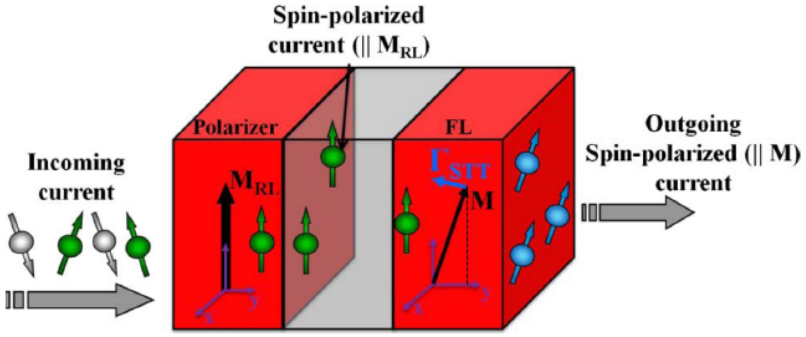



Figure 2.5: STT-induced switching from AP state to P state

## 2.1.6. Operational Regimes

In summary, the data can be read and written from and to an MTJ by applying a current smaller and higher than the critical current $I_C$ with a pulse width $t_{pw}$ through the TMR and STT effects, respectively. However, applying a current over a particular period of time during the write operation generates heat, resulting in thermal fluctuations in an MTJ. Therefore, the switching behavior of an MTJ can be dominated by thermal switching instead of STT switching, resulting in three MTJ switching regimes: precessional, dynamic, and thermal. The precessional regime is dominated by the STT effect where the pulse width $t_{pw}$ is short. In contrast, thermal stability is dominated in the thermal regime where the pulse width is sufficiently large. The thermal and the STT switching have an equal effect on the switching mechanisms in the dynamic regime Khvalkovskiy et al., 2013; L. Wu, 2021. The relation between the write current, pulse width, and regimes is illustrated in figure 2.6.

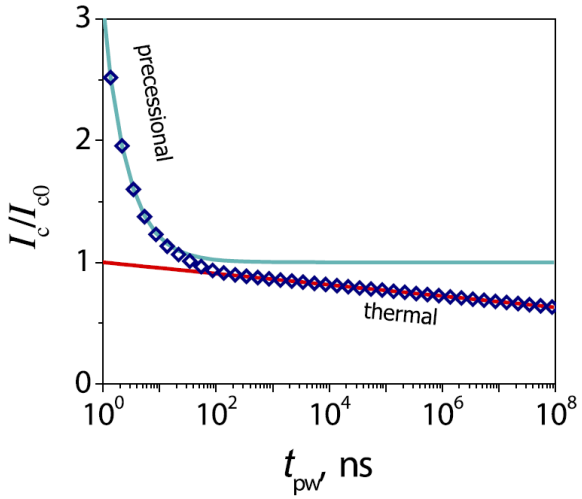



Figure 2.6: Normalized switching current $I_C/I_{C0}$ versus pulse width $t_{pw}$ in the precessional and thermal regimes for STT switching Khvalkovskiy et al., 2013. $I_{c0}$ is the critical current at zero temperature within an infinitely long time.

### 2.1.7. Device Key Parameters

The STT-MRAM key parameters can be classified as technology, electrical, and statistical. The technology parameters are the physical characteristics of the MTJ, and electrical parameters are related to the memory operations in response to an applied current or magnetic field. Statistical parameters represent the MTJ reliability and robustness in the case of multiple memory operations. The parameters are summarized as follows Khvalkovskiy et al., 2013; L. Wu, 2021:

- Technology parameters:
  - $A_0$ is the cross-sectional area of the MTJ, denoting the area of the tunnel barrier. The area affects the resistance of the device and the TMR ratio.
  - $M_s$ is the maximum magnetization the free layer can achieve. Saturation magnetization impacts the thermal stability of the device, the write error rate, and the read error rate.
  - $H_K$ is the magnetic anisotropy field representing the strength of the energy barrier that the free layer has to overcome to switch the MTJ. The field impacts the thermal stability and the switching time of the device.
  - The potential barrier height, $\bar{\varphi}$, refers to the energy required for the electrons to tunnel between the $FL$ and the $RL$ through the Tunnel Barrier (TB). The potential barrier has a direct impact on the resistance of the MTJ.
  - $RA$ is the resistance of the MTJ per unit area. The resistance is directly correlated with the resistance state of the storage element.
  - $TMR$ is the tunnel magneto-resistance ratio representing the TMR effect and the resistance change due to the FL's relative magnetization.
  - The stray field $H_{stray}$ is the magnetic field around $FL$ caused by the layer's magnetization, the field from the pinned layer ($PL$), the field from neighboring devices, and the externally applied magnetic field.
- Electrical parameters:
  - $R_P$ and $R_{AP}$ are the low and high resistance states or parallel and anti-parallel states, respectively, representing the stored data, 0 or 1.
  - $I_c$ is the critical current representing the minimum required current to write data to the device. Note that the critical current for writing 0 differs from the current required to write 1.
  - $t_{pw}$ represents the time for the free layer to switch its magnetization direction while applying a current through the device. Note that the switching time to write 0 may differ from the switching time of writing 1.
- Statistical parameters:
  - Write Error Rate (WER) and Read Error Rate (RER): Write and read error rates are considered key parameters for evaluating the device performance. The number of incorrect write and read operations to the memory cell are indicators of the device's robustness and correctness.

These device parameters are summarized in table 2.1. The STT-MRAM key technology, electrical, and statistical parameters are used in this project as a baseline to evaluate the impact of the defects on STT-MRAM performance. The relations between STT-MRAM parameters are summarized in figure 2.7 and 2.8 Khvalkovskiy et al., 2013L. Wu, 2021.

| Technology Parameters | | Electrical Parameters | | Statistical Parameters | |
|---|---|---|---|---|---|
| $A_0$ | Cross-sectional area | $R_P$ | Resistance in P state | $WER$ | Write Error Rate |
| $M_\mathrm{s}$ | Saturation magnetization | $R_{AP}$ | Resistance in AP state | $RER$ | Read Error Rate |
| $H_\mathrm{k}$ | Magnetic anisotropy field | $I_\mathrm{c}$ | Critical current | | |
| $\bar{\varphi}$ | Potential barrier height | $t_\mathrm{pw}$ | Switching time | | |
| $RA$ | Resistance-area product | | | | |
| $TMR$ | Tunneling magneto-resistance ratio | | | | |
| $H_\mathrm{stray}$ | Stray field | | | | |

Table 2.1: Key technology, electrical and statistical parameters of STT-MRAM Khvalkovskiy et al., 2013L. Wu, 2021. P and AP denote the parallel and anti-parallel states.

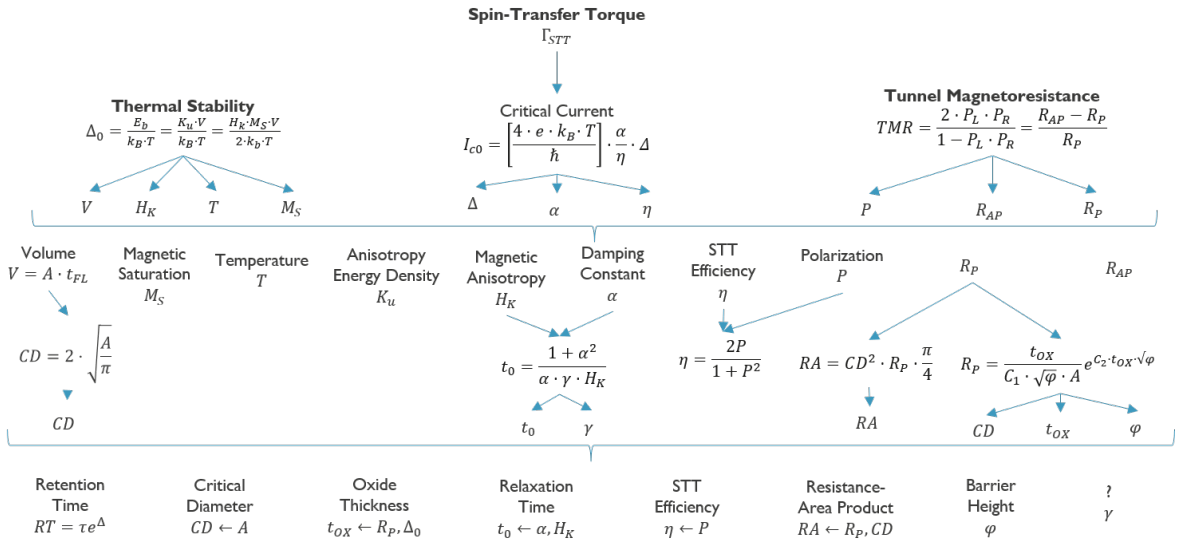



Figure 2.7: Relation and derivation of MTJ parameters of each of the three MTJ principles

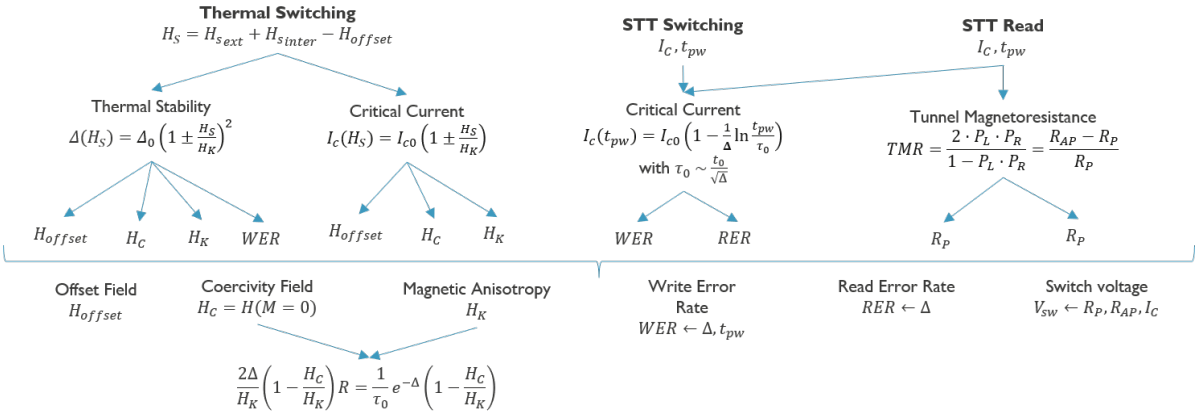



Figure 2.8: Relation and derivation of MTJ parameters of each of the three STT-MRAM operations

## 2.2. Manufacturing Defects

This thesis addresses four manufacturing defects in MTJ for identification and classification: PH, IM, SAFF, and BH. These defects are considered STT-MRAM's internal manufacturing defects taking place in the MTJ, referred to as unique defects. The external defects take place in the transistor and interconnects, referred to as conventional defects.

### 2.2.1. Pinhole

A pinhole (PH) is characterized by a small hole in the tunnel barrier (TB) or the insulating layer in the MTJ. TB is typically made of materials such as magnesium oxide (MgO) or aluminum oxide (AlOx), while $FL$ and $RL$are made of Cobalt Iron (CoFe) or Cobalt Iron Boron (CoFeB). The hole can result in electrical connections between $FL$ and RL, creating an unintended direct path for the electrons; see figure 2.9. TB should tunnel the electrons as an insulating layer. The defect affects the polarization of the electrons (P), barrier height ($\varphi$), and resistance-area product ($RA$). The impact of the defect on the device performance depends on the defect's size and location within the MTJ. The larger the pinhole, the more impact it has on the performance the easier it is to identify. The defect can be caused by improper deposition of materials, damaged tunnel barriers, or contamination during fabrication. The pinhole defect strength is modeled as the relative area of the hole to the cross-sectional area in MTJ, $A_{ph} \in [0, 1]$ L. Wu, 2021.

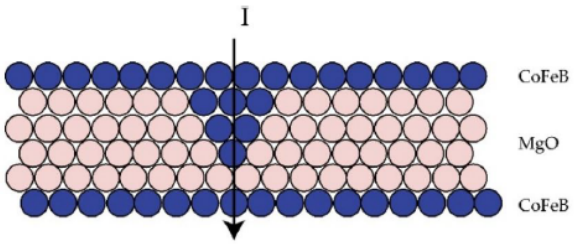
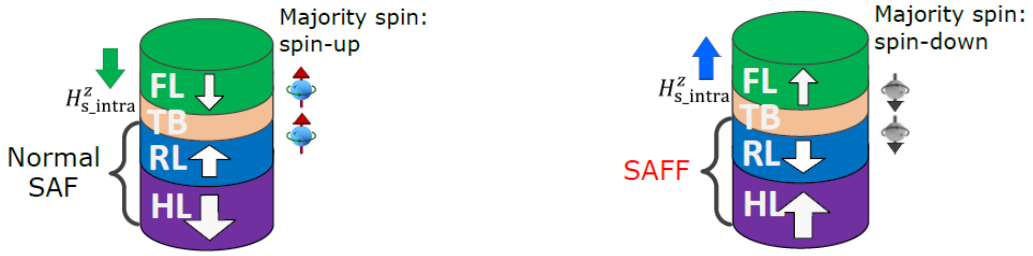



Figure 2.9: Pinhole defect in the tunnel barrier L. Wu, 2021

### 2.2.2. Synthetic Anti-Ferromagnet Flip

Synthetic Anti-Ferromagnet Flip (SAFF) is characterized by an unintended flip in the magnetization of the hard layer ($HL$). HL holds the reference layer ($RL$) magnetization to a fixed orientation. Due to the flip of HL, the $RL$magnetization direction is also flipped, causing the MTJ to have a flipped fixed magnetization. Since the magnetic state of the MTJ only depends on the relative magnetic orientation of the free layer ($FL$) to the reference layer ($RL$), the device's resistance is not impacted. The flipped magnetization does, however, impact the stray field of the device. Due to the flip of $RL$ and HL, the polarity of the stray field $H_{stray}$ at $FL$ also reverses; see figure 2.10. Therefore, the defect impacts the stray field, which impacts the critical current and the switching time due to the neighboring devices with the opposite stray field polarity. The SAFF defect strength is modeled as a binary value denoting the presence or the absence of the defect, $B_{SAFF} = \{0, 1\}$ L. Wu, 2021.



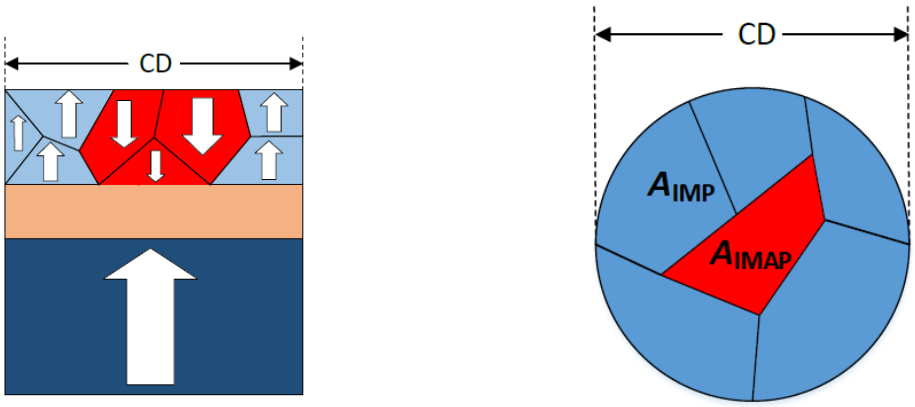

(a) Defect-free (b) Defective

Figure 2.10: Synthetic Anti-Ferromagnet Flip defect L. Wu, 2021

### 2.2.3. Intermediate State

An Intermediate State (IM) defect can be characterized as a third resistive state between the parallel and the anti-parallel state, 0 and 1. The $FL$ consists of domains where each domain represents the magnetization of a part of the layer. In the presence of the defect, some domains do not switch their

magnetization, resulting in a partially switched free layer, see figure 2.11. The physical mechanism of the defect is not yet fully understood, but it is believed to be related to impurities in the MTJ. The unintended third unknown state between $R_{AP}$ and $R_P$ in the MTJ causes faulty memory behaviors and reduces device reliability. The defect also reduces the critical current $I_c$ and the switching time $t_{pw}$. The defect strength is modeled as the relative area of the FL that is not switched, $A_{IMP} \in [0, 1]$ L. Wu, 2021.




(a) Vertical cross-section

(b) Horizontal cross-section

Figure 2.11: Domain regions in the FL representing the Intermediate State defect L. Wu, 2021

### 2.2.4. Back-hopping

A Back-Hopping (BH) defect is characterized as instability in the reference layer ($RL$), which leads to an oscillating switching effect during write operations. The reference layer consists of top and bottom layers, $RL_{top}$, and $RL_{bottom}$, separated by a thin insulator. The defect occurs due to weak magnetic coupling between the top and bottom layers in the RL. This weak coupling results in the $RL_{bottom}$ being well pinned due to the anti-ferromagnetic coupling with the hard layer ($HL$) while $RL_{top}$ is floating and unstable. This instability is affecting the $FL$ switching behavior due to the magnetic coupling between the top reference layer ($RL_{top}$) and the free layer ($FL$) separated by the tunnel barrier (TB), see figure 2.12. The oscillating effect due to the unstable $RL_{top}$ undergoes four hopping phases affecting the $FL's$ magnetization orientation under a write pulse Kim et al., 2016; Yuan et al., 2023a:

- Phase 1: Due to the write pulse, the $FL$ switches its magnetization orientation accordingly.
- Phase 2: Since the magnetization of the $RL_{top}$ is not stable and not fixed, unlike $RL_{bottom}$, the layer switches its magnetization due to the transferred torque from the $FL$.
- Phase 3: The $FL$ switches again its magnetization orientation due to opposite transferred torque from the switched $RL_{top}$.
- Phase 4: The $RL_{top}$ switches again due to the transferred torque from the $FL$, resulting in an infinite cycle of these phases under a write pulse. The cycle stops at the end of the write operation.

The BH defect strength is modeled as the magnetic coupling between the $RL_{top}$ and $RL_{bottom}$, $H_P \in [0, 1]$, also referred to as the effective pinning magnetic field. This field represents the pinning strength of the top layer with the bottom layer.

## 2.3. Device-Aware Test

The device technology parameters characterize the defects due to the physical nature of the defects. However, these defects also affect the electrical parameters due to their correlations with the technology parameters. These correlations and relations are studied by L. Wu in his dissertation L. Wu, 2021. A

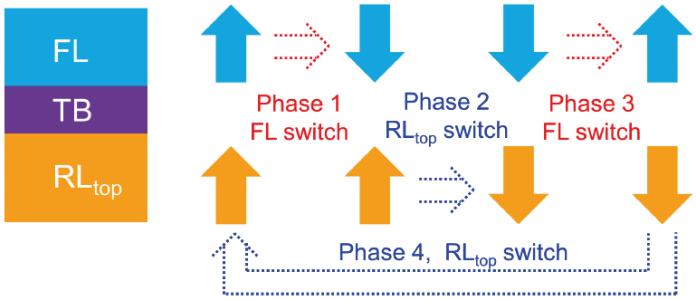



Figure 2.12: Switching stages of the $FL$ and the $RL_{top}$ in presence the Back-Hopping defect

mapping between the two types of parameters enables simulation of the impact of the physical defects at the logical level. The logical impact of the defects can deliver high-level test solutions to capture these defects. This impact of the defects at the logical level is called a fault, which can be caused by multiple physical defects. Therefore, defect type identification at the logical level remains a challenge in integrated circuit (IC) diagnosis. Traditionally, defects are modeled as linear resistors, assuming that the defects are capacitive and resistive. However, due to the magnetic properties of the MTJ, internal defects cannot be modeled as linear resistors. Device-Aware Test (DAT) is introduced Fieback et al., 2019b; L. Wu, Fieback, et al., 2020; L. Wu et al., 2022 to model the defects and their impact on the electrical parameters. The DAT approach does not only improve the test quality of the chips but also summarizes the defective nature of the defects in a compact STT-MRAM model.

The DAT approach consists of three steps:

1. Device-aware defect modeling: In this step, a physical defect is characterized and modeled physically, and the impact of the defect on the technology parameters of the defective device is determined. The technology parameters are mapped to the electrical parameters, resulting in a mapping function of the defect. The model is calibrated with measurement data from defective chips with the defect, resulting in an optimized defective MTJ compact model, see figure 2.13.

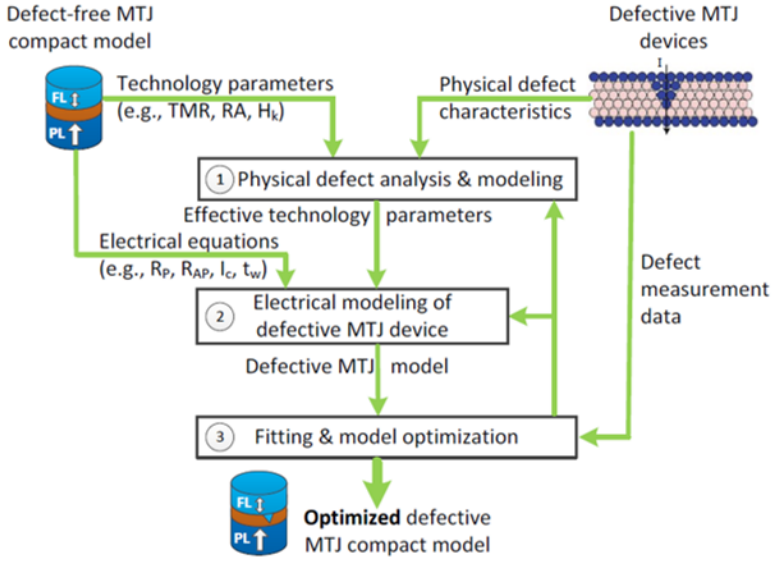



Figure 2.13: Device-Aware Defect Modeling L. Wu, 2021

2. Device-aware fault modeling: In this step, a complete fault space is defined using a fault primitive notation to cover all possible faulty states in STT-MRAMs. A fault analysis through simulations

is performed to validate faults in the presence of the defect.

3. Device-aware test development: In this step, the obtained faults are used to develop test solutions, such as March tests and DfT designs.

Device-Aware Test goes beyond the conventional test approaches by incorporating the physical behavior of the defect into the test development, resulting in more accurate test patterns and a general understanding of the unique defects. The defect models developed will help to understand the impact of defects on the key parameters of STT-MRAM. A general understanding of the unique defects and their impact on device parameters is the first step in developing diagnosis methods to identify defects in STT-MRAM defective devices. In addition, the developed methods to identify defects in this project can also be used to select defective MTJ devices to fit and optimize the defective MTJ compact model.

## 2.4. Conclusion

In this chapter, the basic principles of the MTJ storage element of an STT-MRAM are discussed to allow fundamental memory operations. The thermal stability, the TMR effect, and the STT effect are responsible for reliable data storage, reading data, and writing data to the MTJ, respectively. The correlations between these principles result in different operational regimes. The STT-MRAM internal defects are explained, and how they affect the device key parameters. The impact of defects on key device parameters is summarized in table 2.2.

| Defects | | Technology Parameters | | | | | | | Electrical Parameters | | | | | | Statistical Parameters | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Labels | Strength | $\varphi$ | $A_0$ | $M_S$ | $H_K$ | $RA$ | $TMR$ | $H_s$ | $R_P$ | $R_{AP}$ | $I_{C_r}$ | $I_{C_s}$ | $t_{W_r}$ | $t_{W_s}$ | $WER$ | $RER$ |
| PH | $\uparrow A_{ph}$ | ↑ | - | - | - | ↓ | ↓ | - | ↓ | ↓↓ | ↑ | ↑ | ↓ | ↓ | ↑ | ↑ |
| IM | $\uparrow A_{IMAP}$ | - | ↓ | - | - | - | - | - | ↑ | ↓ | ↓ | ↓ | ↓ | ↓ | ↑ | ↑ |
| SAFF | ↑ Flip | - | - | - | - | - | - | ↑ | - | - | ↑ | ↑ | ↑ | ↑ | - | - |
| BH | $\downarrow H_P$ | - | - | - | - | - | - | - | ↑ | ↑ | - | - | - | - | ↑ | ↑ |

Table 2.2: Impact of the MTJ key parameters by the defects.↑, ↓, and − signs denote increase, decrease, and no impact, respectively.

In conclusion, the fundamental understanding of the targeted defects in this thesis and their impact on the device parameters will help to define the machine learning features, model, and algorithms.

# 3

# Background on VLSI Test & Diagnosis and Machine Learning

This chapter provides a comprehensive background on Very-Large Scale Integration (VLSI) test and diagnostic procedures and their machine learning applications. VLSI is the process of developing and combining ICs. The traditional test and diagnosis procedures applied on STT-MRAM-based chips, explained in section 3.1, will give a fundamental understanding and overview to understand the current challenges in defect identification. The second part of the chapter discusses the existing machine learning applications in VLSI test and diagnosis in section 3.2. An overview of the current machine learning applications in VLSI tests and diagnosis will give us a good understanding of the current challenges in the field. It will guide us in the right direction in STT-MRAM defect classification using machine learning.

## 3.1. Test and Diagnosis Phases

Figure 3.1 shows a chip's design, test, and diagnosis process. The fabrication of a chip requires multiple stages to ensure quality and correctness. After the logical design of a chip, additional circuitry is designed that allows an efficient testing procedure of the chip after the fabrication, called structural test. Design For Testability (DFT) and logic circuitry can be designed in parallel Bushnell and Agrawal, 2004; Wang et al., 2006c. Both methods are verified and synthesized before manufacturing. Synthesis partitions the Register-Transfer Level (RTL) code into the final physical layout. The layout contains the physical cell design and interconnects, considering design constraints such as timing. The designed synthesized chip's functionality is verified before manufacturing, testing, and diagnosis Wang et al., 2009.

The manufactured prototype is characterized and validated to optimize the manufacturing process and correct the design if necessary; see section 3.1.2. After the characterization and validation step, the chip mass production is performed. Each manufactured chip is tested for manufacturing defects and chipped to the customer if it passes; see section 3.1.3. The failed chips during the test and from the customers are diagnosed to optimize the manufacturing process further and reduce the manufacturing defects, see section 3.1.4

### 3.1.1. Design & Verification

Before characterization and production testing phases, design & verification plays a critical role in ensuring the reliability and functionality of the designed chip and the testability of the chip during the production testing. The design phase aims to meet the desired performance and functionality requirements by designing the logic of the circuit using register-transfer level (RTL) code. Design for Testability aims to meet the testability standard to capture the defects or the faults as much and fast as possible during the production testing phase. It involves adding memory cells called test flip-flops that can transfer the test patterns generated by the test algorithms to the designed logic and read

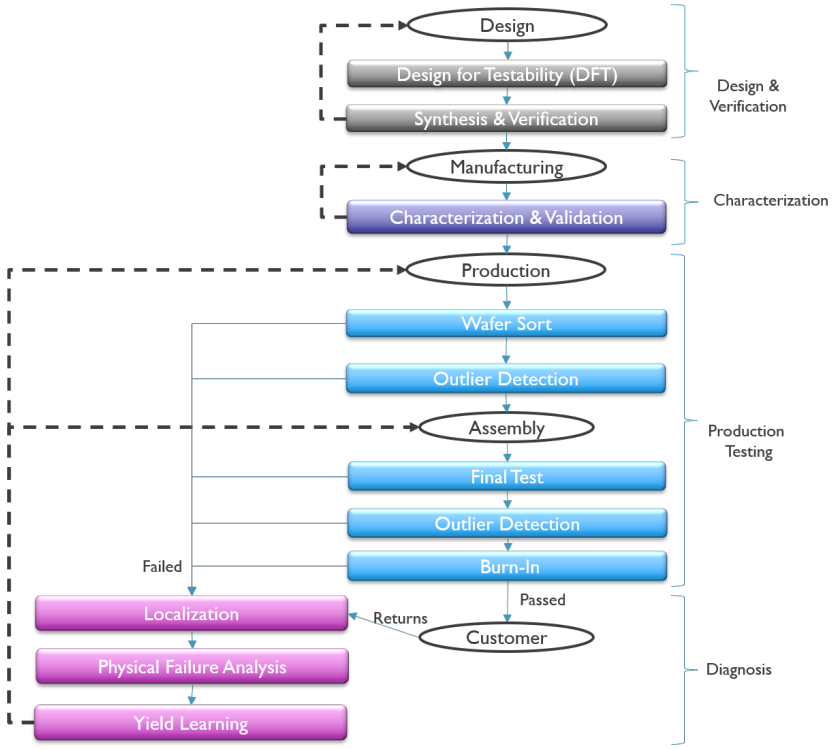



Figure 3.1: VLSI Manufacturing, Testing, and Diagnosis

its response. The circuit design and testability is verified through simulations by considering multiple unwanted scenarios where the chip might fail.

Following the design, the circuit is synthesized from a high-level representation such as RTL to a lower-level representation. The synthesized design represent the final physical layout of the chip ready to be manufactured. The layout is then further optimized through exhaustive testing and analysis to validate the chip's design and functionality before manufacturing. Design & Verification phase serve as crucial step providing a foundation for characterization phase and production testing contributing to high-quality products.

### 3.1.2. Characterization

During the validation stage of a prototype-manufactured chip, the primary goal is to ensure it functions according to its intended design and specifications. This stage involves testing the chip's functionality through functional and parametric tests. A functional test is performed to verify the functionality of a chip by executing a set of test scenarios and input patterns and evaluating the chip's responses with the expected output. Parametric test measures and verifies a chip's electrical performance parameters by applying controlled stimuli and measuring the chip's responses to evaluate characteristics such as voltage levels, currents, timing, power consumption, temperature, and other relevant parameters to ensure the chip meets the required specifications. The validation stage of the manufactured prototype plays an essential role in identifying any design issues before mass production.

Once the verification stage is completed, the chip undergoes the characterization stage focusing on understanding and documenting the chip's performance characteristics. Characterization testing involves parametric tests under different operating conditions, such as voltage and temperature variations. The results can be visualized by a shmoo plot, plotting various electrical features and showing reliable operational regions. Characterization testing aims to create or update the manufactured design's specification (spec) by analyzing the chip's performance limits and corner cases. The operational specification and performance limits give an overview of the boundary conditions for a designer to optimize the chip's integration process. It also provides the customer with insights into the use case for reliable operation in

the field. The characterization phase is essential before the production phase ensuring the manufactured design's correctness and performance Bushnell and Agrawal, 2004.

### 3.1.3. Production Testing

After the validation and characterization testing, mass production is started. The production testing phase is critical in ensuring quality and reliability before shipping the chips to the customer. Each manufactured chip is tested at different stages, including wafer sort and final test indicating whether the chips are defective or not. The objective of the wafer sort and final test is to target defects that occurred during the production and assembly of the chips, respectively. The type of test performed during these stages is called a structural test. Like a functional test, a structural test executes a set of test scenarios and input patterns and evaluates the output with the expected or simulated response. However, the key difference between functional and structural tests is that the former aims to test the function of circuitry. In contrast, the latter aims to test its structure insteadthe test patterns provided during structural test aim to detect faults caused by manufacturing defects Rinitha and Ponni, 2016. Therefore, the test development procedure for generating the desired test patterns during the structural test fundamentally differs from a functional test. The structural test aims to optimize the test time and the accuracy, while the functional test aims to optimize the accuracy only. Therefore, the structural test is performed during production testing for each chip, while the functional test is used during characterization phase for the prototype chip.

By targeting the structure of the chip instead of the functionality, the number of test patterns required for testing the chip can be reduced while keeping an acceptable accuracy. A fault is the impact of the physical defects on the logical level of a digital circuit where several defects can be mapped to the same fault. Therefore, several steps are required for test pattern generation during structural tests, including Defect Modeling, Fault Modeling, and Test Development. Defect Modeling maps the physical defect to an electrical model that enables electrical simulation of the defects. Fault Modeling, conversely, is the process of determining the electrical response during the simulations by injecting the modeled defects. This results in a fault space representing the possible faults that can occur in a circuit. Test development, as the final stage in test pattern generation, is the creation of test algorithms to generate the necessary test patterns to detect faults in the chip. However, one test pattern can map to several faults, such as that one fault can cover multiple defects. The algorithms that generate the desired test patterns are used during wafer sort and final tests to target as many faults as possible Bushnell and Agrawal, 2004. Figure 3.2 illustrates the key difference between functional and structural tests of an OR gate, with oxide breakdown as the physical defect and Stuck-at-0 as the fault.

Wafer sort aims to target defects during the wafer fabrication in each chip using a combination of the structural and parametric tests at the wafer level. On the other hand, the final test aims to target defects that occurred during assembly for each packaged chip using the structural test. The wafer sort and final test processes are automatized using Automatic Test Equipment (ATE) that runs the developed test algorithms for test pattern generation. While the defective chips are screened out through these tests, some faulty chips can pass the tests, and some non-defective chips can fail the test, known as test escapes and yield loss, respectively. Researchers aim to minimize the test escapes by improving the defect modeling and yield loss by developing better test solutions. Test escapes can also be reduced by outlier detection methods performed after the tests. It aims to screen out the chips that passed the tests but still exhibit outlier behavior by analyzing the test results and other relevant features. This stage will ensure that only chips meeting the quality standards proceed further at the expense of losing yield. The chips may also undergo burn-in tests by exposing the chips to high-stress conditions such as voltage and temperature variations to ensure the chip's reliability in the field. Now the passed chips are shipped to the customers, and the failed chips are diagnosed to understand the cause of the defectiveness.

### 3.1.4. Diagnosis

The diagnosis phase plays a vital role in understanding the root causes of chip failures to improve the manufacturing process. The diagnosis aims to improve the yield and reduce the number of failed chips in the future by analyzing the customer returns and failed chips to identify the defects or faults causing

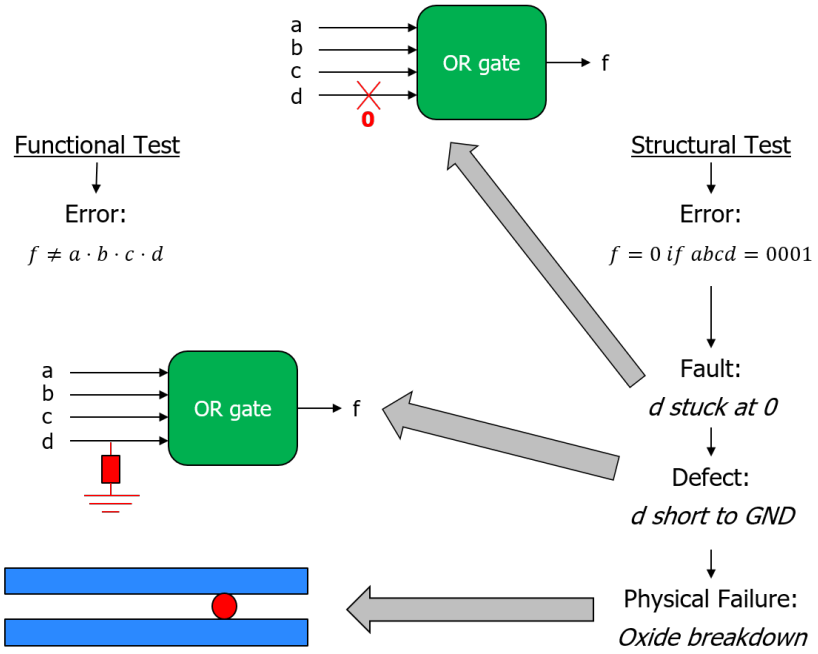



Figure 3.2: Functional vs Structural Test Philosophy

their failure. Through this process, valuable insights can be gained into the weaknesses of the production process to improve the overall yield D. Vallett, 1997. The diagnosis involves localization, PFA, and yield learning. Localization is a key step to pinpoint the location of the defects within the failed chip utilizing the failed test responses from the structural tests. Typically, automated diagnosis algorithms are used for localization by analyzing the scan flip-flops and the corresponding failed test responses. However, other techniques, such as built-in self-test (BIST), are also used. Researchers aim to improve the diagnostic resolution to minimize the candidate locations responsible for the failure Tang, 2010; L. C. Wagner, 1999b.

After the candidate locations are determined, PFA is performed to identify the root cause of the chip failure within the candidate locations Chin et al., 2011. PFA techniques may be destructive, time-consuming, and require specialized equipment, including SEM, Focused Ion Beam (FIB), Decapsulation, and electrical measurements Y. Li and Goyal, 2020; Y. Li et al., 2016; Soden and Anderson, 1993. FIB is a destructive technique that uses a focused beam of ions to remove material from the sample and enable manual examination physically. SEM is a non-destructive technique that can identify defects such as cracks and voids and is used to analyze the surface morphology of failed chips using images generated by the focused electron beam. Decapsulation removes the packaging material that encapsulates using acid etching, for example, by carefully removing the package without damaging the chip allowing direct examination of the die. Lastly, electrical measurements such as power analysis and functional tests are used to pinpoint abnormal behavior in the electrical responses, such as current spikes and timing violations.

Therefore, improving the diagnostic resolution during localization is imperative to reduce costs and guide PFA. There are several methods to guide PFA, such as fault diagnosis. Fault diagnosis aims to identify the candidate faults responsible for the failure in the candidate locations. The fault diagnosis utilizes the failed test responses and their corresponding test input by extracting features to improve the diagnostic resolution and reduce the number of candidate faults. The diagnosed root cause of chip failures and the failed test results are analyzed to improve the production process and increase the yield continually. The information collected from customers, test results, and PFA is used to refine the production process and optimize the yield, known as yield learning. Through iterative analyzing failed chips, locating defects, conducting PFA, and optimizing the manufacturing process, valuable insight can be gained to increase the yield and improve chip quality.

## 3.2. Machine Learning in VLSI Test & Diagnosis

Machine learning has shown great potential in diagnosing and testing chips and other fields. With the increasing complexity of ICs, conventional approaches for testing and diagnosing chips have become more expensive. Machine learning offers a data-driven and automated approach to analyzing large amounts of chip data and extracting valuable insights for test and diagnosis. For example, machine learning models can be trained on labeled datasets containing known characteristics for classification. Machine learning can also help detect anomalies and deviations. Overall, machine learning allows the detection of abnormal behaviors in chips based on the data distribution and the classification of chips based on a set of labels. Machine learning algorithms can handle large datasets and recognize complex patterns, leading to more efficient and effective processes in the chip manufacturing process. This section will discuss machine learning principles and applications in VLSI tests and diagnosis.

### 3.2.1. Machine Learning Principles

Machine learning is a field that focuses on developing models and algorithms that allow a machine to make predictions or decisions. The machine is trained through learning by extracting meaningful patterns from large data. The learning process can be categorized into supervised, unsupervised, and reinforcement learning. Supervised learning aims to train a machine learning model's internal parameters using a labeled dataset and machine learning algorithms to minimize the error between predicted and actual labels. The model is trained using labeled training data and evaluated using labeled test data. On the other hand, unsupervised learning maps the dataset to a machine learning model and uses machine learning algorithms to extract patterns and meaningful insights. The model is trained using unlabelled training data but is not evaluated using unlabelled test data. Reinforcement learning trains an agent to learn from its environment over time and eventually determine the most efficient action that maximizes the rewards using a predefined set of states, rewards, and actions.

Supervised learning is divided into regression and classification, while unsupervised learning is divided into density estimation, clustering, and dimensionality reduction Stratigopoulos, 2018, see figure 3.3. The objective of each machine learning type is explained as follows:

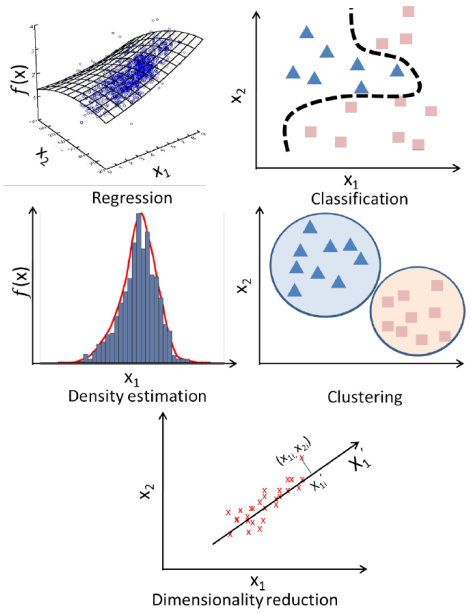



Figure 3.3: Machine learning Types Stratigopoulos, 2018

- Classification: the goal is to classify data based on their features on predefined labels. The machine learning model is trained using a large labeled dataset to classify unlabelled data.

- Regression: similar to classification, regression is used to predict the numerical output value of the trained model rather than labels. The machine learning algorithm learns from labeled training data to create a numerical relation between the input features and the output variable.
- Density Estimation: density estimation is used to estimate the probability distribution of a dataset to understand the characteristics, generate new samples or detect anomalies and outliers.
- Clustering: clustering algorithms group data entries together based on their feature values and patterns in the data. The goal is to create clusters of data entries with similar characteristics without supervision and used to predict the cluster type of unseen data.
- Dimensionality Reduction: the objective is to reduce the number of input features of a dataset without losing essential information. The techniques can be used to reduce data feature dimensions, identify important features or identify outliers.

The model's complexity, representation, and generalization are three key principles that impact machine learning performance. These principles reduce issues such as over-fitting and under-fitting and enable the trained model's ability to generalize well for unseen data while minimizing training errors. Under-fitting and over-fitting refer to the fact that the size of the training dataset depends on the number of features, the higher the number of features, the bigger the dataset. In general, data can be better represented with a high number of representative features or dimensions, leading to an accurately trained machine learning model. However, this may lead to low model generalization to unseen and unlabelled data. Therefore, the trained model should balance between the number and type of features and training accuracy by allowing some errors during training to generalize better for unseen data. These key principles are explained as follows:

- Complexity: The curse of dimensionality refers to the fact that increasing the number of features or the complexity of the model will lead to a model that is well-trained on the training data but may not work well for test data or unseen data, see figure 3.4. The model's complexity is also increased with the output size, such as the number of labels for classification.
- Representation: A representative feature set is crucial to guide the training process and increase training and test accuracy. Therefore, the machine learning model's input features should be chosen wisely to represent the training and unseen data. The process of selecting features is also referred to as feature engineering.
- Generalization: the art of balancing between training errors and test errors does not only depend on the number and type of features but also depend on the training dataset. First, the training dataset should be balanced between the labels. Secondly, the training dataset should be large enough to avoid under-fitting and small enough to avoid over-fitting.

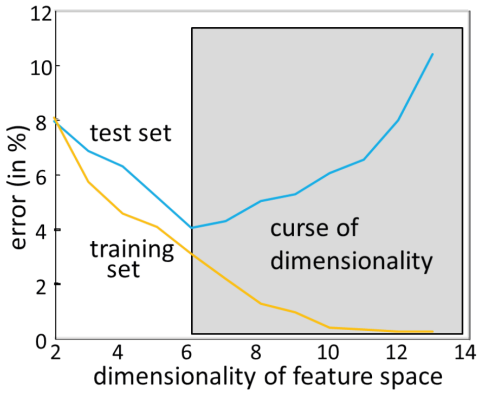



Figure 3.4: Training vs Test Error as function of Complexity Stratigopoulos, 2018

In summary, machine learning aims to learn from data, discover patterns, and make predictions or decisions through statistical analysis, machine learning algorithms and models. Moreover, training an

accurate, effective, and generalized machine learning model introduces several challenges. The size and distribution of the training dataset, the number and type of features that represent the input data, and the number of labels should be considered to design a balanced and representative machine-learning model. Overall, machine learning has great potential for various applications that handle large amounts of data for classification, regression, dimensionality reduction, clustering, and density estimation.

### 3.2.2. Machine Learning in VLSI Test

Testing chips have several stages, as discussed in section 3.1. Figure 3.6 n shows a summary of machine learning applications in each stage of the VLSI test and diagnosis phases. Machine learning applications in testing chips are categorized and explained as follows:

- Outlier Detection: as discussed in section 3.1, outlier detection is used during production testing to screen test escapes after wafer sort and final test. The assumption is that most passed chips are not test escapes, allowing machine learning algorithms to be used, such as density estimation for outlier detection. Data driven approaches Daasch and Madge, 2005 and supervised learning approaches using variational auto-encoders based on neural networks Shintani et al., 2018 are examples for such applications.

- Wafer-level Test: The goal is to exploit die-to-die correlations at the wafer level to reduce test cost by implicitly predicting the performance of untested dies. The prediction model is trained using standard test approaches with a few explicitly tested dies. Unsupervised machine learning techniques such as clustering or density estimation can be used to implicitly predict a chip's performance. Example is supervised learning using neural networks to implicitly identify test escapes based on explicitly tested chips Xanthopoulos et al., 2020.

- Alternate Test: The alternate tests aim to reduce test costs by partially replacing the standard tests for specific chips. The idea behind the method is to predict the chip's performance based on alternative low-cost measurements without applying functional or structural tests. The standard test approaches are only used when the prediction results are unconvincing. Supervised machine learning techniques such as classification for digital circuits and regression for analog circuits are suitable to test chips based on low-cost features. Paper Stratigopoulos and Mir, 2012 presents the framework for alternate testing using two predictive models, regression to estimate the performance parameters and classification as filters to predict whether the die can be used for regression or evaluated by the conventional test approaches.

- Adaptive Test: during functional and structural tests, the chip under test is exposed to several test patterns and conditions. Adaptive test is an approach that dynamically adjusts the test pattern generation and test conditions based on previous test responses from the Chip Under Test (CUT). Reinforcement learning is suitable for this task because of its ability to learn from its environment in real-time and take appropriate actions Maxwell, 2011.

- Test Compaction: test compaction aims to reduce the number of test patterns, reducing test time while maintaining high fault coverage or test accuracy. Machine learning can identify redundant test patterns by learning from a large set of vectors using techniques such as dimensionality reduction that maps certain features to a lower set of features Z. Li et al., 2017.

- Circuit Testability: as discussed in section 3.1, for structural tests, test Flip-Flop (FF)s or test memory cells are inserted in the circuit to provide test patterns and read the test responses. Machine learning techniques are deployed to insert test points to maximize a circuit's testability Pradhan et al., 2018 instead of manual or deterministic insertion.

In summary, machine learning shows great potential to reduce test time and test escapes by supporting existing test approaches. From the current machine learning applications in VLSI testing, machine learning is very effective in guiding the conventional test methods instead of replacing them using historical test data of other chips. However, machine learning does show potential to replace current outlier detection methods for detecting test escapes mainly because machine learning models and algorithms can exploit correlations in datasets that the conventional methods may not cover for detecting outliers.

### 3.2.3. Machine Learning in VLSI Diagnosis

In addition to machine learning applications in testing chips, there are several machine learning applications to increase diagnosis time and accuracy, see figure 3.6. The machine learning application in VLSI diagnosis can be summarized as follows:

- Fault Diagnosis: fault diagnosis is a key process in identifying and localizing faults in integrated circuits. Traditionally, fault diagnosis methods involve analyzing test responses to reduce the time required to pinpoint faulty parts. Supervised machine learning algorithms train labeled datasets using features extracted from the test responses to various test patterns; see figure 3.5. The trained model can calibrate and diagnose faults on unseen datasets from new defective chips with corresponding test responses Gómez and Wunderlich, 2016. However, the defect type responsible for the fault can be diagnosed further to understand the underlying cause of the faulty behavior. Bridge defect types can be classified using a decision forest, and features extracted from the netlist and test results of the diagnosed chips Nelson et al., 2010. Defects such as void, open, and short in Trough-Silicon Via (TSV) can be classified using K-Nearest Neighbor (KNN) and a Random Forest Y.-J. Huang et al., 2018. The models used in these two applications are supervised and trained by simulation data.

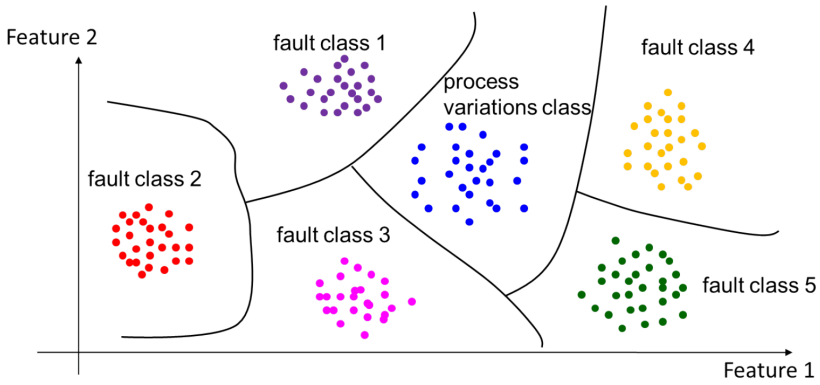



Figure 3.5: Fault classes classification representing defective behavior Stratigopoulos, 2018

- Wafer-level Diagnosis: Wafer-level diagnosis involves diagnosing the failures on the entire wafer. The assumption is that the defects occur in clusters on the wafer containing multiple dies. These clusters can be detected at the early stage of the diagnosis process. Unsupervised learning such as kernel-based clustering is used to identify the defective clusters Sumikawa et al., 2017.
- Volume Diagnosis: the volume diagnosis extends the localization and identification process by analyzing large amount of defective chips and find common faulty behaviours. Detected systematic defects are used to learn yield and tune the manufacturing process. Machine learning models such bayesian learning can be used to identify the common defective features Cheng et al., 2017. The assumption is that the distribution of defective features from large amount of data gives an indication of systematic defects.
- Scan-chain Diagnosis: scan-chain diagnosis aims to locate the faulty scan memory cells. Scan memory elements are used to insert and read the test patterns and the response vectors, respectively. The goal is to identify the faulty scan flip flops instead of the faults inside the logical modules. Unsupervised learning based on bayesian learning with unknown priors can be used to identify the faulty scans Y. Huang et al., 2008.
- Board-level Diagnosis: the board-level diagnosis aims at locating and identifying the faults presented on the entire board instead on the individual components. Supervised learning techniques can be used to identify the faulty components and connections on the board using historical data Ye et al., 2013.

Machine learning shows great potential to reduce diagnosis time and increase diagnostic resolution and accuracy. Existing methods can be replaced with predictive models by utilizing the test results of the

defective chips and historical diagnostic data of other faulty chips. However, diagnosis based on machine learning requires considerable data from simulation, experiments, or historical data. In addition, the diagnosis resolution and accuracy may be affected by the probabilistic nature of the machine learning models and algorithms. Therefore, many applications still rely on traditional approaches when machine learning predictions are less confident.

## 3.3. Conclusion

This chapter introduced integrated circuits and chips' testing and diagnostic phases and their machine learning applications; see figure 3.6 for a summarized overview. It also covered the basics and principles of machine learning and VLSI testing and diagnosis. This background information gives a fundamental and intuitive understanding of the thesis topic and presents gaps for exploration.

Fault diagnosis is the closest to the thesis objective; defect identification and classification of STT-MRAM defects using machine learning. Fault diagnosis methodologies classify faults or fault classes instead of defect types. However, two machine learning applications Y.-J. Huang et al., 2018; Nelson et al., 2010 have shown that it is possible to classify certain defect types from the test results and parametric tests instead of faults.

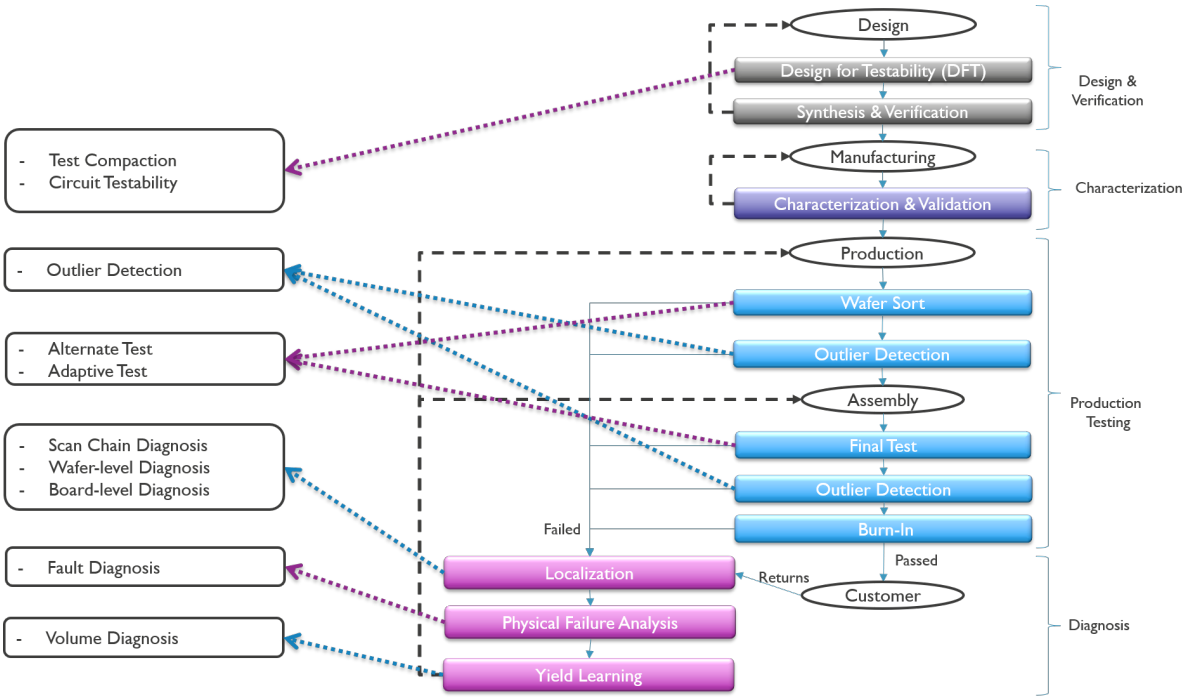



Figure 3.6: Machine Learning Applications in VLSI Test and Diagnosis

# 4

# Diagnosis Methodologies

This chapter proposes two methodologies for defect identification and classification in STT-MRAM devices: DAT-based Diagnosis and Machine Learning-based ML-based Diagnosis. Section 4.2 focuses on an automated method to identify defects using identifying features extracted from measurements. The specified features are derived from the background study performed in chapter 2, where the impact of the defects on the MTJ parameters is studied. The identified defective devices will be labeled training data for supervised machine learning. Section 4.3 explores machine learning techniques and features to classify defects using low-cost measurements. This idea originated from the literature study conducted in chapter 3 by combining Fault Diagnosis and Alternate Test underlying philosophies. By combining defect identification using identifying features and defect classification using low-cost features, structured, automated, and unique methods are developed to diagnose STT-MRAM defects. The experiments, analysis, and evaluation of these methodologies are discussed in the next chapter 5.

## 4.1. Overview

The literature and background study discussed before introduced a research gap in defect identification and classification and showcased potential solutions. This thesis aims to develop and optimize methodologies for defect identification and classification in STT-MRAM technologies by balancing precision and cost-effectiveness. The existing methodologies are either not sufficiently accurate or too costly regarding the measurements and analysis required, as discussed in chapter 1. More efficient and intelligent methods for defect identification and classification in emerging memory technologies are required to improve and speed up the diagnosis process. The proposed approaches in this thesis aim to navigate between maximizing detection accuracy and minimizing measurement and analysis costs where existing methodologies might need to be more effective and efficient for STT-MRAM devices. Two methodologies are introduced in this chapter, DAT-based Diagnosis and ML-based Diagnosis, to identify and classify Pinhole (PH), Intermediate State (IM), SAF Flip (SAFF), and BH (Back-Hopping) defects in STT-MRAM devices.

The DAT-based Diagnosis approach is a structured method to label STT-MRAM devices with defect types using identifying features extracted from specialized measurements. The identifying features are derived from understanding the impact of defects on MTJ parameters and their evolution over quantities like time. DAT-based Diagnosis aims to identify the defect types during diagnosis as accurately as possible from electrical measurements. On the other hand, ML-based Diagnosis leverages machine learning to classify defects using MTJ features extracted from low-cost measurements. This approach utilizes the correlations and patterns between the low-cost MTJ features and the defect types. ML-based Diagnosis aims to identify the defect types during diagnosis by making a trade-off between measurement costs and accuracy. These methodologies offer a framework for diagnosing defects in STT-MRAM devices with their strengths and challenges. Figure 4.1 illustrates the two methodologies with features extracted from the measurements as input and the defect labels as output. $R$, $H$, $WER$, and $t$ denote the resistance, applied magnetic field, write error rate, and time, respectively.

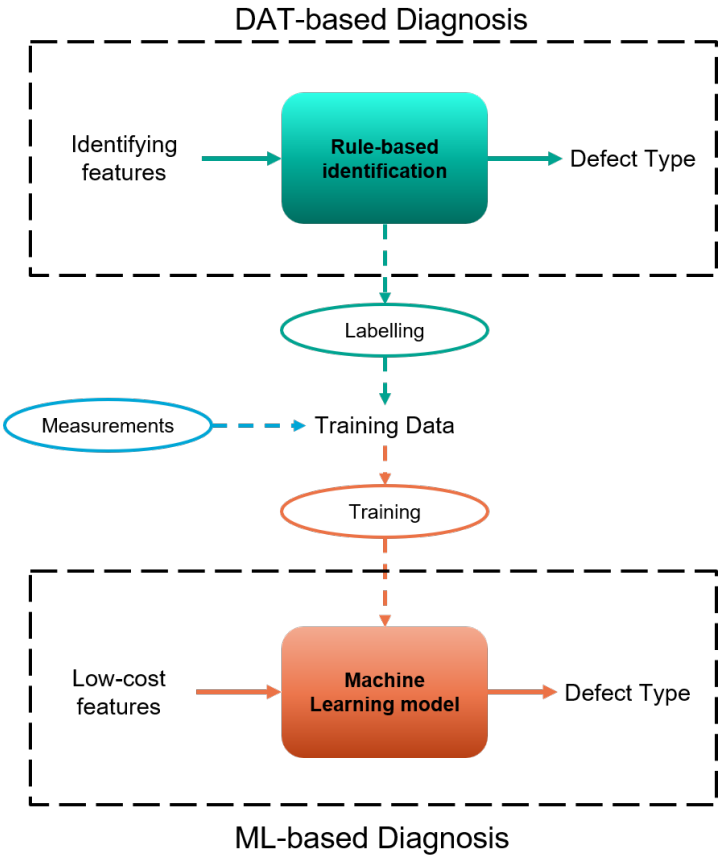



Figure 4.1: ML-Based Diagnosis vs. DAT-based Diagnosis

## 4.2. DAT-based Diagnosis

This section introduces the defect identification method using a systematically developed method called DAT-based Diagnosis used to label the STT-MRAM devices with their corresponding defective type. The objective is to identify distinguishing features that characterize specific defects and label the data using these features. By understanding how defects manifest themselves in the MTJ key parameters, we can extract identifying features that serve as indicators for defect identification. Relevant data required for defect identification are collected by electrical measurements developed for each defect. These data of STT-MRAM devices can be processed to extract the identifying features using fitting functions automatically. The threshold values for the identifying features are then applied as a decision to determine the defect type of an MTJ device. The DAT-based Diagnosis procedure to develop the defect identification system can be summarized as follows:

1. Feature identification: This step identifies distinguishing features for each defect based on understanding the defect's impact on the STT-MRAM key parameters and how these effects evolve over time or other relevant quantities.

2. Feature selection: This step combines the identified distinguishing features from the previous step into one identifying feature for each defect.

3. Feature extraction: Fitting functions that mathematically describe the impact of the defect on the MTJ are determined to extract the identifying feature for each defect automatically.

4. Defect identification: The identifying feature is eventually used to label the devices with the corresponding defect types. The threshold values that serve as a condition for determining the presence of the defects for the identifying features are determined theoretically and experimentally.

### 4.2.1. Feature Identification

In the first step, distinguishing features are identified for each defect through the following two steps:

1. Investigation of the impact of the defects on MTJ parameters.
2. Identification of features that describe the defective behavior of defects.

The defects are characterized by technology parameters instead of electrical and statistical parameters. Therefore, the technology parameters are prioritized for accurate defect identification. The characteristics of the targeted defects and their impact on the MTJ key parameters are discussed in section 2.2 and illustrated in table 2.2. More investigation is required to understand the defective behavior of the defects to identify distinguishing features per defect type. The identified features of the targeted defects are summarized in table 4.1.

Pinhole defect is modeled as the area of the tunnel barrier containing the pinhole by Device-Aware Test L. Wu, 2021. The growth of the pinhole area affects different technology parameters, especially the resistance-area product, and the barrier height, see table 2.2. Therefore, the distinguishing feature that can be extracted is the growth of the pinhole area over time L. Wu et al., 2019, $\uparrow A_{ph}(\uparrow t)$.

Intermediate State defect is modeled as the area of the domains that are not switched during the write operation L. Wu, 2021. However, the intermediate states occur probabilistically over time as depicted by the MTJ compact model L. Wu et al., 2021. Therefore, the resistance over time during write operations from low to high state and vice-versa is considered as a distinguishing feature for Intermediate State defect, $R(t) = P_{IM}(t) \cdot R_{IM} + (1 - P_{IM}(t)) \cdot R_P$ where $R_{IM}$ and $P_{IM}(t)$ denote the intermediate state resistance and the number of occurrence of the intermediate states over time, respectively.

Synthetic Anti-Ferromagnetic Flip defect does not only affect the offset field $H_{offset}$ but also flips the magnetization orientation of the FL and the RL. The flip of the layers results in a flip of the hysteresis loop when applying an external magnetic field L. Wu, Rao, Taouil, et al., 2020. Therefore, the direction of the hysteresis loop is considered a distinguishing feature for SAF Flip defects, $H_{dir}$.

Back-Hopping defect impacts the Write Error Rate ($WER$) as depicted in table 2.2. WER increases in the presence of the defect with respect to the write voltage Yuan et al., 2023b. Therefore, another distinguishing feature of the Back-Hopping defect is the growth of WER over bias voltages, $\uparrow WER(\uparrow V_{bias})$.

| Pinhole | Intermediate State | SAF Flip | Back-Hopping |
|---|---|---|---|
| $\downarrow RA$ | $\downarrow A_0$ | $\uparrow H_{offset}$ | $\uparrow WER(\uparrow V_{bias})$ |
| $\uparrow \varphi$ | $R(t)$ | $H_{dir}$ | |
| $\downarrow TMR$ | | | |
| $\uparrow A_{ph}(\uparrow t)$ | | | |

Table 4.1: Identified features

### 4.2.2. Feature Selection

In this step, a feature for each defect is determined by selecting or combining identified features from the previous step. The selected identifying features are not technology-dependent but rather dependent on the effect of the defects on the behavior of the devices. The selected identifying feature for each defect is summarized in table 4.2.

PH The growth of pinhole area over time can be tracked by the change of $RA$, $TMR$, and $\varphi$ over time. However, according to the summarized relations of the MTJ parameters illustrated in chapter 2 figure 2.7, $RA$, $TMR$ and $\varphi$ depend on both $R_P$ and $R_{AP}$. Therefore, to combine these features into one identified, the decay of $R_{AP}$ over time is chosen as the identifying feature, $\alpha_{R_{AP}}$. Choosing the decay of all the parameters would be redundant and the decay of $R_{AP}$ would be more noticeable. It expected that the decay $R_{AP}$ would be higher than the decay of $R_P$ due to the fact that $TMR$ decreases too,

$\downarrow\downarrow R_{AP} = \downarrow R_P \cdot (1 + \downarrow TMR)$.

IM The probabilistic nature of Intermediate State defect can be characterized by the number of occurrences of intermediate resistive states over time $P_{IM}(t)$. It is assumed that the probability of intermediate resistive state occurring converges to one probability, $\lim_{t\to\infty} P_{IM}(t) = P_{IM_0} \to P_{IM}$. Therefore, the intermediate state's identifying feature is chosen to be that probability, $P_{IM}$.

SAFF Both the direction of the hysteresis loop and the offset field flips or changes, respectively, in the presence of SAF Flip defect. The direction of the hysteresis loop is selected to be the identifying feature of the SAFF defect instead of including the offset field. Measuring the direction of the hysteresis loop is much cheaper than measuring the offset field in terms of the number of measurement cycles required to extract this feature. Additionally, choosing one of those two features is enough to identify the SAFF defect, hence reducing redundancy.

BH In the case of the Back-Hopping defect, the growth of WER over bias voltages is the only identified distinguishing feature. Therefore, the growth of $WER$ over bias voltages denoted as $\alpha_{WER}$ is the identifying feature.

| Pinhole | Intermediate State | SAF Flip | Back-Hopping |
|---|---|---|---|
| $\alpha_{R_{AP}}$ | $P_{IM}$ | $H_{dir}$ | $\alpha_{WER}$ |

Table 4.2: Unique Identifying feature per defect

### 4.2.3. Feature Extraction

The unique identifying features determined above are automatically extracted by mathematical fitting functions and algorithms from the raw measured data. First, the relations between the quantities relevant to the identifying features are studied. These relations are used as fitting functions to automatically extract the fitting parameters. Finally, the identifying features are determined based on the fitting parameters.

Pinhole The decay of $R_{AP}$ is described by equation 4.1 where $a$, $b$, and $c$ are the fitting parameters. It is assumed that the pinhole decay can be modeled as an exponential function and is motivated by the physical phenomenon where certain defects, like pinhole, exhibit exponential decay behavior over time L. Wu, 2021. The fitting parameters $a$ and $b$ are used to calculate the identifying feature. Since the parameters $a$ and $b$ represent the starting value and the decay of the exponential function, respectively, and $c$ only the end value, the identifying feature of the pinhole defect is calculated as $\alpha_{R_{AP}} = a \cdot b$.

$$R_{AP}(t) = a \cdot e^{-b \cdot t} + c \tag{4.1}$$

IM $P_{IM}$ is extracted by an outlier detection algorithm given the raw data of each device as shown in the pseudo-code 1. The algorithm developed receives raw data and determines the number of occurrences of intermediate states in the $R_P$ range. The measurements required to generate these data are as follows:

1. Write 0 to set the MTJs in the low resistive state
2. Write 1 to set the MTJs in the high resistive state
3. Repeat these operations for a fixed number of cycles.

The algorithm is developed in several steps:

1. Set the maximum tolerant threshold to identify a resistive value as an intermediate state, which is set to be 0.6% L. Wu, 2021.

2. Determine the $R_{AP}$ and $R_P$ values of the devices by calculating the median of each resistive range.
3. Compare the values with the set threshold to identify the intermediate states and calculate the identifying feature $P_{IM}$.

Algorithm 1 Extracting Intermediate State Probability ($P_{IM}$)

```
procedure ExtractPim(devices)
    for each dev in devices do
        mini ← min(ydata_set + ydata_reset)
        maxi ← max(ydata_set + ydata_reset)
        mid ← mini + ((maxi − mini)/2)
        thres ← 0.0001
        rps ← []
        for each y_set, y_reset in zip(ydata_set, ydata_reset) do
            if y_set < mid then
                rps.append(ys)
            end if
            if y_reset < mid then
                rps.append(yr)
            end if
        end for
        out_rps ← score(rps, mid, three)
        P_IM ← len(out_rps)/len(rps)
    end for
end procedure
procedure score(data, mid, thr)
    outliers ← []
    median ← median(data)
    threshold ← median + thr × (mid − median)
    for each d in data do
        dev ← abs(d − median)
        if dev > threshold then
            outliers.append(d)
        end if
    end for
    return outliers
end procedure
```

SAFF The SAFF defect can observed from Resistance-Magnetic Field (RH) hysteresis loops where R denotes the resistance of the MTJ and H the applied magnetic field. A defect-free device will result in a hysteresis loop, which can be described by four sigmoids, two for the positive part and two for the negative range. However, in order to observe SAFF defect where the hysteresis loop is flipped, only two sigmoid are required, one for the negative and one for the positive range. The direction of the hysteresis loop $H_{dir}$ is described by two sigmoid functions fitting a half RH-loop, one function for the positive H field and the other for the negative part with $a_i$, $b_i$ and $c_i$ as the fitting parameters where $i$ denote the positive and negative region of the loop, see equation 4.2. Only the fitting parameter $a_i$, which denotes the sign of the equation, is used to extract $H_{dir}$, $H_{dir} = sign(a_1) \wedge sign(a_2)$. Additional parameters are extracted from the two fitting equations, $R_P$, $R_{AP}$, $H_{sw_p}$ and $H_{sw_n}$, which will be discussed in the next section for ML-based Diagnosis.

$$R_i(H) = \frac{a_i}{1 + e^{-H-b_i}} + c_i \quad \text{with } i = [1, 2] \tag{4.2}$$

BH The growth of WER by increasing the write voltage indicates the presence of the Back-Hopping defect. This growth is assumed to be following a power function through the understanding of the defect from literature Yuan et al., 2023b. The growth of $WER$ over bias voltage is described by equation 4.3 with $a$ and $b$ as the fitting parameters. The fitting parameter $a$ represents the scaling factor or the point where the $WER$ starts increasing. Fitting parameter $b$ denotes the exponent or the rate $WER$ increases. Both the parameters represent the Back-Hopping defect strength. Therefore, the identifying feature is extracted from the fitting function as $\alpha_{WER} = a \cdot b$.

$$WER(V) = a \cdot (-V)^b \tag{4.3}$$

### 4.2.4. Defect Identification

The defects are identified by providing thresholds to the identifying features as a condition for the MTJ to contain the corresponding defect type. Defect identification is performed in two different approaches:

- Theoretically: Identify the theoretical range of the identifying features in defect-free cases if applicable. The objective is to find the values for $\beta_i$, which represent the conditional threshold for the identifying features, $f_i$, to determine the defect type. For example, a device contains the pinhole defect if $f_{PH} = \alpha_{R_{AP}} > \beta_{PH}$.
- Experimentally: Performing one-class classification using unsupervised machine learning to determine the final range if theoretical analysis cannot determine the thresholds. Applying a one-class classification algorithm aims to capture defect-free devices using unsupervised machine learning. The boundaries of the resulting cluster in a feature space, including all the measured and extracted features, will determine the range of the identifying features. Figure 4.2 illustrates the concept where the features $f_i$ represent all the identifying features and the low-cost features measured for the ML-based Diagnosis.

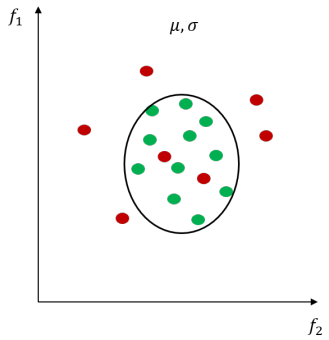



Figure 4.2: One-Class Classification

One-class classification models are designed and will be used to work with only one data class, the defect-free devices. The models learn to distinguish between the majority class (defect-free) and the outliers (defective). It is assumed that the majority of the measured devices are defect-free. For this purpose, various one-class classification algorithms and models are selected and compared as shown in figure 4.3, each with unique advantages and disadvantages to the defect-free class. The trained boundaries of the defect-free class in the complete feature space will denote the thresholds for the identifying features based on the measured data by evaluating the selected one-class machine learning algorithms.

| Methods | Description | Advantages | Disadvantages |
|---|---|---|---|
| **Elliptic Envelope** | Probabilistic model that fits an ellipse | • Can handle high dimensions<br>• Efficient in close outlier detection | • Assumes Gaussian distribution<br>• Cannot handle complex distribution |
| **Isolation Forest** | Tree-based algorithm that partitions the data points | • Can handle complex distributions<br>• Efficient in high dimension | • Inefficient with correlated features<br>• Inefficient with small outlier dataset |
| **One-class SVM** | SVM-based model that fits an optimal hyperplane | • Can handle complex distributions<br>• Efficient in far outlier detection | • Cannot handle high dimensions<br>• Sensitive to the learning parameters |
| **LOF** | Density-based algorithm by comparing the densities of the data points | • Can handle dataset with small outliers<br>• Efficient in close outlier detection | • Cannot handle high dimensions |

Figure 4.3: Comparison between different one-class classification machine learning methods

### 4.2.5. March-Based Diagnosis

The proposed DAT-based Diagnosis utilizes the measured identifying features to identify the defect types. Many industrial chips do not provide the option to measure analog values from the memory array due to the built-in Sense Amplifier (SA); see figure 4.4. Sense amplifier converts the analog read voltage from the memory cells to logical values 1 or 0 using a reference voltage to distinguish between low and high memory states. Therefore, additional circuitry is necessary to measure the feature values. For example, measuring $\alpha_{R_{AP}}$ requires read operations to measure high state resistive value $R_{AP}$ over time. March-based Diagnosis proposes an approach to identify the defect type based on the logical values by adjusting the DAT-based Diagnosis methodology. A March test is a family of memory testing algorithms used to detect and identify faults or defects in memory chips. The purpose of a March test is to ensure that memory cells operate correctly and reliably. A paper based on this industrial approach is written and accepted; see appendix A.

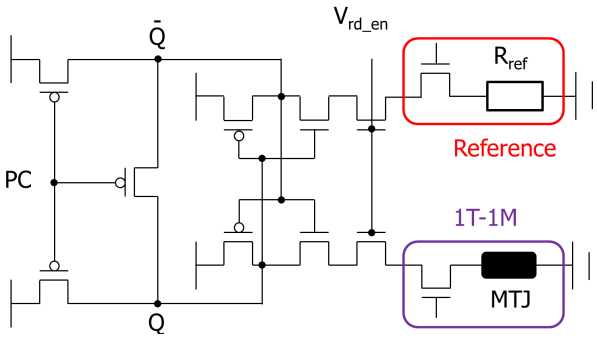
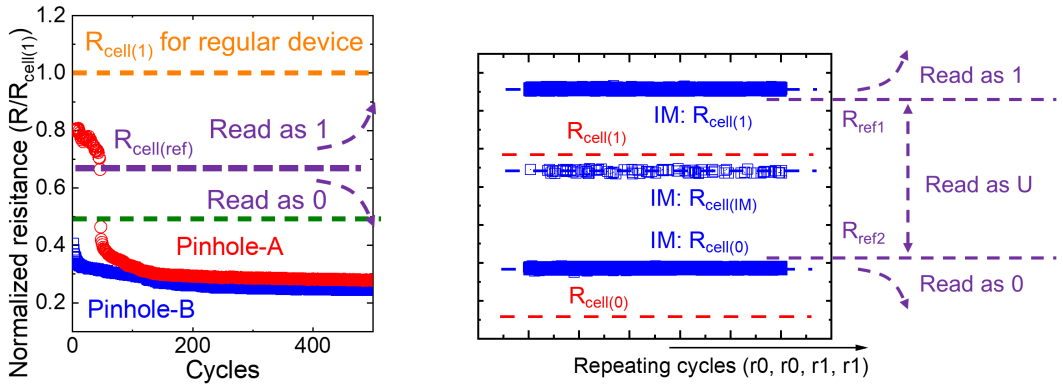



Figure 4.4: Sense amplifier structure

PH Pinhole defect is identified by the feature $\alpha_{R_{AP}}$ representing the $R_{AP}$ decay over time using DAT-based Diagnosis. $R_{AP}$ decay over time cannot be measured due to the built-in analog-to-digital converter in many industrial chips. Therefore, the decay of $R_{AP}$, $\alpha_{R_{AP}}$, should be captured from the $R_{AP}$ digital values. The following march algorithm should be applied $M = \{\Updownarrow (w1, r1)^i\}$ where $M$, $\Updownarrow$, $w1$, $r1$ and $i$ denote the algorithm, that addressing direction is irrelevant, write 1 operation, read operation where 1 is expected and the number of iterations, respectively. However, the effectiveness of this march algorithm depends on the SA structure and the defect strength. This method applies the regular read SA in Fig. 4.5 (a); when the cell resistance is larger than $R_{ref}$, it is read as 1. Otherwise, it is read as 0. For the two Pinhole-defective devices depicted in figure 4.5 (a), only device-A can be diagnosed; the read operations initially provide correct results, followed by incorrect results, with the repeating number

increase. Yet, if the Pinhole-defective cell resistance. If initially lower than $R_{ref}$ (e.g., device-B), read operations initially offer the wrong result, making it impossible to distinguish between Pinholes and other defects. Applying multiple reference resistors in the SA may diagnose a broader range of Pinholes, but it never guarantees to diagnose all Pinholes.




(a) $R_{AP}$ decay over time with a reference resistance to distinguish between 1 and 0

(b) Two reference resistances to distinguish between the intermediate state $R_{IM}$ and the logical states 1 and 0

Figure 4.5: March-based Diagnosis for Pinhole and Intermediate State defects for industrial chips

IM $P_{IM}$ is recognized as the identifying feature for Intermediate State defect and is limited due to the sense amplifier circuit, see figure 4.4. The sense amplifier can only detect two states, and therefore, $R_{IM}$ will be read either as 0 or as 1. Hence, Intermediate State defects can never be detected or diagnosed by a binary analog-to-digital converter, and multiple reference resistors are required to overcome this limitation. For example, in figure 4.5 (b), two reference resistors are utilized to detect three states: '0', '1', and 'U'. The intermediate states are located in the 'U' state region, distinct from the regular '0' or '1' state range. However, it is important to note that other defects, such as the interconnect defect shown in the red square of figure 4.5 (b), may also cause the defective STT-MRAM cell state to be located in the 'U' range. Therefore, diagnosing the Intermediate State requires detecting all three states. To achieve this, the following march algorithm should be employed: $M = \{\Updownarrow (w0, r0, w1, r1)^i\}$, which switches and detects the STT-MRAM cell between '0' and '1' for $i$ times. This guarantees the extraction of the identifying feature $P_{IM}$ from digital-based industrial chips with the 'U' state as the intermediate state.

SAFF $H_{dir}$ representing the direction of the hysteresis loop to detect the SAF Flip defect cannot be extracted directly from the STT-MRAM array with sense amplifiers. STT-MRAM cell resistance cannot be directly read from the R-H measurement. Hence, the following march algorithm should be applied to catch $H_{dir}$: $M = \{\Updownarrow (w0); H_{ext}; \Updownarrow (r0)\}$. This march algorithm consists of three steps:

1. Apply $w0$ for initialization
2. Apply an external magnetic field $H_{ext}$
3. Apply $r1$ operation to detect the final state

Figure 4.6 demonstrates the effectiveness of this method. Under the external magnetic field, only the SAFF-defective devices get switched to the '1' state, while regular devices stay in the '0' state.

BH $\alpha_{WER}$ is the identifying feature of the Back-Hopping defect. However, since the $WER$ is calculated by the binary logical memory value and not the resistance value, the DAT-based Diagnosis for Back-Hopping defect can also be applied to industrial chips with sense amplifiers. The $WER$ growth over bias voltage can be extracted as follows:

1. Perform: $M = \{\Updownarrow (w0, r0)^i\}$
2. Increase the write voltage $V_{bias}$

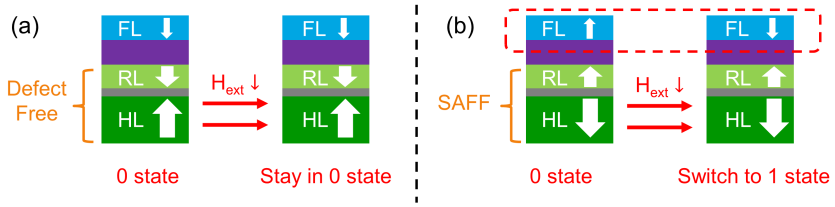



Figure 4.6: March-based diagnosis for SAF Flip defect

3. If $V_{bias} < V_{threshold}$, go to step 1. Otherwise, stop the iteration.

## 4.3. ML-based Diagnosis

This section dives into the ML-based Diagnosis approach, a methodology for classifying defects within STT-MRAM technology using low-cost features. This approach explores the potential to classify MTJ's unique defects classification by utilizing machine learning algorithms and models. The objective is to train a machine learning model to map measurable low-cost MTJ features to defect types and to accelerate the DAT-based Diagnosis method to identify the defect type of an STT-MRAM device using machine learning with features extracted from low-cost measurements instead of the more expensive measurements used to extract the identifying features for DAT-based Diagnosis. This approach requires several steps:

1. Feature Selection: The goal of this step is to select relevant MTJ technology parameters that are cost-efficient to measure and extract. These parameters or features will be used as input for the trained model to predict the defect type of the corresponding MTJ device.
2. Model Selection: The machine learning model to be trained is selected in this step. The model, as well as the features, have a significant impact on the prediction performance of the defect types of the MTJ devices.
3. Hyperparameter Optimization: The selected model's internal parameters referred to as the hyperparameters are optimized in this step.
4. Training and Evaluation: The validation and evaluation of the training process is required in this last step to assess the performance and generalization ability of the model on unseen data.

### 4.3.1. Feature Selection

The MTJ parameters extracted from the RH-Loop measurements, $H_C$, $H_{offset}$, $R_P$ and $TMR$ are used as input features for the trained machine learning models, and the defect types, Pinhole, Intermediate State, SAF Flip and Back-Hopping, as output labels. These features cover the magnetic and electrical behavior of the switching mechanism of an MTJ device and can be extracted through low-cost measurements.

Coercivity Field $H_C$ represents the magnetic field strength required to switch the magnetization of the MTJ layers. It is an important feature because defects can influence the magnetic properties of the device, leading to changes in $H_C$.

Offset Field $H_{off}$ represent the internal magnetic coupling between FL and RL, and like $H_C$, it is indicative of changes in the magnetic behavior of the device that could be related to defects.

Parallel Resistive State $R_P$ represents the electrical resistance of the MTJ device when the magnetic layers are in parallel alignment or in a low resistive state. Changes in $R_P$ can reflect variations in the electrical properties of the device influenced by defects.

Tunnel Magnetoresistance Ratio $TMR$ is a measure of how the resistance of the MTJ device changes based on the relative alignment of the magnetic layers. It is sensitive to both electrical and magnetic variations.

### 4.3.2. Model Selection

Two models are chosen to explore the machine learning potential to classify defects in STT-MRAM devices, K-Nearest Neighbour (KNN) and Neural Network (NN). KNN is chosen due to its simple characteristic, while neural network is more complex due to its flexibility to extract non-linear relations in the provided data. It is worth the exploration to train models with two different characteristics in terms of complexity. Note that the dataset used to train the models is labeled by the DAT-based Diagnosis method discussed before.

K-Nearest Neighbour KNN algorithm is one of the techniques employed in ML-based Diagnosis to classify STT-MRAM defects using low-cost features. KNN operates on the principle that data points with similar characteristics will likely belong to the same class. The algorithm identifies a predetermined parameter $K$ of nearest neighbors from the training set. It assigns a label to the unknown device based on the majority class among its neighbors, as illustrated in figure 4.7. KNN is useful when dealing with relatively small datasets and offers a simple yet effective mechanism for defect classification.

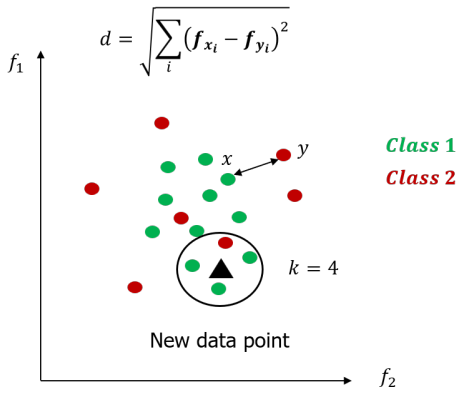
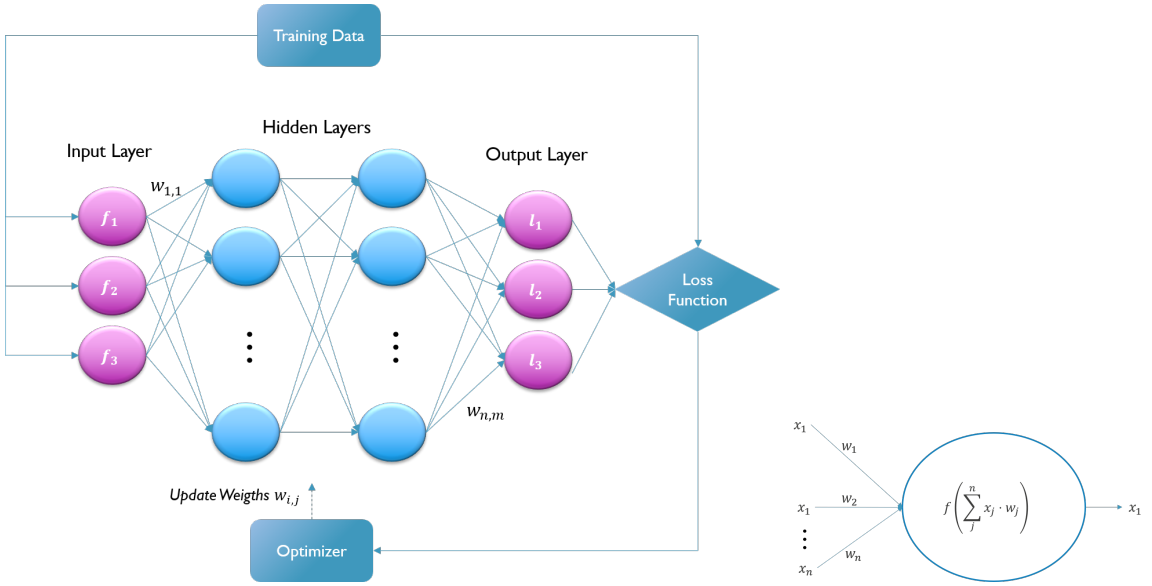



Figure 4.7: K-Nearest Neighbour

Neural Network Another powerful and widely used tool is the Neural Network. The human brain's interconnected neurons inspire neural networks and can capture relationships within complex non-linear data. A neural network can recognize patterns and features associated with various defect types in STT-MRAM devices. The network contains layers of interconnected nodes, each processing the data before passing it to the next layer; see figure 4.8. With good training using labeled data, neural networks can learn to make accurate predictions about defect types. The parameters or the weights of the connection in the neural network are trained using an optimizer that uses the calculated difference between the predicted and actual labels during training to adapt the weights until the values converge. The versatility and adaptability of neural networks and the ability to capture the complexity in the input data make them well-suited for tasks involving non-linear relationships and large datasets.




(a) Neural Network (b) Neuron

Figure 4.8: Neural Network

### 4.3.3. Training and Evaluation

A robust training, evaluation, and validation process is employed to utilize the full potential of ML-based Diagnosis. This process ensures accuracy in identifying and classifying defects. First, the dataset containing labeled examples of devices with known defect types is divided into training, validation, and test sets. The training set serves as the foundation for the model's learning process by adjusting the model's internal parameters or weights to minimize errors in predicting defect types. The validation stage serves as a safeguard against overfitting, a scenario in which the model struggles to generalize to unseen data. The validation occurs in an iterative manner where the training data is divided into K folds or parts. Part of the data is used for training, and the other parts are used for validations in each iteration. In the next iterations, the folds are chosen differently to assess the model's performance and optimize the model. Once the model is tuned and optimized, it undergoes the test phase using the test set. This set represents unseen data to measure the model's ability to generalize to new situations for inference. The model's performance on the test set provides an assessment of its accuracy and effectiveness in classifying defects of new STT-MRAM devices.

In evaluating the performance of the ML-based Diagnosis approach, two essential metrics are used: the F-score and balanced accuracy. These metrics represent how well the models perform in classifying defects. The F-score combines both precision and recall, providing a balanced assessment of the model's ability to identify both true positives (correctly identified defects) and avoid false positives (incorrectly identified defects). A high F score indicates that the model balances precision and recall. Balanced accuracy accounts for imbalanced class distributions in real-world datasets. It ensures that each class contributes equally to the overall accuracy calculation. A higher balanced accuracy means the model effectively classifies defects across all classes, even those with fewer data points. See equation 4.4 for the formulas with True Positive (TP), False Positive (FP), True Negative (TN), and False Negative (FN).

$$
\begin{aligned}
F-score &= \frac{2 \cdot Precision \cdot Recall}{Precision + Recall} \\
Precision &= \frac{TP}{TP+FP} \\
Recall &= \frac{TP}{TP+FN} \\
B-Accuracy &= \frac{Sensitivity + Specificity}{2} \\
Sensitivity &= \frac{TP}{TP+FN} \\
Specificity &= \frac{TN}{TN+FP}
\end{aligned}
\tag{4.4}
$$

The models' capacity to handle imbalanced datasets and classify the defects is assessed by evaluating the models using these metrics. This evaluation methodology is used as a guide during the machine learning design process for STT-MRAM defect classification.

## 4.4. Conclusion

### 4.4.1. Summary

This chapter discussed the methodologies employed for STT-MRAM defect diagnosis in this thesis. The outlined approaches, DAT-based and ML-based Diagnosis, have different perspectives on identifying and classifying defects in STT-MRAM technology. Figure 4.9 summarizes the diagnosis process and workflow for defect identification, classification, and outlier detection. While these methodologies have demonstrated significant potential, it is essential to acknowledge their theoretical limitations. For example, Sidewall defects have some similar properties and impact on MTJ parameters as Pinhole defect L. Wu et al., 2018.

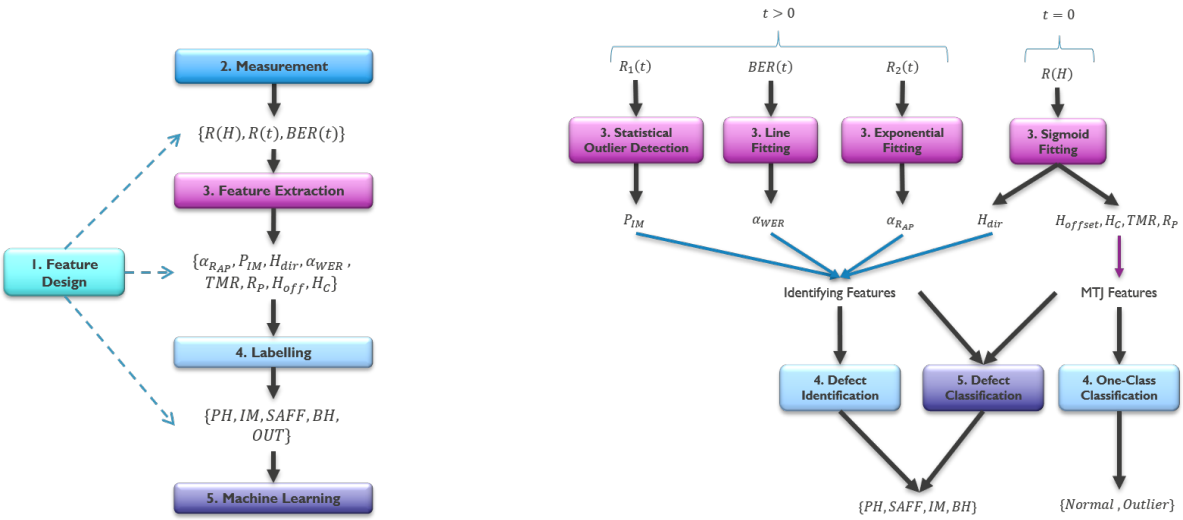



Figure 4.9: Workflow on the left and the design on the right summarizing the thesis theoretical framework

DAT-based Diagnosis presents a comprehensive method to label data by identifying features based on the core nature of defects' impact on STT-MRAM parameters. However, its application may face challenges with certain defects that vaguely manifest themselves, leading to a possible misidentification. Similarly, ML-based Diagnosis utilizes the power of machine learning to achieve a robust classification based on the data labeled by the DAT-based Diagnosis method. However, the assumption that DAT-based Diagnosis works ideally may need to be verified, misleading the training process. In addition,

the mapping of low-cost features to the defect types instead of the identifying features may result in a lower classification accuracy than DAT-based Diagnosis.

### 4.4.2. Scalability

The developed methodologies can be applied in real-time scenarios to identify the defect type of a certain STT-MRAM device using either the DAT-based approach or the ML-based approach. The defect identification is essential to diagnose the failed devices from the test or customer returns. In addition, the methods are applicable for characterization devices for research or development purposes to either filter devices or to further study the defective behavior of the device to update the MTJ compact defective model.

Both DAT-based and ML-based diagnosis methods demonstrate scalability potential. DAT-based Diagnosis methodology, which relies on identifying features automatically extracted from the measurements, can be applied to other defects in STT-MRAM or in other emerging technologies. The methodology demonstrated a structured method from understanding the impact of the defect on the device performance to constructing features that are used to identify the defect types based on simple conditions using thresholds. This framework provides a structured and comprehensive approach to diagnosing defects in emerging technologies in general.

On the other hand, ML-based Diagnosis leverages machine learning algorithms by training a model to map low-cost MTJ features to the defect types. This mapping approach can be applied to defects in STT-MRAM as well as to other emerging technologies. Like DAT-based Diagnosis, ML-based Diagnosis aims to identify features that are relevant to the defects by understanding the impact of the defects on the device performance. However, the idea to create a feature space that leverages the correlation between the MTJ features as well as the correlation between the defect types and the features provides a solid framework for defect modeling and defect classification.

### 4.4.3. Future Recommendations

It is worth noting that some investigation is set aside due to time constraints and thesis objectives. Specifically, the idea is to create a complete feature space that captures the defective behavior of the STT-MRAM by introducing new features. These features go beyond the MTJ parameters by measuring the deviation of the measurement results to the ideal results. This approach may create a foundation for further research investigating new defects and further understanding current defects.

There are several key areas that can be recommended for research and investigation to enhance the developed methodologies. Research should focus on improving the ML-based Diagnosis by exploring other MTJ features and expanding its defect coverage. The identifying features should also be further researched to provide a solid and comprehensive motivation for the selected features. Additionally, investigate alternative labeling techniques, such as PFA methods, that reduce dependence on labeled data for ML-based Diagnosis.

# 5

# Experimental Validation

This chapter presents the implementation and evaluation of the proposed methodologies discussed in the previous chapter 4. Section 5.1 describes the measurement and software setup to collect and extract data required to validate the methodologies. Section 5.2 visualizes and analyzes the extracted data from the measurements. Sections 5.3 and 5.4 focus on the implementation and results of the proposed DAT-based and ML-based Diagnosis, respectively. Overall, this chapter assesses the implemented methodologies on the measured data and validates machine learning potential for STT-MRAM diagnosis in defect classification. The measurements were conducted at IMEC, Research and Development company imec located in Leuven, Belgium, on specialized characterization wafers containing STT-MRAM arrays with additional logic and equipment, such as magnets, to measure the electrical and magnetic properties of the devices.

## 5.1. Experimental Setup

Both the measurement setup and the software to extract the identifying features are discussed in this section. The objective is to determine the setup needed to extract the identifying features for DAT-based Diagnosis and the low-cost features for ML-based Diagnosis discussed in the next section. Three arrays of STT-MRAM devices are used for the measurements. The first array containing 131072 MTJs of 60nm Critical Diameter (CD) and 200nm pitch size is measured. The second array from the same wafer as the first array containing 65536 devices of 200nm pitch size is measured to catch Pinhole and Intermediate State defects. The third array from another wafer with the same characteristics as the first array is measured to assess the designed diagnosis methodologies' performance and generalization ability. The measured datasets are summarized as follows:

- Dataset 1: The set contains data from 131072 MTJ devices with 60nm CD and 200nm pitch size. This dataset serves as the cornerstone for training data and further analysis.
- Dataset 2: The second dataset addresses specific defects not represented in Dataset 1. This dataset is meant to detect pinhole and intermediate state defects not detected by Dataset 1. The devices measured in this set have a CD of 150nm and 200nm pitch size. Unfortunately, Intermediate State defects were not observed in this dataset.
- Dataset 3: The last dataset originated from another wafer but retained the same characteristics as the first array, Dataset 1. This dataset will be used to evaluate the effectiveness of the trained models to ensure their robustness beyond the confines of the training data.

### 5.1.1. Measurement Setup

IMEC offers a highly controlled and state-of-the-art laboratory environment equipped with the latest semiconductor characterization tools and equipment required for precise and accurate measurements to evaluate STT-MRAM devices. The measurements are conducted on unpackaged wafers containing chip modules. Each module contains several STT-MRAM arrays with different characteristics surrounded

by the necessary circuitry to control the devices in the arrays. The measurements are conducted in a controlled environment using a semi-automatic process to load the wafers in the prober and Application Programming Interface (API) to connect the needles to the targeting module. A probecard is used to connect a module to the prober to provide the required current to the arrays and a controller to execute the memory operations. For magnetic operations, a magnet is used to switch the STT-MRAM devices. At last, the operations for the measurements are written in a script to be executed through APIs communicating with the controller. The measurement setup is summarized in table 5.1, and the terminologies are explained as follows:

- Target: the features to be extracted from the measurements
- Range: the range of the variable measurable parameter
- Steps: the sample size of the variable measurable parameter
- Initialization: the initial test before measurement
- Read Voltage: the pulse height for the read operations
- Write Voltage: the pulse height for the write operations
- Read Pulse Width: the pulse width for the read operations
- Write Pulse Width: the pulse width for the write operations
- Cycles: the number of repetitions of the measurement setup
- Sense Amplifier: whether a sense amplifier is used or not

| Setup | $R(H)$ | $R_1(t)$ | $R_2(t)$ | $BER(V)$ |
|---|---|---|---|---|
| Target | $R_P, TMR, H_C, H_{off}, H_{dir}$ | $P_{IM}$ | $\alpha_{R_{AP}}$ | $\alpha_{WER}$ |
| Initialization | $-380\ mH$ | $-380\ mH$ | $380\ mH$ | n/a |
| Magnetic Field | $[2.5,\dots 380, -2.5,\dots -380]\ mH$ | n/a | n/a | n/a |
| Write Voltage | n/a | $[-V_1, V_1]$ | $0.8V$ | $[V_2, \dots, V_3]\ V$ |
| Write Pulse Width | n/a | $15\ ns$ | $50\ ns$ | $10\ ns$ |
| Steps | $20\ mH$ | n/a | n/a | $0.02\ V$ |
| Cycles | 1 | 1000 | 250 | 1000 |
| Read Voltage | Default | Default | Default | Default |
| Read Pulse Width | Default | Default | Default | Default |
| Sense Amplifier | No | No | No | Yes |

Figure 5.1: Setup for stress, RH, and BER measurements

RH $R(H)$ measurement involves applying an external magnetic field to switch the MTJ devices and read their resistances by applying a small current to capture $H_{dir}$ identifying feature to identify the SAFF defect and the MTJ feature $R_P$, $TMR$, $H_C$ and $H_{offset}$ required the ML-based Diagnosis.

R(t)The stress measurements $R_1(t)$ and $R_2(t)$ involve applying pre-determined repetitive write operations over certain cycles and reading the resistance values over time. $R_1(t)$ measurement is used to capture the identifying feature $P_{IM}$ to identify the Intermediate State while $R_2(t)$ is used to extract the identifying feature $\alpha_{R_{AP}}$ for Pinhole defect identification.

Bit Error Rate (BER) $BER(V)$ measurement involves using the sense amplifier to assess the WER by repeating write and read operations over a certain period of time.
As it can be seen from table 5.1, certain voltage parameters are not fixed such as $V_1$, $V_2$ and $V_3$. However, they depend on the switching behavior of the MTJs in the array. Therefore, a voltage sweep is performed across the array to measure all the devices' overall switching probability. Figure 5.2 illustrates the switching probability across write voltages. The three parameters $V_1$, $V_2$ and $V_3$ are chosen from the plot where $V_1$ represents the voltage when $P_{sw} = 50\%$ required for $R_1(t)$ measurement to catch

Intermediate State defects. $V_2$ and $V_3$ represent the write voltage when $P_{sw} \approx 100\%$ and the breakdown voltage, respectively, for catching Back-Hopping defects.

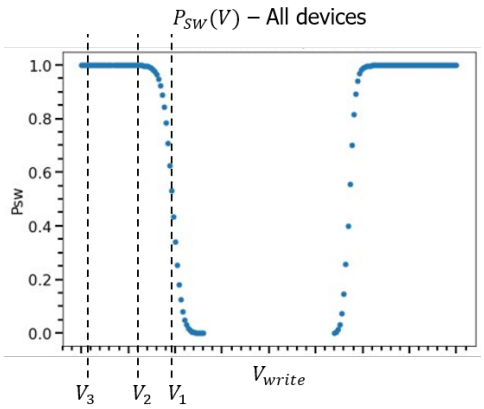



Figure 5.2: Voltage sweep $V_{write}$ to determine overall switching probability $P_{sw}$

### 5.1.2. Data Processing

The raw data from the measurement are provided to a software that extracts the identifying and low-cost features. This software acts as a bridge between the measured electrical data and the defect diagnosis process. It reads the raw data obtained from the measurements and applies fitting functions to extract relevant features. This automated feature extraction process eliminates the need for manual defect identification and ensures consistency and accuracy while handling large datasets. As a result, the software lays the foundation for the subsequent stages of defect identification and classification using machine learning techniques and reducing human error and bias.

The software is divided into modules, each with a specific task: Measurement, Device, Identification, AI, and Feature Extraction modules. The Measurement module reads the files containing the raw data from the measurements accordingly and is stored separately for each device. The Device module contains the data for one STT-MRAM device. The Feature Extraction module contains four different classes representing the defect type, where each class extracts the required features from the raw data for the particular defect type using fitting functions or specific algorithms. The Identification module combines all the features extracted from the STT-MRAM device into one dataset for several tasks, including processing the dataset, plotting the distribution, and labeling the devices accordingly using the identifying features. The Artificial Intelligence (AI) module conducts two main tasks. One task is to apply one-class unsupervised learning on the dataset from the Identification module to label the defect-free and defective classes. The other task is to train a machine learning model to classify the defects using the labeled data by the Identification module. These modules and their connections are summarized and illustrated in figure 5.3.

## 5.2. Data Analysis

This section visualizes and analyzes the data distribution and feature correlations, providing a fundamental understanding of the acquired data guiding the evaluation process. Note that the intermediate state defective devices were not found during the measurements. Therefore, the analysis and development did not consider the identifying feature $P_{IM}$ and the defective label $IM$.

### 5.2.1. Data Distribution

Understanding data distribution is crucial in utilizing machine learning techniques and evaluating the DAT-based and ML-based diagnosis methods. Both the data distribution of the identifying and low-cost features are analyzed and illustrated in figure 5.4.

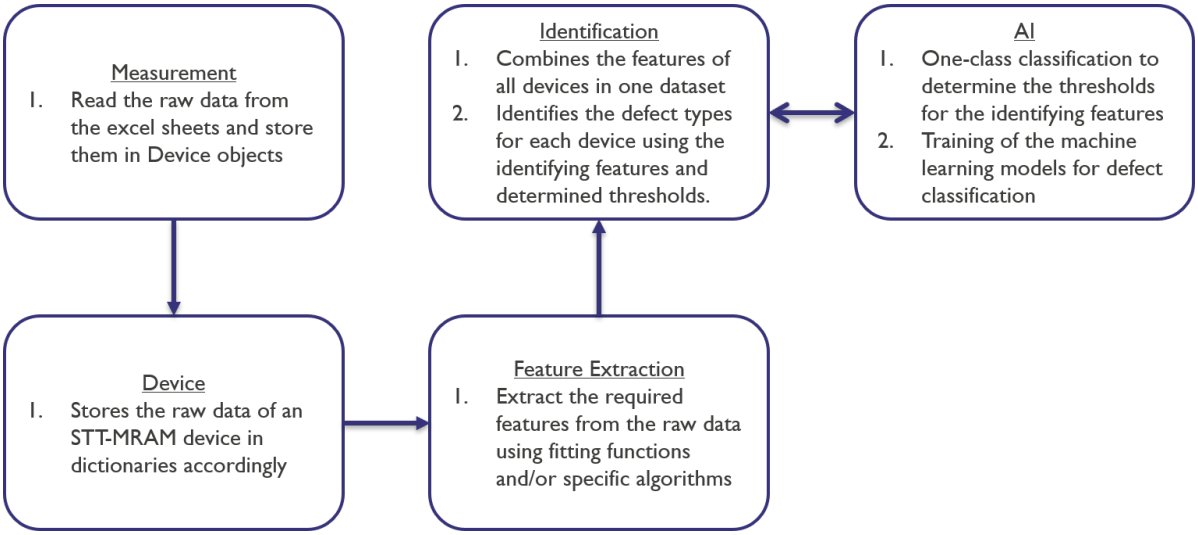



Figure 5.3: Diagram showcasing the software modules for processing the raw measured data.

The identifying features, which serve as indicators for defect identification, show an exponential distribution. This distribution aligns with the expectations as defects cause deviations from the norm exponentially; see equation 5.2. This enables the proposed system to robustly identify and label devices based on the magnitude of these identifying features. In contrast, the low-cost MTJ features utilized for defect classification show a Gaussian distribution; see equation 5.1. This is consistent with our assumptions, as Gaussian distributions are commonly observed in nature. The Gaussian distribution of low-cost features provides a solid foundation for the machine learning models to effectively differentiate between different defect types.

$$f(x) = \frac{1}{\sigma\sqrt{2\pi}} \exp -\frac{1}{2}\left(\frac{x-\mu}{\sigma}\right)^2 \tag{5.1}$$

$$f(x) = \frac{1}{\beta} \exp -\left(\frac{x-\alpha}{\beta}\right) \tag{5.2}$$

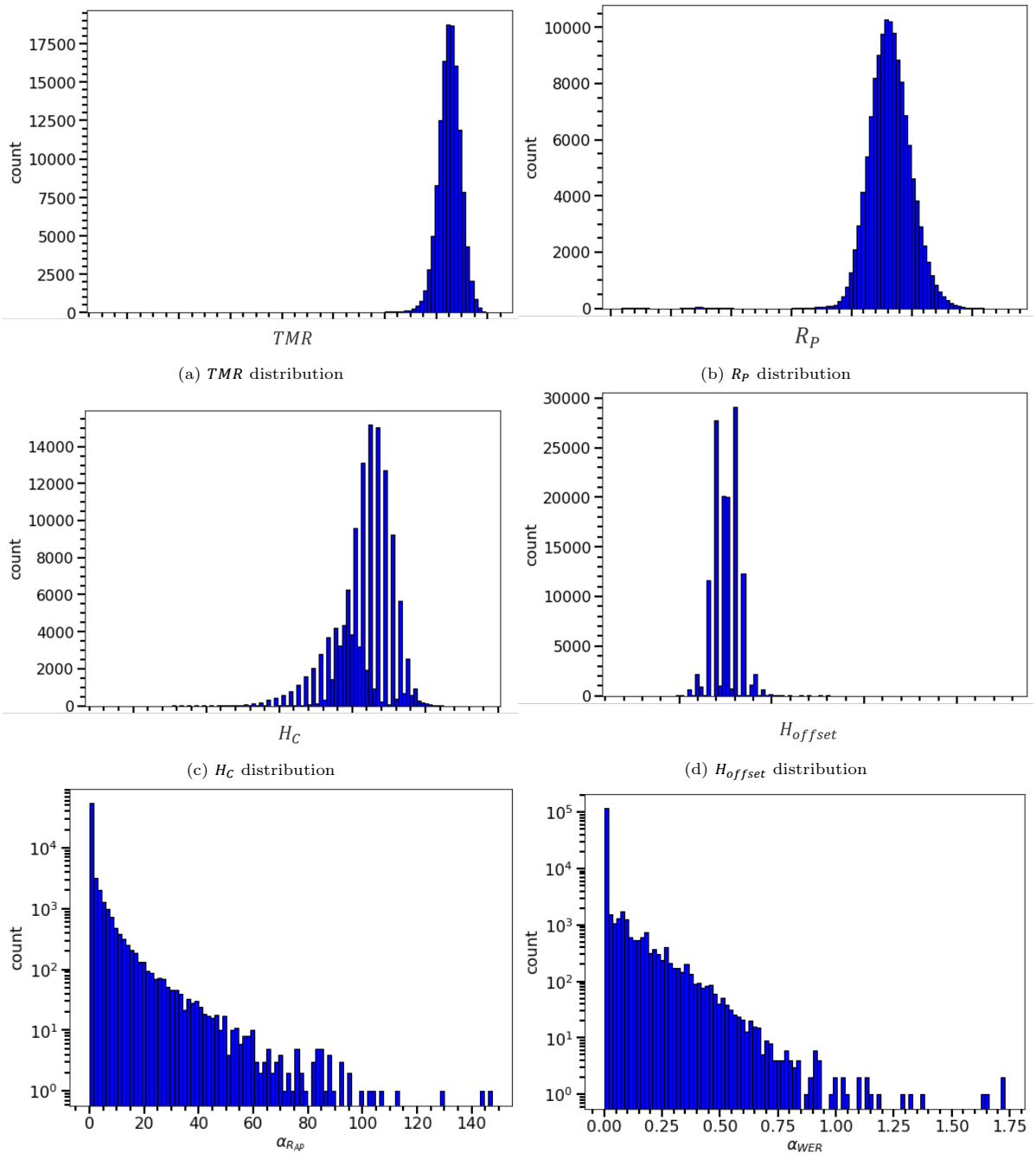
| Fitted Parameters | $TMR$ | $R_P$ | $H_C$ | $H_{offset}$ | $\alpha_{WER}$ | $\alpha_{R_{AP}}$ |
|---|---|---|---|---|---|---|
| $\mu/\alpha$ | 1.445 | 2314.484 | 207.341 | -24.692 | -1.279e-38 | 1.625e-36 |
| $\sigma/\beta$ | 0.087 | 188.432 | 19.153 | 6.854 | 0.016 | 1.506 |

Table 5.1: The calculated parameters of the data distributions with $\alpha$ and $\mu$ denoting the decay and the mean respectively and $\beta$ and $\sigma$ denoting the scale and standard deviation respectively.

These data distributions provide insights that are relevant for evaluating the two developed diagnosis methodologies in terms of defect identification performance, machine learning generalization ability, and outlier analysis.

### 5.2.2. Feature Correlation

In the pursuit of effective defect identification and classification, an analysis of the correlations between the identifying and the low-cost features is conducted. This exploration is necessary to gain insights into the dependencies between the features to aid the development of the machine learning training process. By analyzing feature correlations, we can identify redundancies, dependencies, and potential issues that might impact the performance of our machine-learning algorithms. We calculated the correlation coefficients between each pair of the features using equation 5.3. The resulting correlation matrices of Dataset 1 and Dataset 2 are depicted in figure 5.5.




(a) $TMR$ distribution

(b) $R_P$ distribution

(c) $H_C$ distribution

(d) $H_{offset}$ distribution

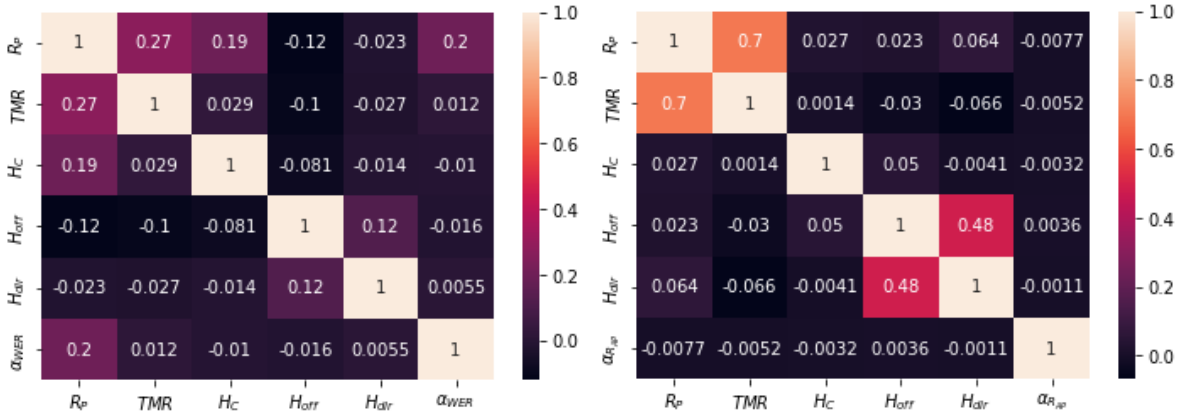
(e) $\alpha_{R_{AP}}$ distribution in log scale

(f) $\alpha_{WER}$ distribution in log scale

Figure 5.4: Data Distribution of the measured and extracted identifying and low-cost features

$$r = \frac{\sum(x_i - \bar{x})(y_i - \bar{y})}{\sqrt{\sum(x_i - \bar{x})^2 \sum(y_i - \bar{y})^2}} \tag{5.3}$$

The correlation matrices show that $TMR$ and $R_P$ are highly correlated in both datasets. This dependency is because $TMR$ equals the ratio of the difference of $R_P$ and $R_{AP}$ and $R_P$. The same trend is observed for $R_P$ and $H_C$ in Dataset 1 but not in Dataset 2. This one-sided dependency may contribute to the reduction in oxide thickness $t_{ox}$, which decreases resistance and increases the interchanged magnetic coupling of RL and FL for 60-nm devices Katayama et al., 2006. At the same time, this behavior




(a) $R_P, TMR, H_C, H_{offset}, \alpha_{WER}$ (CD=60nm) (b) $R_P, TMR, H_C, H_{offset}, \alpha_{R_{AP}}$ (CD=150nm)

Figure 5.5: Feature correlation tables

may not be observed for 150-nm devices due to the high CD relative to the thickness reduction. A small correlation between $TMR$ and $H_{off}$ can also be seen from the correlation matrix of Dataset 1, which can be attributed to the dependency of the oxide thickness and the magnetic coupling of the layers.

On the other hand, we expect correlations between the identifying features and the low-cost features to predict the defect type based on the low-cost features and the labeled training data through the identifying features. Both correlation matrices show that $H_{dir}$ is highly correlated with $H_{offset}$. This correlation contributes to the reversed exhibition of the magnetic field of neighboring MTJ devices in the presence of the SAF Flip defect. Additionally, correlation between $\alpha_{WER}$ and $R_P$ is observed in Dataset 1. In theory, a Back-Hopping defect depends on the device's magnetic properties, not electrical properties, as discussed in chapter 2. Therefore, this correlation cannot be explained at this stage of research. Lastly, $\alpha_{R_{AP}}$ is not correlated with low-cost features. This may impact the machine learning training and prediction performance, allowing the low-cost features to identify the Pinhole defect instead of this identifying feature. It is expected that $\alpha_{R_{AP}}$ would be correlated with $R_P$ and $TMR$ as discussed in Chapter 2. Therefore, further research can be performed to analyze the correlation between the decay of the MTJ's resistance over time and the Pinhole defect.

## 5.3. DAT-based Diagnosis

In the pursuit of designing a systematic approach for identifying unique defects in STT-MRAM devices, a one-class classification is used as discussed in Chapter 4 Section 4.2. The unique class represents the defect-free devices, and the reliable range for the identifying features characterizes defect-free devices. This section will discuss the implementation and results of the methodology applied to the measured devices.

### 5.3.1. Defect Identification

From the previous data analysis, the features have shown Gaussian and Exponential distributions. Therefore, the Elliptic Curve is the suitable machine learning approach for the measured datasets. By defining manual boundaries for the defect-free class, the results confirmed our assumption using balanced accuracy and F-score as shown in figure 5.6 by comparing the local outlier factor, the one-class support vector machine, the isolation forest, and the elliptic curve.

The results are plotted in figure 5.7 with the determined boundaries for the identifying features based on the one-class algorithm (Elliptic Curve). The limits for $\alpha_{WER}$ and $H_{dir}$ are determined using Dataset 1 with the 60nm devices and $\alpha_{R_{AP}}$ with the 150nm devices. These thresholds $\beta_{PH} = 5$, $\beta_{BH}$ and $\beta_{SAFF}$ are used to identify the corresponding defect type based on the extracted identifying features and used as labeled data for machine learning.

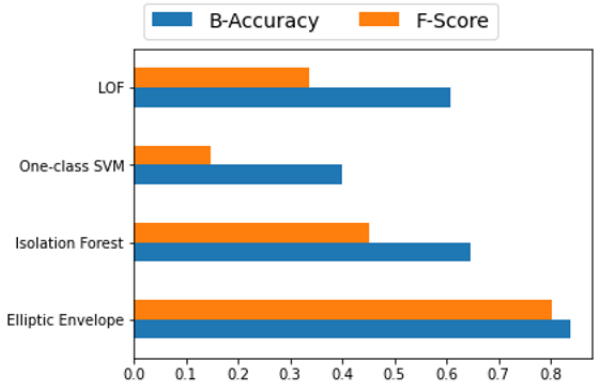



Figure 5.6: Comparison of different algorithms based on F-score and Balanced-accuracy metrics

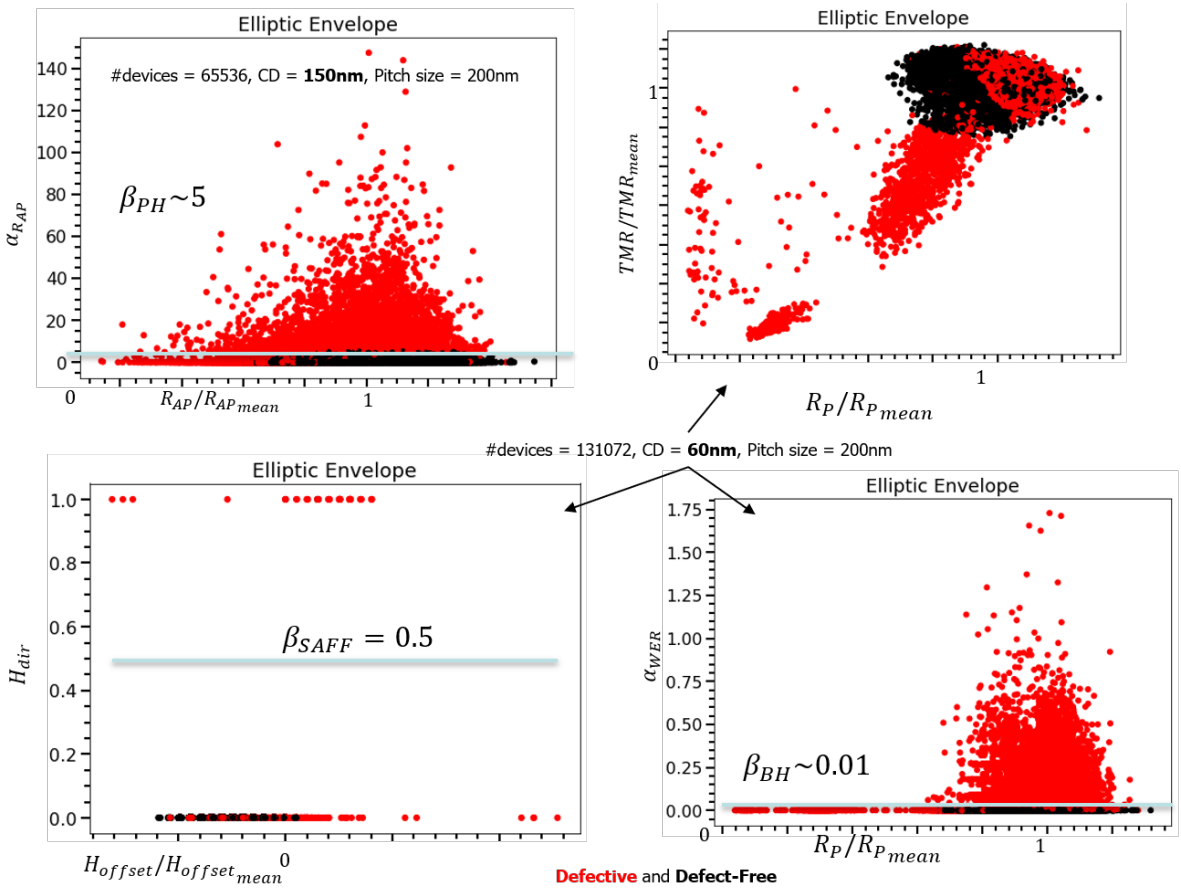
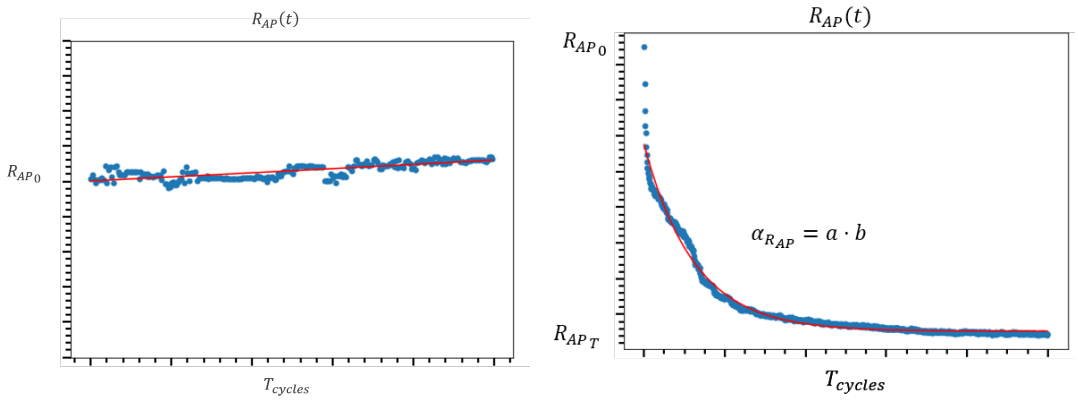



Figure 5.7: The result of Elliptic Curve on two measured arrays, CD=60nm, and CD=150nm

PH Figure 5.8 shows the defect-free and defective case in the presence of the pinhole defect. The exponential decay represented by the identifying feature $\alpha_{R_{AP}}$ is extracted from the measured defective device. From the two cases, it is clear that one device shows a reliable operation over time while the other device shows a growth of the pinhole area over time, resulting in an exponential decrease of $R_{AP}$ as expected.

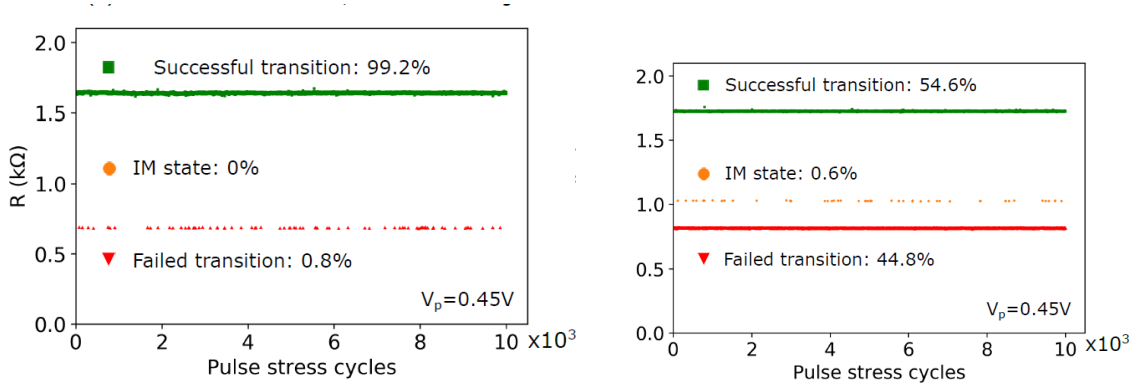
IM Figure 5.9 shows measurement results of two devices, one containing the Intermediate State defect and the other not. The identifying feature $P_{IM}$ is extracted by counting the intermediate states over time. The threshold for the identification is determined based on historical measurements performed by Wu L. Wu, 2021 because no MTJ devices were found with the Intermediate State defect




(a) Defect-Free (b) Defective

Figure 5.8: $R_{AP}$ decay over time due to pinhole defect, $\alpha_{R_{AP}}$

during our measurements. The threshold is determined as $f_{IM} = P_{IM} > \beta_{IM} = 0.6$.




(a) Defect-Free (b) Defective

Figure 5.9: The probabilistic occurrence of intermediate states over time indicating Intermediate State defect L. Wu, 2021

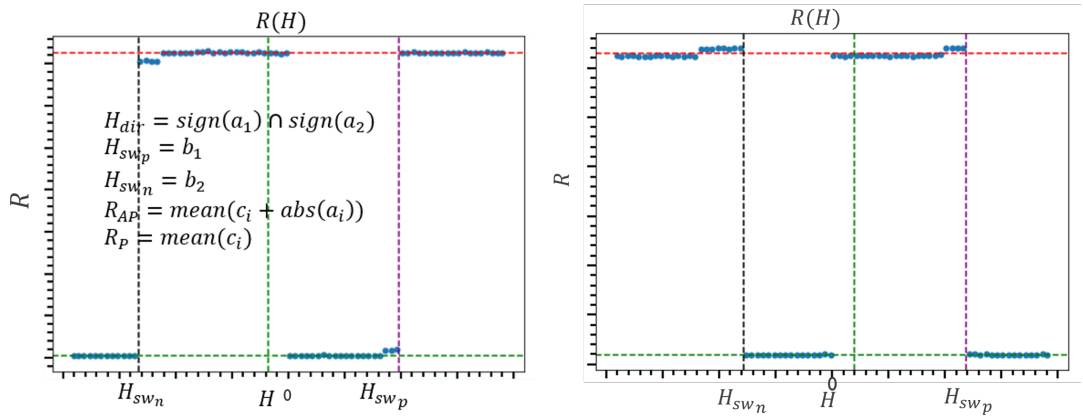
SAFF Figure 5.10 shows the defect-free and the defective cases in the presence of the SAF Flip defect. The identifying feature $H_{dir}$, which represents the direction of the hysteresis loop, can be theoretically determined, $f_{SAFF} = H_{dir} > \beta_{SAFF} = 0.5$. $H_{dir}$ is either 1 or 0, where the value indicates the presence of SAFF defect.

BH The identifying feature $\alpha_{WER}$ for the Back-Hopping defect will be determined through one-class classification. Figure 5.11 shows the defect-free and defective cases containing the Back-Hoppig defect. The fitted power function determined in the feature extraction step extracts $\alpha_{WER}$ using the fitted parameters $a$ and $b$.

In summary, determining the defect type of an MTJ device is performed by assigning a conditional threshold to the identifying features. These thresholds are determined by theoretical analysis and experiments by one-class classification machine learning techniques on the measured dataset.

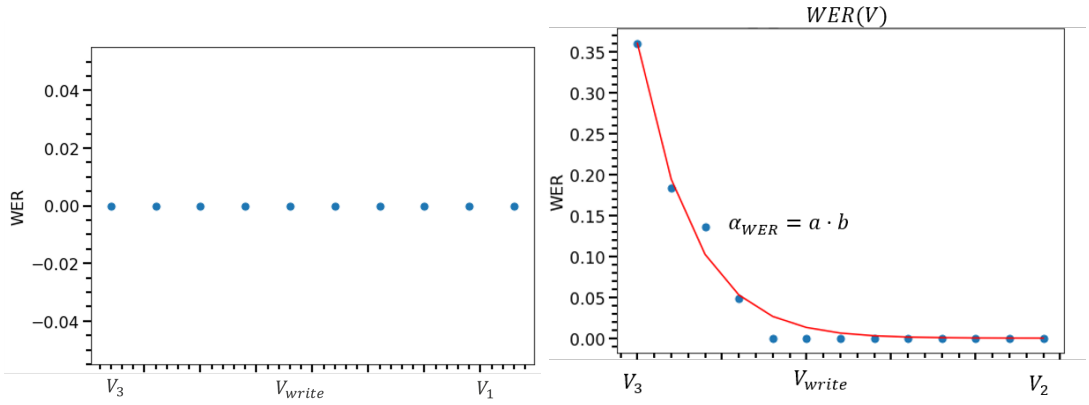
### 5.3.2. Data Labelling

Applying the proposed defect identification methodology using identifying features has shown useful insights. Figure 5.12 shows the results of the defect identification of the Pinhole, SAFF, and Back-Hopping defects on the corresponding datasets plotted with the low-cost MTJ parameters $TMR$, $R_P$, $H_{offset}$ and $H_C$. We can see that the Back-Hopping defect occurs mostly in devices with high $R_P$ and




(a) Defect-Free (b) Defective

Figure 5.10: RH-loop for the defect-free and defective cases containing SAFF defects. Horizontal red and green dashed lines denote $R_{AP}$ and $R_P$, respectively. Vertical black and purple dashed lines denote switching fields $H_{sw_n}$ and $H_{sw}$, respectively. The vertical green represent the offset field $H_{offset}$.




(a) Defect-Free (b) Defective

Figure 5.11: $WER$ increase over bias voltage, $\alpha_{WER}$ indicating Back-Hopping defect

average $TMR$ while uniformly distributed in $H_C$ and $H_{offset}$ plane. This corresponds with our previous feature correlation analysis of $\alpha_{WER}$ and $R_P$. The same expected results are shown for SAFF defect identification, where the defective devices mostly occur when $H_{offset}$ is positive, while the defect-free devices occur when $H_{offset}$ is negative. Lastly, the devices identified as Pinhole defects on Dataset 2 show a random distribution of the low-cost MTJ features.

The histogram shown in figure 5.13 and table 5.4 present the distribution of the defects in the corresponding Dataset 1 and 2. Note that Outlier labeled devices refer to devices that are not defect-free and do not belong to any of the targeted defects. It is observed that most of the MTJs in Dataset 1 are identified as Back-Hopping defective devices, representing 11% of the total measured devices in Dataset 1. On the other hand, the Pinhole defective devices represent 8.4% of the total measured devices in Dataset 2. It is worth noting that the identifying feature $\alpha_{WER}$ for Back-Hopping identification is not extracted from Dataset 2, and the same applies for $\alpha_{R_{AP}}$ for Pinhole identification on Dataset 1. Therefore, the defect-free labeled devices may contain Back-Hopping defects, which may impact ML-based Diagnosis training and evaluation.

We observed distinct patterns associated with different defects by analyzing and identifying features extracted from measurements. By applying our determined threshold values through one-class classification to the identifying features, we could distinguish between devices with defects and those without

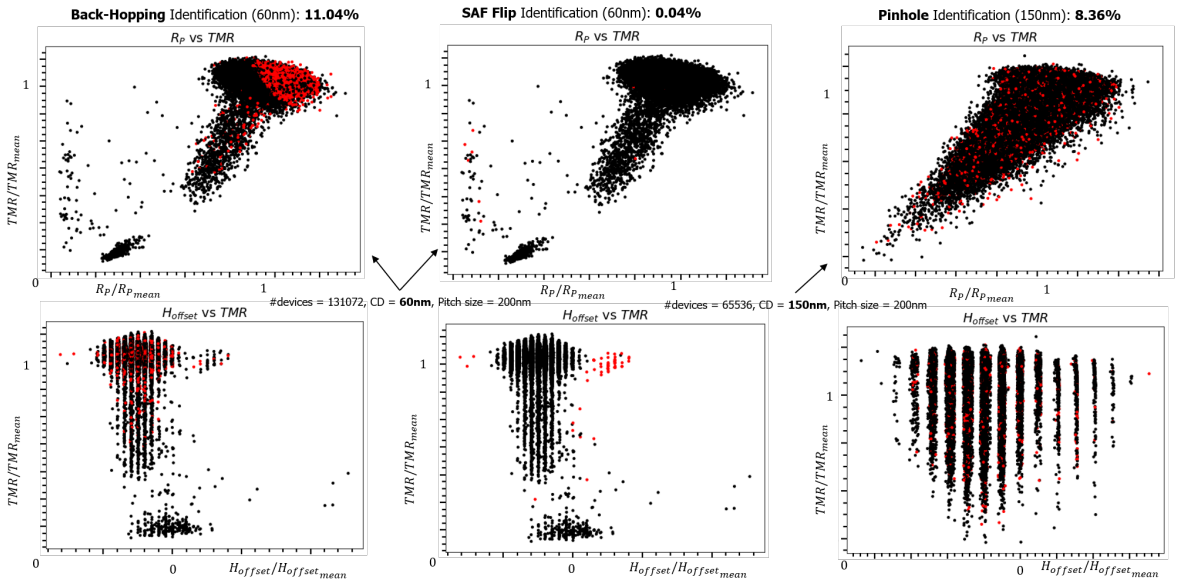
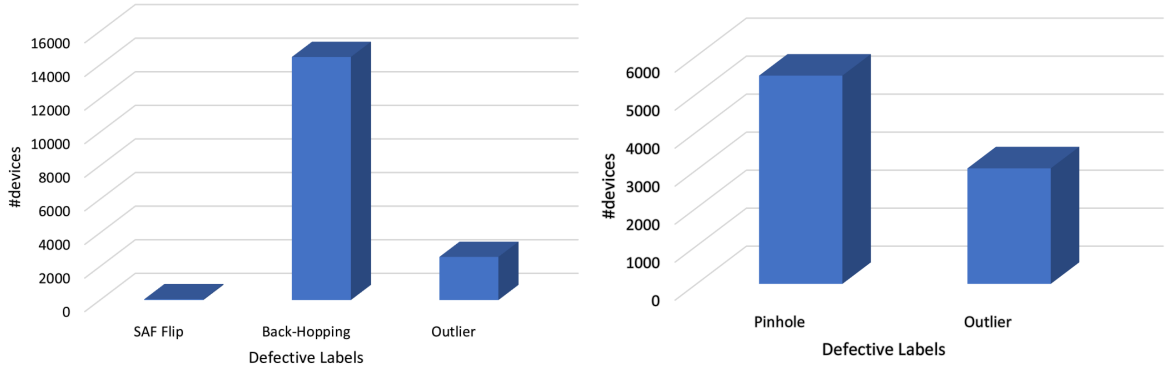



Figure 5.12: Results of DAT-based Diagnosis for defect identification. Red denotes the defective devices.




(a) Dataset to identify SAFF and BH defect (CD=60nm)

(b) Dataset to identify pinhole defect (CD=150nm)

Figure 5.13: histogram denoting the defect type distribution over the measured devices

| SAF Flip | Back-Hopping | Outlier | Defect-Free |
|---|---|---|---|
| 52 | 14470 | 2570 | 113980 |

Table 5.2: Dataset 1: devices=131072, CD=60nm

| Pinhole | Outlier | Defect-Free |
|---|---|---|
| 5480 | 3040 | 57016 |

Table 5.3: Dataset 2: devices=65536, CD=150nm

Table 5.4: Number of identified defects using the proposed DAT-based Diagnosis

and determine the defect type. Note that the Intermediate State defect is not considered as explained before. This approach shows the potential for a robust solution for the real-world semiconductor manufacturing diagnosis process using specialized measurement setup and identifying features to determine the defect type of a given defective device.

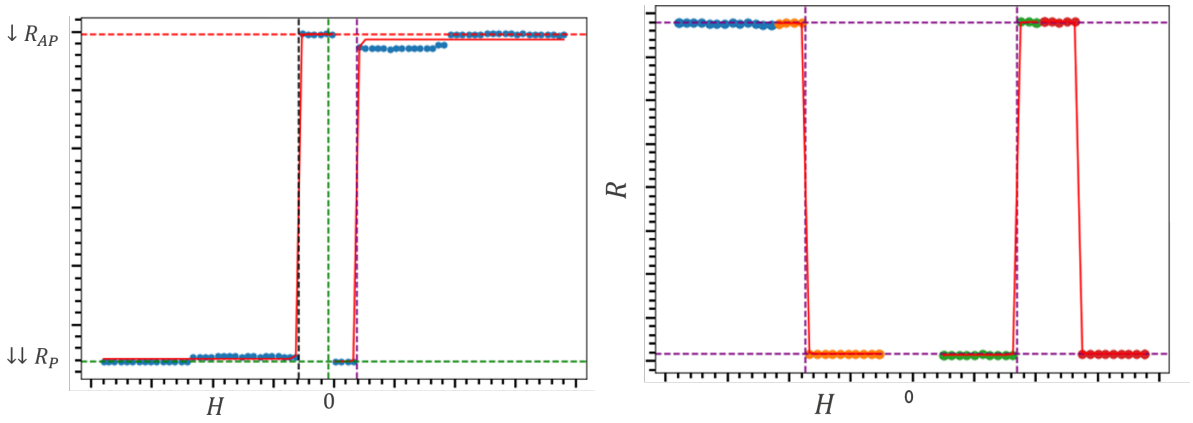
### 5.3.3. Outlier Analysis

Several devices exhibited outlying behaviors that do not belong to the defect-free or targeted defect classes. These outliers deviate from the pattern of the defective and defect-free devices, posing challenges and insights for further research. Figure 5.14 shows three selected devices from the measurements that show outlying behaviors.

Device A displayed normal behavior, showing a smooth transition from a low state to a high state at a certain applied magnetic field. However, the combination of $TMR$ and $R_P$ does not match our overall expectation of high $TMR$ and low $R_P$. The decrease of $R_P$ is also expected to cause a decrease in $TMR$, as many outliers from the previous analysis have shown. Therefore, it seems that the polarization of the electrons is not affected by shorts in the MgO or a decrease in energy barrier $\varphi$.

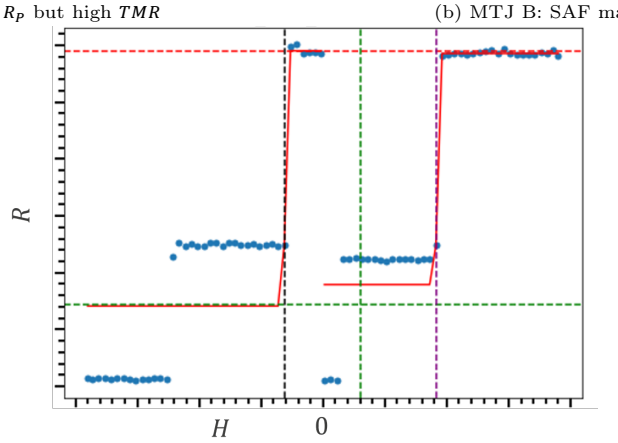
Device B presented an anomalous behavior with a known defect type, the SAFF defect. However, the device shows three switching fields instead of two with consistent $R_P$ and $R_{AP}$ values. This outlying behavior is contributed to the Synthetic Anti-Ferromagnet (SAF) Magnetic Reversal, where the FL switches back to the defect-free state at high magnetic fields where the HL and RL are flipped again.

Device C shows non-probabilistic intermediate states where the device switches to a fixed intermediate state for a range of applied magnetic fields. These three instances of outlying behaviors emphasize the sensitivity of detecting anomalies through automatic fitting and feature extraction. By introducing several features representing the deviation of outliers, we can detect new defects and outlying behaviors in MTJ devices, contributing to STT-MRAM defect characterization research.




(a) MTJ A: Low $R_P$ but high $TMR$

(b) MTJ B: SAF magnetic reversal




(c) MTJ C: Occurrence of non-probabilistic intermediate states

Figure 5.14: Defective outlying behaviors

## 5.4. ML-based Diagnosis

As the final two stages of the diagnosis methodology as explained in Chapter 4, this section will discuss the implementation and evaluation of the proposed ML-based Diagnosis approach. The objective is to identify the type of defect with low-cost MTJ features through supervised learning using labeled training data from the DAT-based diagnosis method. The implementation and evaluation of the method consists of several steps:

1. Hyperparameter Optimization: determining the optimal model's settings or hyperparameters.

2. Training & Evaluation: evaluating the model's performance on the measured datasets.

### 5.4.1. Hyperparameter Optimization

Machine learning models consist of parameters trained by algorithms based on training data and hyperparameters set before training. The effectiveness of machine learning models relies on the choice of machine learning models and their hyperparameters. We will delve into the hyperparameter optimization process conducted for the Neural Network (NN) and K-Nearest Neighbors (KNN) for each defect, leading to the final settings for optimal performance. For the Neural Network, a grid search approach is performed to explore various combinations of hyperparameters, including the number of hidden layers, the number of neurons per layer, activation functions, learning rate, and optimizer algorithm. An iterative search is conducted for the K-Nearest Neighbors to explore the optimal number for the K parameter, denoting the number of neighbors to select during inference.

Through systematically selecting various combinations and evaluating the performance, we identified the optimal configurations for each model for each defect classifier; see table 5.5 for the final settings. The final Neural Network architecture for the SAFF defect classifier consists of the activation function $Relu$, a learning rate of $\alpha = 0.0001$, an optimizer $Adam$, and three hidden layers where the first, second, and third layers consist of 10, 30, and 10 neurons. $Relu$ hyperparameter is an activation function that sets the output of a neuron to zero if its value is less than or equal to zero and remains the same for values greater than zero. $Adam$ and $sgd$ is an optimization algorithm that finds the optimal weights for the internal parameters of the model using the learning rate $\alpha$. The final value for the K parameters of the SAFF classifier is determined to be 2.

| Parameters | SAFF | BH | PH |
|---|---|---|---|
| Activation | Relu | Relu | Tanh |
| Alpha | 0.0001 | 0.05 | 0.0001 |
| Layers | 10,30,10 | 20 | 10,30,10 |
| Solver | adam | adam | sgd |

(a) Neural Network

| Parameters | SAFF | BH | PH |
|---|---|---|---|
| #neighbours | 2 | 30 | 10 |

(b) K-Nearest Neighbour

Table 5.5: Final parameter settings for each classifier

### 5.4.2. Training & Evaluation

After training the Neural Network and K-Nearest Neighbors models, evaluating their performance on unseen data using the final determined hyperparameters is essential. Datasets 1 and 2 acquired from the measurements on the original wafer are divided into training data and test data representing 80% and 20%, respectively, allowing us to evaluate the training on test data using the F-score and Balanced accuracy as metrics. Dataset 3, acquired from the measurements on a new wafer with the same characteristics as the original wafer, is used to assess the models' ability to generalize well to unseen data and devices from other wafers, considering the process variations. The training and evaluation process is summarized as follows:

- Training: The models are trained using the training data, optimizing the model's weights or internal parameters.

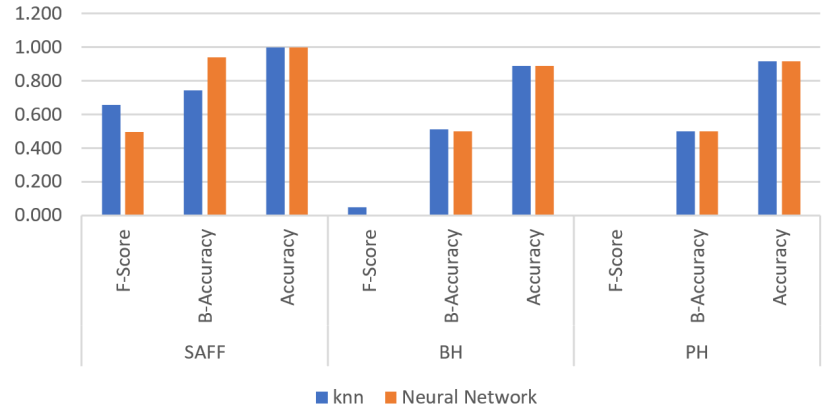
- Test: The model's classification performance is evaluated using test data.
- Evaluation: The model's generalization performance is assessed using the evaluation dataset.

Table 5.6 and histogram shown in figure 5.15 present the training and evaluation process results with corresponding data using an additional Accuracy metric that does not consider the imbalance in the dataset. Both models demonstrated good results for the SAFF defect, suggesting their effectiveness in capturing this particular defect. The SAFF defect shows relatively less variance in classification performance across both Neural Network and KNN models. However, it can be observed that SAFF defect classification on the new wafer does not show the same trend using KNN. This is mainly because the Neural Network captures process variations and complex patterns in the training data while KNN does not, leading to better generalization performance. This pattern shows the Neural Network's capacity to capture complex relationships within the data and its flexibility in handling diverse features for classification. The Back-Hopping classifiers do not show the same trend as the SAFF classifiers for training and evaluating a new wafer.

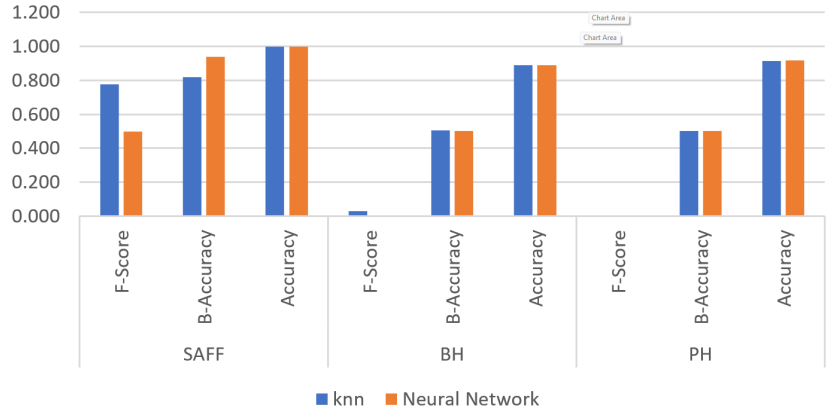
In conclusion, the results obtained after training and evaluating the Neural Network and K-Nearest Neighbors models are auspicious for SAFF defect classification and less for Pinhole defect classification. The models exhibited robustness in identifying defects within the STT-MRAM technology, showcasing their generalization capability across different devices and wafers. The high F-scores and Balanced Accuracy values confirm the accuracy and reliability of the proposed methodology. It is worth noting that the evaluation of the Pinhole defect on the new wafer should not be considered in the generalization assessment since its models are trained on 150nm devices while the new wafer data consists of 60nm devices.

| Defects | Scores | KNN | | | Neural Network | | |
|---|---|---|---|---|---|---|---|
| | | Train | Test | Wafer | Train | Test | Wafer |
| SAFF | F-Score | 0.656 | 0.778 | 0.000 | 0.497 | 0.497 | 0.444 |
| | B-Accuracy | 0.744 | 0.818 | 0.500 | 0.939 | 0.939 | 0.954 |
| | Accuracy | 1.000 | 1.000 | 1.000 | 0.999 | 0.999 | 0.999 |
| BH | F-Score | 0.049 | 0.029 | 0.039 | 0.000 | 0.000 | 0.000 |
| | B-Accuracy | 0.512 | 0.506 | 0.505 | 0.500 | 0.500 | 0.500 |
| | Accuracy | 0.890 | 0.889 | 0.942 | 0.889 | 0.889 | 0.891 |
| PH | F-Score | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 |
| | B-Accuracy | 0.500 | 0.500 | 0.500 | 0.500 | 0.500 | 0.500 |
| | Accuracy | 0.917 | 0.915 | 0.904 | 0.917 | 0.917 | 0.915 |

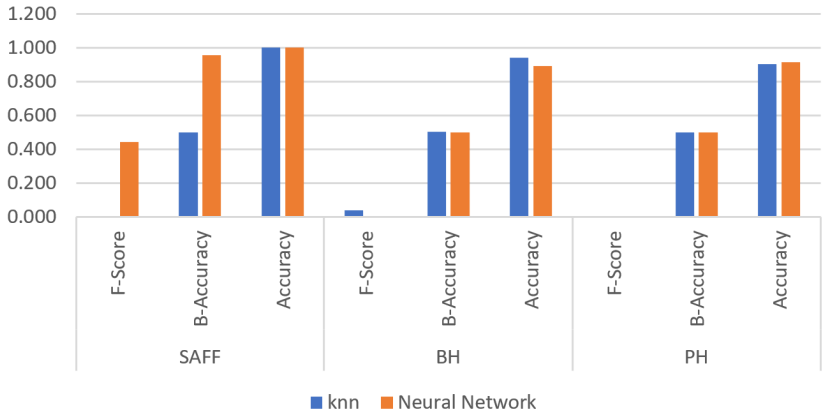
Table 5.6: ML-based Diagnosis results of each classifier using F-score, Balanced-accuracy and overall Accuracy




(a) Training




(b) Test




(c) New wafer

Figure 5.15: ML-based Diagnosis results of each classifier using F-score, Balanced-accuracy and overall Accuracy

## 5.5. Comparison & Discussion

This chapter explores two proposed approaches: DAT-based Diagnosis and ML-based Diagnosis for STT-MRAM defect identification and classification. Both methods were developed to understand defects and create effective solutions to detect them. DAT-based Diagnosis uses identifying features extracted from semi-expensive electrical measurements to label the devices with corresponding defect types. This approach shows the potential of automatic defect identification using behavioral rather than technology-dependent features. By deriving identifying features using fitting functions and applying threshold values from one-class classification techniques, we could identify defects in STT-MRAM

devices. However, the identification is not validated using PFA techniques to confirm the defects. Another limitation of DAT-based Diagnosis is the assumption that the chosen identifying features may also cover other defects, such as Side-wall defects.

On the other hand, ML-based Diagnosis harnessed the power of machine learning to classify defects based on low-cost MTJ features. By utilizing algorithms and models like K-nearest Neighbors and Neural Networks, this approach showed an efficient way to detect defects in terms of cost. By training the models on labeled data, we established a framework for defect classification. The resulting F-scores and Balanced Accuracy metrics show the method's potential for accurate defect classification. The results have shown that SAFF defects can be well classified, which can contribute to the feature correlation between its identifying feature and the low-cost features. The Back-Hopping and Pinhole defects are poorly classified because the low-cost features are not well correlated with their identifying feature. The main limitation of this methodology is that the models are trained with the assumption that the DAT-based Diagnosis is solid since it is used to label the training data for the machine learning models.

Comparing these two methodologies, DAT-based Diagnosis shines in its precision in identifying specific defects using behavioral identifying features. On the other hand, ML-based Diagnosis presents a more generalized approach that can efficiently classify defects using broader features extracted from low-cost measurements. The most suitable method depends on the desired defect detection precision and the measurement cost.

# 6

# Conclusion

This final chapter summarizes the findings and insights from this thesis to explore methodologies for defect identification and classification of STT-MRAM devices using novel and machine learning techniques. The primary objective of the thesis was to develop efficient and accurate solutions for diagnosing defects in emerging STT-MRAM technology due to its magnetic properties. The methodologies were systematically developed and evaluated to provide the benefits and limitations for further research. The first two chapters 2 and 3 discussed the principles of STT-MRAM technology and conventional VLSI test and diagnosis methodologies as the foundation for the following chapters, where the proposed methods were introduced and evaluated. Chapter 4 discussed the DAT-based and ML-based Diagnosis methodologies and the theoretical understanding of the methodologies. Chapter 5 discussed the implementation of the methodologies on real chips developed at IMEC imec and analyzed using the proposed methodologies. The thesis also discussed March-based Diagnosis building upon the DAT-based Diagnosis targeting industrial chips with built-in sense amplifiers, leading to an accepted paper, see appendix A.

The DAT-based Diagnosis is a structured approach to label STT-MRAM data with defect types using identifying features automatically extracted from specialized measurements to maximize defect detection accuracy. The method proved accurate for defect identification based on understanding the defect's impact on the MTJ parameters and their evolution over other quantities, such as time. The ML-based Diagnosis presents the potential of machine learning models such as K-Nearest Neighbors and Neural Networks in classifying defects based on MTJ features extracted from low-cost measurement to minimize measurement costs and maximize defect detection accuracy.

The experimental validation of the methodologies showed that both DAT-based and ML-based Diagnosis produced expected and desirable outcomes. DAT-based Diagnosis effectively identifies defects using relatively expensive identifying features. ML-based Diagnosis demonstrated its strength in utilizing machine learning models and algorithms to achieve robust defect classification using low-cost MTJ features. However, both methods showed certain theoretical and experimental limitations. DAT-based Diagnosis assumes that the theory behind developing the identifying features is solid without validating using Physical Failure Analysis. With this in mind, ML-based Diagnosis employs training data labeled using the DAT-based Diagnosis identification approach, assuming the solidity of the identification process. Examining data distributions, feature correlations, and evaluating machine learning models using F-score and Balanced Accuracy presented challenges in classifying Pinhole and Back-Hopping defects, likely due to an insufficient understanding of the defect's behavior over time or other related variables. Therefore, an outlier analysis is performed to guide future research in analyzing outliers to optimize the compact MTJ defective model.

The methodologies presented in this thesis provide a solid framework for future research and development to enhance the diagnosis process for STT-MRAM devices. While DAT-based and ML-based Diagnosis methods have shown potential in defect identification and classification, further refinement is required to provide a more robust, efficient, and accurate diagnosis process. Further research could enhance the precision of the DAT-based Diagnosis by introducing identifying features for new defects.

In addition, advanced PFA techniques are required to validate the introduced identifying features. ML-based Diagnosis aims to map low-cost MTJ features to defect types by training a machine learning model using predefined labeled data. Future research can explore additional MTJ features using more advanced machine learning models to close the bridge between MTJ parameters and defect types. The thesis has touched upon the potential of creating a complete feature space representing the deviation of the defective MTJs from the defect-free devices. The feature space should contain behavioral features from various measurements showcasing the defective behavioral variation of the devices, leading to a more comprehensive and adaptive defect identification system.

In conclusion, this thesis marks significant progress toward addressing STT-MRAM defect identification and classification challenges. The methodologies proposed in this thesis offer a different perspective, integrating machine learning with domain-specific knowledge to improve STT-MRAM technology diagnosis and contribute to developing and commercializing emerging memory technologies.

# A

# Scientific Paper

In this appendix, you will find the accepted paper that has emerged from this thesis. The paper represents an extension of DAT-based Diagnosis on industrial chips. I am honored to announce that the paper has been accepted at the Asian Test Symposium (ATS), highlighting its contribution to the field and its significance of the research conducted during this thesis. Please refer to the paper on the next page and I also thank all the authors for their contribution to the research.

# Device Aware Diagnosis for Unique Defects in STT-MRAMs

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***Abstract*—Spin-Transfer Torque Magnetic RAMs (STT-MRAMs) are on their way to commercialization. However, obtaining high-quality test and diagnosis solutions for STT-MRAMs is challenging due to the existence of unique defects in Magnetic Tunneling Junctions (MTJs). Recently, the Device-Aware Test (DA-Test) method has been put forward as an effective approach mainly for detecting unique defecting STT-MRAMs. In this study, we propose a further advancement based on the DA-Test framework, introducing the Device-Aware Diagnosis (DA-Diagnosis) method. This method comprises two steps: a) defining distinctive features of each unique defect by characterization and physical analysis of defective MTJs, and b) utilizing march algorithms to extract distinctive features. The effectiveness of the proposed approach is validated in an industrial setting with real devices and data measurement.**

***Index Terms*—STT-MRAM, unique defect, test, diagnosis, device-aware method.**

## I. Introduction

Spin-Transfer Torque Magnetic RAMs (STT-MRAMs) have emerged as a promising technology thanks to their competitive writing performance, low power consumption, retention, and endurance [1]. Since its early commercialization in 2006, world-leading foundries and producers (such as TSMC, Samsung, Intel, and Everspin) have entered the MRAM market, leading to a substantial increase in single-chip storage capacity from 4 MB to 1 GB [1–5]. Further development of such chips requires high-quality testing and diagnosis methods.

Previous works on STT-MRAM testing and diagnosis can be classified into two types: works on conventional defects and works on unique defects in Magnetic Tunneling Junctions (MTJs). Works on conventional defects, such as the interconnect and contact defects, assume that such defects can be modeled as *linear resistance*; they are mainly based on march algorithms [6–13], similar to what has been done for DRAMs and SRAMs [14,15]. On the other hand, simply modeling unique defects in MTJs with linear resistance results in a low-quality test solution [16–18]; physical mechanism of unique defects involves both the magnetic field impact and the spin-transfer torque (STT) effect. To solve this challenge, the Device-Aware Test (DA-Test) method is introduced [17,18]. The DA-Test approach refers to characterizing unique defects, and designing a specific compact model for the defective MTJ that incorporates the impact of physical defects into the technology parameters of the device, leading to more accurate test solutions for unique defects [18–20]. However, all these works only focus on detecting unique defects, while no research has been conducted on the diagnosis of these defects. Especially, while the DA-Test method has demonstrated advantages in testing unique defects, it is not well-suited for diagnosing these defects, as its primary optimization lies in fault detection rather than defect recognition. For example, one test solution, such as the one proposed for Pinholes [19], may detect multiple defects at the same time, thus infeasible in diagnosis. Therefore, a dedicated diagnosis approach for unique defects becomes essential to enhance the yield learning of STT-MRAMs.

This work presents the Device-Aware Diagnosis (DA-Diagnosis) framework, which builds upon the structure of DA-Test but takes a further step towards specializing in recognizing defects. In the DA-Diagnosis framework, the diagnosis is achieved by employing a primitive march algorithm to extract distinctive features of each unique defect. Through measurement data in real chips, we demonstrate that the DA-Diagnos approach is cost-effective, flexible, and practical in diagnosing unique defects for STT-MRAMs. Contributions of this work are as follows:

- Present the framework of the DA-Diagnosis method for unique defects in STT-MRAMs.
- Define distinctive features of four unique defects in MTJs.
- Design the primitive march algorithm by extracting distinctive features for each unique defect.
- Prove the effectiveness of the DA-Diagnosis method through measurement data for STT-MRAM chips.
- Evaluate the merits and limitations of the proposed DA-Diagnosis methods.

The rest of this paper is organized as follows. Section II introduces the STT-MRAM basics. Section III introduces the STT-MRAM array used in this work, the set-up of characterization, and the targeted unique defects. Section IV offers the framework of the DA-Diagnosis method for unique defects in STT-MRAMs. Section V applies the proposed DA-Diagnosis framework to the targeted unique defects. Section VI concludes this paper.

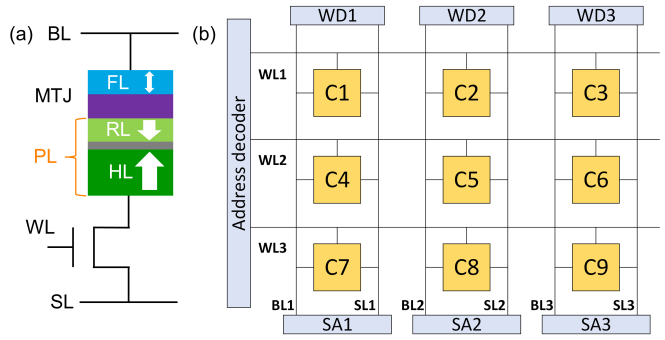


Fig. 1. (a) Simplified MTJ stack and 1T-1M cell, (b) STT-MRAM array.

## II. Background

This section introduces the basic principle of the MTJ device, 1T-1M cell, and the STT-MRAM array.

### A. MTJ device

The fundamental data storage element in STT-MRAMs is the MTJ; it demonstrates the one-bit data storage by encoding two bi-stable resistance states.

Fig. 1 (a) presents the simplified schematic of an MTJ. Typically, the MTJ consists of an ultra-thin dielectric Tunnel Barrier (TB) sandwiched between a Free Layer (FL) and a Pinned Layer (PL). The FL is a thin ferromagnetic layer, whose magnetization can be switched through write operations. The TB is a thin insulator made of MgO. The PL is a multiple-layer stack composed of Reference Layer (RL), a thin metal spacer, and Hard Layer (HL). The MTJ has two stable resistance states depending on the magnetization direction of FL and RL. If the magnetization of the two layers is in parallel, the MTJ presents low resistance (i.e., P or '0' state); if in anti-parallel, the MTJ presents high resistance (i.e., AP or '1' state). By applying a current through the device, the MTJ state can be switched between 'P' and 'AP' states.

### B. 1T-1M cell

Fig. 1 (a) illustrates the structure of a 1 Transistor - 1 MTJ (1T-1M) bit cell with three terminals connecting to the Bit Line (BL), Source Line (SL), and Word Line (WL). During write operations, the voltage of WL selects the cell, and the voltage between the BL and SL controls the operation type. For example, the $1w0$ operation is performed by connecting the BL to $V_{\mathrm{DD}}$ and the SL to the ground, generating a writing current flowing through the MTJ, and switching the MTJ state from AP to P. In read operations, a small read current $I_{\mathrm{rd}}$ is offered to detect the MTJ resistance while avoiding unwanted state switches.

### C. STT-MRAM array

Fig. 1 (b) presents a 3×3 STT-MRAM array with associated peripheral circuits. In the array, cells in the same row share the same WL, and cells in the same column share the same BL and SL. The peripheral circuit consists of the address decoder, the Write Driver (WD), and the Sense Amplifier (SA). The address decoder selects the device, the WD applies the write and read pulses, and the SA detects the device states.

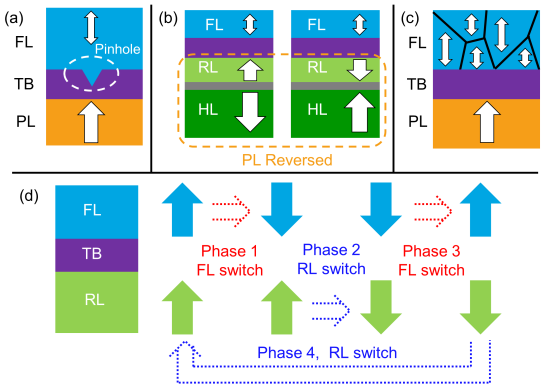


Fig. 2. Mechanisms of defects (a) Pinholes, (b) SAFF, (c) IM, (d) BH.

## III. Experiment Set-up

This section introduces an overview of a) the experiment set-up, and b) the basics of the targeted defects in this work.

### A. Measurement and test set-up

In this work, we perform measuremens on a $1\,\mathrm{Mbit}$ STT-MRAM array (structure same as Fig. 1 (b)). The MTJ Critical Diameter (CD) is $60\,\mathrm{nm}$, and the pitch (distance between neighboring cells) is $200\,\mathrm{nm}$. Additional efforts have been dedicated to circuit design, enabling direct characterization of the 1T-1M cell, which is not typically found in commercial STT-MRAM productions [21]. For example, we are able to extract the resistance of the entire 1T-1M cell ($R_{cell}$) between BL and SL (as in Fig. 1 (a)). This allows us to perform both device-level characterization and circuit-level read/write operations on the same STT-MRAM chip.

### B. Targeted defects

This study targets diagnosing four unique defects in STT-MRAMs: Pinhole [19,20], Synthetic Anti-Ferromagnet Flip (SAFF) [22], Intermediate-state (IM) [23,24], and Back-hopping (BH) [25,26]. These defects are selected because they have been well-studied, and the DA-Test method has been successfully applied to them [18]. Notice that some unique defects are not included here since their mechanism has not been fully understood. The methodology outlined in this work can potentially be applied to them, yet further investigations on the physical mechanisms have to be conducted. To guarantee that each of the four unique defects can also be distinguished from conventional defects, we conduct Spice simulations to observe the STT-MRAM faulty behaviors in the presence of all possible interconnect and contact defects by following the process in [27], which will not be discussed extensively here. The basic of the four unique defects is presented as follows:

*1) Pinholes [19,28]:* The Pinhole is introduced by the physical imperfection in the MgO or the FL/MgO interface, as presented in Fig.2 (a). This defect has a significant impact on the MTJ tunneling performance, resulting in degradation of MTJ resistance and Tunnel Magneto Resistance (TMR), and further introduces incorrect read destructive faults like $< 1r1/0/0 >$ (i.e., perform the read '1' operation on an MTJ with initial state '1', but the final state becomes '0').

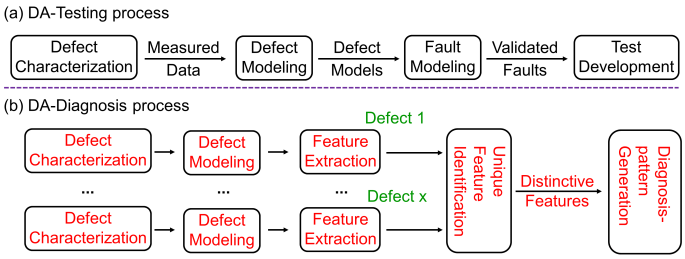


Fig. 3. Framework of STT-MRAM test and diagnosis development

*2) SAFF [22]:* As presented in Fig. 2 (b), the SAFF defect occurs when the PL magnetization gets unexpectedly reversed during manufacturing. This leads to a reversal of the RL magnetization due to the coupling effect [29]. SAFF leads to a high Write Error Rate (WER) depending on the neighbor cell states, and may cause intermittent passive neighborhood pattern sensitive faults [22].

*3) IM [23,24]:* The IM defect, as shown in Fig. 2 (c), occurs when the FL is not unified. In contrast to the '0' and '1' states, the IM-defective cell may enter a specific stable intermediate state between two regular states when only a portion of the FL gets switched. Therefore, hard-to-detect write faults are observed for IM-defective cells, like $< 1w0/U/- >$ (i.e., perform the write '0' operation on an MTJ with initial state '1', but the final MTJ state becomes an undefined state 'U' between regular '0' and '1' states).

*4) BH [25,26]:* The BH, as demonstrated in Fig. 2 (d), is caused by the unstable RL. When a write pulse is applied, the RL with low stability undergoes an unexpected switch, subsequently triggers a sequence of FL or RL switches, and forms a four-phase loop (Fig. 5 (a)). The BH-defective device continuously oscillates between the '0' and '1' states during write operations, resulting in a high WER.

## IV. Methodology

This section introduces the DA-Test/Diagnosis frameworks.

### A. Framework of DA-Test

Fig. 3 (a) illustrates the framework of the DA-Test process for STT-MRAMs with four steps [17,18]:

*1) Defect Characterization:* This step characterizes defect features by measuring defective MTJ performance with electrical and magnetic approaches.

*2) Defect Modeling:* This step aims to model manufacturing defects. While conventional defects are modeled as resistors [14], unique defects require the DA-Test, which integrates the impact of physical defects into parameters of regular MTJ models, and obtains defective MTJ models.

*3) Fault Modeling:* This step defines the fault space and validates it through circuit-level (Spice) simulations.

*4) Test Development:* This step generates the test solution for all validated faults through march-based or Design For Test (DFT) approaches.

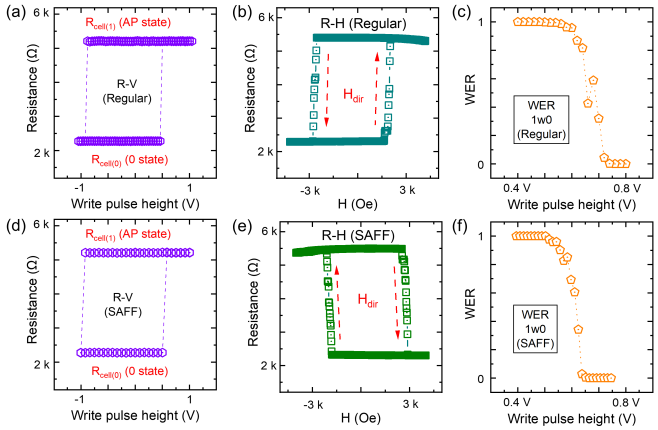


Fig. 4. Characterization of defect-free device: (a) R-V, (b) R-H, (c) WER; Same characterization of SAFF-defective device: (d) R-V, (e) R-H, (f) WER.

### B. Framework of DA-Diagnosis

The DA-Test is optimized to detect faults, yet does not provide the distinctiveness for defects. For example, the march test algorithm designed for detecting Pinholes in [19] may detect other defects such as BH. In this work, we introduce the DA-Diagnosis process, a new approach that identifies each defect through unique features, and provides march-based diagnosis solutions. As presented in Fig. 3 (b), the DA-Diagnosis method follows five steps:

*1) Defect characterization:* This step involves characterizing MTJs. In this work, we apply three common measurement methods: R-V measurement, R-H measurement, and WER extraction. For example, measurement data for defect-free devices are presented in Fig. 4 (a) - (c), compared with those for SAFF-defective devices in Fig. 4 (d) - (f).

*2) Defect modeling:* This step designs models for manufacturing defects. In this work, we directly adopt defect models from previous works [19,23,23,26].

*3) Feature extraction:* This step extracts the features of defective devices based on the characterization and physical analysis. Here, features refer to the electrical or magnetic parameters that can be extracted from the measurement data. All possible features from the three measurement methods are extracted, such as summarized in TABLE I (next section).

*4) Unique feature identification:* The three steps above will be repeated for the four unique defects (by measurement) and all possible conventional defects (by simulation). This step forms the feature-dictionary by concluding all the features of both conventional and unique defects. Distinctive features are then extracted for each unique defect. Here, a distinctive feature refers to the parameter behaving uniquely to a specific defect, thus allowing for the diagnosis. For example, the reversed R-H hysteresis loop direction (reversed $H_{dir}$) extracted from the R-H measurement is the only distinctive feature of SAFF, as presented in Fig. 4 (b) and (e); while other measurements show the same features for both SAFF-defective and defect-free STT-MRAM cells.

*5) Diagnosis pattern generation:* This step generates the diagnosis solutions to recognize distinctive features. Here,

we only apply the march-based diagnosis method, which is time-efficient and practical for STT-MRAM arrays. Other methods, like device characterization and Physical Failure Analysis (PFA), are not considered. Characterization methods for prototype MTJs are usually not practical for *STT-MRAM arrays*, such as the R-V measurement, where it is infeasible to directly extract the MTJ resistance from the structure shown in Fig. 1 (b). PFA methods, like Transmission Electron Microscopes (TEM), are usually costly, time-consuming, and destructive [30]. The final output of the DA-Diagnosis method is the march algorithm for diagnosing each unique defect. If regular march algorithms cannot diagnose certain types of unique defects, additional approaches are applied, like the external magnetic field. For example, the march-based diagnosis for SAFF requires the external magnetic field, which is presented as: $\{\Updownarrow(w0); \Updownarrow(w0_{Hext}); \Updownarrow(r0)\}$. This march algorithm consists of three steps: a) apply $w0$ to all devices for initialization, b) apply an external magnetic field for the whole chip to perform the $w0$ operation, c) apply $r0$ operation to all devices (Details will be discussed later).

Notice that the process variation does not affect unique features of defects, hence no impact on the diagnosis method.

## V. Application of the methods for STT-MRAMs

This section applies DA-Diagnosis for four targeted unique defects. The order we present the four unique defects depends on their frequency of occurrence in our measurement/test data (i.e., Pinhole, BH, SAFF, IM).

### A. Defect characterization

In this step, we first perform the three measurement methods (i.e., R-V, R-H, and WER extraction) on all the devices of 1 MB STT-MRAM cells; an example of results is shown in Fig. 4 for SAFF. To save space, other measurement data is not shown. On the other hand, we extract the MTJ faulty behaviors in the presence of all possible interconnect and contact defects through spice simulations, following the process in [31].

### B. Defect modeling

As device-aware defect models of the four targeted unique defects are reported in our previous works [19,22,23,26], we therefore make use of them directly.

### C. Feature extraction

In this step, we summarize all the features we extracted from the R-V, R-H, and WER measurement data for the four unique defects as well as the interconnect & contact defects; the results are reported in TABLE I.

TABLE I. Feature-dictionary of defects

| | R-V | | | R-H | WER |
|---|---|---|---|---|---|
| | $R_{cell-0}$ | $R_{cell-1}$ | $R_{cell-IM}$ | $H_{dir}$ | |
| Pinhole | ↓ | ↓ | NA | NA | NA |
| SAFF | NA | NA | NA | RD | ↕ |
| IM | NA | NA | IB | NA | ↑ |
| BH | NA | NA | NA | NA | ↑ |
| Interconnects & contacts | ↓, ↑, NA | ↓, ↑, NA | NA | NA | ↓, ↑, NA |

Where the symbols used in the table are described below:

| | |
|---|---|
| $R_{cell-0}$ | Cell resistance in state '0' |
| $R_{cell-1}$ | Cell resistance in state '1' |
| $R_{cell-IM}$ | Cell resistance in state intermediate state |
| $H_{dir}$ | R-H hysteresis loop direction |
| WER | Write error rate |
| ↑ | Increase |
| ↓ | Decrease |
| RD | Reversed direction |
| NA | Not affected |
| ↕ | Higher or lower depending on neighboring cells |
| IB | Intermittent behavior |

The last row presents all possible situations with the presence of interconnect and contact defects; for instance, $R_{cell}(0)$ may increase, decrease, or stay constant depending on the nature of the interconnect and contact defects. As an example, Fig. 4 shows the results for SAFF, from which the corresponding features are extracted, and included in TABLE I.

### D. Distinctive feature identification

This step extracts the distinctive features of each unique defect. A feature is considered distinctive if it behaves uniquely within the column of TABLE I. For example, the intermittent behavior (IB) of the $R_{cell-IM}$ is identified as the distinctive feature for IM; yet the WER increasing (↑) is not a distinctive one, since this behavior is also observed in the presence of BH and conventional defects. Consequently, the distinctive features of SAFF and IM can be directly derived from TABLE.I; $H_{dir}$ is the distinctive feature of SAFF (i.e. RD), and and the $R_{cell-IM}$ is the distinctive feature of IM (i.e. IB). However, for Pinhole and BH there is no distinctive feature that can be directly extracted from TABLE.I. Hence, there is a need for 'secondary features' extraction, to ensure distinctive features(s) for each unique defect. Next, we present how we do this for Pinhole and BH:

*1) Pinholes:* As presented in TABLE I, the major feature of Pinhole is the reduced $R_{cell-0}$ and $R_{cell-1}$. However, other defects may also exhibit the same feature, like an interconnect defect between BL and SL of the cell (see Fig. 1). To identify the distinctive feature of Pinhole, we rely on the aid of physical analysis. It has been demonstrated that the MgO of the Pinhole-defective MTJ is vulnerable. When applying the stress test by repeating write operations, the MgO of Pinhole-defective devices experiences further damage, thus further lowering the MTJ resistance [20]. In contrast, the stress test has a negligible impact on the MgO of defect-free MTJs, and on the MTJs with other defects. Therefore, we define the distinctive 'secondary feature' as $\alpha(R_{cell-1}) = R_{cell(measured)}/R_{cell(defect-free)}$, being the ratio of the measured $R_{cell}$ compared with that of a defect-free $R_{cell}$ when MTJ in the '1' state; $\alpha$ refers to the ratio. Fig. 5 (a) compares $\alpha(R_{cell-1})$ behaviors under the stress test for pinhole-defective cells, a defect-free cell, and a cell with an interconnect defect. Clearly $\alpha(R_{cell-1})$ of the Pinhole-defective cell decreases with more write cycles, yet $\alpha(R_{cell-1})$ of cells with other defects remains constant.

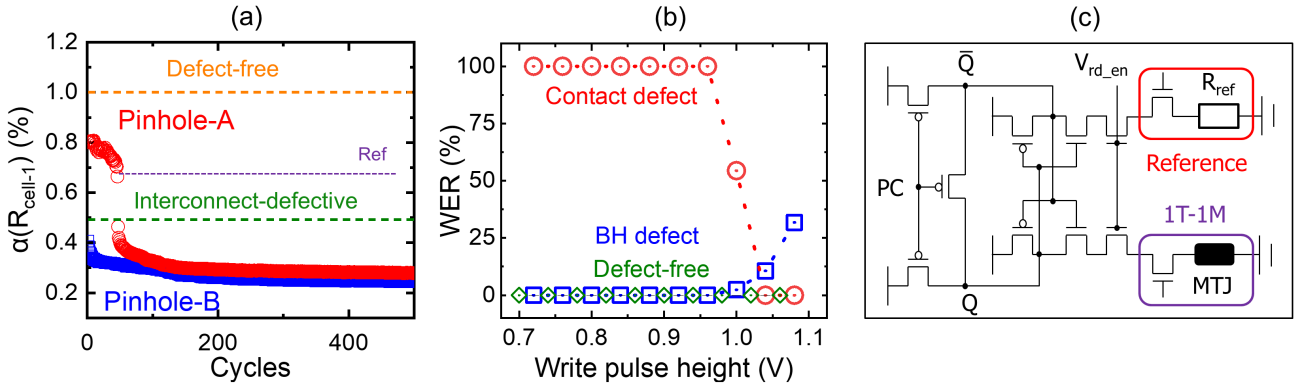


Fig. 5. (a) Unique feature identification for Pinholes, (b) Unique feature identification for BH, (c) SA structure

*2) BH:* As presented in TABLE I, a high WER is the major irregular feature for BH, yet this is not a distinctive one. Other defects, such as a contact defect between BL and the MTJ, can also cause a high WER. Hence, the 'secondary feature' is necessary. Here, we extract the WER with different write pulse heights. The 'secondary feature' is '$\alpha(WER)$', defined as how WER changes with the write pulse height increasing. For BH-defective MTJs, the range of $\alpha(WER)$ is limited considering the MTJ state oscillation; when the write pulse height increases, the WER undergoes only slight changes, without exhibiting extremely high or low values. In contrast, the WER of MTJs with other defects will either approach 100% or 0% with the increase of write pulse height. Fig. 5 (b) compares $\alpha(WER)$ behaviors of a BH-defective cell, a defect-free cell, and a cell with a contact defect. Clearly $\alpha(R_{cell-1})$ increases a bit for the BH-defective cell, but it decreases dramatically and eventually closes to 0 for the cell with a contact defect. Notice that how WER changes with write pulse depends on various factors like the BH defect strength [26].

### *E. Diagnosis-pattern generation*

This step generates the diagnosis patterns. The final output of this step is a set of march algorithms that can be practically performed on industrial STT-MRAM chips. Next, we present how to design the algorithm for each targeted unique defect. TABLE II summarizes the final result of this section.

*1) Pinholes:* While $\alpha(R_{cell-1})$ serves as the distinctive feature of Pinhole, the STT-MRAM cell resistance cannot be directly extracted through the STT-MRAM array. For example, we utilize the march algorithm: $\{\Updownarrow (w1, r1)^i\}$ to diagnose Pinhole, indicating repeating $w1$ and $r1$ operations for 'i' times, where $i \geq 30$ according to our measurement. The effectiveness of this march algorithm depends on the SA structure and the defect strength (i.e. Pinhole area [19]). Our work applies the regular SA as given in Fig. 5 (c). If $R_{cell} \geq R_{ref}$, then SA gives '1', otherwise '0'. For the two Pinhole-defective devices depicted in Fig. 5 (a), only device-A can be diagnosed; the read operations initially provide correct results, followed by incorrect results, with repeating write operations. Yet, if the Pinhole-defective $R_{cell}$ is initially lower than $R_{ref}$ (e.g., device-B), read operations initially provide wrong results, making it impossible to distinguish between Pinholes and other defects. Applying multiple reference resistors in the SA, such as in [20], may diagnose a broader range of Pinholes, but it never guarantees to diagnose all Pinholes.

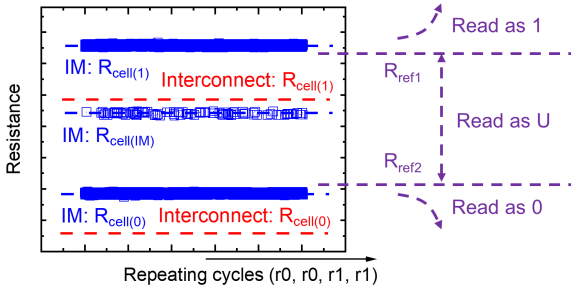


Fig. 6. Diagnosing for IM

*2) BH:* $\alpha(WER)$ is the distinctive feature of BH, it can be extracted from the STT-MRAM array in three steps: a) Set up the write pulse height $V_p$ properly (i.e. spec); b) Apply march algorithm $\{\Updownarrow (w0, r0)^i\}$, where 'i' depends on the targeted WER; c) Repeat steps a) and b) with $V_p' = 2V_p$. The BH is diagnosed if read operations provide wrong results in both steps b) and c). Notice that we can also adjust write pulse width rather than pulse height for the BH diagnosis.

*3) SAFF:* $H_{dir}$ is recognized as the distinctive feature of SAFF. However, the R-H measurement cannot be applied to regular STT-MRAM arrays, since the STT-MRAM cell resistance cannot be directly extracted. Hence, we apply the following algorithm to observe $H_{dir}$ : $\{\Updownarrow (w0); \Updownarrow (w0_{Hext}); \Updownarrow (r0)\}$. This march algorithm consists of three steps: a) apply $w0$ for initialization, b) apply an external magnetic field, and c) apply $r0$ operation to detect the final state. In the presence of SAFF, the state of the faulty cell will flip to '1'; hence diagnosis is guaranteed.

*4) IM:* $R_{cell-IM}$ is recognized as the distinctive feature of IM. However, detecting $R_{cell-IM}$ is limited by the SA circuit. The SA applied in this work (Fig. 5 (c)) can only detect two states, and $R_{cell-IM}$ will be read either as '0' or as '1'. Hence, IM can never be detected nor diagnosed. To overcome this limitation, multiple reference resistors are required for the SA. For example, the results presented in Fig. 6 are obtained by such SA utilizing two reference resistors to detect three states: '0', '1', and 'U', representing the intermediate state.

TABLE II. CONCLUSION OF DIAGNOSIS FOR UNIQUE DEFECTS

| Defect | Mechanism | Related steps in STT-MRAM fabrication | Unique feature | Diagnosis patterns | Comments |
|---|---|---|---|---|---|
| Pinholes | Physical imperfections in MgO or FL/MgO interface [32] | MgO or FL deposition, Annealing [32] | $\alpha(R_{cell-1})$ | $\{\Updownarrow (w1, r1)^i\}$ | Higher coverage with multiple references |
| SAFF | PL magnetization reversed [22] | Unknown | $H_{dir}$ | $\{\Updownarrow (w0); \Updownarrow (w0_{Hext}); \Updownarrow (r0)\}$ | Require external magnetic field |
| IM | Non-unified FL [33] | Unknown | $P_{IM}$ | $\{\Updownarrow (w0, r0, w1, r1)^i\}$ | Require multiple references |
| BH | RL instability [25] | PL deposition [25] | $\alpha(WER)$ | 1.$\{\Updownarrow (w0, r0)^i\}$<br>2. adjust write pulse<br>3.$\{\Updownarrow (w0, r0)^i\}$ | Require the adjustment of write pulses |

However, it is important to note that other defects, such as the interconnect defect between BL and SL, may also cause the defective STT-MRAM cell state to be located in the 'U' range (see Fig. 6). Therefore, diagnosing IM requires the detection of all three states. To achieve this, we employ the march algorithm: $\{\Updownarrow (w0, r0, w1, r1)^i\}$, where $i \geq 10$ according to our measurement. Notice IM has an intermittent behavior. In the presence of contact or interconnect defects, the read operations will result *permanently* in 'U, 1' or in '0, U'. However, in the presence of IM, the read operations will result most of the time in '0, 1', and *intermittently* in 'U, 1' or '0, U'. Hence the difference between read values will distinct contact & interconnect defects from IM.

## VI. CONCLUSION AND DISCUSSION

This work shows the importance of device-aware defect modeling for defect diagnosis. Understanding how the defects impact the different technology parameters of the device, and hence also the electrical parameters of the device is of great importance. It facilitates the development of diagnosis algorithms that can efficiently distinguish the different unique features of the different defects. We demonstrated the superiority of the approach using industrial STT-MRAM chips.

## ACKNOWLEDGEMENTS

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