Extension of the Common-Mode Range of Bipolar Input Stages Beyond the Supply Rails of Operational Amplifiers and Comparators

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***Abstract*—When the input voltage of an operational amplifier or comparator with a bipolar input stage exceeds the range of normal operation, the polarity of the output signal reverses and the input bias current increases to excessive large values. Saturation of the input transistors restricts the sensing of differential voltages to a common-mode (CM) range roughly between the positive and the negative supply rails. This paper describes input stage configurations that not only provide solutions to prevent the signal reversal and the excessive increase of input bias current, but that also provide an extension of the CM range far beyond the supply rails, while the transconductance for differential input voltages remains constant. Integrated implementations of the input stages realized a CM range reaching +15 V at a single supply voltage as low as 1 V, while the input bias current was limited to 6 μA.**

I. Introduction

THE increasing number of battery-operated and low-power applications has created a need for integrated circuits operating at low supply voltages, even as low as 1 V. At such low supply voltages it is not imaginary that input signals exceed the supply voltage. This is, for instance, the case when the input signals of the low-voltage application originate from sources with larger supply voltages or from sensors with large common-mode disturbances. In input devices with a bipolar input stage, such as operational amplifiers (op amps) or comparators, one specific problem becomes apparent. Namely, if the common-mode (CM) input voltage exceeds the supply voltage rails, reversal of the output signal and an increase of input bias current occur due to saturation of the input transistors [2]–[4]. Reversal of the signal polarity in a feedback loop leads to instability or oscillations, and an increasingly large input bias current leads to breakdown of the input transistors. In comparators and in voltage followers, the same problem can occur if the voltage of just one input terminal exceeds the supply rails. To always guarantee correct operation of low-voltage op amps and comparators, prevention of these saturation problems is very important.

Previously, rail-to-rail input stages have been realized [1], which allow the CM-input voltage to exceed just beyond the two supply voltage rails without causing saturation of the input transistors. Also, circuits with signal-reversal protection for input signals going just beyond the rails (about 0.5 V) have been implemented before [2]–[4]. Those circuits prevent the output signal from reversing polarity when the input transistors saturate. In none of those circuits, however, is the excessive increase of the input bias current for large CM-input voltages limited.

In this paper solutions are described that provide an extension of the CM input range far beyond the supply rails, without signal reversal or an excessive input bias current. The input stage configurations are designed in such a way that transconductance is constant for the total (extended) CM range.

In Section II the problems caused by saturation of the input stage are explained in more detail, and we take a look at the existing input stage configurations that can prevent signal reversal. We will see that those existing input stage configurations do not satisfy the demand for a large CM range with signal reversal protection and limitation of the increasing input bias current. In Section III we present new input stage configurations that provide a solution for the saturation problems and an extension of the CM range beyond the supply rails. In Section IV the measurement results of the realized input stages are shown. Finally, Section V gives a conclusion.

II. Conventional Input Stages

In this section we analyze the saturation problems and the limitations on the CM range of conventional input stages in order to obtain a better understanding of the use and the operation of the novel input stages which will be presented in the next section.

First we take a look at what happens in an input stage when the CM-input voltage reaches either the upper or the lower limit of the CM range. A simplified schematic of a conventional n-p-n input stage is shown in Fig. 1(a). The input signal consists of a differential-mode component V_D, which is amplified by the input stage, and a common-mode component V_{CM}.

In case the CM-input voltage V_{CM} is raised too far above the positive supply voltage V_{CC}, the input transistors saturate and the base–collector (BC) junctions become forward biased. First the base currents increase to $1/2I_{EE}$ because of the decreasing current gain, but eventually the current through the forward-biased BC junctions makes the input bias current

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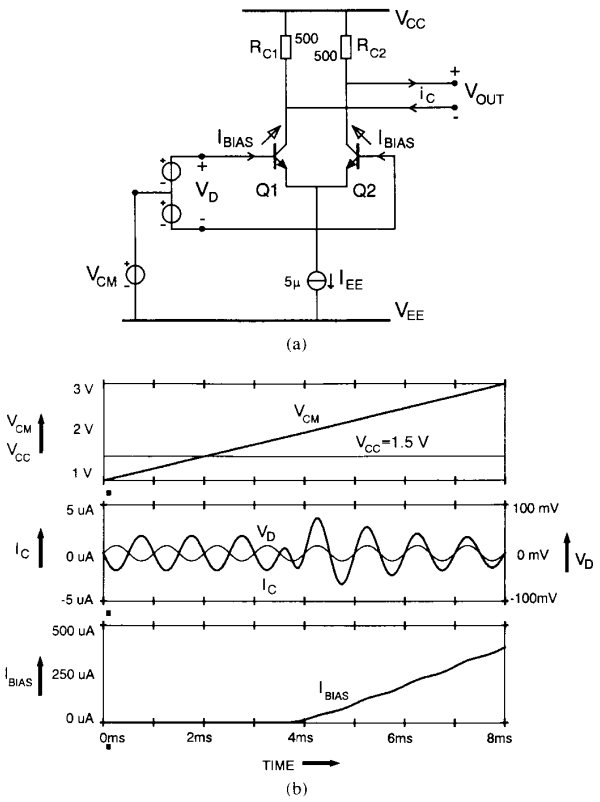

Fig. 1. (a) A conventional n-p-n input stage. (b) Simulation of the CM behavior.

increase to much larger values. Also, reversal of the output signal occurs because the BC junctions are no longer inverting the signal transfer, but become conductive so that the signal transfer is noninverting. In Fig. 1(b) the effects are demonstrated by a simulation. The upper plot in Fig. 1(b) shows the CM-input voltage slowly rising from 1 to 3 V as a function of time, while crossing the supply voltage of 1.5 V. The plot in the middle shows the sinusoidal differential input signal and the collector output signal of the input stage. The effect of signal reversal is clearly visible around $V_{CM} = 2$ V, at $t = 4$ ms. The lower plot in Fig. 1(b) shows how the input bias current I_{BIAS} rapidly rises from a small value (normal base current) to an excessive value, as soon as the input transistors become deeply saturated for V_{CM} rising more than 0.5 V above the positive supply. Both the effect of signal reversal and of excessive input bias current need to be avoided since they may lead to instability or breakdown of the circuit.

In case the CM-input voltage of the n-p-n input stage, shown in Fig. 1(a), is lowered and drops below 0.7 V, the current source I_{EE} saturates and, as a result, the bias current of the input stage and the amplification of the input signal decrease and finally diminish completely. This problem can be solved by adding a p-n-p input stage for the lower part of the CM range. However, a p-n-p input stage saturates for CM voltages falling too far below the negative supply, which causes the same problems as described for the n-p-n input stage.

The problem of signal reversal for CM voltages exceeding beyond the supply rails has been previously acknowledged. Three existing solutions to prevent signal reversal are explained below.

Placing diodes in series with the collectors, as shown in Fig. 2(a), simply prevents the collector current from flowing in the wrong direction. In input stage configurations in which current mirrors are used at the collectors of the input stage, a diode protection for signal reversal is inherently implemented. At high CM-input voltages, when the input transistors $Q1$ and $Q2$ saturate, diodes $D1$ and $D2$ block the currents and the signal through the forward-biased BC junctions. This way, signal reversal is prevented and, also, the increase of the input bias current is limited because the base currents of $Q1$ and $Q2$ in saturation are restricted to $1/2I_{EE}$. The operation of the reversal protection with diodes is demonstrated in Fig. 2(b). Clearly, in the middle plot, we see that the output signal does not reverse but is reduced to zero when the input transistors saturate for $V_{CM} = 1.4$ V, at $t = 1.6$ ms. When comparing the level of V_{CM} where the amplitude of the output signal approaches zero in Fig. 2(b) to the CM range in Fig. 1(b), we see that the CM range is reduced by one diode voltage of 0.6 V. Naturally, this reduction is because of the diode-voltage drop at the collectors. Rather than diminishing the signal amplitude to zero at the edge of a reduced CM range, as in Fig. 2, it is preferable to have a continuation of the output signal and an extension of the CM range.

The overcompensation method shown in Fig. 3(a) extends the CM range to the maximum possible for conventional input stages [2], [3]. Two double-size BC junctions $Q3$ and $Q4$ are placed in parallel to the input transistors $Q1$ and $Q2$ and are cross-coupled at the collectors. At high CM-input voltages, these extra transistor junctions prevent reversal of the output signal since the reversed signal at the collectors of the saturated normal input transistors is overcompensated by a larger signal of opposite polarity from the extra input transistors. The effect is shown in the simulation results of Fig. 3(b): the sinusoidal output signal does not change polarity for CM voltages above the supply. Unfortunately, the amplitude of the output signal does not stay constant but depends upon the CM-input voltage, which means that the transconductance of the input stage is not constant. Another disadvantage is that the input bias current still increases to excessive values for CM-input voltages exceeding more than 0.5 V beyond the supply voltage.

Another implementation of an input stage providing signal reversal protection by means of overcompensation is shown in Fig. 4 [4]. Transistors $Q11$ and $Q12$ operate as voltage-clamped current followers for CM voltages rising above the limits where the input stage $Q1, Q2$ saturates. The base–emitter (BE) junctions of the lateral p-n-p's $Q11$ and $Q12$ can be matched, in certain chip processes, to the BC junctions of the vertical n-p-n's $Q1$ and $Q2$, so that the emitter signals of $Q11$ and $Q12$ are related to the saturated-collector signals of $Q1$ and $Q2$ and can be used to correct the polarity of the signal at the output. Also, here the increasing input bias current is not limited since the input junctions are clamped to a reference voltage through cascode transistors $Q31$ and $Q32$.

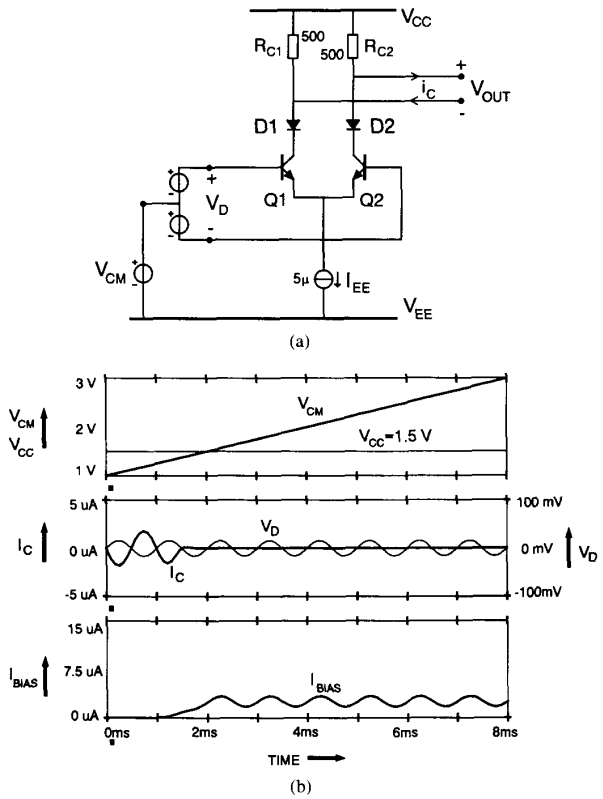

Fig. 2. (a) An input stage with output reversal protection using diodes. (b) Simulation of the CM behavior.

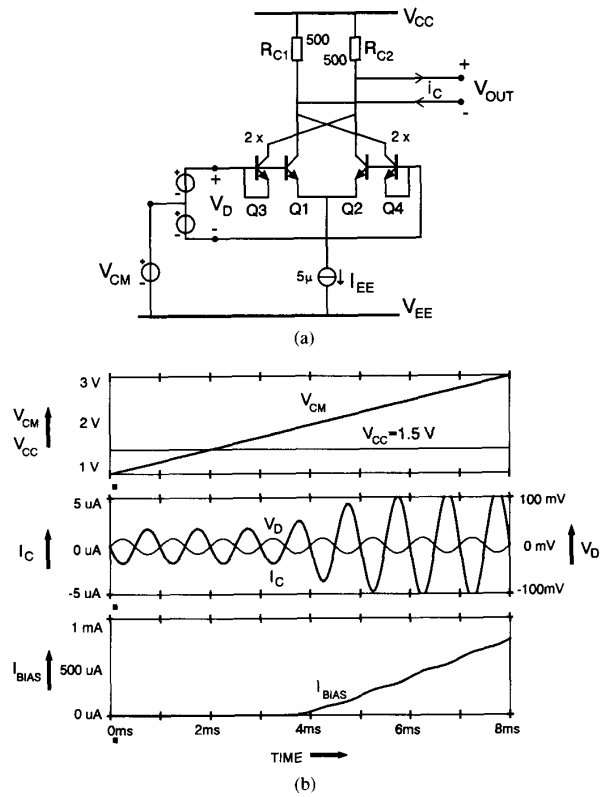

Fig. 3. (a) An input stage with output reversal protection using overcompensation. (b) Simulation of the CM behavior.

Similar principles as described in this section can be used to prevent signal reversal in a p-n-p input stage for CM-input voltages dropping below the negative supply rail.

Though the conventional input stages, explained in this section, can provide a protection for signal reversal, they do not provide a limitation of the increasing input bias current, nor allow CM-input voltages exceeding far beyond the supply rails.

III. Input Stages Providing Common-Mode Extension

In this section we will explain how by the use of an additional so-called common-base input stage an extension of the CM range far beyond the supply rails can be realized. First we will explain the properties of this additional input stage, and then we will explain the possibilities of combining this input stage with conventional input stages.

The occurrence of the saturation problems in op amps and comparators results from the fact that for input stages a common-emitter (CE) input stage configuration, as shown in Fig. 1(a), is always chosen, for reasons of power gain, noise, input resistance, input current, etc. When giving in on some of these parameters, a differential input stage in a common-base (CB) configuration, as shown in Fig. 5, can be chosen. This p-n-p configuration has no saturation limits on the input CM range around the positive supply voltage because the emitters are used as inputs.

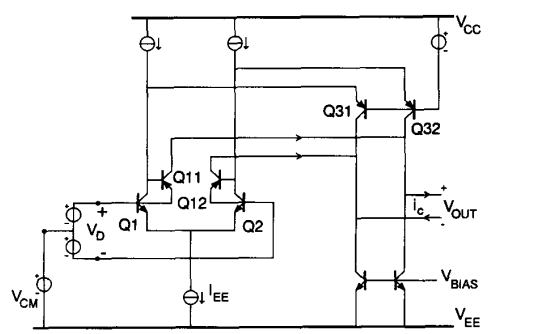

Fig. 4. An alternative input stage configuration with output reversal protection by means of overcompensation.

Each input is connected to the emitters of two parallel p-n-p transistors. The diode-connected transistors $Q3$ and $Q4$ are used for biasing, while the collectors of the other transistors, $Q1$ and $Q2$, are used to pass on the signal to the outputs. The input stage is built up differentially and biased by current source I_{EE} at node 1. The bias current of each transistor equals $1/2I_{EE}$, which sets the transconductance of the transistors. To determine the transconductance of the complete input stage, we first calculate the differential input resistance r_{in} of the input stage, which is defined by a series connection of two parallel

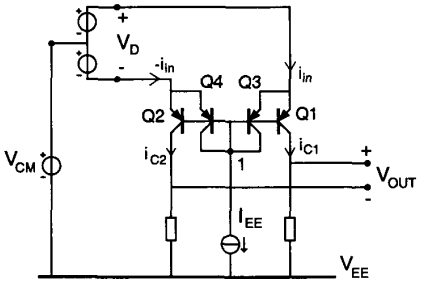

Fig. 5. A CB input stage for CM extension above the positive supply.

TABLE I
COMPARISON OF CB INPUT STAGE AND CE INPUT STAGE

	CE input stage	CB input stage
Transconductance	I_{EE} / $2V_T$	I_{EE} / $2V_T$
Input impedance	$4\beta V_T$ / I_{EE}	$2V_T$ / I_{EE}
Input bias current	I_{EE} / 2β	I_{EE}
Current gain	β	½

V_T= kT/q , β= transistor current gain, I_{EE}= tail current of differential pair

emitter resistances:

$$r_{in} = \frac{1}{g_{m1} + g_{m3}} + \frac{1}{g_{m2} + g_{m4}} = \frac{1}{g_m} = \frac{2kT}{q \cdot I_{EE}}. \quad (1)$$

The input voltage divided by this input resistance gives the input current signal i_{in}. Because the input current splits up equally into the two emitters at each input, the CB input stage operates as a current follower which passes on only half of the input current signal to each output. This means that the total transconductance G_m, defined as the ratio of the differential output current, $i_C = i_{C1} - i_{C2}$, to the differential input voltage v_D, is equal to

$$G_m = \frac{i_{C1} - i_{C2}}{v_D} = \frac{\frac{1}{2}v_D/r_{in} + \frac{1}{2}v_D/r_{in}}{v_D} = \frac{1}{r_{in}} = g_m = \frac{q \cdot I_{EE}}{2kT}. \quad (2)$$

The properties of the CB stage are summarized in Table I. The transconductance of the CB input stage is equal to that of a conventional input stage if the same value for the bias current I_{EE} is used.

The new circuit designs are based on combinations of a conventional CE input stage and the CB input stage of Fig. 5. It is important that the input stage configurations are designed in such a way that the added circuitry does not deteriorate the overall behavior for input voltages within the normal CM range, defined as the range in which a conventional input stage is operating. Another important demand is that the transconductance remains constant within the total CM range. This is especially important in op amps, where the transconductance of the input stage controls slewing rate, bandwidth, and stability [5]. In the novel input stage configurations these important demands are taken into account.

The following input stage configurations are presented to demonstrate the possibilities of CM extension. Firstly, a configuration for extension of the CM range of an n-p-n input stage above the positive supply rail is explained. Secondly, a similar CM extension circuit for a conventional p-n-p input stage is described. Thirdly, extension of the CM range below the negative supply rail is discussed. And, finally, we explain the limitations of the presented CM extension circuits.

A. CM Extension for n-p-n Input Stages Above the Positive Supply Rail

Fig. 6(a) shows a novel input stage configuration which consists of an n-p-n differential input stage $Q11, Q12$ and an additional CB input stage $Q21$–$Q24$. The biasing of these input stages is designed in such a way that the conventional n-p-n input stage operates in its own part of the CM range and the CB stage in the extended area of CM range above the positive supply. A folded cascode $Q31, Q32$ is used to add the collector signals of both stages. The outputs of the input stage configuration can be coupled on to a second stage, using V_{BIAS} for CM feedback or differential-to-single conversion [2], [3].

To clearly understand the principle of operation, imagine a slowly rising CM-input voltage as illustrated in the upper plot of the simulation shown in Fig. 6(b). When the CM-input voltage is low, the current I_{EE} flows through the two resistors at node 2 into diode-connected transistor $Q1$, biasing node 1 at a voltage $V_{CC} - 0.4$ V, node 2 at $V_{CC} - 0.6$ V, and node 3 at $V_{CC} - 0.8$ V. The current through $Q1$ is reflected into $Q3$ and $Q4$ for biasing the folded cascode circuit $Q31, Q32$, and is also reflected through $Q2$ and $Q5$ into $Q6$ for biasing the conventional input stage $Q11, Q12$. The collector signal of the conventional input stage flows into the emitters of the folded cascode circuit $Q31, Q32$ and creates an output signal V_{OUT}. When the CM-input voltage reaches $V_{CC} + 0.2$ V, transistors $Q21$–$Q24$, with their bases biased at node 1, become conducting and take over the reference current I_{EE}. As a result the current through $Q1$ is reduced, and the bias currents for the conventional input stage and for the folded cascode are turned off. The CB input stage amplifies the input signal with the same transconductance and passes it on with the correct polarity to the output V_{OUT}. In the small take-over range, where both input stages are operating, the transconductance stays constant as well because the sum of the bias currents of the two input stages always equals I_{EE} [2]. The second plot in Fig. 6(b) shows how the output signal continues with a constant amplitude when the CM voltage exceeds the saturation limit of the conventional input stage ($V_{CC} + 0.5$ V). A further increase of the CM voltage causes the voltage at nodes 1, 2, and 3 to rise as well, which prevents forward biasing of the BC junctions of $Q3$ and $Q4$. The BE junctions of $Q1$–$Q4$ are put further into reverse bias, but this does no further harm as long as breakdown is avoided. The voltage at the collector nodes of the conventional input stage

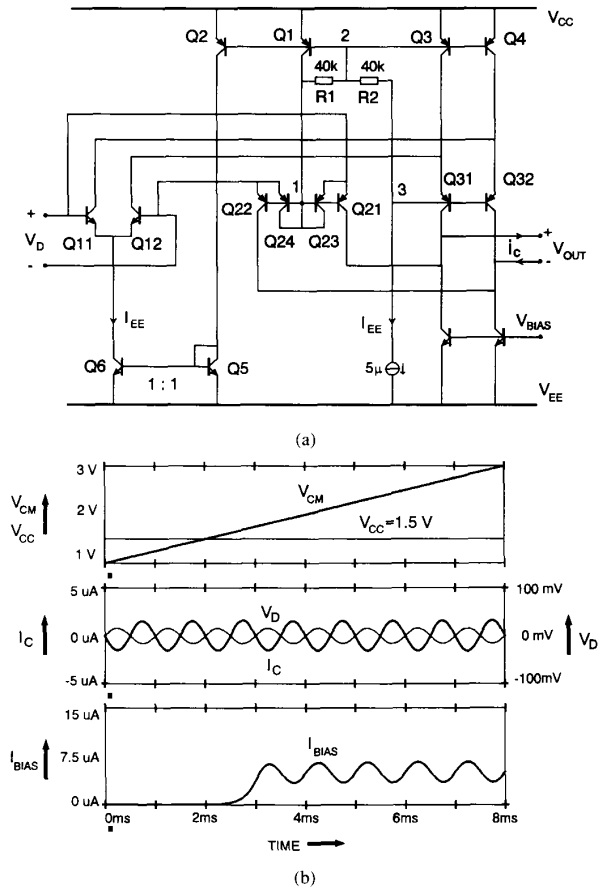

Fig. 6. (a) CM extension circuit for an n-p-n input stage. (b) Simulation of the CM behavior.

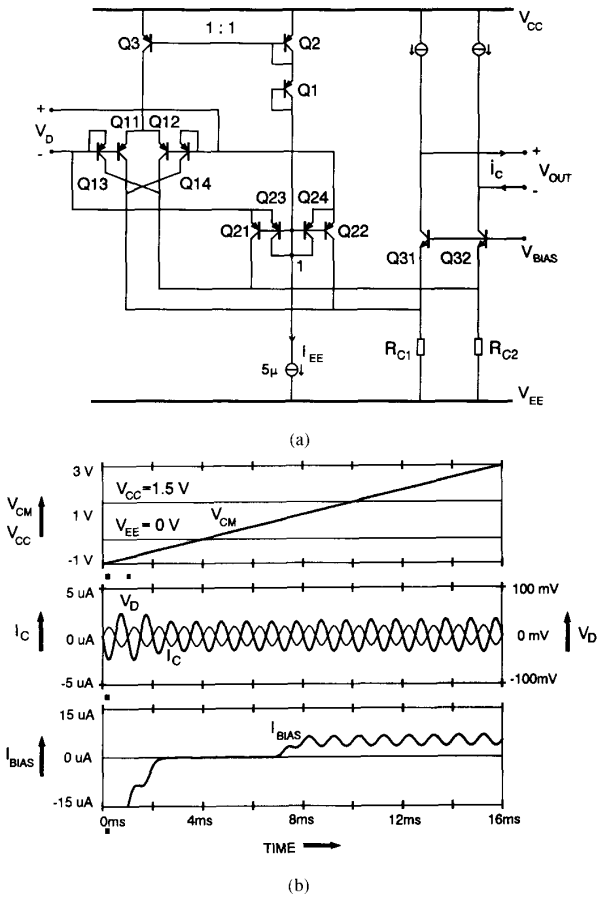

Fig. 7. (a) CM extension circuit for a p-n-p input stage. (b) Simulation of the CM behavior.

$Q11, Q12$ will also rise. This way, forward biasing of its BC junctions and increase of its input bias current are prevented. The last plot in Fig. 6(b) shows that the (dc, average) input bias current does not rise any further than 1 I_{EE}, the input current of the CB input stage.

Notice that the input stage configuration of Fig. 6(a) is biased in such a way that it can operate at supply voltages down to 1 V. Also we would like to point out that it is possible to combine the input stage with existing rail-to-rail input stage configurations [1]–[3], to achieve a CM range extending from the negative supply rail to far above the positive supply

B. CM Extension for p-n-p Input Stages Above the Positive Supply Rail

In Fig. 7(a) another input stage configuration is shown, which uses a conventional p-n-p input stage and a p-n-p CB input stage to extend the CM range beyond the positive supply rail. This input stage is designed especially for comparators. Vertical n-p-n input transistors cannot be used in comparators, because the large differential input signals of the comparator would lead to breakdown of the n-p-n BE junctions. Therefore, a CM extension circuit using only p-n-p input transistors is very useful.

In the circuit shown in Fig. 7(a), the conventional p-n-p input stage $Q11, Q12$ is combined with the CB differential stage $Q21$–$Q24$, using a very simple bias circuit $Q1$–$Q3$. This realizes a CM extension at the top of the CM range. To prevent the problem of signal reversal at the bottom limit of the CM range, transistors $Q13$ and $Q14$ are added for overcompensation, which however, does not provide more than 0.5-V CM extension below the negative supply rail (see Section II). One more-complicated CM extension circuit for a p-n-p input stage has been previously noticed in literature [6].

The principle of operation is similar to that of the previously explained input stage. The voltage at node 1 is biased by using two diodes, $Q1$ and $Q2$, connected to the supply. When the CM-input voltage rises above $V_{CC} - 0.6$ V, transistors $Q21$ and $Q22$ switch on and take over the bias current I_{EE}, turning off the current through the conventional input stage $Q11, Q12$. The CB input stage can take over just before saturation of $Q3$ starts to affect the operation of the conventional p-n-p input stage. The collector signals of both input stages are added in the cascode circuit $Q31, Q32$, and the total signal results at the outputs. The simulation results for a CM-input voltage varying from -1 to $+3$ V and a supply voltage of 1.5 V are shown in Fig. 7(b). The minimum supply voltage for the input stage

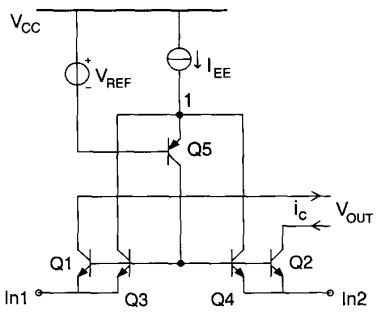

Fig. 8. A CB input stage for CM extension below the negative supply.

configuration of Fig. 7(a) is determined by two diode voltages and one saturation voltage, $2V_{BE} + V_{\mathrm{SAT}}$, which is about 1.3 V for small bias currents.

C. CM Extension Below the Negative Supply

Extension of the CM range below the negative supply rail would be very simple if the circuits presented above could just be turned upside-down replacing n-p-n's by p-n-p's and vice versa. However, we have to be aware of substrate diodes which become active when certain nodes are biased outside the voltage range between the supply rails. In a standard bipolar process, n-p-n transistors are implemented with an n-type collector, and p-n-p transistors with an n-type base, in a p-type substrate. Thus, there are large p-n diodes from the n-p-n collectors and from the p-n-p bases to the substrate, which is connected to the negative supply rail. Taking this fact into account for an input stage with CM extension below the negative supply rail means that n-p-n collector voltages and p-n-p base voltages always have to stay biased above the negative supply voltage.

The circuit shown in Fig. 8 is our proposed common-base n-p-n input stage, which can be used for CM extension below the negative supply rail. Inserting p-n-p transistor $Q5$ between the bases and the collectors of input transistors $Q3$ and $Q4$ makes it possible to separate the base and the collector voltages of these diode-connected transistors. The collectors of the n-p-n input transistors will now always stay biased at a voltage above the negative supply rail, even when the emitters and the bases of the input transistors are dragged down by the CM-input voltage to a level far below the rail. Several input stage configurations with the common-base n-p-n input stage of Fig. 8 are possible, as long as the restriction on the n-p-n collector voltages and the p-n-p base voltages is taken into account when designing the bias circuitry.

D. Limitations of the CM Extension Circuits

We would like to point out some general considerations about the CM extension circuits.

As mentioned previously, the limit of the extension of the CM range is determined by the breakdown voltages of the transistors. Relative to negative supply voltage, the BC breakdown voltage of p-n-p transistors (e.g., $Q21, Q22, Q31$, and $Q32$ in Fig. 6(a)) and of n-p-n transistors (e.g, $Q6$ and the transistor in I_{EE}) is the limiting factor. Relative to the positive supply voltage, the limit depends upon the BE breakdown voltage of p-n-p transistors ($Q1$–$Q4$). Whichever of these limits is the lowest determines the maximum of the extended CM range.

At first sight one may think that the added input transistors will affect specifications of the conventional input stage such as noise and input capacitance. However, because the extra input transistors are completely off when the conventional input stage is in operation, these effects are negligible. The properties of the presented configurations can easily be derived, given that within the normal CM range the conventional input stage is active and for the rest of the CM range the extra input stage is active. There is a small take-over range, in the order of 100 mV, where both stages are active and where there is a transition from one set of parameters to the other. Special care has to be taken with respect to properties like CM rejection in the take-over range.

The CM extension can only have effect if the often-used protection diodes between input terminals and the supply connections are omitted. This means that in order to protect the input stages from breakdown at very large input voltages, another kind of protection has to be used. We can, for example, consider using a series of diodes or Zener diodes for protection.

IV. Realizations and Measurements

The input stages of Figs. 6(a) and 7(a) have been realized on a semicustom chip with standard lateral p-n-p's and vertical n-p-n's. The photograph in Fig. 9 shows one of the integrated input stages. In a simple experiment we verified the operation of the CM extension of the input stages. Figs. 10 and 11 show oscilloscope plots resulting from experiments on the input stages of, respectively, Figs. 6(a) and 7(a). The triangular waveform indicates the CM-input signal slowly varying between -0.5 and +15 V. The single supply voltage is at 5 V and the input signal is a 1-kHz sine wave of 25-mV amplitude. The sine-wave signals on the scope plots indicate the measured output voltage across a 30-kΩ load. The plots prove that both input stages operate correctly for CM voltages far above the positive supply rail ($V_{CC} = 5$ V), and that the input stage of Fig. 7(a) also operates correctly for CM voltages around and below the negative supply rail ($V_{EE} = 0$ V). The measured CM-input ranges and the minimum supply voltages of the input stages of Figs. 6(a) and 7(a) are shown in Table II. The limits of the extension of the CM range correspond to the breakdown voltages of the used chip process. We noticed that the input bias current and the transconductance slowly increase as a function of the CM-input voltage due to the Early effect (see Figs. 10 and 11). That is why the values of the maximum input bias current indicated in Table II are a little larger than the theoretical value of $5\,\mu$A ($= I_{EE}$).

Another experiment showed that the comparator input stage of Fig. 7(a) is able to deal with digital 0–5-V differential input signals even at a supply voltage as low as 1.3 V. This feature could be a valuable property for future low-voltage comparators.

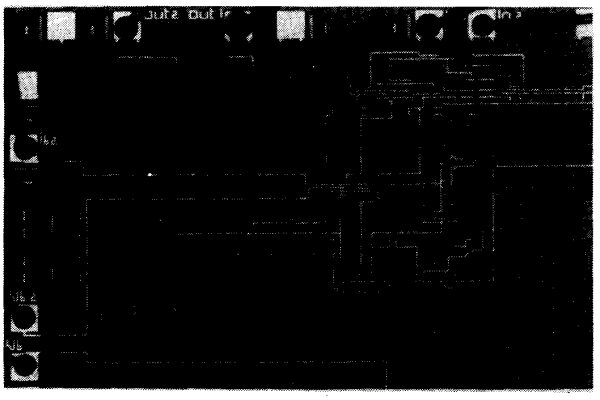

Fig. 9. Chip photograph of one realized input stage.

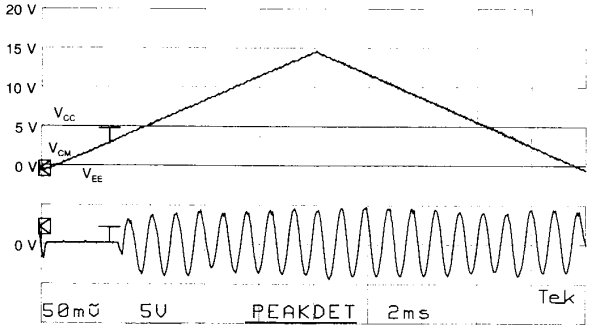

Fig. 10. Oscilloscope plot of an experiment to test the CM range of the circuit of Fig. 6(a).

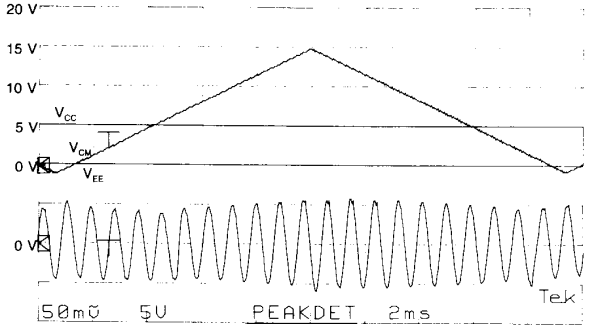

Fig. 11. Oscilloscope plot of an experiment to test the CM range of the circuit of Fig. 7(a).

V. Conclusion

Input stages are presented that realize an extension of the CM-input range of op amps and comparators to far beyond the positive and the negative supply rails. The extended CM range is limited by process-determined breakdown voltages rather than by the supply voltage. Also, the saturation problems of conventional op amp and comparator input stages at the limits of the CM range are solved satisfyingly in the new input stage configurations: reversal of the signal polarity is prevented and the input bias current is limited to a value related to the quiescent current of the input stage. Several combinations of input stages were proposed to cover different parts of the CM range, in between the supply rails, above the positive supply, and below the negative supply. The presented configurations have the important advantage that within the (unreduced) normal CM range the same specifications as those of conventional input stages can be met, while beyond the limits of the normal CM range correct operation of the input stage and a constant transconductance are still guaranteed, but with some degraded specifications. Applying these new input stages will expand the universality of future op amps and comparators. For example, a low-voltage comparator with input CM extension, supplied with only 1.5 V, can operate correctly in a 0–5-V TTL environment. Op amps will no longer have saturation problems in voltage-follower configurations when the input signal exceeds the supply rails, and comparators will be able to sense differential voltages correctly even for CM voltages far beyond the supply rails.

TABLE II
Measurements of the Realized Input Stages

Realized input stage of:	Fig.6(a)	Fig.7(a)	Unit
Normal CM range	0.7 – V_{CC}+0.1	-0.2 – V_{CC}-0.7	V
Extended CM range(s)	0.7 – +15	-0.5 – +15	V
Minimum supply voltage	1.0	1.3	V
Normal input bias current	0.025	0.05	μA
Maximum input bias current	6	6	μA

for V_{CC}= 5V, V_{EE}= 0V, I_{BE}= 5μA, T= 293K

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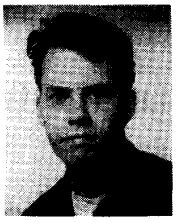

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