Opto-electrical approaches for high efficiency and ultra-thin c-Si solar cells

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The need for cost reduction requires using less raw material and cost-effective processes without sacrificing the conversion efficiency. For keeping high the generated photo-current, an advanced light trapping scheme for ultra-thin silicon wafers is here proposed, exhibiting absorptances up to 99% of $4n^2$ classical absorption limit for wafer thinner than 35 µm. Such excellent optical performance does not reflect optimal electronic properties due to high recombination rate of the nano-textured surface. Therefore, we propose a passivation method involving both wet etching and high quality passivation coating of the nano-textured surface. For wet etching time longer than 30 s recombination rate of the nano-textured one while keeping the averaged reflectance below 2% (between 300 and 1050 nm). Electrical simulations based on such findings indicate that for wafer thinner than 35 µm conversion efficiency higher than 25% can be achieved.

1. Introduction

Crystalline silicon (c-Si) solar cell technology represents more than 80% of the total PV market [1]. To maintain the dominant market position in future, this technology requires the use of cost-effective processes and fewer materials, such as thinner wafers. Moreover, when thinner wafers are used, bulk recombination is reduced and as consequence implied open circuit voltage (iV_{OC}) increases [2].

However, Si is a semiconductor with indirect band-gap, therefore, absorption in the near infrared region (NIR) of the solar spectrum is dramatically reduced when using thinner wafers.

To enhance light absorption in ultra-thin (<40 µm) c-Si absorber layer we have recently experimentally demonstrated an advanced light trapping scheme which delivers photo-current density (J_{PH}) higher than the one predicted by the $4n^2$ absorption enhancement [3]. Our approach is based on decoupling front and back morphologies in order to maximize the light absorption. In spite of the light trapping performance very close to the theoretical absorption enhancement limit, the electronic properties of our structure are not optimal. Such high recombination rate is due to (i) enlargement of the surface area of the conical front nanotexture and (ii) front surface defects created during the reactive ion etching (RIE) deployed for the front nano-texture. In this work, a method for efficient passivation of nano-textured surfaces [4] aiming to obtain high implied open-circuit voltage (iV_{oc}) is deployed. The advanced passivation scheme we propose is based on a wet chemical etching followed by dry thermal oxidation. Reducing electrical recombination on nano-textured surfaces is extremely important to fabricate high efficiency devices. By using our findings in terms of light trapping and electrical passivation we have simulated with 2-D opto-electrical software [5] interdigitated back contacted (IBC) c-Si solar cells [6] with efficiency higher than 25% with a wafer thickness of 40 µm.

3. Advanced light trapping scheme for ultra-thin c-Si aborbers

In our recent work, we experimentally demonstrated that nano-texture at the front side (FS) and micro-texture at the back side (BS) of a thin c-Si slab, combined with the state-of-the-art back reflector **Fig. 1**, resulted in a measured absorptance that is 99% of the one predicted by $4n^2$ enhancement factor see **Fig. 2**. In more details our optical system involved: conical front nano-texture for broadband light in-coupling, pyramidal rear alkaline texture for efficient light scattering in the silicon bulk and metallic SiO₂ / Silver or dielectric SiO₂ / Distributed Bragg Reflector (DBR) where used to maximized internal rear reflectance. The nano-texture was fabricated via mask-less reactive ion etching process using a gaseous mixture of SF₆ and O₂. The rear side of the wafer was processed to feature a random pyramidal micro-texture that was coated with dry thermal SiO₂ and photonic distributed Bragg Reflector (DBR) or a silver metal reflector. The random pyramidal micro-texture was obtained by etching of c-Si wafer in a TMAH-IPA alkaline bath (see **Fig. 1**).



Fig. 1. Cross-sectional SEM image of 20-µm thick textured c-Si wafer. In the right-side insets, close-ups of the front textured b-Si coated with thermal SiO₂ and of the textured BS coated with thermal SiO₂ and 6 pairs of a-Si:H (69 nm) / a-SiN_x:H (145 nm) are shown. All images were taken at 45° tilt angle. The surfaces of our wafers were textured using low-cost and industrially-scalable processes.



Fig. 2. J_{PH} calculated from measured c-Si bulk absorptance spectra under AM1.5 illumination between 350 nm and 1200 nm as function of wafer thickness for SiO₂ / DBR or SiO₂ / Ag BRs. Theoretical implied photocurrent density from $4n^2$ absorptance limit is also reported.

3. Advanced passivation technique for nano-textured surfaces

In a new experiment, following the realization of the conical front nano-texture on 285 μ m thick FZ wafers, we applied a wet-etching treatment based on TMAH [4] for 15, 30, 45 and 60 seconds (see **Fig. 3**) called defect removal etching (DRE). The nano-textured samples together with a reference 285 μ m thick double-side polished FZ wafer were coated on both sides with dry thermal SiO₂ deposited at 1050° C. For different etching times we investigated the morphological aspect and the overall opto-electrical performance of the silicon absorber. To this end, we used (i) Sinton lifetime tester to measure effective minority carrier lifetime (τ_{eff}), (ii) PerkinElmer spectrophotometer to test the front side reflectance (R) of the samples and (iii) SEM imaging for carrying out the ratio between the front effective area and the projected area on a flat surface (A^F/A_{proj}). As presented in **Fig. 4**, in case of no DRE and SiO₂ coating,

nano-texturing of wafers resulted in a poor τ_{eff} . However, we found that already after 15 s of etching time τ_{eff} increases with respect to the 0 s of DRE. This is related to the decrease of the defect density at front surface after the wet etching. **Fig. 5** reports the averaged R between 300 nm and 1050 nm for the five nano-textured wafers coated with SiO₂ as well as the A^F/A_{proj} (bottom x-axis) and the DRE time (top x-axis). The sample that received 30 seconds of DRE exhibited R < 5% and $\tau_{eff} > 150 \ \mu$ s, representing an optimal compromise between electrical and optical properties.



Fig. 3. (a)-(e) Cross sectional SEM images of FS n-T fabbricated via RIE after 0, 15, 30, 45 and 60 seconds of DRE coated with 40 nm of dry thermal SiO₂, respectively. On each SEM image, the ratio between the effective front surface area (A^{F}) and the correspondent projected area (A_{Proj}) is reported. By increasing the time of DRE, surface smoothening is clearly observed.





Fig. 4. Effective minority carrier diffusion lifetime (τ_{eff}) as function of the injection level (Δn) measured with Sinton as function of the DRE time. After 30 s of DRE, τ_{eff} , three times higher with respect to the 0 s DRE sample were achieved.

Fig. 5. Reflectance (R) averaged between 300 nm and 1050 nm. Numbers next to the data points are the values of AF/Aproj ratio calculated form SEM reported in **Fig. 3**.

3. Opto-electrical simulations of nano-textured IBC c-Si solar cells

We performed opto-electrical simulations for predicting the conversion efficiency as function of the wafer thickness and bulk lifetime (τ_{bulk}) of nano-textured IBC c-Si solar cells. For this purpose we used Quokka free-were 2-D simulator [5]. By using the optical assumption of Lambertian light trapping together with minimization of the electrical recombination [7] (see 3-D sketch in **Fig. 6**) conversion efficiency of 25.7% can be reached for wafers around 40 µm (see area plot in **Fig. 6**), even in case of low quality wafers (i.e. low τ_{bulk}).

Conclusions

In this work we have presented an advanced light trapping scheme based on the combination of nano- and micro-texturing exhibiting absorptances up to 99% of $4n^2$ classical absorption limit for wafer thinner than 35 μ m. In order to tackle the enhancement of the recombination rate of

the nano-textured surface we propose an advanced passivation scheme based on a wet etching called DRE of the nano-textured surface followed by dry thermal SiO₂. An improvement of the minority carrier lifetime was observed after 30 s oF DRE. Moreover, 30 s of DRE were considered as good compromise to achieve bot low recombination rate and low reflectance of the nano-texturing. By using these findings we have used a opto-electrical simulator to predict the efficiency of ultra-thin c-Si nanotextured IBC solar cells. Efficiency of 25.7% were achieved by using wafer thickness of 40 μ m and bulk lifetime around 1 ms.



Fig. 6. On the right, 3-D sketch of simulated IBC c-Si solar cell; On the left, conversion efficiency (η) as function of wafer thickness and τ_b simulated with opto-electrical simulator, setting effective front surface recombination velocity $S^F_{eff} = 5$ cm/s and back saturation current density $J_0 = 10$ fA/cm² [7]. Conversion efficiency of 25.7% was simulated for wafer thickness around 40 μ m of τ_{bulk} below 1 ms.

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