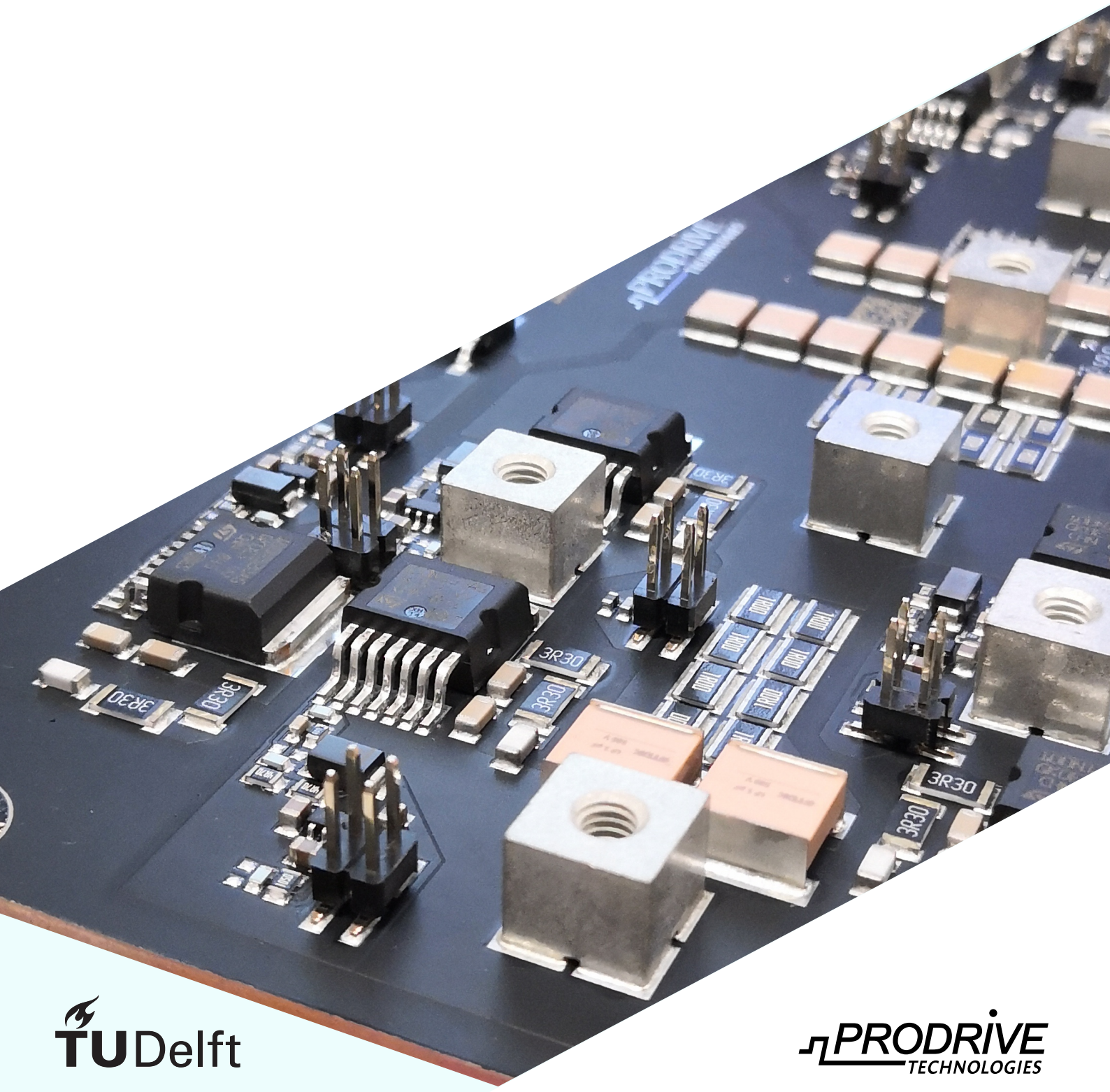
Prodrive-Select Rectifier: Modelling and Optimization of a Three-Phase Buck-Type PFC Rectifier

Thomas Gerrits



TU Delft

PRODRIVE TECHNOLOGIES

Prodrive-Select Rectifier: Modelling and Optimization of a Three-Phase Buck-Type PFC Rectifier

by

Thomas Gerrits

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Abstract

This research introduces the Prodrive-Select Rectifier, a novel three-phase buck-type power factor correction rectifier suitable for mains interfaced AC-to-DC conversion as, for example, can be found in on-board battery chargers for electric vehicles. The Prodrive-Select Rectifier shows excellent mains current total harmonic distortion, especially when interleaving of the converter branches is considered, and achieves competitive efficiencies by utilization of three-level buck circuits and a capacitive midpoint which allows for complete zero-voltage switching of the high-frequency power MOSFETs. In this work, two modulation schemes are proposed and analysed with regard to their zero-voltage switching capabilities. In addition, the complete converter analysis including steady-state analysis, transient closed-loop control and component-level volume and loss modelling is thoroughly described. In order to obtain an objective performance indication, the topology is compared to a state-of-the-art buck-type rectifier, namely the Swiss Rectifier. The proposed modelling techniques are implemented by means of a virtual prototyping routine yielding a Pareto-front in the power density versus efficiency performance space from which an optimal design is selected using multi-objective optimization. This Pareto-optimal design operates under partial soft-switching conditions and achieves a conversion efficiency of 98.3% at 2.9kW/dm^3 power density. The modelling and optimization techniques are verified by an 11-kW, 1.3-kW/dm^3 hardware demonstrator for conversion of a 400-V rms line-to-line AC input into a 400-V nominal DC output. Measurements show efficiencies higher than 97.5% in the range of 4kW-11kW, with 97.7% peak efficiency and <4% total harmonic distortion at full power.

Thomas Gerrits
Eindhoven, October 2019

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Contents

1 Introduction

As of September 2019 the Tesla Model 3 boasts a market share of 4.1% in The Netherlands. In the middle class segment the car makes up a substantial 15.5% of all sold cars. With more than 13.000 sold Model 3's, the year 2019 is rapidly on its way to becoming the first year in which an electric vehicle (EV) is the nations most sold car. The total electric vehicle sales are approaching 30.000 units, already beyond the total projected sales for the entirety of 2019. Consequently, 9% of all new cars are fully electric. The main driving force behind this transition is the government backing making electric lease cars financially more attractive than traditional combustion engine vehicles.

The popularization of Electric Vehicles (EVs) and Plug-in Hybrid Electric Vehicles (PHEVs) paired with increased governmental support elicits the need for research into practical and standardized charging procedures. Currently, 24.000 charging stations are 24/7 accessible in The Netherlands, marking an increase of +344% with respect to 2014. The charging of DC batteries in EVs from an industrial AC grid means the converters required for the power conversion are inherently AC-to-DC converters. Recent research [1],[2] reviews a multitude of topologies for EV charging with power levels ranging from 4.4kW to 240kW [3], where three-phase AC-to-DC converters are the norm. The types of EV chargers are categorized into on-board and off-board chargers, as depicted in Figure 1.1*a*. Off-board chargers are located inside the charge installation and are less constricted by weight and size requirements, while on-board chargers are located inside the vehicle and these requirements are thus of greater importance to car manufacturers.

A typical block diagram of an on-board charger is seen in Figure 1.1*b* [4]. An EMI filter is placed at the input in order to filter high frequency noise and decouple the charger from the AC grid. An AC-to-DC rectifier with subsequent power factor correcting (PFC) converter are placed in order to comply with standards regarding the grid power quality, i.e. power factor and total harmonic distortion (THD). An isolated DC-to-DC converter is placed with the aim of electrically shielding the EV from the grid and charging the DC battery.

As seen in Figure 1.1*b*, the AC-to-DC and PFC stage can be combined into a single active converter, e.g. the Swiss Rectifier [5], called a PFC rectifier. This type of PFC rectifier reduces the total system size by integrating two converters and provides a controllable DC link voltage. The isolated DC-DC converter, often implemented with a Dual Active Bridge (DAB), operates at optimal conditions with a voltage transfer ratio of 1 [6]. This means that with varying battery voltage the controllable DC link voltage further increases system efficiency.

This research introduces a novel, three-phase, buck-type PFC rectifier, named the Prodrive-Select Rectifier, which could be used, among other applications, as the PFC rectifier stage of an on-board EV charging system. The operating principle of the Prodrive-Select Rectifier, as well as, the converter modelling and design optimization are discussed in detail. The theoretical analysis and simulations are verified with measurements on an 11-kW, 1.3kW-L hardware demonstrator.

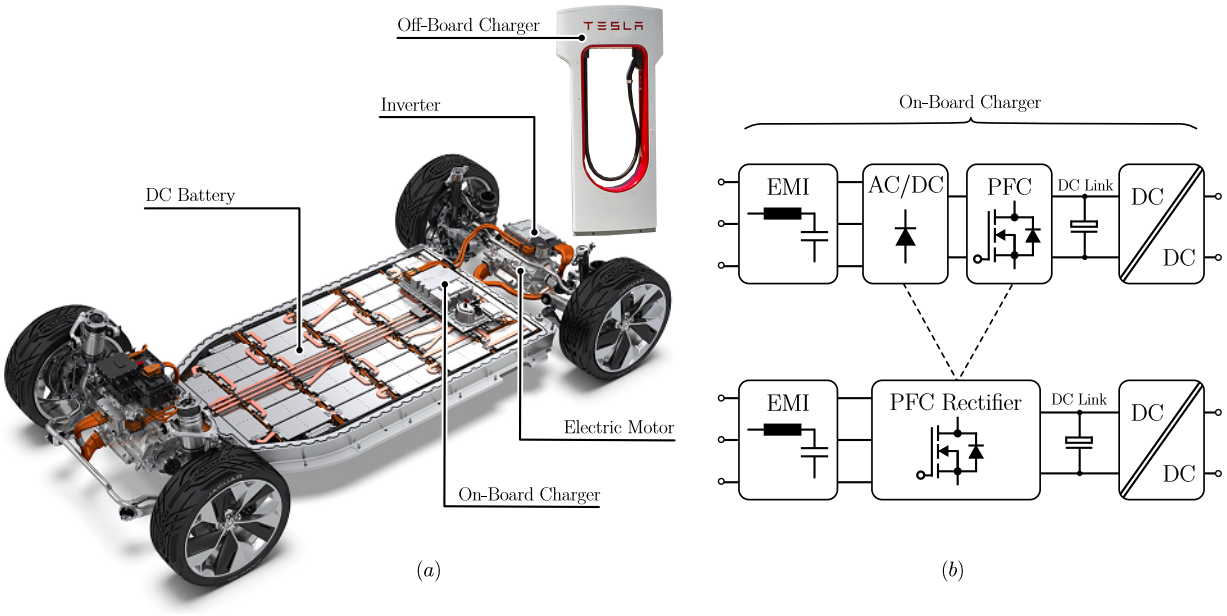

Figure 1.1: (*a*) Jaguar I-Pace powertrain concept with Tesla Supercharger. (*b*) Typical block diagram of on-board chargers with an EMI filter, an AC/DC converter, a PFC converter and an isolated DC/DC converter. Source: [7]

1.1. Background

According to the standard IEC61851 on-board EV chargers up to 14.4kW fall into charging mode 1 and 2. Furthermore, three-phase operation as well as single-phase or split-phase operation can be classified into type 1,2 and level 1,2. Topologies for AC-DC PFC rectifiers in this power range include a passive three-phase rectifier with cascaded PFC stage, or single-stage AC-DC PFC rectifiers such as the six-switch buck-type rectifier or the Swiss Rectifier [8].

Typical charging levels of current generation EV batteries are 300-450V [9],[10]. If a standard three-phase EU grid of 400-V rms line-to-line is utilized for charging these EV batteries, a buck-type rectifier would be necessary in order to avoid additional cascaded bucking stages. A promising topology satisfying these parameters is the Swiss Rectifier, as presented in [5]. This topology utilizes the third-harmonic current injection principle for providing efficient, three-phase rectification to a controllable DC output voltage and PFC of the input power. Compared to conventional PFC rectifiers as the six-switch buck-type rectifier, the Swiss Rectifier benefits from lower EMI filter requirements and less high-frequency semiconductor devices, resulting in increased power density and efficiency. Prototypes have been realized achieving 4 kW/dm^3 with peak efficiencies up to 99.3% [11]. A novel three-phase buck-type PFC rectifier, utilizing the same third-harmonic current injection principle, is presented in this work named the Prodrive-Select Rectifier.

1.2. Research Objectives

The aim of this research is to model and design the Prodrive-Select Rectifier, a three-phase buck-type PFC rectifier using the principle of third-harmonic current injection. The main use-case of the rectifier is to function in an on-board EV charger, but it could, for instance, also be used in other industrial systems requiring three-phase PFC rectifiers such as gradient amplifiers for MRI systems or motor drive systems. The on-board charger use-case requires increased focus on power density and efficiency as these are crucial parameters for the competitive automotive market.

In line with the intended use-case, a set of requirements are formulated and are stated in Table 1.1.

Table 1.1: Design requirements for the three-phase buck-type PFC rectifier.

Description	**Parameter**	**Value**	**Unit**
Three-phase input voltage	$V_{in,3\phi,rms}$	400+10%	V
Output power	P_{out}	11	kW
Output voltage range	V_{out}	300-450	V
Nominal output voltage	$V_{out,nom}$	400	V
Nominal, full load efficiency	$\eta_{100\%}$	>98%	-
Power density	ρ_P	>2	kW/L

Additional standards the rectifier has to comply with:

- Class A EMC standard (CISPR 22)
- OBC Mode 2 (IEC61851)

The introduction of a novel topology raises questions regarding the validity and performance of the topology in its respective use-case and in comparison to similar topologies. For validating the converter's operating principle, the first research objective is formulated:

- *Mathematically describe the operating principle of the Prodrive-Select Rectifier, derive a suitable modulation scheme and develop an applicable controller paired with converter simulation to verify the performance.*

For verifying the topology with respect to the use-case, the second research objective is formulated:

- *Model and design of a Prodrive-Select Rectifier for an 11kW on-board charger with particular focus on power density and efficiency.*

The comparative evaluation of a new topology to similar topologies gives objective performance indications which are crucial to the credibility of the topology. This leads to the formulation of the third research objective:

- *Comparative evaluation of the Prodrive-Select Rectifier to similar three-phase, buck-type PFC rectifiers.*

1.3. Research Methodology

The research methodology is an important factor in the modelling and design of power converters as the accuracy of the employed models relates one-to-one to the validity of the design and the resulting conclusions. Modelling of the power converters is done in MATLAB with custom, mathematical converter steady-state models. These models include converter basic waveform analysis, converter Fourier analysis, component models and system performance models. These models are verified by a combination of simulations in Simulink/PLECS and a hardware demonstrator.

Virtual prototyping of the converter system is applied in order to reach an optimal design without hardware iterations. The multi-objective optimization is possible due to the fully mathematical converter modelling technique. The comparative evaluation is done by using the proposed modelling techniques on various topologies. When the converters are all evaluated using the same models the absolute accuracy of the models can be neglected as the comparison is valid nonetheless.

1.4. Thesis Outline

The thesis is divided into several chapters:

The *second* chapter is a literature review of relevant topics with respect to three-phase PFC rectifiers and zero-voltage switching principles. Here the principle of third-harmonic current injection is explained and an example is given of a zero-voltage switched buck circuit.

The *third* chapter introduces the Prodrive-Select Rectifier and elaborates on the converter analysis. The converter analysis is used as a building block when designing a Prodrive-Select Rectifier. Two modulation schemes are explored and compared against each other.

The *fourth* chapter investigates the proposed closed-loop control of the Prodrive-Select Rectifier. Relevant dynamic waveforms, such as converter start-up, are shown, as well as, steady-state waveforms in order to verify the converter analysis.

The *fifth* chapter is dedicated to the converter and component modelling techniques in order to shed light on the employed models. All relevant topics, such as inductor modelling, semiconductor modelling and EMC modelling are addressed. A converter modelling scheme is given which outlines the modelling steps in sequential fashion.

The *sixth* chapter elaborates on utilizing the models and setting up a virtual prototyping routine in order to optimize the converter design. The chapter formulates a design space and elaborates on the optimal operating conditions which result in the best performance of power density versus efficiency.

The *seventh* chapter is a comparative evaluation of the Prodrive-Select Rectifier and the Swiss Rectifier. The Prodrive-Select Rectifier is derived from the Swiss Rectifier and thus a comparison between the two can give an objective performance indication.

The *eighth* chapter verifies the previous modelling chapters by the design and measurement of a hardware demonstrator. The hardware demonstrator is highlighted in the design space and is used to verify converter performance aspects such as efficiency, power density and thermal behaviour.

2

Literature Review

2.1. Introduction

This chapter is a literature review on relevant topics with regards to three-phase PFC rectifiers, the principle of third-harmonic current injection and a soft-switching method for MOSFET half-bridges. This research is focused on on-board chargers for EVs as depicted in Figure 2.1. The aim lies on the PFC rectifier stage in the charger system. In this research the denotation PFC rectifier means an active rectifier that does the tasks of rectifying the AC grid voltage, power factor correction of the input currents and controlling of the DC link voltage.

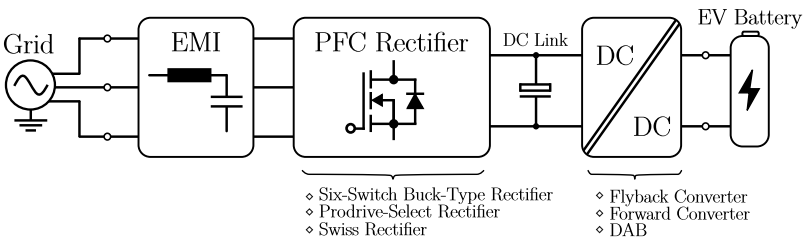

Figure 2.1: Block diagram of on-board charger topology with possible converter implementations for the PFC rectifier and isolated DC-DC converter.

It is assumed that the isolated DC-DC stage is implemented with a DAB and has a voltage transfer ratio of 1 in order to operate at its most efficient point. This leads to the reviewed PFC rectifier systems being a buck-type in order to charge current generation EV batteries from a standard EU three-phase grid. As on-board chargers are attached to the vehicle, the efficiency and power density are of increased importance. An approach to increasing power density is to increase the switching frequency of the active semiconductors. This usually leads to a decrease in the passive component volumes, facilitating an increased power density but at the cost of efficiency as the switching losses of the semiconductors scale proportional to the switching frequency. In order to accommodate the increased switching frequency, soft-switching methods can be used to decrease the switching losses of the PFC rectifier.

2.2. Three-Phase Buck-Type PFC Rectifiers

As the name suggests, three-phase buck-type PFC rectifiers have three tasks. Namely, performing rectification of the three-phase AC grid, applying power factor correction of the input current and outputting a controllable voltage that is lower than the wave-rectified three-phase line-to-line voltage. Widely used topologies satisfying these requirements are the six-switch buck-type PFC rectifier [12] or the more industry standard six-switch boost-type PFC rectifier with cascaded buck converter, as depicted in Figure 2.2.

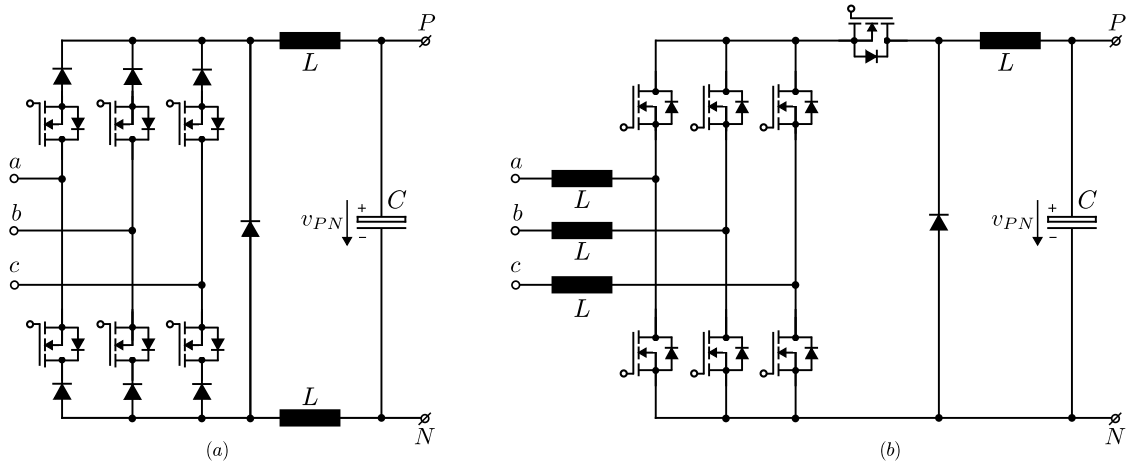

Figure 2.2: Circuit topology for (*a*) six-switch buck-type PFC rectifier and (*b*) six-switch boost-type PFC rectifier with cascaded buck converter.

In order to draw purely active power from the grid ($P = S$), to avoid component over-dimensioning and grid pollution, the converter has to shape the inputs currents sinusoidal and in phase with the grid voltage, as depicted in Figure 2.3*a*, called power factor correcting. This relationship between voltage and current is characterized by a power factor λ equal to 1 and ensures ohmic mains behaviour of the converter. Figures 2.3*b* and 2.3*c* show non-ohmic behaviour where the phase current has non-unity power factor λ and/or displacement power factor Φ.

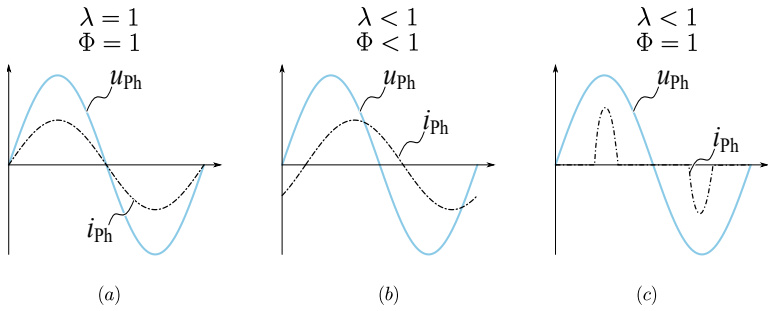

Figure 2.3: Single phase AC voltage u_{ph} and current i_{ph} for different current displacement factor Φ and THD with corresponding power factor λ.

The mains behaviour of the converter can be qualitatively described by the power factor λ, the displacement power factor Φ and the total harmonic distortion (THD) [12]:

$$\lambda = \frac{1}{\sqrt{1 + \mathrm{THD}_i^2}} \cdot \cos(\phi_1) \tag{2.1}$$

where the displacement power factor $\Phi = \cos(\phi_1)$ and ϕ_1 the angle between the voltage and the current of the fundamental frequency. The THD of a waveform is a measure of the harmonic content of higher order harmonics compared to the fundamental and can be described as:

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_1} \tag{2.2}$$

Figures 2.3*b*,*c* show single-phase AC waveforms with respectively low displacement power factor Φ and high THD. In both cases the power factor λ is below 1. Standards have been introduced to limit the THD or harmonic current injection of grid connected rectifiers in order to maintain a clean grid, a grid devoid of electrical pollution, such as the IEC norm 555-3, prepared by the International Electrical Commission (IEC).

Table 2.1: Realized prototypes of three-phase buck-type PFC Rectifiers.

Topology	Technology	Rated Power	Efficiency	Power Density
Six-Switch Buck-Type Rectifier [13]	Si MOSFET	5 kW	98.8%	2.2 kW/dm^3
Swiss Rectifier [5]	Si IGBT, SiC Schottky	7.5 kW	96%	2.94 kW/dm^3
Interleaved Swiss Rectifier [11]	SiC MOSFET	8 kW	99.1%	4 kW/dm^3
Interleaved Prodrive-Select Rectifier	SiC MOSFET	11 kW	97.7%	1.3 kW/dm^3

Table 2.1 summarizes the implementation of four three-phase buck-type PFC rectifiers, each indicated with their figure-of-merits. Note that the converter prototype of this work, the Interleaved Prodrive-Select Rectifier, is competitive in the efficiency and power specification, but concedes in the power density. Chapter 8 is dedicated to the implementation and measurement of the converter prototype and further elaborates on this topic.

2.2.1. Three-Phase Buck-Type Third-Harmonic Current Injection PFC Rectifiers

A subset of three-phase PFC rectifiers are the third-harmonic current injection rectifiers, an example of which is shown in Figure 2.4*b*. An implementation of a rectifier using this principle can be seen in Figure 2.6.

Third-Harmonic Current Injection Figure 2.4 depicts a passive three-phase rectifier with and without third-harmonic current injection, where v_{PN} and i_{PN} are identical. As seen in Figure 2.4*a*, the phase currents are formed by segments of i_{PN}. At any given time, two of the three phases are conducting, namely the phases with the highest and lowest voltage. Figure 2.4*b* illustrates the principle of third-harmonic current injection (THCI) where a triangular current is injected into the phase with the middle voltage. This ensures all three phases are continuously conducting. Furthermore, the injected phase current allows active shaping of the remaining phase currents by means of i_{yt} and i_{yb}. As seen in Figure 2.4*b*, the phase current and part of the injection current combine to equal the output current i_{PN} during $30° > \omega t > 150°$:

$$i_a - i_{yt} = i_{PN}$$

This ensures that the phase currents exhibit sinusoidal shapes proportional to the phase voltage during the entire grid cycle, thus achieving unity power factor. An example of a converter working with this principle can be found in [14].

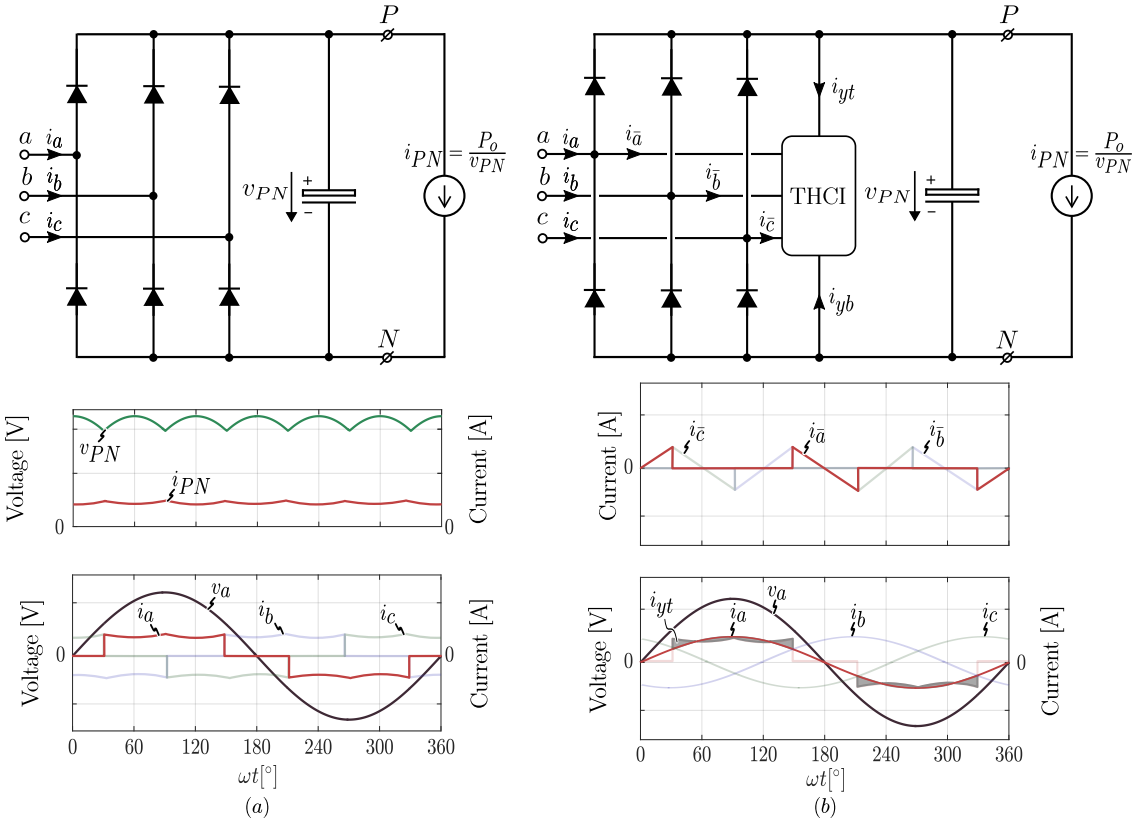

Figure 2.4: (*a*) Basic topology of a passive three-phase rectifier with constant power load. Typical waveforms show low power factor due to the fact that only two phases are conducting i_{PN} at any given moment. (*b*) Basic topology of passive three-phase rectifier with active third-harmonic current injection and constant power load, e.g. hybrid active third-harmonic injection buck-type rectifier (H3R). Typical waveforms show unity power factor due to the triangular third-harmonic current which is injected into the originally not conducting phase [12].

Input Voltage Selector One way to implement THCI is by electrically connecting the phase with the middle voltage to the converter by means of an Input Voltage Selector (IVS). These rectifiers extend the traditional passive three-phase rectifier ($D_{ax,bx,cx}, D_{za,zb,zc}$) with three four-quadrant switches ($S_{aya}, S_{byb}, S_{cyc}$) shown in Figure 2.5*a*. The IVS has three input terminals (a, b, c) and three output terminals (X, Y, Z) and alternately connects one of the input terminals to one of the output terminals in a specific way. Of the three-phase grid voltages present at the input terminals the highest is connected to the output terminal X, the middle voltage is connected to the output terminal Y and the lowest voltage is connected to the output terminal Z. This realizes a three-phase network on nodes X, Y, Z where the voltages are piece-wise sinusoidal. The voltages on the input and output terminals can be seen in Figures 2.5*c* and *d*. Figure 2.5*b* depicts the conduction state of the IVS for phase ϕ.

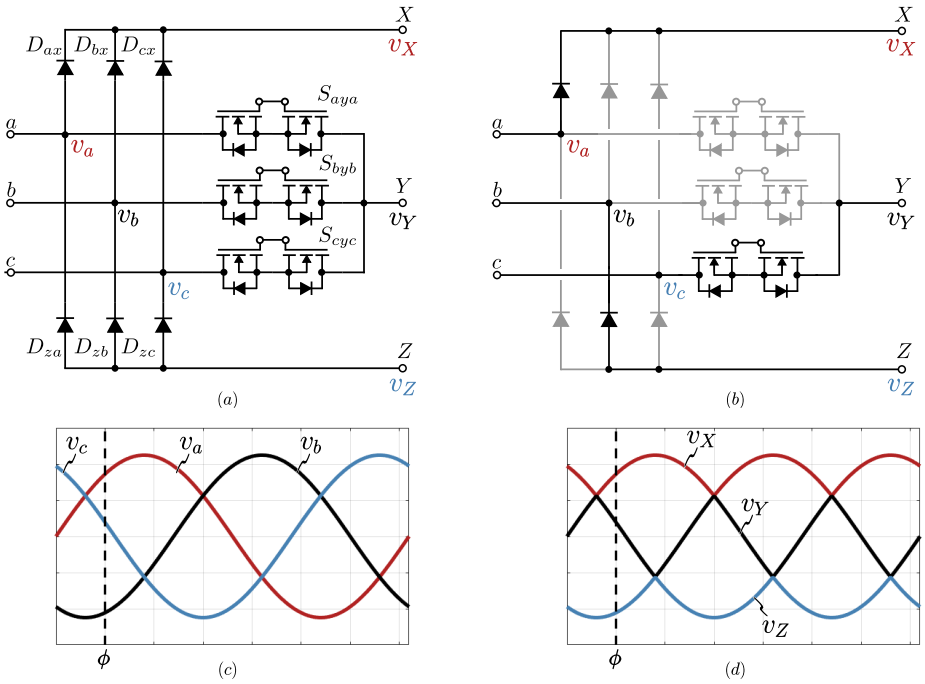

Figure 2.5: The Input Voltage Selector (*a*) circuit topology (*b*) conduction states for phase ϕ (*c*) input voltage waveforms (*d*) output voltage waveforms.

Swiss Rectifier A promising three-phase buck-type PFC rectifier using the principle of third-harmonic current injection is the Swiss Rectifier [5], depicted in Figure 2.6. The rectifier uses the IVS as an input stage and has two series connected buck circuits, denoted as top and bottom buck circuit. The bottom buck circuit is an inverted buck circuit which transfers power in the opposite direction as the top buck circuit. The common node of the buck circuits is connected to the node Y. The task of the buck circuits it to create a stable voltage between P and N and to achieve unity power factor at the input of the converter. The top buck circuit actively shapes the current i_x to be proportional to the voltage v_{XM} while the bottom buck circuit shapes the current i_z to be proportional to voltage v_{ZM}, as seen in Figures 2.6*b* and 2.6*c*. Currents i_x, i_y and i_z can be assumed a balanced three-phase system, which implies $i_x + i_y + i_z = 0$. As a result, the injected current i_y resembles a triangular current with three times the grid frequency.

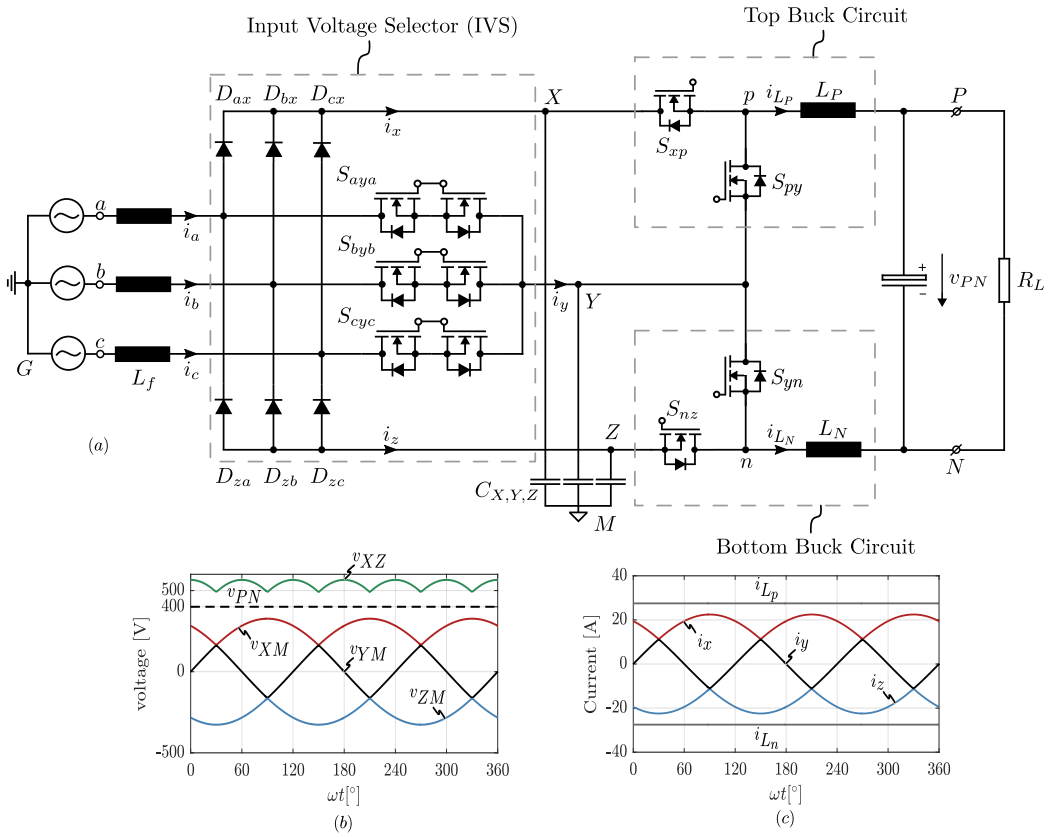

Figure 2.6: (*a*) Basic circuit topology of the Swiss Rectifier connected to a three-phase grid and a resistive load depicted with typical (*a*) voltage and (*b*) current waveforms.

If the three intermediate currents i_x, i_y and i_z are proportional to the intermediate voltages v_{XM}, v_{YM} and v_{ZM}, the functioning of the IVS ensures that the currents i_a, i_b and i_c are proportional to the voltages v_a, v_b and v_c, thus achieving unity power factor.

The output voltage v_{PN}, shown in Figure 2.6*b*, can be controlled to any voltage between zero and the minimum value of v_{XZ}, whilst retaining unity power factor. This converter is thus a single stage AC-to-DC rectifier with a controllable DC output voltage lower than the minimum value of the wave-rectified six-pulse voltage waveform. Realized prototypes of the Swiss Rectifier can be found alongside other three-phase buck-type PFC rectifiers in Table 2.1.

Swiss Rectifier ZVS In order to facilitate an increase in switching frequency the possibility of zero-voltage switching (ZVS) with the Swiss Rectifier is investigated. The zero-voltage switching, as explained in Section 2.3, requires an inductor current envelope where the bottom envelope lies below zero. Figure 2.7 shows typical voltage and current waveforms of the Swiss Rectifier. As is evident from the figure, the inductor current envelope exhibits local minima ($\theta_{1,2,3}$) where there is no inductor current ripple, originating from the fact that voltage v_{XM} and v_{ZM} are equal during these periods. Subsequently, i_{L_n} shows local minima when v_{ZM} and v_{YM} are equal. Since the average inductor current $\langle i_{L_P} \rangle$ is positive with AC-to-DC energy flow, the local minima results in a loss of ZVS around $\theta_{1,2,3}$, indicated by a red inductor current envelope. The effect is more pronounced with increased output power or lower output voltage as the average inductor current increases. In order to combat this, the inductor current envelope could be increased by lowering the inductance or the switching frequency. However, this would largely increase the conduction losses in the converter negating the effect of ZVS. A different solution is to use interleaved buck circuits, sharing the output power, in order to decrease the average inductor current and thus minimize the loss of ZVS. However, because of the local minima in the inductor current envelopes the Swiss Rectifier is not an ideal converter to use in complete ZVS scenarios.

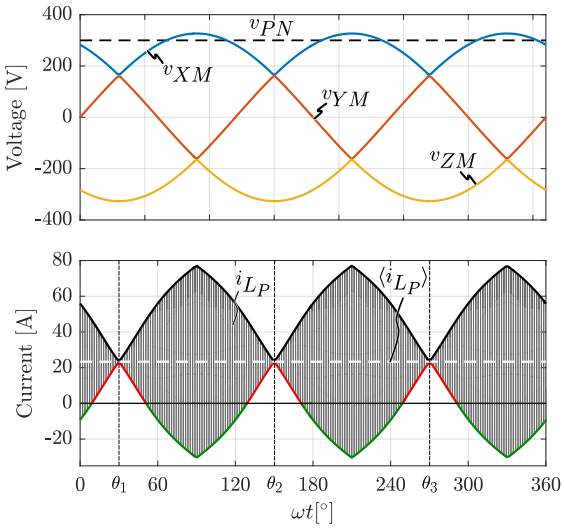

Figure 2.7: Swiss Rectifier intermediate voltage, output voltage and inductor current for v_{PN} = 300V and P_o = 7kW.

2.3. Zero-Voltage Switching

The zero-voltage switching of MOSFETs is commonly used to reduce or eliminate the switching losses that occur during turn-on or turn-off of a MOSFET. Full ZVS topologies have the benefit of allowing a higher switching frequency without the setback of increased switching losses significantly contributing to the decrease in system efficiency. Figure 2.8 shows a method for achieving ZVS in a MOSFET half-bridge with the aid of an imposed inductor current. The figure depicts turn-off of S_2 and zero-voltage turn-on of S_1.

Figure 2.8*a* depicts the freewheeling state before t_1 where S_2 is conducting positive drain-source current. At t_1 switch S_2 is opened while the inductor current $i_1 = i_L$. A resonant transition occurs between the inductor current and the MOSFET capacitances which discharges capacitance $C_{oss,1}$ and charges capacitance $C_{oss,2}$. Ideal resonant commutation, both ZVS and ZCS, is achieved at t_2 when $C_{oss,1}$ has been discharged completely and the inductor current i_L has decayed to zero. At t_2 switch S_1 achieves lossless turn-on at zero drain-source voltage and zero current.

ZVS is also possible if the inductor current has not decayed to zero at t_2 or if S_1 turn-on occurs later in time, after $C_{oss,1}$ has already been discharged completely. In this case diode D_1 is forced into conduction by the inductor current and still allows for zero-voltage turn-on as the diode forward voltage is assumed negligible compared to V_{DC}.

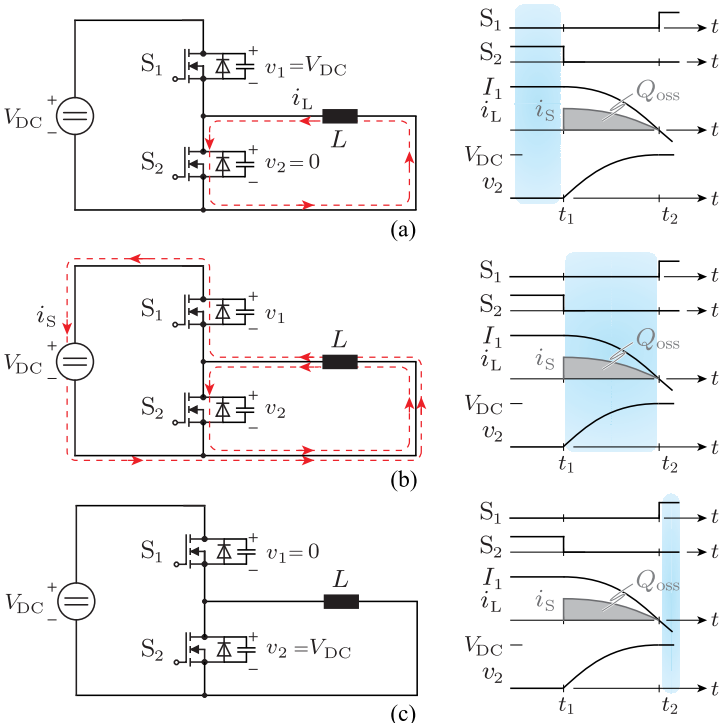

Figure 2.8: Soft-switching transition of a MOSFET bridge leg and an inductor L: (*a*) free-wheeling interval with inductor current $i_1 = I_L$; (*b*) switch S_2 turns off and resonant transition starts with additional current path through the dc source; (*c*) end of transition when the drain–source voltage of S_2 has reached the source voltage, i.e., $v_2 = V_{DC}$, and switch S_1 turns on at zero voltage. Source: [15].

Note that turn-off of S_2 is not completely lossless as there exists a voltage and current overlap in the MOSFET channel after t_1. A way to greatly reduce the turn-off losses of S_2 is by adding additional parallel capacitance across S_2 in order to delay the voltage rise and thus reduce the voltage and current overlap, often also called ZVS in literature [16]. Furthermore, the additional parallel capacitance reduces the $\frac{dv}{dt}$ of the voltage transition, easing the gate driver and EMC filtering requirements. The additional parallel capacitance does, however, increase the total charge Q_{oss} which needs to be removed or delivered by the inductor current, thus increasing the required reactive power and consequently the conduction losses.

2.4. Summary

This chapter serves as an introduction to the topic of three-phase buck-type PFC rectifier and aims to relate the converter design choices to overall converter and system impact. A selection of state-of-the-art prototypes are summarized and the Swiss Rectifier, along with the general third harmonic current injection principle are described in detail.

A zero-voltage switching method for MOSFET half-bridges is discussed and the Swiss Rectifier is analysed for its ZVS capabilities. It is concluded that with the standard implementation of the Swiss Rectifier it is impossible to achieve complete ZVS of the high frequency semiconductors.

3

Prodrive-Select Rectifier

3.1. Introduction

This chapter presents a novel three-phase buck-type PFC rectifier utilizing the principle of third-harmonic current injection named the Prodrive-Select Rectifier (PSR), see Figure 3.1. As is evident, this rectifier topology is derived as a variant on the Swiss Rectifier to be able to operate the converter in full ZVS conditions. With the Prodrive-Select Rectifier it is possible to achieve similar performance compared to the Swiss Rectifier, subsequently outperforming standard buck-type AC-DC rectifiers. The operating principle, the conduction states and the component stresses are discussed and the rectifier topology is analysed in detail.

3.2. Prodrive-Select Rectifier Topology

The circuit topology of the Prodrive-Select Rectifier is depicted in Figure 3.1. This topology utilizes an Input Voltage Selector (IVS) and series-connected three-level buck converters. This three-phase PFC rectifier combines the operation of these two subsystems to achieve unity power factor at its input and single-stage AC-to-DC conversion with a controlled DC output voltage. The functional explanation of the IVS can be found in Section 2.2.1. The task of the high-frequency 3L buck circuits is to create a stable voltage across v_{PN} and to shape the intermediate currents i_x, i_y and i_z. The intermediate currents can be shaped by controlling the average current in switches S_{xp}, S_{yp}, S_{ny} and S_{nz}. If these currents are shaped to be piece-wise sinusoidal and proportional to the three-phase voltages v_{XM}, v_{YM} and v_{ZM}, unity power factor is achieved at the input.

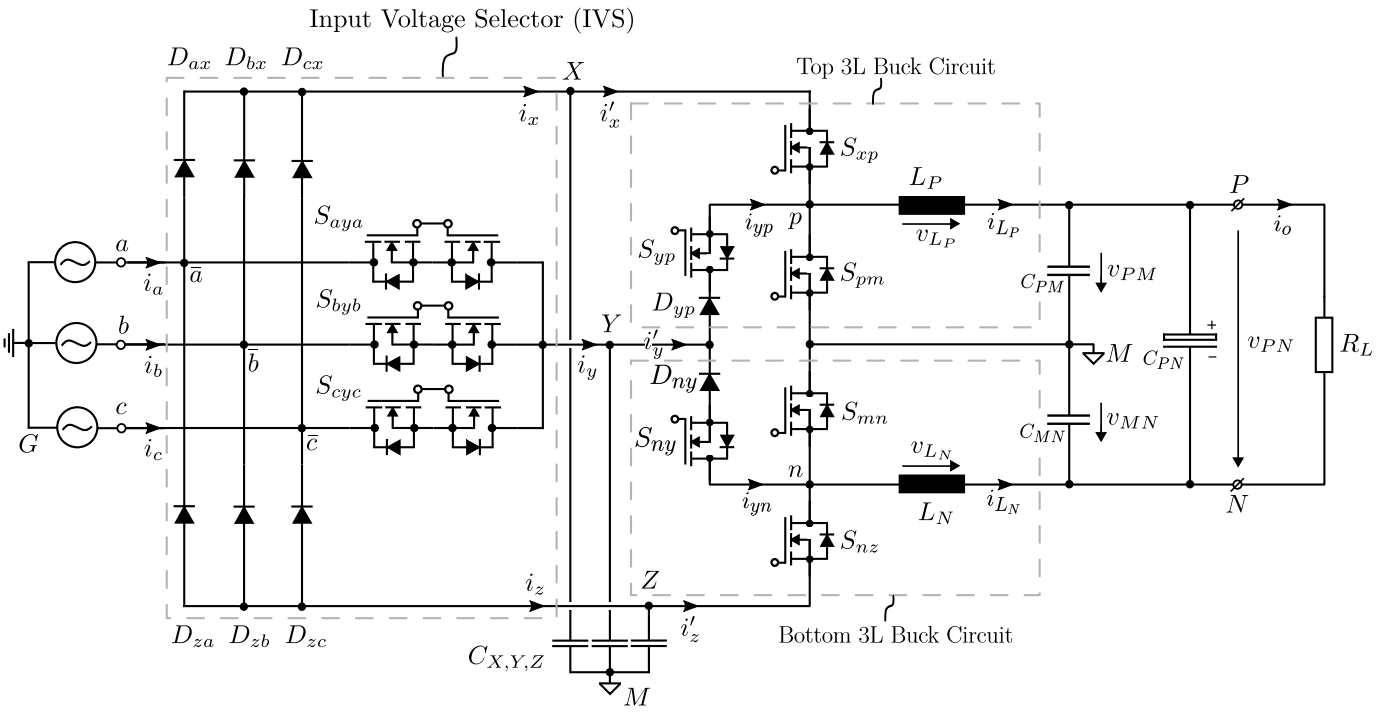

Figure 3.1: Circuit topology of Prodrive-Select Rectifier connected to a three-phase grid and a resistive load.

In the Prodrive-Select Rectifier the common node of the series-connected buck circuits is connected to midpoint M. Midpoint M is furthermore connected to the star connection of input capacitors C_X, C_Y and C_Z and to the midpoint of output capacitors C_{PM} and C_{MN}. This type of connection yields two decoupled buck circuits, meaning that both buck circuits can be analysed separately, as shown in Figure 3.4. Switch-nodes p and n are connected to node X and Z through a single active switch, allowing standard bucking action from nodes X, Z to nodes P, N. In order to allow bi-directional current flow between the buck circuits and the injection node Y, a third level is added to the switch-nodes p and n. Deviating from the standard buck circuit switch-nodes p and n are connected to node Y through an anti-series connection of a diode and a MOSFET, creating a current uni-directional, voltage bi-directional switch. The arrangement and function of these switches ensure that the top 3L buck circuit injects positive i_y current (i_{yp}) and the bottom 3L buck circuit injects negative i_y current (i_{yn}), while retaining complete voltage blocking capability during sectors when the switch is not conducting.

The reason for deviating from the standard, 2L buck circuit is to increase the controllability over the inductor current waveforms and to prevent local minima in the inductor current envelope, as detailed in Chapter 2.2.1, in order to allow for complete ZVS of the semiconductors in the Prodrive-Select Rectifier. The largest contributor to the switching losses are the turn-on losses of switches S_{xp} and S_{nz}. As explained in Section 2.3, zero-voltage turn-on of switches S_{xp} and S_{nz} can be achieved by ensuring an imposed negative inductor current before turn-on, as shown in Figure 3.3*a*. Depicted in Figure 3.2 is the inductor ripple and corresponding current envelope for inductor L_P. Evident is the lower current envelope (green) which lies completely below zero during the entire grid cycle. This means it is possible to achieve complete zero-voltage turn-on of switch S_{xp}. This analysis extends to switch S_{yp} due to the mirrored nature of the buck circuits.

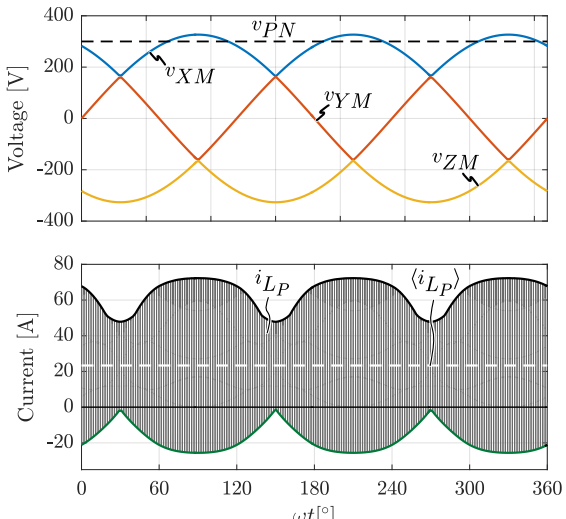

Figure 3.2: Prodrive-Select Rectifier intermediate voltages, output voltage and inductor current for v_{PN} = 300V and P_o = 7kW.

Further switching losses could occur during other switching instances, e.g. turn-off of switch S_{xp}. Figure 3.3 depicts the turn-on and turn-off transitions for two implementations of the Prodrive-Select Rectifier. As explained in Section 2.3, the turn-off losses of switch S_{xp} can be reduced by placing a parallel capacitance across the drain and source. This same method can be used for diminishing turn-off losses in switches S_{yp} and S_{pm} in the top 3L buck circuit. The turn-on instance of switch S_{yp} is inherently lossless as the turn-on can be timed to occur only when the voltage on node p is *higher* than the voltage on node Y, i.e. after turn-on of switch S_{xp} (see Figure 3.7*b*). This means the complete voltage is blocked by diode D_{yp}, allowing zero-voltage turn-on of switch S_{yp}. The turn-on of switch S_{pm} is furthermore lossless when the inductor current i_{L_P} is positive (which is always the case with AC-to-DC power flow), due to the reversed mechanism as explained in Section 2.3. This analysis can be extended to the switches of the bottom 3L buck circuit. Thus, complete ZVS of all high-frequency semiconductors can be achieved in the Prodrive-Select Rectifier.

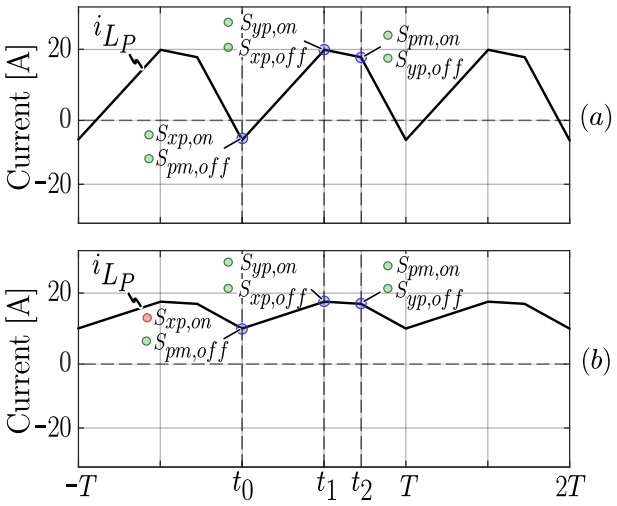

Figure 3.3: Typical waveform of the Prodrive-Select Rectifier inductor current with switching transitions for (*a*) complete ZVS implementation (L_P = small) and (*b*) partial hard-switching implementation (L_P = large). Each transition is accompanied by a green (soft-switching) or red (hard-switching) indication.

3.2.1. Steady-State Analysis

The steady-state analysis of the Prodrive-Select Rectifier is split into two main segments, namely the *Input Voltage Selector* and the *3L buck circuits*. The IVS is analysed only for the mains frequency f_{mains}, Low-Frequency (LF), behaviour, while the 3L buck circuits are analysed for the switching frequency f_{sw}, High-Frequency (HF), behaviour. It is assumed that $f_{sw} >> f_{mains}$.

Input Voltage Selector (IVS) A detailed explanation of the IVS can be found in Section 2.2. The IVS has three input terminals (a, b, c) and three output terminals (X, Y, Z). It is connected to the three-phase grid and forms the input stage of the Prodrive-Select Rectifier. The IVS consists of a passive three-phase rectifier (D_{ax}, D_{bx}, D_{cx}, D_{za}, D_{zb}, D_{zc}), and three active four quadrant switches (S_{aya}, S_{byb}, S_{cyc}), implemented through an anti-series connection of two MOSFETs. The steady-state waveforms during one grid cycle can be seen in Figure 2.5. The voltages v_a, v_b and v_c form a standard, balanced three-phase network. At each moment in time the highest phase voltage is connected to the output terminal X and the lowest phase voltage is connected to the output terminal Z through the passive diode rectifier. The middle phase voltage is then connected to terminal Y through the active four quadrant switches.

The IVS can be described as:

$$\begin{aligned} v_{XM} &= \max(v_a, v_b, v_c) \\ v_{YM} &= \text{med}(v_a, v_b, v_c) \\ v_{ZM} &= \min(v_a, v_b, v_c) \end{aligned} \tag{3.1}$$

Furthermore, in steady-state with unity power factor operation the current through the IVS can be described as:

$$\begin{aligned} i_x &= \max(i_a, i_b, i_c) \\ i_y &= \text{med}(i_a, i_b, i_c) \\ i_z &= \min(i_a, i_b, i_c) \end{aligned} \tag{3.2}$$

3L Buck Circuits The equivalent circuit models for both the top and bottom 3L buck circuit can be seen in Figure 3.4. A few assumptions are made if only the steady-state behaviour is analysed.

$$
\begin{aligned}
&v_{XM} = \langle v_{XM} \rangle, \quad v_{YM} = \langle v_{YM} \rangle, \quad v_{ZM} = \langle v_{ZM} \rangle \\
&v_{PM} = \langle v_{PM} \rangle, \quad v_{NM} = \langle v_{NM} \rangle \\
&v_{PN} = \langle v_{PN} \rangle = \text{constant} \\
&\langle i_{L_P} \rangle = -\langle i_{L_N} \rangle = \langle i_o \rangle = \text{constant}
\end{aligned}
$$

Where $\langle\rangle$ denotes the switching-cycle-averaged value of a parameter.

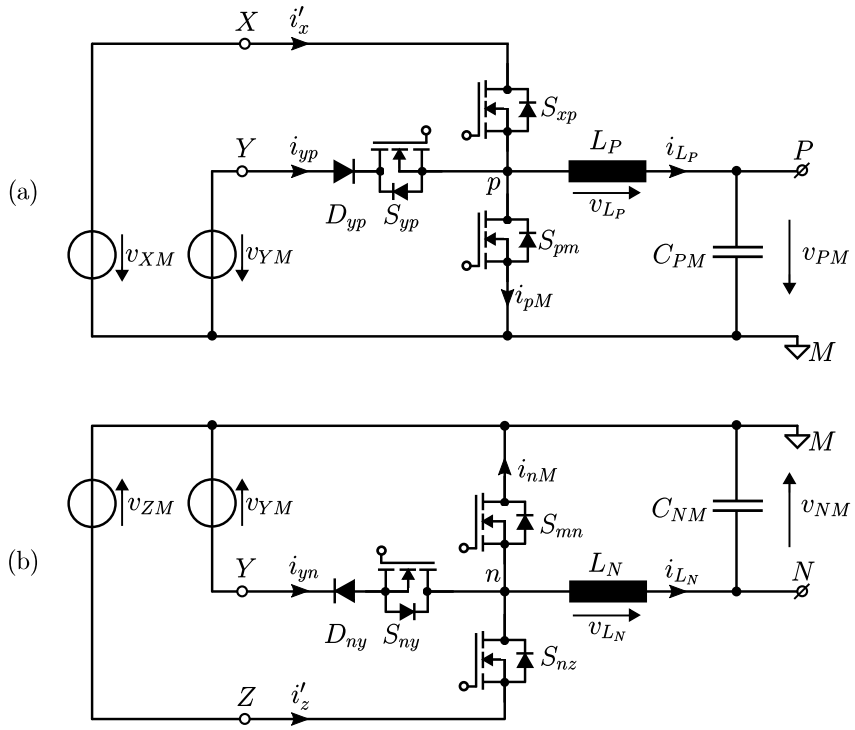

Figure 3.4: Equivalent circuit model of (a) top 3L buck circuit and (b) bottom 3L buck circuit where the IVS has been replaced by equivalent sources v_{XM}, v_{YM}, v_{ZM}.

By applying Kirchhoff's voltage law, the following equations are derived:

$$
\begin{aligned}
&v_{PM} = \langle v_{pM} \rangle = d_{xp} \cdot v_{XM} + (d_{yp} - d_{xp}) \cdot v_{YM} \\
&v_{NM} = \langle v_{nM} \rangle = d_{nz} \cdot v_{ZM} + (d_{ny} - d_{nz}) \cdot v_{YM} \\
&v_{PM} - v_{NM} = v_{PN}
\end{aligned} \tag{3.3}
$$

Where d denotes the duty cycle of the corresponding switch. In steady-state the switching-cycle averaged volt-second across an inductor is zero, $\langle v_{L_P} \rangle, \langle v_{L_N} \rangle = 0$, and thus $\langle v_{pM} \rangle = v_{PM}$ and $\langle v_{nM} \rangle = v_{NM}$

By applying Kirchhoff's current law, the following equations are derived:

$$\langle i_{L_P} \rangle = \langle i_{yp} \rangle + \langle i'_x \rangle - \langle i_{pM} \rangle \tag{3.4}$$

$$\langle i_{L_N} \rangle = \langle i_{yn} \rangle + \langle i'_z \rangle - \langle i_{nM} \rangle \tag{3.5}$$

From these equations, in combination with the operation of the IVS and PFC criteria, the duty-cycles for each active high-frequency switch can be derived as explained in Section 3.2.3.

When analysing the entire converter as depicted in Figure 3.1, the output can be analysed with respect to neutral point G. The operation of the 3L buck circuits does not change and, thus, it is sufficient to derive an expression for the voltage from midpoint M to neutral point G (v_{MG}). An equivalent circuit can be seen in Appendix A, Figure A.1.

Two assumptions can be made when analysing the voltage v_{MG}. If the assumption is made that there is no voltage differential between node G and node M, then the following equation applies.

$$v_{MG} = 0$$

The steady-state waveforms for the operation with $v_{MG} = 0$ can be found in Figure 3.5. Figure 3.5a,b shows the main converter voltage waveforms. Figure 3.5c shows the converter's average intermediate and inductor currents. Figure 3.5d shows the duty cycles for the 3L buck circuit switches as calculated in Section 3.2.3. The 3L buck circuits average input currents form the piece-wise sinusoidal shapes required for achieving unity power factor. The injection current i'_y is formed by both i_{yp} and i_{yn}. The following statements are formulated about the converter currents:

$$\begin{aligned} i_x &= \langle i'_x \rangle \\ i_y &= \langle i'_y \rangle = \langle i_{yp} \rangle + \langle i_{yn} \rangle \\ i_z &= \langle i'_z \rangle \end{aligned} \tag{3.6}$$

If the assumption is made that the voltages v_{PM} and v_{NM} are constant then the following equation applies and a 150Hz component is injected on v_{MG}:

$$v_{MG} = \frac{(v_{XN} - v_{YN}) \cdot d_{xp} + v_{YN} \cdot (d_{yp} + d_{ny}) + (v_{ZN} - v_{YN}) \cdot d_{nz}}{d_{yp} + d_{ny}} \tag{3.7}$$

The steady-state waveforms for $v_{MG} \neq 0$ can be found in Appendix A, Figure A.2

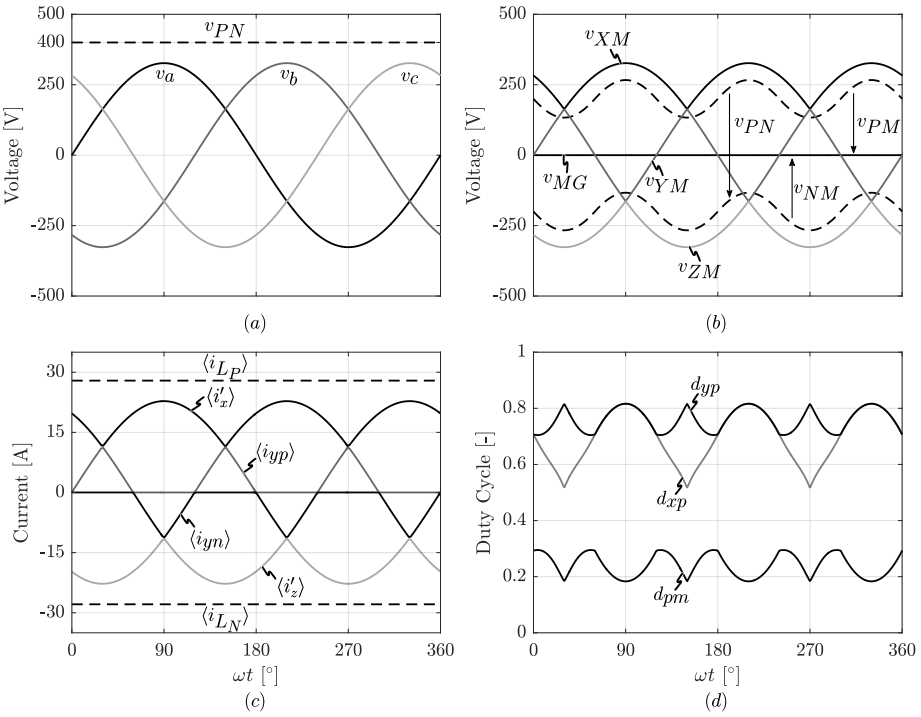

Figure 3.5: Grid-cycle averaged waveforms of (a) three-phase grid and output voltage V_{PN} (b) 3L buck circuit input and output voltages (c) intermediate currents and inductor current and (d) duty-cycles for S_{xp} and S_{yp} under the assumption $v_{MG} = 0$.

3.2.2. Conduction States and Modulation

The analysis of the conduction states and the modulations schemes is shown here for the top 3L buck circuit as the analysis of the bottom 3L buck circuit is identical, but mirrored. The conduction states of the top 3L buck circuit can be seen in Figure 3.6. Evident are the three levels which can be applied to switch-node p, named conduction states I, II and III.

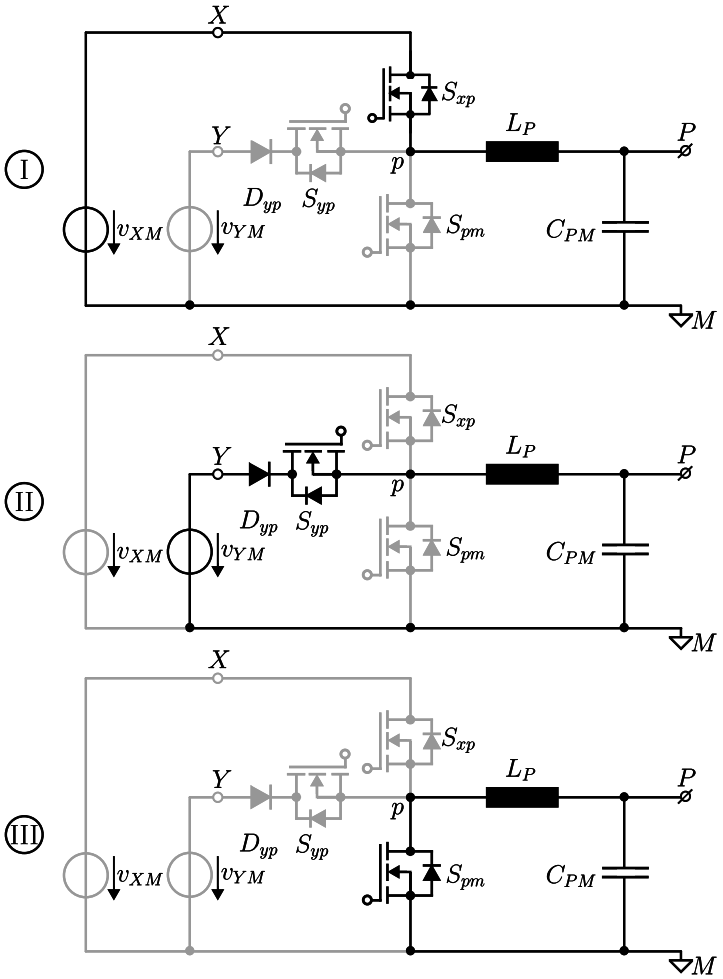

Figure 3.6: Conduction states of the top 3L buck circuit.

With these three levels the 3L buck circuit has to satisfy the steady-state equations of Section 3.2.1. Depending on the carrier wave the conduction sequence and duration of each state differs, which results in a different steady-state condition and inductor current waveforms. The switching cycle waveforms for both a triangular carrier and a sawtooth carrier are shown in Figure 3.7. Depicted in this graph are, sequentially, the conduction states of the switches, the inductor voltage, the inductor current and the switch currents.

The switch currents are formed by segments of the inductor current, each corresponding to the inductor current during their respective conducting time intervals. This means that the average switch currents can be calculated as:

$$\langle i_S \rangle = \frac{1}{T_{sw}} \int_{T_x} i_{L_P}(t) \mathrm{d}t \tag{3.8}$$

Where T_{sw} denotes the time interval of the complete switching cycle, T_x the time interval(s) during which the switch is conducting and $\langle i_S \rangle$ the average switch current.

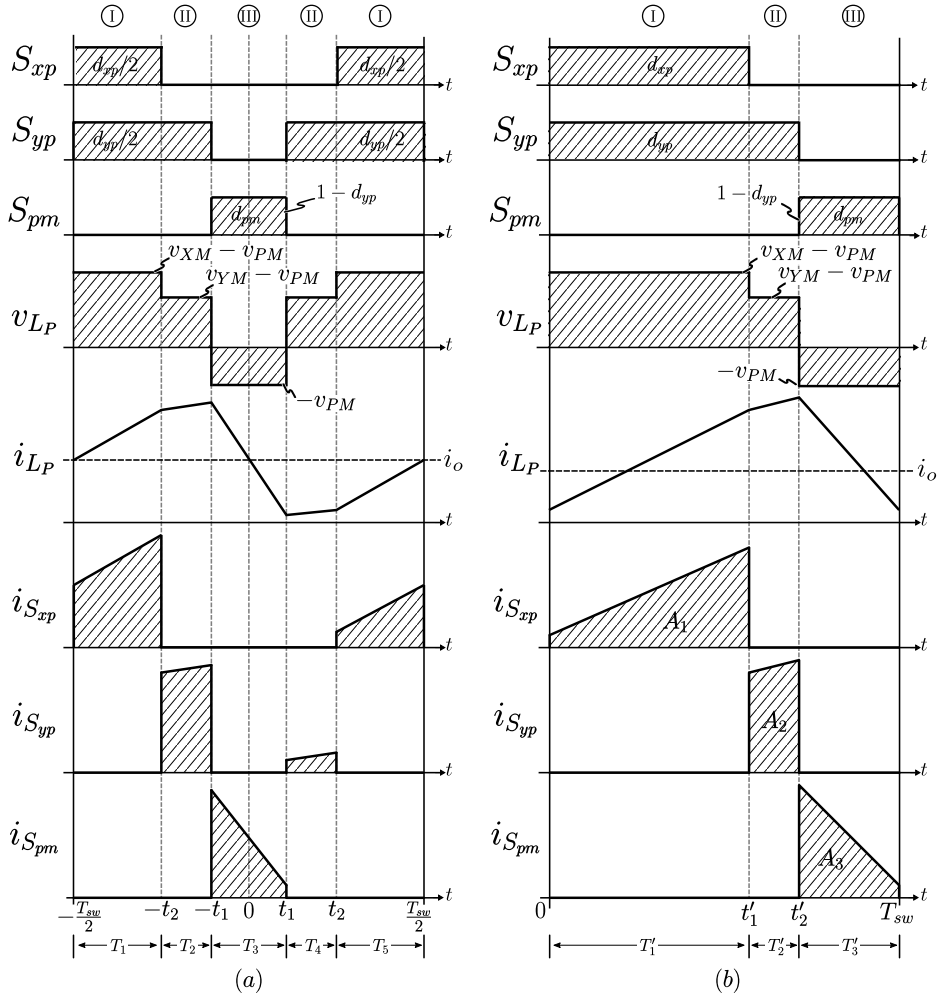

Figure 3.7: Modulation scheme of the top 3L buck circuit with (a) triangular carrier wave and (b) sawtooth carrier wave where the conduction states I,II,III correspond to Figure 3.6.

For the triangular carrier wave, i_o always lies at the center of the switch currents, described by:

$$\frac{\Delta I_S}{2} = \hat{I}_S - i_o \tag{3.9}$$

If Equation 3.9 holds, the average switch current of equation 3.8 can be simplified to:

$$\langle i_S \rangle = d \cdot i_o \tag{3.10}$$

Essentially, the average switch current $\langle i_S \rangle$ is equal to the switch duty cycle d times the output current i_o. The simplification of the average switch current equations are a large advantage for the triangular carrier wave modulation when calculating duty-cycles, see Section 3.2.3. However, if complete ZVS of S_{xp} is to be achieved, it is no longer possible to use the triangular carrier wave modulation. The triangular carrier wave modulation employs a conduction sequence of III,II,I,II. In order to soft turn-on switch S_{xp} at t_2 the inductor current has to be negative, which means that the inductor current has to be negative during T_4 as well. In this case, during T_4 no current flows through S_{yp} as this is prevented by the anti-series diode D_{yp} and instead the negative inductor current forces conduction state I. In this case the steady-state conditions are no longer met and this modulation scheme is thus not possible when trying to operate the buck circuit with negative inductor current.

In order to combat this the sawtooth carrier modulation from Figure 3.7*b* can be used, which ensures a conduction sequence of I,II,III. This combination means that conduction state I directly follows conduction state III which allows soft turn-on of switch S_{xp} if the inductor current is negative at the end of T_3'. At the

end of T_1' the inductor current has once again become positive, meaning conduction state II can naturally follow conduction state I. This conduction sequence allows the steady-state conditions to be met irrespective of the inductor current polarity. However, for sawtooth carrier modulation Equation 3.9 is no longer valid, thus the average switch current equations can no longer be simplified which leads to increased complexity of the duty-cycle calculations, see Section 3.2.3.

3.2.3. Duty Cycle Calculation

Triangular Carrier As explained in Section 3.2.2 the triangular carrier wave modulation scheme can use the simplified average switch current of Equation 3.10. For each switch in the top 3L buck circuit the average switch current can then be denoted as:

$$\begin{aligned}\langle i_{S_{xp}}\rangle &= \mathrm{d}_{xp}\cdot i_o\\ \langle i_{S_{yp}}\rangle &= (\mathrm{d}_{yp}-\mathrm{d}_{xp})\cdot i_o\\ \langle i_{S_{pm}}\rangle &= \mathrm{d}_{pm}\cdot i_o = (1-\mathrm{d}_{yp})\cdot i_o\end{aligned}$$

In order to guarantee unity power factor the average switch current in switches S_{xp} and S_{yp} can be set to $\langle i_{S_{xp}}\rangle = i_x$ and $\langle i_{S_{yp}}\rangle = i_{yp}$, where $i_{yp} = \max(i_y, 0)$ denoting only positive values of i_y. This leads to an equation for the duty cycles as:

$$\begin{aligned}\mathrm{d}_{xp} &= \frac{i_x}{i_o}\\ \mathrm{d}_{yp} &= \mathrm{d}_{xp} + \frac{i_{yp}}{i_o} = \frac{i_x + i_{yp}}{i_o}\end{aligned} \tag{3.11}$$

Where S_{yp} can be left on in conduction state I without negative consequences due to the fact that $v_{XM} > v_{YM}$, thus reducing the switching instances and simplifying the modulation scheme. These equations are used to derive a voltage relationship as detailed in Section A.2. The duty cycles for the triangular carrier wave, for both 3L buck circuits, can then be described as:

$$\begin{aligned}\mathrm{d}_{xp} &= \frac{2}{3}\cdot\frac{v_{XM}\cdot v_{PN}}{v_{1ph,ampl}^2}\\ \mathrm{d}_{yp} &= \frac{2}{3}\cdot\frac{(v_{XM}+v_{YMp})\cdot v_{PN}}{v_{1ph,ampl}^2}\\ \mathrm{d}_{nz} &= -\frac{2}{3}\cdot\frac{v_{ZM}\cdot v_{PN}}{v_{1ph,ampl}^2}\\ \mathrm{d}_{ny} &= -\frac{2}{3}\cdot\frac{(v_{ZM}+v_{YMn})\cdot v_{PN}}{v_{1ph,ampl}^2}\end{aligned} \tag{3.12}$$

Where $v_{YMp} = \max(v_{YM}, 0)$ the positive values of v_{YM} and $v_{YMn} = \min(v_{YM}, 0)$, the negative values of v_{YM}. These duty cycles are derived from the current dependency of the switch currents, ensuring correct behaviour of the currents i_x, i_y and i_z. The criteria on the output voltage can be verified by inputting the duty cycle Equations 3.12 into the average voltage Equations 3.3.

Sawtooth Carrier For the sawtooth modulation scheme the average switch currents can not be simplified, and Equation 3.8 has to be used in order to calculate these. The average switch currents for the top 3L buck circuit can be described as:

$$\begin{aligned}\langle i_{Sxp}\rangle &= \frac{1}{T_{sw}}\int_0^{t_1'} i_{L_P}(t)\mathrm{d}t = A_1\\ \langle i_{Syp}\rangle &= \frac{1}{T_{sw}}\int_{t_1'}^{t_2'} i_{L_P}(t)\mathrm{d}t = A_2\\ \langle i_{Spm}\rangle &= \frac{1}{T_{sw}}\int_{t_2'}^{t_3'} i_{L_P}(t)\mathrm{d}t = A_3\end{aligned} \tag{3.13}$$

An increased degree of freedom results from the utilization of the third level in the 3L buck circuit as opposed to the standard 2L circuit. This means that a volt-second balance alone is insufficient to constrain the system as this results in infinite possibilities. It is opted to extend the constraints on the system by setting the average switch currents equal to the required currents for unity power factor. A system of equations is created which describes all the constraints placed on the system:

$$\begin{aligned}&A_1 + A_2 + A_3 = i_o\\ &A_1 = i_X\\ &A_2 = i_{Yp}\\ &\mathrm{d}_{xp} + \mathrm{d}_{yp} + \mathrm{d}_{pm} = 1\\ &\mathrm{d}_{yp} \geq \mathrm{d}_{xp}\\ &i_{LP}(0) = i_{LP}(T_{sw})\end{aligned} \tag{3.14}$$

This system of equations can be solved analytically, but results in huge duty-cycle equations which become unusable. Therefore, it is opted to solve this system semi-analytically. By releasing one parameter, for instance d_{xp}, the equations can be rewritten to be only dependent on that parameter. The parameter d_{xp} can then be brute force swept until all conditions are met. Alternatively, the system of equations can be solved by a solver function, such as *fsolve()* or *fmincon()* in MATLAB. The duty-cycles for both the triangular and sawtooth modulation scheme for varying output voltage v_{PN} can be seen in Figure 3.8.

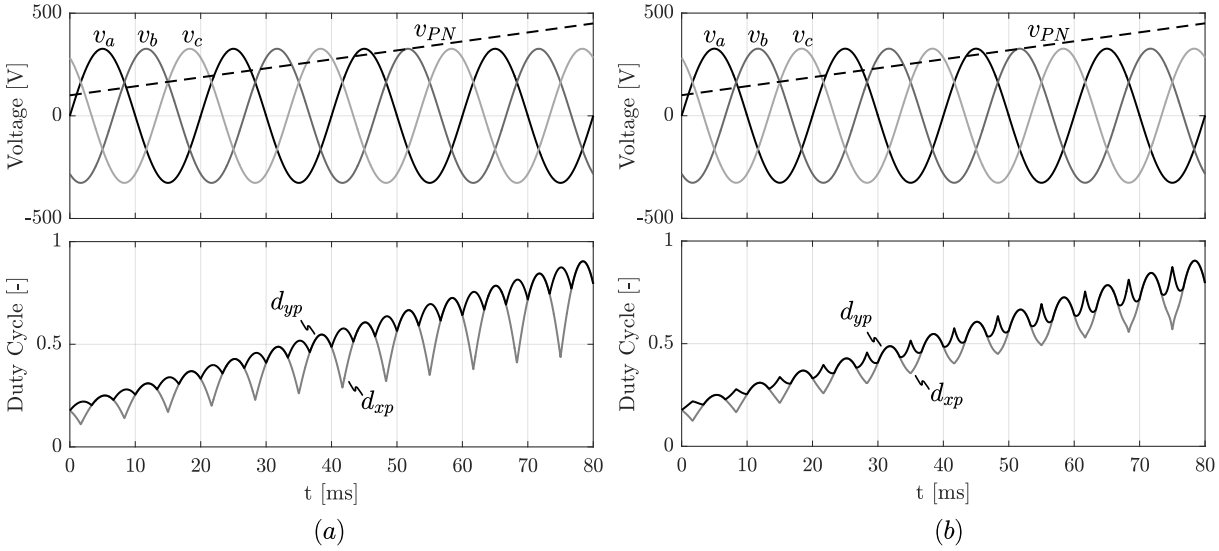

Figure 3.8: Duty-cycles d_{xp} and d_{yp} for varying v_{PN} for (*a*) triangular carrier modulation and (*b*) sawtooth carrier modulation.

For the remainder of this thesis the sawtooth carrier modulation is used for complete or partial soft-switching designs of the Prodrive-Select Rectifier. The triangular carrier modulation is used in Chapter 8 for demonstration of a complete hard-switching design.

3.3. Semiconductor Stresses

The semiconductor stresses determine which maximum blocking voltage the semiconductor should be able to withstand. Higher blocking voltages are usually paired with increased switching losses as the drain-source capacitance is generally increased. The blocking voltage furthermore determines which class of semiconductors are feasible for use, i.e. Si, SiC, GaN. The semiconductor blocking voltages for the Prodrive-Select Rectifier can be found in Table 3.1.

Table 3.1: Prodrive-Select Rectifier semiconductor maximum blocking voltages.

Semiconductor	Parameter	Value	Unit
S_{xp}	$v_{ds,S_{xp},max}$	357.5	V
S_{yp}	$v_{ds,S_{yp},max}$	179	V
S_{pm}	$v_{ds,S_{pm},max}$	357.5	V
D_{yp}	$v_{ak,D_{yp},max}$	537	V
S_{nz}	$v_{ds,S_{nz},max}$	357.5	V
S_{ny}	$v_{ds,S_{ny},max}$	179	V
S_{mn}	$v_{ds,S_{mn},max}$	357.5	V
D_{ny}	$v_{ak,D_{ny},max}$	537	V
$D_{abc,xz}$	$v_{ak,D_{abc,xz},max}$	620	V
S_{yabc}	$v_{dsd,s_{yabc},max}$	537	V

Input Voltage Selector The IVS consists of the passive diodes D_{ax}, D_{bx}, D_{cx}, D_{za}, D_{zb}, D_{zc} ($D_{abc,xz}$) and the bi-directional switches S_{aya}, S_{byb}, S_{cyc} (S_{yabc}). The maximum blocking voltage of the passive diodes ($S_{abc,xz}$) is the maximum line-to-line voltage:

$$v_{ak,D_{abc,xz},max} = v_{G,l-l,max} = v_{G,1ph,ampl} \cdot \sqrt{3} = 620V$$

The bi-directional switches (S_{yabc}) have a maximum blocking voltage of the minimum line-to-line voltage:

$$v_{dsd,S_{yabc},max} = v_{G,l-l,min} = v_{G,1ph,ampl} \cdot \frac{3}{2} = 537V$$

The rms and average current through the passive diodes $D_{abc,xz}$ can be analytically calculated as:

$$i_{D_{abc,xz},rms} = \frac{2}{3} \cdot \frac{P_o}{V_{G,1ph,ampl}} \cdot \sqrt{\frac{1}{6} + \frac{\sqrt{3}}{8\pi}}$$

$$i_{D_{abc,xz},avg} = \frac{1}{\sqrt{3}\pi} \cdot \frac{P_o}{v_{G,1ph,ampl}}$$

The rms and average current through the bi-directional switches S_{yabc} can be analytically calculated as:

$$i_{S_{yabc},rms} = \frac{2}{3} \cdot \frac{P_o}{V_{G,1ph,ampl}} \cdot \sqrt{\frac{1}{6} - \frac{\sqrt{3}}{4\pi}}$$

$$i_{S_{yabc},avg} = 0$$

In order to make a selection of the semiconductors for the IVS it is necessary to consider a certain safety margin in case of undesirable oscillations or grid transients. It is possible to use semiconductors in the range of 900V or 1200V, where a margin of >40% is considered sufficient. In the IVS the switching losses of the bi-directional switches can be neglected as the switching frequency is only twice the mains frequency which contributes to negligible switching losses. The dominant factor for this choice is then the on-state losses. For $D_{abc,xz}$ diodes should be selected with low forward-voltage, while for S_{yabc} MOSFETs with low $R_{DS,on}$ are recommended.

3L Buck Circuits The high-frequency 3L buck circuits contain the active switches S_{xp}, S_{yp}, S_{pm}, D_{yp}, S_{nz}, S_{ny}, S_{mn}, D_{ny}. The stresses can be derived from the conduction states from Section 3.2.2 and are shown for the top 3L buck circuit, as the stresses for the bottom 3L buck circuit are analogous.

The maximum blocking voltage of semiconductor S_{xp} is the maximum voltage of v_{XM}:

$$v_{ds,S_{xp},max} = v_{XM,max} = v_{G,1ph,ampl} = 357.5V$$

The maximum blocking voltage of semiconductor S_{yp} is the maximum voltage of v_{YM}:

$$v_{ds,S_{yp},max} = v_{YM,max} = v_{G,1ph,ampl} \cdot \frac{1}{2} = 179V$$

The maximum blocking voltage of semiconductor D_{yp} is the maximum voltage between X and Y:

$$v_{ak,D_{yp},max} = v_{XY,max} = v_{G,1ph,ampl} \cdot \frac{3}{2} = 537V$$

The maximum blocking voltage of semiconductor S_{pm} is the maximum voltage of v_{XM}:

$$v_{ds,S_{pm},max} = v_{XM,max} = v_{G,1ph,ampl} = 357.5V$$

The rms and average current of the semiconductors is not shown analytically as this varies per modulation scheme, instead these should be estimated through the definition as:

$$i_{S,avg} = \frac{1}{T}\int_T i_S dt$$
$$i_{S,rms} = \sqrt{\frac{1}{T}\int_T i_S^2 dt}$$

These high-frequency semiconductors suffer from significantly higher switching losses than the IVS and these can no longer be ignored. Section 5.5.2 explains the modelling of the semiconductor losses.

The 3L buck circuit semiconductors could be implemented with standard Si MOSFETs, but other choices such as SiC or GaN are also of interest. This research has focused on the use of SiC MOSFETs for these semiconductor devices because of their superior on-state resistance and switching performance. For the active switches S_{xp}, S_{pm}, S_{nz}, S_{mn} it is possible to use devices with a blocking voltage of 450V, where a safety margin of $\approx$ 20% is taken into account. For the diodes D_{yp}, D_{ny} semiconductor devices with a blocking voltage of 650V can be used if a safety margin of $\approx$ 20% is taken into account. The two active switches in the injection path S_{yp}, S_{ny} can be implemented with 250V devices.

3.4. Summary

This chapter serves as the introduction of a novel three-phase buck-type PFC rectifier, named the Prodrive-Select Rectifier. The circuit topology, along with typical waveforms, are depicted and described in detail. The Prodrive-Select Rectifier utilizes the third-harmonic current injection principle and contains two series connected three-level buck circuits which allow for complete ZVS of the high-frequency semiconductors.

A mathematical steady-state analysis of the 3L buck circuits is provided in which different operating conditions, regarding the capacitive midpoint common-mode voltage, are highlighted. Two modulation schemes, along with their conduction states, are investigated. It is concluded that solely the sawtooth carrier modulation scheme is suitable when ZVS of the semiconductors is required.

Furthermore, the chapter describes the duty cycle calculation for both modulation schemes and determines the stresses for both the low- and high frequency semiconductors.

4

Closed-Loop Control

4.1. Introduction

This chapter investigates the proposed closed-loop control of the Prodrive-Select Rectifier. Relevant dynamic waveforms, such as converter start-up, are shown, as well as, steady-state waveforms in order to verify the converter analysis. The Prodrive-Select Rectifier, as shown in Figure 6.8, is simulated both with and without interleaving of the output stages. The relevant parameters during transient simulation are the output voltage regulation, the input current THD, the grid power factor and the converter start-up behaviour. Table 4.1 summarizes the converter parameters of the performed simulation of the Prodrive-Select Rectifier.

Table 4.1: Simulated Prodrive-Select Rectifier parameters.

Description	Parameter	Value	Unit
single phase rms voltage	$v_{G,1ph,rms}$	230	V
single phase peak voltage	$v_{G,1ph,ampl}$	325	V
Mains frequency	f_G	50	Hz
Output voltage	v_{PN}	400	V
Output power	P_o	11	kW
Buck inductance	L_P/L_N	15	μH
Switching frequency	f_{sw}	72	kHz
Output voltage ripple	$v_{PN,pp}$	$\pm$1	V
Input current THD	$\text{THD}_{i_{abc}}$	<8%	-
Input displacement factor	Φ	>0.99	-
Input power factor	λ	>0.99	-

4.2. Control Scheme

Figure 4.1 shows the proposed standard control scheme of the Prodrive-Select Rectifier. The controller uses a voltage measurement on the output voltages v_{PM} and v_{MN} which is used to create v_{PN} and v_{bal}. The DC bus voltage V_{PN} is compared with the set-value v^*_{PN} and fed into a slow outer loop voltage PI controller. The output of this controller is the set-value of the inductor DC current i^*_{ampl}. The two inductor currents i_{LP} and i_{LN} are measured and averaged to create i_L and compared to the set-value i^*_{ampl} before being fed into a joint fast inner loop current PI controller. The output of the inductor current controller is the set-point for the switch-node voltage v_{sn}. The balance P controller on v_{bal} is responsible for correcting any imbalance between v_{PM} and v_{MN}. The output of the balanced switch-node voltage is multiplied by the reference signals REF_{xyz} to transform the DC set-point into a piece-wise sinusoidal set-point for the active switches. The signal is then divided by $\frac{3}{4} \cdot \hat{U}_{abc} = \frac{3}{4} \cdot v_{G,1ph,ampl}$ = 243.75V, as this is the maximum achievable output voltage per buck circuit and normalizes the duty-cycles to a value between 0 and 1.

A phase-locked loop (PLL) is placed on voltage measurements of the three-phase grid. The PLL locks onto the grid frequency and together with the reference generator outputs grid parameters such as grid frequency (f_{abc}), grid voltage amplitude ($\hat{U}_{abc}$) and grid phase (ϕ_{abc}). The reference generator creates the duty cycles for the bi-directional switches (d_{IVS}) of the IVS, and generates the signals REF$_{xyz}$, which are in phase with the three-phase grid. The reference signals have to be shaped to be proportional to the duty-cycles of Section 3.2.3. For the triangular carrier modulation scheme the reference signals (duty-cycle shapes) are valid for the entire operating range and irrespective of component values. The duty-cycles for the sawtooth carrier modulation however vary with converter parameters such as output voltage, output power and L_P inductance. The non-linear dependence on these parameters has to be incorporated in the reference generator, e.g. with a look-up table, in order to use the control scheme of Figure 4.1.

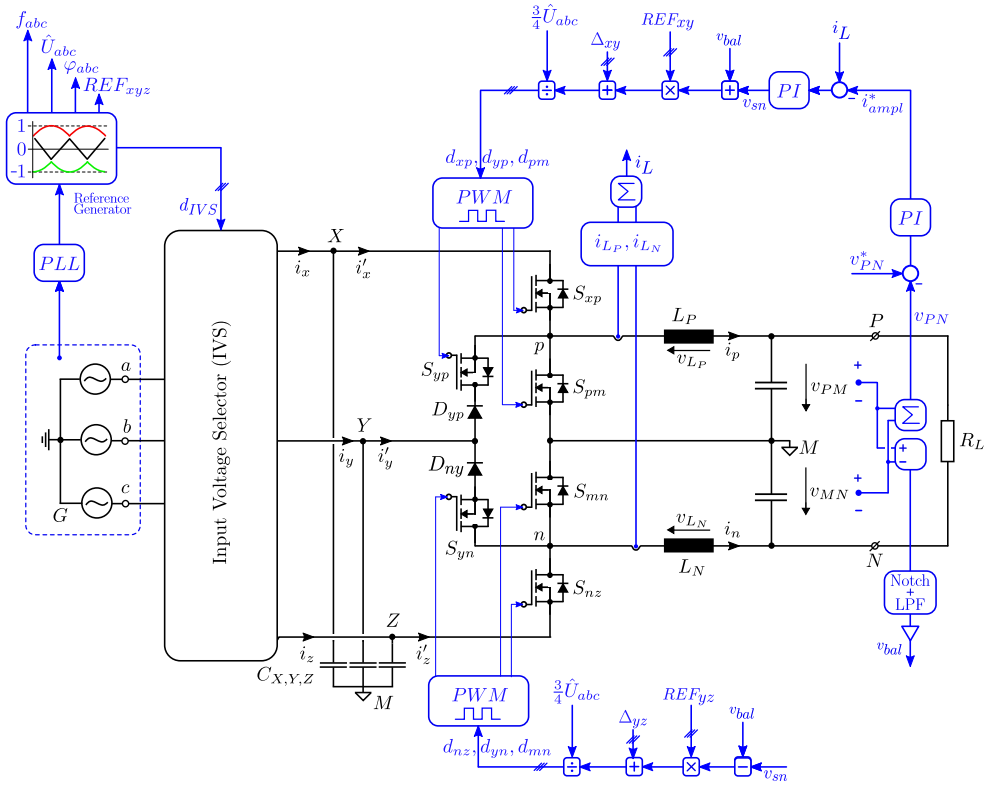

Figure 4.1: Proposed *standard* control scheme for the Prodrive-Select Rectifier.

If a constant reference signal is used in combination with the sawtooth carrier modulation, the extended control scheme of Figure 4.2 is proposed. In this case the reference signal REF$_{xyz}$ is only an approximation of the duty cycle shapes, without dependence on converter parameters. In this control scheme current PI controllers are added on i_x,i_y and i_z placed cascaded to the inductor current controllers to ensure these currents follow the correct shapes proportional to voltages v_{XM}, v_{YM} and v_{ZM}. These controllers have relatively little control but correct the small deviation from the ideal sine wave in case of converter parameter variation and alleviate the need for look-up tables in the reference generator.

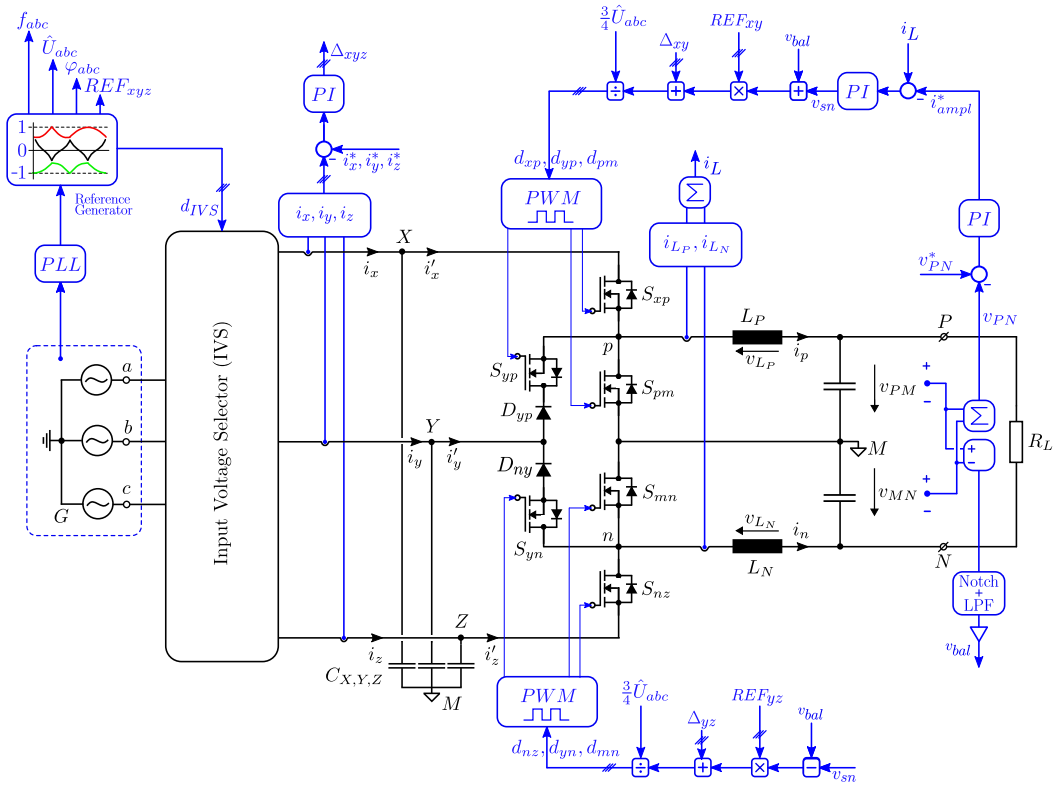

Figure 4.2: Proposed *extended* control scheme for the Prodrive-Select Rectifier with i_x,i_y,i_z current controllers.

4.3. Simulation

The simulation of the Prodrive-Select Rectifier is done in Simulink/PLECS. Figure 4.3 shows the simulated waveforms for the rectifier during start-up both with and without an interleaved output stage using the standard control scheme from Figure 4.1. The simulation parameters are listed in Table 4.1. The switching frequency is chosen at 72kHz because this is the switching frequency of the built prototype (see Section 8). The inductance L_P and L_N equals 15μH because this results in a soft-switched interleaved variant. Evident from Figure 4.3 is the voltage regulation of v_{PN} to the set-point of 400V. The voltage step from 0V to 400V takes roughly 15ms. In steady-state the peak-to-peak voltage ripple on the output $v_{PN,pp}$ equals ±1V.

The fundamental of the current waveforms i_a, i_b and i_c is taken when considering the displacement factor of the converter. In both simulations the displacement factor $\Phi > 0.99$. Furthermore, the THD of the input currents, as explained in Section 2.2, equals less than 8% in both cases. The main cause of the harmonic distortion in the current waveform is the switching of the IVS at the sector boundaries, similar to the Swiss Rectifier. Due to the nature of the controller, the current distortion also produces a distortion in the third phase, which does not participate in the commutation. Extensive research has been done in this field in order to minimize the produced current distortion [11], [17], [18]. Possible solutions include an extended controller that applies PWM to the selector switches S_{yabc} at the sector boundaries or an interleaving of the output stages in order to reduce the amplitude of the current distortion. Note that the amplitude of the distortion is reduced significantly when an interleaved variant is simulated as in Figure 4.3*b*.

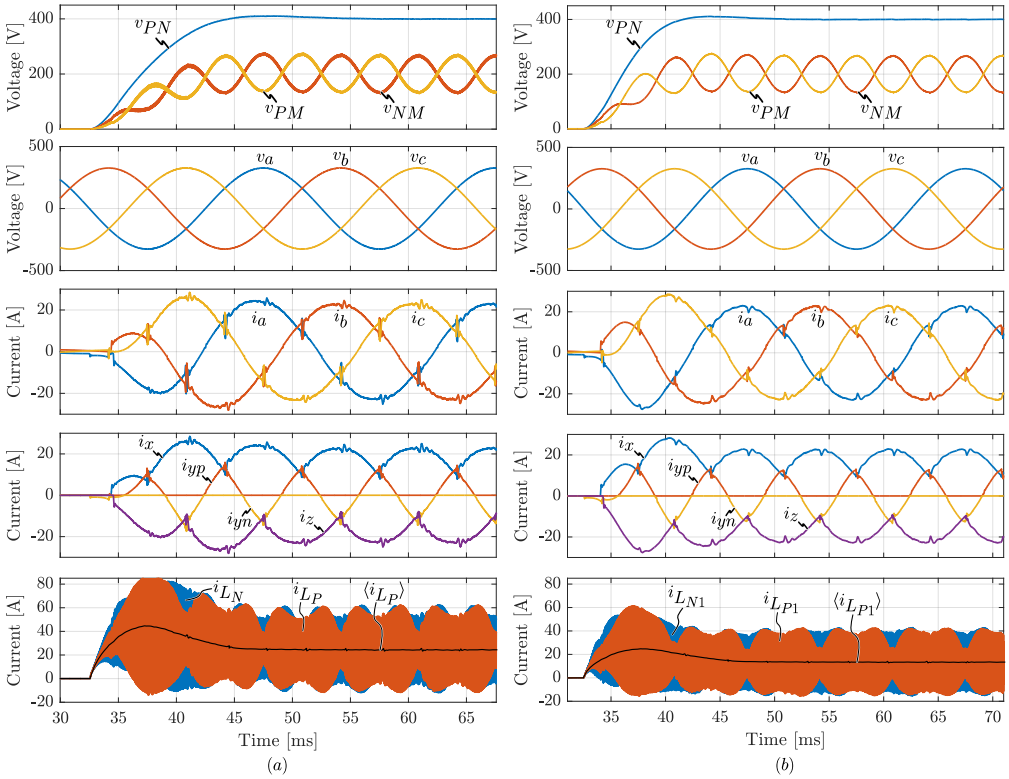

Figure 4.3: Simulink/PLECS simulation of the the start-up and steady-state behaviour of the Prodrive-Select Rectifier [(*a*) non-interleaved and (*b*) once interleaved] with the standard control scheme of Figure 4.1 (sawtooth carrier) and the converter parameters as specified in Table 4.1.

Further harmonic distortion is introduced due to the implementation of the standard control scheme, where the duty cycles estimated with REF_{xyz} do not produce perfect sinusoidal input currents due to parameter variation and non-linear effects. An option to mitigate this effect is to use the extended control scheme of Figure 4.2. The THD and Φ combined contribute to a power factor of above 0.99 for both simulations.

After t = 55ms the converter has reached steady-state. The converter intermediate currents i_x, i_{yp}, i_{yn} and i_z exhibit the same piece-wise sinusoidal shapes as determined in Chapter 3. Furthermore, the inductor average and ripple current correspond to the waveforms calculated with Fourier modelling in Chapter 3.

4.4. Summary

This chapter proposes two closed-loop control scheme for the Prodrive-Select Rectifier. The chapter is purposefully kept short because the control of the PFC rectifier is out of scope for this work. The proposed control schemes contain fast inner-loop current controllers and slower outer-loop voltage controllers. A simulation of a non-interleaved and interleaved variant of the Prodrive-Select Rectifier verify the previously determined steady-state models and show compliance with expected power quality parameters such as THD and power factor.

5

Modelling of the Main Converter Components

5.1. Introduction

The modelling of power converters has been a much discussed topic in research where a strong emphasis is put on the mathematical approach, as opposed to a simulation-based approach, because a solid analytical base model paves the way for more advanced modelling and optimization techniques [19]. Detailed mathematical multi-physics models of the converter and the individual components provide a complete picture when all performance aspects, such as volume, losses, EMI and thermal stress, are included in the design space. The goal of this mathematical modelling is to derive the performance trade-offs dependent on a set of optimization parameters, such as switching frequency or inductance, for a certain converter topology or configuration by means of rapid, virtual prototyping. The proposed modelling technique allows for the specification of a broad design space within which optimal implementations are only visible through multi-objective optimization. In this work the performance space is limited to the power density and efficiency.

This chapter describes the mathematical converter modelling approach of this research; Basic Analysis, Fourier Analysis and Component Models are discussed in detail. The benefits of the proposed approach and the individual models are discussed and conclusions are drawn on the performance trade-offs specific to the optimization parameters of efficiency and power density and applied to the hardware demonstrator of the Prodrive-Select Rectifier as described in Chapter 8.

5.2. Modelling Approach

Figure 5.1 shows the modelling approach proposed by this research. The complete mathematical model and component libraries are implemented in MATLAB. First, converter operating parameters, such as input voltage v_i, output voltage v_o, output power P_o, EMC limits, have to be specified in order to evaluate the electrical characteristics within which the converter is operating. Next, the converter specific parameters are specified. These include, for instance, the converter topology, the interleaved stages, the paralleled switches, the modulation scheme, etc.

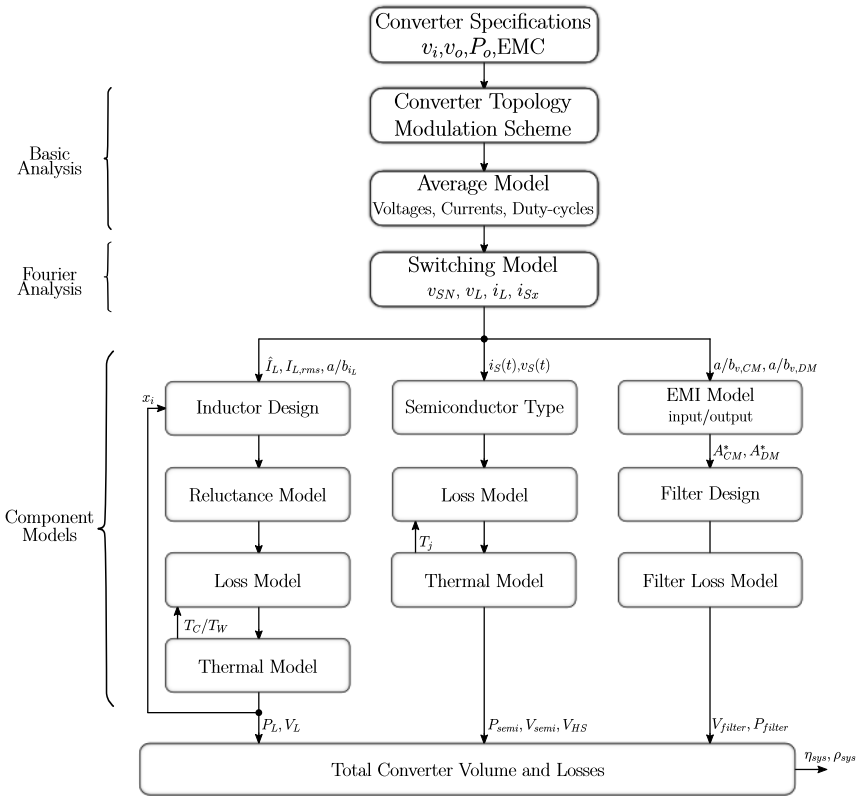

Figure 5.1: Proposed converter modelling approach block diagram where initial converter and component specification are an input and the complete system efficiency and volume are an output.

Based on these inputs, the converter-specific average model is used to derive the resulting waveforms. The derivation of the average model of the Prodrive-Select Rectifier can be found in Section 3.2.1. In the case of the Prodrive-Select Rectifier the average model calculates grid cycle voltages, currents and duty-cycles, for example; v_a, v_{XM}, i_x, i_{Lp} as depicted in Figure 3.1. The converter topology specifications and the average model are denoted as the Basic Analysis and described in Section 5.3.

Using the results of the average model, the switching model derives switching cycle waveforms for the important converter components, such as the switch node voltage v_{SN}, the inductor voltage v_L. the inductor current i_L or the switch currents i_{Sx}. These switching cycle waveforms are analysed firstly in the Fourier domain in order to increase the modelling possibilities, in particular with respect to EMC modelling. The obtained Fourier coefficients can be used to calculate a time vector of the switching cycle waveforms through the inverse Fourier transform as discussed in Section 5.4.

The main components of the converter can now be analysed separately with their respective switching cycle or grid cycle averaged waveforms. The component models can be separated into inductor model, semiconductor model and EMI model. The required outputs from each component model are the losses and volume of that component. Additional outputs can include semiconductor junction temperature T_j, inductor core and winding temperature T_C/T_W or required attenuation A^*_{CM}, A^*_{DM}. These models give a detailed but fractured performance indication of the modelled converter.

As a final step, a summation of the component model outputs gives an estimation of the total converter volume and losses which can be translated to converter power density and efficiency. This modelling approach results in a generalized and effective framework that is ideal for modelling a converter with a large design space, for instance modelling a converter for a variety of switching frequencies.

5.2.1. Virtual Prototyping Routine

The mapping of the design space into the performance space can be automatized by means of a virtual prototyping routine which results in an objective performance indication of the converter for all chosen modelling parameters [20]. The proposed virtual prototyping routine is depicted in Figure 5.2. Evident is the subdivision into *Global* Design Space, *Component* Design Space, and Performance Space. The global design space specifies converter operating conditions, converter topology parameters and the design variables. An example of a global design space can be found in Table 6.1. The component design space specifies component selection parameters, component material parameters and component design variables. An example of a component design space can be found in Table 6.2.

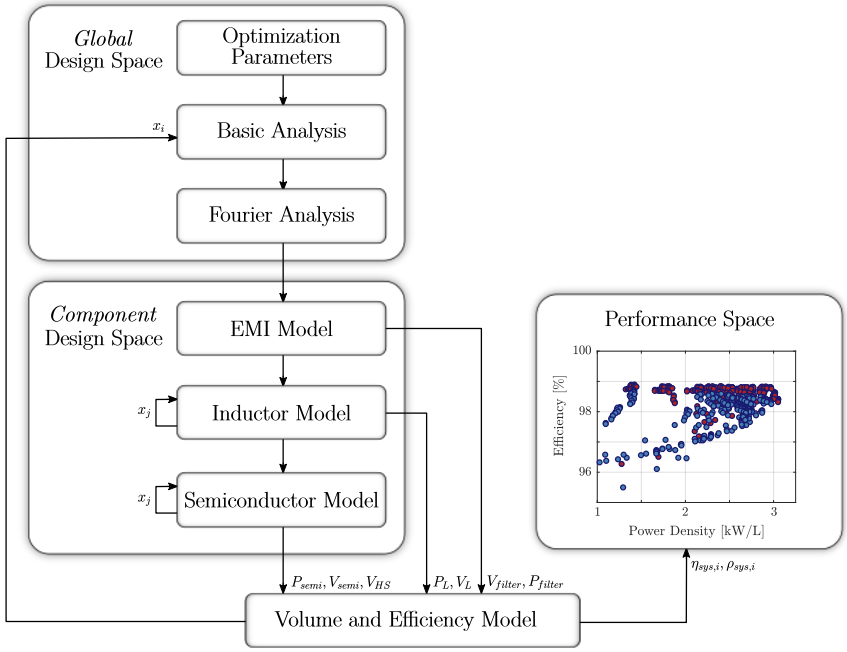

Figure 5.2: Proposed virtual prototyping routine utilizing the converter modeling approach depicted in Figure 5.1. The global and component design spaces are a user input depending on the optimization parameter and design freedom. x_i denotes the i^{th} iteration of the global design space and x_j denotes the j^{th} iteration of the component design space. The volume and efficiency model outputs the system volume and efficiency for x_i.

The virtual prototyping routine sequentially calls the Basic Analysis, Fourier Analysis, EMI Model, Inductor Model, Semiconductor Model and Volume and Efficiency Model. An iteration x_i of a global design space variable leads to a reiteration of the complete modelling loop, while an iteration x_j of a component design space variable leads to a local component model loop. Component design space iterations are not all output to the volume and efficiency model, but they are locally optimized for, for instance, lowest losses or volume, before the j^{th} iteration is selected as the optimal implementation and passed along.

Each iteration x_i corresponds to a component optimized implementation of the global design parameters and subsequently the volume and efficiency model produces a total system volume and power density estimation for the i_{th} iteration which is passed along to the performance space. When all global design variables have been looped, the performance space is filled with all possible implementations of the converter system bounded by the design space. Manipulation of the performance space yields a discernible Pareto-front from which an optimal design can be selected. Chapter 6 puts this routine into practice with the design optimization of the Prodrive-Select Rectifier for an 11-kW on-board EV charger.

5.3. Basic Analysis

The basic analysis includes the converter topology, modulation scheme and average model as explained in Section 5.2. This section is converter specific and is an essential first step in analytical modelling of power converters. The approach is to derive mathematical formulations of all converter specific, grid-cycle averaged waveforms through manipulation of Kirchhoff's current and voltage laws, as well as, inductor volt-second and capacitor ampere-second balance equations. The basic analysis of the Prodrive-Select Rectifier can be found in Chapter 3. An example of grid cycle average waveforms for the Prodrive-Select Rectifier can be seen in Figure 3.5. This analysis can already give an indication of the average current and voltage ratings of the converter components without detailed switching cycle analysis.

5.4. Fourier Analysis

The Fourier analysis is used to generate switching cycle waveforms of the converter components. A single-sided Fourier description of a square wave can be derived in terms of its amplitude (U), duty-cycle (D) and phase-shift (ϕ), from the generalized Fourier equations:

$$\begin{aligned} x_T(t) &= a_0 + \sum_{n=1}^{\infty} [a_n \cos(n w_0 t) + b_n \sin(n w_0 t)] \\ a_0 &= \frac{2}{T}\int_T x_T(t)\cdot \mathrm{d}t \\ a_n &= \frac{2}{t}\int_T x_T(t)\cdot \cos(n w_0 t)\cdot \mathrm{d}t, \qquad (n \neq 0) \\ b_n &= \frac{2}{T}\int_T x_T(t)\cdot \sin(n w_o t)\cdot \mathrm{d}t \end{aligned} \tag{5.1}$$

The Fourier coefficients a and b of a one-level square wave can be described as:

$$\begin{aligned} a_n &= \frac{2U}{n\omega T}\cdot\left(\sin(n\omega T\left[D+1/\phi\right]) - \sin(n\omega T/\phi)\right), \qquad (n \neq 0) \\ b_n &= \frac{2U}{n\omega T}\cdot\left(\cos(n\omega T/\phi) - \cos(n\omega T[D+1/\phi])\right) \\ a_0 &= U\cdot D \end{aligned} \tag{5.2}$$

where a and b are the Fourier coefficients and $x_T(t)$ the time domain signal. This description is used to generate the Fourier coefficients of circuit voltage waveforms, i.e. switch-node voltage or inductor voltage. The coefficients are used to generate a time-domain representation of the switching-cycle waveform by an inverse Fourier transform, an example of which is given for the Prodrive-Select Rectifier as seen in Figure 5.3*a*. The inductor voltage is used to calculate the inductor current by performing an integration action, where the following dependency holds:

$$\begin{aligned} a_{i_L} &= -\frac{b_{v_L}}{n\omega L} \\ b_{i_L} &= \frac{a_{v_L}}{n\omega L} \end{aligned} \tag{5.3}$$

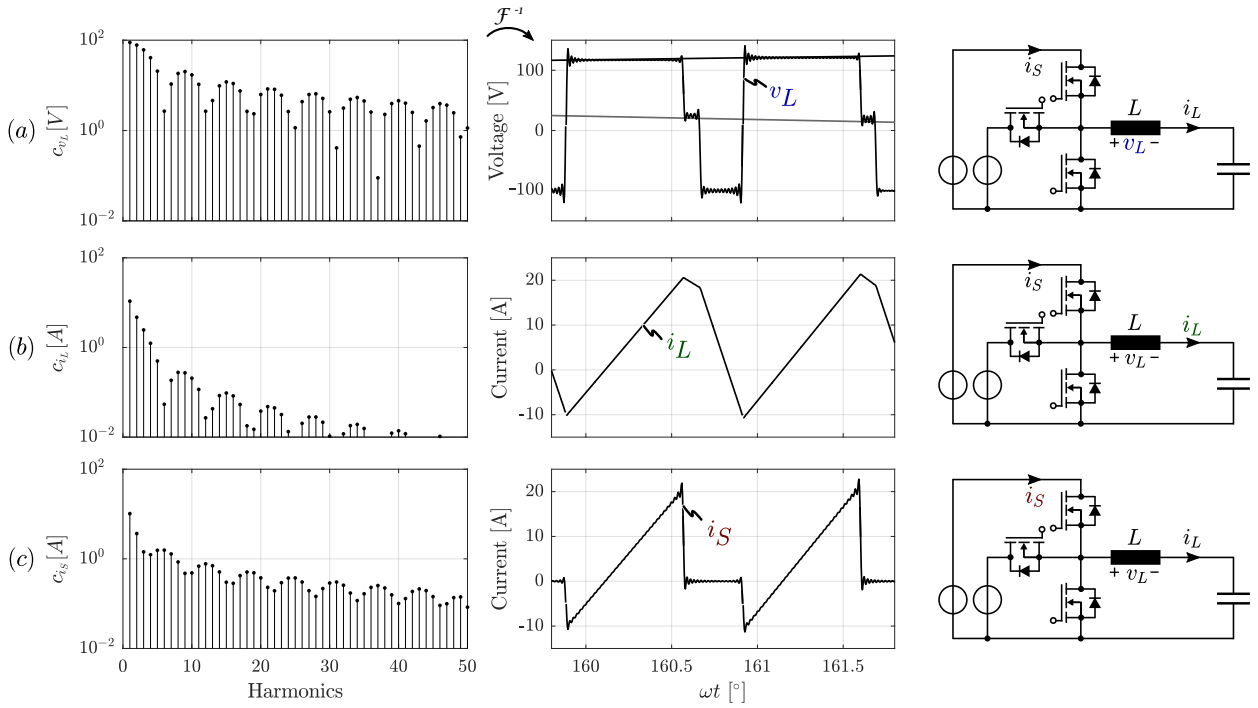

Figure 5.3: Example of Prodrive-Select Rectifier top 3L buck circuit Fourier analysis with (*a*) Inductor voltage Fourier spectrum c_{v_L} and corresponding time-domain restored waveform v_L, (*b*) Inductor current Fourier spectrum c_{i_L} and corresponding time-domain restored waveform i_L, (*c*) Switch discontinuous current Fourier spectrum c_{i_S} and corresponding time-domain restored waveform i_S.

With the inductor current Fourier coefficients obtained, they can be used to give a switching-cycle representation of the waveform as seen in Figure 5.3*b*. The inductor current Fourier coefficients can then be used to calculate the switch current Fourier coefficients. These can be achieved by performing a time-domain multiplication of a windowing function with the inductor current. The windowing function selects only the time interval during which the switch is conducting, and sets the switch current to zero during the remaining time interval. Due to the convolution theorem, the operation can be described as:

$$\mathscr{F}\{h\} = \mathscr{F}\{f \cdot g\} = \mathscr{F}\{f\} * \mathscr{F}\{g\}$$

The resulting Fourier coefficients are used to generate a switching-cycle representation of the switch currents, as seen in Figure 5.3*c*. Further uses of this modelling approach are the derivation of capacitor voltage waveforms. Similar integration equations as in equation 5.3 can be used to generate the capacitor voltage waveform from the capacitor current Fourier coefficients. This can, for instance, be used to verify the peak-to-peak voltage ripple on the DC output capacitor.

5.5. Component Modelling

This section describes the multi-physics modelling of the converter components. The task of these models is to provide an accurate representation of the components performance in terms of losses, heat generation, volume, etc. The accuracy of the complete modelling approach is largely dependent on the accuracy of the employed component models [19].

5.5.1. Inductor Modelling

Electromagnetic inductive component modelling in power converters is a much researched topic in literature [21]. Parameters such as winding or core losses are frequency and waveform dependent. The Fourier modelling framework forms an excellent basis for accurate inductor modelling as the Fourier coefficients can represent the current or flux waveforms in the frequency domain, enabling the calculation of these frequency dependent parameters. For this research an existing inductor design and loss modelling framework, based on the Fourier modelling technique, has been selected. The mathematical basis of the model can be found in [19], [22], [23] and is briefly explained in the following sections.

The inductor modelling, as depicted in Figure 5.1, is a recursive model where x_i symbolizes the i^{th} iteration of an inductor design. This means that for one converter implementation and operating point the model can iterate on different inductor designs satisfying the requirements set in the Basic Analysis step. A design space can be specified in terms of relevant inductor parameters in order to create a performance space of inductor volume versus losses with the subsequent loss and volume models. Various optimization routines for inductive components have been applied in research which can select optimal inductor designs for each converter implementation [19], [22]. This thesis implements a crude thermal model for the wire and core temperature in order to select the smallest possible design which retains acceptable temperatures.

Inductor Design

The inductor design is an important step as it generates the physical inductor parameters required for the analytical calculations of the inductor losses and the practical realization of the inductor. The physical inductor parameters include, but are not limited to, the number of turns, the winding geometry and the air gap. These parameters are selected based on the core type, core size, core material, wire diameter, required inductance etc. Here the design space for the inductor input parameters is specified. This step requires the use of databases for, for instance, core types, core materials or Litz wire specifications.

Reluctance Model

The reluctance model of an inductor is necessary for estimating the core flux density (B) in order to verify inductor core operating conditions specified by manufacturers. Important input parameters include the core and air gap reluctance, as well as, the number of turns and inductor current [19].

Inductor Core Losses

The inductor flux waveforms are related to the inductor current waveforms. Generally speaking the current waveforms in switch-mode power supplies are piece-wise linear of shape due to the nature of the volt-second across the inductors. When trying to estimate the inductor core losses dependent on the flux waveform this poses a problem as the Generalized Steinmetz Equations (GSE), using the Steinmetz parameters k, α and β, are only applicable for sinusoidal flux waveforms. Improvements have been done to the GSE in order to allow calculation of core losses with the Steinmetz parameters for arbitrary flux waveforms, termed the improved Generalized Steinmetz Equations (iGSE) [24]. With the iGSE the core losses can be calculated as:

$$P_{core,V} = \frac{1}{T}\int_0^T k_i \cdot \left|\frac{\mathrm{d}B}{\mathrm{d}t}\right|^{\alpha} \cdot (\Delta B)^{\beta-\alpha}\mathrm{d}t \tag{5.4}$$

Where ΔB is the peak-to-peak flux density and

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi}|\cos\theta|^{\alpha}\cdot 2^{\beta-\alpha}\mathrm{d}\theta} \tag{5.5}$$

Furthermore, the parameters k, α and β are parameters extracted from datasheets provided by the core manufacturers. Further improvements to the core loss modelling is possible by taking DC-bias and relaxation effects into account, termed the i^{2}GSE [25]. This model, however, requires additional parameterization to be performed on the cores, in contrast to the iGSE.

Inductor Winding Losses

Another source of losses in the inductor are the winding losses. The winding losses occur due to the inductor current passing through an inductor winding. It is assumed that the used conductor is a Litz bundle. The resistance in inductor windings increase with frequency due to eddy currents. The origin of the eddy currents can be separated into three different sources. Namely, self-induced eddy currents leading to skin-effect losses P_s, eddy currents originating from an external alternating magnetic field, e.g. the magnetic field from other windings, resulting in external proximity-effect losses $P_{P,e}$ and eddy currents generated in the Litz bundle itself due to an internal magnetic field, leading to internal proximity-effect losses $P_{P,i}$.

The skin effect losses (including DC losses) per unit length of a Litz bundle can be calculated as shown in [26], [22], by:

$$P_{S,L} = n_s \cdot R_{\mathrm{DC,s}} \cdot F_R(f) \cdot \left(\frac{\hat{I}^2}{n_s}\right) \tag{5.6}$$

With $\hat{I}$ being the Fourier amplitude coefficients of the conductor current $i(t)$ as explained in Section 5.4. $R_{DC,s}$ is the per unit length per strand DC resistance calculated as:

$$R_{\mathrm{DC,s}} = \frac{4}{\sigma \pi d_s^2} \tag{5.7}$$

Where σ is the electrical conductivity of the conductor material and d_s the strand diameter of the Litz bundle.

The per unit length proximity-effect losses in a Litz bundle can be calculated as shown in [22], by:

$$\begin{aligned} P_{P,L} &= P_{P,L,e} + P_{P,L,i} \\ &= n_s \cdot R_{\mathrm{DC,s}} \cdot G_R(f) \cdot \left(\hat{H}_e^2 + \frac{\hat{I}^2}{2\pi^2 d_b} \right) \end{aligned} \tag{5.8}$$

Where $\hat{H}_e$ is the peak external magnetic field strength, commonly calculated with the method of mirroring [27], and d_b the Litz bundle diameter.

Inductor Loss Model *Inputs* The inputs to the inductor loss model are the Fourier coefficients of the inductor current, the peak inductor current, the rms inductor current and the inductor specifications, i.e. inductance, wire type, core type, originating from the inductor design. These parameters include Steinmetz parameters, core geometry/type, air gap specification, inductor winding geometry and configuration, etc.

Inductor Loss Model *Outputs* The inductor loss model outputs are the total inductor losses, subdivided into core losses P_c and winding losses P_w. Further outputs can include worst-case peak flux density inside the core in order to verify the core saturation of the inductor design within the converter steady-state operating point.

Inductor Volume Model

The inductor volume is largely determined by the core and corresponding bobbin size. It is assumed that the inductor windings do not add to the inductor boxed volume. In the case that the inductor volume is purely determined by the core and bobbin, the boxed volume of the inductor can be estimated from datasheet geometry parameters of the core and bobbin.

Inductor Thermal Model

An estimation of the inductor's thermal behaviour is necessary in order to be able to select an optimal core size. If multiple core sizes are specified in the design space the optimization routine should select the smallest possible core which has acceptable temperatures. The inductor thermal model is split into two separate models, namely a wire thermal (T_W) model and a core thermal (T_C) model, which can be seen in Figure 5.4.

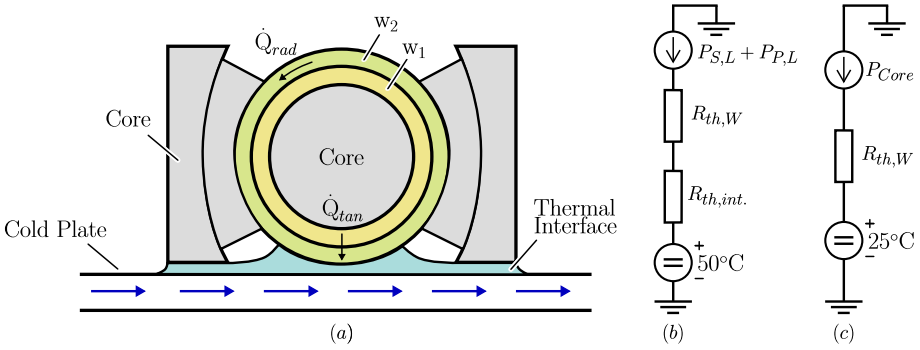

Figure 5.4: (*a*) 2D sketch of the inductor, depicted with core, two winding layers ($w_{1,2}$), thermal interface paste and cold plate. (*b*) Electrical equivalent circuit of the employed 2D thermal model for the inductor wire temperature. It is assumed that there is no radial heat flux $\dot{Q}_{rad} = 0$ and that the all the tangential heat flux is concentrated in the bottom 1/4 of the windings which are in contact with the thermal interface. (*c*) Electrical equivalent circuit of the employed core thermal model. It is assumed that the core equally emanates heat from its entire surface to the ambient air.

The core temperature differential to the ambient air can be estimated by:

$$\Delta T_C = P_{Core} \cdot R_{th,core} \tag{5.9}$$

where $R_{th,core}$ is the core specific thermal resistance which is a datasheet parameter. A smaller core corresponds to a higher thermal resistance.

The wire temperature differential to the cold plate can be estimated by:

$$\Delta T_W = (P_{S,L} + P_{P,L}) \cdot R_{th,W} \tag{5.10}$$

Where the thermal resistance of the windings can be calculated as shown in [28], by:

$$R_{th,W} = \frac{l_w}{4} \cdot \frac{N}{A_{cu} \cdot \lambda_{cu}} \tag{5.11}$$

Here l_w is the average winding turn length, N the number of layers, A_{cu} the copper cross-sectional area and λ_{Cu} the thermal conductivity of copper. This simplification of $R_{th,W}$ assumes all heat flux is distributed equally across 1/4th of the inductors windings and only has a tangential component $\dot{Q}_{tan}$, which is valid when one side of the inductor windings are connected to a cold plate. Furthermore, it is assumed that the windings are pure copper instead of litz bundles with a correction with the fill factor (d_{fill}) of litz bundles as:

$$A_{cu} = \pi \cdot \left(\frac{d_b \cdot d_{fill}}{2} \right)^2 \tag{5.12}$$

5.5.2. Semiconductor Modelling

This section describes the multi-physics modelling of the semiconductors with respect to their electrical and thermal performance [19],[23]. The semiconductors are a crucial part of any converter and contributes significantly, roughly 30-60%, to the total losses. This research focuses on the modelling of MOSFETs and power diodes.

Conduction Losses

The semiconductor conduction losses are a function of their internal parameters and the electrical operating conditions and can be described as:

$$P_{c,sw}^{fet} = \frac{1}{T_{sw}} \int_{T_{sw}} R_{ds,on}(i_{ds}(t), T_j, V_{gs}) \cdot i_{ds}(t)^2 \cdot \mathrm{d}t \tag{5.13}$$

where $R_{ds,on}$ is the MOSFET drain-source on-resistance which depends on the instantaneous drain-source current, the MOSFET junction temperature and the gate-source voltage. As shown in [23], a 2nd-order approximation of $R_{ds,on}$ can be made with respect to the varying parameters by using fitting functions on the datasheet parameters in order to find an analytical, generalized expression for $R_{ds,on}(i_{ds,on}(t), T_j, v_{gs})$.

Equation 5.13 describes the conduction losses during one switching cycle and can be expanded to the entire grid cycle as:

$$P_c^{fet} = \frac{1}{T_{gr}} \int_{T_{gr}} P_{c,sw}^{fet} \cdot \mathrm{d}t \tag{5.14}$$

The conduction losses of a power diode can be described by their forward voltage times the instantaneous diode current as:

$$P_c^{diode} = \frac{1}{T} \int_T v_F(i_d(t), T_j) \cdot i_d(t) \cdot \mathrm{d}t \tag{5.15}$$

The diode forward voltage is a function of the instantaneous diode current and the diode junction temperature. Datasheet fitting for these parameters result in a generalized expression for the forward voltage in order to determine the switching losses. The same grid-cycle averaging operation as equation 5.14 is used when analyzing the converters steady-state behaviour.

Conduction Loss Model Inputs The conduction loss model requires the time-domain semiconductor current waveforms for each switching cycle. These are provided by the Switching Model through Fourier analysis as explained in Section 5.4. These waveforms are needed because of the dependency between drain-source current i_{DS} versus drain-source on-state resistance $R_{DS,on}$ for the MOSFETs and diode current i_d versus forward voltage v_F for the diodes. Consequently, estimating the switching cycle average conduction losses by using the switching cycle rms current diminishes in accuracy as the peak-to-peak ripple increases.

Further inputs are the semiconductor junction temperature and the MOSFET gate-source on-voltage. Both these parameters largely influence the conduction behaviour of the semiconductor as can be seen in Figure 5.5, showing some fitted functions for a state-of-the-art 1200V SiC MOSFET. The gate-source voltage must be specified in the Semiconductor Type selection stage, and should ideally be chosen as high as possible. The junction temperature is an output of the thermal model.

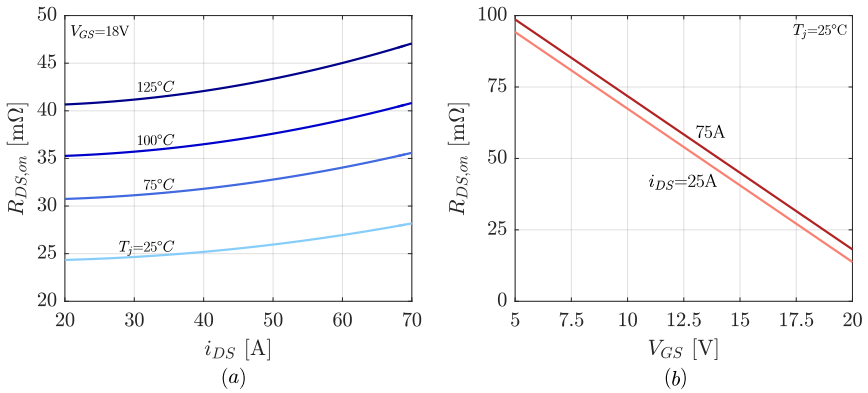

Figure 5.5: Fitted functions for 1200V SiC MOSFET SCTH100N120G2AG [29] for (*a*) drain-source current i_{DS} versus drain-source on-state resistance $R_{DS,on}$ for different junction temperatures T_j and (*b*) gate-source voltage V_{GS} versus drain-source on-state resistance $R_{DS,on}$ for different drain-source currents i_{DS}.

Conduction Loss Model Outputs The outputs of the conduction loss model are the conduction losses for each semiconductor, both the switching-cycle waveform and averaged over switching-cycle and grid-cycle. The averaged losses are used to estimate converter steady-state efficiency, while the switching-cycle losses are used to calculate semiconductor temperature swing.

Switching Losses

The switching losses of the active semiconductors are calculated as:

$$P_{sw}^{fet} = f_{sw} \cdot \left[E_{on}(i_{DS}, T_j, v_{DS}, R_{g,on}) + E_{off}(i_{DS}, T_j, v_{DS}, R_{g,off}) \right] \tag{5.16}$$

Where the parameters E_{on} and E_{off} correspond to the turn-on and turn-off energy and are dependent on the drain-source current i_{DS}, the semiconductor junction temperature T_j, the drain-source voltage v_{DS} and the turn-on or turn-off gate resistance $R_{g,on,off}$. These dependencies can be extracted from manufacturer datasheets and a generalized expression can be found for E_{on} and E_{off}.

Depending on the calculated switching transition, i.e. hard/soft turn-on/turn-off, the total switching losses for a semiconductor for one switching cycle equals a combination of the E_{on}/E_{off} curves. As explained in the following *Zero-Voltage-Switching Modelling* paragraph, the E_{on}/E_{off} curves are adjusted in terms of voltage across and current through the semiconductor in order to accommodate complete and incomplete zero-voltage switching. When a parallel capacitance is added across the MOSFET, the E_{on}/E_{off} curves have to be adjusted further as the switching transient is dramatically changed. As detailed in Chapter 8, for the hardware demonstrator the E_{on} curve has to be increased by 15% and the E_{off} curve decreased by 75% to compensate for a parallel capacitance of 1nF.

Switching Loss Model Inputs The inputs to the model are first of all the switched current i_{DS} and the switched voltage v_{DS}, which are the dominating factors when calculating the switching losses. Figure 5.6 shows fitted functions for the turn-on and turn-off losses for a 1000V SiC MOSFET. Further model inputs are the on- and off-state gate-source voltage $V_{GS,on}/V_{GS,off}$, the external gate resistance $R_{g,on,off}$, and the semiconductor junction temperature. Note that the SiC MOSFETs have negligible temperature dependency, as opposed to traditional Si MOSFETs [30]. The external gate resistance and the gate-source voltage have to be specified in the Semiconductor Type selection stage, while the semiconductor junction temperature is an input from the semiconductor thermal model.

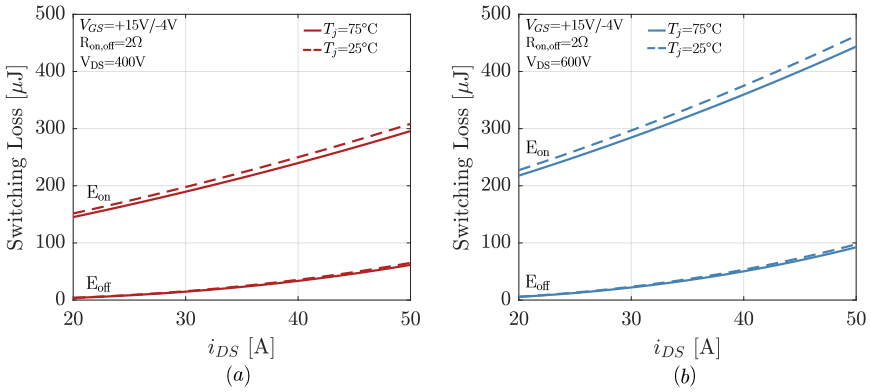

Figure 5.6: Switching loss function fittings for 1000V SiC MOSFET C3M0065100K for different junction temperatures T_j and (*a*) drain-source voltage V_{DS} = 400V and (*b*) drain-source voltage V_{DS} = 600V. The E_{on} and E_{off} curves are compensated to correspond to the intrinsic loss distribution [31]

Switching Loss Model Outputs The outputs of the switching loss model are the total switching losses for each semiconductor, the transient switching cycle waveform, as well as, the average switching-cycle and grid-cycle waveform. The averaged losses are used to estimate converter steady-state efficiency, while the switching cycle losses are used to calculate the semiconductor temperature swing. Furthermore, the breakdown of the switching losses in turn-on and turn-off losses can be used to verify the soft-switching conditions of the converter.

Zero-Voltage-Switching Modelling As explained in Section 2.3, zero-voltage switching of a semiconductor can be achieved by means of a resonant transition between the semiconductor drain-source capacitance C_{DS} and buck inductor L. In a half-bridge implementation as shown in Figure 5.7, the stored inductive energy relocates the stored charge Q_{oss} from one drain-source capacitor to the complementary capacitor. The non-linear capacitance versus voltage behaviour of C_{DS} and the time varying inductor current i_L results in complex calculations when solving for charge equivalence required for complete soft-switching. Linearization of the non-linear system by means of charge-equivalent capacitance ($C_{Q,eq}$) and energy-equivalent capacitance ($C_{E,eq}$) results in an analytically solvable system [15]. These models often make assumptions such as constant inductor current or infinite dead-time, which limit the use when calculating incomplete zero-voltage transitions. Especially the varying inductor current greatly influences the zero-voltage switching transition when small inductance values are used, as large $\frac{\mathrm{d}i}{\mathrm{d}t}$ is expected.

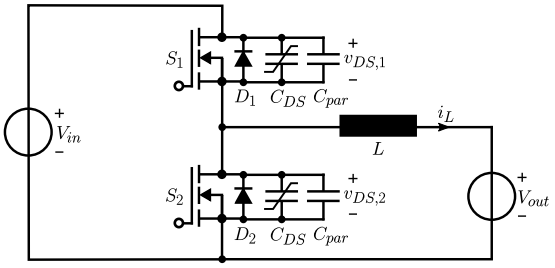

Figure 5.7: Bridge leg implemented with MOSFETs connected to a buck inductor L. The MOSFETs are depicted with package internal drain-source capacitance C_{DS} and externally placed parallel capacitance C_{par}.

Increased accuracy can be achieved when a numerical approach is used to compute the instantaneous charge in both C_{oss} and L. Figure 5.8 shows example waveforms of a complete and incomplete zero-voltage switching transition where varying i_L and C_{oss} are taken into account. The output capacitance C_{oss} of a MOSFET, as commonly specified in datasheets, can be described as:

$$C_{oss} = C_{DS} + C_{GD}$$

The non-linear behaviour of C_{oss} versus drain-source voltage can be seen in Figure 5.8*a*. Further depicted in Figure 5.8*a* is the stored charge Q_{oss}. Figure 5.8*b* depicts a complete zero-voltage switching transition where the instantaneous drain-source voltage $v_{DS,1}(t)$ has decayed to zero before the end of the dead-time. Figure 5.8*c* shows an incomplete zero-voltage switching transition where the large $\frac{\mathrm{d}i}{\mathrm{d}t}$ after t=0 pushes the inductor current to zero before the resonant transition is complete. The semiconductor then turns on at zero current with the remaining drain-source voltage at t=700ns, which can be used for estimating the ZVS losses by the switching-loss model of Section 5.5.2.

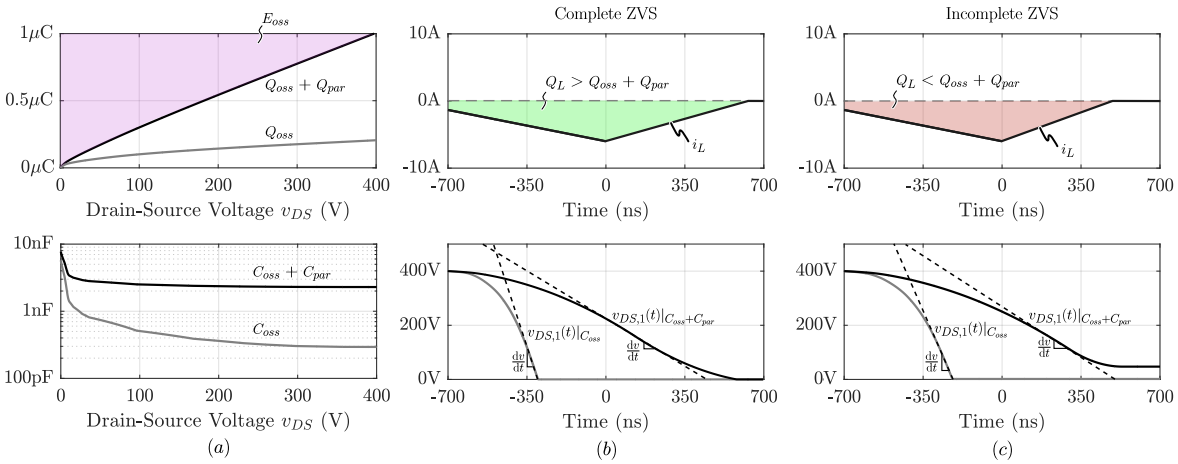

Figure 5.8: (*a*) Non-linear behaviour of the MOSFET drain-source capacitance C_{oss} and related stored charge Q_{oss}, both with and without parallel capacitance C_{par} (assumed constant). (*b*) Complete ZVS transition with numerical calculation taking into account varying i_L and non-linear C_{oss} dependency. (*c*) Incomplete ZVS transition where the inductive energy is insufficient to completely remove all charge from $C_{oss} + C_{par}$. Where t_{dead} = 1400 ns. Gradual inductor current slope variation and back-commutation is ignored in this model.

Furthermore evident from Figure 5.8*b*,*c* is the large difference a parallel capacitance C_{par} makes on the $\frac{\mathrm{d}v}{\mathrm{d}t}$ during the resonant transition. The decreased voltage slope reduces high-frequency EMI emissions and reduces gate driver stress. This does, however, come at the cost of increased required Q_L.

Gate-Drive Losses

Switching at high frequencies attributes to the non-negligible effect of the gate-drive losses, which scale proportional to the switching frequency. The gate-source voltage transient during MOSFET switching is accompanied by the charging or discharging of the gate capacitance. The gate-drive losses can be expressed in terms of the total gate capacitance charge Q_g, the gate-source voltage differential ΔV_{gs} and the switching frequency f_s as:

$$P_{gd} = Q_g \cdot \Delta V_{gs} \cdot \frac{1}{T_{gr}} \int_0^{T_{gr}} f_s \cdot \mathrm{d}t \tag{5.17}$$

Where P_{gd} denotes the grid cycle averaged gate-drive losses.

Semiconductor Thermal Model

The semiconductor thermal model is used to estimate the semiconductor junction temperature, which is dependent on the semiconductor losses and thermal interfacing design. Figure 5.9 shows the proposed semiconductor thermal model for this research. It is assumed the semiconductor is an SMD component placed on a metal core PCB (MCPCB), further interfaced to a cold plate through an aluminum block. This way the heat is extracted from the bottom side of the semiconductor and conducted through the MCPCB and aluminum block to the cold plate. The equivalent circuit shows the various thermal resistances present in the heat conduction path. It is assumed that the cold plate has a constant temperature of 50°C.

Furthermore, it is assumed that each semiconductor is surrounded by a certain area of PCB and aluminum block which is scalable in order to enforce a certain steady-state average temperature. The heat flux is assumed to be distributed uniformly across the PCB copper foil in order to use the 2D thermal model of Figure 5.9*b*.

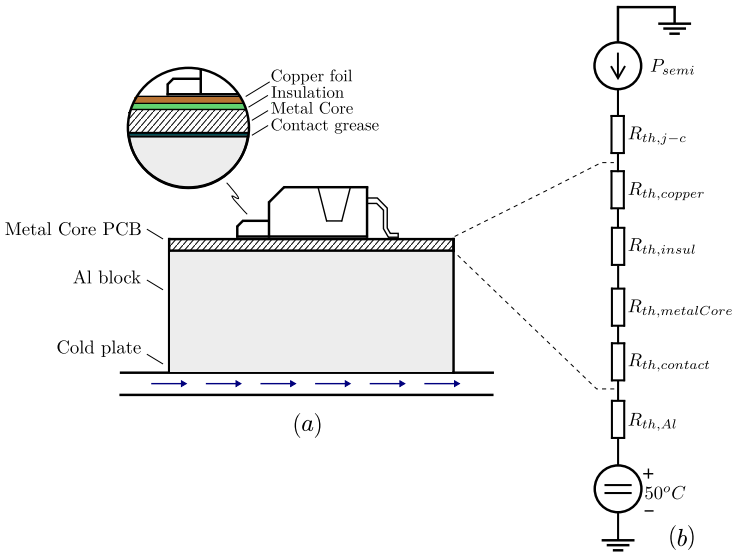

Figure 5.9: (*a*) Semiconductor thermal model to calculate the semiconductor junction temperature T_j and (*b*) corresponding equivalent electrical circuit model.

The thermal resistance of the semiconductor package is dominant in this 2D model. The junction-to-case thermal resistance of the semiconductor $R_{th,j-c}$ can be derived from the datasheet graphs for thermal impedance. Depending on the modelled frequency, e.g. grid cycle frequency or switching frequency, the thermal resistance can be taken as the real part of the thermal impedance at that frequency $R_{th,j-c}(\omega) = \mathrm{Re}(Z_{th,j-c}(\omega))$. The inclusion of the thermal impedance allows increased accuracy when calculating semiconductor thermal swing. Furthermore, it is assumed that the rest of the thermal resistances do not have a frequency dependency.

The remaining thermal resistances have to be calculated. Depending on the thickness (d), area (A) and conductivity (λ) of the material these thermal resistances can be estimated by:

$$R_{th} = \frac{d}{\lambda \cdot A}$$

An iterative method is used for reaching a steady-state semiconductor loss and temperature. An initial guess is given for the semiconductor temperature with which the losses are calculated. The losses are then input to the thermal model, which might result in a different temperature as the initial guess, which results in different losses. The loss and thermal model are iterated until there is negligible temperature differential between iterations.

Furthermore, when a steady-state temperature has been reached, it is verified whether the semiconductor temperature is below the maximum allowed temperature of 80°C. If this is not the case, the aluminium

block and MCPCB are enlarged, effectively decreasing all thermal resistances except $R_{th,j-c}$. This process is repeated until there is enough cooling to satisfy all semiconductor maximum allowed temperature ratings.

Semiconductor Thermal Model *Inputs* The inputs for the semiconductor thermal model are the total semiconductor losses, both averaged and during a switching-cycle, which are generated by the semiconductor loss model. The semiconductor junction-to-case thermal resistance and the maximum semiconductor temperature should be specified in the Semiconductor Type stage. Further specification of the PCB and cooling interface geometry is internal to the model.

Semiconductor Thermal Model *Outputs* The outputs of the semiconductor thermal model are the junction temperatures of all semiconductors, both averaged and during a switching-cycle. Furthermore, the dimensions of the MCPCBs and aluminium blocks are outputs as well.

Semiconductor Volume Model

The volume of the semiconductors is specified as the volume of all components required to operate the semiconductors, e.g. gate drivers, snubbers, or the volume of the MCPCB. This is estimated by the footprint area for the semiconductor and the package height, both derived from the datasheet. A margin of 200% is taken for the gate driving circuit, layout margins and power connections. The volume of the aluminium interfacing block between the MCPCB and the cold plate is taken as wasted space as this interfacing is only a necessity due to the practical implementation and would ideally be left out. The heatsink volume corresponds to the cold plate volume, which is the MCPCB area times the thickness of the cold plate.

5.5.3. EMI Modelling

In order to comply with certain standards regarding high-frequency electromagnetic interference, e.g. CISPR 22 class A/B, EMI filters have to be designed. These filters usually take up a significant amount of space and thus the design and modelling of EMI must be accurate in order to correctly dimension the design. The Fourier modelling approach of Section 5.4 can be used for deriving the common- and differential-mode noise sources of the converter.

Generally, a Line Impedance Stabilization Network (LISN) is used for measuring the conducted DM and CM emissions. The LISN functions as a bi-directional filter, both shielding the converter from noise from the grid and providing a relatively constant impedance for the converter in order to guarantee measurement reproducibility. The modelling approach as stated in [32],[33] is extended to the modelling of the Prodrive-Select Rectifier, the LISN and the test receiver.

Differential-Mode Filter Model

In order to estimate the differential-mode (DM) behaviour of the converter it is necessary to model the rectifier and LISN with an equivalent circuit model. Figure 5.10 depicts the DM equivalent circuit for the Prodrive-Select Rectifier with an arbitrary number of filter stages n_{DM}. The noise source $i_{noise,DM}$ is modelled as an equivalent current source originating from capacitive midpoint M and can be described with the Fourier coefficients as obtained in Section 5.4. The noise current can be seen as the equivalent noise current composed of the high-frequency switch currents i'_x,i'_y and i'_z, as depicted in Figure 3.1. The noise source can be referred to the input side, in front of the IVS, by modelling the time-behaviour of the IVS, i.e. the noise source in phase a is a combination of the currents i'_x, i'_y or i'_z.

An equivalent noise source is obtained for each phase, which are equal to each other when averaged over one grid cycle. Figure 5.10 can then be used as a high-frequency single-phase equivalent circuit.

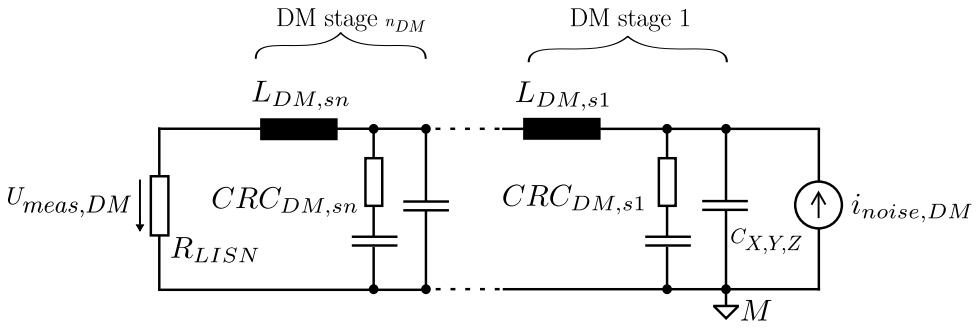

Figure 5.10: High-frequency single-phase differential-mode equivalent circuit.

In order to estimate the required attenuation of the DM filter, a worst-case estimation of the DM emissions is needed. Figure 5.11 depicts the worst-case DM equivalent circuit, where it is assumed that all the high-frequency noise current is fed directly into the LISN measuring resistor R_{LISN}. This circuit neglects the influence of C_{XYZ} and assumes they are placed before the IVS. Attached to the LISN is an EMC test receiver which performs a Quasi-Peak (QP) measurement to measure the annoyance of a signal [32]. The modelling of the test receiver is a much discussed topic in literature [34], [35], and is necessary to get a complete model of the EMI measurement setup. An assumption can be made that the total high-frequency rms noise current is an adequate estimation of the QP detection voltage at the EMI test receiver [33].

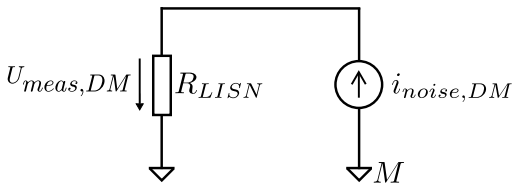

Figure 5.11: High-frequency worst-case differential-mode equivalent circuit.

Figure 5.12 depicts the calculated noise voltage $U_{meas,DM}$ across R_{LISN} in dBμV for an interleaved Prodrive-Select Rectifier with an effective switching frequency of 144kHz. The specifications according to CISPR 22 for the class A EMC limits starts at 150kHz, meaning the first and assumed highest quasi-peak detection point is at the first multiple of the effective switching frequency above 150kHz, called the design frequency f_D. At the design frequency the total rms noise voltage of higher harmonics is bundled and results in the estimated differential-mode quasi-peak measurement $U_{meas,DM,QP}$.

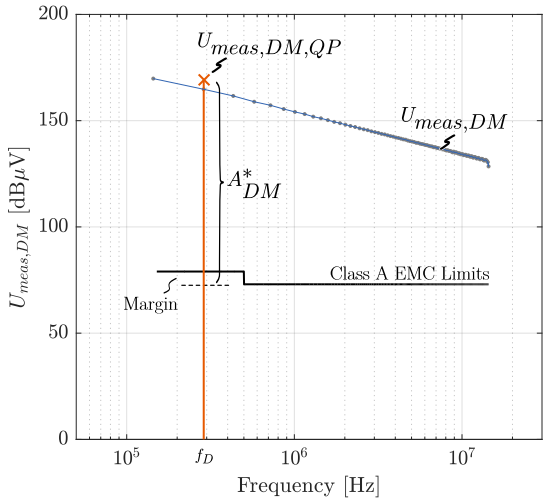

Figure 5.12: Modelled differential-mode quasi-peak detector worst-case measurement for an interleaved 72kHz Prodrive-Select Rectifier.

The required attenuation A^*_{DM} can be found by:

$$A^*_{DM} = U_{meas,DM,QP} - \text{Limit}_{DM} + \text{Margin}_{DM}$$

Differential-Mode Filter *Design* The attenuation at the design frequency is the input for the design of the differential-mode filter. Depending on the required attenuation and nominal filter current the optimum filter topology has been selected as a two-stage *CLC* filter [36]. An high-frequency approximation of the DM filter combined with a volume minimization function results in an analytical equation for the optimal capacitance value for a two-stage CLC filter with equal component values [36], [37].

$$C_{DM} = \sqrt[3]{\frac{k_{L,powder} \cdot I^2_{max} \cdot 10^{A^*_{DM}/20}}{k_{C,foil,X2} \cdot v^2_{max} \cdot R_{LISN} \cdot \omega^2_D}} \tag{5.18}$$

Where $k_{C,foil,X2} = 45 \times 10^{-6}$ $[m^3/FV^2]$ and $k_{L,powder} = 3.95 \times 10^{-3}$ $[m^3/HA^2]$ are volumetric coefficients for X2 foil capacitors and powder core inductors respectively [37]. X2 rated foil capacitors have to be used for the differential-mode filter design because of their safety rating. V_{max} and I_{max} are the maximum voltage and current rating of the filter component and ω_D the design frequency in rad/sec. It should be noted that in terms of control stability equal attenuation in both filter stages is not ideal and possibilities for improvement lie in the redistribution of filter stage attenuation, which goes at the cost of volume optimization [5].

Further limitations on the DM filter are presented when the system power factor and node voltage fluctuations are considered. The DM capacitance should be large enough to limit the peak-to-peak voltage ripple on nodes X, Y and Z and small enough to have acceptable power factor at low power operation.

The maximum total DM capacitance can be calculated by:

$$C_{DM,tot} = \frac{\sqrt{\left(\frac{P}{\lambda}\right)^2 - P^2}}{\omega_G \cdot |V|^2} \tag{5.19}$$

Where P is the active power, λ the required power factor, ω_G the grid frequency in rad/sec and $|V|$ the amplitude of the grid voltage phasor. These limitations result in a per stage DM capacitance design freedom with a minimum and a maximum. If the filter components calculated with equations 5.18 result in a capacitance value outside these limits, the maximum or minimum value of C_{DM} should be taken. With a fixed C_{DM} the value for L_{DM} can be estimated through a high-frequency approximation of a two-stage CLC filter [36]:

$$L_{DM} = \frac{10^{A^*_{DM}/20}}{\omega_D^3 \cdot C_{DM}^2 \cdot R_{LISN}} \tag{5.20}$$

Differential-Mode Filter *Volume Model* The volume of the differential mode filter components can be estimated by their peak stored energy and volumetric coefficients derived for component specific implementations [37], [38]. Assuming the stored energy is in direct relation to the volume:

$$\begin{aligned} V_{L_{DM}} &= k_{L,powder} \cdot L_{DM} \cdot I_{rms}^2 \\ V_{C_{DM}} &= k_{C,foil,X2} \cdot C_{DM} \cdot V_{rms}^2 \end{aligned} \tag{5.21}$$

Note that this is an estimate of the component volumes and not of the complete filter. For an estimate of the complete filter volume it is necessary to take a margin into account for certain implementation parameters, e.g. mounting, connections, PCB, airflow. A margin of 200% or 2.0 is taken in order to compensate for these effects in the volume model as the sum of the individual components amounts to roughly 50% of the total filter volume.

Differential-Mode Filter *Loss Model* The losses in the differential-mode filter are dominated by the inductor LF AC losses and the capacitor ESR losses. For the inductor LF AC losses a model is used which iterates on a set of toroidal core shapes and fits them with solid copper windings in order to achieve the required inductance. The lowest volume inductor design is chosen and the length of the windings determine the winding LF AC resistance. The inductor LF AC losses are then estimated by:

$$P_{L,i,DM} = 3 \cdot R_{L,i,DM} \cdot i_{G,1ph,rms}^2 \tag{5.22}$$

The high-frequency capacitive current in the DM capacitors can result in significant losses as the internal ESR of the capacitors dissipate the rms capacitive current, especially the first stage DM capacitors should handle up to 20Arms. For the loss model it is assumed that the first stage DM capacitors are implemented with Ceralink LP series capacitors. The capacitive losses can then be estimated as:

$$P_{C,i,DM}(f) = 3 \cdot R_{ESR}(T_c, V_{DC}, f) \cdot i_{DM,rms}^2(f) \tag{5.23}$$

Where R_{ESR} is dependent on the case temperature (T_c), the capacitor DC offset voltage (V_{DC}) and the frequency of the noise current (f). These dependencies can be fitted from datasheet parameters and graphs.

Common-Mode Filter Model

In order to estimate the common-mode (CM) behaviour of the converter it is necessary to model the rectifier and LISN with an equivalent circuit model. Figure 5.13 depicts the common-mode equivalent circuit for the Prodrive-Select Rectifier with an arbitrary number of filter stages n_{CM}. The common-mode noise source originates from the pulsed voltages on switch node v_{pM} and v_{nM} and can be described as:

$$v_{CM} = \frac{\sum_{n=1}^{n_i} v_{pG,i} + \sum_{n=1}^{n_i} v_{nG,i}}{2 \cdot n_i} \tag{5.24}$$

Where n_i is the amount of interleaved output stages of the rectifier and $v_{pG,i}\,/\,v_{nG,i}$ the switch-node voltage to G for output stage i, where G denotes the PE connection of the AC source. The CM driving voltage v_{CM} is capacitively coupled to G through a heatsink capacitance C_{HS}, in this case denoting a lumped capacitor of all parasitic capacitances of the semiconductors to G.

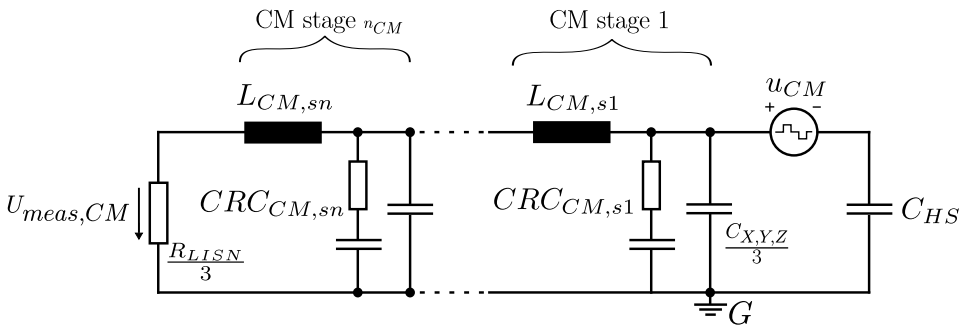

Figure 5.13: High-frequency common-Mode equivalent circuit with arbitrary number of filter stages n_{CM}.

In order to estimate the required attenuation of the CM filter, a worst-case estimation of the CM emissions is needed. Figure 5.14 depicts the worst-case CM equivalent circuit, where it is assumed that all the high-frequency noise voltage manifests across the LISN measuring resistor $R_{LISN}/3$. A worst-case approximation for C_{HS} is an infinite capacitance as this creates a short to G, not contributing any attenuation.

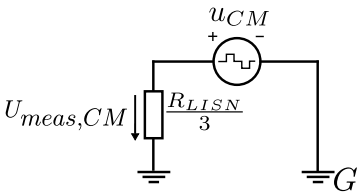

Figure 5.14: High-frequency worst-case common-mode equivalent circuit.

Figure 5.15 depicts the calculated noise voltage $U_{meas,CM}$ across $R_{LISN}/3$ in dBμV for an interleaved Prodrive-Select Rectifier with an effective switching frequency of 144kHz. The specifications according to CISPR 22 for the class A EMC limits starts at 150kHz, meaning the first and assumed highest quasi-peak detection point is at the first multiple of the effective switching frequency above 150kHz, called the design frequency f_D. At the design frequency the total rms noise voltage of higher harmonics is bundled and results in the estimated common-mode quasi-peak measurement $U_{meas,CM,QP}$.

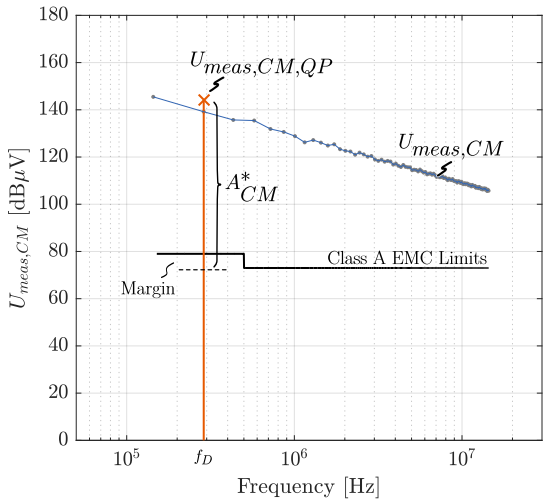

Figure 5.15: Modelled common-mode quasi-peak detector worst-case measurement for an interleaved 72kHz Prodrive-Select Rectifier.

The required attenuation A^*_{CM} can be found by:

$$A^*_{CM} = U_{meas,CM,QP} - \text{Limit}_{CM} + \text{Margin}_{CM}$$

Common-Mode Filter *Design* The common-mode input filter is largely restricted in terms of total capacitance from one of the phases to PE as the capacitance is in direct relation to the maximum allowed earth leakage current $I_{PE,rms,max}$. The 50 Hz AC phase voltage results in a capacitive current to PE. In a balanced three-phase system these currents cancel and do not contribute to the leakage current. However, the leakage current rating has to also be met when one phase is lost. This means an equation can be formulated for the total, per phase, input common-mode capacitance as [37]:

$$C_{CM,i,tot} = \frac{I_{PE,rms,max}}{1.1 \cdot V_{G,1ph,rms} \cdot 2 \cdot \pi \cdot f_G} \tag{5.25}$$

Where f_G is the grid frequency and $V_{G,1ph,rms}$ the single-phase rms voltage. The earth leakage current is typically limited to 3.5mA. However, a margin of 1.5mA is provided for other sources of earth leakage current not originating from the common-mode filter such as input protection varistors or output capacitively coupled common-mode current. This results in a per phase allowed common-mode capacitance of 25nF. Furthermore, the capacitors attached from phase to PE have to fulfill the Y1 safety rating. The optimal filter topology for the common-mode input filter is determined as a two-stage *LCLC* filter [36]. With a fixed common-mode capacitance the required common-mode inductance can be calculated as:

$$L_{CM} = \sqrt{\frac{10^{A^*_{CM}/20}}{\omega_D^4 \cdot C_{CM}^2}} \tag{5.26}$$

Common-Mode Filter *Volume Model* The volume of the common-mode filter capacitors can be estimated by their peak stored energy and volumetric coefficients derived for component specific implementations [37], [38]. Assuming the stored energy is in direct relation to the volume:

$$V_{C_{CM}} = k_{C,foil,Y1} \cdot C_{CM} \cdot V_{rms}^2 \tag{5.27}$$

Where $k_{C,foil,Y1} = 3 \times 10^{-3}$ $[m^3/FV^2]$ is the volumetric coefficient for Y1 rated foil capacitors. The nanocrystalline VITROPERM500F is modelled as the core material because of the high permeability and flux density saturation point, allowing high inductance in relatively low volume. The volume of the common-mode filter inductors can be estimated through their required frequency dependent impedance, current rating and core material permeability [37]. The area product $A_e A_w$ can be calculated as:

$$A_e A_w = 10^{[\log[Z_{CM}(f_D)] - 2{,}243 - 2 \cdot \log(I_{rms})] / [0{,}181 \cdot \log(|\mu| \cdot f_D \cdot 10^{-5})]} \tag{5.28}$$

where the area product is calculated through an empirically derived function and related to the inductor boxed volume through a set of practical inductor designs.

Common-Mode Filter *Loss Model* The dominant factor in the input common-mode filter losses are the CM choke 50Hz AC losses, originating from the wire LF AC resistance and the phase rms current. A fitting was made for three-phase CM chokes with respect to their inductance and corresponding DC resistance. The common-mode filter losses are then estimated by:

$$P_{L,i,CM} = 3 \cdot R_{L_{i,CM}} \cdot i_{G,1ph,rms}^2 \tag{5.29}$$

5.6. Total Volume and Losses

The main outputs of the individual component models are the losses and volumes. The component models for capacitors, inductors, semiconductors and EMC filters represent the most impactful subsystems in terms of converter efficiency and power density and can therefore serve as an approximation of total converter losses and volume. Converter subsystems generating losses that have previously been neglected in this approach are the auxiliary electronics (low-power voltage rails), the control electronics (FPGA, microcontroller) and measurement and protection circuits. In order to increase the accuracy of the model an approximation of these losses, termed the auxiliary losses P_{aux}, can be made in the order of 15W and added to the summation of the total converter losses. The converter system efficiency can then be estimated as:

$$\eta_{\text{sys}} = \frac{P_{\text{i}} - P_{\text{loss}}}{P_{\text{i}}} \cdot 100\%$$

A similar scenario occurs when estimating the converter volume from the summation of the individual component volumes. When looking at practical implementations of power converters there are certain margins which have to be taken into account when deriving the total converter volume. These margin exist due to variables such as physical mounting restrictions, electrical isolation restriction, PCB and interconnection volume, etc. Component model specific margins have been implemented in the component volume models derived from the physical implementation of the Prodrive-Select Rectifier prototype as discussed in Chapter 8. Aside from this, a margin of +20% or 1.2 is taken for the total converter volume in order to account for the previously described volume mismatch. The converter system power density can then be estimated as:

$$\rho_{\text{sys}} = \frac{P_{\text{o}}}{V_{\text{box}}}$$

5.7. Summary

This chapter summarizes the modelling of the main converter components as proposed in this work. Firstly, the modelling approach is described in detail where the converter model is separated into the basic converter analysis, Fourier analysis, component models and total converter models. This mathematical model can be further utilized for rapid virtual prototyping as discussed in Chapter 6.

The Basic analysis and Fourier analysis are briefly mentioned and substantiated in a mathematical formulation. The component modelling is elaborated on in more detail. The main converter component models are the inductor model, the semiconductor model and the CM and DM EMI model. For each component the relevant parameters are described, such as the inductor core and winding losses, the semiconductor switching and conduction losses or the EMI volume and losses. Lastly, all the component models are combined in order to map the converter implementation onto the performance space. For this work the adopted performance space is total converter power density and efficiency. Additional performance spaces could, for instance, include total converter cost but these are excluded from this research.

6

Design Optimization

6.1. Introduction

This chapter outlines the design optimization of the Prodrive-Select Rectifier. The proposed modelling techniques of Chapter 5 are utilized to generate the converter performance in terms of component losses and volumes. A design space is specified from within one or more optimal designs are expected to emerge. Firstly, certain relevant parameter dependencies are highlighted with the goal of proving the strength of the modelling technique. Furthermore, these dependencies highlight the different design approaches possible within the considered design space of the Prodrive-Select Rectifier.

Secondly, the design space is completely mapped onto the performance space by brute force calculation. This research does not employ any optimization routines in order to narrow the design space, e.g. as applied in [39]. Brute force can be applied as the complete calculation of one implementation from the design space takes approximately 45s-120s, meaning the entire design space could be evaluated in approximately 10-20 hours. Further data manipulation results in a set of Pareto-optimal designs called the Pareto-trajectory. This power density versus efficiency trajectory forms the design vector from which an optimal design is selected depending on the weighting factor of respective performance parameters.

6.2. Methodology

As explained in chapters 1 and 2, and summarized in the requirements Table 1.1, an 11kW three-phase buck-type PFC rectifier is to be designed based on the Prodrive-Select Rectifier topology. The performance metrics of importance are the converter's efficiency and power density. Based on these requirements a design space is specified for the optimization as seen in Table 6.1. It is assumed that the converter system is connected to a standard European grid with a frequency of 50Hz. Furthermore, the nominal output voltage is specified at 400V, with a maximum, continuous output power of 11kW. Besides power factor and EMI compliance this leaves 3 global design parameters, namely the switching frequency, the buck inductance and the number of interleaved buck stages. These three global parameters are selected as variables as they have the largest influence on the performance space and the range is chosen in order to provide a design space within which an optimum is expected. The switching frequency design vector is chosen as:

$$f_{sw} \in \{24, 30, 36, 42, 48, 54, 60, 66, 72, 78, 84, 90, 96, 102, 114, 126, 144, 200, 250, 300\}[\text{kHz}]$$

The inductance design vector is chosen as:

$$L_{P,N} \in \{10, 12.5, 15, 17.5, 20, 25, 30, 40, 50, 60, 70, 80, 90, 100, 125, 150, 175, 200, 225, 250, 300\}[\mu\text{H}]$$

The interleaving vector is chosen as:

$$n_i \in \{1, 2, 3\}$$

Furthermore, the carrier wave is selected as the sawtooth carrier (see Section 3.2.2) as the design space envelopes both hard- and soft-switched variants of the Prodrive-Select Rectifier. The phase shift ϕ_k of the interleaved stages can be described as:

$$\phi_k = \phi_1 + k \cdot 2 \cdot \pi / n_i \qquad \text{with} \quad k \in \{1, 2, .., n_i\}$$

Where k is the stage number and n_i the number of interleaved stages. Further phase shift between top and bottom buck circuits is also possible. This phase shift is, however, fixed to zero as it does not provide any benefits in terms of conduction or switching losses, as the buck circuits are decoupled, and is disadvantageous with respect to the CM noise voltage.

Table 6.1: Prodrive-Select Rectifier optimization global design space for 11kW implementation.

Description	**Parameter**	**Value**	**Unit**
Single phase rms voltage	$v_{G,1ph,rms}$	230	V
Single phase peak voltage	$v_{G,1ph,ampl}$	325	V
Mains frequency	f_G	50	Hz
Output voltage	v_{PN}	300-450	V
Nominal output voltage	$v_{PN,nom}$	400	V
Output power	P_o	11	kW
Switching frequency	f_{sw}	24-300	kHz
Buck inductance	L_P / L_N	10-300	μH
Interleaved buck stages	n_i	1-3	-
Carrier Wave	-	Sawtooth	-
Power factor at full power	$\lambda_{100\%}$	0.99	-
Power factor at 20% power	$\lambda_{20\%}$	0.9	-
Earth Leakage Current	$i_{PE,leak}$	2.5	mA
EMI compliance	-	Class A	-

Besides global design parameters, there are also component specific design parameters such as semiconductor selection, inductor core geometry, inductor wire selection, etc. termed component design space which can be found in Table 6.2. This table specifies a set of design variables in terms of semiconductor choices and inductor core sizes. Other design parameters such as inductor wire type, core material or core geometry are fixed parameters in order to reduce the size of the component design space. For the same reason the MOSFET choices are limited purely to SiC MOSFETs. The two local design variables are thus semiconductor choice and inductor core size which are chosen because of their large influence on respectively converter efficiency and volume. The PQ core geometry is chosen due to the availability of a large range of core sizes and in order to limit the design space to one core geometry. The ferrite core material N95 is chosen due to the electrical parameters of the buck inductors (DC offset, large B swing, low $\hat{B}$) and the switching frequency operating range as specified in the global design space. Litz wire is chosen as the inductor wire type because of the expected increased efficiency due to the reduction of skin effect losses at the design switching frequency starting at 24kHz.

In terms of heatsinking, the approach of Section 5.5.2 is used. This design is dependent on the converter system layout, which is predetermined to correspond to the converter layout of Chapter 8. This way the accuracy of the volume model is expected to be higher compared to non-specific layout designs where the heatsink volume is purely determined by the converter losses. The heatsink design and volume model is scaled both with MCPCB area and inductor core size. Furthermore, the heatsink volume is iteratively incremented in order to reach the same steady-state junction temperature for all the semiconductors for all the design implementations.

Table 6.2: Prodrive-Select optimization component design space.

Component	**Selections**	**Note**
LF Semiconductors	DSP25-12AT	1200V Si Diode
	SCTH100N120G2AG	1200V SiC MOSFET
HF Semiconductors	SCTH100N120G2AG	1200V SiC MOSFET
	SCTH90N65G2V7	650V SiC MOSFET
	C3D10065E	650V SiC Diode
	C5D50065D	650V SiC Diode
Magnetics	$\in$ {PQ50/50, PQ60/42, PQ60/52, PQ65/44, PQ65/54, PM74/59, PM87/70, PM114/93 }	Core sizes
	N95	Core material
	Litz Wire	Wire type
	$\in$ { 0.05, 0.071, 0.1}[mm]	Strand diameter
Heatsink	MCPCB + Coldplate (50^oC)	Scalable Design
Input EMI Filter	CM: *LCLC* filter	Automated Design (sec. 5.5.3)
	DM: *CLC* filter	Automated Design (sec. 5.5.3)
Output EMI Filter	CM: *LC* filter	Fixed Design
	DM: *LC* filter	Fixed Design
	Bulk Capacitance	Fixed Choice

The design of the buck inductors, and especially the choice of core size, dominate the converters achievable power density. An automated inductor design model is implemented as described in Section 5.5.1, where the smallest core size is selected in combination with the lowest losses for a design which results in acceptable wire and core temperatures. The increase of power density resulting from smaller core sizes greatly outweighs the increase in efficiency with larger cores, justifying this core selection routine.

An automated DM input filter design is employed which calculates the lowest volume DM filter as specified in Section 5.5.3. Furthermore described in Section 5.5.3 is the automated CM filter design that calculates the component values needed for reaching the required CM attenuation. The output CM/DM filter is chosen as a fixed design which meets the performance requirement for the entire design space. Possible improvements to the output EMI filter optimization are to apply similar automated design approaches as the input EMI filters in order to optimize the filter design for each design implementation.

Now that a global and a local design space has been specified, the developed virtual prototyping routine of Chapter 5 can be configured to calculate the expected efficiency and volume for each design configuration. Since no optimization routine is implemented, each global design parameter iteration has to be brute force calculated. The calculation time of one design iteration varies greatly depending on the grid cycle points, switching cycle points, Fourier harmonics and global design parameters. With the following settings an execution time between 50s-150s is achieved with relative tolerance in the calculated efficiency of 0.02% as compared to a high accuracy calculation.

- Grid Cycle Points = 150
- Switching Cycle Points = 150
- Fourier Harmonics = 75

With an average calculation-speed of 36 iterations per hour, a reasonable performance space is calculated within approximately 24 hours. The design space then envelopes two completely different design extremes in terms of global design variables, namely a hard-switching high-inductance design with high efficiency and low power density and a soft-switching low-inductance design with lower efficiency and higher power density. Furthermore, the design space includes all the possible designs in between these extremes, allowing an objective comparison of the global and local design variables.

6.3. Optimization Results

The virtual prototyping routine is run for the global and local design space specified in Section 6.2. Figure 6.1 shows the Pareto-front for various iterations of the global design space, namely interleaved variants $n_i = 1,2,3$ and different HF semiconductor choices. Evident is that the non-interleaved variant (Figure 6.1*a*) allows for the highest possible power density, as there are only two inductors present in the design. The non-interleaved designs, however, perform worst in terms of efficiency, as the full load power is delivered by one HF buck circuit. The twice interleaved design variants (Figure 6.1*c*) perform best in terms of efficiency as three HF buck circuits share the load power, but pay with decreased power density. The once interleaved designs (Figure 6.1*b*) perform well in both categories and $n_i = 2$ is selected as the preferred amount of interleaved output stages.

Paralleling of the HF semiconductors is not taken into account in this work because of the large increase in expected computation time. The impact that paralleling would have on the results is a reduction of power density due to increased semiconductor area and increased efficiency due to parallel conduction paths. This could potentially result in different Pareto-front trajectories where, for instance, the non-interleaved designs perform best.

When investigating the Pareto-front for the interleaved Prodrive-Select Rectifier one can observe an increase in efficiency when the SCTH90N65G2V7 semiconductor is used for the HF switches. This is to be expected as this semiconductor has lower $R_{DS,on}$, as well as, lower turn-on and turn-off losses. The Pareto-trajectory can be described as a line from low power density - high efficiency (I) to high power density - lower efficiency (II). The Pareto-optimal design parameters result in a knee-point on the right side of the Pareto-trajectory (II), after which there is a sharp decrease in both efficiency and power density.

The designs centered around I in Figure 6.1 result from a low switching frequency (24-36kHz) and a high inductance (200-300μH). This point is expected to have the highest efficiency as the low switching frequency results in relatively low switching losses, while the high inductance results in hard-switching and low rms currents. However, a disadvantage of this design combination is the low power density, resulting from the large required core size in order to obtain the inductance value. This design direction has for instance been taken in the interleaved Swiss Rectifier of [11].

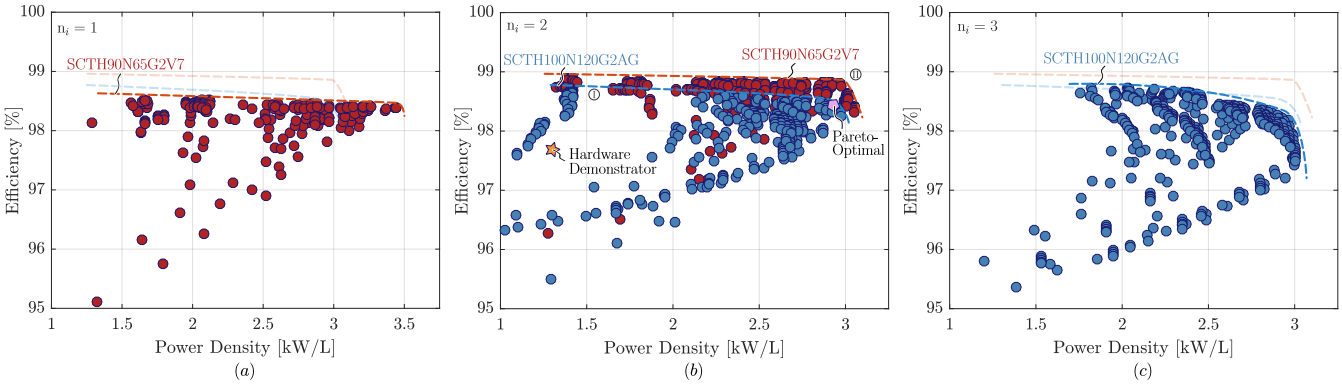

Figure 6.1: Efficiency vs. power density Pareto-front for Prodrive-Select Rectifier with global design parameters as specified in Table 6.1. (*a*) Non-interleaved n_i=1 implementation, (*b*) once-interleaved n_i=2 implementation, (*c*) twice-interleaved n_i=3 implementation. The Pareto-trajectory is shown for implementations with two different HF semiconductors, namely the SCTH100N120G2AG and the SCTH90N65G2V7.

The designs centered around II in Figure 6.1 correspond to implementations with relatively high switching frequency (54-84kHz) and small inductors (15-60μH). These designs have the best performance in terms of power density due to the small inductor core size. A drop in efficiency is to be expected as the switching losses increase proportional to the switching frequency and the decreased inductance value results in larger rms currents. However, the decreased inductance produces large current ripple which ensures partial or complete zero-voltage switching of switches s_{xp} and S_{nz} (see Section 2.3), which consequently allows for an acceptable efficiency at low inductance values.

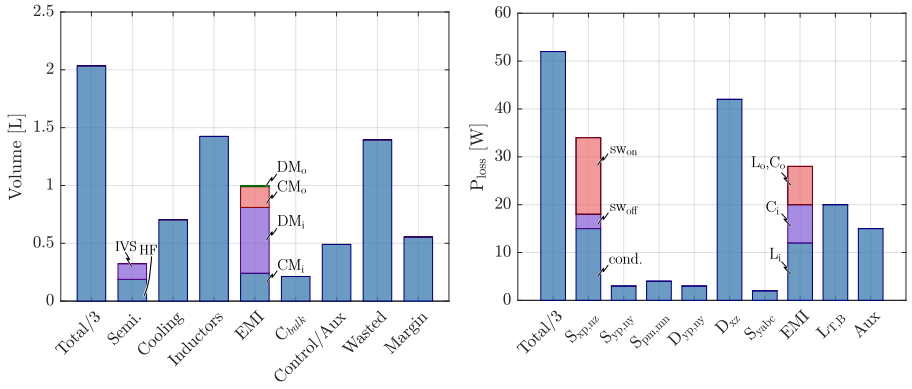

Figure 6.2: Volume and loss breakdown of Prodrive-Select Rectifier (η = 98.6%, ρ = 1.80kW/L) with n_i = 2, $L_{P,N}$ = {200μH, PQ74/59}, f_{sw} = 24kHz, LF = {Passive: DSP25-12AT, Bidir.: SCTH100N120G2AG}, HF = {SCTH100N120G2AG, C5D50065D}.

The benefit of designs around II compared to designs around I is best illustrated through Figures 6.2 and 6.3. Figure 6.2 depicts the volume and loss breakdown for a design around I, while Figure 6.3 shows a design around II. Evident is the large difference in inductor volume and the resulting difference in total converter volume. An increase of nearly a liter and a decrease of power density by more than 1kW/L is observed. In terms of losses an increase of total losses by ≈20W can be observed in Figure 6.3 with respect to Figure 6.2, completely originating from increased semiconductor losses. The HF semiconductor losses of the hard-switched variant of Figure 6.2 are dominated by the turn-on and conduction losses of switches $S_{xp,nz}$. The soft-switched variant of Figure 6.3 results in negligible turn-on losses, while the conduction and turn-off losses are increased for all HF switches. The increase in losses amounts to a drop in efficiency of 0.2%.

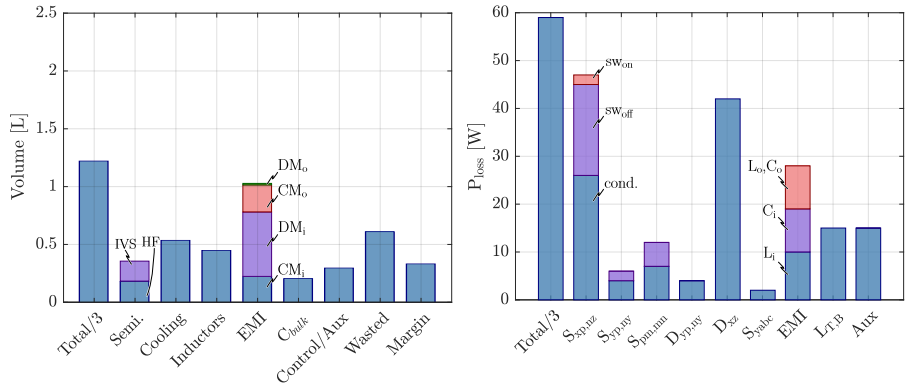

Figure 6.3: Volume and loss breakdown of Prodrive-Select Rectifier (η = 98.4%, ρ = 2.90kW/L) with n_i = 2, $L_{P,N}$ = {17.5μH, PQ50/50}, f_{sw} = 72kHz, LF = {Passive: DSP25-12AT, Bidir.: SCTH100N120G2AG}, HF = {SCTH100N120G2AG, C5D50065D}.

The Pareto-optimal trajectory of SCTH90N65G2V7 based designs from Figure 6.1 does not exhibit the same downward slope as the SCTH100N120G2AG based designs. This can be attributed to the fact that the relative percentage of HF semiconductor losses compared to the total losses is lower in the case of the more efficient SCTH90N65G2V7 designs, meaning a percentage-wise change similar to the SCTH100N120G2AG designs in the HF semiconductor losses does not produce nearly as much difference in the converter efficiency.

Furthermore, it should be noted that a large contributor to the total losses are the D_{xz} losses, signifying the IVS passive rectifier diode losses. These losses are irrespective of the global design parameter variation and are thus a bottleneck when trying to achieve converter efficiencies above 99%. A reduction of

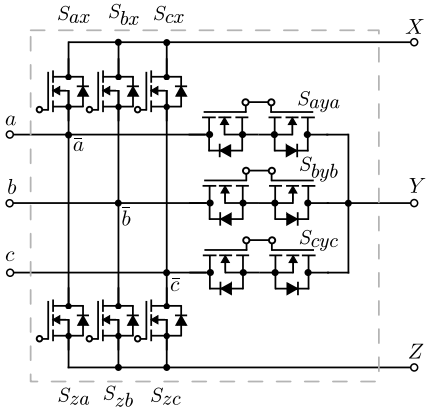

Figure 6.4: Input Voltage Selector (IVS) implemented with synchronous rectification switches.

the D_{xz} losses by ≈20W is possible when synchronous rectification is implemented with SCTH100N120G2AG SiC MOSFETs, as illustrated in Figure 6.4. This does, however, come paired with increased complexity and cost of the converter and is thus not further investigated.

6.3.1. Pareto-Optimal Design

A subset of global design parameters can be identified which result in optimal converter implementations according to the Pareto-front comparison of Figure 6.1, corresponding to location II. A more dense mesh of the performance space is evaluated around this point in order to find the optimal design implementation. Figure 6.5 shows the performance space for an interleaved Prodrive-Select Rectifier with a reduced design space of:

$f_{sw} \in \{60, 62, 64, 66, 68, 70, 72\}$ [kHz]

$L_{P,N} \in \{12.5, 15, 17.5, 20, 25, 30, 40, 50, 60, 70, 80\}$ [μH]

HF Semiconductor: {SCTH100N120G2AG, SCTH90N65G2V7}

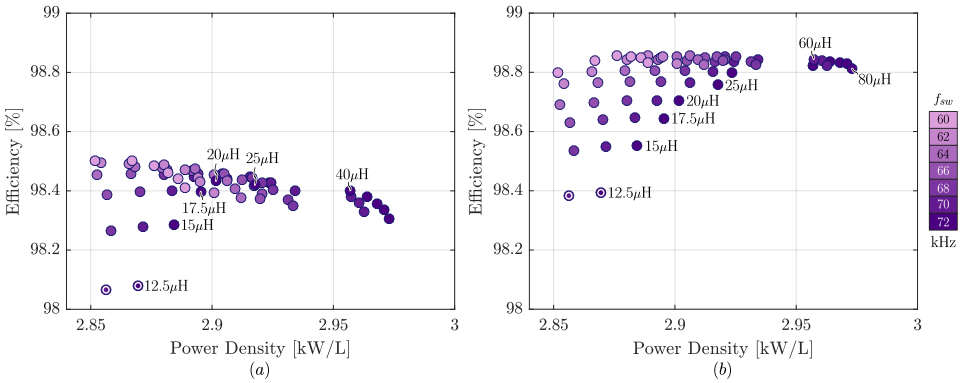

Figure 6.5: Power density vs. efficiency Pareto-front for interleaved Prodrive-Select Rectifier with increased detail around Pareto-optimal global design parameters as shown in Figure 6.1 for HF semiconductors (*a*) SCTH100N120G2AG and (*b*) SCTH90N65G2V7. White circles denote a design which achieves complete ZVS.

These global design parameters translate into the best performance in terms of power density and efficiency because they result in usage of the smallest core size (PQ50/50), while also limiting the semiconductor losses and requiring relatively little attenuation due to the effective switching frequency ($f_{sw,eff} = 2 \times f_{sw}$) being below the 150kHz class A measuring frequency. A switching frequency of 72kHz is selected as the optimal choice as this results in the highest power density with acceptable efficiency and will henceforth be used for further optimization.

Complete ZVS is achieved at the design implementations marked with a white circle in Figure 6.5. As shown in Section 7.3.2, the complete ZVS of the Prodrive-Select Rectifier does not result in the most efficient design, as initially expected. The reason for this is the required inductance value for complete ZVS (at v_{PN} = 400V) resulting in large inductor current ripples, which in turn cause increased conduction losses in the semiconductors due to large rms currents. Furthermore, the turn-off losses are significantly increased by the large inductor current ripple.

Partial ZVS of the 72kHz implementation is achieved for all inductance values ranging from 15μH to 30μH. This operating mode combines the reduced turn-on losses of ZVS with the reduced inductor current ripple of hard-switching variants. For

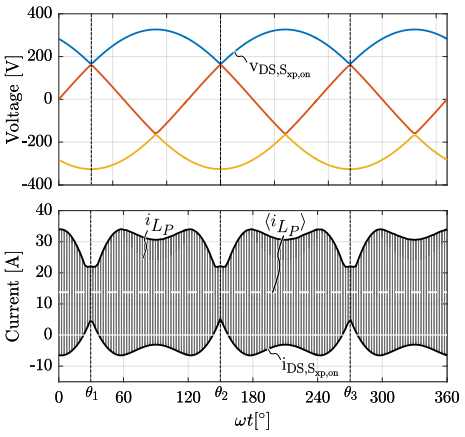

Figure 6.6: Prodrive-Select Rectifier typical waveforms for f_{sw} = 72kHz, $L_{P,N}$ = 20μH and n_i = 2. Loss of ZVS at $\theta_{1,2,3}$ corresponds to minimum v_{DS} and thus limits the turn-on losses.

the HF semiconductor selection of SCTH100N120G2AG the partial ZVS operating of the design implementation with $L_{P,N}$ = 20μH results in the highest efficiency. The reason for the shifting of the most efficient design from complete ZVS to partial ZVS is, in part, due to previously mentioned increased current ripple under complete ZVS. However, a second cause can be identified which limits the increase of hard-switching turn-on losses contrary to initial expectation and thus presents partial ZVS or hard-switching variants as viable options. The cause being that the hard-switching of the HF semiconductors $S_{xp,nz}$, expected to greatly reduce the efficiency, coincides with local minima around $\theta_{1,2,3}$ in the semiconductor's drain-source voltage as illustrated in Figure 6.6. The reduced v_{DS}, thus, limits the increase in turn-on losses when transitioning from ZVS to hard-switching designs.

For the HF semiconductor selection of SCTH90N65G2V7 (Figure 6.5*b*), hard-switching designs ($L_{P,N} > 30\mu H$), not the partial ZVS designs, result in the most efficient designs. The main reason for this discrepancy between the two semiconductor choices can be attributed to the fact that the datasheet for SCTH90N65G2V7 reveals a counter intuitive relationship where E_{off} is significantly larger than E_{on} for high drain-source currents. This diminishes the benefit of complete or partial ZVS and thus results in hard-switching designs to be the most efficient because of the lower conduction losses.

However, it is expected that the characteristics of the SCTH100N120G2AG designs are more close to reality. Firstly, the datasheet values for the SCTH90N65G2V7 were measured incorrectly, providing inconclusive results at best. Secondly, as explained in Section 2.3, a reduction of turn-off losses and increase of hard turn-on losses is to be expected when parallel capacitance is added across the MOSFETs drain-source terminals. This in turn increases the efficiency of the complete and partial ZVS designs, thus justifying these designs as viable options compared to hard-switched variants.

The partial ZVS designs ($L_{P,N} = 15-30\mu H$) for f_{sw} = 72kHz are selected as the optimal implementation for the interleaved Prodrive-Select Rectifier. In order to choose a definite design, a final comparison is done where the converter efficiency across the entire output voltage range is averaged as:

$$\eta_{avg} = \frac{\eta_{300V} + \eta_{350V} + 2 \cdot \eta_{400V} + \eta_{450V}}{5} \tag{6.1}$$

Where η_{400V} is weighted twice as this is the nominal operating voltage. Figure 6.7 shows the average efficiency (η_{avg}) for the partial ZVS designs implemented with HF semiconductor choice of SCTH100N120G2AG. Higher inductance values result in higher power densities as the required DM attenuation at the input is reduced with reducing current ripples. However, zero-voltage switching has further benefits compared to hard-switching in terms of control and high-frequency CM EMI. Firstly, shifting between hard and soft-switching during normal operation has negative effects on the control stability as the controller is tuned to the switch-node behaviour during dead-time of one of the two, and is not equipped to handle shifting between transition types, as detailed in Chapter 8. Secondly, a low-current, soft-switched turn-on generates far less high-frequency CM EMI due to the reduced voltage slope of the switch-node, as illustrated in Figure 5.8. Therefore, it is expected to benefit the converter's operation to select a design implementation which is largely soft-switching, while ensuring acceptable efficiency. These reasons combined tip the scale for selection of f_{sw} = 72kHz and $L_{P,N}$ = 20μH as the optimal design implementation selected from the design space specified in Table 6.1, denoted by a hexagon in Figure 6.7. The design indicated with a star in Figure 6.1 corresponds to the realized prototype, further elaborated in Chapter 8.

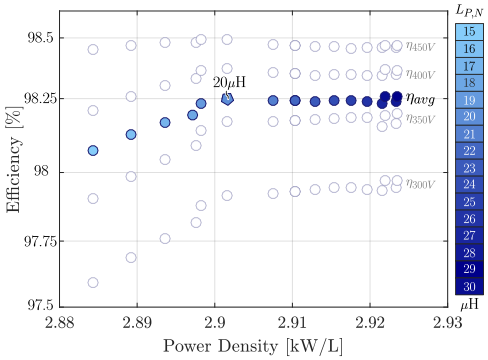

Figure 6.7: Prodrive-Select Rectifier averaged efficiency across the output voltage range for f_{sw} = 72kHz and HF semiconductor SCTH100N120G2AG, with inductance values $L_{P,N}$ selected to envelope the transition from complete ZVS to complete hard-switching designs. The hexagon indicates the Pareto-optimal design.

Design Specification The Pareto-optimal design specification can be found in Table 6.3 with corresponding schematic representation in Figure 6.8. The interleaved Prodrive-Select Rectifier is depicted with 2-stage *LCLC* input CM filter, a *CLC* input DM filter and single-stage *LC* output CM/DM filter. The IVS is implemented with a passive diode-rectification stage. Table 6.3 specifies the electrical characteristics, the semiconductor choices and the passive component values.

Table 6.3: Prodrive-Select Rectifier Pareto-optimal design specification.

	Component	Designator	Value	Unit	Selection	Note
Electrical	*Mains AC Input*	$v_{gr,1ph,rms}$	230	V	-	-
	Nominal DC Output	$v_{o,nom}$	400	V	-	-
	Output Power	$P_{o,nom}$	11	kW	-	-
	Switching Frequency	f_{sw}	72	kHz	-	-
	Interleaved Stages	n_i	2	-	-	-
Semiconductors	*Passive Rectifier Diodes*	D_{ax},D_{bx},D_{cx} D_{za},D_{zb},D_{zc}	-	-	DSP 25-12AT	-
	Bidir. Selector Switches	S_{aya},S_{byb},S_{cyc}	-	-	SCTH100N120G2-AG	-
	HF Buck Circuit Switches	S_{xp},S_{yp},S_{pm} S_{nz},S_{ny},S_{mn}	-	-	SCTH100N120G2-AG	-
	HF Buck Circuit Diodes	D_{yp},D_{ny}	-	-	C3D10065E	-
Passives	*Buck Inductors*	L_P,L_N	20	μH	PQ50/50, N95, 4.2mm	11 Turns HF-Litze 1006x0,071mm
	DM Output Filter	$C_{DM,o}$	5	μF	-	-
		$Cd_{DM,o}$	5	μF	-	-
		$RCd_{DM,o}$	0.4	Ω	-	-
	CM Output Filter	$L_{CM,o}$	2.8	mH	-	-
		$C_{CM,o}$,$Cd_{CM,o}$	4.7	μF	-	-
		$RCd_{CM,o}$	50	Ω	-	-
	Electrolytic Bulk Capacitor	C_{PN}	960	μF	-	-
	1st Stage Input DM Filter	$L_{DM,1}$	3	μH	-	-
		$C_{DM,1}$,$Cd_{DM,1}$	2.26	μF	-	-
		$RCd_{DM,1}$	4	Ω	-	-
	2nd Stage Input DM Filter	$C_{DM,2}$,$Cd_{DM,2}$	2.26	μF	-	-
		$RCd_{DM,2}$	1	Ω	-	-
	1st Stage Input CM Filter	$L_{CM,1}$	1.1	mH	-	-
		$C_{CM,1}$,$Cd_{CM,1}$	6.25	nF	-	-
		$RCd_{CM,1}$	600	Ω	-	-
	2nd Stage Input CM Filter	$L_{CM,2}$	1.1	mH	-	-
		$C_{CM,2}$,$Cd_{CM,2}$	6.25	nF	-	-
		$RCd_{CM,2}$	30	Ω	-	-

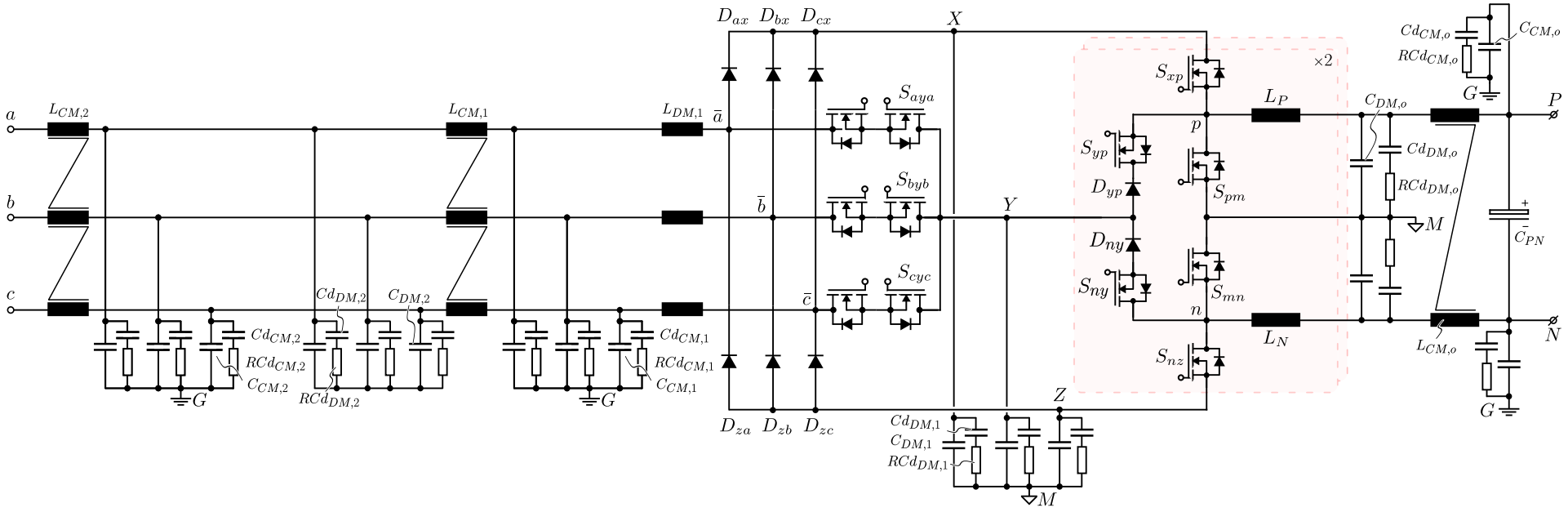

Figure 6.8: Schematic representation of the Pareto-optimal Prodrive-Select Rectifier as described in Section 6.3.1. The EMI input filter consists of 2-stage *LCLC* CM filter and a *CLC* DM filter. The EMI output filter consist of a single-stage *LC* CM and DM filter. The 3L buck circuits are implemented twice in order achieve interleaving of the output stages.

6.4. Summary

This chapter describes the design optimization of the Prodrive-Select Rectifier prototype design by utilizing the modelling technique presented in Chapter 5. The methodology of specifying the global design space is described in detail and summarized by a set of variable system parameters, such as switching frequency, buck inductance and interleaved stages, and a set of fixed parameters, such as input grid connection, output power and carrier wave. A further component design space is determined and summarized by a set of variable component choices, such as the HF MOSFETs and the inductor core size, and a set of fixed designs, such as the heatsink concept and the output EMI filter.

After determining the global and local design spaces, the virtual prototyping routine is initiated and the results of the performance space mapping are interpreted. A distinction is made between two design methodologies which both result in a Pareto-optimal design, but located in a different position on the Pareto-trajectory. The separate component impact on the total system efficiency and power density is observed by means of a volume and loss breakdown.

A design space with increased detail is formulated around a knee-point in the Pareto-trajectory. The detailed design space includes a smaller range of inductances and switching frequencies, and extends the scope to include multiple voltages in the converter output voltage range. An optimal design implementation is found utilizing partial soft-switching and interleaved output stages, a switching frequency of 72kHz and a buck inductance of 20μH.

7

Comparative Evaluation

7.1. Introduction

In this chapter a comparison study is conducted between the Prodrive-Select Rectifier and the Swiss Rectifier, using the previously presented modelling techniques. The result is an objective performance comparison between both topologies, giving insight into the relative strengths and weaknesses of each topology. Furthermore, comparisons of the Swiss Rectifier to other three-phase buck-type rectifiers, retrieved from literature, are presented in order to extend the scope of the comparison.

7.2. Methodology

The two converter systems that are compared in detail are the Prodrive-Select Rectifier and the Swiss Rectifier, as shown in Figures 2.6 and 3.1. In order to create an equal basis the converters are investigated in their simplest, non-interleaved variant. A further design space is specified in terms of the electrical characteristics and converter global variables as summarized in Table 7.1.

Table 7.1: Comparative evaluation design space for three-phase buck-type PFC rectifiers.

Description	**Parameter**	**Value**	**Unit**
single phase rms voltage	$v_{G,1ph,rms}$	230	V
single phase peak voltage	$v_{G,1ph,ampl}$	325	V
Mains frequency	f_G	50	Hz
Output voltage	v_{PN}	300-450	V
Nominal output voltage	$v_{PN,nom}$	400	V
Output power	P_o	5	kW
Switching frequency	f_{sw}	25-300	kHz
Buck Inductance	L_P/L_N	15-300	μH
Power factor at full power	$\lambda_{100\%}$	0.99	-
EMI compliance	-	Class A	-

The output power level P_o has been lowered, compared to the 11-kW use-case, to allow reasonable efficiencies of both converter systems in a non-interleaved variant. Further operating ranges are specified by the output voltage range of 300V-450V, with a nominal design output voltage of 400V. The converters are connected to a standard European three-phase grid and shall achieve a power factor of >0.99 at full load. The switching frequency (of the high-frequency buck circuits) is a variable allowed to range from 25kHz to 300kHz and the buck inductance can vary between 15μH and 300μH in order to envelope multiple design strategies, e.g. high-frequency zero-voltage switching or low-frequency hard-switching. The 2-D Pareto-front is an account of converter power density (ρ) versus efficiency (η). The global design variables switching frequency (f_{sw}) and buck inductance (L) are of most relevance due to their impact on the converter performance on the Pareto-front.

The semiconductors for the IVS and the buck circuits are fixed for both converter systems and can be found in Table 7.2. The IVS is equal for both converter systems and consists of three-phase rectifier diodes and SiC MOSFETs as bi-directional switches. The buck circuits are implemented with 1200V SiC MOSFETs in both converter systems as these switches can be effectively used for both topologies at the rated power level without the need for paralleling. The high-frequency diode in the Prodrive-Select Rectifier buck circuit is implemented with a SiC diode.

Table 7.2: Semiconductor choices used in the comparison of the Swiss Rectifier and Prodrive-Select Rectifier.

	Semiconductor	**Selected**	**Semiconductor**	**Selected**
Buck Circuits	S_{xp},S_{nz}	SCTH100N120G2AG	S_{xp},S_{nz}	SCTH100N120G2AG
	S_{py},S_{yn}	SCTH100N120G2AG	S_{yp},S_{ny}	SCTH100N120G2AG
			S_{pm},S_{mn}	SCTH100N120G2AG
			D_{yp},D_{ny}	C3D10065E
IVS	$D_{abc,xz}$	DSP25-12AT	$D_{abc,xz}$	DSP25-12AT
	S_{yabc}	SCTH100N120G2AG	S_{yabc}	SCTH100N120G2AG
	Swiss Rectifier		*Prodrive-Select Rectifier*	

The use-case of the converter systems is the front-end AC-to-DC converter of a two-stage, isolated on-board EV charger, as detailed in Chapter 2. The performance space is specified as the power density versus efficiency. Parameters relevant to this comparison are;

- ◇ Semiconductor stresses
- ◇ Semiconductor losses (P_{semi})
- ◇ Inductor peak stored energy ($P_{L,peak}$)
- ◇ Normalized required DM/CM attenuation (A^*_{norm})

The semiconductor stresses give an indication of the type of semiconductors which can be used for the topology in terms of breakdown voltage rating. This can play a large part in the efficiency of a converter as, for instance, MOSFET switching losses and $R_{DS,on}$ vary greatly depending on the v_{DS} rating.

The semiconductor losses are a large contributor to the system efficiency and are thus an indication of the converter performance. A maximum junction temperature and swing for the semiconductors can be specified in order to guarantee certain converter lifetime parameters. As specified in Table 7.2 the same semiconductors are used for both converters in order to provide an objective comparison. A possible improvement to this is the scaling of semiconductor die area as in [11].

The inductor peak stored energy can be assumed proportional to the inductor volume through a volumetric coefficient k_L as:

$$v_L = k_L \cdot L \cdot \hat{I}^2$$

This means that the peak stored energy $P_{L,peak} = \frac{1}{2} \cdot L \cdot \hat{I}^2$ of the converter gives an indication of the inductor size at that operating point, which attributes a significant amount to the total converter volume.

The converter normalized required attenuation is a measure of the required EMI filter size. As the modelling technique described in Section 5.5.3 derives a required attenuation parameter for the first effective switching frequency above 150kHz, the standard required attenuation is not an illustrative parameter when different switching frequencies are compared. Therefore, it is assumed that the input EMI filter is a two stage *LCLC* filter for both the CM and DM, allowing a normalization of the required attenuation by 80dB/dec to 150kHz. This allows the design of a filter with the same cut-off frequency but different attenuation levels for converter systems with different switching frequencies.

7.3. Converter Comparison

7.3.1. Semiconductor Stresses

The semiconductor voltage stresses for the Prodrive-Select Rectifier can be found in Table 3.1. The semiconductor voltage stresses of the Swiss Rectifier are summarized in Table 7.3. The blocking voltages of the IVS are the same for both converter systems. For the Swiss Rectifier all the semiconductor devices in the top and bottom buck circuits have a maximum blocking voltage of:

$$v_{XY,max} = v_{G,1ph,ampl} \cdot \frac{3}{2} = 537V$$

This means that the four HF semiconductors of the Swiss Rectifier have to be implemented with 650V devices if a safety margin of ≈20% is taken into account. An increase from four to eight semiconductor devices can be observed in the 3L buck circuits of the Prodrive-Select Rectifier. However, the devices in the main power path (S_{xp},S_{pm},S_{nz},S_{mn}) can be implemented with 450V devices. The lower breakdown voltage usually being paired with decreased switching losses and lower $R_{DS,on}$. Two active switches in the injection path (S_{yp},S_{ny}) can be implemented with 250V devices. Lastly, the two diodes in the injection path (D_{yp},D_{ny}) have to be implemented with 650V devices.

Table 7.3: Swiss Rectifier Semiconductor Maximum Blocking Voltages

	Semiconductor	**Parameter**	**Value**	**Unit**
Buck Circuits	S_{xp}	$v_{ds,S_{xp},max}$	537	V
	S_{py}	$v_{ak,D_{yp},max}$	537	V
	S_{nz}	$v_{ds,S_{nz},max}$	537	V
	S_{yn}	$v_{ak,D_{yn},max}$	537	V
IVS	$D_{abc,xz}$	$v_{ak,D_{abc,xz},max}$	620	V
	S_{yabc}	$v_{dsd,s_{yabc},max}$	537	V

Due to the scarcity of low voltage, high power SiC MOSFETs there is not yet a clear advantage of the Prodrive-Select Rectifier over the Swiss Rectifier as the semiconductors would have to be implemented with 650V devices if purely SiC semiconductors are evaluated. Lower voltage Si or GaN semiconductor devices could be evaluated which could mean a reduction of conduction losses compared to the 650V SiC devices. In the case of Si devices, however, this goes at the cost of switching losses, which means they are only a viable option when applying ZVS of the active semiconductors.

7.3.2. Semiconductor Losses

Figure 7.1 shows the semiconductor switching, conduction and total losses for both the Prodrive-Select Rectifier and the Swiss Rectifier. The white line in the lower left corner symbolizes the design implementations that achieve complete ZVS. As discussed in Chapter 6, the ZVS designs do not result in the most efficient designs as can also be derived from the semiconductor loss figures. Evident in Figure 7.1*a* is the sharp increase in conduction losses when complete ZVS is achieved, this corresponds to the increase of inductor current ripple (Δi_L). Furthermore, Figure 7.1*b* shows a slight increase in the switching losses in complete ZVS designs driven by the current ripple generating large turn-off losses.

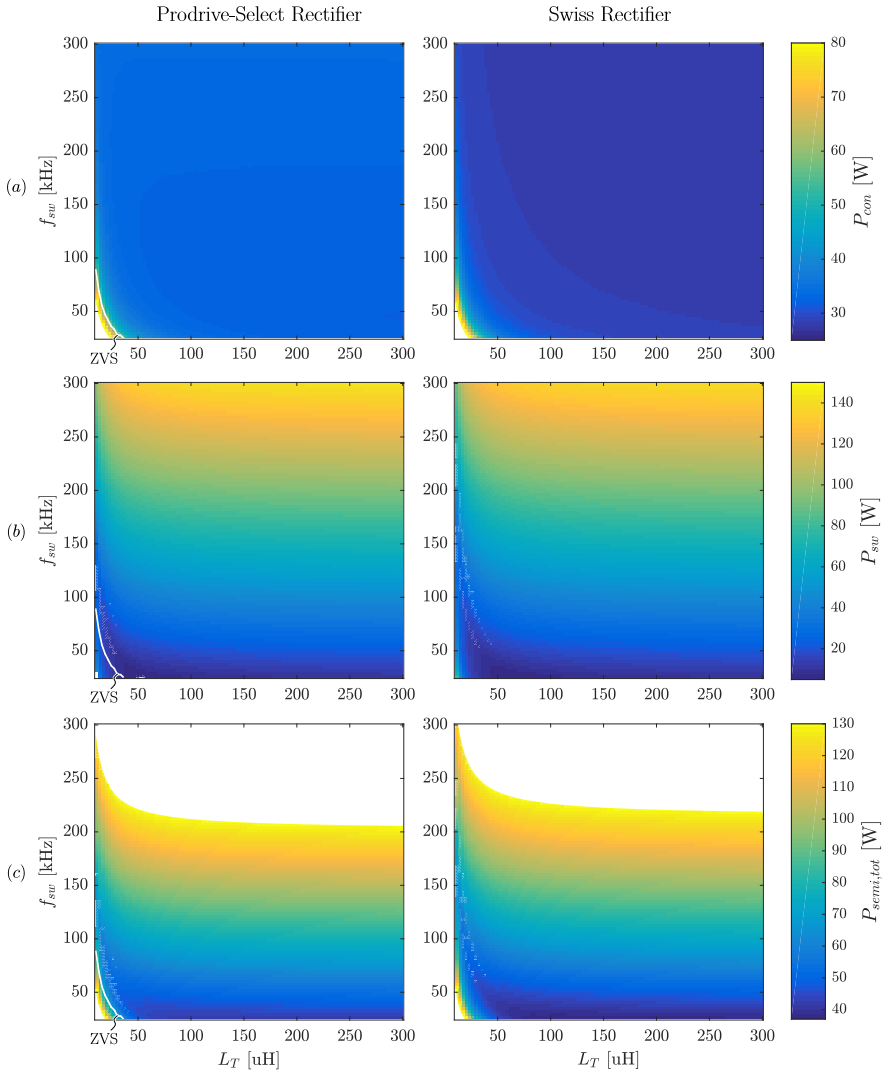

Figure 7.1: Semiconductor (*a*) conduction losses, (*b*) switching losses, and (*c*) total losses for the Prodrive-Select Rectifier and the Swiss Rectifier at nominal output voltage ($V_{PN} = V_{nom}$).

Combined, these two facts reflect the conclusions of Chapter 6 where Pareto-optimal designs are found to be just above the ZVS line, corresponding to partial ZVS design implementations. Moreover, the expected advantage ZVS would give the Prodrive-Select Rectifier (decreased switching losses) over the Swiss Rectifier can be seen to be nullified by the increased current ripple. The reason for this is further elaborated in Section 6.3.1. A global comparison of the two suggest nearly equal performance in terms of total semiconductor losses across the entire design space at nominal output voltage. A slight advantage is evident to the Swiss Rectifier in terms of conduction losses due to the lower number of semiconductors in the injection current path.

7.3.3. Inductor Peak Stored Energy

Figure 7.2 shows the inductor peak energy for the L_P and L_N inductors. Both topologies exhibit nearly identical peak energies, with a small advantage to the Prodrive-Select Rectifier most evident around the complete ZVS line. This is due to marginally lower total inductor current ripple.

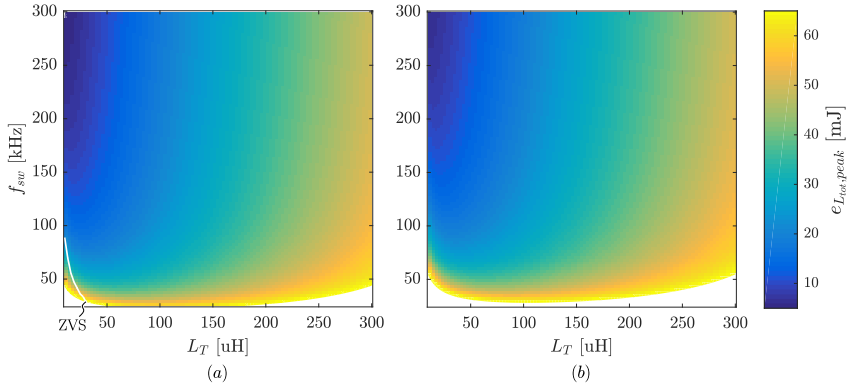

Figure 7.2: Inductor peak stored energy for $L_{P,N}$ for (*a*) Prodrive-Select Rectifier and (*b*) Swiss Rectifier.

7.3.4. Normalized Required Attenuation

Figure 7.3 depicts the normalized required attenuation $A^*_{CM,norm}$ and $A^*_{DM,norm}$ for both the Prodrive-Select Rectifier and the Swiss Rectifier. Evident is that both topologies have very similar filtering requirements, as the topologies have similar high frequency behaviour. This means the filter design results in similar component values and thus the volume of the filters are also about equal in both converter systems.

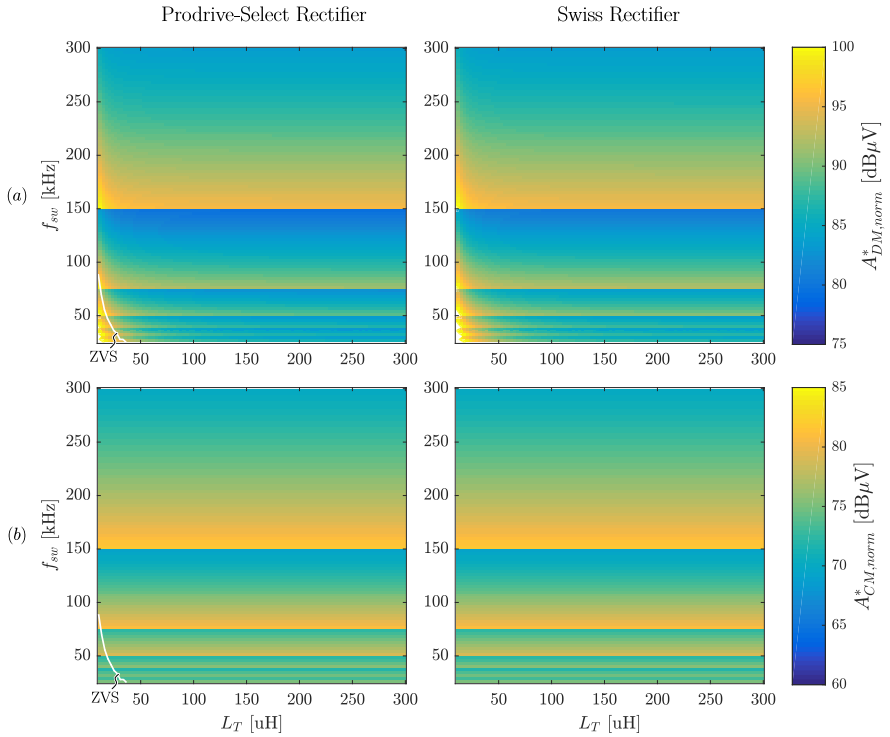

Figure 7.3: (*a*) Differential-mode normalized required attenuation (*b*) common-mode normalized required attenuation for the Prodrive-Select Rectifier and the Swiss Rectifier.

No clear difference in the normalized required attenuation exists between the compared converter systems. Furthermore, the CM and DM noise of the Swiss Rectifier is within a few dB of the noise generated by the six-switch buck-type rectifier, implicating no performance difference with respect to EMI filtering between any of the three converter systems [5].

7.3.5. Comparison Conclusion

From the converter comparison it can be concluded that the Prodrive-Select Rectifier and the Swiss Rectifier have very similar performance in the relevant performance aspects. An advantage to the Prodrive-Select Rectifier is the possibility for semiconductor switch implementation with lower voltage ratings, while an advantage to the Swiss Rectifier are slightly lower conduction losses. Figure 7.4 depicts a comparative evaluation between the Swiss Rectifier and the 6-Switch Buck-Type Rectifier originating from [5]. This comparison highlights the relative strengths of the Swiss Rectifier compared to a typical 6-Switch Buck-Type summarized as lower conduction and switching losses which translate into higher achievable efficiency. This comparison can be extended to the Prodrive-Select Rectifier by means of the preceding comparison between the Prodrive-Select and the Swiss Rectifier. It should be noted that even though the Prodrive-Select Rectifier does not provide an obvious advantage over the Swiss Rectifier it does function as a viable and versatile alternative which can be deployed by Prodrive as a Buck-Type PFC Rectifier without infringing external patents.

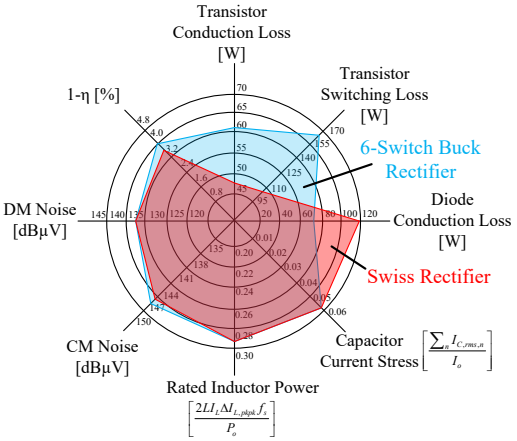

Figure 7.4: Comparative evaluation of the Swiss Rectifier with the 6-Switch Buck-Type Rectifier. (The more advantageous system covers the smaller area in the diagram). Source: [5]

7.4. Pareto-Optimal Designs

The performance space for both converters is shown in Figure 7.5. The efficiency (η_{avg}) is calculated by equation 6.1, where it is an average of the converter efficiency at various output voltage ratings. The design in terms of buck inductors and EMI filters is done for the nominal output voltage of $v_{PN} = 400V$.

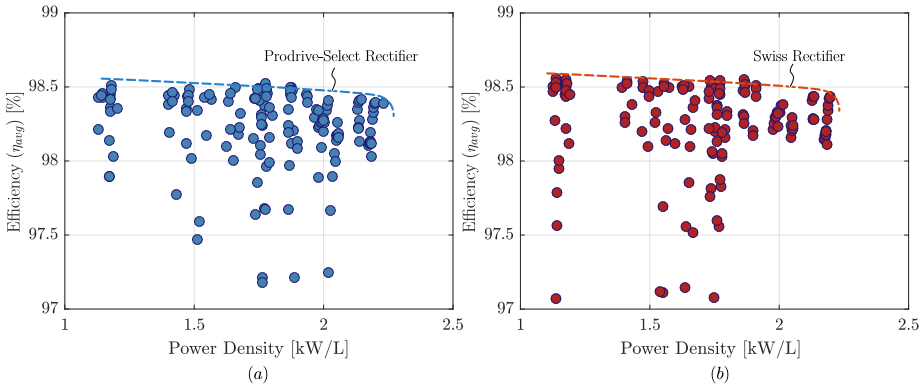

Figure 7.5: Pareto-front of power density vs. efficiency of (*a*) the Prodrive-Select Rectifier and (*b*) the Swiss Rectifier.

Evident is the similar relative characteristic of the Pareto-optimal trajectory, indicated by the dashed line, for both converter systems. No definitive advantage can be derived in favour of either of the rectifier systems, as they both yield nearly identical power densities and efficiencies. The Pareto-optimal design for the design space specified in Table 7.1 corresponds to a partial ZVS design of $L_{P,N} = 30\mu$H and $f_{sw} = 144$kHz. This combination exhibits low semiconductor losses due to the partial zero-voltage switching and reduced EMI filtering requirements due to the switching frequency being below the 150kHz class A measuring frequency.

7.5. Summary

This chapter serves as the comparative evaluation of the Prodrive-Select Rectifier with the Swiss Rectifier. A design space is specified which creates and equal footing for both converter systems. Certain converter parameters are fixed in the design space, such as the semiconductors, the grid connection and the output power. Four converter parameters are chosen for comparison which are representative for the total converter performance.

Firstly, the semiconductor stresses reveal an advantage to the Prodrive-Select Rectifier due to the nature of the buck circuits. This advantage is, however, negated by the limited availability of low voltage, high power SiC MOSFETs. Further comparison of the converter's semiconductor losses, inductor peak stored energy and required attenuation reveal a similar performance between both PFC rectifiers. This is further confirmed by the Pareto-front, where there is no clear advantage to either converter on the power density versus efficiency performance space. The Prodrive-Select is compared to the six-switch buck-type rectifier and a clear advantage is found in favour of the Prodrive-Select Rectifier in terms of switching and conduction losses.

8

Hardware Demonstrator and Measurement Results

8.1. Introduction

This chapter describes the prototype design of the Prodrive-Select Rectifier and the model verification of the proposed modelling techniques. Design choices for the prototype are clarified and an in-depth description of the converter and its components is provided. Two different design implementations are measured; one with small buck inductance ($L_{P,N}$ = 18.4μH) and one with large buck inductance ($L_{P,N}$ = 200μH). Typical electrical waveforms of the rectifier are depicted and verified with the experimental measurements. Finally, power measurements are performed at mains 220-V AC input voltage and 400-V nominal DC output voltage resulting in an efficiency and THD curve with respect to output power. The component and total volume of the converter are evaluated and a conclusion is formulated about the prototype in the performance space. A loss breakdown of the hardware demonstrator with $L_{P,N}$ = 18.4μH operating at full power is discussed in detail.

8.2. Prototype Converter Design

A Pareto-optimal design of the Prodrive-Select Rectifier, found in Chapter 6, utilizing interleaved and partial soft-switching output stages (buck circuits) is implemented and verified. This design uses a once interleaved variant with a switching frequency of 72kHz and a buck inductance of 20μH. The prototype is designed in order to approach this optimal implementation. A schematic representation of the complete prototype can be seen in Figure 6.8 and a summary of all electrical parameters, the relevant components and their values can be found in Table 8.1. In order to limit the design effort involved in the prototype design phase, certain segments of the design are reused from an existing product from Prodrive Technologies.

EMI Filter The input EMI filter consists of a 2-stage DM and CM filter, placed between the input terminals a, b, c and $\bar{a}, \bar{b}, \bar{c}$ and including the capacitors placed on nodes X, Y, Z. The EMI input filter is reused from an existing three-phase rectifier product because this rectifier's noise sources are comparable to the Prodrive-Select Rectifier noise sources both in terms of frequency and amplitude. A disadvantage of the reuse of the EMI filter is the unnecessarily high attenuation leading to non-optimal EMI filter volume, as is evident from the volume breakdown.

The output EMI filter consists of a single stage DM filter formed by the buck inductors and the DM capacitors to midpoint M. A single stage CM filter is placed cascaded to the DM filter and consists of a CM choke and Y-rated CM capacitors to PE. A bulk electrolytic capacitor is placed from P to N with a value of 960 μF.

Semiconductors The IVS is implemented with a passive rectifier in order to decrease the cost and complexity of the converter. The passive rectifier diodes chosen are 1200V Si diodes which can support more than 17kW nominal operation at 400-V rms line-to-line three-phase input. MOSFETs are placed anti-series to the top three diodes of the passive rectifier due to the reuse of the IVS. These switches are not necessary for the

design and their impact is discussed in Section 8.5. The bi-directional switches are implemented with 1200V SiC MOSFETs with ultra-low $R_{ds,on}$. The gate signals are kept separate in order to allow for a higher flexibility in the control strategy during sector transitions [17].

The high-frequency semiconductors of the 3L buck circuits are implemented with the same 1200V SiC MOSFETs. Ideally, switches with lower blocking voltages would be chosen as stated in Section 6. However, a shortage of components has resulted in the use of 1200V SiC MOSFETs for the prototype implementation. It is expected to result in a slight decrease of efficiency compared to the Pareto-optimal design but will not have an impact on the system power density. A parallel capacitance of 1nF is placed across these MOSFETs in order to decrease the turn-off losses. The injection diodes are implemented with a parallel connection of two SiC diodes. Two are placed in parallel in order to allow full power operation of the converter at low output voltages.

Buck Inductors The inductors are implemented with an N95 PQ65/54 core with 1.8mm airgap. Eleven turns of the HF litz wire with 1890 strands of 0.071mm results in an inductance of 18.4μH. This design was bounded by the reuse of the core and wire type, which results in a rather large total inductor volume. According to the Pareto-optimal design, a PQ50/50 core should be used for optimal performance. The inductor design aims to reach the optimal 20μH inductance value.

Prototype Mechanics An unfolded version of the prototype can be seen in Figure 8.1. There are two large PCBs which take up the entirety of the converter area, namely, the control board and the power board. The IVS and the HF board are placed underneath the power board and are interfaced to the cold plate through aluminium blocks. The input EMI filter is split between the control board, the EMI filter board and the power board. Further depicted are the gate drivers, the buck inductors and the FPGA board. A volume breakdown of the total converter system can be found in Section 8.3.

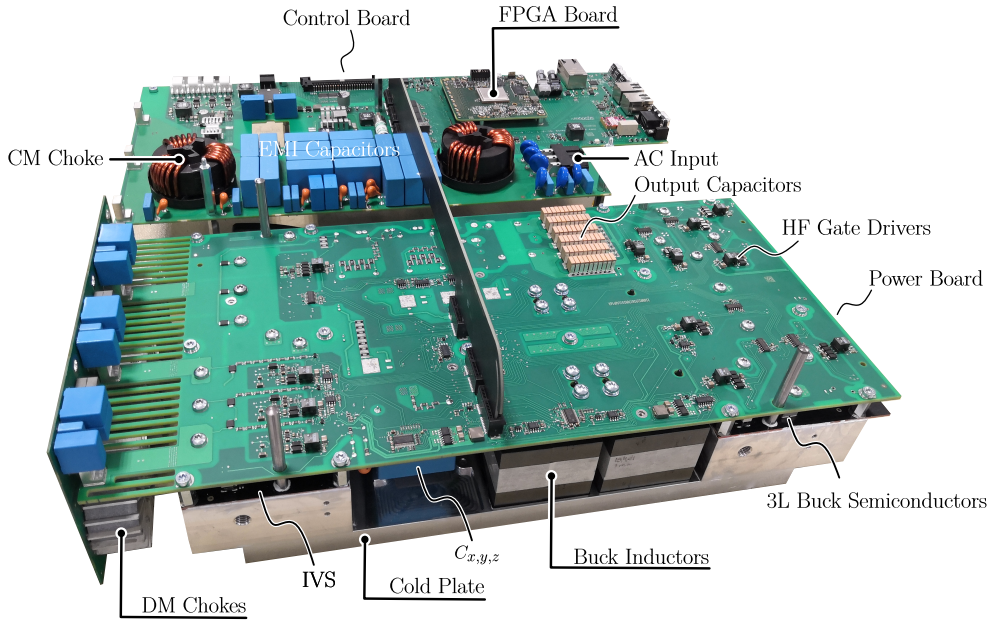

Figure 8.1: Unfolded prototype of the Prodrive-Select Rectifier with dimensions *104*mm x *412*mm x *201*mm. An output power of 11kW is reached with a total system efficiency of >97.5% and a power density of 1.3kW/L.

Table 8.1: Prodrive-Select Rectifier prototype component values and selection.

	Component	Designator	Value	Unit	Selection	Note
Electrical	*Mains AC Input*	$v_{gr,1ph,rms}$	230	V	-	-
	Nominal DC Output	$v_{o,nom}$	400	V	-	-
	Output Power	$P_{o,nom}$	11	kW	-	-
	Switching Frequency	f_{sw}	72	kHz	-	-
	Interleaved Stages	n_i	2	-	-	-
Semiconductors	*Passive Rectifier Diodes*	D_{ax},D_{bx},D_{cx} D_{za},D_{zb},D_{zc}	-	-	DSP 25-12AT	-
	Bidir. Selector Switches	S_{aya},S_{byb},S_{cyc}	-	-	SCTH100N120G2-AG	-
	HF Buck Circuit Switches	S_{xp},S_{yp},S_{pm} S_{nz},S_{ny},S_{mn}	-	-	SCTH100N120G2-AG	-
	HF Buck Circuit Diodes	D_{yp},D_{ny}	-	-	C3D10065E	2x Parallel
Passives	*Buck Inductors*	L_P,L_N	18.4	μH	PQ65/54, N95, 1.8mm	11 Turns HF-Litz 1890x0,071mm
	DM Output Filter	$C_{DM,o}$	18	μF	Ceralink 500V FA10	-
		$Cd_{DM,o}$	18	μF	Ceralink 500V FA10	-
		$RCd_{DM,o}$	0.4	Ω	-	-
	Electrolytic Bulk Capacitor	C_{PN}	960	μF	-	-

8.3. Volume Breakdown

Table 8.2 summarizes the calculated and actual volumes of the individual converter components. All components that are specified with a designator are graphically shown in Figure 8.2. A total system volume of 8612 cm^3 or 8.6 L corresponds to a system power density of 1.3 kW/L when nominal 11 kW output power is assumed. A *Delta* column in Table 8.2 shows the percentage difference between the calculated and the actual component volumes. The *Total* column shows the percentage of the total volume the component occupies.

Table 8.2: Prodrive-Select Rectifier prototype volume breakdown.

	Component	**Designator**	**Calculated** [cm^3]	**Actual** [cm^3]	**Delta** [%]	**Total** [%]
HF	*Semiconductors*		13.36	13.36	-	-
	Gate drivers		-	4.93	-	-
	Snubbers		-	2.26	-	-
	Other		-	264	-	-
	Total	V_{HF}	193	282	-32%	3%
IVS	*Semiconductors*		20.05	20.05	-	-
	Gate drivers		-	3.70	-	-
	Snubbers		-	1.70	-	-
	Other		-	194	-	-
	Total	V_{HF}	186	215	-13%	2%
EMI Filter	CM_o		18.0	14.3	+26%	-
	DM_o		29.2	60.6	-52%	-
	$CM_i + DM_i$		1041	954	+9%	-
	Other		-	490	-	-
	Total	V_{EMI}	1088	1519	-28%	18%
Other	Buck Inductor	$V_{L_{P,N}}$	885	793	+12%	9%
	Cooling Plate	V_{cooling}	643	1221	-47%	14%
	Cooling Interface	$V_{\text{Al,block}}$	1006	1276	-21%	15%
	Auxiliary	V_{aux}	380	827	-54%	10%
	Surplus	V_{surplus}	719	2479	-	29%
	Total Converter	$V_{\text{converter}}$	5100	8612	-41%	

The HF semiconductors take up 3% of the total volume. A difference of -32% is evident when compared to the calculated volume. This is mostly due to PCB layout and interconnection margins being larger than modelled. The IVS takes up 2% of the total converter volume. A delta of -13% also originates from the inaccuracy of the calculated margins.

The complete EMI filter, both input and output, takes up 18% of the total volume. On an individual filter level a large delta of -52% is seen in the DM output filter (DM_o). This is due to the prototype DM output filter being designed for a 900V output bus, which results in larger DM output capacitors, as opposed to the modelled output bus voltage of 400V. A difference of -28% in the calculated volume of the total EMI filter is observed and can be attributed to the fact that the interconnection and layout of the filtering (denoted as *other*) takes up almost 0.5 L, which is underestimated in the model.

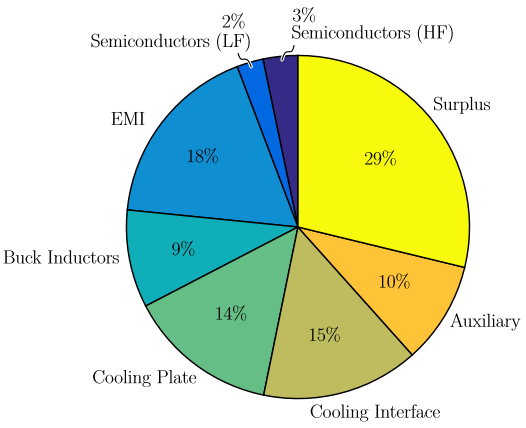

Figure 8.2: Prodrive-Select Rectifier prototype volume breakdown. In terms of electrical components the Buck Inductors and the EMI filter take up the most volume, while the LF and HF semiconductor are only a fraction of the total volume.

Further notable volumes are the cooling plate and cooling interface, taking up 14% and 15% of the total volume, respectively. The cooling plate is a crucial component which functions as the heatsink for most of the converters lossy components. A delta of -47% is observed and results from the fixed

dimensioning of the prototype. The prototype mechanics were designed for a converter with 6 instead of 4 inductors and thus the cooling plate is scaled accordingly. The model, however, shows that the volume could be decreased by >0.5 L if the mechanics were adjusted to accommodate only 4 inductors. The cooling interface is classified as 'wasted' volume, as the aluminium blocks only deteriorate the thermal performance and increase the volume. The interface is, however, needed in order to thermally couple the MCPCBs to the cold plate.

The auxiliary converter systems such as power rails, isolated supplies and the FPGA board take up 10% of the total volume. A large delta of -54% is observed due to the same reason as the cooling plate. The expected converter area is higher for the prototype than for an optimal implementation of the Prodrive-Select Rectifier due to the different number of inductors assumed in the design.

The final converter measurements are 104 x 412 x 201 (mm^3), resulting in 8.6 L of boxed volume. A delta of -41% to the calculated boxed volume can be explained by the surplus volume of 2.5 L. This surplus in the prototype is largely attributed to the volume between the power board and the control board. The height between these two PCBs is dominated by the height of the input EMC filter components, while the rest of the area is free air. This area is not taken into account in the converter volume model. Furthermore, the calculated volume assumes an optimal implementation of the Prodrive-Select Rectifier and, thus, shows that a large reduction in converter volume is possible.

A prototype with a power density of 1.3 kW/L is not yet competitive with the state-of-the-art three-phase buck-type rectifiers as stated in Table 2.1. The low resulting power density is mainly attributed to the fact that the design, of which this prototype has reused some components, is for a 20-kW boost-type PFC rectifier, meaning the design choices, e.g. component ratings, creapage and clearance rules etc., are non-optimal for an 11-kW buck-type PFC rectifier. However, as stated in Chapter 6, a Pareto-optimal implementation of the Prodrive-Select Rectifier with smaller buck inductors can result in power densities nearing 3 kW/L.

8.4. Measurement Results

Measurements of the prototype are done in order to verify the operating principle and the modelling techniques. A picture of the measurement set-up can be found in Appendix A, Figure A.3. A balanced three-phase mains is simulated with a *Chroma 61845*. An electronic load *EA-ELR 91500-30* is used for sinking the output current and the power measurements are done with a *Yokogawa WT5000* power analyzer. A nominal mains voltage of 220V is used because the PLL, depicted in Figure 4.1, shows the least noise at this voltage.

Input Current THD The first measurement verifies the power factor correcting capability of the converter. As explained in Chapter 2, the THD is a measure of the quality of the mains current drawn by the converter. Typically, the THD of the mains AC input currents has to be below 15%. More strict guidelines are set in place for, for instance, the aircraft industry, where a THD of less than 5% is required. The measured THD across the entire output power range of the hardware demonstrator with $L_{P,N}$ = 18.4μH can be found in Figure 8.3*b*. A THD below 5% can be observed for the power levels between 5kW and 8kW.

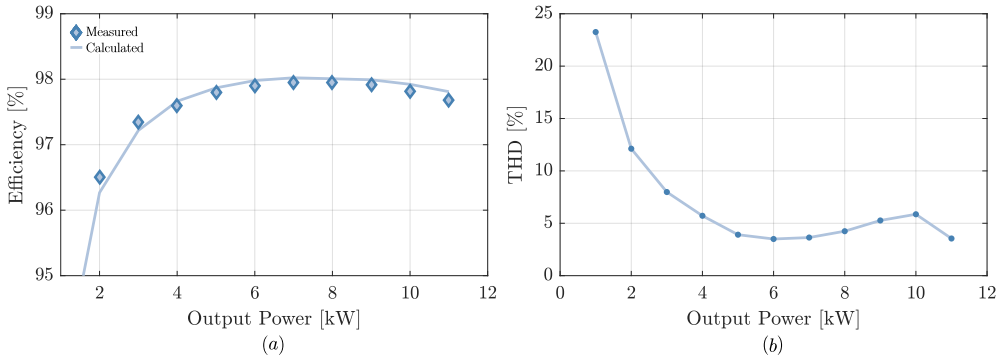

Figure 8.3: Measurements of the hardware demonstrator of Figure 8.1 with $L_{P,N}$ = 18.4μH, 220-V mains AC input and 400-V DC output. (*a*) Measured and calculated efficiency versus output power P_{out}, demonstrating efficiencies >97.5% for >4kW output power and 97.69% efficiency at full power. (*b*) The total harmonic distortion (THD) versus the output power, showing 3.5% THD at full power and a peak around 10kW due to partial hard-switching. The measurements are done using a *Yokogawa WT5000* power analyzer.

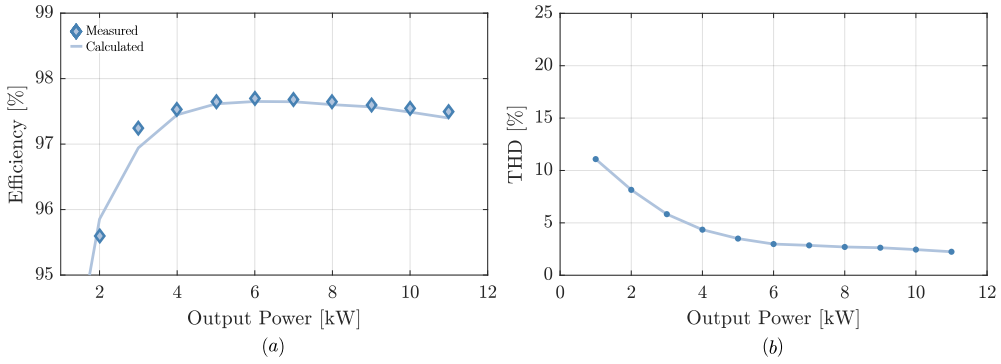

Figure 8.4: Measurements of the hardware demonstrator of Figure 8.1 with $L_{P,N}$ = 200μH, 220-V mains AC input and 400-V DC output. (*a*) Measured and calculated efficiency versus output power P_{out}, demonstrating efficiencies >97% for >4kW output power and 97.48% efficiency at full power. (*b*) The total harmonic distortion (THD) versus the output power, showing 2.2% THD at full power. The measurements are done using a *Yokogawa WT5000* power analyzer.

An increase in the THD to 6% occurs around 10kW. This increase in THD can be explained by the fact that the converter is partially hard-switching between 6kW and 11kW. The control scheme of Chapter 4 does not take the transition between hard- and soft-switching into account. Due to the necessary dead-time injected between the switching of the 3L buck circuit MOSFETs, the converter's input-to-output transfer function changes depending on the location in the line-cycle and whether the converter is hard- or soft-switching, as illustrated in Figure 6.6. This change to the transfer function manifests itself in a temporary system gain decrease when the converter is hard-switching. In order to combat this, dead-time compensation is implemented with a feed-forward structure which estimates when the converter is hard-switching and adjusts the

controller gain appropriately. With dead-time compensation the hardware demonstrator reaches 3.5% THD at full output power. The measured converter input currents at full power are depicted in Figure 8.5.

In order to verify the validity of the operating principle and controller without transitions between hard- and soft-switching, the hardware demonstrator is further measured with $L_{P,N}$ = 200μH. This inductance value ensures complete hard-switching at all output powers and the THD measurements are depicted in Figure 8.4*b*. A steady decrease in the THD is observed to 2.2% at full power. Overall, the THD is lower than the $L_{P,N}$ = 18.4μH implementation. Firstly, this can be attributed to the fact that the converter is completely hard-switching and thus there is no transient in the system transfer function. Secondly, the large inductance is accompanied by small inductor current ripple which allow for easier control of the inductor average currents and lower dynamic response. This is especially evident when looking at the mains AC input currents of Figure 8.5. Even though the THD of both converter implementations are close, significant high frequency disturbance can be seen in Figure 8.5*a*. This is mainly attributed to the fact that the buck circuits consist of lower inductance, which increases the buck circuit's bandwidth and subsequently its sensitivity to high-frequency noise.

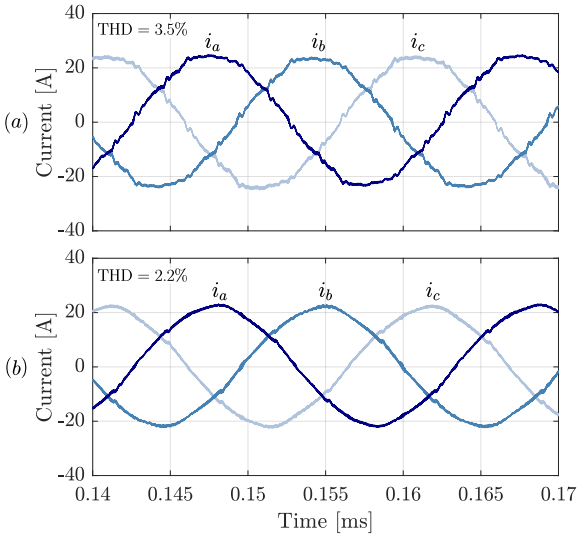

Figure 8.5: Measured converter input currents $i_{a,b,c}$ for 11kW operation at 220-V mains AC input voltage and 400-V DC output voltage for (*a*) hardware demonstrator of Figure 8.1 with $L_{P,N}$ = 18.4μH and (*b*) $L_{P,N}$ = 200μH.

Efficiency Figures 8.3*a* and 8.4*a* depict the measured and calculated efficiency for both hardware prototype implementations. Figure 8.3*a* shows efficiency measurements of the hardware demonstrator with $L_{P,N}$ = 18.4μH. An efficiency above 97.5% at >3kW output power, a peak efficiency of 97.95% at 7kW and a full power efficiency of 97.69% at 11kW is achieved. Furthermore, the modelling techniques of Chapter 5, applied to the prototype design, produce a set of calculated efficiencies. A calculated loss breakdown of the hardware demonstrator with $L_{P,N}$ = 18.4μH is discussed in Section 8.5. A delta of +0.12% is observed between the calculated and the measured efficiency at full power operation, which amounts to a mismatch of +13W. This error is mostly attributed to the error margins of the employed model. In particular the switching loss model of the HF semiconductors is subject to a large error. The placement of a parallel capacitance across the MOSFET drain-source influences the E_{on}/E_{off} curves. Especially the voltage-current $V \cdot I$ overlap during a switching transient is influenced due to the voltage delay. Without proper switching loss measurements of the semiconductor devices, it is challenging to quantify the error margins. An analytical switching loss model could be employed in order to more accurately estimate these losses [40].

Further inaccuracy of the employed models is observed in the auxiliary losses. These losses mainly include the PCB and wiring losses. Depending on an estimation of the wire, trace and connector resistance, the auxiliary losses can vary by as much as ±15W at full power operation, accounting for an error margin of ±0.14% in the total calculated system efficiency at 11kW. Lastly, the power measurements done by the power analyzer are also subject to an error margin (97.69% at 11kW error margin: {97.65%-97.73%}) due to error margins on the voltage and current measurement. Without proper verification of the converter efficiency with, for instance, a high accuracy calorimetric loss measurement [11], the error margin of the power measurement can not be narrowed.

Figure 8.4*a* shows the efficiency measurements for the hardware demonstrator with $L_{P,N}$ = 200μH. This design is characterized by low inductor ripple current, corresponding to low switch rms current, and complete hard turn-on of switches $S_{xp,nz}$. The measurements show a peak efficiency of 97.75% at 6kW and a full power efficiency of 97.48% at 11kW. Compared to the implementation with the small inductance, the complete hard-switching variant shows a decrease in efficiency of -0.21% at full power, mainly attributed

to the increased switching losses. Due to the relatively low voltage across the semiconductor during hard-switching, the switching losses are still acceptable and thus a reasonable efficiency is achievable. However, the large inductance peak stored energy equals ≈35mJ while the small inductance peak stored energy equals ≈22mJ, which can be directly linked to inductor volume as stated in Chapter 7. It can be concluded that the small inductance, soft-switching design achieves both higher efficiency and lower inductor stored energy. The downside of the small inductance, soft-switching design is the higher dynamic response of the buck circuits and the partial soft- and hard-switching transitions which increase the control complexity.

3L Buck Circuit Waveforms Figure 8.6 depicts the measured and modelled waveforms for the intermediate, piece-wise sinusoidal voltages v_{XM},v_{YM} and v_{ZM}, the DC output voltage v_{PN}, the inductor voltage v_{L_P} and the inductor current i_{L_P}. Evident is a slight non-linearity of the measured v_{L_P} due to the intermediate voltage nodes varying during a switching cycle, which is not modelled. The switching-cycle variation of the intermediate voltage nodes is caused by the ampere-second balance of the capacitors $C_{X,Y,Z}$. As explained in Section 5.5.3, the size of this capacitor is chosen in order to limit the voltage variation and to provide reasonable power factor at low output power. Furthermore, a large peak-to-peak voltage ripple is present on v_{PN} which is attributed to the fact that the CM output filter is not assembled in the hardware demonstrator.

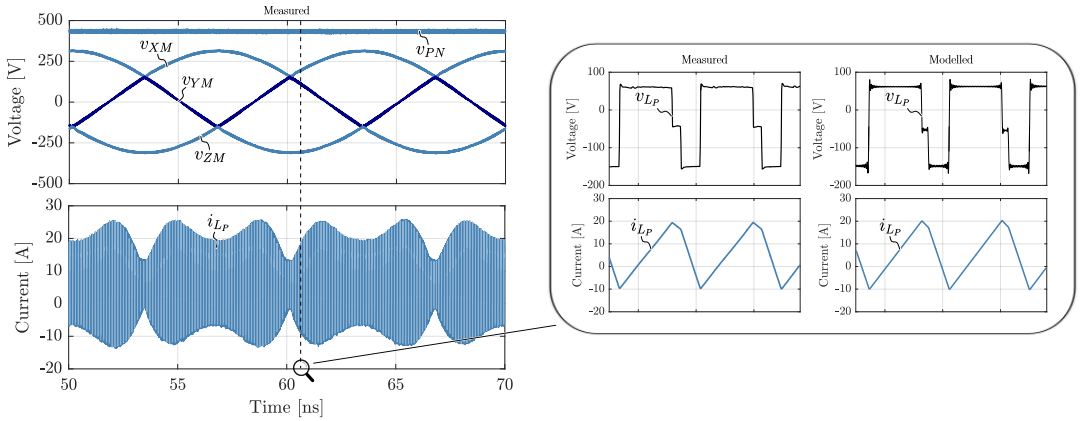

Figure 8.6: Measured and modelled (50 Fourier coefficients) waveforms of the hardware demonstrator with $L_{P,N}$ = 18.4μH at nominal 400-V DC voltage and 5kW output power. Depicted are the intermediate voltages after the IVS (v_{XM}, v_{YM}, v_{ZM}), the output voltage (v_{PN}) and the inductor current (i_{L_P}). The zoomed in figure shows the three-level volt-second across the inductor v_{L_P} and the resulting inductor current i_{L_P}.

8.5. Loss Breakdown

Figure 8.7 shows the calculated loss breakdown of the hardware demonstrator with $L_{P,N}$ = 18.4μH at 11kW and 400-V nominal DC output voltage. The largest loss contributors are the HF semiconductors $S_{xp,nz}$ and the passive diode rectifier D_{xz}, each contributing to >25% of the total losses. The losses in $S_{xp,nz}$ are subdivided into half conduction losses and half switching losses. For the implemented partial hard-switching design, the turn-on losses are non-negligible and account to nearly 7% of the total losses. The total losses of all HF semiconductors amount to 43% of the total losses.

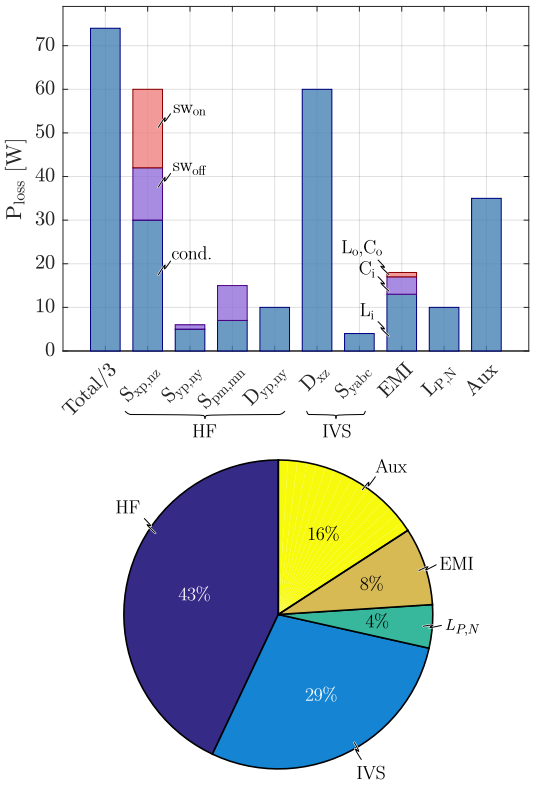

Figure 8.7: Calculated loss breakdown of the hardware demonstrator with $L_{P,N}$ = 18.4μH at nominal operation of 11kW with 220-V mains AC input voltage and 400-V DC output voltage. The auxiliary losses include PCB and wiring losses.

Compared to Figure 6.3, the conduction losses of D_{xz} are drastically increased. The reason for this increase is the fact that the hardware demonstrator is implemented with anti-series switches acting as precharge switches. These blocking switches are not necessary for the buck-type Prodrive-Select Rectifier, but are still present in the conduction path, adding an additional 20W to the total losses. The total IVS losses contribute 29% to the total losses and are the second largest share.

Further notable loss contributors are the EMI filter and auxiliary losses. The EMI filter losses contribute to 8% of the total losses and largely consist of the input EMI filter conduction losses. The auxiliary losses include the PCB and wiring conduction losses and account for 16% of the total losses. This is mainly due to the losses in the input and output conductors used to connect the measurement setup. The final loss contributors are the buck inductors $L_{P,N}$ that amount to just 4% of the total losses.

8.6. Summary

This chapter serves as a hardware demonstrator design specification and experimental verification of the modelling techniques. The hardware demonstrator is discussed in detail with a depiction in Figure 8.1 and a summary of the main converter components in Table 8.1. The reuse of certain converter elements results in a total system power density of 1.3kW/L, significantly less than the Pareto-optimal implementation of >2,9kW/L as specified in Chapter 6. A thorough volume breakdown details the contribution of the different converter components to the total hardware demonstrator volume. Furthermore, the measured component volumes are compared to the calculated Pareto-optimal volumes and critical design deviations are highlighted.

Efficiency and THD measurements are performed on the hardware demonstrator for an implementation with both $L_{P,N}$ = 18.4μH and $L_{P,N}$ = 200μH. A difference is observed as the small inductance variant performs better in overall system efficiency and stored inductor energy while the large inductance variant achieves lower input current THD. The modelling techniques of Chapter 5 are applied to the hardware demonstrator and show an accuracy in the efficiency calculation to the measured value of 0.12% at 11kW output power. The main sources of error in the models and the measurements are discussed and typical voltage and current waveforms of the 3L buck circuits are depicted. A loss breakdown of the hardware demonstrator with $L_{P,N}$ = 18.4μH is discussed in detail.

9 Conclusions

This research introduces a novel, three-phase buck-type PFC rectifier, named the Prodrive-Select Rectifier, applicable to function as the rectifying and power factor correcting stage of an on-board EV charging system. Furthermore, the buck-type PFC rectifier allows for a controllable DC output voltage which is lower than the wave-rectified three-phase line-to-line voltage. The research objectives include the description of the operating principle of the introduced topology, the modelling and design of an 11-kW variant of the PFC rectifier for on-board EV charging systems and the comparative evaluation of the introduced topology with similar three-phase, buck-type PFC rectifiers.

Relevant literature and background information is discussed with respect to three-phase buck-type PFC rectifiers, the third-harmonic current injection principle, the Swiss Rectifier and a zero-voltage switching method for MOSFET half-bridges. It is concluded that the Swiss Rectifier is not ideal for complete zero-voltage switching of the high-frequency semiconductors due to local minima in the inductor current envelopes. Subsequently, the circuit topology of the Prodrive-Select Rectifier is detailed which, in essence, functions similarly to the Swiss Rectifier. However, through the utilization of three-level buck circuits and a capacitive midpoint, the Prodrive-Select Rectifier allows for complete zero-voltage switching of the high-frequency semiconductors. The steady-state analysis of the Prodrive-Select Rectifier forms a mathematical basis for further modelling and design. The 3L buck circuit's conduction states, two modulation schemes and corresponding duty cycle calculations are thoroughly described.

A concise description of two proposed closed-loop control schemes and transient converter simulations in Simulink/PLECS support the previous theoretical analysis and suggest excellent dynamic performance of the Prodrive-Select Rectifier. A semi-analytical modelling approach with virtual prototyping routine is introduced to form the basis for subsequent Pareto-front generation and design optimization. An analytical Fourier switching cycle model is used for the derivation of converter electrical waveform descriptions. The main converter components, i.e. semiconductors, inductors, EMI filters, are separately modelled with a multi-physics approach. Finally, the component model outputs, i.e. component losses and volumes, are aggregated in order to provide a power density and efficiency performance calculation on a system level.

A global and component design space is determined for an 11-kW Prodrive-Select Rectifier with 230-V rms mains input and 400-V nominal DC output. The converter variables with the most impact on power density and efficiency are determined as the buck inductance, the switching frequency and the number of interleaved output stages. The execution of the proposed virtual prototyping routine leads to a performance space mapping and the distinction of a Pareto-front. It is concluded that a low inductance, high switching frequency design approach ensures the best performance trade-off for the on-board EV charging use-case. A Pareto-optimal, partial soft-switching design is identified and detailed, which utilizes interleaved output stages, 72kHz switching frequency and a buck inductance of 20μH. The Pareto-optimal design achieves a conversion efficiency of 98.3% and a power density of 2.9kW/dm^3.

In order to form an objective performance estimation, the Prodrive-Select Rectifier is compared to the Swiss Rectifier and the six-switch buck-type rectifier in terms of semiconductor stresses, semiconductor losses, inductor peak stored energy and normalized required attenuation. It is concluded that the Prodrive-Select Rectifier and the Swiss Rectifier have very similar performance in all aspects, resulting in near identical Pareto-fronts, while subsequently outperforming the six-switch buck-type rectifier.

The operating principle, control structure and modelling techniques are verified by an 11-kW, 1.3-kW/dm^3 hardware demonstrator with a buck inductance of $L_{P,N}$ = 18.4μH. Experimental results of the hardware demonstrator show an efficiency of 97.7% and 3.5% total harmonic distortion at full power 11-kW operation. The calculated full power efficiency, through the proposed modelling approach, shows a mismatch of +0.12% or +13W. Furthermore, measurement of the hardware demonstrator with $L_{P,N}$ = 200μH justifies the proposed design approach as it performs worse in system efficiency and inductor peak stored energy, but shows improved THD.

The three research objectives, as specified in Section 1.2, have been completed by providing mathematical analysis of the converter, developing an appropiate control scheme, identifying a Pareto-optimal converter design and comparing the Prodrive-Select Rectifier to similar PFC rectifiers, respectively. The design requirements of >98% system efficiency and >2kW/dm^3 power density, as specified in Table 1.1, have been met by the proposed Pareto-optimal design, but not by the hardware demonstrator.

9.1. Future Work

The main research objectives of this thesis are accomplished, but there still exists a number of research topics for future work. There are several subjects which were either ignored, briefly discussed or not anticipated throughout the duration of this research. Most prominently, the modelling of the converter components does not take certain electrical characteristics and parasitics behaviour into account. Summarized are a set of proposed future work topics.

- The switching loss model, as detailed in Section 5.5.2, is based on extracted datasheet parameters. Due to the placement of parallel capacitance across the MOSFET drain-source, these E_{on}/E_{off} curves are altered and expected to be the largest source of error in the calculated versus measured efficiency. Further elaboration of the switching loss models is needed in order to more accurately predict these losses during all MOSFET switching transients.
- During the experimental measurement phase of this research, it was deduced that the transitions between hard- and soft-switching of the hardware demonstrator during a line-cycle introduced a significant drop in the system gain, leading to system instability. Two remedial measures can be taken in order to achieve a stable system. Firstly, a dead-time compensation structure can be added to the closed-loop control structure. Ideally this is not based on a feed-forward implementation as is the case with the current hardware demonstrator. Secondly, a non-Pareto-optimal design implementation could be chosen which ensures complete soft-switching of the HF semiconductors, i.e. by utilizing smaller buck inductance or lower switching frequency, and prevents system instability.
- The hardware demonstrator consists of a considerable amount of reused components which leads to an implementation which does not represent the Pareto-optimal design and performs worse in terms of power density and efficiency. Consequently, it should be considered to build a prototype specifically designed for the Prodrive-Select Rectifier which more accurately demonstrates the expected state-of-the-art performance of the Pareto-optimal design.
- Furthermore, the performance space could be extended to include the total converter cost. Especially for industrial applications, searching for a cost-optimal implementation could be even more valuable than an efficiency or power density optimal implementation. Examples of multi-objective optimization of converter systems in a three-dimensional performance space of power density, efficiency and cost can be found in [19].

A

Appendix A

A.1. Steady-State Analysis

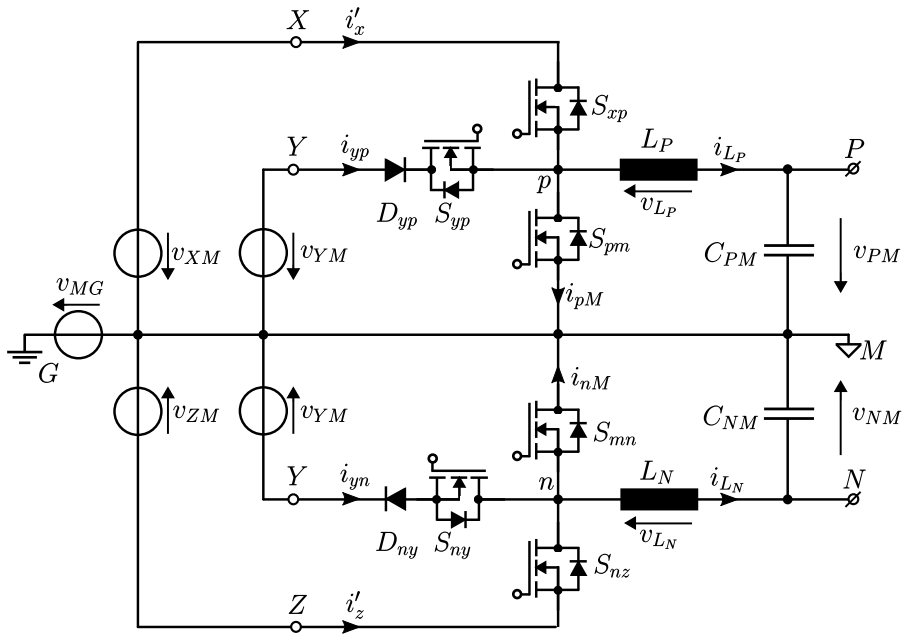

Figure A.1: Equivalent circuit model of 3L buck circuits referred to neutral point *G*.

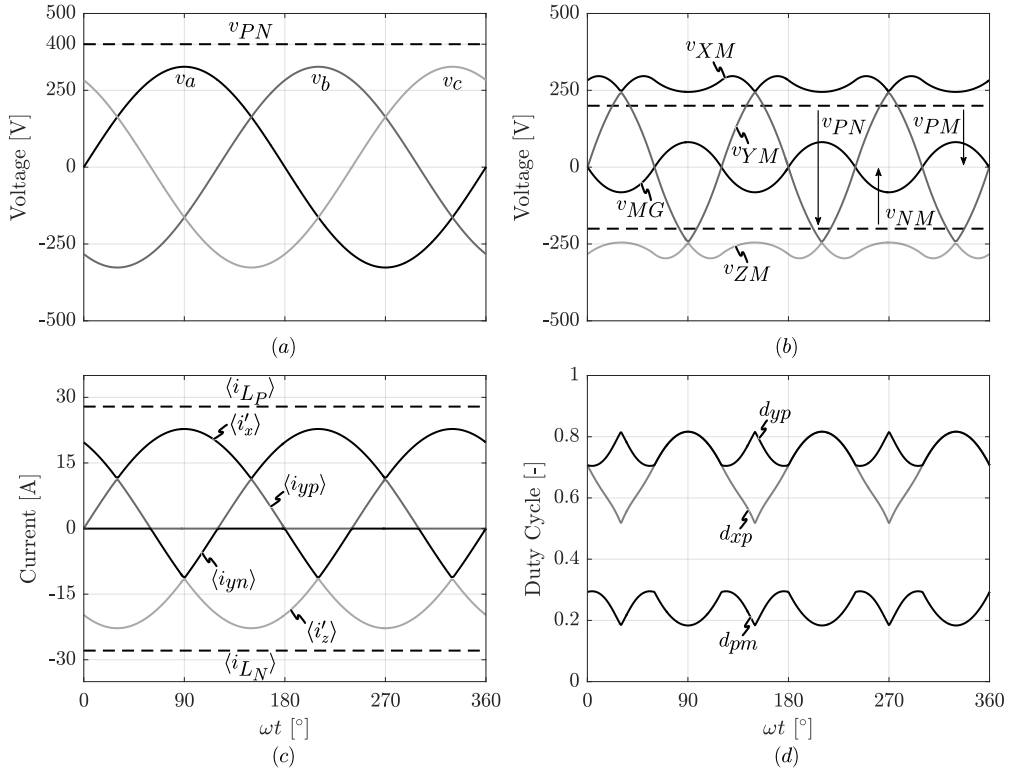

Figure A.2: Grid-cycle averaged waveforms of (*a*) three-phase grid and output voltage V_{PN} (*b*) 3L buck circuit input and output voltages (*c*) intermediate currents and inductor current and (*d*) duty-cycles for S_{xp} and S_{yp} under the assumption $v_{PM} = v_{NM}$ = constant.

A.2. Duty-Cycle Derivation

As derived in section 3.2.3:

$$d_{xp} = \frac{i_X}{i_o} \tag{A.1}$$

The output current can be described as:

$$i_o = \frac{P_o}{v_{PN}}$$

The single phase current amplitude can be described as:

$$i_{1ph,ampl} = \frac{2}{3} \cdot \frac{P_{3ph,i}}{v_{1ph,ampl}}$$

The current i_X can then be denoted as:

$$i_X = i_{1ph,ampl} \cdot \frac{v_{XM}}{v_{1ph,ampl}} = \frac{2}{3} \cdot \frac{P_{3ph,i} \cdot v_{XM}}{V^2_{1ph,ampl}} \tag{A.2}$$

Combining equations A.1 and A.2 gives an expression for d_{xp} as:

$$d_{xp} = \frac{2}{3} \cdot \frac{P_{3ph,i} \cdot V_{XM} \cdot V_{PN}}{V^2_{1ph,ampl} \cdot P_o}$$

Under the assumption that $P_{3ph,i} = P_o$:

$$d_{xp} = \frac{2}{3} \cdot \frac{v_{XM} \cdot v_{PN}}{v^2_{1ph,ampl}}$$

The same procedure can be used to derive the duty cycles for d_{yp}, d_{ny} and d_{nz}.

A.3. Supportive Figures

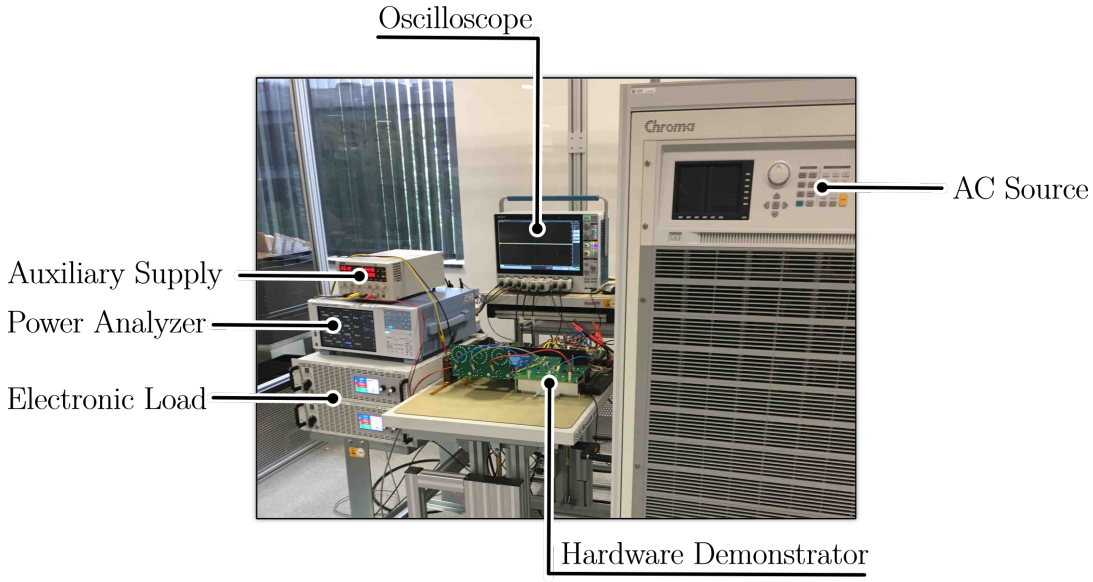

Figure A.3: Measurement setup of the hardware demonstrator for the Prodrive-Select Rectifier.

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