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A Scalable Isolated Gate Driver With Programmable Frequency and Duty Cycle for Series-Connected SiC MOSFETs

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ABSTRACT To enhance the voltage-handling capability of a switch, the series connection of switching devices is a cost-effective method that preserves many advantages of mature low-voltage devices. Dynamic voltage imbalance and electrical isolation for the devices at the high voltage (HV) side are two important challenges associated with series connection topology. Transformer-coupled gate drivers are excellent for providing both dynamic voltage balance and high galvanic isolation. However, they can only provide the switching function at the transformer pulse frequency. To generate complex waveforms of future power-electronics-dominated grids, a switch with user-defined turn-ON/OFF timing is required for testing grid assets under high-voltage conditions. This article presents a simple, cost-effective open-loop gate driver that overcomes this limitation by introducing two sets of complementary pulse transformers to initialize programmable frequency and duty cycle. Successful experimental verification of the series-connected SiC MOSFETs prototype is performed at 3.2 kV at various frequencies and duty cycles. The article also demonstrates that the measurement probes placed across series-connected MOSFETs significantly affect the voltage distribution and validate a compensation mechanism.

INDEX TERMS High-voltage switch, high-voltage testing, isolated gate driver, medium-voltage (MV) dc applications, series-connected SiC MOSFETs, voltage balancing.

NOMENCLATURE

C_c	Capacitance of Zener diode.
C_{compi}	Compensation capacitor for the ith MOSFET.
C_{ds}	Drain–source capacitance.
C_p	Parallel capacitance of probes.
C_{gs}	Gate-source capacitance.
C_{gd}	Gate-drain capacitance.
C_{iss}	Input capacitance of SiC MOSFET.
C_r	Compensation capacitance.
C_{rss}	Reverse transfer capacitance of SiC MOSFET.
C_{oss}	Output capacitance of SiC MOSFET.
C_{pac}	Dielectric capacitance due to heatsink.
C_{probe}	Capacitance introduced by probe.
C_{ps}	Dielectric coupling capacitance.
D	Junction dice size.
D_3	Schottky diode 3.
dV_{ds}/dt	Rate of change of drain–source voltage.
dV_{gs}/dt	Rate of change of gate–source voltage.
f_A	Oscillation frequency.
f_r	Resonance frequency.
k	Coupling coefficient.
L_r	Leakage inductance.
M	Mutual inductance.
MV	Medium voltage.
O.C.	Open circuit.
R_g	Gate resistance.

S.C.	Short circuit.
SiC	Silicon carbide.
V_C	Junction voltage.
V_{ds}	Voltage between drain and source.
V_{T+}	Upper threshold voltage.
V_{T-}	Lower threshold voltage.
V_{ds}	Drain-to-source voltage.
V_{gs}	Gate-to-source voltage.
C_{oss}	Output capacitance of SiC MOSFET.
ρ	Material resistivity.

I. INTRODUCTION

Due to the energy transition, more and more dc is being introduced in the power grid, not only at low voltage and (ultra) high voltage but also at MV levels [1]. Consequently, there is an increase in demand for high-frequency, high-voltage switching devices for dc MV grid applications. Higher efficiency and power density can be achieved by increasing the voltage-blocking capability of switching devices of a power converter [2]. Although there are custom-made SiC devices under test in research laboratories that go as high as 10 and 15 kV, however, the commercially available SiC MOSFETs can handle voltages up to 1.7 kV [3], [4]. Apart from the scarce availability, the excessive cost of these experimental high-voltage devices makes commissioning and maintenance in MV conversion applications quite challenging. More importantly, the gate-driving circuitry required to control these 10/15-kV SiC MOSFETs needs to be custom made as commercial-off-the-shelf gate-driving solutions fail to comply with the required high-voltage isolation requirement [4]. In addition, Hudgins et al. [5] show that the specific ON-resistance of power semiconductor switches increases exponentially as $R_{\text{ds-on}} \propto {V_B}^{2.3\sim2.5}$, where V_B is the device breakdown voltage. As a result, the current-handling capability of high-voltage SiC MOSFETs decreases quickly, which could make them unsuitable for large-capacity MV converters.

Above in view, making a high-voltage switch using commercially available mature low-voltage devices in series is one of the most effective topologies, which costs significantly less and provides higher efficiency [6]. Bolotnikov et al. [7] show that two or more series-connected MV devices attribute superior ON-resistance and higher density current compared with one individual higher voltage switch. Therefore, series-connected switching devices effectively increase the blocking voltage capabilities to answer application constraints above 1.7 kV.

With the ability to connect commercially available and mature but lower breakdown-voltage switches in series, MV converters can be built with a significant cost reduction. Even though commercially available insulated gate bipolar transistor (IGBTs) offer breakdown voltages up to 6.5 kV, their switching speed is limited. The chip area of SiC MOSFET is smaller in comparison with IGBT; it results in smaller parasitic capacitances and higher intrinsic switching speeds of SiC MOSFET [8]. That is why SiC MOSFETs excel in providing not only fast switching performance but also a significant reduction in form factor, which results in compacting the size of the converters. A comprehensive comparison among 1.2-, 2.2-, and 3.3-kV SiC MOSFETs presented in [7] reveals that the higher blocking voltage can be achieved with 1.2-kV SiC MOSFETs in series, as the safe operation of 2.2 kV/3.3 kV devices requires up to 45% derating, making 1.2-kV SiC MOSFET a better choice to be employed in series connection topology.

With the advantages offered by the high switching speed of SiC MOSFETs come two significant challenges of voltage imbalance and high-voltage isolation in series connection topology [9]. Transformer-coupled gate-driving techniques are effective in dealing with these difficulties but the method has a limitation of only being able to switch the series-connected stack of switches at the transformer frequency. The series-connected switches cannot be kept ON or OFF for a longer duration. There is a need for a scalable, cost-effective, and simple open-loop voltage-balancing gate driver with high galvanic isolation that can provide a user-defined ON/OFF function. The arbitrary switching function with variable ON/OFF time is especially essential for generating complex high-voltage waveshapes to test the grid assets for future power-electronics-dominated grids of renewable sources [10]. More importantly, a gate driver with programmable frequency and duty cycle will also enable the series-connected topology to be incorporated as a key building block beyond any typical 1.7 kV application. This will not only result in the mass integration of high-voltage switches in direct MV applications but will also bring a fast price reduction in the learning curve of MV to high-voltage converter technologies [11].

The advancements in wide-bandgap semiconductor technology have the potential to offer high-voltage switches up to 30 kV in the near future to implement MV converters without series connection and multilevel topologies [12]. However, the knowledge base of the series-connected MV switches will certainly open up new possibilities with the new generation of semiconductor switches beyond 30 kV in high-voltage applications [12].

For an extensive adoption of high-voltage series-connected MOSFETs in MV to high-voltage converter applications, it is crucial to select a voltage-balancing technique that is simple, easy to implement, and open loop since feedback networks increase the complexity in terms of design layout and isolation. A comprehensive literature review conducted on voltage-balancing techniques presented in [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], and [28] shows that the methods for dynamic and static voltage-balancing optimization can be broadly categorized into four main types: voltage clamping, passive balancing, active gate control, and gate current synchronization. Fig. 1 attempts to consolidate the voltage-balancing techniques and draws the reader's attention to the magnetically coupled gate-driving technique

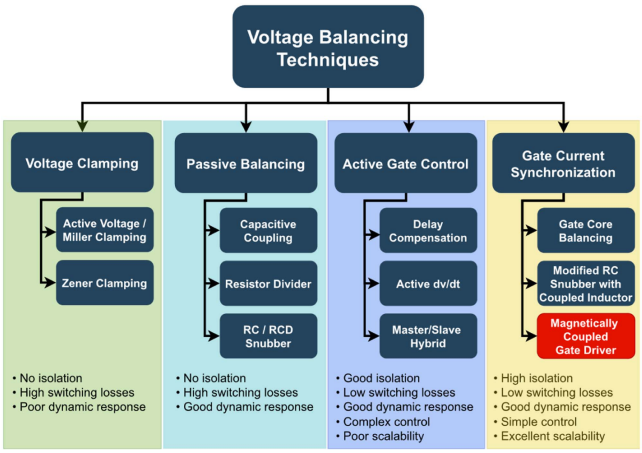


FIGURE 1. Overview of voltage-balancing techniques.

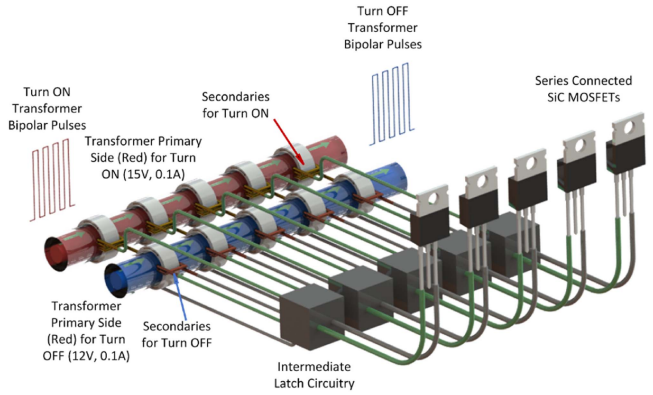


FIGURE 2. Concept demonstration—Pulse transformers (turn ON 15 V/0.1 A and turn OFF 12 V/0.1 A) arrangement with high-voltage-insulated cable passing through toroidal cores.

pursued in this article. A scalable magnetically isolated transformer-coupled gate-driving method is proposed in [29].

An analysis of gate driver architectures conducted by Zhao et al. [23] has shown that these magnetically isolated gate drivers provide a simple and economical solution for high-frequency applications (ranging from 2.5 to 50 kHz) with voltages exceeding 8 kV, particularly when an increased number of series devices is required [23]. In the transformer-coupled method, the gate current fed to each SiC MOSFET in series is synchronized with the help of a current transformer.

With a similar approach, high-voltage series-connected MOSFETs gate driver designs were presented in [30], [31], [32], [33], and [34] where pulse transformers were used to synchronously drive the series-connected SiC MOSFETs, and capacitive snubbers were employed to provide additional passive balancing.

The transformer-coupled gate-driving technique is excellent in scalability, enabling the connection of multiple SiC MOSFETs in series without substantial modifications to the gate-driving architecture. Scalability is achieved through transformer coupling, which ensures effective isolation of the high-side MOSFETs' floating source terminals from the single low-voltage primary-side wire loop, eliminating the need for complex-level-shifting circuits. The primary limitation to scalability lies in the insulation between the high-voltage source terminals and the low-voltage primary, as the insulation material must safely withstand increasing voltage levels. So for instance, with 30 series-connected MOSFETs at approximately 1 kV per MOSFET, the source terminal of the topmost device reaches 29 kV. The insulation material and transformer core design must safely handle this voltage difference without breakdown or degradation. As the number of series-connected MOSFETs increases, the thickness of the cable insulation grows to maintain safe isolation, and with that, the transformer core size must increase to accommodate the thicker insulation. However, advanced insulating materials, such as polyimide (Kapton), polytetrafluoroethylene (PTFE) (Teflon), and crosslinked polyethylene (XLPE), provide high dielectric strength ranging from 24 to over 300 kV/mm while maintaining durability and flexibility, enabling ultrathin insulation layers. These materials minimize the thickness of cable insulation and the size of the transformer core, ensuring compact yet effective high-voltage isolation. While parasitic losses also pose a limitation, the dominant factor remains the insulation requirements, which set the practical bounds of scalability.

However, with advantages, such as scalability, high-voltage isolation, and matching gate signal offered by transformer-coupled gate drivers, there are some limitations as well. Due to the inherent nature of transformer operation, these techniques have a constant frequency operation [30] with no control over programming the switching frequency and duty cycle. So, if for example, the series-connected MOSFETs stack needs to be kept ON for 10 ms and OFF for 90 ms, then the pulse transformers are unable to develop the required charge on the input capacitance C_{iss} of respective SiC MOSFET, as the discharge time constant of C_{iss} is in the order of few microseconds. Such variable ON/OFF time operation is especially desired in high-voltage dielectric testing of future power-electronics-dominated grid assets [10].

To resolve this dependency on the switching frequency of the pulse transformer, this article builds on the technique proposed in [35] by introducing two mutually exclusive transformers enabling the user-defined operation frequency and duty cycle of the series-connected SiC MOSFETs switch. The dual transformer concept is demonstrated in Fig. 2. The pulse transformers operate mutually exclusive to ensure a fail-safe transition.

The high-frequency design not only maintains the required charge on C_{iss} but also significantly reduces the size of the transformer to make the switch compact. The technique is validated through experiments at various frequencies and duty cycles. The article has elaborated on the technique's working principles and selection of components in detail.

Moreover, a recent transformer-coupled technique has employed additional passive snubber capacitors (660 pF) to limit

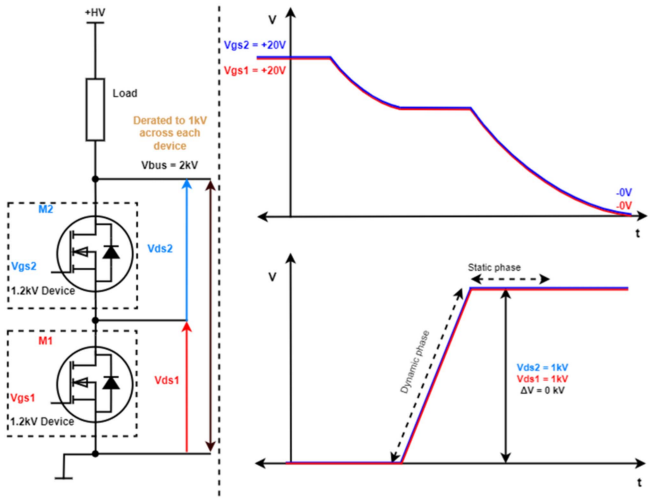


FIGURE 3. Ideal case of synchronous switching between series-connected SiC MOSFETs.

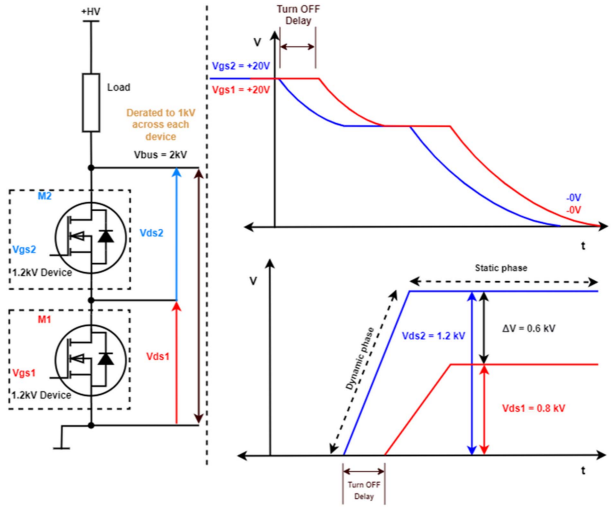


FIGURE 4. Asynchronous switching between series-connected SiC MOSFETs due to turn-OFF delay.

the dynamic voltage imbalance [30]. The technique presented in this article has demonstrated that, with matching gate signals, the need for passive capacitive snubbers is eliminated, and a nearly even voltage balance can be achieved. More importantly, the article has elaborated on the impact of probe-introduced impedances on the voltage imbalance that has not been reported before. This impact is necessary to be considered, especially while choosing snubber capacitor as wrong capacitance might result in dynamic voltage imbalance when the measurement probes are no more placed in the circuit. Subsequently, a compensation mechanism is presented to cancel probe influence during voltage measurement across series-connected switches to observe the correct voltage across the series-connected SiC MOSFETs.

The rest of this article is organized as follows. Section II briefly covers the challenges of equal voltage sharing among series-connected SiC MOSFETs, the most significant influencing voltage imbalance factors, and the research gap. Section III gives a detailed description of the new transformer-coupled gate current synchronization-driving technique with programmable frequency and duty cycle. Section IV presents the experiments, results, and observations. Finally, Section V concludes this article.

II. SERIES CONNECTION OF SIC MOSFETS

A. FACTORS AFFECTING VOLTAGE SHARING BETWEEN SERIES-CONNECTED SIC MOSFETS

In an ideal scenario, when synchronous gate signals are applied to the series-connected SiC MOSFETs, the voltage across the SiC MOSFETs should be equal at all times, as shown in Fig. 3. However, in reality, the voltage sharing is not equal across the individual switches in both static and dynamic phases. Stressing the semiconductor device over its rated breakdown voltage might result in permanent damage to the switch. Static phase imbalance can be easily resolved by placing a static resistor of megaohm values across drain–source terminals of the individual SiC MOSFETs [30]. Dynamic phase imbalance is, however, complicated with many variables involved. Dynamic voltage imbalance requires complex techniques for nearly equal voltage distribution among the series-connected MOSFETs [12].

There is a significant relation between gate-driving signal and dynamic voltage imbalance across drain–source terminals of series-connected SiC MOSFETs [2]. In general, there are two categories of asynchronous gating signals. The first category consists of the time delay between gate control signals for series-connected SiC MOSFETs, as depicted in Fig. 4. The gating signal of the top SiC MOSFET (in blue) turns OFF the switch M_2 quicker, resulting in an unequal voltage sharing between V_{ds2} (in blue) and V_{ds1} (in red). The dV_{ds}/dt slope defines the dynamic phase of the voltage sharing, while ΔV defines the difference in the static phase of the voltage sharing. Typically, a mismatch of a few nanoseconds (time delay) between gate signals for series-connected SiC MOSFETs can result in a difference of a few kilovolts across the individual device [36]. The next category of the asynchronous gating signals is distinguished in terms of the dV_{gs}/dt slope, as visualized in Fig. 5. Even if the control signals arrive at the respective gate terminal simultaneously, the time it takes to raise the gate voltage above the miller plateau voltage varies the V_{ds} response. This slope difference results in unequal voltage sharing in both static and dynamic phases [2]. These asynchronous gating signals are a significant contributor to the dynamic voltage imbalance problem, as only a 4-ns delay can result up to 40% voltage imbalance [2]. A few other factors also affect the voltage distribution. Fig. 6 shows the capacitive network that influences the balanced voltage distribution. The physical structure of an SiC MOSFET exhibits intrinsic parasitic capacitances, namely C_{gs} (gate–source), C_{gd} (gate–drain), and C_{ds} (drain–source).

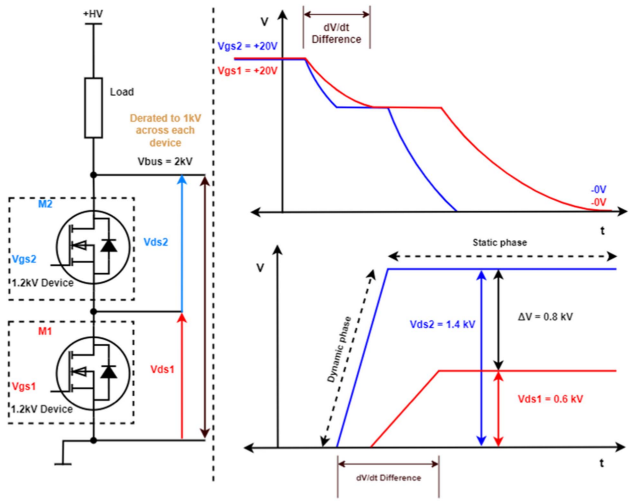


FIGURE 5. Asynchronous switching between series-connected SiC MOSFETs due to different in dV_{gs}/dt slope.

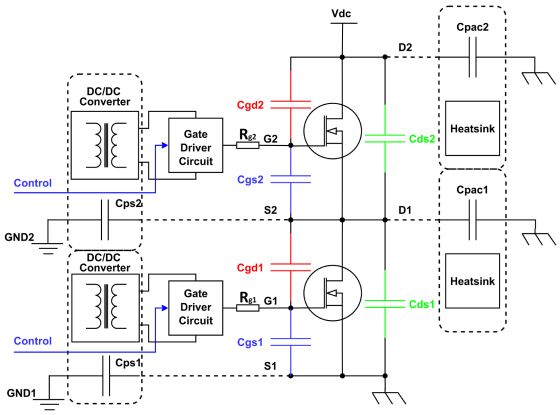


FIGURE 6. Potential parasitic capacitive contributors to unequal voltage sharing.

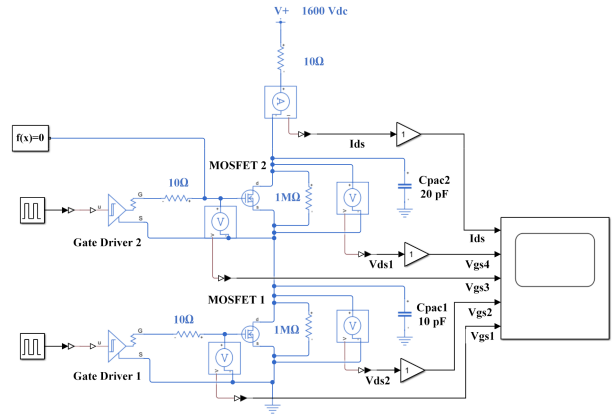


FIGURE 7. MATLAB simulation to evaluate the effect of intrinsic and extrinsic capacitance on voltage sharing.

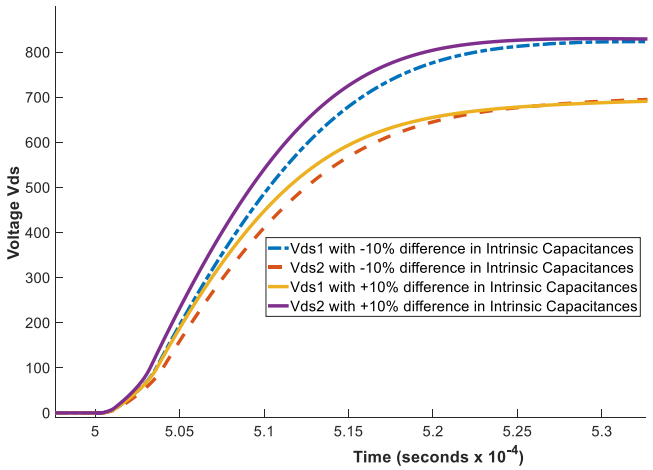


FIGURE 8. V_{ds} voltage distribution on two switches during turn-OFF due to a mismatch of 10% intrinsic capacitance.

Typically, in the datasheet of a MOSFET, the capacitance curves of said capacitances are not explicitly mentioned but are described as a graph of the following [37].

1) Input capacitance: $C_{iss} = C_{gs} + C_{gd}$.
2) Reverse transfer capacitance: $C_{rss} = C_{gd}$.
3) Output capacitance $C_{oss} = C_{gd} + C_{ds}$.

In addition to the intrinsic capacitive network, there are a few extrinsic capacitive couplings that influence equal voltage sharing across synchronously driven series-connected SiC MOSFETs [2]. The use of multiple dc–dc converters to drive high-side SiC MOSFETs is inevitable. The isolation transformers for the dc–dc converters exhibit dielectric couplings C_{ps1} and C_{ps2} referred to as common ground [38]. As can be seen in Fig. 6, both the control grounds (GND1 and GND2) and power grounds are shorted on the input side of the dc–dc converters. Moreover, to enhance heat conduction from the junction to the ambient, it is a common practice to mount device on a heatsink, which is earthed. Although SiC MOSFETs are electrically isolated from the heatsinks, the dielectric capacitances C_{pac1} and C_{pac2} are developed, which offer an alternative path for conduction current flowing through SiC MOSFETs [12]. The turn-ON and turn-OFF process of an SiC MOSFET is mainly the charging and discharging of these parasitic capacitances and the process variation or manufacturing defects define the deviation in the capacitance values for individual SiC MOSFETs [9], [39]. The general trend of the capacitance curves shows that the C_{iss} capacitance depends on the drain–source voltage V_{ds} mainly because C_{gd} varies with V_{ds} [37].

To test the effect of the process variation on voltage sharing, a MATLAB simulation, as shown in Fig. 7, is performed where C_{gs}, C_{gd}, and C_{ds} are the intrinsic capacitances that undergo $\pm 10\%$ parametric sweep without any difference in gating signals. It is pertinent to mention that these intrinsic capacitances are nonlinear, and their values with voltage variation are simulated as per graphs given in SiC MOSFETs datasheet [37]. Furthermore, to study the effect of the extrinsic capacitances, 10 and 20 pF capacitors are introduced across the drain–source terminal of each series-connected SiC MOSFETs. The results for the parametric sweep simulation are presented in Figs. 8 and 9, which clearly show that the 10%

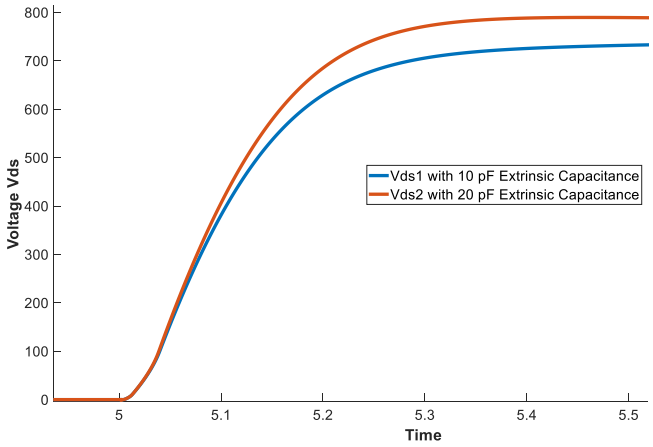


FIGURE 9. V_{ds} **voltage distribution on two switches during turn-OFF due to the presence of different extrinsic capacitances.**

variation in both static and dynamic phases of the V_{ds} voltage is comparatively less significant compared with the imbalance created by the gating signal mismatch mentioned before.

To conclude, the overall factors influencing voltage balancing across series-connected SiC MOSFETs are summarized as follows.

1) Gate signals difference introduced by the gate driver circuit and associated power supply.
2) Process variation in intrinsic parasitic capacitances (C_{gs}, C_{gd}, and C_{ds}).
3) External capacitance to ground introduced by the heatsink or dc–dc converters (C_{ps} and C_{pac}).
4) Difference in gate resistances (R_g).
5) Parasitic inductance introduced by the interconnects between series-connected devices.

With the findings from the preliminary simulations and study [12], the gate signal mismatch is one of the most significant causes of the voltage imbalance. The extrinsic capacitances can be minimized using the multistep packaging approach presented in [12]. The intrinsic tolerances of the above-mentioned variables can be minimized by sorting and careful selection of components from a single production batch where the process variations would be minimal [23], [40].

B. CHALLENGES ASSOCIATED WITH THE GATE-DRIVING CIRCUIT

In a series connection, all stacked devices are considered as high-side MOSFETs apart from the bottom-most MOSFET, as their respective source terminals are floating on the drain of the lower adjacent MOSFET. The bottom-most MOSFET is referred to as low-side MOSFET, as its source terminal is referred to both control and power grounds. One commonly employed solution is creating a floating power supply using an isolated dc–dc converter. However, this technique has a limitation, as to cascade multiple high-side devices, multiple dc–dc converters and external gate control signals must be

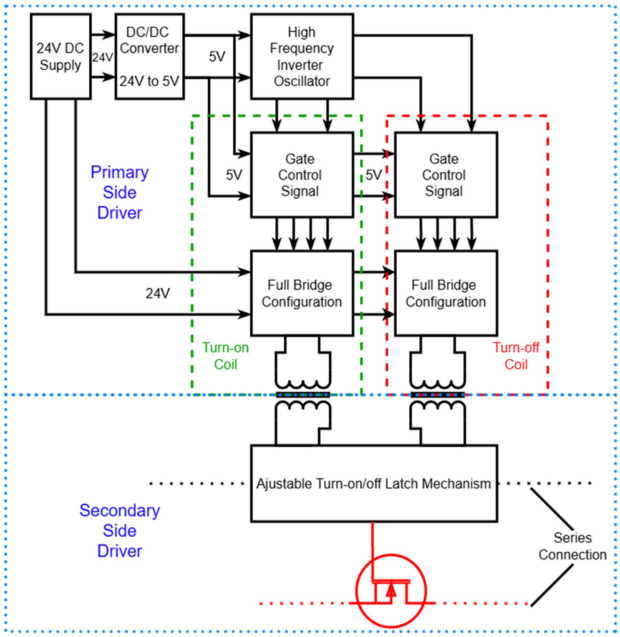


FIGURE 10. **Block diagram for the proposed scheme.**

used. These additional components bring various start-up and propagation delays, which again create the timing delay of the gate signals limiting the ability to switch the series-connected SiC MOSFETs synchronously. An alternate nonisolated gate driving integrated where the floating power supply for the high-side MOSFET is generated by bootstrapping a charged capacitor, which floats on the source. However, this technique also has limitations as the level shifter mechanism introduces a propagation delay, and high-voltage transients can easily reach the blocking capacity of the bootstrap diode and permanently damage the control circuitry and its peripherals.

III. GATE CURRENT SYNCHRONIZATION-DRIVING TECHNIQUE WITH PROGRAMMABLE DUTY CYCLE

A. CIRCUIT DESCRIPTION AND OPERATION

To resolve the aforementioned limitations, a gate current synchronizing driver with a programmable frequency and duty cycle for series-connected SiC MOSFETs is designed with a transformer-coupled system to achieve synchronous switching and high-voltage isolation. Fig. 10 shows the block diagram of the proposed gate driver design, broadly divided into primary- and secondary-side drivers. On the primary side, there are two single-turn high-voltage-insulated turn-ON/OFF loops driven with ±24 V bipolar pulses using full-bridge converters. The turn-ON and turn-OFF coils are driven complimentary to each other. The secondary-side driver includes an adjustable turn-ON /OFF latch mechanism for arbitrary switching functions for the SiC MOSFETs connected in series. Each series-connected SiC MOSFET will have its own two secondary coils, one for turn-ON and the other for turn-OFF and latch mechanisms. The power required for the gate control is fed

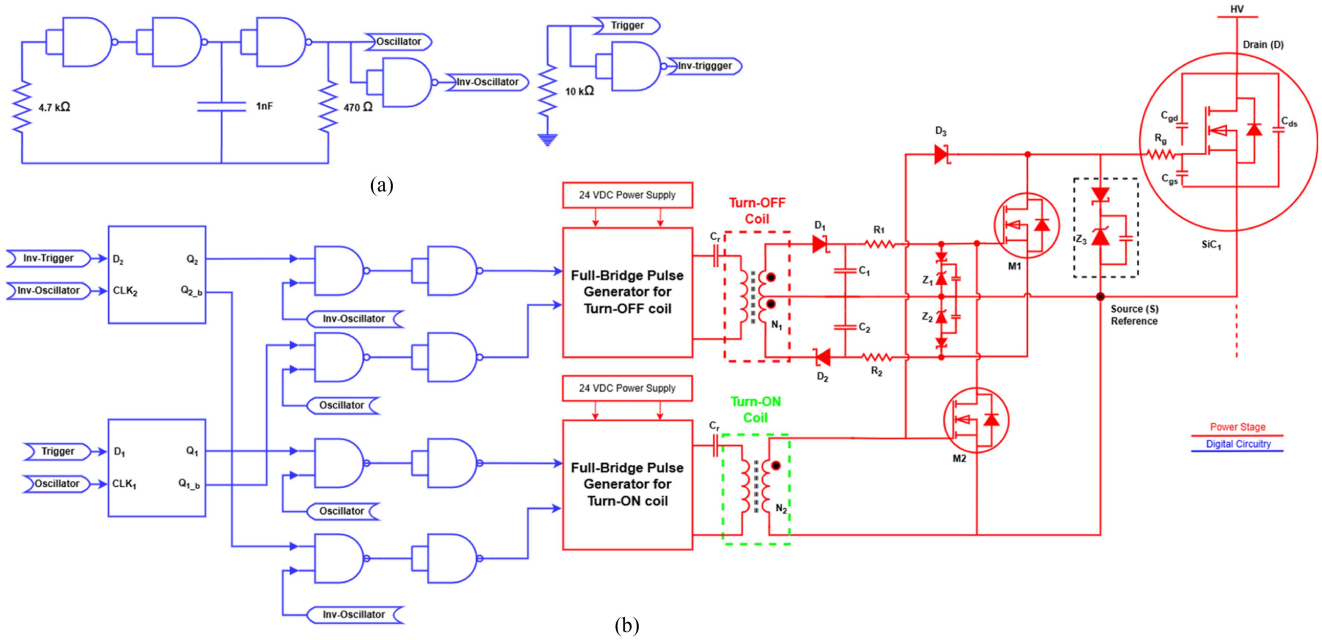


FIGURE 11. (a) Oscillator circuit. (b) Gate current synchronization-driving circuit with programmable frequency and duty cycle.

externally from a 24 V_{dc} power supply. An onboard nonisolated dc–dc converter generates a 5-V logic power supply to power up the respective digital control circuitry. The circuit operation starts from the primary side of the circuit with the oscillator, as shown in Fig. 11. Fig. 12 shows the corresponding timing diagram illustrating the modulation process to generate respective gate control pulses for the full-bridge pulse generator. The user-defined digital turn-ON and turn-OFF signals are modulated and converted into two streams of mutually exclusive pulses. These streams work together on the primary side to drive the full-bridge converter, generating ±24 V bipolar voltage pulses across the single-turn high-voltage turn-ON loop during the entire period of the ON-signal. The turn-OFF coil remains inactive during this time. The turn-OFF digital signal is converted to drive the full bridge in a similar way across the single-turn high-voltage turn-OFF loop and the other coil remains inactive during this period.

On the secondary-side driver section, a small-signal MOSFET latch facilitates controlling the switching frequency and duty cycle of series-connected SiC MOSFETs, irrespective of the frequency at which the pulse transformer is driven. The turn-ON/OFF latch mechanism consists of two secondary windings wound on two toroidal cores and two low-voltage signal MOSFETs M_1 and M_2, for each series-connected SiC MOSFET. During turn-ON, a half-wave rectifier is constructed with Schottky diode D_3 and C_{iss} capacitance of SiC MOSFETs, which is clamped at 15 V with Zener diode Z_3 as recommended in [37] to drive the SiC MOSFET with a recommended voltage of +15 V for optimum switching performance. A small-signal MOSFET used for M_2 is driven directly with the transformer's bipolar voltage. When the turn-ON coil is energized, the drain of the M_2 transistor ensures that the capacitor C_1 is discharged and transistor M_1 cannot turn ON. Similarly,

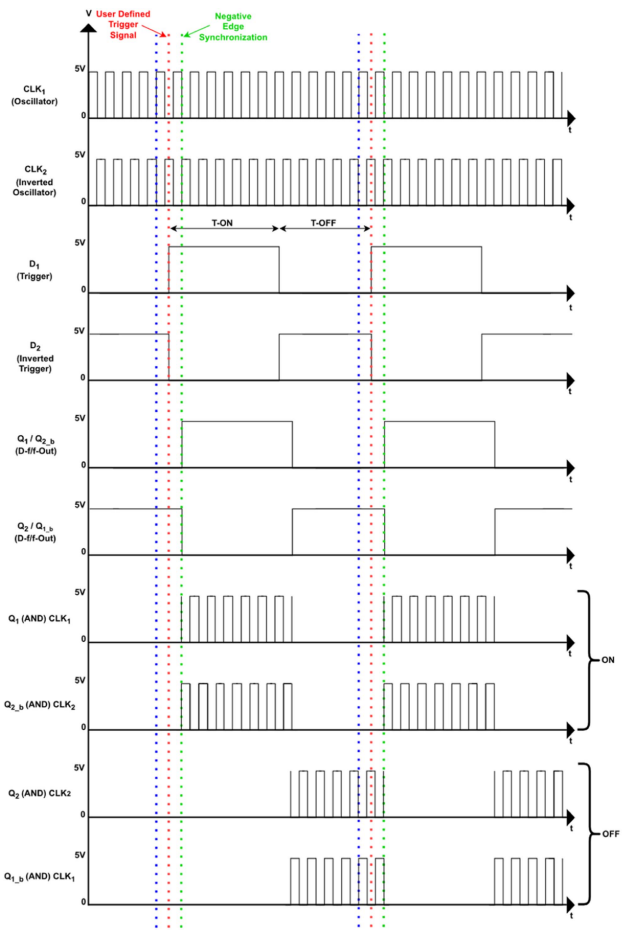


FIGURE 12. Detailed timing diagram for circuit, as presented in Fig. 14, where user-defined ON and OFF trigger signals are modulated over 167 kHz complementary digital signals to drive the coil between the full-bridge circuits.

when the turn-OFF coil is energized, the gate of the SiC MOSFET is pulled to negative potential to avoid the false turn-ON of SiC MOSFETs in series.

The turn-OFF coil is designed as a center-tapped secondary to generate a dual polarity supply. During turn-OFF, two half-wave rectifiers are constructed with the help of Schottky diodes connected with a center-tapped transformer. The center tap of the transformer is connected to the midpoint of the split capacitor arrangement. Zener diode Z_1 is selected with a reverse breakdown potential of 12 V connected to the gate of M_1, whereas Zener diode Z_2 has a 4.7 V reverse breakdown voltage connected to the source of M_1. This configuration subjects the gate of the SiC MOSFET during turn-OFF to negative voltage instead of ground to better extract charges from gate capacitance C_{iss}. The turn-ON and turn-OFF coils are energized in a mutually exclusive fashion, and the latch mechanism is achieved.

Zener diodes are typically used in reverse bias for voltage clamping, with their p–n junction acting as a capacitance that decreases with increasing reverse voltage until the Zener breakdown point, where it stabilizes [41]. At high frequencies (around 100 kHz) with fast switching speeds (10 μs), this capacitance can distort the diode's behavior. To improve clamping, a Schottky diode and a shunt capacitance are added, allowing efficient clamping without the charging/discharging of the Zener diode's capacitance, as highlighted in the black box in Fig. 11(b) [41].

B. OPERATIONAL MODES

Fig. 13 describes the turn-ON mode of the switch and highlights the components responsible for turning ON the series-connected SiC MOSFETs. The blue measurement probes direct the reader to follow the timing diagram, as shown in Fig. 15. The positive half pulse propagates through diode D_3 and clamped by Zener diode Z_3 at +15 V, charges the gate capacitance C_{iss} of the main series-connected SiC MOSFET SiC_1 to gate voltage V_{gs3}, as shown in Fig. 13(a). As soon as the input voltage becomes equal to or less than the gate voltage V_{gs3}, the diode D_3 becomes reverse biased and stops the flow of charge across the gate–source terminal from draining. The diode remains in reverse-biased mode during the negative half cycle and becomes forward biased as soon as the input voltage becomes greater than the gate voltage V_{gs3} of the SiC_1 MOSFET, as shown in Fig. 13(b). The SiC_1 MOSFET during this whole period remains ON. At the same time, this positive half cycle of the transformer pulse turns ON the small-signal MOSFET M_2, which drains the gate charge of M_1 to keep it OFF. It is pertinent to mention that once the gate capacitance is fully charged, the main SiC MOSFET is fully turned ON, and the gate capacitance behaves like an open circuit. However, since a very small leakage current still flows through the gate–source terminal, the next positive pulse replenishes this tiny loss, and a very little current flows through the circuit during the subsequent positive pulses.

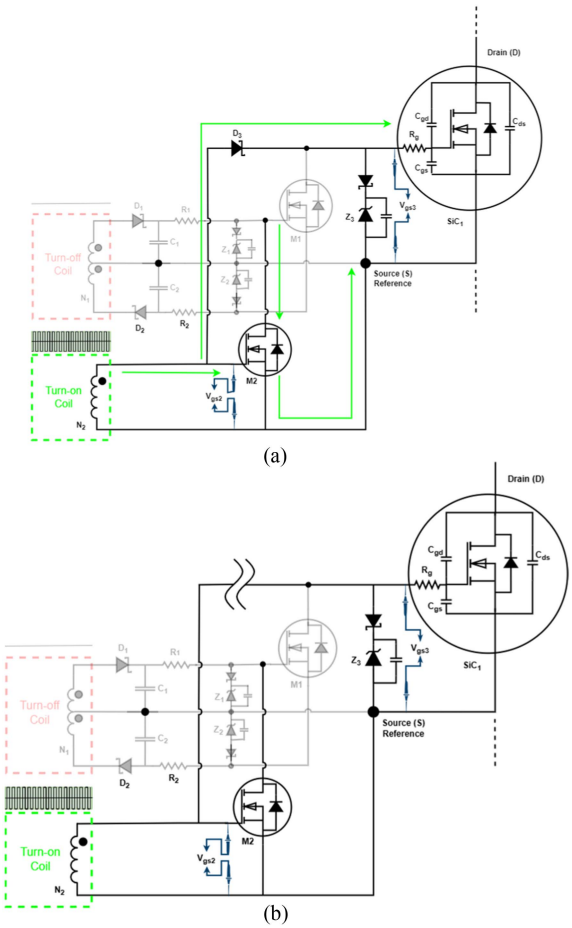


FIGURE 13. Illustration of the turn-ON mechanism for series-connected SiC MOSFETs, highlighting M_2's role in synchronizing with SiC_1 and controlling M_1, with D_3 charging C_{iss} to switch SiC_1 ON, and timing diagram correlation with Fig. 15. (a) Circuit during positive half voltage pulse. (b) Circuit during negative half voltage cycle.

Similarly, Fig. 14 depicts the active components of the secondary-side driver circuit during the turn-OFF phase of the series-connected SiC MOSFETs. The positive half cycle across the turn-OFF secondary propagates through diode D_1 and clamped by Zener diode Z_1 at +12 V, and charges the gate capacitance C_{iss} of the small-signal MOSFET M_1 to gate voltage V_{g1}, as shown in Fig. 14(a). The only difference with the turn-ON coil during turn-OFF is that a center tap transformer configuration is used that allows the negative half of the secondary voltage to propagate through diode D_2 clamped by Zener Z_2 at −5 V and establish a negative voltage across the source terminal of the small-signal MOSFET M_1 during the negative half cycle. This topology generates a dual polarity supply from the turn-OFF coil across capacitors C_1 and C_2 switching the small-signal MOSFET M_1 to ON-state. The drain–source path of this MOSFET discharges the stored gate charge across the main SiC MOSFET SiC_1. The negative polarity at the source terminal of M_1 is generated to pull down and better

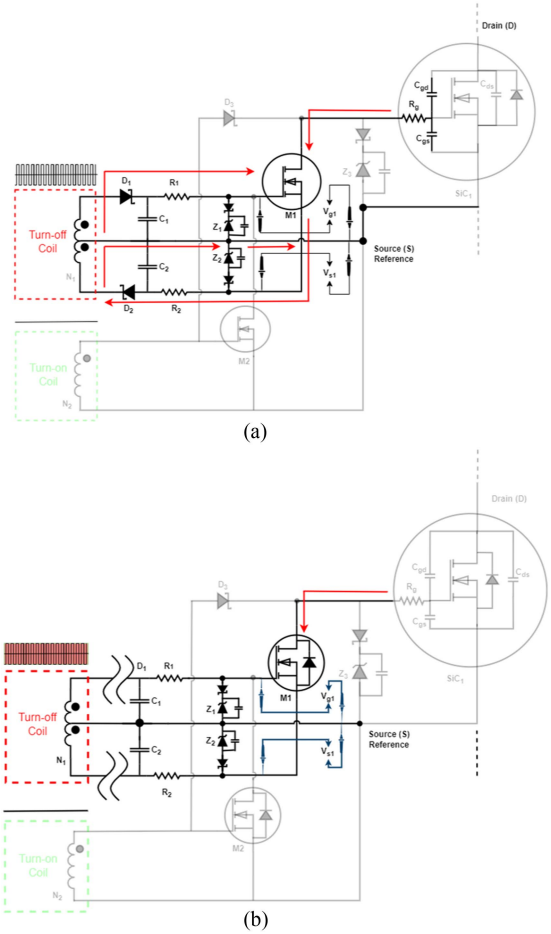


FIGURE 14. Active components in the secondary driver circuit during turn-OFF phase, illustrating dual polarity supply generation and timing diagram correlation with Fig. 15. (a) Circuit during positive half voltage pulse. (b) Circuit during negative half voltage cycle.

extract the stored charge switching the main SiC MOSFET SiC_1 to OFF-state.

This whole cycle is synchronously executed across all series-connected SiC MOSFETs, providing them with matching gate voltages and switching them at the same time ensuring nearly even voltage distribution among them all.

C. TEMPORAL ANALYSIS

The timing diagram of the voltage waveforms is shown in Fig. 16. The circuit has two dynamic phases and two steady-state conditions during turn-ON and OFF. Positive waveforms, as shown in Fig. 16(a), are both similar for turn-ON and turn-OFF coils. However, the negative waveform, as shown in Fig. 16(b), is only for the turn-OFF coil, which has a center-tapped transformer configuration. Moreover, for the turn-OFF coil, the voltage waveforms and corresponding timings (t_0–t_7) in Fig. 16(a) and (t_8–t_{12}) in Fig. 16(b) are occurring at the same time.

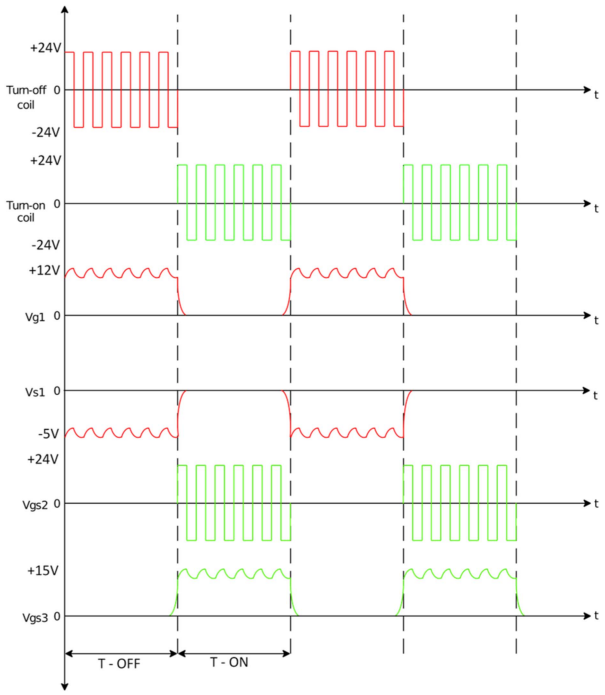


FIGURE 15. Voltage waveforms for the functional schematic, as presented in Figs. 13 and 14.

1) 0–T_0

From 0 to t_0, the voltage rises on the secondary side of the transformer to the miller plateau. The gate starts charging at this instant and the MOSFET turns ON after crossing the threshold voltage V_{th}.

2) T_0–T_1

From t_0 to t_1, the secondary voltage increases and is clamped by the Zener diode. The gate capacitance C_{iss} is charged, and the gate voltage V_{gs} reaches the clamped secondary voltage. The diode allows charges to flow in the forward direction only during this time period.

3) T_1–T_2

The circuit enters the steady state and, during this time period, very little charge flows since the gate capacitance is fully charged. The gate voltage V_{gs} is maintained at a steady level by Zener diode.

4) T_2–T_3

When the secondary voltage drops below the gate voltage, the top diode enters reverse bias, halting charge flow in the opposite direction and maintaining the gate voltage. This sudden diode turn-OFF stops the current flow, creating a negative electromotive force that causes a sharp voltage drop and oscillations due to the inductance of the turn-ON transformer and the circuit's capacitances. The circuit in this state behaves like an open circuit. Although the gate–source resistance is in the megaohms range, a very little gate leakage current is still able

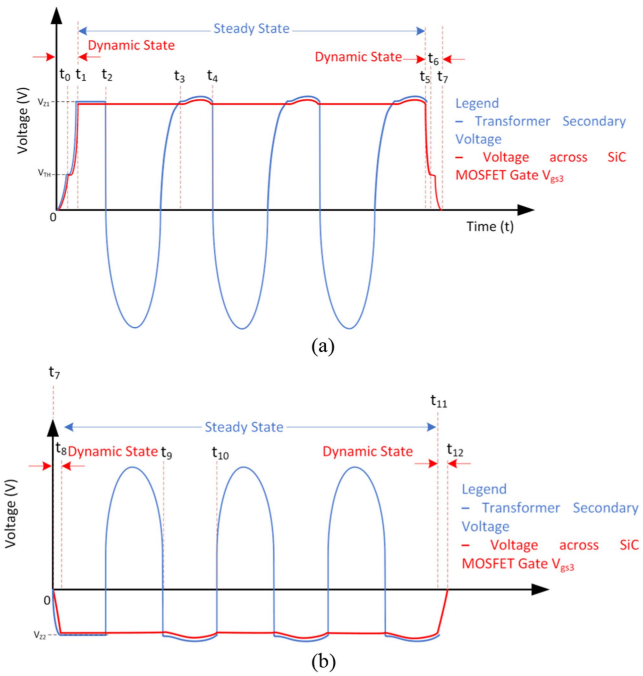


FIGURE 16. **Voltage waveform profiles across secondary and across SiC MOSFET gate. (a) Voltage waveforms across the gates of MOSFETs connected on secondaries. (b) Voltage waveforms across the lower half of the turn-OFF secondary coil.**

to flow during this short duration, but this current is too small to result in any significant loss of gate voltage.

5) T_3–T_4

When the next positive pulse reaches above the gate voltage, the diode is forward biased again to allow very little charge to flow again to replete the charge lost during the second phase of the cycle. As a result, a small ripple appears on top of the gate voltage in line with secondary voltage signal. This ripple can be minimized by increasing the transformer switching frequency to ensure fast replenishment of the gate charge and minimize the discharge.

6) T_4–T_5

The circuit enters the steady state.

7) T_5–T_6

The circuit enters the dynamic state of turning OFF from t_5. At this instant, the MOSFET M_1 turns ON and provides path to extract charges from the gate of main SiC MOSFET. It reaches to threshold voltage V_{th} and the main SiC MOSFET turns OFF below this voltage.

8) T_6–T_7

From t_6 to t_7, the gate charge continues to drop and the gate voltage comes down to zero.

TABLE 1. ***LCR*** **Meter Measurements for Computing Coupling Coefficient**

N_1	N_2	L_1(μH)	L_2(μH)	k	$L_1(O.C.L_2)$	$L_1(S.C.L_2)$	M(μH)
1	1	0.3	9.04	0.426	10.09	8.75	0.7
	2		20.7	0.454	10.55	8.38	1.13
	3		30.8	0.423	10.3	8.45	1.28
	4		55	0.436	10.5	8.5	1.77
	5		76	0.433	10.4	8.45	2.07

9) T_7–T_8

The voltage on the lower half of the center-tapped secondary side rises and is clamped at −5 V by the Zener diode across the source terminal of the turn-OFF MOSFET M_1 with respect to the ground.

10) T_8–T_9

The circuit enters the steady state, and this negative voltage ensures better charge extraction from the gate of the main SiC MOSFET that is connected to the drain of turn-OFF MOSFET $M1$ during the OFF cycle.

11) T_9–T_{10}

The charge is replenished again during this phase, and a small negative ripple appears.

12) T_{11}–T_{12}

The turn-OFF coil stops getting the transformer pulses, and the negative voltage goes down to the ground during this phase.

D. TRANSFORMER DESIGN

The selection of the transformer toroidal core can be determined using the following equations:

$$A = \frac{E}{k\, f\, B_m N_p} \tag{1}$$

$$B = \frac{LI}{NA} \tag{2}$$

$$L = \frac{BNA}{I} \tag{3}$$

where A is the area of the toroidal core, B is the magnetic flux density, E is the voltage, f is the transformer operating frequency, I is the current, k is the form factor, L is the inductance, and N_p is the number of turns on the primary side. Based on equations (1)–(3), a suitable toroidal core (part number TX13/7.9/6.4-3C90) was selected [42]. Minimizing the number of turns in the transformer is important as it directly correlates to the leakage inductance. Therefore, one turn is selected for the primary-side coil to minimize leakage inductance. A simulation of the coupling coefficient between a high-voltage-insulated loop and secondary windings wound on toroidal cores has been performed on an finite element modelling (FEM)-based ANSYS Maxwell 3-D model, as shown in Fig. 17. The computed coupling coefficients are verified with open-circuit (O.C.) and short-circuit (S.C.) tests using a keysight U1733C *LCR* meter. Table 1 demonstrates the results for performed O.C./S.C. tests, and the coupling

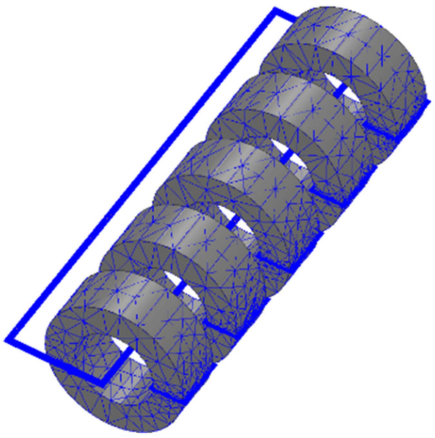


FIGURE 17. Meshing in the finite element modelling (FEM) simulation of the transformer using ANSYS Maxwell 3-D.

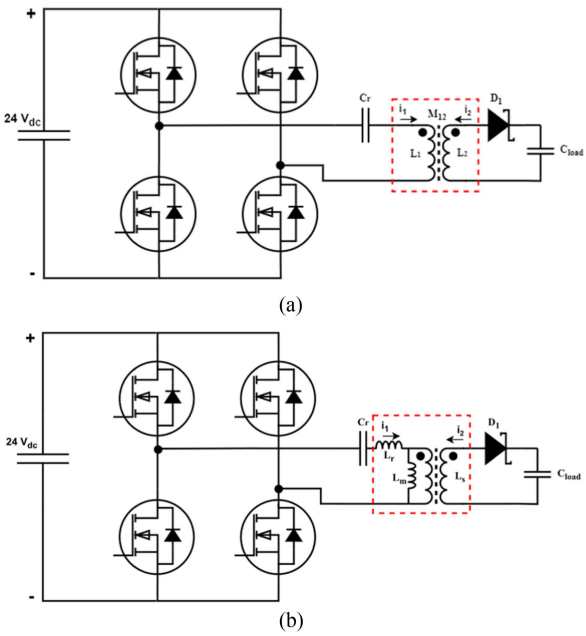


FIGURE 18. (a) Transformer circuit with self- and mutual inductances. (b) Equivalent circuit to calculate primary-side compensation capacitor for high-voltage loop [45].

coefficient is computed as follows [43], [44]:

$$k = \sqrt{1 - \frac{L_1\,(S.C.L_2)}{L_1\,(O.C.L_2)}} = \frac{M}{\sqrt{L_1 L_2}}. \tag{4}$$

The number of turns of the secondary coils must also be minimal to reduce the leakage inductance. With calculated coupling coefficients, the minimum number of turns that can produce a voltage above the gate threshold (+15 V for SiC MOSFETs) is 2. Therefore, turns for the secondary side are selected to be 2. Since the turn-OFF coils have small-signal MOSFETs, which can be switched at 12 V, the turn-OFF coil is also given two turns with a center tap. This configuration creates a circuit symmetry.

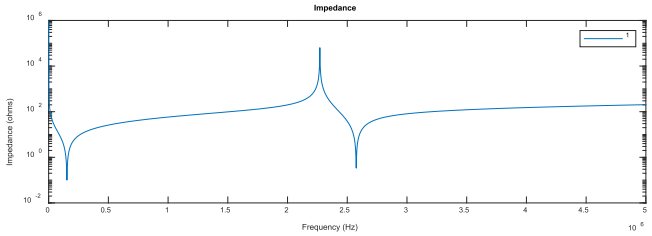


FIGURE 19. Impedance profile of the proposed *LCLC* circuit.

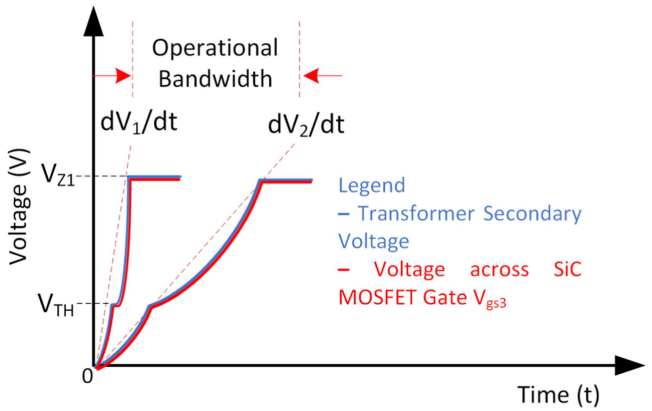


FIGURE 20. Rising voltage waveform bandwidth profile.

TABLE 2. V_{ds} Measurement Across Each Series-Connected SiC MOSFET

S No.	Drain-Source Voltage	Value Observed	%age deviation
1.	V_{ds1} (Bottom most MOSFET)	800.1 V	~ 0%
2.	V_{ds2}	803.5 V	~ 0.4375%
3.	V_{ds3}	790 V	~ 1.25%
4.	V_{ds4}	794.5 V	~ 0.8125%

The circuit mainly consists of a transformer with a primary and secondary side, each with specific reactive components (inductances and capacitances). The primary side of the transformer has a self-inductance L_1 in series with a compensation capacitor C_r, forming an LC circuit. The secondary side has a self-inductance L_2 in series with a rectifier diode and a capacitive load C_{load}, which is the gate capacitance C_{iss} of the MOSFET. Together, this network forms an $LCLC$ (inductor–capacitor–inductor–capacitor) circuit with two resonant frequencies, one on the primary side and another on the secondary side.

A simplified circuit diagram of the compensation network and its equivalent circuit model is presented in Fig. 18. The analysis is for the time period that the diode is conducting, and hence, we can consider it as a short circuit with a voltage drop only. In typical transformer designs, inductance on the primary side is compensated with a capacitor in order to minimize reactive impedance. The value of compensation capacitor C_r can simply be determined using the following equation [45]:

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{5}$$

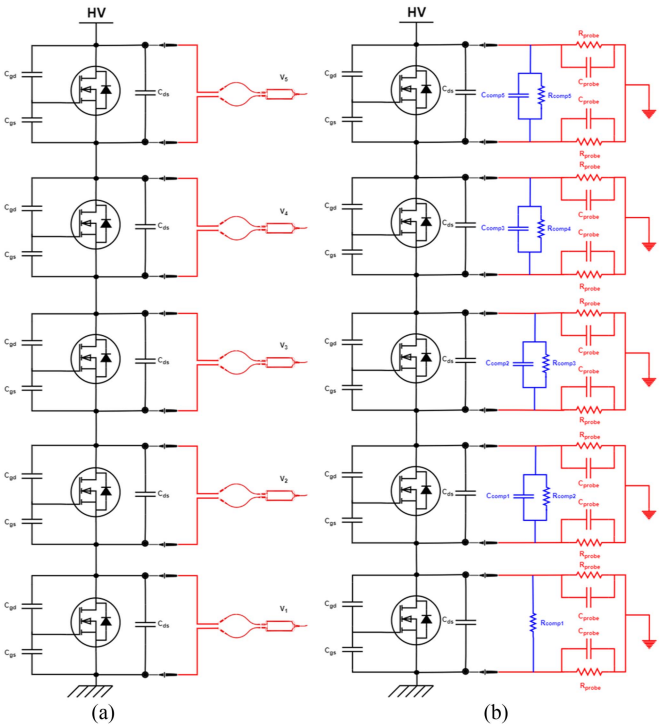


FIGURE 21. **(a) Circuit diagram for four SiC MOSFETs in series with differential probe placement. (b) Circuit diagram for four SiC MOSFETs in series with probe-introduced impedances and *RC* compensation.**

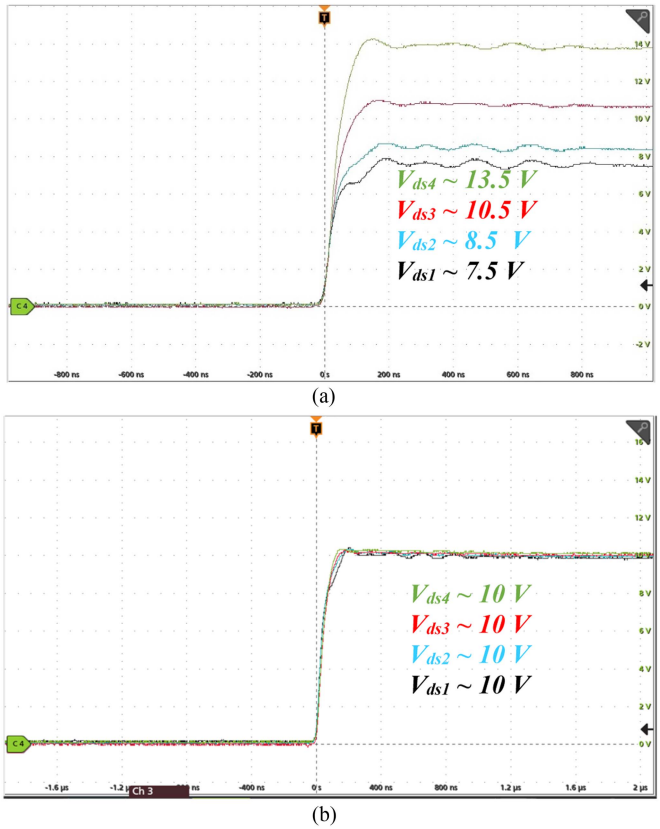


FIGURE 22. **(a) Drain-to-source (V_{ds}) voltage across four SiC MOSFETs in series during turn-OFF with no probe compensation. (b) Drain-to-source (V_{ds}) voltage across four SiC MOSFETs in series during turn-OFF with probe compensation.**

where f_r is the resonance frequency, $L_r = L_1$ when L_2 is open circuited (refer to Table 1), and $L_m = L_1 - L_r$.

The total impedance of the circuit, considering the transformer coupling and both resonance frequencies, can be analyzed by modeling the equivalent impedance on the primary side

$$Z_{\text{eq}} = \frac{V_{\text{in}}}{I_{\text{in}}} \tag{6}$$

where Z_{eq} represents the effective impedance seen by the source at the primary side. This impedance is a function of the primary inductance L_1, compensation capacitor C_r, and the reflected impedance of the secondary side through the transformer coupling. The secondary circuit's impedance, reflected to the primary side, is given by

$$Z_{\text{Ref}} = \frac{Z_{\text{secondary}}}{n^2} = \frac{1}{j2\pi f_{\text{secondary}} C_{\text{load}} n^2} \tag{7}$$

where $Z_{\text{secondary}}$ is the impedance of the secondary circuit and $n = \sqrt{\frac{L_1}{L_2}}$ is the turn ratio of the transformer. The total effective impedance at the primary side is

$$Z_{\text{eq}} = j\omega L_1 + \frac{1}{j\omega C_r} + Z_{\text{Ref}}. \tag{8}$$

The values of L_1, C_r, L_2, and C_{load} determine the operational characteristics and resonance conditions of the circuit. The primary side consists of an inductance L_1 and a compensation capacitor C_r. The resonance frequency of the primary side is determined by the following formula:

$$f_{\text{primary}} = \frac{1}{2\pi\sqrt{L_1 C_r}}. \tag{9}$$

This frequency f_{primary} can be adjusted by selecting appropriate values for C_r, making the primary side resonate at the desired frequency. The secondary side is connected to a rectifier diode and a capacitive load C_{load}, which represents the gate capacitance C_{iss} of the MOSFET. The secondary self-inductance L_2 resonates with the capacitive load C_{load}. The resonant frequency for the secondary side is given by

$$f_{\text{secondary}} = \frac{1}{2\pi\sqrt{L_2 C_{\text{load}}}}. \tag{10}$$

The gate capacitance C_{iss} is typically small, leading to a relatively high resonance frequency on the secondary side. When the circuit operates at or near the primary resonance frequency f_{primary}, the primary LC circuit becomes resonant, allowing maximum current to flow through the primary winding of the transformer. At this frequency, the impedance of the primary circuit is minimized due to resonance, maximizing the voltage transfer to the secondary side. When the circuit operates at or near the secondary resonance frequency $f_{\text{secondary}}$, the secondary LC circuit becomes resonant. This resonance

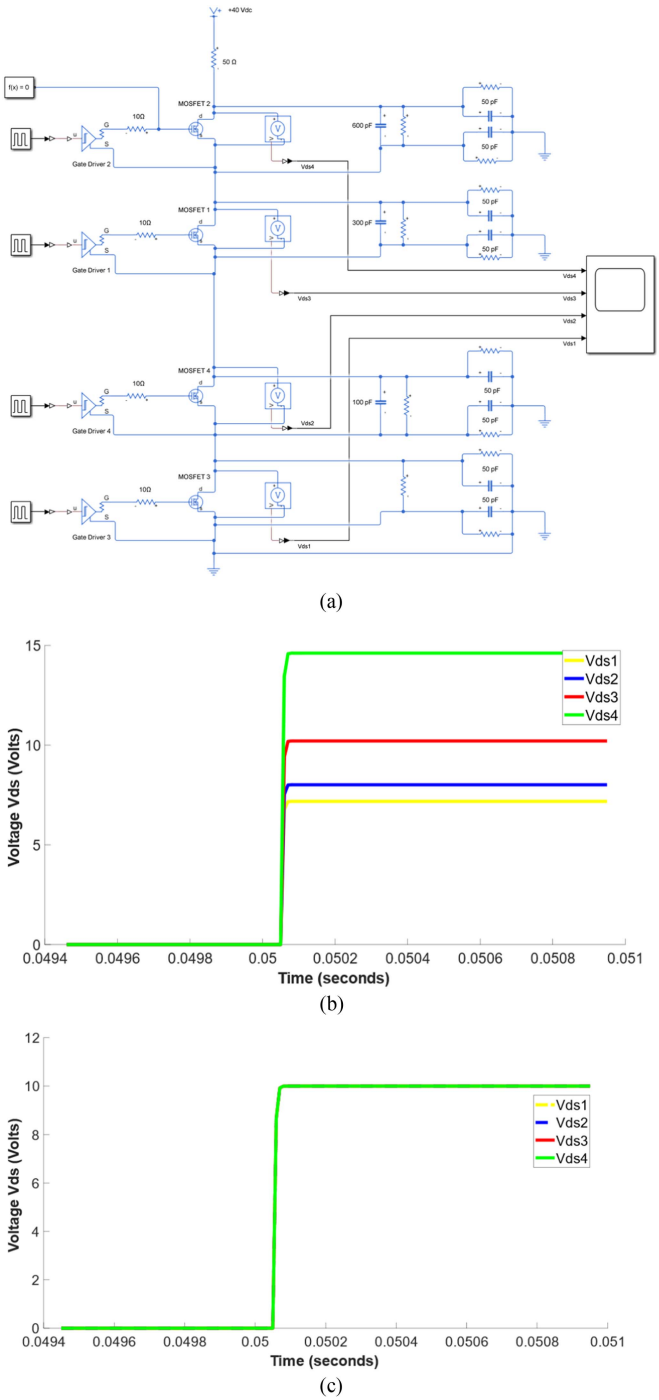


FIGURE 23. (a) MATLAB simulation driving four series-connected MOSFETs with probe impedances attached on drain–source terminals. (b) Drain-to-source (V_{ds}) voltage across four SiC MOSFETs in series during turn-OFF with no probe compensation. (c) Drain-to-source (V_{ds}) voltage across four SiC MOSFETs in series during turn-OFF with probe compensation as per (12).

facilitates efficient energy transfer from the secondary inductor L_2 to the capacitive load C_{iss} of the MOSFET gate. At this frequency, the impedance of the secondary circuit is minimized, leading to optimal charging and discharging of the gate capacitance.

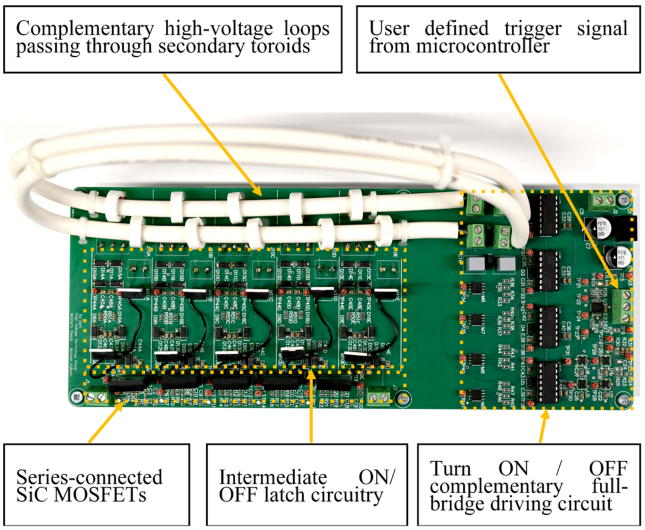


FIGURE 24. Prototype board with high voltage (HV) turn-ON/OFF single-turn loops passing through toroid cores coupled to the five series-connected SiC MOSFETs through intermediate circuitry.

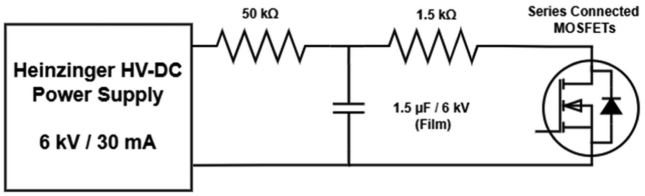
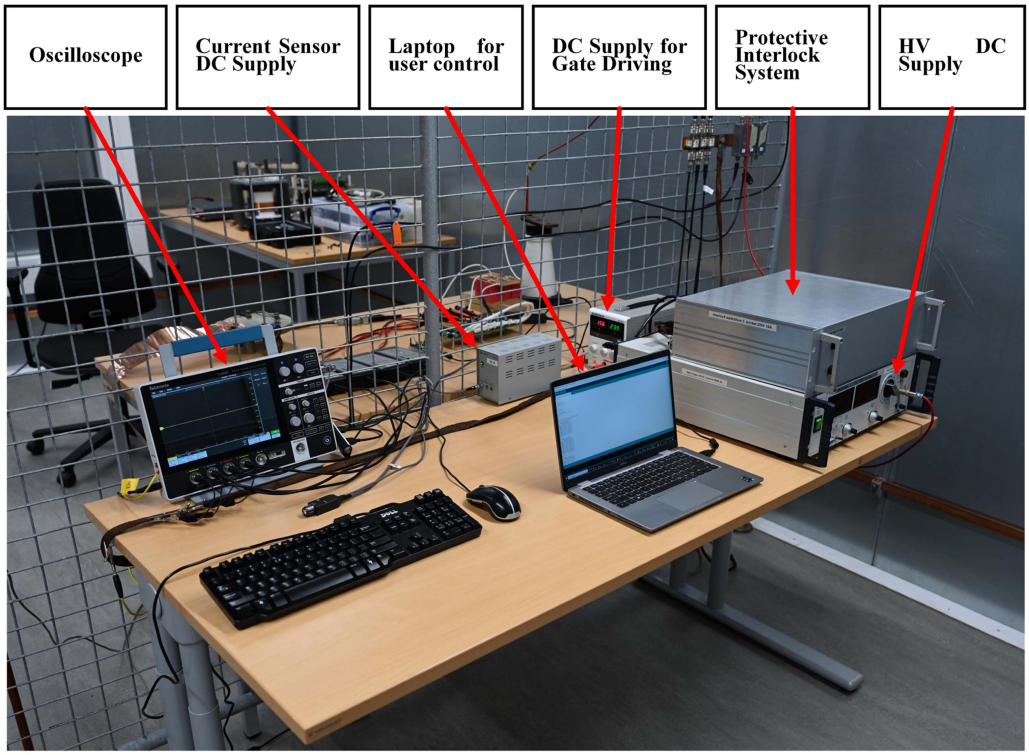


FIGURE 25. Block diagram of test setup for high-voltage dc test on the developed series-connected switches module.

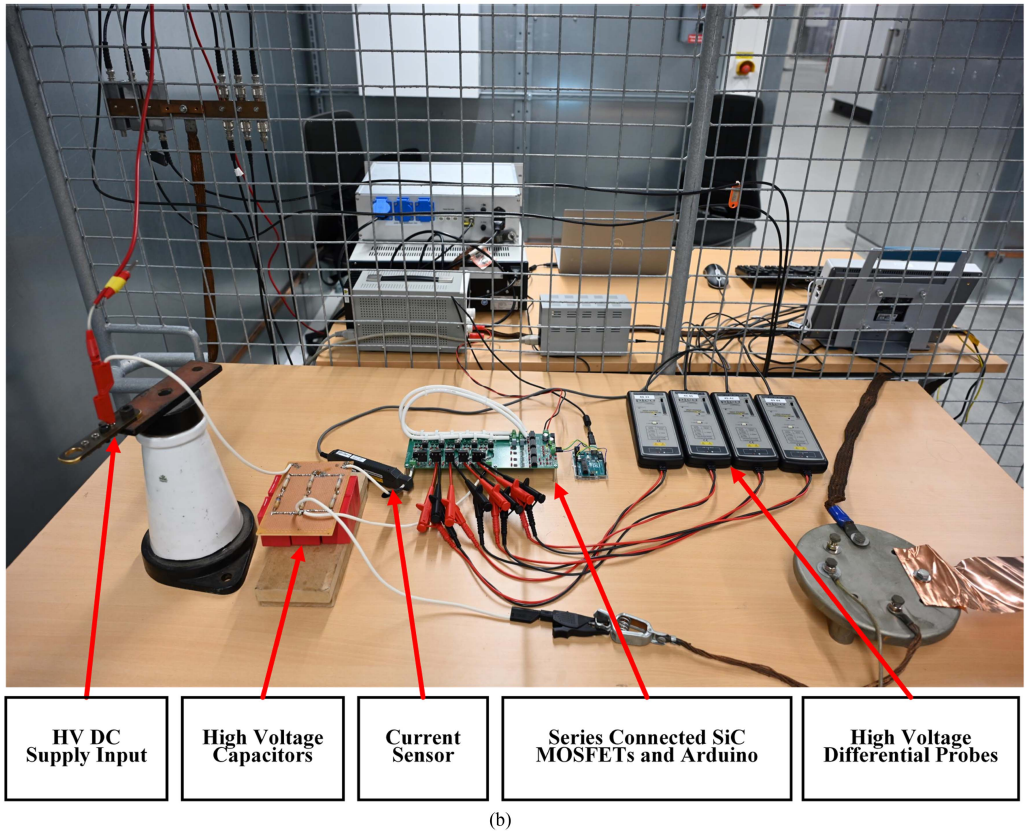
Since the proposed circuit's objective is to charge the gate capacitance of the series-connected MOSFETs in the first pulse and has separate windings for turn-ON and turn-OFF, therefore, it does not require operation at the resonance frequency. The described *LCLC* circuit allows for flexible operation over a wide linear range of frequencies between the primary-side resonance frequency f_{primary} and the secondary-side resonance frequency $f_{\text{secondary}}$, as shown in Fig. 19. The circuit operation frequency can be set to any desired frequency by setting the primary compensation capacitor C_r allowing flexibility depending on the switching speed and other requirements.

It is pertinent to mention that the primary objective of the described circuit is not to operate at any particular resonant frequency. The main aim is to turn ON the MOSFET on the secondary side of the transformer by charging the gate capacitance in the first pulse. This can be done by selecting any resonant frequency and corresponding primary-side compensation capacitor. The prime importance is the *dv/dt* of the rising edge of the driving pulse rather than the complete waveform. This rising edge *dv/dt* can lie anywhere between primary- and secondary-side resonance frequency *dv/dt*, as shown in Fig. 20.

Frequencies between 100 and 500 kHz offer an optimal tradeoff, avoiding large components and excessive losses, and in this article, a 167-kHz operating frequency was chosen to



(a)



(b)

FIGURE 26. **(a) Control and monitoring setup installed outside the Faraday's cage with 24-V dc supply, Heinzinger HVdc supply, oscilloscope, and a PC to input user-defined signal to Arduino. (b) High-voltage test setup inside protective Faraday's cage with high-voltage capacitors, current sensor, series-connected MOSFETs prototype printed circuit board (PCB), Arduino, and four high-voltage active differential probes attached to the source–drain terminals of four series-connected SiC MOSFETs.**

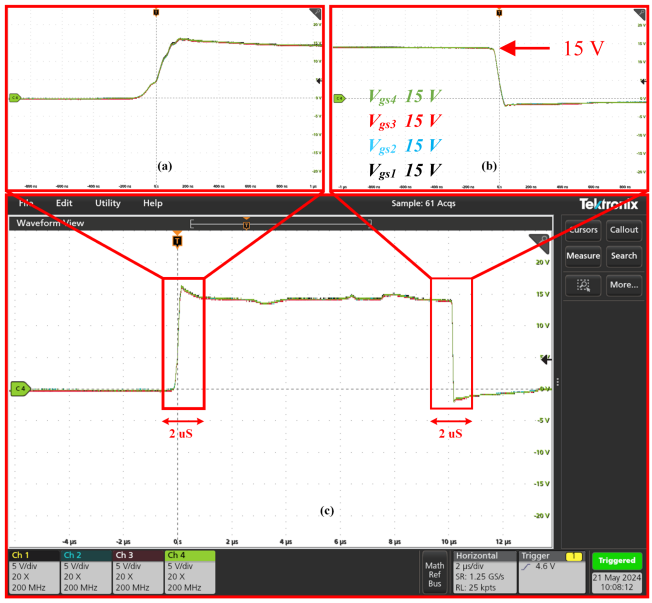


FIGURE 27. Gate-to-source (V_{gs}) voltage across four SiC MOSFETs in series during turn-ON and turn-OFF.

balance efficient power transfer, manageable component size, and minimized losses. While higher frequencies are feasible and potentially can improve performance significantly, they may introduce challenges, such as greater electromagnetic interference and thermal management issues. However, future work could involve overcoming challenges associated with higher megahertz-level frequencies.

E. MODULATOR CIRCUIT DESIGN

The transformer coupling with the primary compensation capacitor is driven by a full-bridge circuit. The gate pulses for the full-bridge square wave generator are integrated into the primary-side driver, as depicted in Fig. 15. A 5-V trigger input is taken externally that specifies the user-defined frequency and duty cycle for the series-connected SiC MOSFETs. An internal inverter-based oscillator is designed with Schmitt-triggered two-input NAND gates. The oscillating frequency is tuned using (11) [46] and the full-bridge circuit drives the pulse transformers at the tuned frequency. The thresholds V_{T+} and V_{T-} are described in the datasheet of NAND gate IC [47]

$$f_A = \frac{1}{2\,RC\,\ln\left(\frac{V_{T+}}{V_{T-}}\right)}. \tag{11}$$

IV. PROBE INFLUENCE IN VOLTAGE IMBALANCE AND COMPENSATION IN V_{DS} VOLTAGE MEASUREMENT

Equal voltage sharing among series-connected SiC MOSFETs is evaluated based on drain-to-source V_{ds} voltage across each switch. During the turn-OFF of a MOSFET, the V_{ds} voltage rises from zero to the applied voltage, and the capacitances C_{oss} and C_{iss} discharge, forcing the MOSFET to transition from the conduction mode to the voltage-blocking mode. Fig. 21(a) illustrates how isolated differential probes are placed to measure V_{ds} across each SiC MOSFET with respect to its own source voltage. In the user manual of the differential probe [48], it is shown that an approximately 10-MΩ resistance to ground is introduced by the probe. Zhao et al. [23] have shown that, for a MOSFET in the OFF-state, the resistance between drain and source terminals is a few hundred megaohms, and a 10 MΩ resistance introduced by the probes would provide a low-resistance path to ground, causing unequal voltage sharing during the static phase. Fig. 21(b) represents the probe resistances in red introduced during measurement and the need for compensation resistors shown in blue to counteract the unequal voltage sharing [23]. To compensate for the effect of this added resistive network, compensation resistors are added from within the range of a few hundred kiloohms to provide a path of least resistance to the current flowing to the ground. Zhao et al. [23] have elaborated the calculation of compensation resistor values using KVL/KCL in detail. The pattern of the values for the compensation resistance values decreases from the bottom MOSFET toward the top, and the values depend on the total number of switches in the series [23].

Similarly, the user manual of the differential measurement probe also shows that the differential probes introduce 10 pF capacitance in parallel with the 10 MΩ resistor, as shown in red in Fig. 21(b) [48]. This added capacitive network creates a V_{ds} voltage imbalance during the dynamic phase in increasing order from the bottom to the top MOSFET, as shown in Fig. 22(a), where a V_{ds} of 40 V is applied across four series-connected SiC MOSFETs. The intrinsic capacitances C_{iss} and C_{oss} of the SiC MOSFET need to be discharged to the ground through the gate terminal. The probes introduce additional capacitances affecting the charging and discharging of said capacitances. Hence, the capacitance introduced by the probe influences the voltage sharing among the series-connected switches significantly. To compensate for the voltage imbalance during dynamic turn-OFF instances of the V_{ds}, the capacitance introduced by the probes must be compensated. Like resistive compensation, the capacitive compensation is calculated using KVL/KCL. Converse to compensation resistance, the compensation capacitance value increases from bottom to top. The capacitive compensation, as shown in blue in Fig. 21(b), is calculated using the following equation:

$$C_{compi} = \frac{n\,(n+1)}{2} \times C_p \tag{12}$$

where $C_{\text{comp}i}$ is the ith compensation capacitor starting from the bottom and $C_p = C_{\text{probe}} \| C_{\text{probe}}$.

Fig. 22(b) shows the nearly balanced V_{ds} waveforms after capacitive compensation. However, this additional compensation capacitance due to parallel connection slows the turn-OFF process by a few nanoseconds; hence, the compensation capacitance needs to be optimized to provide acceptable dV_{ds}/dt slope. It is noteworthy that these compensating resistors and capacitors only ensure voltage balancing when probes are employed for V_{ds} measurements. When the switch is

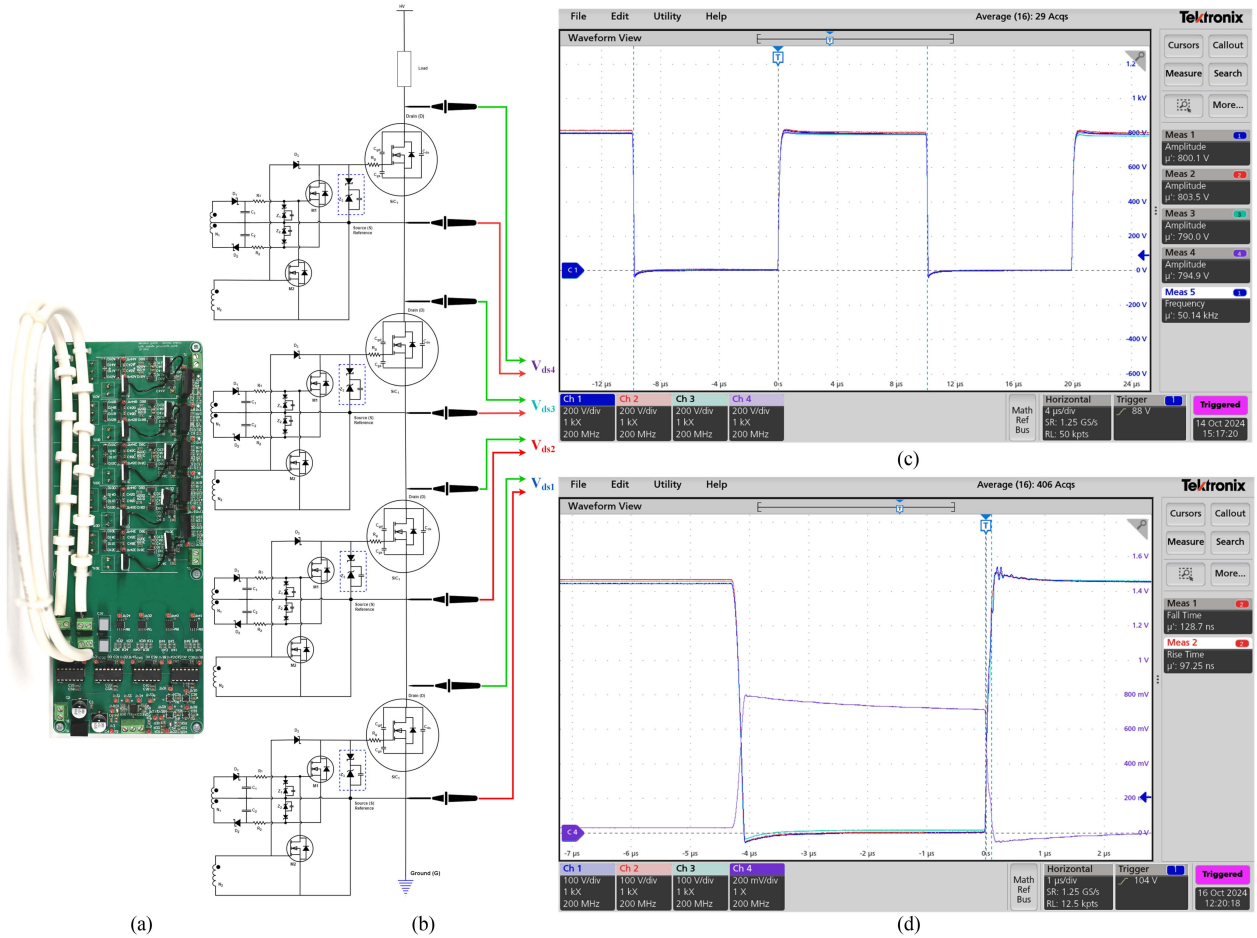


FIGURE 28. **(a) Prototype PCB. (b) High-voltage-side circuit *V*ds measurement diagram. (c) *V*ds across each series-connected SiC MOSFET. (d) Rise/fall time and current across series-connected SiC MOSFETs.**

used in normal operation, compensation is unnecessary since no probe will be connected to individual series-connected MOSFETs.

A simple MATLAB simulation, as shown in Fig. 23(a), is performed to verify the impact of additional capacitance introduced across drain–source terminals of series-connected MOSFETs by differential probes. Fig. 23(b) shows the imbalance created by probe capacitances and Fig. 23(c) shows the voltage balance achieved across series-connected MOSFETs after introducing capacitor compensation as per (12).

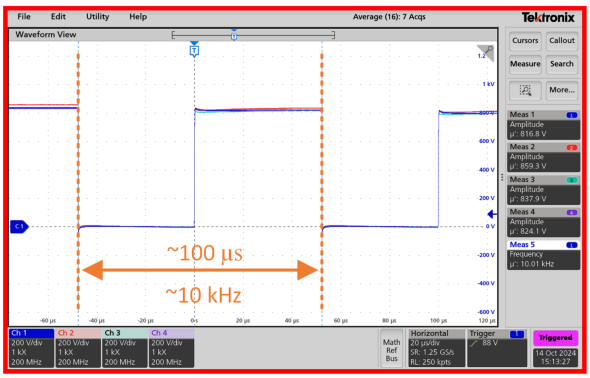
V. EXPERIMENTAL RESULTS

The prototype board with five IMW120R220M1H Infineon CoolSiC 1.2-kV SiC MOSFETs connected in series is shown in Fig. 24. After verifying the prototype operation, the V_{ds} voltage of 3.2 kV is applied from a dc test source, and various waveforms are captured. It is pertinent to mention that, although the prototype is built to accommodate five SiC MOSFETs in series, the experimentation was performed with V_{ds} applied across four SiC MOSFETs, and waveforms captured are for only four MOSFETs since a four-channel oscilloscope was used to perform the measurements. The switching frequency of the pulse transformer is set at approximately 167 kHz.

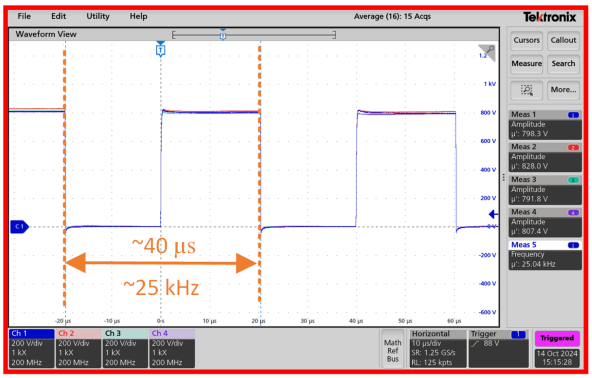
A. VOLTAGE BALANCING AT HIGH VOLTAGE

The high-voltage dc test setup block diagram for the developed module is shown in Fig. 25. Fig. 26(a) shows the control and monitoring station established outside the protective high-voltage Faraday's cage. The setup includes a four-channel oscilloscope, a laptop for user-defined frequency/duty cycle input, a dc lab supply for powering up the printed circuit board (PCB) board, a protective interlock system, and a high-voltage Heinzinger HVdc 6 kV/30 mA dc power supply. A high-voltage capacitor bank is charged from the high-voltage power supply, and then the voltage developed across the capacitor is switched to prevent the power supply from tripping due to a high current surge.

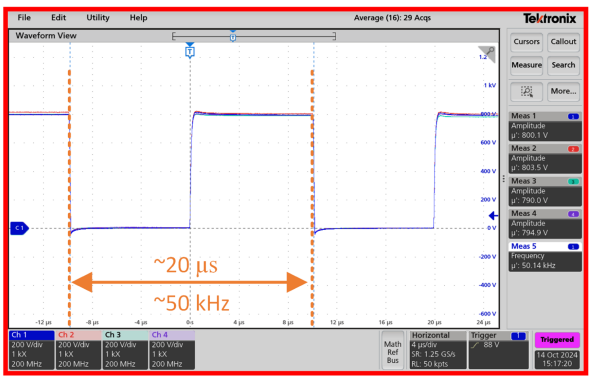
Fig. 26(b) shows the high-voltage test setup established inside the protective Faraday's cage. High-voltage PCB is fed through the capacitor bank connected to the Heinzinger HV power supply. The high-voltage differential probes are attached to the drain–source terminals of four series-connected SiC MOSFETs. A current sensor is placed across the drain–source cable to measure the current flowing through the circuit. The variable frequency and duty cycle programming is configured through Arduino as shown. The switching frequency of the complete series-connected SiC MOSFETs is set



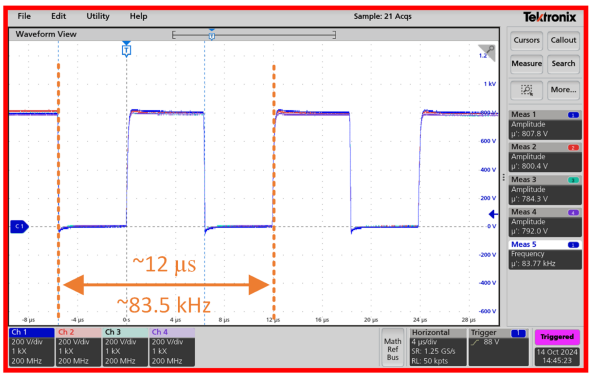
(a)



(b)

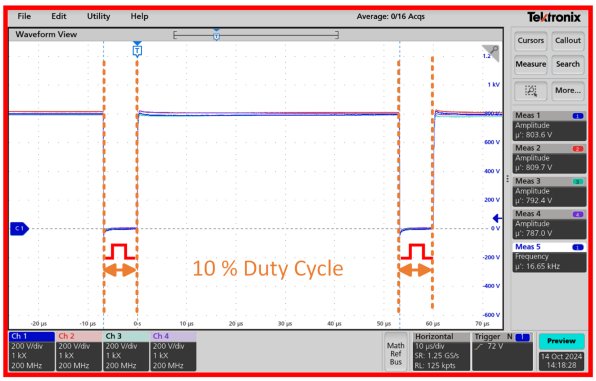


(c)

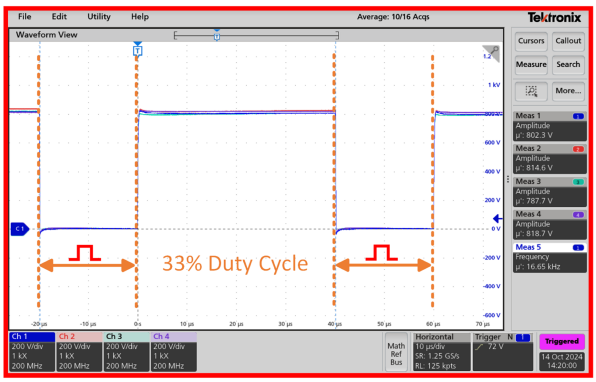


(d)

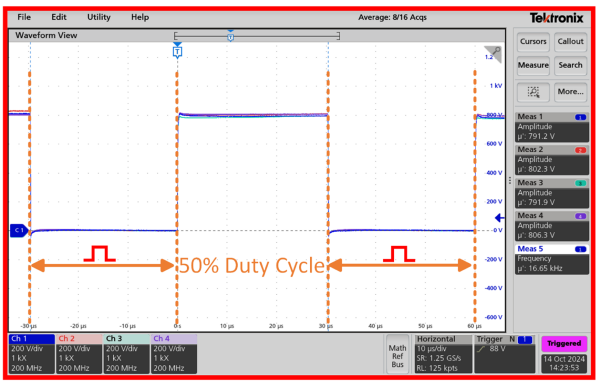
FIGURE 29. V_{ds} voltage across four SiC MOSFETs in series switching at (a) 10, (b) 25, (c) 50, and (d) 83.5 kHz with 3.2 kV applied voltage.



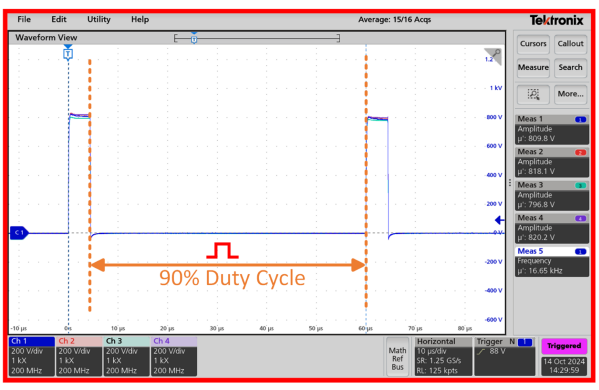
(a)



(b)



(c)



(d)

FIGURE 30. V_{ds} voltage across four SiC MOSFETs in series switching at 16.7 kHz with (a) 10% duty cycle, (b) 33% duty cycle, (c) 50% duty cycle, and (d) 90% duty cycle.

higher than 10 kHz, and after every few cycles, the switching module is kept open for a short duration to allow the capacitors to recover the depleted voltage.

One approach to verify voltage balancing between series-connected switches is to capture the gate-to-source V_{gs} voltages across each switch. Active differential probes TA057 with an attenuation ratio of 20:1 are employed across the gate–source terminal of each series-connected SiC MOSFET to measure gate voltage. Matching 15 V peak V_{gs} signal waveforms with turn-ON and turn-OFF instances across four series-connected SiC MOSFETs can be observed in Fig. 27. The charging profile of the input capacitance C_{iss} for each SiC MOSFET appears to be similar. The ripple observed in the waveform results from the pulse transformer switching at 167 kHz. The series-connected MOSFETs stack will turn completely ON when it crosses the Miller plateau voltage of 4.5 V.

Subsequently, active high-voltage differential probes TA044 were placed across drain–source terminals of each series-connected SiC MOSFET to measure the V_{ds} voltage. Fig. 28 illustrates the prototype PCB measurement diagram with V_{ds} waveforms measured across each series-connected MOSFET using high-voltage differential probes. A nearly even distribution of a total of 3.2 kV switching at 50 kHz with 50% duty cycle across four switches can be observed in Fig. 28(c). The same are tabulated in Table 2.

Fig. 28(d) shows the V_{ds} voltage rise time of 97.25 ns and fall time of 128.7 ns under specific conditions (oscillator speed 167 kHz, series-connected MOSFETs switching speed 50 kHz, and load resistance 1.5 kΩ). A current sensor N2780B by Keysight Technologies is employed to measure current across the entire series of connected switches. The datasheet of the sensor shows that the voltage of 0.1 V represents the current of 1 A [49]. The green waveform in Fig. 28(d) shows the current I_{ds} flowing across the series-connected switches. A maximum current of 8 A (shown as 800 mV) can be observed under specific conditions. It is pertinent to mention that the load for most of the high-voltage testing applications is capacitive and resistive, which requires a maximum current of nearly 0.2 A [10]. Hence, for high-voltage testing applications, the switch's current-handling capability is satisfactory. Since the load in the majority of tests is capacitive, the inductive load has not been included in this study.

Subsequently, similar measurements were carried out across each series-connected MOSFETs stack for different frequencies and duty cycles to ascertain gate driver's performance. Fig. 29(a), (b), (c), and (d) shows the series-connected SiC MOSFETs switching around 3.2 kV at 10, 25, 50, and 83.5 kHz frequency, respectively. A nearly equal voltage distribution across all switches can be observed. The entire switch can switch at a maximum of half the switching frequency of the transformer. The maximum switching frequency can, therefore, be

$$f_{\text{switch\_max}} = f_{\text{transformer}}/2. \tag{13}$$

Similarly, different duty cycles were configured, and the V_{ds} waveforms across each series-connected MOSFET were measured. Fig. 30(a), (b), (c), and (d) shows around 3.2 kV V_{ds} switching at 16.7 kHz with 10%, 33%, 50%, and 90% duty cycles, respectively. Again, nearly equal voltage distribution across all switches can be seen. The duty cycle is the ratio of the transformer frequency and the switching frequency

$$\text{Duty Cycle} = \left(f_{\text{pwm}}/f_{\text{transformer}}\right) * 100\%. \tag{14}$$

So, if the switching frequency of the series-connected MOSFETs = 10 kHz, then the transformer frequency must be ≥ 1 MHz in order to obtain a duty cycle of 1%. The transformer frequency is the limiting factor in order to achieve both series-connected MOSFETs stack switching frequency and the minimum achievable duty cycle. The higher the transformer frequency, the higher the switching frequency and duty cycle resolution of the entire series-connected MOSFETs stack.

VI. CONCLUSION

High-frequency high-voltage switching modules are needed for MV dc power grid testing applications. They can be made by putting well-proven low-voltage semiconductor devices in series. The major challenge in developing a high-voltage switching module with series-connected switches is to drive the switches with high-voltage isolation and to ensure even dynamic voltage distribution across each switch. Transformer-coupled gate-driving methods are limited to switching the series-connected switch stack at pulse frequency.

Testing with complex high-voltage waveshapes is foreseen to prepare for the future renewable rich and power-electronics-dominated grid. Series-connected switching devices with programmable frequency and duty cycles have the potential to generate these complex waveshapes. Earlier transformer-coupled gate drivers have a fixed frequency operation and, thus, cannot be used to keep the switch ON and OFF as per a custom user-defined duty cycle. This article has summarized the factors responsible for the dynamic voltage imbalance across series-connected SiC MOSFETs and the limitations of the previous techniques to achieve user-defined arbitrary switching functionality. Subsequently, the article elaborates in detail on a technique that provides a programmable turn-ON/OFF mechanism to make the frequency and duty cycle of the series-connected MOSFETs independent of the high-frequency transformer coupling. The technique demonstrated nearly even balanced voltage across four series-connected SiC MOSFETs. The switch has been demonstrated experimentally to perform at 3.2 kV with various frequencies and with various duty cycles.

In addition, the article has shown that the effect of measurement probes while measuring V_{ds} across individual switches on voltage imbalance is quite significant, and compensation resistors and capacitors need to be placed correctly across each switch to get accurate information about the voltage distribution across individual switches during measurements. These passive compensation components are removed during

normal switch operation when no probe is present across every single MOSFET. This phenomenon is particularly important as passive snubber values reported in previous studies may not have taken the probe impact into account leading to voltage imbalance when no probe is placed across series-connected MOSFETs.

The presented gate driver has the potential to make the simple, cost-effective, high-voltage switch using series-connected SiC mosfets a key building block for MV dc converter applications, especially to create complex voltage waveshapes for high-voltage testing of power-electronics-dominated future grid assets. These high-voltage switches could also significantly contribute to accelerating the technology development for MV and high-voltage converters.

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