MASTER THESIS

A LOW OUT-OF-BAND NOISE 2.5GHZ DTX

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Master of Science Thesis

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Science is a wonderful thing
if one does not have to earn one's living at it.

Albert Einstein

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1

INTRODUCTION

1.1. INTRODUCTION

[1]

WITH the phenomenal development of the wireless industry and telecommunication techniques, wireless connectivity has become an essential service in our daily lives. In recent years, with the advancement of the wireless industry, more and more applications of high data rates have emerged in customer mobile phones. Most of them are driven by the entertainment industry. According to research by Cisco company [3], over 75% of the internet bandwidth is utilized for online video streaming. Nowadays, people desire more sophisticated applications on their mobile phones, including features like 4K video streaming, video gaming, and the Internet of Things (IoT). As a result, the escalating demand for high-data-rate communication represents an unstoppable trend. Figure 1.1 presents a forecast of the development of wireless communication data in various applications up to 2030.

In this scenario, there is a need for higher and faster communication standards. In wireless communication, there are two primary types of communication standards. One is known as cellular communication, which has undergone evolution through several generations over the past few decades. It began with the first generation (1G), characterized by analog technology and slow transmission speeds. The second generation (2G) introduced the Global System for Mobile Communications (GSM), marking the transition to digital communication. This was followed by the third generation (3G), which employed wideband code division multiple access (W-CDMA), and the fourth generation (4G), built on the 3rd Generation Partnership Project Long-Term Evolution (3GPP LTE).

The latest standard is the 5G New Radio (5G-NR), developed by 3GPP. This standard enables significantly higher data rates and supports a wider range of applications compared to long-term evolution (LTE). Another category of wireless communication in-

[1] Part of this Chapter is written as a part of a free elective course, ET4399, preparation for an MSc Project at the University.

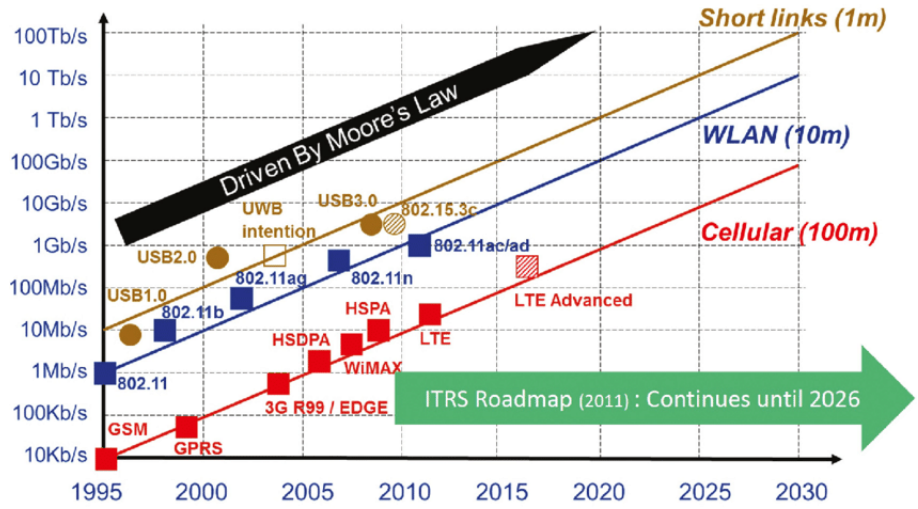


Figure 1.1: Wireless communication traffic growth[15]

cludes technologies such as near-field communication (NFC), Bluetooth, ultra-wideband (UWB), and wireless local area networks (WLANs) based on IEEE 802.11 standards. These advancements introduce both new opportunities and challenges for radio frequency (RF) integrated circuit design.

1.2. DIGITAL TRANSMITTERS ADVANTAGES AND CHALLENGES

1.2.1. ADVANTAGES OF DIGITAL TRANSMITTERS

As the wireless standards continue to develop, modern wireless transmitters (TXs) must meet more strict requirements of wireless communication systems. These stringent requirements include wide RF/modulation bandwidth, spectral purity/out-of-band noise of better than -40dBm/MHz, inband linearity surpassing -36dB, and system energy efficiency of better than 30% for these MIMO TXs. Although purely analog TXs still deliver the required RF power and linearity, they suffer from several disadvantages. These TXs are fully analog and demand quiescent current and voltage biases. Thus, they consume a lot of power, and these TXs are not CMOS-friendly, so they cannot be effortlessly migrated to the advanced CMOS process. Moreover, given the more complex modulation techniques employed in 5G communication systems, maintaining ideal linearity in the TXs becomes challenging. However, there is a trade-off between the linearity and efficiency of the RF TXs. Higher linearity leads to less efficiency and vice versa. Consequently, it is essential to find an efficient and linear TX structure to meet the requirements for high-quality data transmission.

Despite the continuous evolution of wireless standards, the advancement of RF CMOS integrated circuit technology has progressed in parallel, driven by ongoing improvements in CMOS technology. These advancements have resulted in higher-speed operations and smaller chip sizes, as predicted by Moore's Law, which predicts that the

number of transistors on a microchip doubles approximately every two years. This exponential growth in transistor density has allowed RF CMOS circuits to achieve greater processing power, reduced power consumption, and enhanced performance, making them a critical component in the development of modern wireless communication systems.

In this projected trend, transistor switching speeds have been accelerated and become much more friendly for digital signal processing. This perspective also results in much more power-efficient wireless solutions that require a high degree of integration. Digitally assisted approaches are preferred over Traditional analog transmission methods [25] because digitally-intensive TXs Can reap the rewards of higher switching speed, minimum transistor length, and low supply voltage and headroom in nanoscale CMOS technology [23]. Consequently, a significant shift has occurred over the last two decades, with most RF circuits being extensively integrated digitally using CMOS technology. Based on that, various digital TX structures have been proposed to satisfy modern wireless systems' power and linearity requirements.

1.2.2. CHALLENGES OF DIGITAL TRANSMITTERS

Digital and analog TXs differ in handling signals in a wireless data communication system. A traditional wireless system transmits data from a TX to a receiver (RX). The process involves converting digital baseband data into an analog signal using a digital-to-analog converter (DAC). The analog signal then undergoes a low-pass filter (LPF) to suppress the sampling spectral replicas and its quantization noise. This signal is further frequency translated by an upconverting mixer using a local oscillator (LO). A power amplifier then amplifies the resulting modulated RF signal to ensure reliable reception at the receiver's end of the wireless channel. Finally, the signal is radiated through the antenna.

In the digital TX, the signal is directly upconverted to the RF domain by an RF-DAC. Nonetheless, this method has one main drawback. Due to the absence of a reconstruction filter after D/A conversion, the quantization noise of the baseband and its sampling spectral replicas are also upconverted to RF and amplified at the output of the TX[23]. Therefore, developing a new structure for the digital TX to suppress out-of-band noise is crucial.

1.3. THESIS OBJECTIVE

From the preceding discussion, DTX has a main drawback in that its sampling noise remains unfiltered, leading to high noise levels at specific frequencies. The substantial quantization noise may adversely impact receiver performance. This thesis addresses this issue by proposing a novel implementation of fully integrated digital-intensive sub-6-GHz transmitters. This design incorporates a bandpass reconstruction filter in the RF domain to ensure a low out-of-band (OOB) noise floor, aligning with emission mask requirements. Additionally, the transmitter is optimized for operation in frequency division duplexing (FDD) systems, and special attention is given to suppressing TX leakage noise within the receiver band to prevent desensitization when the transmitter and receiver operate concurrently.

The thesis objective requirements are summarized in Table 1.1, which outlines the

complete design objectives for the 40 nm CMOS DTX.

Parameter	Specification
Process Technology	40 nm CMOS
Operational Frequency	2.5 GHz
Modulation Bandwidth	Up to 100 MHz
Peak RF Output Power	> 30 dBm
Peak PAE(%)	>30%
Out-of-Band Noise	Better than -134 dBm/Hz

Table 1.1: Summary of design requirements

1.4. THESIS OUTLINE

This thesis contains the following:

- **Transmitter Architectures Review**
  The second chapter explores the foundational principles of digital transmitters and power amplifiers. It provides a comprehensive overview of various techniques to enhance the average efficiency of wireless systems. Furthermore, this chapter discusses several innovative digital transmitter designs specifically developed to mitigate receiver band noise and introduces a power amplifier called the switched-capacitor power amplifier.

- **Switched-Capacitor Power Amplifier and Power Combining Design**
  Chapter 3 delves into the switch-capacitor power amplifier (SCPA) design, focusing on optimization strategies and the design of the associated power-combining network. This chapter highlights key considerations in achieving efficient power amplification.

- **An 8-Bit RF DAC with FIR Filter Noise Suppression**
  Chapter 4 presents the design of an 8-bit RF Digital-to-Analog Converter (DAC) integrated with a finite impulse response (FIR) filter. It discusses methodologies for suppressing sampling replicas and quantization noise within the receiver's bandwidth, ensuring improved signal integrity.

- **Simulation Results**
  Chapter 5 provides a detailed analysis of the simulation results derived from the cascade configuration based on spectral characteristics. This chapter illustrates the spectrum of the RF output, demonstrating the performance of the proposed designs.

- **Conclusion and Future Insights**
  Chapter 6 synthesizes the thesis findings and offers insights into prospective research directions and future developments in the field.

2

TRANSMITTER ARCHITECTURES REVIEW

[1] This section will discuss digital TX architectures and power amplifiers (PAs) and their performance metrics. It will also explain several efficiency improvement approaches. Finally, some novel and valuable structures, such as Switch-capacitor power amplifiers (SCPA), Class-G PA, and transformer-based mix domain FIR filters, which are crucial in this thesis, will be discussed.

2.1. TX FIGURES-OF-METRIT

2.1.1. DELIVERED RF POWER

In a traditional wireless transmission system, a specific link budget requires a designated output power level to meet certain signal-to-noise ratio (SNR) requirements for its RX companion. In other words, the link budget determines the peak or maximum radiated RF power. Moreover, to elevate the spectral efficiency of the wireless systems, nonconstant envelope modulation strategies, such as orthogonal frequency division duplexing (OFDM) as illustrated in Fig 2.1, which comprises many sub-carriers, are employed. This feature requires the TX systems to operate most of the time in the power back-off (average power domain) region, indicating a relatively high "peak-to-average power Ratio" (PAPR) that is defined as follows:

$$PAPR = \frac{P_{RF-MaX}}{P_{RF-Mean}} = \frac{Max[x^2(t)]}{\overline{x^2(t)}} \tag{2.1}$$

A large PAPR indicates a significant variation between the signal's peak and average power levels, which can pose challenges in wireless communication systems due to increased complexity and potential for distortion during transmission. Apart from that,

[1] Part of this Chapter is written as a part of a free elective course, ET4399, preparation for an MSc Project at the University.

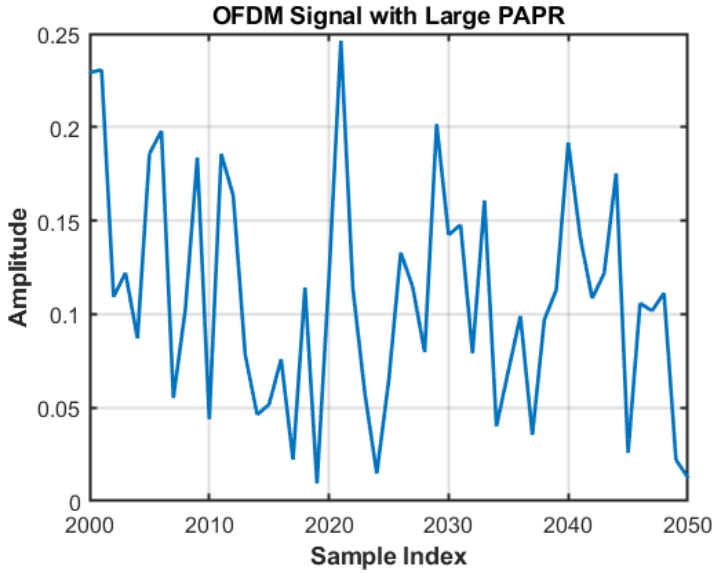


Figure 2.1: OFDM signal in time domain

the TX must be efficient at its peak and back-off region to have an efficient TX using this modulation scheme. Achieving this efficiency requires the implementation of efficiency-enhanced techniques in the design of the intended TX.

2.1.2. LINEARITY

Linearity reflects the degree of distortion in the TX output signal. As mentioned, in modern wireless communication, nonconstant modulation schemes such as high-order quadrature amplitude modulation (QAM) and OFDM signals are employed to maximize the utilization of spectrum resources, improving the systems' spectral efficiency.

Because high-order modulation schemes introduce amplitude and phase information into signals, it becomes necessary to linearly amplify the signals whose amplitude information is transmitted without distortion. If the PA exhibits nonlinearity, it will exhibit distinct responses to signals of different amplitudes, resulting in non-linear distortion. This distortion can negatively impact metrics such as ACPR (Adjacent Channel Power Ratio) and EVM (Error Vector Magnitude), ultimately deteriorating the quality of the radiated signal.

Hence, PA must meet stringent linearity requirements, both in-band signals, in which the receiver can correctly identify the instantaneous signal values, and out-of-band signals to not interfere with transmissions on neighboring frequency channels.

2.1.3. EFFICIENCY

A PA is used at the front end of the TX chain right before the antenna to boost the TX signal strength and overcome the loss of the wireless communication path. A PA amplifies

its input signal to deliver the necessary RF power. Strengthening its input signal requires DC-current and bias voltages. Therefore, its "efficiency" becomes another crucial metric in the design of a PA. The efficiency of a PA is represented in two ways: Drain efficiency and power-added efficiency.

The drain efficiency is the ratio between P_{out} and P_{DC}. P_{out} is the output power delivered to the load, which is calculated using V_{RF}, the output voltage, I_{RF}, and the output current:

$$P_{out} = \frac{V_{RF}}{\sqrt{2}} \cdot \frac{I_{RF}}{\sqrt{2}} \tag{2.2}$$

Vdc is the supply voltage, and Idc is the supply current. The DC supply power is given by:

$$P_{dc} = V_{dc} \cdot I_{dc} \tag{2.3}$$

The definition of drain efficiency is the ratio of output power to consumed direct power, typically denoted by η. The calculation formula is as follows:

$$\eta_{drain} = \frac{P_{out}}{P_{DC}} \tag{2.4}$$

The "Power Added Efficiency" (PAE) determines the ratio of the effective delivered power and the DC dissipation. The effective power is P_{out} minus P_{in}. The formula for calculating PAE is as follows:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{2.5}$$

According to the formula defining efficiency, if the DC power P_{DC} is entirely converted into a fundamental RF power P_{out}, the PA will achieve 100% efficiency. To achieve that goal, the DC dissipation energy (P_{dis}) must be zero. In its equation, v(t) and i(t) represent the voltage and current across the transistor, respectively; the formula for DC dissipation energy can be expressed as:

$$P_{dis} = \frac{1}{T} \int_0^T v(t) \cdot i(t) = 0 \tag{2.6}$$

Additionally, the harmonic power must be zero where V_n and I_n represent the amplitude values of the nth harmonic's voltage and current and ϕ denotes their phase. This equation can be expressed as:

$$P_{out,nf} = \frac{1}{2} \cdot V_n \cdot I_n \cdot \cos\phi = 0 \tag{2.7}$$

2.1.4. SPECTRAL PURITY

The ultimate goal of this project is to suppress the leakage of the TX noise at the RX band and guarantee the frequency-division duplexing (FDD) operation. The TX must demonstrate stringent spectral purity. The out-of-band spectral purity of a digital TX (DTX) is

measured as the adjacent Chanel power ratio (ACPR), which is defined as follows:

$$ACPR(dBc) = 10\log\frac{P_{Adj}}{P_{Main}} \tag{2.8}$$

where P_{Adj} and P_{Main} are the power in the adjacent and main channels, respectively. In TX, achieving a low ACPR is crucial to ensure the required RX signal quality in the FDD system.

2.2. PA ARCHITECTURES REVIEW

TX Power consumption Breakdown demonstrates that PA has the largest contribution at full power for both on-chip and off-chip PAs. On-chip PAs demand high linearity and efficiency, serving as a crucial component in modern wireless TXs. As the 5G communication system increases frequency and power levels, the design of on-chip PA RF becomes more challenging due to more intricate modulation schemes. Although the design of the power amplifier is quite complicated, its evaluation criteria are relatively straightforward, focusing on only two critical metrics: linearity and efficiency.

In the pursuit of optimizing PAs' linearity and efficiency, pioneers in RF PA technology have classified and analyzed them based on their operational characteristics. PAs can be broadly categorized into two main types: linear amplifiers and switch-mode amplifiers.

2.2.1. PA CLASSES

Linear PAs include Class-AB, Class-B, and Class-A PAs, while switch-mode PAs encompass Class-D and Class-E PAs. They are categorized according to their conduction angle, determined by the bias condition used in the final stage. Linear PAs have the advantage of amplifying the input signal linearly. However, achieving high efficiency with linear power amplifiers is a challenge.

Consequently, switch-mode PAs are gaining popularity, rapidly switching the output devices between fully on and fully off states. When the input voltage is positive, the transistor in a switch-mode PA turns on, allowing current to flow, yet the voltage across its terminals remains zero. In contrast, when the voltage is negative, the transistor is turned off, and the output voltage rises, with zero current flowing through the transistor. Since the transistor in the switch mode does not consume power, all the DC energy can be converted into RF energy. Therefore, theoretically, a switch-mode PA can achieve a drain efficiency of 100%. High efficiency is the primary advantage of switch-mode PAs, but they exhibit inferior linearity. Moreover, when operating at high frequencies, parasitic effects prevent the CMOS from perfectly behaving like a switch, making harmonic control very challenging.

Class A power amplifier

In an ideal class-A PA where the drain voltage is allowed to swing up to $2V_{DC}$, the RMS value of the sinusoidal output voltage and the drain current is:

$$V_{out} = \frac{V_{DC}}{\sqrt{2}} \tag{2.9}$$

$$I_{out} = \frac{I_{DC}}{\sqrt{2}} \tag{2.10}$$

Hence, the drain efficiency of class-A PA is:

$$\eta_{Class-A} = \frac{P_{out}}{P_{DC}} = 50\% \tag{2.11}$$

Class B power amplifeir

The DC bias point is typically located near the transistor threshold voltage for Class B PAs. The transistor conducts only when the input signal has a positive swing, resulting in a half-wave rectified sine-wave drain current. The fundamental component of the drain current is:

$$I_m = \frac{1}{\pi}\int_0^{\pi} I_{peak}\cos^2 wt\, d\,wt = \frac{I_{peak}}{2} \tag{2.12}$$

The DC supply current is the average of the current waveform:

$$I_{dc} = \frac{1}{2\pi}\int_0^{\pi} I_{peak}\cos wt\, d\,wt = \frac{I_{peak}}{\pi} \tag{2.13}$$

Hence, the relationship between output and the DC supply is

$$I_{dc} = \frac{2\sqrt{2}}{\pi} I_{out,rms} \tag{2.14}$$

$$V_{dc} = \sqrt{2}\cdot v_{out,rms} \tag{2.15}$$

$$\eta_{Class-B} = \frac{P_{out}}{P_{DC}} = \frac{\pi}{4} = 78.5\% \tag{2.16}$$

Class AB PAs

Class AB PA is an amplifier positioned between Class A and Class B, with a conduction angle ranging between π and 2π.

Class D PA

Professor Baxandall introduced the Class D Power Amplifier in 1959[4]. It consists of a paired set of switching transistors, M1 and M2, along with a resonant-tuned load at the fundamental frequency. Figure 2.2 shows a circuit of the Class D CMOS RF power amplifier, in which a PMOS and an NMOS are used as switching devices.

Under ideal conditions, the voltage and current of the transistors in a Class D Power Amplifier do not overlap, resulting in zero DC power dissipation for the D-class PA. Apart from that, concerning harmonic power dissipation, the output voltage waveform of a Class D PA is a square wave signal, and due to the presence of a resonant load, the output current waveform is a semi-sinusoidal wave. Performing a Fourier series expansion

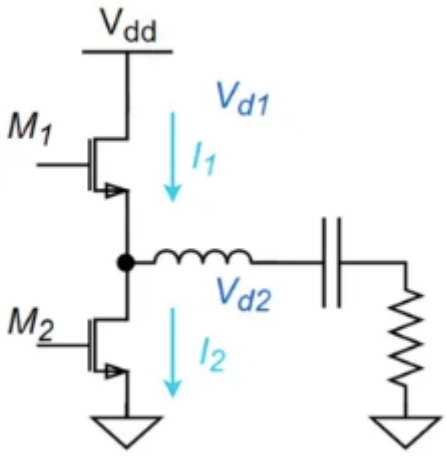


Figure 2.2: Class D structure

on the square wave signal yields zero even harmonic components, while the Fourier expansion of the semi-sinusoidal wave results in zero odd harmonic components. The alternation of voltage and current in the harmonic components is zero, leading to the ideal Class D PA having no harmonic power dissipation. However, due to their parasitic capacitance, the Class D PA can't operate at very high frequencies.

2.3. MODERN DIGITAL TX ARCHITECTURES

This project focuses on digital TX design. This section introduces several state-of-the-art DTX architectures.

Digital Power Amplifier (DPA) architectures, which digitally modulate envelope signals, have garnered significant interest owing to the numerous advantages of CMOS technology scaling. As they integrate into more advanced CMOS technology, several benefits emerge. Firstly, there is a decrease in production costs. Secondly, faster switching speeds become achievable with a shorter channel length and smaller parasitic capacitance. Third, a reduction in supply voltage contributes to diminished dynamic power dissipation. Additionally, DPA could use digital approaches like digital pre-distortion(DPD) to solve the nonlinearity issues in power amplifiers.

Digital PA (DPA) architectures, which digitally modulate envelope signals, have gained substantial interest due to the numerous advantages of CMOS technology scaling. As they are implemented and integrated into more advanced CMOS technology, several benefits emerge:

- There is a decrease in production costs;

- A shorter channel length and smaller parasitic capacitance make faster switching speeds achievable;
- A reduction in supply voltage contributes to diminished dynamic power dissipation;
- DPA could use digital approaches like digital pre-distortion(DPD) to solve the nonlinearity issues in DPA.

2.3.1. DIGITAL POLAR TX

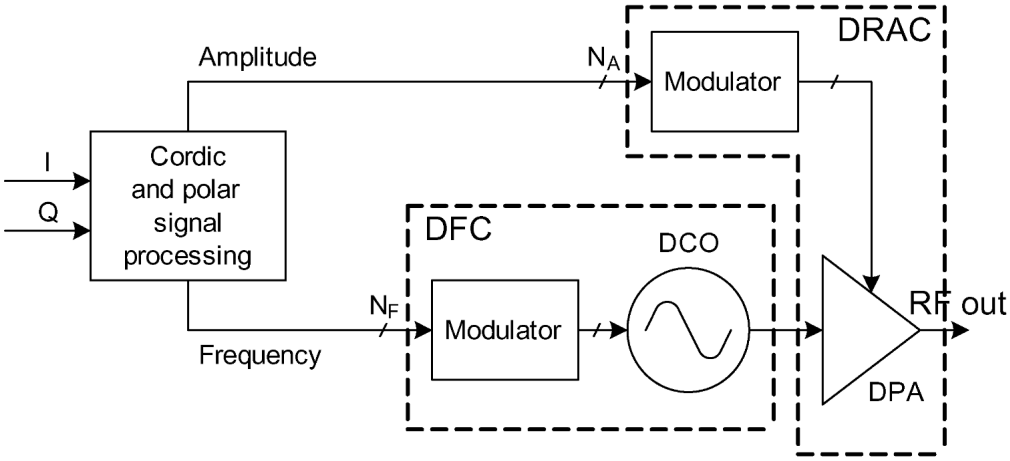


Figure 2.3: digital polar transmitter circuit[24]

Fig 2.3 depicts a conceptual block diagram of digital polar TX. The fundamental concept of polar modulation originates from envelope elimination and restoration, initially proposed by Leonard R. Kahn in 1952[14]. The polar TX separates the RF signal into envelope and phase components. As the phase component remains constant, this enhances efficiency.

The initial I/Q data are generated from the digital baseband processor. These signals then pass through the CORDIC block to convert the IQ data into envelope and phase counterparts.

The operation of the CORDIC is as follows:

$$A(t) = \sqrt{I^2(t) + Q^2(t)} \tag{2.17}$$

$$\phi(t) = \tanh \frac{Q(t)}{I(t)} \tag{2.18}$$

The frequency deviation output signal is fed into a phase modulator, which can be constructed using an all-digital phase-locked loop (ADPLL). Based on the frequency

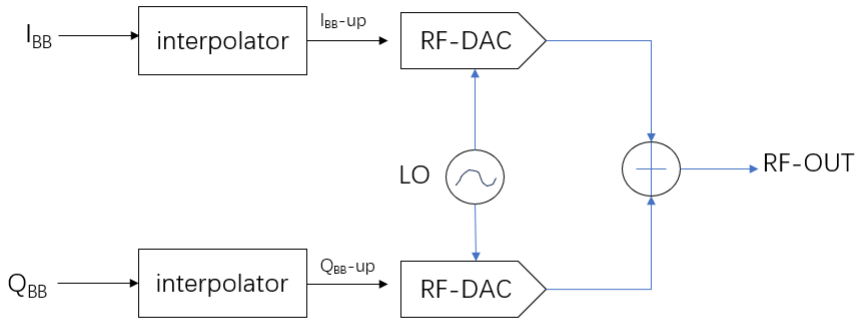


Figure 2.4: Cartesian (I/Q)-based digital transmitter structure

data, it generates a clock carrier, which is then fed into the DPA. Subsequently, the DPA produces an RF output, with the envelope being controlled by the amplitude modulation signal.

The discussion above shows that the polar configuration has very high efficiency. However, a closed-loop phase modulator such as an all-digital-PLL (ADLL) typically cannot handle very wideband signals due to the loop bandwidth and DCO nonlinearity[24]. Due to the bandwidth expansion caused by the CORDIC, polar TXs face limitations in handling wideband signals.

2.3.2. DIGITAL CARTESIAN TX

Fig 2.4 illustrates a simplified diagram of a Cartesian (I/Q)-based Digital Transmitter, first introduced in [2]. This architecture aims to maintain the benefits of the digital-intensive approach while mitigating the bandwidth expansion issue of its polar variant. The crucial distinction between the polar approach and the Cartesian approach lies in the fact that the Cartesian digital transmitter eliminates the need for CORDIC operation. Consequently, bandwidth expansion is eliminated, allowing the Cartesian transmitter to operate effectively with wideband signals.

The digital Cartesian TX operates as follows. To uphold high spectral efficiency in digital communications systems, baseband information is typically represented by two orthogonal data bit-streams, each modulated by its corresponding orthogonal carrier signal[2]. Hence, to begin with, the digital signal processor produces two sets of data: the in-phase (I) signal and the quadrature (Q) signal. Next, the interpolator up-samples those signals; this process guarantees that the sampling spectral replicas will be knocked down and located far away from the carrier and thus can easily be filtered out[2]. Accordingly, the signal drives the radio-frequency digital-to-analog converter (RF-DAC) banks, which supersede low-path filter (LPF), mixer, and DPA blocks. This process directly converts the input digital signal to an RF-OUT. Finally, at the output of an I/Q DTX, orthog-



Figure 2.5: back-off-for-class-B-amplifier

onal vector recombination is applied to achieve power combining.

Regrettably, the original Cartesian DTX suffers from an in-band linearity drawback, primarily from the interaction between the I-branch and the Q-branch. When employing a 50% duty cycle digital I/Q carrier, undesirable overlap summation occurs, leading to signal degradation in both linearity and Error Vector Magnitude (EVM). Hence, to tackle these challenges, Alavi et al. [2] employed a 25% duty cycle for clock signals to upconvert the I and Q signals. This configuration ensures no overlap, and the summation accurately produces the correct two-state output signal.

2.4. EFFICIENCY ENHANCEMENT TECHNIQUES

The progress in contemporary wireless communication standards and the adoption of high-order modulation schemes have led to increased challenges in the design of PAs, resulting in adopting high-order modulation schemes, such as the nonconstant envelope modulation, which combines numerous sub-carriers, causing rapid changes across a relatively broad dynamic range. As such, these signals experience a relatively large PAPR.

Nonetheless, traditional power amplifiers exhibit high efficiency only when operating at their maximum output power. In the power back-off region, the efficiency of a conventional PA declines dramatically as the output voltage swings due to a lower supply voltage being reduced for a certain output power level. For example, as illustrated in Fig. 2.5, the efficiency of an idealized Class B amplifier at maximum output power is 78.5%. Still, it decreases to approximately 30% in its average power region.

However, not all amplifiers must operate in their maximum power region. Operating in the saturation region of these power amplifiers will result in signal peak clipping and distortion of the signal envelope. Therefore, the power amplifier must sacrifice efficiency and operate at a back-off power level to avoid clipping and distortion. The trade-off of

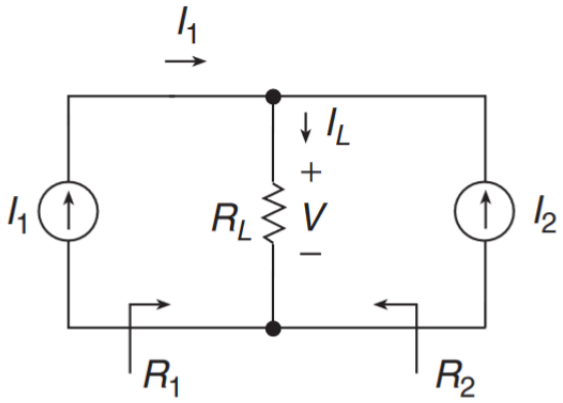


Figure 2.6: Circuit with load impedance modulation

power is the low-efficiency PA with the high PAPR signal. Therefore, it is crucial to explore techniques for enhancing power amplifier efficiency.

2.4.1. DOHERTY EFFICIENCY ENHANCEMENT

Over time, various techniques have been proposed to improve efficiency in the power back-off region. Such as envelope tracking, out-phasing configuration, and doherty techniques. In this section, we will introduce the Doherty configuration.

W.H. Doherty proposed this technique in 1936[11], primarily as an efficiency enhancement structure. This topology achieves enhanced power back-off efficiency by using active load modulation[21]. Moreover, it only relies on straightforward circuitry to achieve a significant efficiency improvement, making it a preferred choice for base station applications.

The circuit with load impedance is illustrated in Fig 2.6, where two amplifiers represent the current source I1 and I2, and a power combiner network connects both to load R_L.

Simple Kirchhoff circuit theory shows that if current source #2 supplies a current I2, and current source #1 supplies a current I1, both currents flow into the load resistor so that the voltage appearing across the load resistance is:

$$V_L(t) = R_L(I_1 + I_2) \tag{2.19}$$

The current source #1 observes the load impedance as:

$$Z_1 = R_L(\frac{I_1 + I_2}{I_1}) \tag{2.20}$$

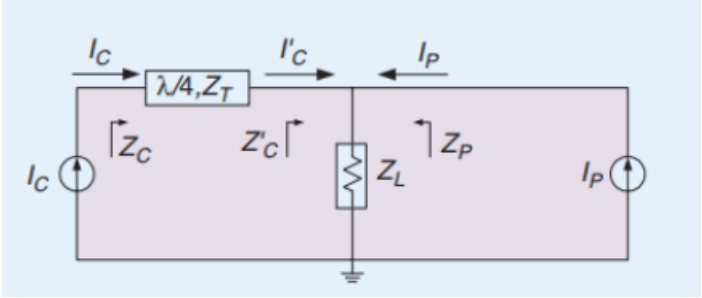


Figure 2.7: equivalent circuit of Doherty PA

and the other side impedance can be expressed as:

$$Z_2 = R_L(\frac{I_1 + I_2}{I_2}) \tag{2.21}$$

The two current sources only have amplitude differences and converge onto the load resistor R in the same phase. This arrangement affects the load impedance seen by one of the current sources by the presence of the other current source. For instance, the impedance seen from Z_1 can be increased if I_1 and I_2 operate in phase but decreases if they run out of phase.

The Doherty amplifier operates on the same concept as discussed above. The basic equivalent circuit of Doherty PA topology is shown in Fig 2.7. It consists of two amplifier circuits: one referred to as the Carrier or Main PA and the other as the Peaking PA, and a $\lambda/4$ transmission-line-based impedance inverter. The Main PA is typically biased in AB or B class, while the Peak PA is usually biased in class C. Both PAs have their output terminals matched to 50 ohms.

In the following equation, Z_c is the transmission line's characteristic impedance, and I_1 and I_2 represent the main and peak current. When the output signal is below the 6 dB power-back-off region, only the main PA is active; the impedance seen from the main PA is a constant and can be expressed as:

$$Z_{main} = \frac{Z_c^2}{Z_L} \tag{2.22}$$

The Peak PA activates when the input signal power reaches a certain threshold, generally larger than 6dB power back off from the maximum total output power (Vout is between Vout,peak/2 and Vout, peak). Now, the impedance seen from the main PA is as follows:

$$Z_{main} = \frac{Z_c^2}{\frac{I_1+I_2}{I_1} Z_L} \tag{2.23}$$

When the peak amplifier is activated, the impedance for the main will be lower with the increase of I_2. The peak amplifier keeps the Main PA close to voltage saturation by

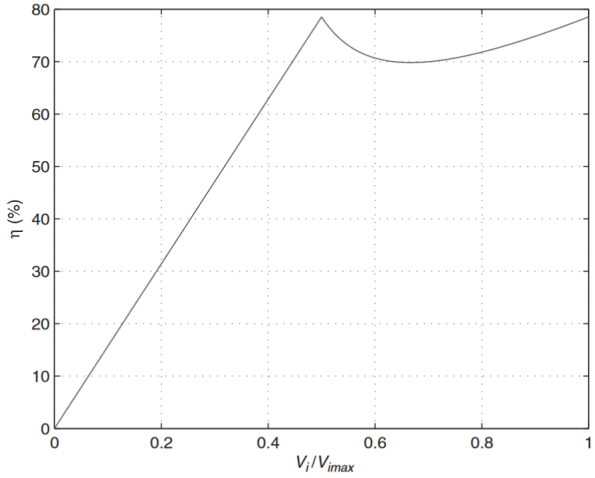


Figure 2.8: Doherty efficiency curve versus input voltage

pulling down its load. Thus, the output current of the Main PA increases while its drain voltage remains constant. Figure 2.8 depicts the overall efficiency of the Doherty power amplifier as a function of the normalized input voltage. Compared to traditional power amplifiers, the overall average drain efficiency improves significantly.

2.5. FIR FILTER FOR SAMPLING NOISE SUPPRESSION

One 5G mobile communication goal is to achieve simultaneous two-way communication. Such a system allows devices to simultaneously conduct uplink and downlink communication, enabling real-time conversations, video calls, data transfer, and more without waiting. However, in these systems, the elimination of a SAW filter between the TX output and RX requires a stringently low transmitter noise floor, such as -156dBc/Hz, which is necessary at the RX band to avoid RX desensitization[12].

Let's review the topologies that enhance noise performance in the RX band. Using an FIR-like configuration, the DTX could achieve a low noise floor with less complexity among those topologies. The following section introduces the structures of several FIR-based DTXs, including the direct FIR filter, the transformer-based mixed-domain FIR filter, and the mix-domain transformer-based FIR filter combined with a switch capacitor PA. These FIR topologies exhibit significant noise suppression. We will compare their noise and power efficiency performance in the following subsections.

2.5.1. DIRECT FIR-BASED QUANTIZATION NOISE FILTER

In 2011, Wagdy[13] proposed a new transmitter architecture, a direct digital-to-RF modulator with an Embedded RF FIr-based filter to achieve the out-of-band noise requirements for most standards localized at the corresponding RX band. This digitally modulated TX architecture is scalable and wideband and exploits the advantages of modern

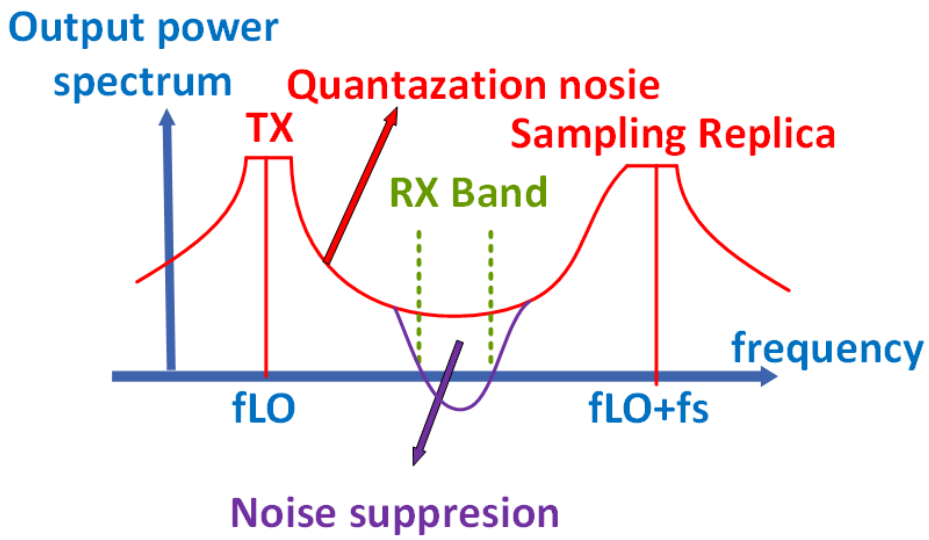


Figure 2.9: FIR DDRM output power spectrum

technologies. In his work, instead of aiming to reduce the global out-of-band quantization noise, it filters specifically at RX frequencies by implementing an FIR filter function. The FIR filter function is embedded in DTX, which acts directly at radio frequency and can be realized with moderate complexity. Note that the most challenging out-of-band noise requirements are localized at the corresponding RX band. Figure 2.9 shows the output power spectrum of the RF modulator with and without an FIR filter.

It is readily apparent from Figure 2.9 that employing FIR filtering significantly reduces the dominant noise at the frequency of the RX band. In practice, the FIR filter structure can be easily implemented by summing the output of several correctly sized RF modulators shown in Fig. 2.10. By changing the coefficient of each TX or the RF current contribution value of each TX, a quantization noise notch is realized in the RX band. Finally, a fourth-order FIR filter comprises four RF modulators, each preceded by a delay flip-flop (FFS). The benefits of this structure are that the RF FIR filter decreases the quantization noise floor at the RX band by more than 22 dB. However, this DTX needs a more linear summation of the output.

2.5.2. TRANSFORMER-BASED MIXED-DOMAIN FIR FILTER

The Mixed-Domain FIR filter was introduced in [6], which presents an S-band RF I/Q power DAC TX with an embedded mixed-domain FIR filter to suppress out-of-band quantization noise. One challenge in FIR-based quantization noise filtering from past research is that embedding FIR filters in switching-class PAs is ineffective due to the solid digital control word to the amplitude/phase nonlinearity, adversely affecting filtering[23]. In [17], to combat the conductance-to-solid amplitude/phase nonlinearity of switching-class digital PAs, a transformer-based FIR architecture is proposed that en-

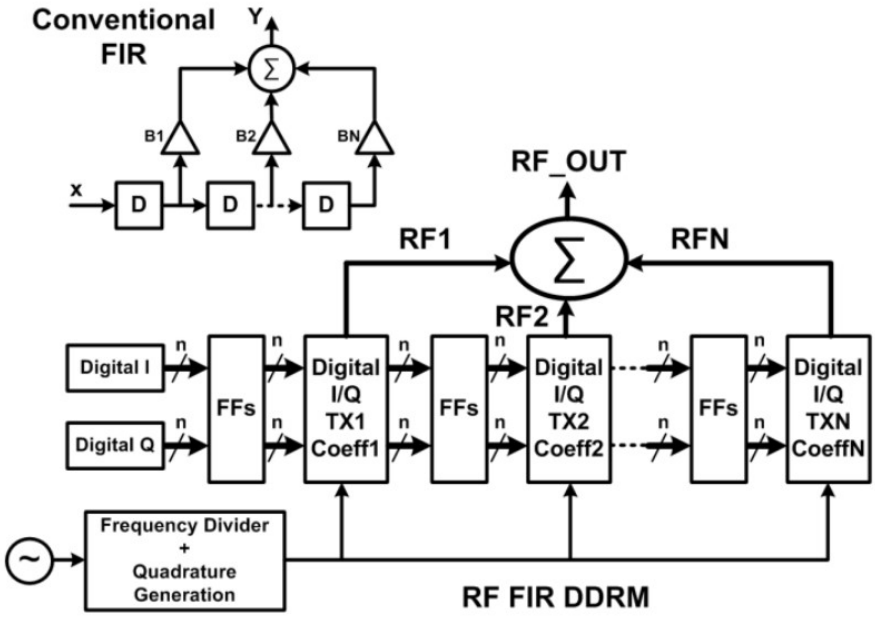


Figure 2.10: The FIR IQ DDRM architecture ([13])

sures the completion of filtering after the nonlinearity [6].

Figure 2.11 presents the structure of the transformer-based FIR filtering configuration, where the baseband data of PA #1 is delayed with respect to that of PA #2, and summation is performed across the transformer. The key insight is that the transformer participates in the FIR filtering by providing the necessary addition of delayed signals. Hence, filtering is functionally completed after conductance, which avoids amplitude/phase nonlinearity [6]. As the transformer is nominally a linear summer, the filtering quality is unaffected by the nonlinearity and improves the filtering performance.

2.6. SWITCHED-CAPACITOR POWER AMPLIFIER (SCPA) ARCHITECTURES

However, the topologies discussed above have a vital drawback. Because they all use typical current-combined RF power amplifiers, which leads to drastic variations in drain impedance, this kind of variation will severely increase the nonlinearity of the digital transmitter, such as AM-AM distortion, and cause an increase in the effective noise floor. Based on that condition, switched-capacitor power amplifiers provide an excellent solution to resolve this issue, address variations in source impedance associated with the digital control word, and enhance the transmitter's linearity for effective noise floor suppression.

The SCPA offers the advantage of a stable output impedance throughout the digital

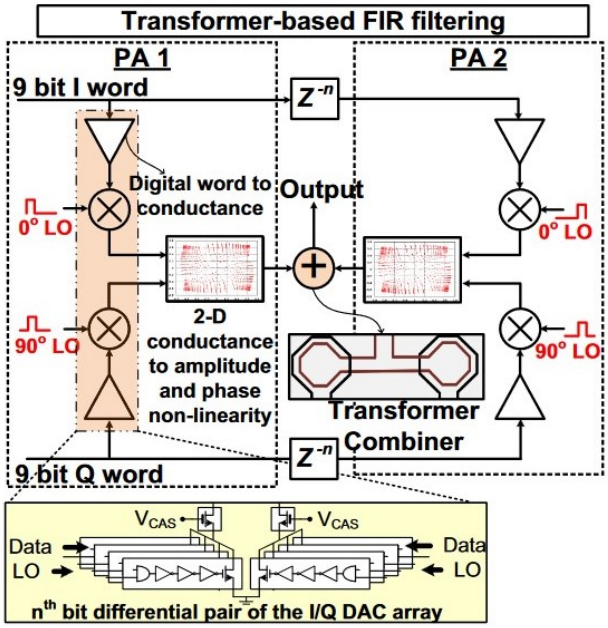


Figure 2.11: proposed transformer-based FIR filtering with addition across the transformer([6],p.414)

control world, which will be elaborated on in the subsequent section. This characteristic enhances the transmitter's linearity and improves the FIR summation's effectiveness. Yoo [29] introduced a digital-based switch-capacitor power amplifier architecture in 2011 that achieves output amplitude control by precisely controlling charge transfer in a capacitor array.

A block diagram of an SCPA is shown in Fig. 2.12. The switched-capacitor PA (SCPA) comprises an array of precision capacitors and a bandpass matching network. The array of capacitors can switch at the RF carrier frequency between the supply voltage and ground or hold at signal ground [28]. Based on a digital code applied proportionately to the envelope signal's amplitude, specific bottom plates are switched between supply voltage and GND at the RF carrier frequency. Capacitors that are not selected remain connected to signal ground. As a result, the total capacitance linked to the matching network remains constant since no top plate is ever switched. Hence, the frequency response is fixed, and the bandpass matching network must not be tuned over envelope amplitude.

Based on the preceding discussion, it is evident that the SCPA technique avoids the nonidealities associated with conventional DPA and achieves high accuracy due to the precision capacitance ratios that CMOS technology traditionally provides.

To calculate the output power and power efficiency of the SCPA, note that the SCPA operates like a class-D PA with a capacitive voltage divider in series resonance with the matching network[29]. The output voltage can be quantized by capacitance and the total array capacitance. The output voltage Vout can be described as:

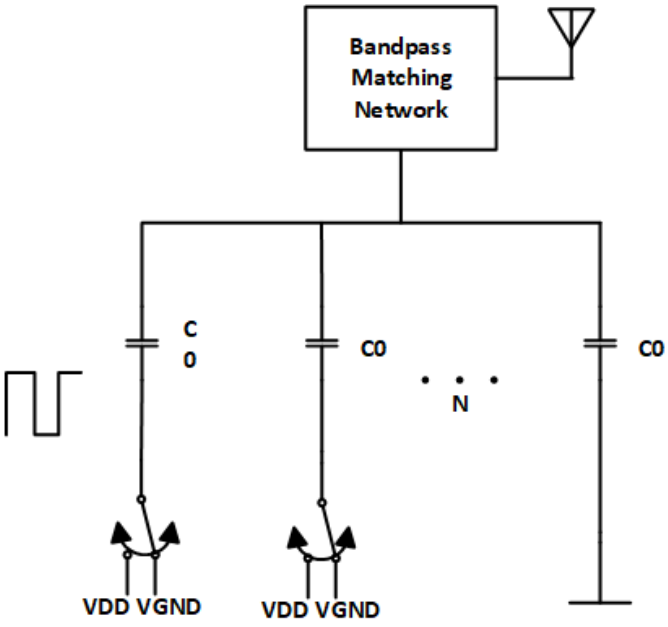


Figure 2.12: ideal single-ended SCPA

$$V_{\text{out}} = \frac{C_{on}}{C_{tot}} \cdot V_{\text{DD}} \tag{2.24}$$

If we define n as the number of unit capacitors switched between the supply voltage and ground, N is the total number of capacitors, and R_{opt} is the calculated optimal resistance; the output voltage can be expressed as follows:

$$V_{\text{out}} = \left(\frac{n}{N}\right) V_{\text{DD}} \tag{2.25}$$

Due to the Fourier series, the fundamental component of the output voltage is:

$$V_{\text{out}} = \frac{2}{\pi}\left(\frac{n}{N}\right) V_{\text{DD}} \tag{2.26}$$

Therefore, the total output power can be shown as:

$$P_{\text{out}} = \frac{2}{\pi^2}\left(\frac{n}{N}\right)^2 \frac{V_{\text{DD}}^2}{R_{\text{opt}}} \tag{2.27}$$

The dynamic power required to charge and discharge the capacitance is:

$$P_{\text{SC}} = C_{\text{in}} V_{\text{DD}}^2 f \tag{2.28}$$

The C_{in} is just a series of on-capacitance and off-capacitance. Hence is equal to:

$$C_{\text{in}} = \frac{n(N-n)}{N^2} \cdot C_{tot} \tag{2.29}$$

The power-added efficiency is defined as:

$$PAE = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{sc}}} \tag{2.30}$$

$$= \frac{4n^2}{4n^2 + 2\pi^2 n(N-n)\dot{f}C_{tot}R_{opt}} \tag{2.31}$$

Theoretically, the switched capacitor power amplifier (SCPA) consistently offers higher power-added efficiency due to reducing capacitive parasitics with CMOS technology scaling.

2.6.1. LINEARITY COMPENSATION FOR SCPA

An ideal SCPA does not suffer any linearity to efficiency trade-off as a conventional current-mode DPA. An SCPA with ideal switches and capacitors is linear, with no signal amplitude or phase distortion. In practical scenarios, the AM-AM distortion is small in an SCPA due to the excellent capacitor matching. However, AM-PM distortion can become prominent due to various factors. One such factor is the difference in resistance between the NMOS and PMOS devices. As the digital control word changes, the modulation of envelope amplitude will transfer into the time domain, inducing phase modulation and resulting in AM-PM distortion.

To solve that issue, A novel voltage-tolerant power amplifier, the Class G Switched-Capacitor[26], has been proposed to enhance the AM-PM distortion. The Class G SCPA can utilize the supply voltage twice to improve output power and linearity simultaneously. The increase in output power is straightforward, as it can take advantage of higher supply voltage. As for the improvement in linearity, it addresses AM-PM distortion by compensating for the time differences in two operating regions, which will be discussed in detail.

Class-G amplifier has two operating modes, VDD mode and 2VDD mode. The circuit of two different modes is shown in Fig 2.13.In the VDD mode, the input capacitance can be described as:

$$C_{\text{in}} = \frac{n(N-n)}{N^2} \cdot C_{tot} \tag{2.32}$$

The transition charging/discharging time can be further derived as:

$$\Delta t = C_{tot} \times \frac{(N-n)}{N^2} \frac{V_{\text{DD}}}{I} \tag{2.33}$$

As shown in this equation, the increased number of the units cell(n), the shorter the charging/discharging time, corresponding to a frequency shift, resulting in a leading behavior in the AM-PM [16].

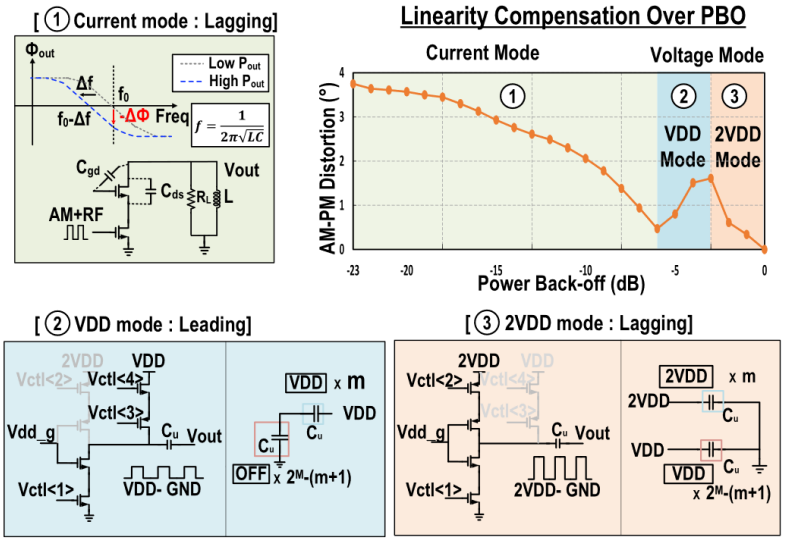


Figure 2.13: Class G linearity compensation[16]

When operating in the 2VDD mode, C_{in} is just C_{tot}, and the transition time can be described by the equation:

$$\Delta t = C_{tot} \times \frac{(N+n)}{N^2} \frac{V_{\mathrm{DD}}}{I} \tag{2.34}$$

Hence, the time becomes longer with increased n, leading to a lag in AM-PM distortion. The final simulation results of AM-PM distortion are shown in Fig. 2.13, and we can see from the graph that the Class G SCPA could have better linearity performance.

2.7. CONCLUSION AND DISCUSSION

This chapter examines several commonly used performance metrics for transmitters (TXs). It then provides a comprehensive explanation of power amplifiers, detailing their essential functions and characteristics. We then describe and evaluate two distinct digital transmitters (DTXs) types, highlighting their respective advantages and applications. Finally, we present innovative designs of noise-suppression DTXs and switched-capacitor power amplifiers, discussing their contributions to enhancing overall system performance.

3

SWITCHED CAPACITOR POWER AMPLIFIER AND POWER COMBINE DESIGN

Modern wireless transmitters (TXs) must adhere to increasingly rigorous specifications to meet the stringent spectral mask requirements for the FCC standards. These strict conditions significantly complicate the design of the final stage of the transmitter, particularly the Power Amplifier (PA). The PA must achieve several critical objectives:

1. High Efficiency: The PA must be designed for high efficiency, converting as much input power as possible into the output signal to minimize energy loss.

2. Linearity: Linearity in the PA is crucial for maintaining spectral purity, ensuring that the transmitted signal adheres to the required spectral mask without causing interference.

3. High Output Power: The PA must deliver sufficient output power to ensure the transmitted signal maintains strength over long distances or through obstacles.

The Switched-Capacitor Power Amplifier (SCPA) improves AM-AM linearity and achieves high power efficiency [29]. Additionally, specific techniques must be applied to meet the desired peak power specification of 30 dBm at carrier frequencies. Consequently, this design incorporates an SCPA with a transformer-based matching network and power combining to boost output power. The chapter consists of three sections: Section 3.1 explains the principles of the switched-capacitor power amplifier, Section 3.2 covers switch size optimization strategies and methods for enhancing power efficiency, Section 3.3 introduces the driver design, and Section 3.4 concludes the chapter.

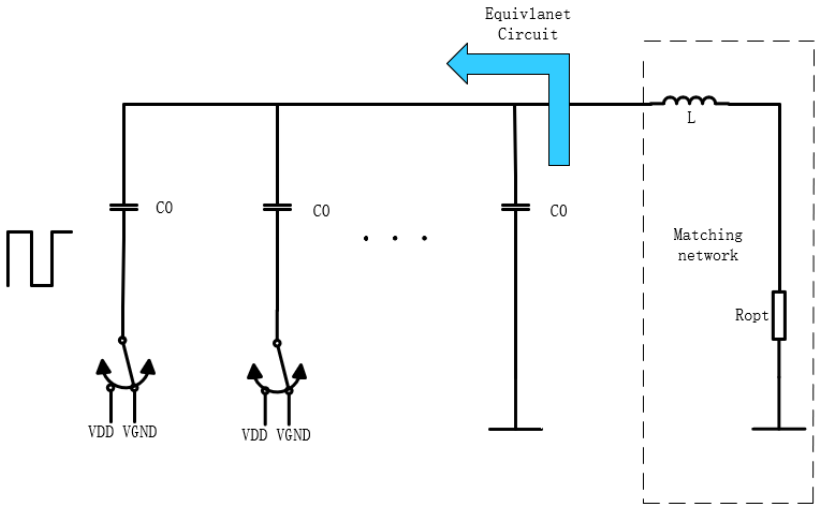


Figure 3.1: Simplified SCPA

3.1. THE PRINCIPLE OF SCPA

To achieve higher efficiency and improved spectral purity in power amplifiers, there is growing interest in more efficient switching PA circuits and systems operating linearly for nonconstant envelope modulation [29].A power amplifier known as the switched-capacitor power amplifier (SCPA) has gained momentum. It utilizes an array of precisely assigned capacitors that function as a voltage divider. This design takes advantage of advanced CMOS scaling, which helps to reduce parasitic effects, enables faster switching operations, and ensures more accurate capacitance ratios. These benefits allow the SCPA to operate at higher frequencies while maintaining excellent AM-AM linearity, ensuring efficient performance in high-speed applications.

While considering efficiency, linear analog PAs are not energy-efficient because their DC power consumption remains constant even when the RF output power decreases. This inefficiency is further exacerbated when using modulation schemes with high PAPR (e.g., QAM) [28]. In contrast, the SCPA behaves like a Class-D amplifier, where its DC power decreases as its RF output power decreases. This occurs because some of the units connected to the ground are deactivated, preventing them from consuming DC power and providing high efficiency. Figure 3.1 shows the simplified structure of the SCPA. It shows that the SCPA comprises an array of precise switching capacitors and a matching network. The top plates of all capacitors are connected, while the bottom plates of the active (on) capacitors are connected to a CMOS switch that toggles between VDD and ground in each RF cycle. In contrast, the bottom plates of the inactive (off) capacitors

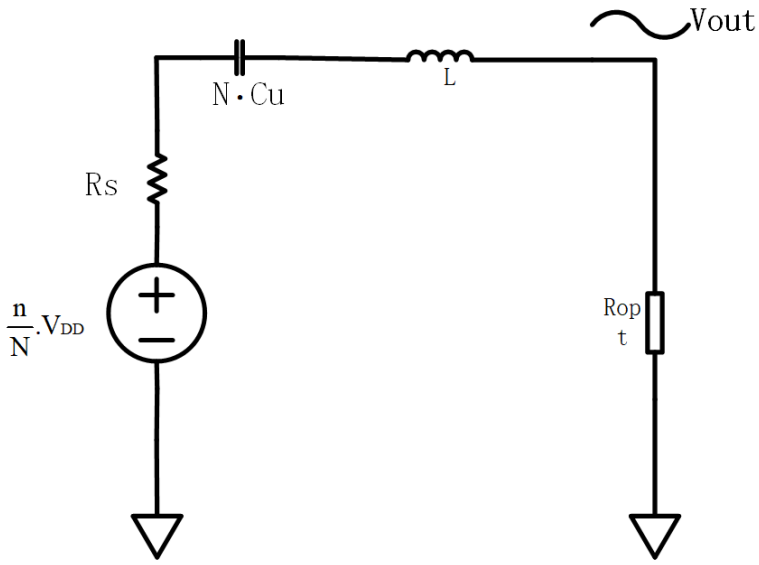


Figure 3.2: Thévenin-equivalent circuit of SCPA

are directly tied to the ground. The selection of on and off states for the capacitors is determined by the input digital amplitude code. A significant advantage of this structure is that the total capacitance remains unchanged with the input code, as all the capacitors' top plates are connected. Figure 3.2 illustrates the equivalent circuit seen from the matching network. In this context, the switching array functions as a Thévenin voltage source, scaled by n/N, where n is the number of unit capacitors whose bottom plates are switched between VDD and ground, and N is the total number of capacitors. The output voltage level is proportional to the input digital code and reaches its maximum when n is equal to N. The total capacitance of the system is given by:

$$C_{\text{total}} = N \cdot C_u$$

Where C_u represents the unit capacitance, R_s refers to the non-ideal switch resistance arising from the circuit's MOSFETs operated as lossy switches. This code-independent capacitance simplifies the design of the matching network by ensuring stable impedance across varying input codes.

The voltage and power equations of the SCPA have been discussed in Chapter 2.6. Now, attention must be focused on key variables in the equivalent circuit. First is R_{opt}, which determines the maximum RF output power of the SCPA. Additionally, we must consider the non-ideal switch resistance R_s and the unit capacitance C_u. It is essential to choose appropriate values for both the MOSFET size and the unit capacitance C_u to optimize the performance of the SCPA, ensuring both optimal efficiency and functionality.

3.2. SCPA DESIGN TECHNIQUE

3.2.1. POWER COMBINE TECHNQIUE

First, the structure is designed based on the output power requirements, initially focusing on the desired delivered RF output power of 30 dBm. In doing so, a drawback of the SCPA technique must be considered: it relies on fast-switching, deeply-scaled CMOS transistors, which require operation at relatively low supply voltages. This makes it challenging to achieve the high output power levels needed for communication applications such as WiMax and LTE.[27]. According to the total output power equation, the maximum power is achieved when the number of active unit cells n equals the total number of available unit cells N. Therefore, the maximum power $P_{\max}$ equation is given by:

$$P_{\max} = \frac{2}{\pi^2} \frac{V_{\mathrm{DD}}^2}{R_{\mathrm{opt}}} \tag{3.1}$$

Where V_{DD} is the supply voltage and R_{opt} is the optimum load resistance. Achieving the required high output power of 30 dBm (1 W) would theoretically require a very small R_{opt}, around 1 ohm. However, attaining such a low resistance value is impractical due to limitations in circuit components and physical constraints.

To address this problem, a power-combining method using on-chip transformers is adopted. These techniques increase the effective load resistance seen by the individual amplifier units, making it feasible to achieve the desired output power without encountering the impractical constraints of a 1-ohm load. This approach not only increases the peak output power but also enhances dynamic range by selectively activating or deactivating individual SCPA cores [27]. Additionally, to implement an FIR structure as a notch filter (this will be discussed in Chapter 4), a high-resolution SCPA comprising an appropriate power combining scheme is needed.

To achieve the required power, we need to determine both the number of parallel transformer stages and the turn ratio of each transformer. When all power amplifiers (PAs) have the same output impedance, the impedance R_{opt} seen by each SCPA (switched-capacitor power amplifier) is given by:

$$R_{\mathrm{opt}} = \frac{R_L}{N_{PC} \cdot m^2} \tag{3.2}$$

Where N_{PC} represents the number of parallel stages, and m is the turn ratio of each transformer, R_L is the load resistance, which is set to 50 Ω. Consequently, the equation for the maximum power with the transformer is:

$$P_{\max_\mathrm{transformer}} = N_{PC}^2 \cdot m^2 \cdot \frac{2}{\pi^2} \cdot \frac{V_{\mathrm{DD}}^2}{R_{\mathrm{L}}}. \tag{3.3}$$

However, a larger turn ratio will dramatically increase the power loss of the transformer. Therefore, the turn ratio m is fixed at 1. Under these conditions, to meet the required power delivery while balancing area efficiency, an 8-way transformer configuration with eight SCPA-RFDACs is selected, as shown in Figure 3.3, and the R_{opt} for each is set to 6.25 Ω.

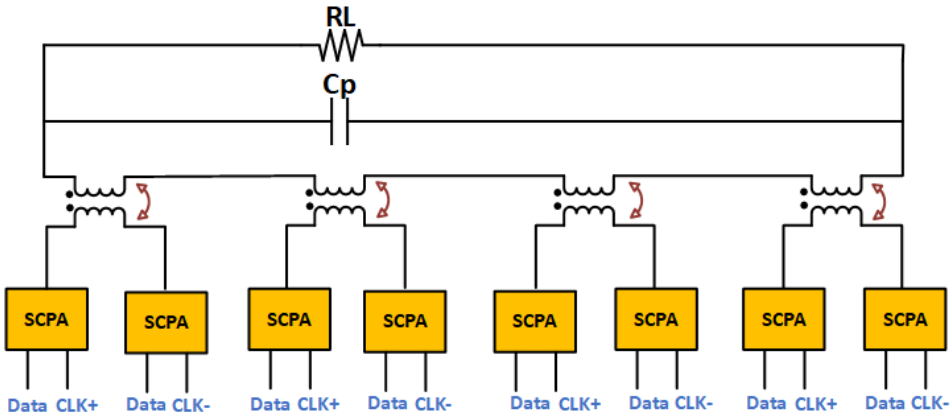


Figure 3.3: Block diagram of the eight-way power-combined SCPA

This configuration ensures both power efficiency and a compact design. The required delivered RF power for each SCPA is 21 dBm, and with R_{opt} set to 6.25 Ω, it can achieve 22 dBm RF output power, meeting the desired specifications.

3.2.2. REAL TRANSFORMER ELECTRIC MODEL

In this design, transformers are crucial components in power combining techniques, and an electric model of the real transformer has been developed for simulation purposes. Based on [17], the equivalent circuit model of a real, lossy transformer captures practical imperfections, including leakage inductor and magnetic coupling inductor. The leakage inductance and magnetizing inductance is represented by the term:

$$\text{Leakage inductance} : (1-k^2)L_p \tag{3.4}$$

$$\text{Magnetizing inductance} : k^2 L_p \tag{3.5}$$

Here, k is the coupling factor, which ranges from 0 (no coupling) to 1 (perfect coupling). Additionally, resistive losses are modeled by resistors R_p and R_s, which arise due to the limited quality factor of the primary and secondary inductors. The input to the transformer is the differential RF output of the power amplifier, as shown in Figure 3.3. Hence, the transformer is split into two identical units, the values are divided by two and its overall structure is illustrated in Figure 3.4. At the core of this model is an ideal transformer with a specified turns ratio, representing perfect energy transfer between the windings.

3.2.3. SCPA OPTIMIZATION STRATEGY

Secondly, the power loss of the circuit must be considered. For simplicity, the capacitor, inductor, and transformer matching network are assumed to be ideal. Therefore, the remaining losses are related to the transistor switch's on-resistance, the dynamic

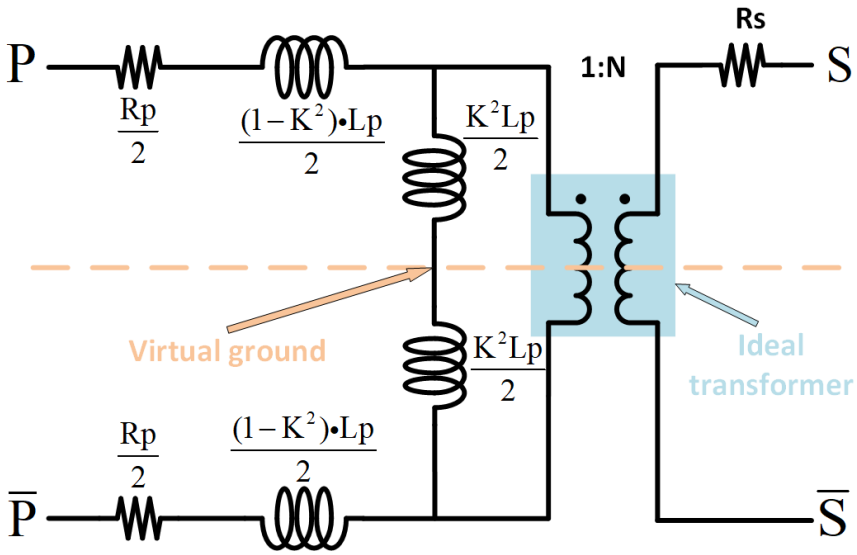


Figure 3.4: Lossy Transformer equivalent circuit

power consumed during charge and discharge cycles, and the driver power consumption. Based on the equivalent circuit loss model, the key variables influencing these losses are R_s and C_u (with R_{opt} set to 6.25 Ω). These factors collectively reduce the RF peak power. A circuit simulation is conducted at 2.5 GHz to determine the maximum output power, optimizing the CMOS device size and unit capacitance value for peak performance.

Figure 3.5 presents the simulation results of PRF versus the multiply factor and unit capacitance. The multiplication factor reflects the number of transistors connected in parallel, where each transistor has a length of 40 nm and a width of 120 nm for NMOS and 240 nm for PMOS.

In the graph, the output power increases as the multiplication factor rises. This is because, in the equivalent circuit diagram, R_s represents the on-resistance of the NMOS and PMOS transistors. By increasing the transistor size through the addition of more parallel transistors, the on-resistance R_s decreases. According to equation (3.4), this reduction in R_s increases RF output power, as lower on-resistance allows more power to be delivered to the load.

$$P_{\text{max}} = \frac{2}{\pi^2} \cdot V_{\text{DD}}^2 \cdot \frac{R_{\text{opt}}}{R_s + R_{\text{opt}}}, \tag{3.6}$$

However, the on-resistance decreases as the number of transistors increases, but parasitic capacitance eventually becomes significant. This parasitic capacitance consumes power during operation, lowering the power amplifier's efficiency. Furthermore, a larger multiplication factor increases the chip area, imposing additional design challenges. As a result, the multiplication factor is set to 220 to balance RF output power and efficiency.

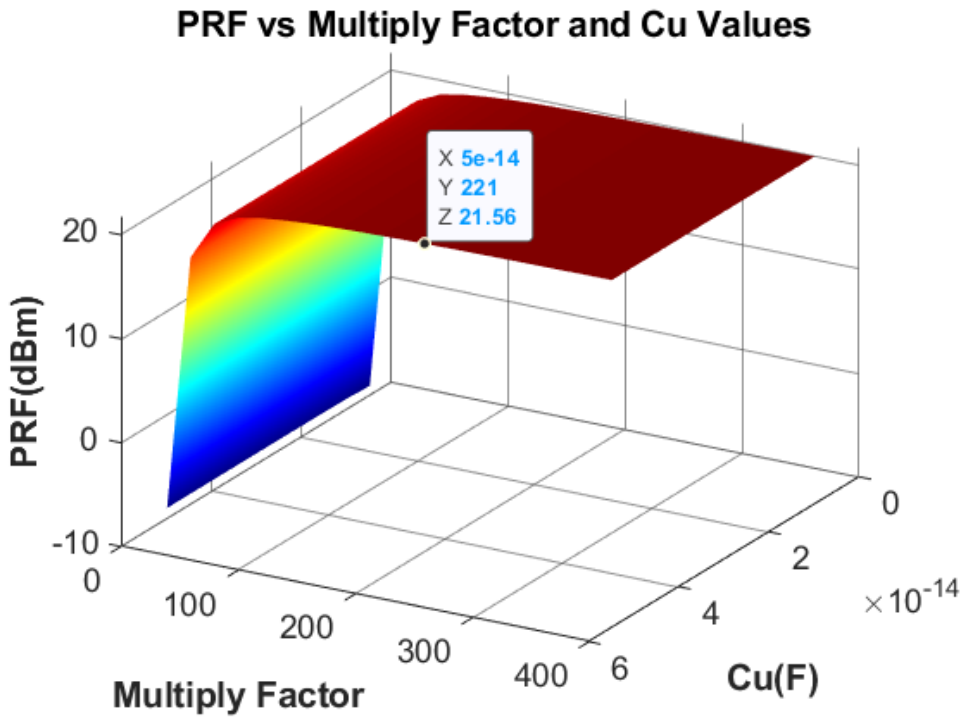


Figure 3.5: Unit capacitor optimization

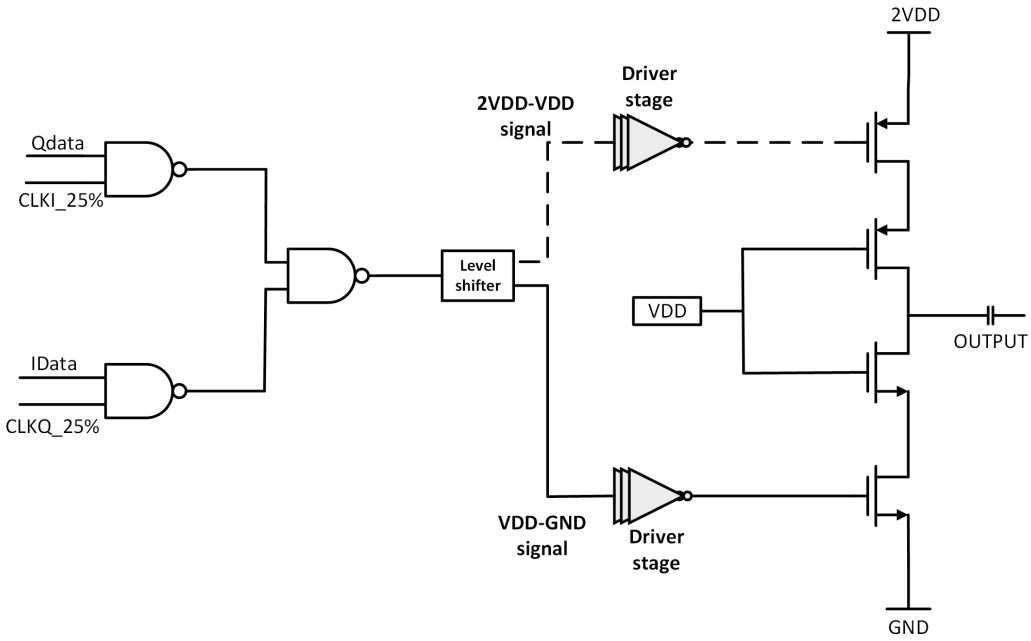


Figure 3.6: Single SCPA Unit

Since we have already determined the transistor size, the next step is to choose the value of the SCPA unit capacitance. Based on simulation results, it is important to note that while the unit capacitance C_u does not directly affect the output power, a larger C_u increases dynamic power dissipation, as shown in equation (2.28). Therefore, a smaller unit capacitance ($C_{\text{series_unit}}$) is preferred to reduce power consumption.

After careful evaluation, a unit capacitance of 5 fF was selected to balance performance and practicality. The point on the graph shows that with $C_u = 5$ fF and a multiplication factor of 220, the output power reaches 21.5 dBm, which meets the requirements for a single SCPA.

3.3. DRIVER DESIGN OF THE SCPA

In the Digital Power Amplifier (DPA) concept, the relatively large input capacitance (C_{in}) of the SCPA segments is driven by digital signals. A cascoded version of the SCPA is employed to increase power output further. As a result, the voltage swing must be sufficiently high to activate the power amplifier properly. The design of the single SCPA unit is depicted in Figure 3.6.

The single SCPA unit includes a level shifter and a chain of inverters with increasing sizes, designed to transmit the digital drive signal from the logic gates to the input of the power amplifier. This arrangement ensures that the large input capacitance is effectively driven, allowing efficient signal transmission to the output stage. To further improve the system's overall efficiency, the rise and fall times of each inverter stage must be mini-

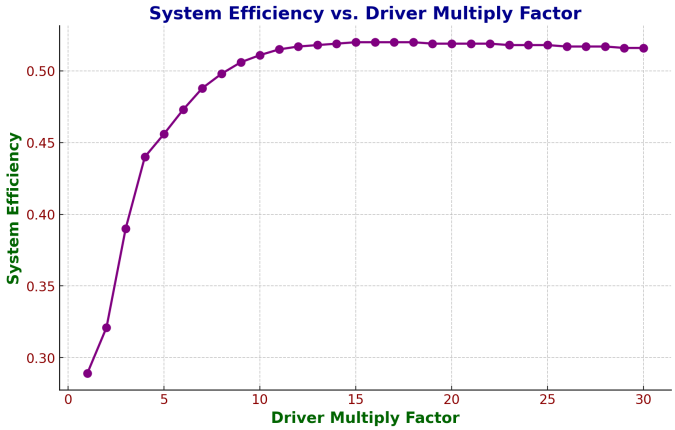


Figure 3.7: System efficiency vs Last stage driver multiply factor

mized, enabling energy-efficient driver operation while allowing the power amplifier to achieve its highest efficiency [8]. Consequently, the size and the number of stages in the inverter chain must be carefully selected.

Since the unit size of the SCPA is fixed, the load capacitance C_L is 27 fF for the PMOS and 17 fF for the NMOS. To drive the SCPA effectively, the larger capacitance (27 fF) is selected as C_L for designing the inverter chain. Using different drivers for the PMOS and NMOS inputs could result in signal misalignment, causing the SCPA to operate in a region where both the PMOS and NMOS are simultaneously active, which would reduce the output power.

The equivalent switch resistance R_{dr} of the inverter determines the driver's ability to manage the load, where a lower R_{dr} corresponds to a larger and more powerful driver. However, a large driver will result in unnecessary power consumption, as the load power amplifier may already be driven adequately. Because the load is fixed, there is an optimal size for the last stage driver. This optimization is achieved by carefully selecting the multiplication factor for the final stage driver in the inverter chain to drive the SCPA efficiently.

Figure 3.7 shows the circuit simulation results of system efficiency as a function of the last stage multiplication factor. The system efficiency initially increases, then decreases. The optimal value for the multiplication factor is 15, where the system efficiency reaches its peak.

As shown in Figure 3.8, the propagation inverter chain can be analyzed to evaluate its performance. Here, C_L represents the PA input capacitance, and f is the ratio of the size of one inverter to the next in the chain.$C_{\text{dr,i1}}$ represents the input capacitance of the first inverter in the chain. $C_{dro,N}$ represents the output capacitance of the last inverter in the chain. Assuming the chain has N stages, each consecutive inverter is scaled by a factor of f. The overall effective fan-out is defined as:

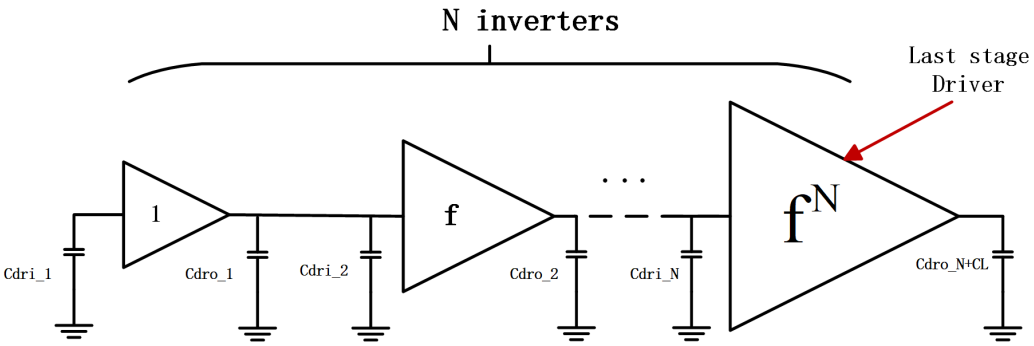


Figure 3.8: Driver buffer chain with its parasitic capacitance

$$F = \frac{C_L + C_{dro,N}}{C_{\text{dri},1}} \tag{3.7}$$

The values of N and f are unknown. As described in [22], a trade-off exists between a given technology's power consumption and driver speed. To achieve the highest power efficiency, f has a known relationship with R_{drN} and t_{p0}, where t_{p0} is the delay time of the minimum-sized inverter, which is 2.33 ps in 40 nm technology. The equation representing this highest efficiency relationship is:

$$f = \gamma \frac{\ln(2) R_{\text{dr1}} C_L}{t_{p0}}. \tag{3.8}$$

When the last stage size is set to 14 times the intrinsic minimum-sized inverter, its $R_{\text{dr1}} = 7.5\,\text{k}\Omega$, $\gamma = 1$, and $C_L = 27\,\text{fF}$. After calculation, the multiplication factor f is 60. Therefore, only two stages are needed, as the last stage inverter size is only 14 times its minimum size. After simulation, the first stage inverter size is set to 4 times the minimum to achieve the highest system efficiency.

3.3.1. LEVEL SHIFTER

To provide as much power as possible, a cascoded version of the SCPA is used, necessitating a level shifter's inclusion. A level shifter capable of operating at frequencies near 2.5 GHz is shown in Figure 3.9. The primary function of the level shifter is to translate input signals with a voltage swing of V_{DD} to higher voltage levels, specifically between V_{DD} and $2V_{\text{DD}}$.

The level shifter operates by utilizing complementary input signals, V_{in} and $\overline{V_{\text{in}}}$, to control the switching behavior of NMOS and PMOS transistors, effectively facilitating voltage level translation between different power domains. When V_{in} is high, NMOS transistor MN1 turns on, pulling its drain to the ground, while MN2 remains off, allowing its drain to charge up to V_{DD}. Simultaneously, PMOS transistor MP2 turns on, pulling its drain to $2V_{\text{DD}}$, while MP1 remains off, leaving its drain at V_{DD}. Conversely, when V_{in} is

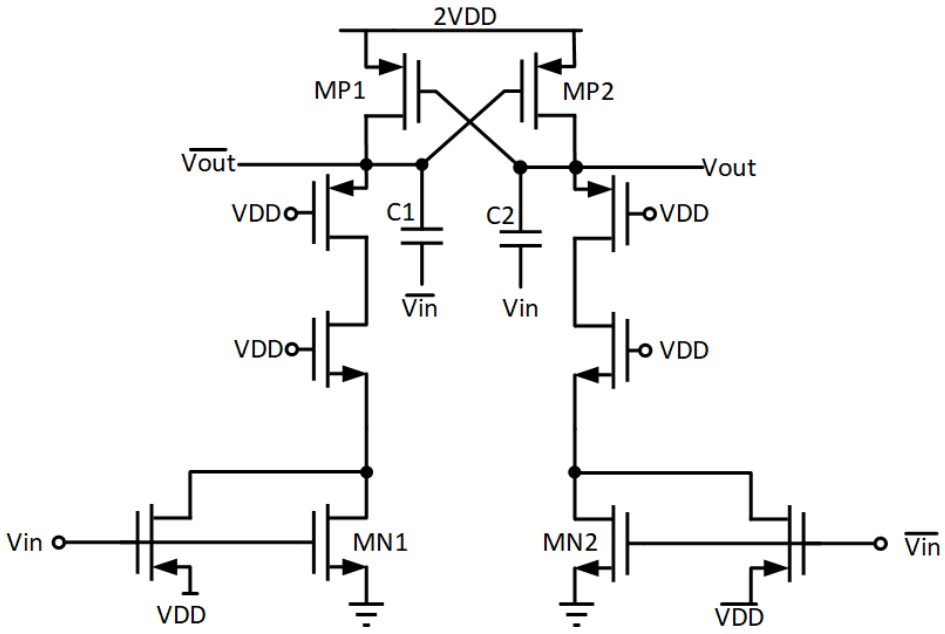


Figure 3.9: level shifter

low, the roles of the transistors reverse, ensuring that MN2 pulls its drain to the ground and MP1 pulls its drain to $2V_{DD}$. This complementary switching mechanism enables the level shifter to translate signals between low and high voltage levels, making it an essential component for interfacing circuits that operate at different voltage standards.

Capacitive coupling is employed to enhance the speed of the level shifter. Capacitors C1 and C2 are used to couple the input signals to the gates of MP1 and MP2. This coupling accelerates the switching behavior of the transistors, significantly improving the performance of the circuit[9].

3.4. CONCLUSION

In conclusion, this chapter provided an in-depth exploration of the design principles and optimization strategies for the Switched-Capacitor Power Amplifier (SCPA). It also introduced the integration of a transformer-based matching network and power-combining techniques. Furthermore, the design of the driver circuit, encompassing the inverter chain and level shifter, was discussed in detail, illustrating how these components enhance the overall system performance. These insights are vital for the effective implementation of SCPA technology in modern wireless communication systems, paving the way for enhanced performance and reliability in transmission.

4

AN 8-BIT RF DAC WITH FIR FILTER NOISE SUPPRESION

The chapter unveils the 8-bit I/Q RF-DAC circuit-level design based on the switched-capacitor PA with the power combining technique introduced in Chapter 3. It covers digital logic design, clock quadrature LO generation, and interpolation. Also, Up-sampling FIR filtering in the digital domain and mixed-domain FIR filter design are discussed, aiming to achieve a low out-of-band noise digital transmitter. The chapter is structured as follows: the implementation of the switched-capacitor RF-DAC will be covered in Section 4.1, and Section 4.2 describes the quadrature 25% clock generation. Finally, noise suppression techniques are presented in Section 4.3, and Section 4.4 will be the conclusion.

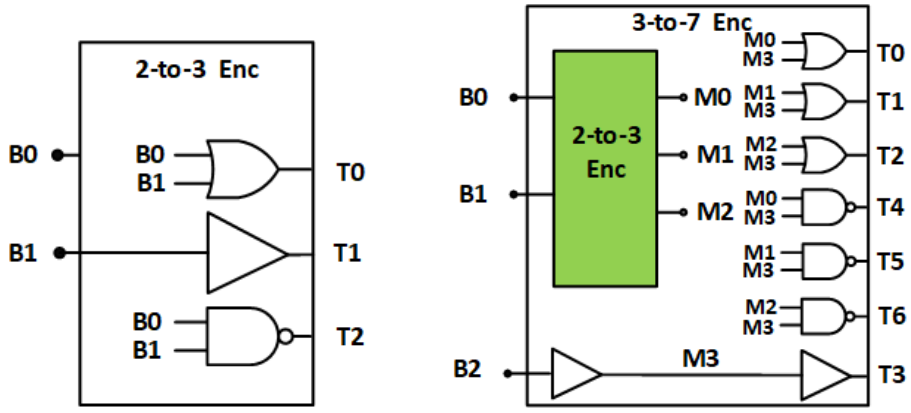
4.1. 8-BIT ALL-DIGITAL IQ RF-DAC

4.1.1. SEGMENTED RF-DAC STRUCTURE

As mentioned earlier, this work focuses on minimizing the noise of digital transmitters. The sampling quantization noise limits the dynamic range of the digital transmitter. It can be expressed as an equation of its N-bit resolution (N), the modulated signal's peak-to-average power ratio (PAPR), and the oversampling ratio(or), defined as $F_S/(2 \times BW)$, as follows [5]:

$$DR = 6.02N + 1.76 + 10\log_{10}(or) + 3 - PAPR$$

From the equation, we can infer that higher resolution improves dynamic range (DR), translating to lower sampling noise. However, this comes at the cost of increased power consumption and complexity, making it a trade-off between quantization noise, power consumption, and the overall complexity of the digital transmitter. After considering these factors, an 8-bit I/Q signal, including one sign bit, was selected for the digital transmitter..



(a) 2-to-3 Thermometer Encoder

(b) 3-to-7 Thermometer Encoder

Figure 4.1: Thermometer Encoders

Referring to above equation, the plus 3dB factor accounts for the I and Q signal operations. Based on this formula, the predicted dynamic range is 54.9 dBc, assuming a target bandwidth (BW) of 100 MHz, a PAPR of 9 dB, and a sampling frequency (F_S) of 2.5 GHz after up-sampling. This dynamic range is adequate to satisfy the transmission (TX) requirements of both current and future wireless communication systems.

4.1.2. THERMOMETER ENCODERS OF 2-TO-3 AND 3-TO-7

For high-resolution RF-DACs, binary digital signals must be converted to thermometer codes to avoid non-monotonic behavior and mid-code transition glitches. However, relying solely on thermometer-coded DACs introduces several challenges, including numerous encoders, significantly increasing chip area and power consumption. To mitigate these issues while preserving performance, a segmented approach is adopted. This method divides the DAC into a combination of binary-weighted and thermometer-coded unary cells. Specifically, an 8-bit resolution is segmented into four most significant bits (MSB) and three least significant bits (LSB), ensuring monotonicity in the mixing DAC while balancing complexity and performance. This design uses binary-to-thermometer encoders, including one 3-to-7 encoder and two 2-to-3 encoders, as illustrated in Figure 4.1.

The 2-to-3 encoder comprises a bit-wise OR gate, bit-wise AND logic, and a buffer. In this configuration, the TO and T2 outputs of the thermometer code are generated through AND and OR operations on the two binary input bits, B0 and B1, respectively. Meanwhile, B1 is directly equal to T1. The three-to-seven encoder is implemented in two stages. First, intermediate three-bit thermometer codes (BB0, BB1, BB2) are generated, with A3 buffered to equal A2, ensuring consistent output timing. In the second stage, these intermediate codes derive the final bits B0, B1, B2, B4, B5, and B6 of the 7-bit thermometer code via AND and OR operations involving A3. The B3 bit equals A3, with an extra buffer synchronizing the timing across all output bits.

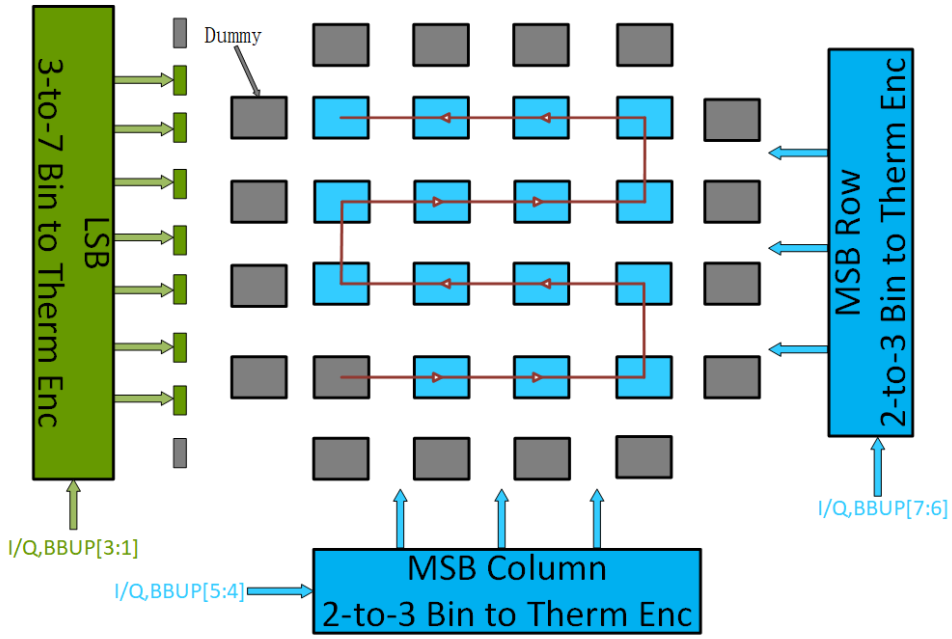


Figure 4.2: 8-bit RF-DAC floor plan

4.1.3. 8 BIT RF-DAC FLOOR PLAN

Such a complex RF-DAC design requires careful layout strategies to optimize performance. First, two times two-to-three binary-to-thermometer encoders generate column and row selection signals for the 2x2, 4-bit MSB matrix. This design requires two separate encoders to generate I/Q signal paths, ensuring area efficiency and reducing mismatch using a more compact signal routing. Besides, the LSB unit consists of eight smaller DRAC unit cells arranged in a single row (1×7) within the DRAC unit bank.

Likewise, even rows begin from the right side, while odd rows start from the left, forming a “snake” traversal pattern. This arrangement ensures that the MSB thermometer units are continuously traversed between even and odd rows, mitigating the related nonlinearity. Consequently,DNL of the RF-DAC and glitches associated with the dynamic switching of the matrix switches are effectively controlled, keeping them below one least significant bit (LSB)[1]. Further, the MSB and LSB unary matrices are surrounded by unary dummy cells to enhance matching accuracy. The overall floor plan of the 8-bit DRAC is illustrated by the arrow lines in Figure 4.2.

4.1.4. SINGLE-ENDED DIGITAL RF-DAC CELL

The RF-DAC unit cell comprises a purely digital logic section, illustrated in Figure 4.3. The digital logic section includes a decoding logic block, a retiming flip-flop, and an I/Q up-converting circuitry. Row/column selection is managed by an AND–OR decoder, determining whether a specific cell is activated. A master/slave D flip-flop (DFF) synchro-

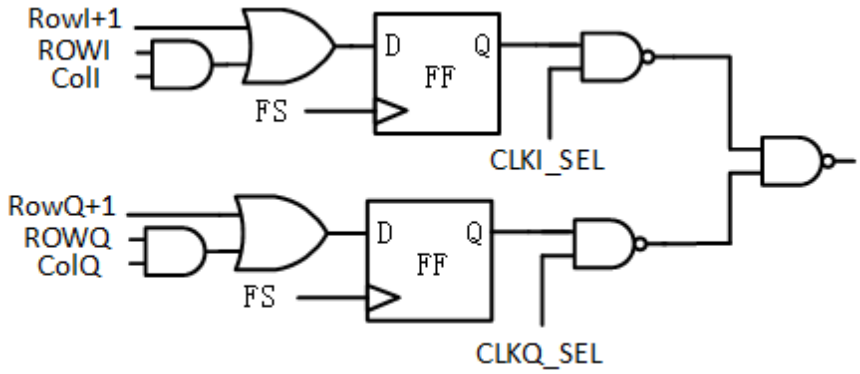


Figure 4.3: I/Q RF DAC unit cell

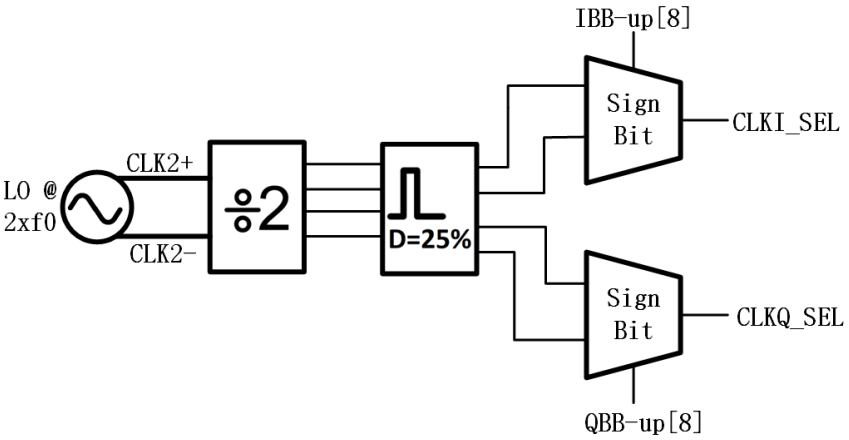
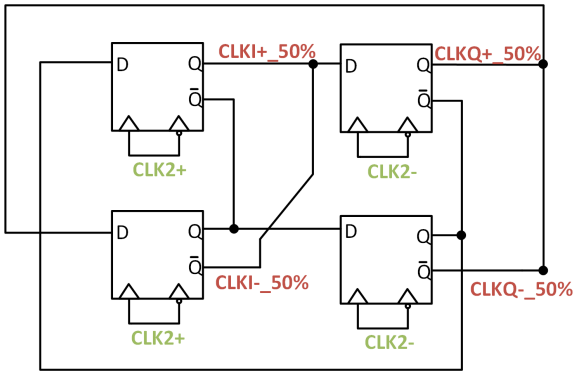


Figure 4.4: Block diagram of the clock generator implementation

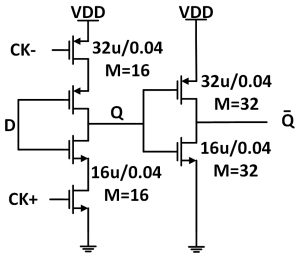
nizes all I/Q power cells with the master clock (FS) to guarantee proper timing. After synchronization, the digital data are up-converted using 25%-LO clocks through a bitwise NAND operation. Next, the up-converted I/Q bitstreams are orthogonally summed using a bitwise NAND gate to perform I/Q interleaving before being fed into the SCPA, discussed in Chapter 3. To secure consistent timing, all critical digital logic is implemented using symmetrical gates, balancing the delay from input to output and maintaining uniform fan-out.

4.2. CLOCK GENERATOR

This section describes the clock generation process, with the complete diagram of the clock generator shown in Figure.4.4.



(a) ÷2 divider topology



(b) C²MOS latch and inverter

4

4.2.1. HIGH-SPEED DIFFERENTIAL DIVIDERS

From Figure 4.4, an off-chip differential clock signal CLK2$^+$/CLK2$^-$, operating at twice the fundamental frequency ($2 \times f_0$), is applied to cascaded divide-by-two frequency dividers. This setup generates the desired local oscillator (LO) signal at the fundamental frequency f_0. The configuration produces four differential quadrature clock signals: $\text{CLKI}^+_{50\%}$, $\text{CLKQ}^+_{50\%}$, $\text{CLKI}^-_{50\%}$, $\text{CLKQ}^-_{50\%}$, each with a 50% duty cycle and a 90° phase difference.

This division is achieved by a ÷2 divider, and its topology arrangement is shown in Figure 4.5a. The divider is designed utilizing flip-flop technology, comprising four C^{2}MOS latches arranged in a loop [1]. The input of each latch is denoted as D, and the outputs are Q and $\overline{Q}$. The C^{2}MOS latch schematic is shown in Figure 4.5b. Notably, each C^{2}MOS latch includes an additional inverter, and their outputs are connected back-to-back. This connection aligns the four differential clock phases. It improves quadrature clock phase accuracy to provide signal integrity, prevent corruption, and align the divided output signals[5]. Besides, to enhance the divider's frequency of operation, the clock and data inputs of the C^{2}MOS latches are reciprocated compared to a conventional C^{2}MOS latch. This lowers the delay of the latch and, hence, diminishes the entire loop delay of the divider[1].

4.2.2. DIFFERENTIAL QUADRATURE 25% DUTY CYCLE CLOCK GENERATOR

The design employs an I/Q power-cell sharing method, where the upconverted I and Q signals are digitally added together while sharing a single power cell. This configuration necessitates using 25% duty cycle LO clocks to prevent overlapping the summed I and Q signals. Moreover, the non-overlapping nature of the 25% duty cycle ensures that the I and Q signals are processed independently without interference, preserving their orthogonality. This is essential for maintaining accurate modulation and demodulation in communication systems. The approach enhances overall efficiency and helps conserve valuable die area in integrated circuits, making it particularly advantageous for compact, high-performance designs.

The designated 25% duty cycle LO generation is performed using an AND gate. As illustrated in Figure 4.6, the duty cycle generation circuit produces four-phase 25% LO

clocks by performing a bit-wise AND operation on the corresponding LO pairs, resulting in the desired 25% duty cycle clock. It is worth mentioning that the AND gates are implemented symmetrically to equalize clock delays, ensuring balanced timing and load condition[5].

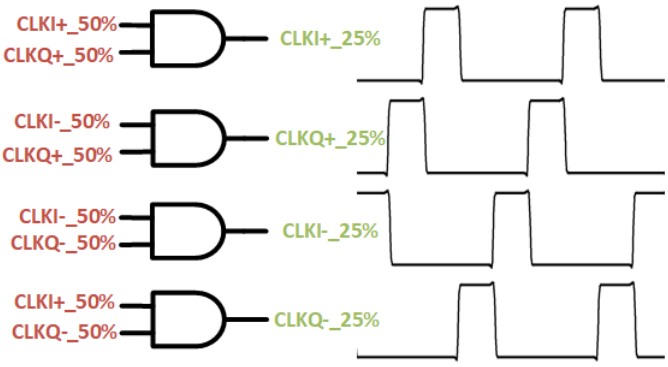


Figure 4.6: AND operation to generate 25% duty cycle LO

4.2.3. COMPLEMENTARY QUADRATURE SIGN BIT SELECTOR

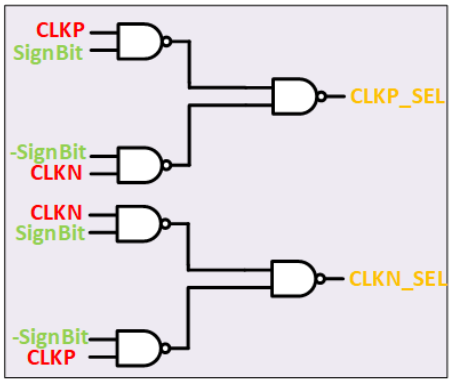
The proposed DTX system is designed based on I/Q signed data, where each sample comprises $N-1$ unsigned bits representing amplitude, accompanied by one sign bit. This configuration allows for efficient representation of the signal's amplitude and its associated sign. The signed I/Q data consists of two explicit sign bits, IBB-up[8] and QBB-up[8], to differentiate between negative and positive I/Q values.

As mentioned, this design exploits signed I/Q data, resulting in a doubled swing in the signed IQ approach, which leads to higher output power. However, the digital power amplifier can only process the amplitude level of the digital I/Q data[5]. To address this, a sign bit selector must be embodied into the RF-DAC to select the output LO based on the sign of the I/Q data. As depicted in Figure 4.4, a sign bit selector utilizes a multiplexer to select the data. The multiplexer, shown in Figure 4.7a, utilizes a NAND gate to select the corresponding clock signal. This configuration is employed after the generation of the 25% clock. Based on the selection control, the complementary LO pairs can be exchanged, thus covering all four quadrants of the constellation diagram. Figure 4.7b shows the specific clock pairs.

4.3. LOW OUT-OF-BAND NOISE DIGITAL TRANSMITTER ARCHITECTURE

4.3.1. DIGITAL BASEBAND SIGNAL PROCESSING

One of the challenges associated with digital-intensive transmitters (DTX) is the contamination caused by sampling spectral replicas, mainly due to the absence of low-pass filters. According to the sampling theorem [20], the analog output of a DAC inherently includes sampling spectral replicas. These replicas arise from sampling complex digital baseband signals and are subsequently translated to the RF band, where they can



(a) Multiplexer for Sign bit selection

SignQ	SignI	CLKIP	CLKQP	CLKIN	CLKQN
0	0	fLO, 0	fLO, 90	fLO, 180	fLO, 270
0	1	fLO, 180	fLO, 90	fLO, 0	fLO, 270
1	1	fLO, 180	fLO, 270	fLO, 0	fLO, 90
1	0	fLO, 0	fLO, 270	fLO, 180	fLO, 90

(b) Sign bit and related complementary clock pairs

Figure 4.7: Overview of the sign bit selector and its complementary clock pairs

degrade the transmitted signal's quality, introducing unwanted distortions.

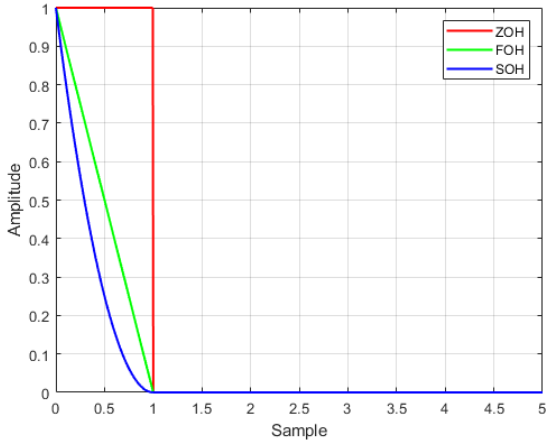
The signal can be partially reconstructed digitally through upsampling and digital filtering (interpolation) using a larger sampling frequency F_S to mitigate the effects of sampling spectral replicas. This frequency F_S should be an integer ratio of the carrier frequency f_{LO} to avoid timing synchronization issues [18].

To achieve the wideband suppression of sampling spectral replicas (SSRs), interpolation FIR filters such as zero-order hold (ZOH), first-order hold (FOH), second-order hold (SOH), or even higher-order hold can be implemented. These filters are characterized by sinc, sinc², sinc³, and sinc^N transfer functions, respectively. These filters' impulse and magnitude responses are depicted in Figures 4.8a and 4.8b. These filters are utilized to upsample complex baseband signals at F_{BB} by a factor of 4, extending up to F_S (equivalent to f_{LO}), thereby effectively suppressing the SSRs located $n \cdot F_{Ss}$ away from f_{LO} and reducing them below the modulator noise floor [18]. The selection of F_{BB} and the upsampling factor is crucial as it balances the location of the SSRs, data path power consumption, and filter complexity. This design opts for FOH interpolation filters in the digital baseband processing as a trade-off between in-band distortion and out-of-band replica suppression.

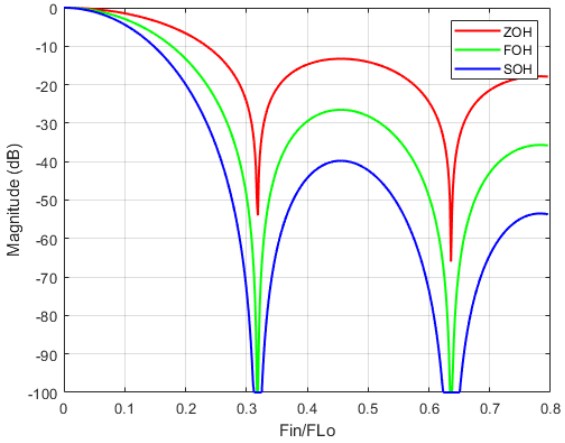
To conclude, interpolation upsampling filters are vital in the digital domain, as they ensure that the upsampled signal remains smooth, continuous, and free of alias artifacts. By effectively relocating sampling replicas beyond the desired frequency range and reducing undesirable frequency components, these filters significantly enhance the signal integrity for further processing or analysis.

4.3.2. MIXED-DOMAIN FIR FILTER DESIGN TECHNIQUE

In modern wireless communication systems, spectrally efficient signal transmission reduces out-of-band noise and boosts overall system performance. One proposed method to address this issue in digital I/Q transmitters incorporates advanced signal generation algorithms, as introduced in [19], which especially target out-of-band noise reduction in the receiver (RX) band.



(a) ZOH, FOH, SOH Impulse response



(b) ZOH, FOH, SOH Magnitude response

Figure 4.8: ZOH, FOH, SOH filters

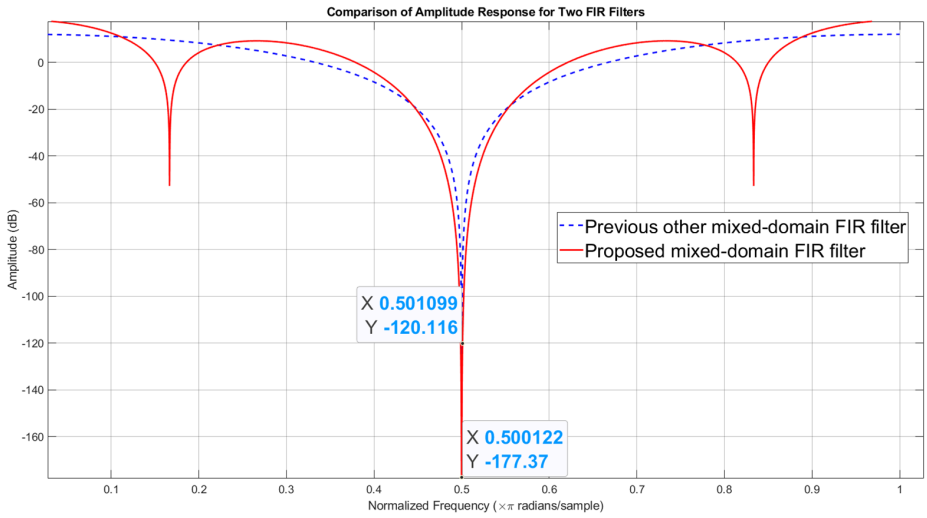


Figure 4.9: Fir filter amplitude response

Another approach highlighted in [6] suggests embedding a finite impulse response (FIR) filter directly into a Cartesian digital transmitter. In this regard, the transformer functions as a linear summer, adding delayed replicas of signals and effectively concluding the filtering process. However, the FIR filter design in [6] relies on a cascaded two-tap structure, which provides only limited noise suppression and is sub-optimalfor reducing out-of-band noise in the RX band.

To address this limitation, our proposed design introduces an 11-tap emulation of an 8-tap symmetric FIR filter. The corresponding filter transfer function can be expressed as

$$H(s) = G\left(1 + 2e^{-2s\tau} + e^{-4s\tau} + e^{-6s\tau} + 2e^{-8s\tau} + e^{-10s\tau}\right) \tag{4.1}$$

This new FIR structure offers significantly greater noise suppression, as demonstrated by the comparison in Figure 4.9. The improved design leads to enhanced notch depth and better performance in out-of-band noise reduction, making it superior to the previously proposed structure.

Finally, the design is embedded within a highly linear and mismatch-resilient switched-capacitor digital power amplifier (PA) architecture. This mixed-domain FIR filtering approach reasonably enhances notch depth and overall noise suppression. Consequently, the linear summation performed by the FIR filter strongly suppresses quantization noise in the receiver (RX) band, thereby enhancing overall system performance. The detailed functional block diagram of the proposed 8-way mixed-domain digital transmitter (DTX) is shown in Figure 4.10, which illustrates all DTX components and the function of the embedded FIR filter.

This design illustrates the MATLAB RF output in Figure 4.11. The figure compares the signal without the mixed-domain FIR filter to the results of the proposed FIR filter, and

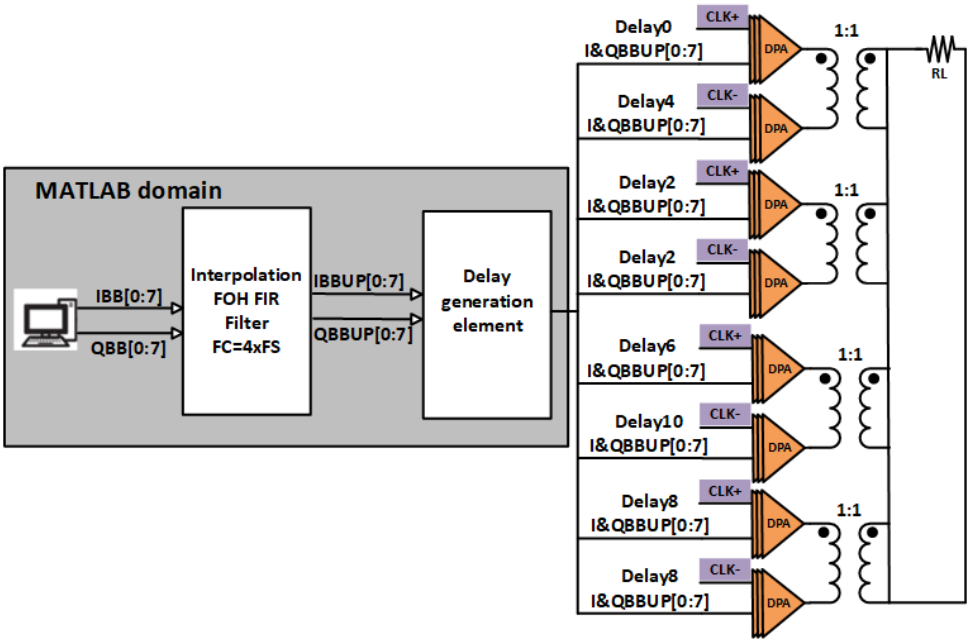


Figure 4.10: Detailed block diagram of the proposed 8-way mixed domain DTX

the filter from [7], highlighting the creation of a deep notch at a specific frequency. The detailed results from accurate circuit simulations will be presented in Chapter 5. The notch location is directly influenced by the delay and maximum output level, offering 30 dB more suppression than the previous mixed-domain FIR filter, demonstrating a significant improvement. In this design, the delay is introduced by a True Single-Phase Clock (TSPC) flip-flop, which operates with the local oscillator (LO) and generates a 400 ps delay. As a result, the notch is positioned at 625 MHz relative to the main tone. This precise notch placement is crucial for effective out-of-band noise suppression, ultimately enhancing overall system performance.

4.3.3. DELAY ELEMENT DESIGN

In this design, a TSPC D-flip-flop is used to generate a precise delay of 400 ps, corresponding to the period of the LO clock. The schematic shown in Figure 4.12 illustrates how the circuit achieves this functionality.

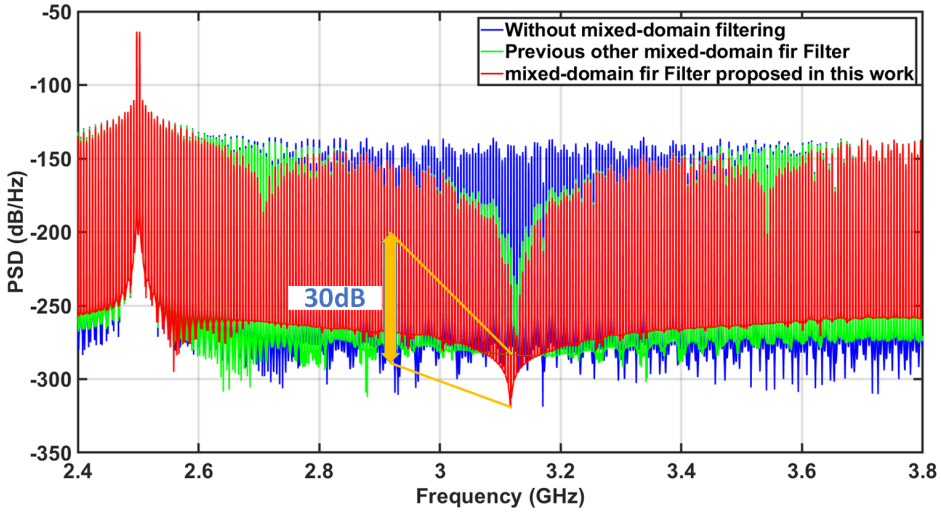


Figure 4.11: Maltalb simulation RF output with various fir filter

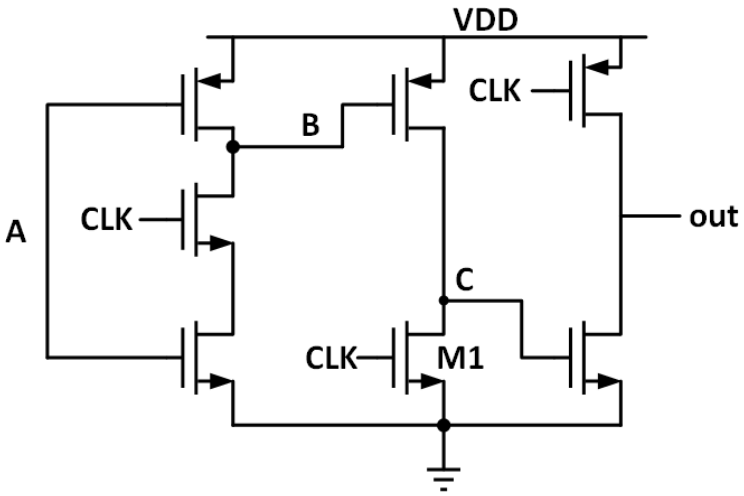


Figure 4.12: TSPC flip-flop

M1 must be strong enough to pull the drain nodes to a logical ZERO when the corresponding PMOS transistor is active, ensuring proper operation. To achieve this, M1 is sized with a width approximately three times larger than the PMOS. This sizing guarantees that the M1 has sufficient drive strength to maximize the speed and efficiency of the circuit.

The delay line in Figure 4.13 generates corresponding delay data, with a maximum of 10 increments, each contributing up to 400 ps. This delay data can be employed in the

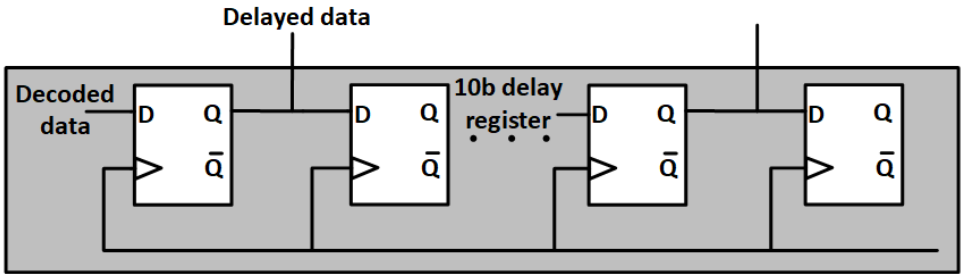


Figure 4.13: Delay generation chain

design of the FIR filter.

4.4. CONCLUSION

This chapter demonstrates the design and implementation of the 8-bit I/Q switch-capacitor-based RF-DAC and proposes a structure embedding interpolation and mixed-domain FIR filtering to reduce out-of-band noise.

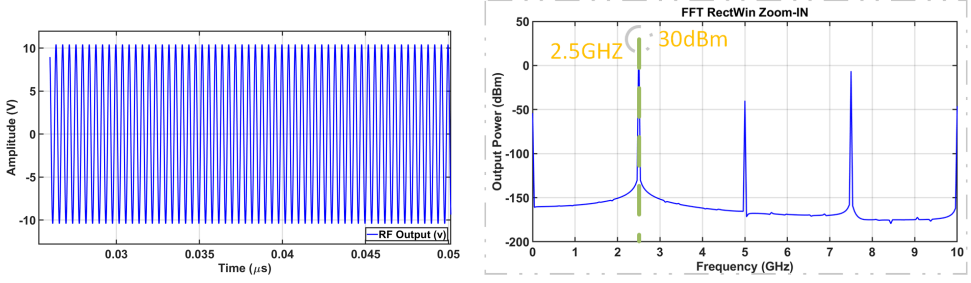
5

SIMULATION RESULTS

Previous chapters discussed the various parts of the proposed DTX. This chapter presents and analyzes key simulation results. First, a static simulation of the power amplifier's output power and efficiency will be examined versus frequency and input code. Next, the power spectral density (PSD) and output power spectrum will be compared with and without the FIR filter. Lastly, a dynamic simulation using a 160 MHz 64-QAM signal will be performed to analyze the transmitter's performance.

5.1. STATIC SIMULATION

The DTX is first characterized by static, continuous-wave (CW) simulation. The peak performance of the proposed DTX occurs when the IQ code is set to its maximum code, i.e., 127. Figure 5.1 shows the time-domain signal and the peak output power, which reaches 30 dBm.



(a) static test time

(b) static test frequency

Figure 5.1: static test

The pie-chart graph of the DTX power consumption at peak power is shown in Figure 5.2. The RF output power is 1.1 W, with the capacitor switching loss ($P_{sw\,loss}$) at 0.83 W and the MOS resistor loss ($P_{R\,loss}$) at 0.41 W, contributing to the total drain DC power.

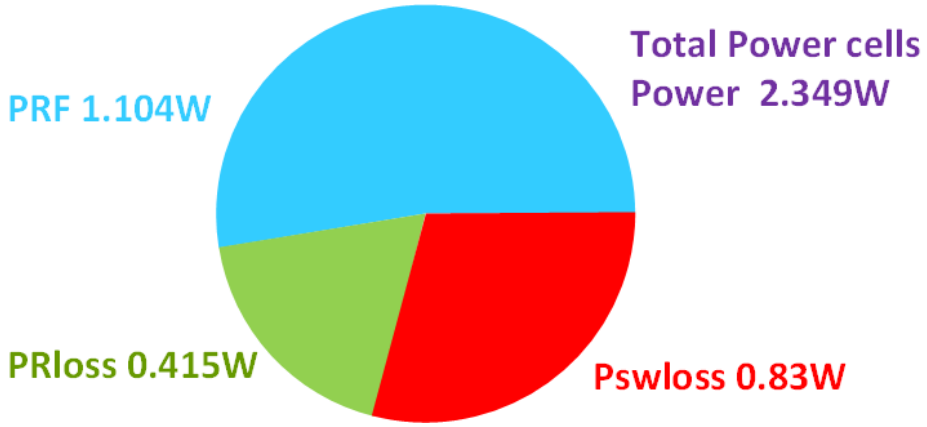


Figure 5.2: power consumption at full power 2.5GHz

The drain efficiency and system efficiency are simulated versus the RF output power. Drain Efficiency (DE) is calculated by:

$$\mathrm{DE}(\%) = 100 \times \frac{P_{RF_Out}}{P_{DC_Power_Cells}} \tag{5.1}$$

System Efficiency (SE) is calculated by:

$$\mathrm{SE}(\%) = 100 \times \frac{P_{RF_Out}}{P_{DC_Power_Cells} + P_{DC_All_Blocks}\,\text{(Except clk generator and data delay element)}} \tag{5.2}$$

To evaluate the DTX Power Back-Off (PBO) performance, the corresponding I_{BB}/Q_{BB} data are swept from 127 to 16. The measured drain and system efficiencies as a function of output power at a frequency of 2.5 GHz are presented in Figure 5.3. The peak system efficiency is approximately 52.3%, while the efficiency at a 6 dB power back-off is 30.69%.

To assess the linearity of the transmitter, we conducted simulations examining the relationship between input code and output voltage, as well as the phase of the output voltage. The results are illustrated in Figure 5.4. Both plots demonstrate how the output voltage behaves as the IQ code increments from 16 to 127. The graph analysis shows that the amplitude modulation to amplitude modulation (AM to AM) exhibits a linear behavior. In contrast, the transition from amplitude modulation to phase modulation (AM to PM) reveals noticeable distortion, indicating the presence of non-linear characteristics in the output phase to the input code.

5.2. TWO TONE SIGNAL SIMULATION

Here is the simulation of the two-tone test without and with the proposed FIR filter. Figure 5.5 shows the time domain simulation.

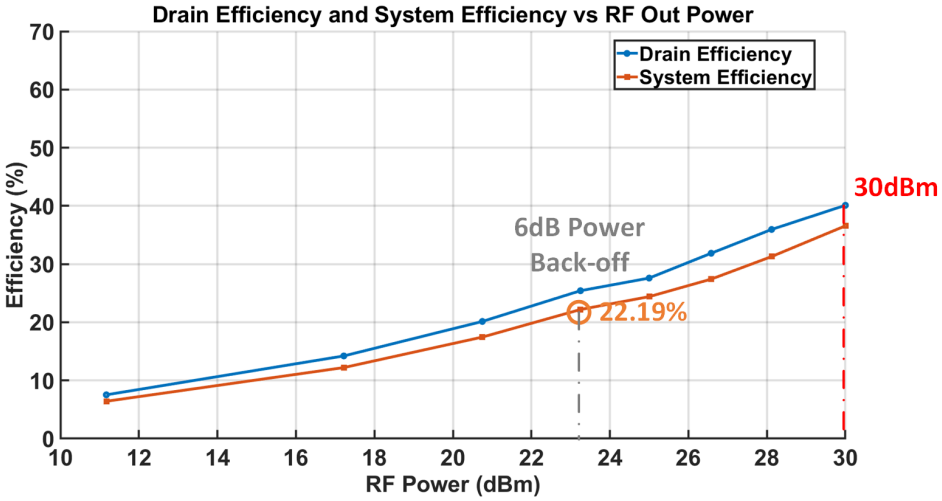


Figure 5.3: Drain Efficiency and System Efficiency vs. RF Output Power at 2.5GHz

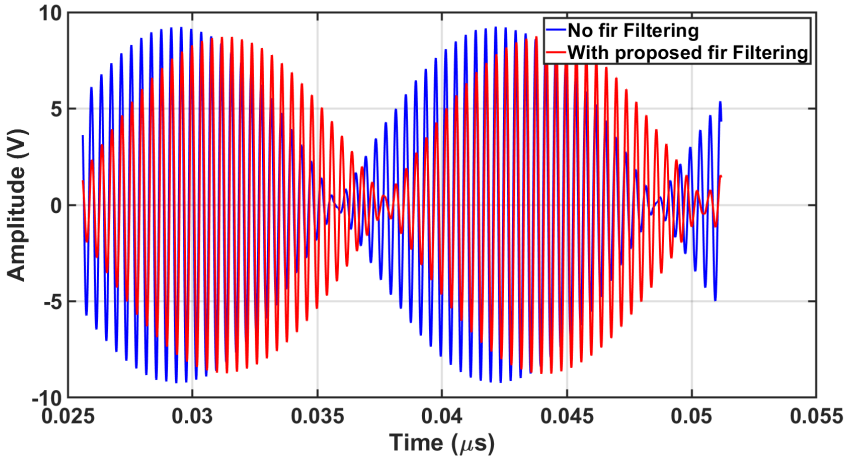
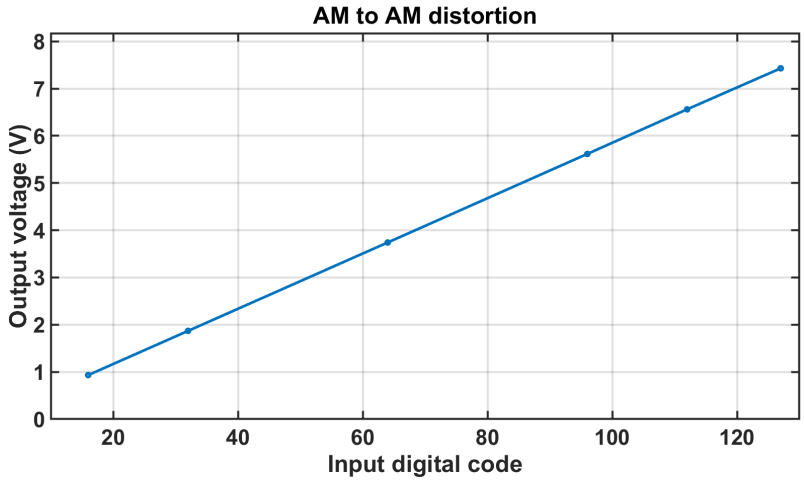
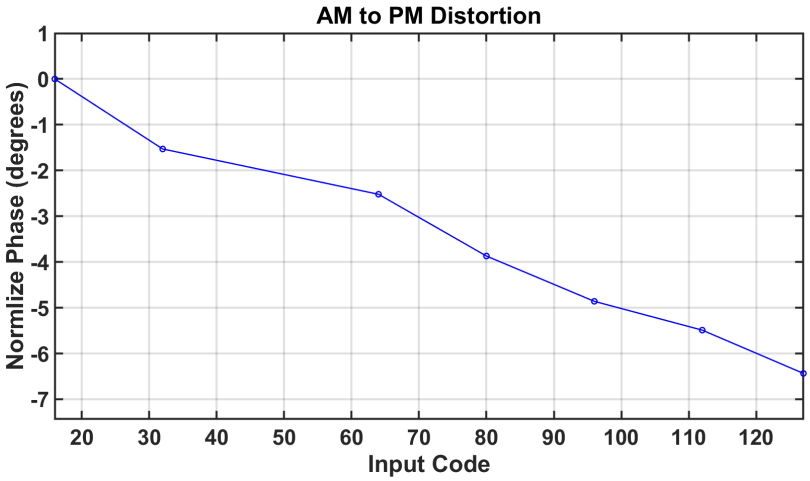


Figure 5.5: two tone signal for with and without filter time domain

In Figure 5.6, we present the simulation results using the proposed FIR filter. The target signal achieves an two tone output power of 23.4 dBm and an average noise output power level of -58.5 dBm. This proves the effectiveness of the proposed FIR filter in enhancing signal quality and reducing noise.



(a) AM to AM distortion



(b) AM to PM distortion

Figure 5.4: Linearity simulation

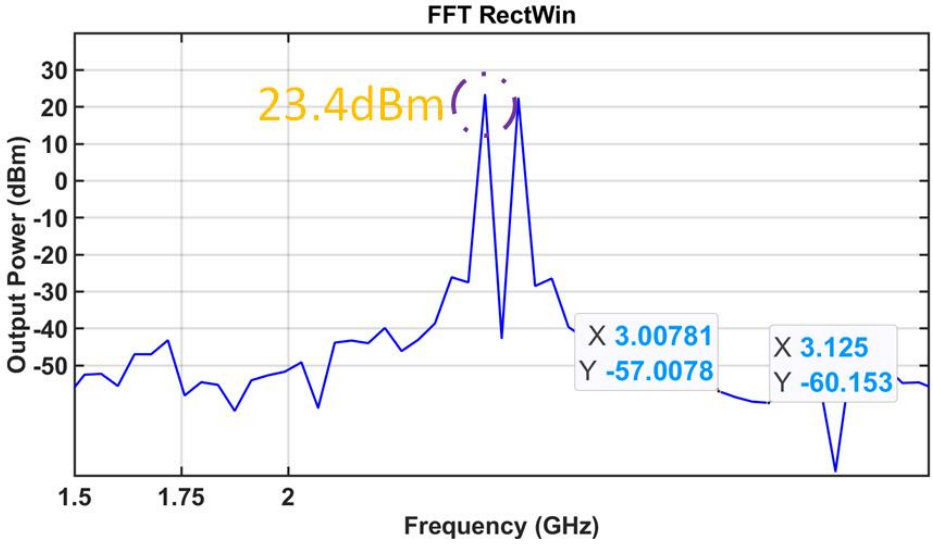


Figure 5.6: two tone signal with fir filter frequency domain

The power spectral density (PSD) comparison shows a deep notch in noise suppression within the target band, indicating that the noise level is improved by 30 dB in the target frequency band.

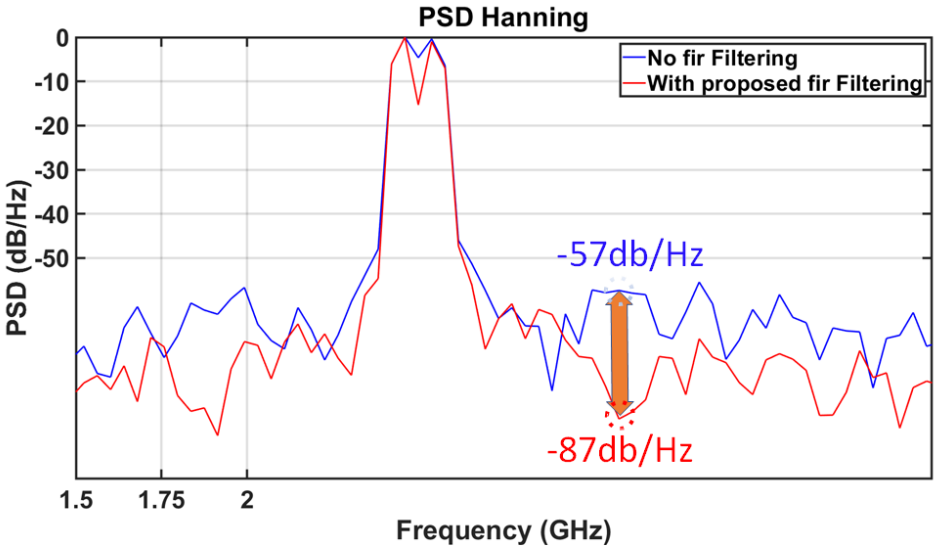


Figure 5.7: two tone signal for with and without filter configurations

5.3. DYNAMIC SIMULATION

To test the modulation scheme's linearity and the see the noise suppression, 64 quadrature amplitude modulation (QAM) signals with a bandwidth of 160 MHz were generated in MATLAB and fed into the circuit.

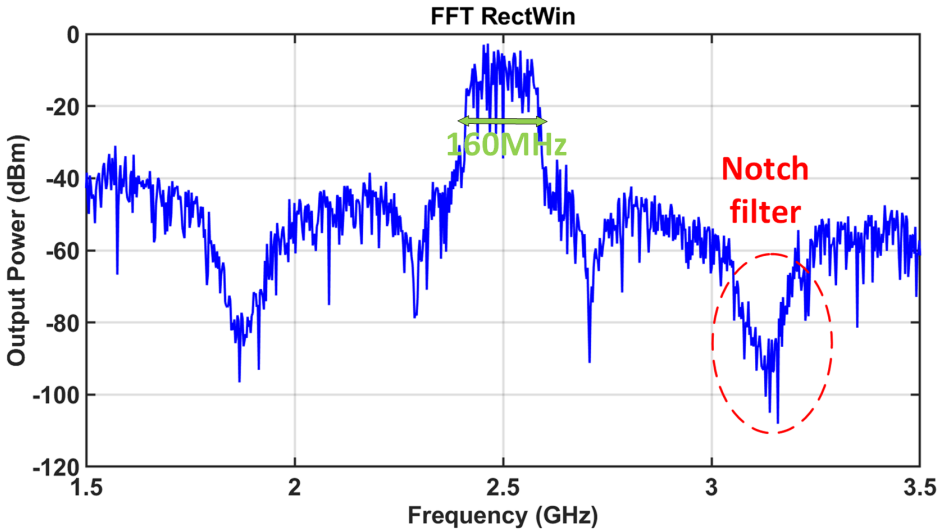


Figure 5.8: 64QAM clos-in output spectrum

	JSSC 2011[10]	JSSC 2015[30]	RFIC 2013[6]	ISSCC 2013	This work
Architecture	Switched-capacitor digital polar TX	Quadrature Switched-Capacitor PA	Class E/F digital IQ TX with embedded 2-tab mixed-domain FIR	Class D^{-1} current-combined digital IQ TX	Switched-capacitor digital IQ TX with 8-way power combined mixed domain FIR
Frequency	2.25 GHz	2.0 GHz	2.4 GHz	2.44 GHz	2.5 GHz
Resolution	6b amplitude, off chip phase mod	7b IQ	9b IQ	13b IQ	8b IQ
Sampling Freq	160 MHz	190 MHz	200 MHz	800 MHz	625 MHz
Peak Power	25.2 dBm	20.5 dBm	29.9 dBm	24.7 dBm	30 dBm
Peak System Efficiency	45%	20%	38%	43%	36.59%
Modulation Waveform	802.11g OFDM 64-QAM	LTE OFDM 64-QAM	802.11g OFDM 64-QAM	802.11g OFDM 64-QAM	Single-carrier 64-QAM
Noise Floor at Target Frequency	-113.5 dBc/Hz	-123 dBc/Hz	-134 dBc/Hz	-133 dBc/Hz	-104 dBm/Hz

Table 5.1: Performance Summary and Comparison

6

CONCLUSION AND FUTURE WORK

6.1. CONCLUSION

In this thesis, we have explored the design and implementation of a Digital Transmitter (DTX) utilizing a Switched-Capacitor Power Amplifier (SCPA) combined with a Finite Impulse Response (FIR) filter to suppress out-of-band quantization noise and achieve high linearity and efficiency.

In Chapter 3, we focused on the design of the SCPA architecture, optimizing the size of the transistors and series capacitors to maximize power and efficiency. A power combining technique was implemented to further enhance the overall output power, ensuring that the SCPA operates efficiently at the target power levels.

In Chapter 4, we introduced the complete DTX structure, including a novel mixed-domain FIR filter, which effectively suppresses quantization noise and out-of-band spectral replicas. This combination of SCPA and FIR filter technologies meets the target specifications for out-of-band noise levels and ensures the transmitter operates efficiently across the desired frequency range. The FIR filter plays a crucial role in maintaining spectral purity, which is essential for compliance with modern wireless communication standards.

Finally, through rigorous simulations and analysis, we demonstrated that the proposed DTX architecture can achieve a peak RF output power exceeding 30 dBm. The design also suppresses noise in frequency-division duplexing (FDD) and time-division duplexing (TDD) scenarios.

6.2. FUTURE WORK

In this work, the layout design of the digital transmitter has not yet started; therefore, the next step will be to develop the layout for this transmitter, laying the groundwork for the subsequent phases of research. After the layout is completed, post-layout simulations will validate the design's functionality and performance under real-world conditions, incorporating parasitic effects and other layout-related considerations. Once the post-layout simulations are finalized, further optimizations can be explored, including

integrating Digital Predistortion (DPD) techniques to improve linearity and reduce distortion, which is essential for achieving high-efficiency operation, especially in power amplifiers.

Then, a programmable delay generator could be designed and integrated into the circuit, allowing for precise control over the position of the notch in the frequency response. This adjustment would enhance the system's practicality by enabling the notch to be shifted to target specific interference or unwanted signal components, thus improving the overall flexibility and functionality of the design in real-world applications.

Additionally, digital filtering can be applied at the baseband level to suppress out-of-band noise further, ensuring compliance with stringent spectral emission masks. Incorporating an SRAM and the follow-up interpolation circuit will enhance data processing efficiency and improve signal handling and reconstruction in the RF domain. These advancements will improve the digital transmitter's overall performance, making it more suitable for high-data-rate wireless communication systems.

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