Analysing the properties and applications of wafer-scale mono-layer graphene

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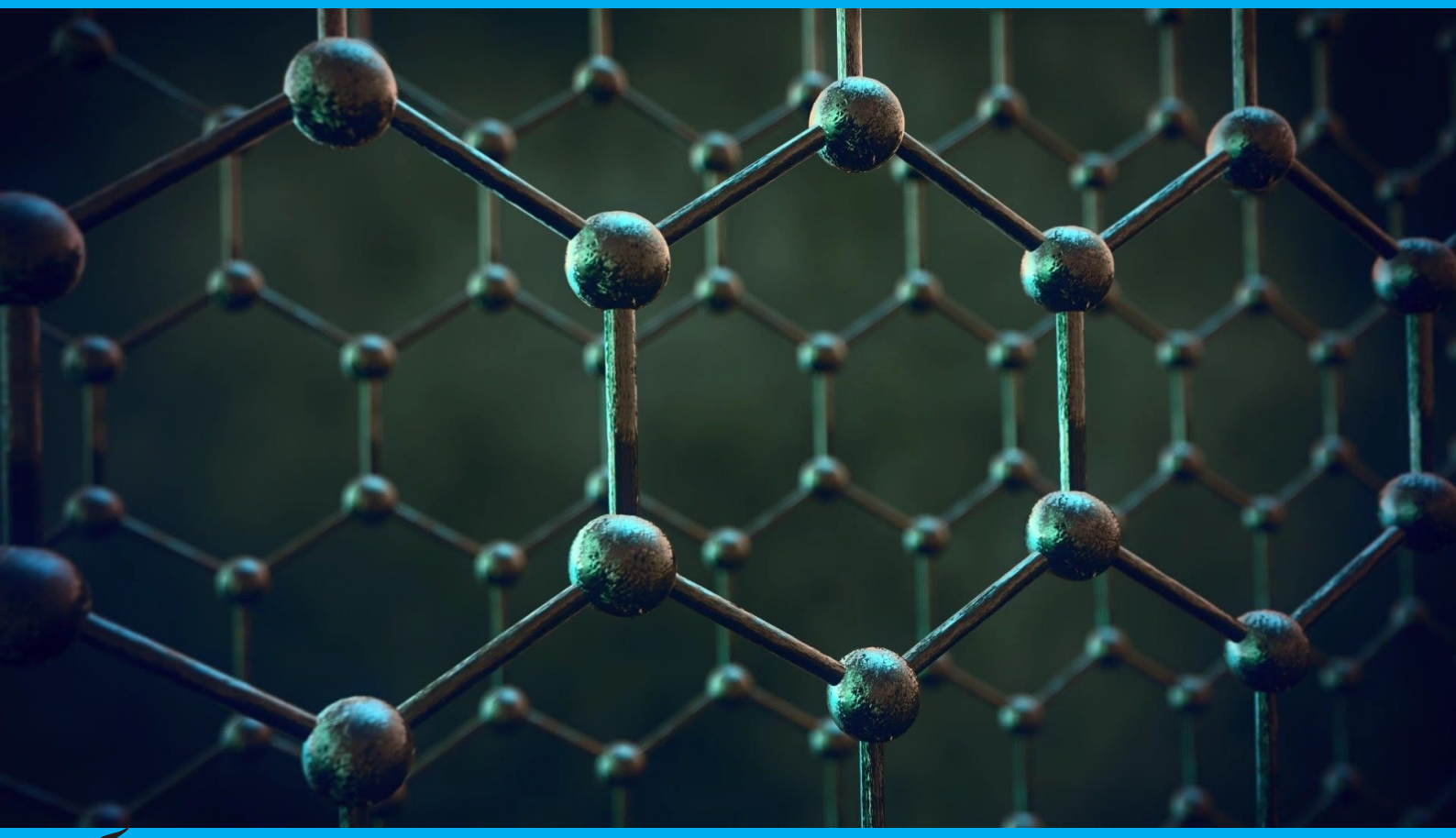

TU Delft

Analysing the properties and applications of wafer-scale mono-layer graphene

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Abstract

Graphene is two-dimensional allotrope of carbon with a honeycomb-like lattice structure. It shows exceptional properties in electrical, optical, thermal, mechanical and chemical fields. And due to its excellent properties, it is being researched to be used in many applications such as, sensors, graphene transistors, opto-electronics, etc. To realize these applications in an industrial scale, reliable methods to grow and transfer graphene need to be developed. Methods such as chemical and mechanical exfoliation, chemical vapour deposition (CVD), etc. are a few methods which are used to synthesize graphene. And wet transfer, electrochemical delamination, etc, are a few methods to transfer graphene on to the required substrate. Graphene is sensitive to chemicals and processing steps, hence the properties/behaviour of graphene varies based on the fabrication and transfer technique used.

Applied Nano-Layer(ANL) is a company based in Delft, that fabricates and transfers wafer-scale mono-layer graphene. As mentioned before, the properties/behaviour of graphene changes based on the fabrication and transfer technique used. Therefore, in this thesis, the properties/behaviour of monolayer graphene provided by ANL, is analyzed.

In this thesis, electrical properties like channel resistance, resistivity and mobility were analyzed. Also, the optical behaviour of graphene where pauli-blocking stops the absorption of light at dirac point, is analyzed. Few questions related to design of the process flow, working of the fabricated devices, propagation of light in the waveguides, modulation of light and effect of process flow on graphene, were answered to properly analyze the above stated properties/behaviour of graphene. First, a wafer-scale silicon waveguide was designed using COMSOL and BeamLab. The derived width of the waveguide was found to be for the values of 1 um to 4 um and the optimal cladding thickness was found to be 20 nm. Then, the designed waveguide structures were translated onto a mask that would be used in the fabrication of the electro-absorption modulators. Second, a cleanroom compatible process flow for the fabrication of Hall bars and electro-absorption optical modulators was designed and optimized. Several testing steps were performed to find the optimal parameters required in the process flow. Third, the hall bars and the optical modulators were fabricated in the clean room , Else-Kooi Lab(EKL), using the designed masks and process flows.

The electrical properties were analyzed by extensively measuring the hall bars. As an example, the average channel resistance, dirac voltage, average resistivity and average mobility of a graphene hall bar with dimensions 2 um x 2 um was measured/calculated to be 6.74 kΩ, 75.9 V, 1.7 kΩ and 1573.28 cm^2/Vs respectively. Similarly, the values for 11 other dimensional devices were measured/calculated. The optical behaviour was analyzed by testing the electro-absorption optical modulator. A few waveguides were tested for propagation of light and a power of 0.8 uW was measured for an input power of 0.6 mW, which suggests that light successfully propagates though the waveguides. Graphene modulation was tested using back gate biasing and an average dirac voltage of 73.33 V was observed for 2 um x 2 um hall bar device on the optical modulator die. These two when done simultaneously theoretically should modulate light. Lastly, the impact of process flow on graphene/ graphene devices was checked. And a drastric fall to 30% working devices(for optical modulators) from 60% working devices (for hall bars) with increase in process flow steps concludes that the number of processing steps does affect the graphene/ graphene devices.

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List of Abbreviations

ANL : Applied Nano Layers
SLG : Single Layer Graphene
MLG : Multi Layer Graphene
SSA : Specific Surface Area
CNT : Carbon Nano Tubes
CVD : Chemical Vapor Deposition
DMEU : 1,3-Dimethylacetamide
DMA : N,N-Dimethyl-acetamide
NMP : N-methylpyrolidone
GO : Graphite Oxide
GNR : Graphene Nano Ribbons
PMMA : Poly Methyl Metacrylate
IPA : Isopropyl Alchohol
PDMS : Polydimethylsiloxane
TRT : Thermal Released Tape
GHE : Graphene Hall Elements
FET : Field Effect Transistor
MSM : Metal Semiconductor Metal
TIR : Total Internal Reflection
XPS : x-ray photo-electron spectroscopy
SOI : Silicon on Insulator
PR : Photo Resist
PVA : Poly Vinyl Alcohol
RIE : Reactive Ion Etching
DRIE : Deep Reactive Ion Etching
vdp : Van der Pauw
EKL : Else Kooi Laboratary BHF : Buffered Oxide Etch Hydrogen Flouride
HBr : Hydrogen Bromide
Cl_2 : Chlorine
O_2 : Oxygen
Si : Silicon
SiO2 : Silicon dioxide
Au : Gold
Cr : Chromium
Cu : Copper
Ni : Nickel
Mo : Molybdenum
Ir : Iridium
FB : Flat Band

List of used prefixes

c - centi (10^-2)
m - milli (10^-3)
u - micro (10^-6)
n - nano (10^-9)
f - femto (10^-15)
k - kilo (10^3)
M - mega (10^6)
G - giga (10^6)

1

Introduction

Graphene is a two-dimensional (2D) layer of carbon atoms, packed tightly in a honeycomb lattice structure. By 2D, we mean that when you inspect a graphene film it is only one atom thick in one of the 3 scalar dimensions. It was thought that graphene was found in very little quantities in the past centuries through graphitic materials and only recently we have realized that you might actually create graphene when writing with pencils. In 2004, graphene was rediscovered, isolated and characterized by Andre Geim and Konstantin Novoselov, Novosolev et al. [1]. This 2D material exhibits unique electrical, mechanical and physical properties, such as very high mobility (5000cm^2/Vs)[2], very low resistivity[2], a absorption of 2.3%[3], etc. There are many scholary articles which discuss different uses of graphene. These range from researching on using graphene for seinsing different parameters. Examples for few graphene sensors are chemical sensors, electrochemical sensors, hall sensors (Magnetic field sensors), electric-field sensors, pressure sensors, mass sensors, strain sensors, photo-electric sensors, photo-detectors, etc[4]. Other uses include controlling the electrical properties of graphene for electro-optical modulation[5][6], graphene transistors[10][11] and using the optical bheavior of graphene to implement graphene opto-electronics[5] and photonics[5] and biosensing[5].

Optical Modulation or to be more specific, electro-absorption modulation using graphene is one of the applications that we will discussed in more depth (Chapter 4), in the later stages of the report. The structure of an electro-absorption modulator is shown in the figure 1.1. You have a rectangular silicon waveguide, with a few tens of nm thick oxide around it acting as a cladding. Then you have a graphene film on top of the oxide, which is biased to the dirac point, so that it stops absorbing the evanescent field that is observed at the cladding-air interface, due to the light propagating through the waveguide. Doing this to send 1's and 0's at particular intervals, the signal can be modulated. Since graphene has really high mobility (as high as 200,000 cm^2/V.s at room temperature), it can be used for higher modulation speeds when compared to traditional modulators [7].

However, for the above mentioned implementations, reliable methods to fabricate/deposit graphene would be needed. And as a good quality graphene film cannot be grown on the more common substrates such as Silicon, methods for reliable transfer of graphene on to required substrates to fabricate devices using graphene would also be needed. Which is why several methods for the production and transferring of graphene have been published and different companies/institutes use their own methods to deposit/fabricate and transfer graphene. The production methods include chemical and mechanical exfoliation, epitaxial growth on SiC and chemical vapour deposition (CVD). Whereas for the graphene transfer, methods like delamination using water-intercalation, electro-chemical delamination and transfer using polymer support substrates have been published. However, the method used for fabrication and transfer, affects the quality or the properties of the graphene films. For example, table 1.1 shows how the properties of graphene films are affected based on the transfer method used. In the table, different parameters are compared. We first see bands like G, 2D and D, which are peaks observed in the Raman spectrum that help in analysing the quality of the graphene films (Raman spectroscopy will be looked into more detail in the next chapter). Then we see intensity ratios, the sheet resistance and mobilities.

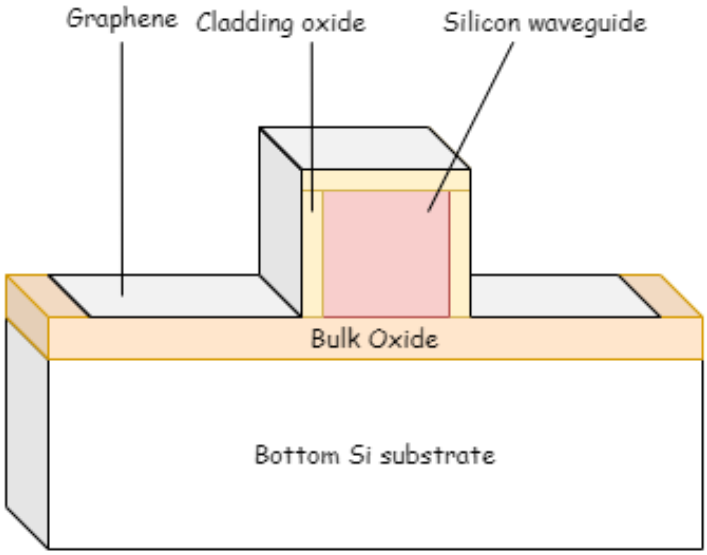


Figure 1.1: Structure of an electro absoption optical modulator using graphene.

Method	Growth substrate	Target substrate	[G cm^{-1}]	[2D cm^{-1}]	[D cm^{-1}]	I_{2D}/I_G	I_D/I_G	Sheet resistance	Field-effect mobility	No. layer
Wet transfer	Cu	SiO_2/Si	1560–1620	2660–2700	1300–1400	2.0			4050 $cm^2 v^{-1} s^{-1}$ (carrier-mobility)	95% one-layer
(polymer-assisted)	Cu	SiO_2/Si glass	1588	2690	1350	8.0–11.0	0.06–0.12	980 Ω sq^{-1}		one-layer
	Cu	SiO_2/Si PET	1583	2642	1320	3.1	0.06	255 Ω sq^{-1} (on glass)	5602 $cm^2 v^{-1} s^{-1}$ (hole-mobility)	one-layer
									4535 $cm^2 v^{-1} s^{-1}$ (electron mobility)	
Polymer-free	Cu	SiO_2/Si		2700				810 Ω sq^{-1}	6300 $cm^2 v^{-1} s^{-1}$ (on BN)	One-layer
Electrochemical	Pt	SiO_2/Si	1590	2685		2.0–3.0	<0.05		7100 $cm^2 v^{-1} s^{-1}$	Mostly one-layer
	Cu	PET	1582	2678				275 Ω sq^{-1}	350 $cm^2 v^{-1} s^{-1}$ (6 K)	>95% one-layer
Dry transfer	Cu	PDMS	1584	2681	1350	2.43	0.2			one-layer
	SiC	SiO_2/Si	1530	2700	1380		0.037 ± 0.008	175 Ω sq^{-1}	1348 $cm^2 v^{-1} s^{-1}$	one-layer
Face-to-face	Cu	SiO_2/Si	1560–1620	2690	1350				3800 $cm^2 v^{-1} s^{-1}$ (hole mobility)	one-layer
Transfer free	SiO_2/Si		1592	2685	1351	>2			667 $cm^2 v^{-1} s^{-1}$ (room temperature)	one-layer

Table 1.1: The properties of transferred graphene film by different method [35]

One such company called Applied Nanolayers (ANL) which produces and transfers high quality monolayer-graphene films for waferscale graphene devices fabrication, is interested in knowing the properties and the behaviour of the graphene films fabricated by them. This brings us to the Research Question for this Master Thesis which is framed as follows, "Analyzing the properties and application/behaviour of wafer-scale monolayer graphene". This master thesis is done in collaboration with ANL, where they provide the monolayer graphene for device fabrication and then few devices (such as Hall-bars and Electro-opitcal modulators) are fabricated and then used to measure/analyze the properties/behavior. The research question looks to be a little too broad, so to further elaborate it, we divide it into a few sub-questions as we are mostly just interested

in electrical properties and optical behaviour, but not all the properties. Sub-questions such as,

- Can a working process flow be designed for fabrication of graphene Hall bars and graphene Electro-absorption modulators?
- Is the voltage shift in the measurements, caused by the charge trapped in the oxide significant?
- Can a wafer-scale waveguide be designed and optimized for a light source of working wavelength 1320 nm?
- Can a measurable amount of light successfully propagate through a Silicon waveguide?
- Can light be modulated by using graphene electro-absorption modulators and hence, the aborption behaviour of graphene be tested?
- Does the process flow affect the properties of graphene and working of graphene devices?

were raised and some of these questions will be looked into and tried to be answered, for this master thesis. In this report, we first look into the background theory of graphene in chapter 2. The background theory consists of topics such as the different properties of graphene, different methods to fabricate/deposit graphene and transfer it and a few applications of graphene. Then we see how Raman Spectroscopy is used to check the quality of graphene or the defects in graphene and end the background theory with a few ways to contact graphene in devices.

In chapter 3, we move onto the simulations done in both BeamLab and COMSOL to find the optimum dimensions for the waveguide and the cladding for the electro-optical modulators. We also look into the simulations done for finding the optimal taper angle at the entrance of the waveguide, such that the angle is not too harsh for the light entering the waveguide.

We look into the process flows used for the fabrication of hall-devices which is used to analyze the electrical properties and for the electro-optical modulators in chapter 4. We also look into the difficulties faced during the fabrication of these devices.

In chapter 5, we look into the fabrication and measurement results of the devices that were fabricated. We also try to measure the amount of charge trapped within the oxide and if the charge trapped affects the transfer characteristics of the devices significantly.

Lastly, we end the report with the conclusion of the master thesis in chapter 6, followed by the appendix where we see the other simulation results and images of the fabricated devices that weren't shown in the main report.

2

Graphene

In this section, we provide the background literature for all the important information that is needed, when trying to understand Graphene.

Firstly, we dive into the properties of graphene, where we look into the excellent properties that graphene exhibits in every field of application. We start of with electrical properties, followed by optical, thermal and mechanical properties. And then finally end the subsection with chemical properties.

Secondly, we move onto the different graphene fabrication techniques. We start of with mechanical and chemical exfoliation. Then we look into the more common industrially used method in Chemical Vapor Deposition (CVD), followed by the more uncommon methods such as decomposition of carbides and splitting of nanotubes.

Thirdly, we explore the different graphene transfer techniques, where we see how graphene is transferred from its growth substrate to the target substrate. The target substrate is the substrate on which the graphene devices are fabricated. We mainly look into wet transfer, dry transfer and electro-chemical delamination.

Fourthly, we explore Raman spectroscopy, which is the measurement technique used to analyse the quality of graphene.

And finally, we look into a few graphene applications and a few ways to contact graphene/metallize graphene.

2.1. Properties of Graphene

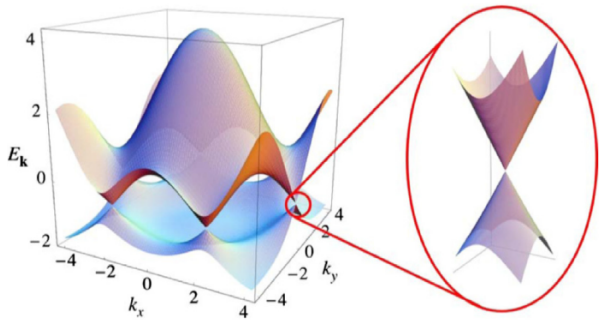


Figure 2.1: Band structure of graphene showing the dirac point.[2]

In 1946, the electronic structure of graphene was first described as the theoretical building block to describe graphite. Graphene possesses multiple outstanding properties in terms of mechanical strength, electrical conductivity, thermal conductivity and optical transperancy. These properties will briefly be looked

into below.

2.1.1. Electrical Properties

The conduction and valence bands of graphene are cones that touch at the dirac points, which is why graphene is considered as a zero-gap semiconductor. These Dirac points are in six locations in momentum space and are labelled as K and K' points of the Brillouin zone as shown in the figure 2.1. Two of the six dirac points are independent and the rest four are equivalent by symmetry (A total 3K and 3K' points). The energy varies linearly near the dirac points with the magnitude of momentum and hence follows a linear dispersion relation. This linearity is due to the massless nature of the Dirac Fermion. The dispersion equation can be seen in [14]. However, if the in-plane direction is no longer infinite, graphene's electronic structure would change and they are referred to as graphene nano-ribbons. The bandgap would be zero if it is "zig-zag" and would be non-zero if it is "armchair"[13]. This however is a zero-th order approximation and in reality is a bit more complex.

The behavior of graphene is found to be ambipolar, which means graphene can work with both electrons and holes. The energy band of graphene semiconductor is found to have a zero band gap. When no voltage is applied, the fermi level lies in the intersection of a cone-like energy band structure or the Dirac point, with the same carrier density for both the electrons and the holes. Hence why when graphene is used in FET's, different gate voltages show unique conductivity. It is also found that, the carrier density and the gate voltage are in a linear relationship. The type of carrier density in graphene can be continuously changed between electrons and holes by applied ambipolar gate voltages. For example, negetive Vg induces holes and a positive Vg induces electrons as shown in the figure 2.2(a) and the relation between the gate voltage and conductivity is shown in figure 2.2(b). Also, graphene can be doped using metal electrodes and typically graphene is p-type doped. More applications of the ambipolar behaviour of graphene can be seen in [10] and [11].

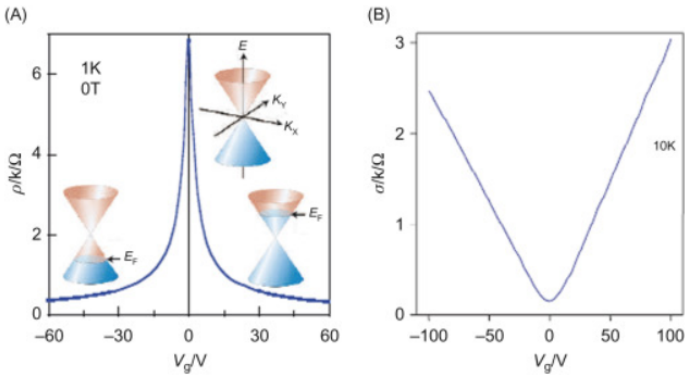


Figure 2.2: (a)Relationship between Vg and resistivity. (b) Relationship between voltage and conductivity.[10]

When it comes to the sensitivity towards other materials, graphene exhibits high sensitivity when in the proximity of other materials like high-k dielectrics, superconductors and ferromagnetics [13] because electron waves propagate within a single-atom layer, which can be both a good thing and a bad thing. It can be a good thing as the high sensitivity can be used as an advantage to make sensors/detectors. It can be a bad thing as graphene devices could be susceptible to interference easily.

Graphene also displays remarkable electron mobility at room temperature of about 15000 $cm^2.V^{-1}.s^{-1}$[15]. The mobility of both the holes and electrons are almost the same and the mobility is independent of temperature between 10K and 100K, while showing little change at room temperature. This implies that the dominant scattering mechanism is defect scattering.

Graphene exhibits a resistivity of 10^{-6} Ohm.cm[16] which is even lesser than the resistivity of silver, which shows the lowest known resistivity at room temperature. It's permittivity changes with frequency and over a range of microwave to millimeter wave frequencies, it is roughly 3.3.

All in all, graphene exhibits excellent electrical properties which allows the ability to explore its usage in many

electronic devices and applications.

2.1.2. Optical Properties

Graphene, albeit extremely thin, is still a visible material and can be seen without the use of a microscope. It absorbs around 2.3% of white light which is quite a high amount for a 2-dimensional material[3]. In addition, graphene is still very much transparent to the human eye which can have many uses like in transparent conductors, etc.

By superimposing monolayer-graphene on Si wave-guides, the interaction with light could be enhanced. Absorption increases from ~0.1 dB at normal incidence to thousands of dBcm^{-}1 when the light propagates along the wave-guide. By changing the fermi energy E_f of the mono-layer graphene, the absorption can be varied. When the fermi energy level is larger than the energy of the photons propagating, E$_p$*h*, the graphene is more transparent as a result of Pauli blocking and index of refraction changes[5].

2.1.3. Thermal Properties

The thermal conductivity of low dimensional carbon materials like carbon nanotubes and graphene, is excellent and could be as high as 3000-6000 W/mK[2]. This added to their excellent structural stability at high temperatures, they are widely proposed as thermal management materials.

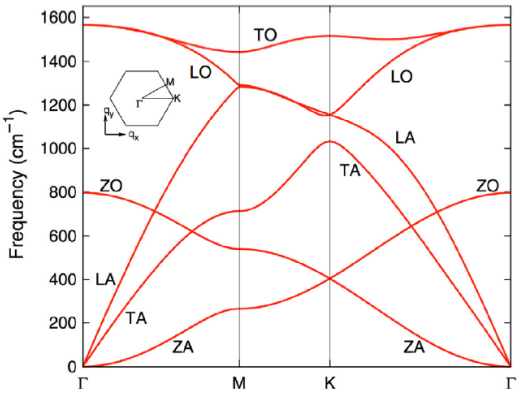


Figure 2.3: Phonon dispersion in graphene[2]

Early measurements of the thermal conductivity of suspended graphene is found to be upto 5300 W/mK[17]. Further research primarily on defected but more scalable CVD graphene have shown that, it is unlikely to reproduce such high thermal conductivity measurements, producing a wide range of thermal conductivities between 1500-2500 W/mK for suspended Single Layer Graphene. The large range of values for the thermal conductivity is due to the variations in the processing conditions of graphene and the quality of the graphene itself. Also, it is observed that if the Single Layer Graphene (SLG) is supported by an amorphous material, the thermal conductivity further decreases to 500-600 W/mK at room temperature, resulting in scattering of the graphene lattice waves by the substrate and can be even lower for few layer graphene encased in amorphous oxide.

Despite graphene being a 2D structure, it has 3 acoustic phonon modes. LA and TA which are the two in-plane modes that have linear dispersion relation and ZA which is the the out of plane mode that has a quadratic dispersion relation. Due to this, the thermal conductivity that is dependant on T^2 contribution, due to the linear modes is dominated by the T$^{1.5}$ contribution, due to the out of plane mode at low temperatures. Moreover, the thermal conductivity of graphene increases with its size, with the resolved conductivities of LA, TA and ZA converged to 315, 520 and 2600 W/mK respectively[18]. The relation between thermal conductivity vs the size and the temperature is shown in figure 2.4.

In-plane thermal conductivity of graphene is also gated due to weak coupling between the layers and as the number of layers in the graphene increase, the thermal conductivity approaches the conductivity of graphite. The measured thermal conductivity as a function of number of layers is shown in figure 2.5.

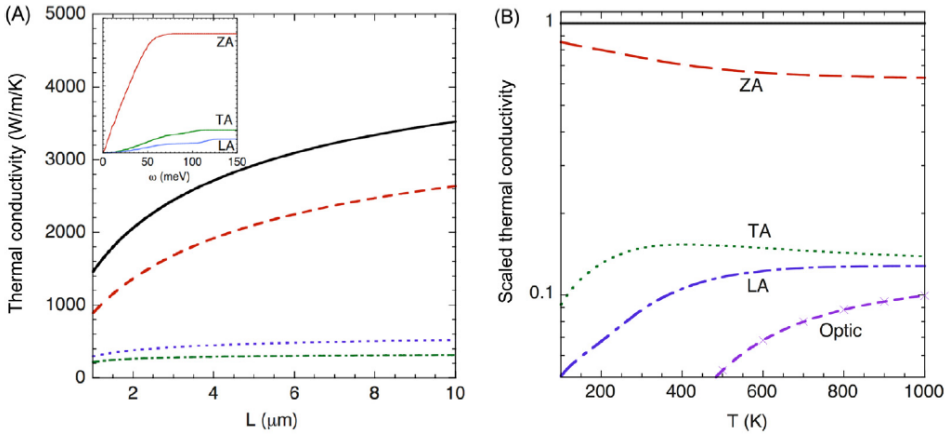


Figure 2.4: Effect of phonon modes on the thermal conductivities of graphene[2]

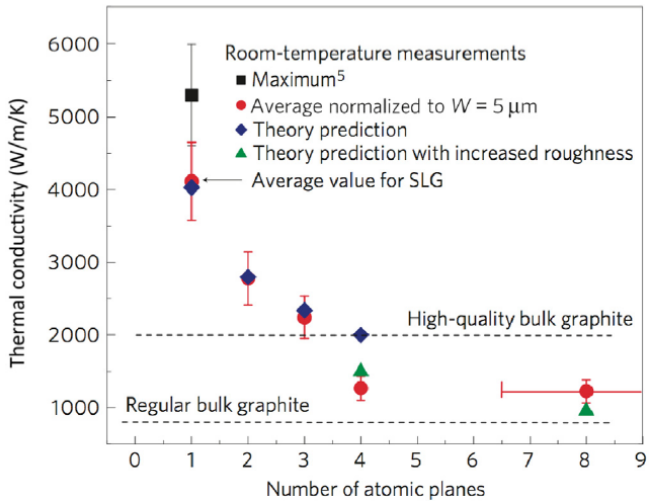


Figure 2.5: Graphene conductivity as a function of the number of layers[2]

2.1.4. Mechanical Properties

When it comes to the mechanical properties of graphene, the measurements for the mechanical properties have been performed by nano-indentation of suspended graphene layers in an Atomic Force Microscope (AFM). The Young's modulus has been measured to be 0.5 TPa and the second and third order elastic stiffness has been measured to be 350 nm^{-}1 and -690 nm^{-}1 respectively[19]. The stiffness at which the graphene breaks is measured to be 1 TPa and its intrinsic strength (ultimate tensile strength) is 130 GPa which makes it one of the strongest materials ever tested. The two-dimensional density of graphene is measured to be 0.763 mg/sq.m[13].

Graphene however, is also relatively brittle with a fracture toughness of about 4MPam compared to the fracture toughness of metals which like in the range of 15-50 MPam[20]. This indicates that imperfections in the produced graphene is likely to crack in brittle manner similar to ceramic materials. In poly-crystalline graphene, specifically the graphene produced from CVD, have defects in them, such as grain-boundaries and vacancies. These defects also affect the mechanical properties of graphene. How the mechanical properties change based on the defects are shown in Frank et al. [19].

2.1.5. Chemical Properties

The theoretical specific surface area (SSA) of graphene is 2630 m^2/g. This is a lot higher than any of the reported values for carbon black (900m^2/g) or Carbon Nano Tubes (CNTs) (100~1000m^2/g) and is similar to activated carbon[21]. Because of it's 2 dimensional structure, suspended graphene is the only form of carbon

or solid material in which every atom is available for chemical reaction on both the sides (top and bottom) for the atoms in the centre and the special chemical reactivity is shown by the atoms that are on the edge of the sheets. Graphene also has the highest edge to atoms ratio of any allotrope. Defects within the sheets is found to increase the chemical reactivity[22]. The temperature at which graphene burns is very low, i.e less than 350 $^{\circ}$C and the reaction between the basel plane of SLG and oxygen occurs at the onset temperature below 260 $^{\circ}$C[23]. Graphene is modified commonly with oxygen and nitrogen containing funtional groups and determination of these structures requires them to be well controlled.

It is reported that SLG is about hundred time more reactive than multilayer graphene sheets[24]. Graphene can also self-repair the holes in its sheets when exposed to carbon containing molecules like hydrocarbons. When graphene is bombarded with pure carbon atoms, the atoms completely fill the holes by perfectly aligning into hexagons.

2.2. Graphene Fabrication

As mentioned previously, there are multiple ways to fabricate graphene, like chemical and mechanical exfoliation, epitaxial growth on SiC and chemical vapour deposition (CVD). Each of these methods are discussed briefly below.

2.2.1. Mechanical Exfoliation

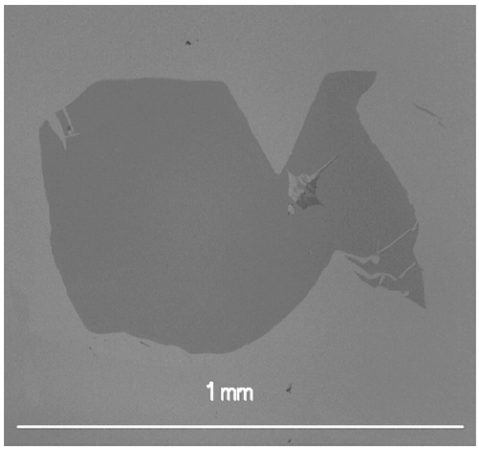


Figure 2.6: Mechanically exfoliated graphene flake on 300 nm SiO_2 [4]

Mechanical Exfoliation of Graphene is one of the first methods used for depositing mono-layer and few-layer graphene strips. Thin flakes are peeled from a bulk graphite sample using high tack tapes[25]. Continuously peeling the same graphite piece, reduces the thickness of the flakes being peeled up to the dimensions suitable for usage on micro-scale SiO2 substrates. Initially, the samples would be of tens of microns of thickness, but further peeling would result in flakes of mono-layer graphene. One such flake of a mono-layer graphene on a 300 nm SiO2 substrate, exfoliated using this method is shown in figure 2.6. To inspect the number of layers in the graphene flakes, Raman Spectroscopy can be used and characteristics of mono-layer graphene can be observed in figure 2.7, when compared to multi-layered graphene. The number of layers in the graphene flakes can also be inspected by observing the quantized light absorption of each graphene layer. However, Mechanical Exfoliation isn't suitable for large-scale fabrication, due to the process not being as controllable as other processes.

2.2.2. Chemical Exfoliation

Figure 2.8 shows a graphene film which is produced by chemical exfoliation. Exfoliation of graphite can be done using organic solvents like 1,3-Dimethylacetamide (DMEU), N,N-Dimethyl-acetamide (DMA), N-methylpyrolidone (NMP),etc. J.Doe et al [26] suggests NMP can be used for high quality monolayer graphene production. Ultrasonication in NMP allows the organic solvent to intercalate the graphite layers and produce mono-layer and few-layer graphene flakes. The yeild for monolayer is about 1 to 12 percent by weight. During the exfoliation process, the energy required to exfoliate graphite is given by the graphene-solvent interface

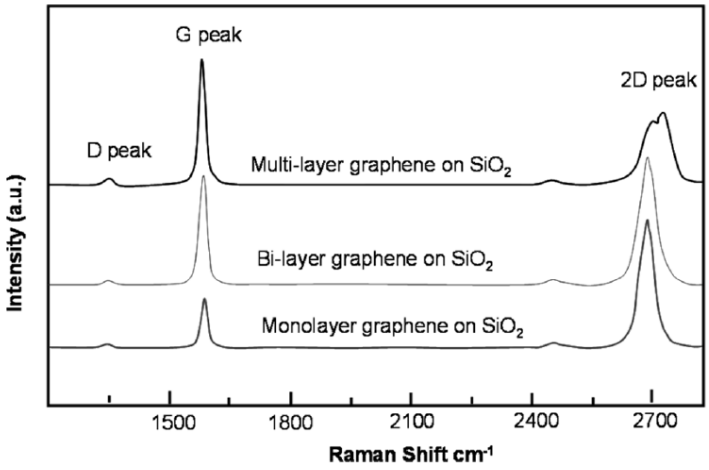


Figure 2.7: Raman Spectra for single, bi and few-layer graphene films on SiO_2 [4]

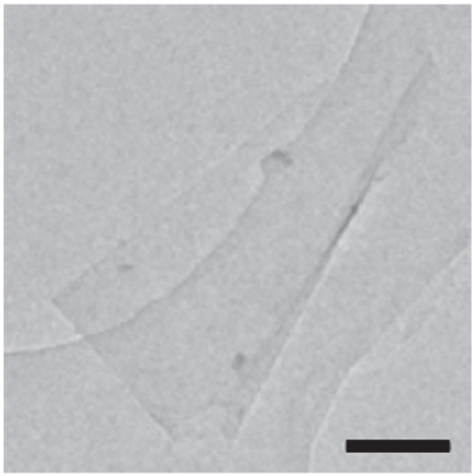


Figure 2.8: Image of a mono-layer graphene film exfoliated chemically from graphite[26]

where both the graphene and the solvent have similar surface energies. Use of interhalogen intercalents followed by dissolution in aqueous solutions to cultivate bilayer and trilayer graphene has been demonstrated in [27]. The hydrophylic nature of graphite oxide (GO) can also be used to exfoliate graphene layers using ultrasonication in aqueous solutions[28]. Many efforts for the chemical exfoliation of graphene have been made, but further measures have to be taken to improve the control over the number of layers and to reduce the number of defects within the flakes produced.

2.2.3. Chemical Vapor Deposition (CVD)

Chemical Vapor Deposition or CVD is the method in which volatile precursors either react with a substrate or decompose onto substrate surface, to deposit the required material on the said substrate. CVD is generally advantageous compared to other methods because it is inexpensive and produces large area graphene. When it comes to CVD of graphene, hydrocarbon precursors decompose to carbon radicals on the surfaces of metal substrates and form mono-layer and/or few-layer graphene. The use of metallic substrates have their own advantages such as, the metallic substrate acting as a catalyst to the reaction by reducing the energy barrier of the reaction and determining the deposition mechanism, which alters the quality of graphene deposited. The metal substrate used for deposition can be Copper (Cu), Nickel (Ni), Molybdenum (Mo), Palladium (Pd), Iridium (Ir), etc. In this subsection, we briefly look into CVD of graphene on Ni and Cu substrates.

When it comes to graphene CVD on Ni, it is a carbon segregation and precipitation process which means that the carbon atoms deposit and precipitate on the substrate to form the graphene. Different rates of segregation are observed when using different cooling rates. And these differences in segregation rates affect the quality

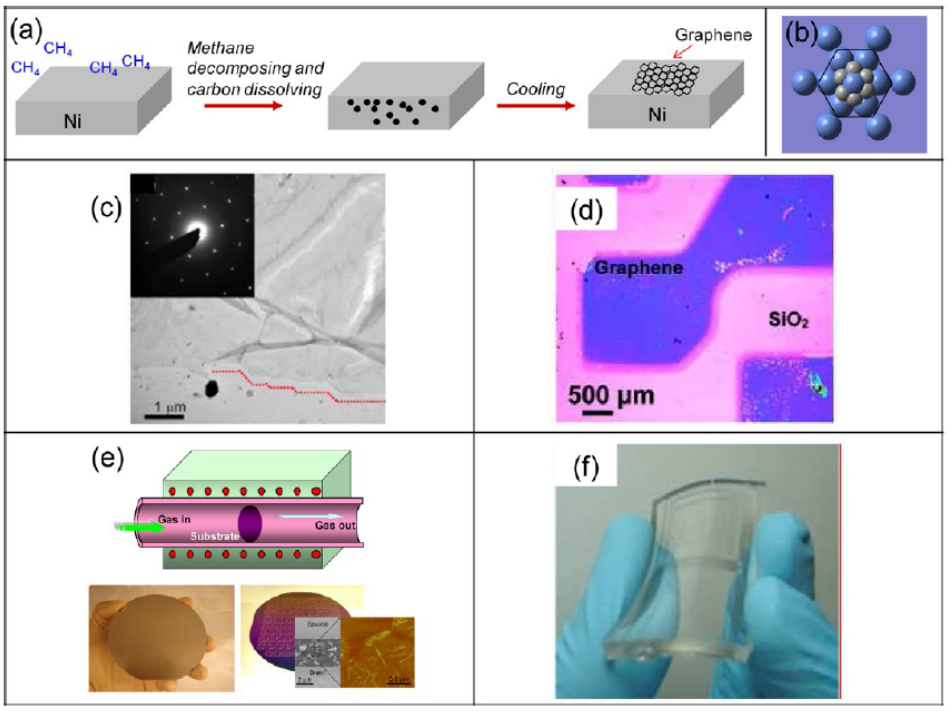


Figure 2.9: (a) Schematic of graphene formation on Ni. (b) Schematic of graphene atoms on Ni smaller atoms. (c) Image of graphene edges. (d) Graphene transferred onto SiO_2 substrate. (e) Full waferscale deposition of graphene. (f) Flexible and Transparent graphene on PDMS substrate.[29]

and thickness of the graphene layers deposited. [29] shows medium cooling rates deposit fewest graphene layers due to optimal carbon segregation. The poly-crystalline structure of the Ni substrate also affects the number of layers deposited. Defects like grain-boundaries in the structure results in multi-layer deposition of graphene at these said grain-boundaries due to the surface being uneven (as seen in figure 2.10), which is why annealing the Ni substrate before the CVD may improve the quality of graphene deposited. The hydro-carbon concentration may also affect the thickness of the graphene deposited. The Ni substrate can also be used to grow graphene structures with certain shapes. Such a structure with step-shaped edges is shown in figure 2.9(c) Such structures are patterned on Ni substrate by controlling the growth of graphene at different positions and the geometry of the grown substrates can be retained when transferred to insulator substrates. The orientation of the crystalline structure of Ni also affects the monotonicity of the graphene deposited with the (111) configuration showing better results than the poly-crystalline Ni surface in which the dark patches are the areas with multi-layer graphene due to the dark grains as seen in figure 2.10.

Another one of the substrates for depositing graphene is the Cu substrate. It is particularly used to deposit high quality single-layer graphene on Cu films. The quality of deposited graphene changes when compared to Ni-substrate due to the differences in the carbon solubility and the catalytic effect. Usage of a Cu-substrate has also shown advantages like having good control on the growth, low cost and the ability or ease of transfer after the deposition[29]. Figure 2.11 shows the graphene grown on Cu substrate and some wrinkles in the graphene sheet can be observed. These wrinkles are formed due to the difference in the coefficient of thermal expansion of Cu and graphene. The wrinkles can go across the Cu grain boundaries which indicates that the graphene is continuous. The graphene grown on Cu substrate can be then transferred to other substrates like SiO2, Si and glass as seen the figure 2.11(c),(d) and the analysis shows that >95 percent of the layer consists of mono-layer graphene. When compared to growth on Ni-substrate, parameters such as cooling rates and substrate-film thickness have little to no influence on the graphene CVD on Cu. The comparison is shown in figure 2.12 and it can be seen that the graphene grown on Ni has significantly more multi-layers than the graphene grown on Cu where the graphene grown on the Cu-substrate is a uniform mono-layer compared to the multiple multi-layer flakes on the graphene grown on the Ni-films. The difference in uniformity is due to the process involved in the growth. Ni-substrate uses segregation, whereas Cu-substrate uses decomposition. The nature of the segregation process leads to difficulty in controlling the formation of multi-layers. Whereas, once a mono-layer is formed on the Cu-substrate, the already formed graphene layer covers the Cu surface

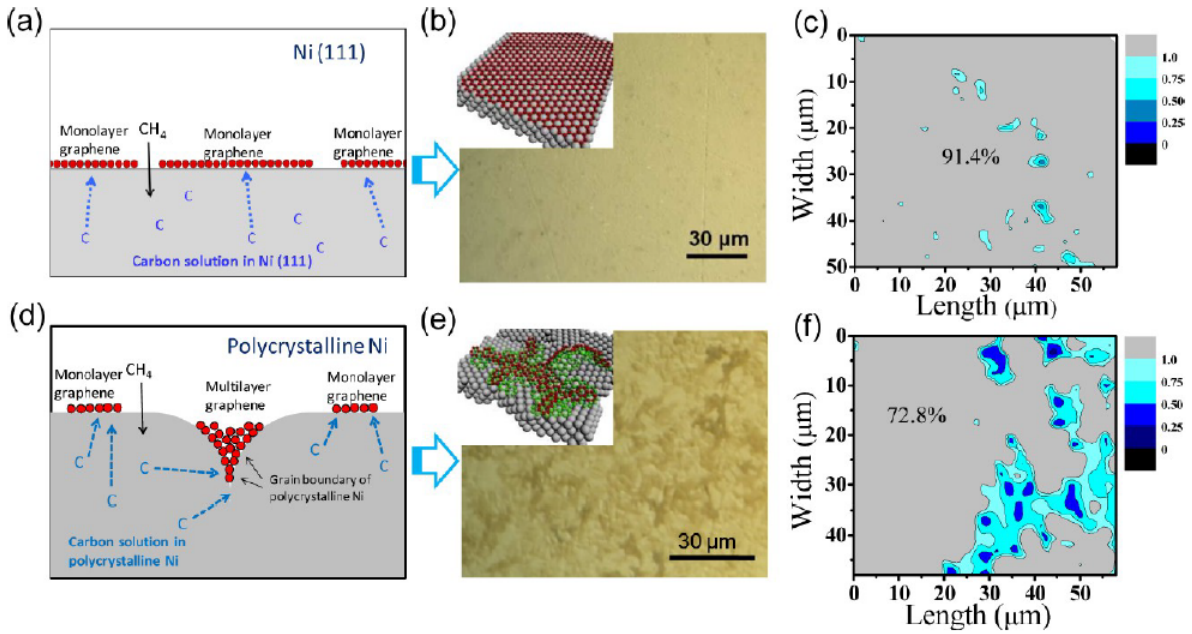


Figure 2.10: Schematic of Graphene growth on (a)Ni(100) and (d)Polycrystalline Ni. Optical Imaging of Graphene growth on (b)Ni(100) and (e)Polycrystalline Ni. Mapping of Raman spectra of Graphene growth on (c)Ni(100) and (f)Polycrystalline Ni[29]

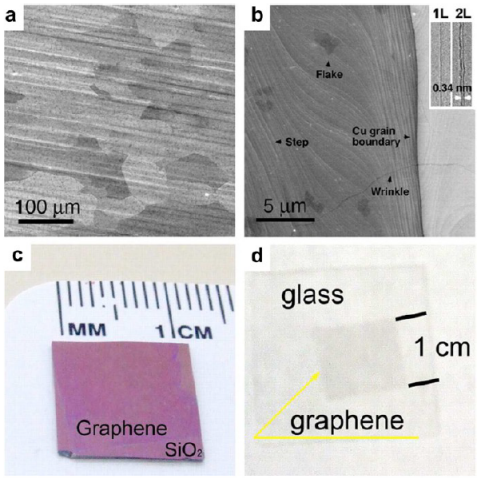


Figure 2.11: (a) SEM image of Graphene on Cu foil with growth time of 30 minutes. (b)High-Resolution image of Graphene, which is later transferred onto (c)Si/SiO_2 substrate and (d) Glass. (c)[29]

and the hydro carbon is deprived from the Cu catalyst which halts the decomposition and growth. Thus, graphene production on Cu can be seen as a self-limiting and robust process And it can be concluded that graphene CVD on Cu is preferred over Ni if highest quality mono-layer graphene is required.

2.2.4. Decomposition of Carbides/Epitaxial growth on carbides

Decomposition of carbides is a particular route in which the graphene is grown on the substrate itself. Carbide substrates such as SiC, undergo thermal decomposition at the surface layer level, to produce ultra-thin graphene layers. Firstly, 6H-SiC is cleaned at high temperatures under a Si flux to prevent the sublimation of Si during the cleaning step. Then the substrate is annealed at high temperatures in Ultra High Vacuum (UHV), where the surface of the SiC undergoes various reconstructions, until the graphitization temperature (1350 $^{\circ}$C for Si face, 1150 $^{\circ}$C for C face) when the surface graphene layers form. The first C layer passivates the surface and the subsequent C layers are decoupled from the substrate and exhibit the properties of graphene. figure 2.13 is the image of epitaxial graphene on 6H-SiC (0001) which has an average thickness of 1.2 mono-layers.

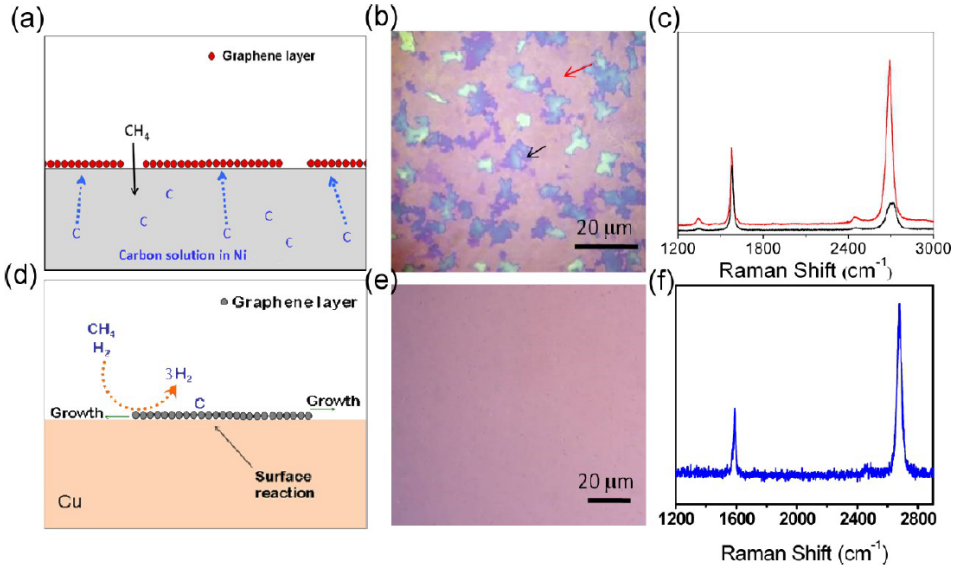


Figure 2.12: Schematic showing graphene deposition on (a)Ni and (d)Cu. Optical images of graphene grown on (b)Ni and (e)Cu transferred onto Si/SiO_2 substrate. Raman spectra of graphene grown in (c)Ni and (f)Cu. [29]

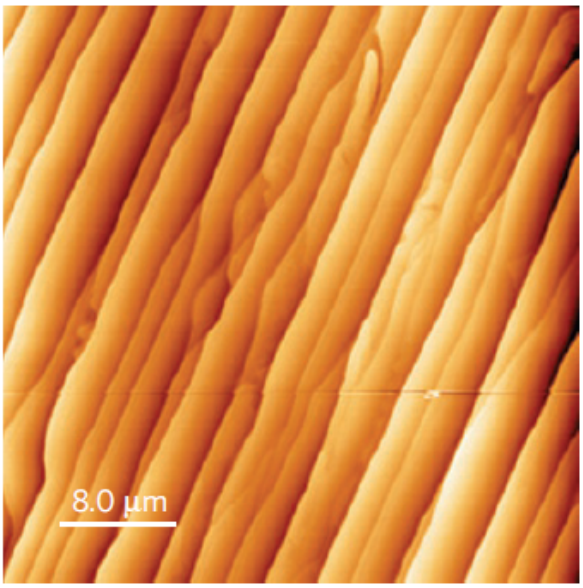


Figure 2.13: Image of graining on epitaxial graphene on 6H-SiC(0001)[30]

2.2.5. Splitting CNTs

CNTs or Carbon Nano-tubes have been described as rolled up sheets of graphene and [31][32] shows how graphene nono-ribbons [GNRs] have been made by unraveling CNTs. In Kosynkin et al. [31], GNRs are obtained by suspending CNTs in concentrated H_2SO_4 followed by treating the CNTs with $KMnO_4$. Where as in Jiao et al.[32], GNRs have been converted from CNTs by controlled plasma-etching of CNTs that are partially embedded in polymer film.

2.3. Transfer of graphene layers on to substrates

Majority of the methods used to produce graphene is done with chemicals or substrates such as metal-catalysts, tack-tapes, organic solvents, etc and in order to use this graphene for it's required applications, it would need to be transferred onto suitable substrates based on the requirements. For example, graphene needs to be transferred onto Si or SOI substrates for electrical applications like sensors, graphene FET's, etc.

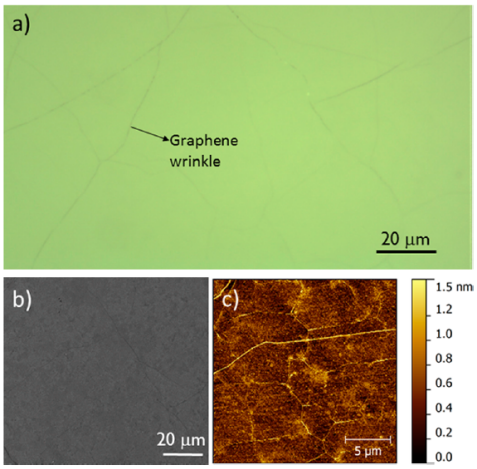


Figure 2.14: (a)Optical image, (b)SEM image and (c)AFM image showing wrinkles in graphene transferred onto another substrate.[33]

The transfer of graphene films has its own set of problems such as, not having a uniform 2D mono-layer film as seen in figure 2.14 , where wrinkles are observed on the deposited graphene on Cu-metal substrate which might cause problems in case of a bad transfer on to the substrate. Or the strength of the bonds between the growth substrate and graphene layer is too high, which might complicate the de-lamination of graphene films from the substrate. And this is the reason why transferring graphene is an important process for large-scale graphene device production and a reliable graphene transfer method has to be developed. Below we will look into a few transfer methods that have been published.

2.3.1. Wet transfer

Wet transfer is the process, where graphene layers are protected using solvents and then the growth substrate is wet-etched away leaving the sole-graphene films which can be transferred onto any required substrate. Polymers can be used as supporting layers to aid the transfer process and one such process for Cu/Ni- CVD graphene transfer using a polymer as a supportive layer is shown in figure 2.15.

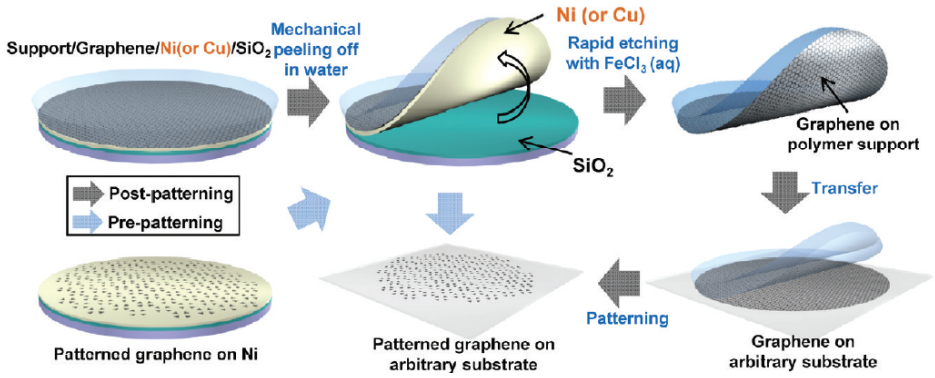


Figure 2.15: Schematic illustration showing the transfer of graphene films using a polymer support layer, grown on Cu/Ni substrates.[34]

Similarly, Wet transfer of CVD graphene on Cu-substrate is done by using polymer layers such as Poly Methyl Metacrylate (PMMA) as a supporting layer. PMMA has many prominent features, such as good wetting capability, low viscosity, good flexibility and dissolubility in organic solvents. The transparency of PMMA also allows to observe the process of Cu removal. The transfer method is as follows.

- Firstly, graphene films are grown on both the sides of the Cu foil.
- Graphene on one side of the Cu substrate is removed using O2 plasma, in order to etch the Cu substrate.
- PMMA is coated on the surface of graphene/copper and then cured.
- The underlying copper is etched away by the etchant, then washed by Deionized water (DI water).

- The PMMA is then removed using Acetone and the graphene film is washed by DI water and dried.

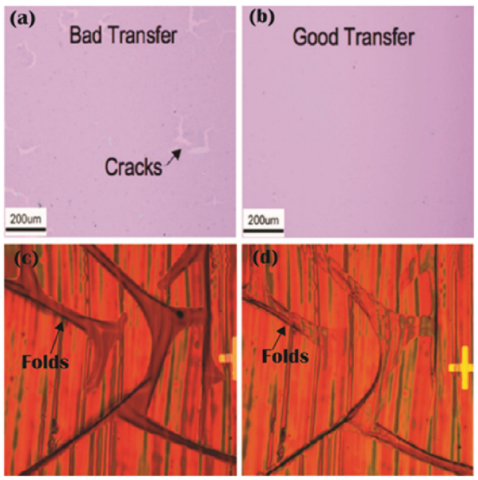


Figure 2.16: Optical images of graphene transferred onto Si/SiO_2 substrates using (a) traditional method, (b) using PMMA,(c) Before baking the stack and (d) after baking the stack at 150 °C[35]

As shown, in the figure 2.16 (a) cracks were formed on the transferred graphene, due to the graphene not being fully contacted to the metal substrate during the production. To limit the cracking, the graphene films were given a second PMMA coating and cured, after etching the Cu substrate and being transferred onto the SiO2/Silicon substrate. The results of this, can be seen in figure 2.16 (b). Some water may be trapped between the graphene and PMMA which would cause more abnormalities on the transferred graphene. Hence, baking the sample to evaporate the water before removing PMMA would improve the quality of the transferred graphene. figure 2.16 (c) and (d) show the samples before and after baking the samples/stacks at 150 °C.

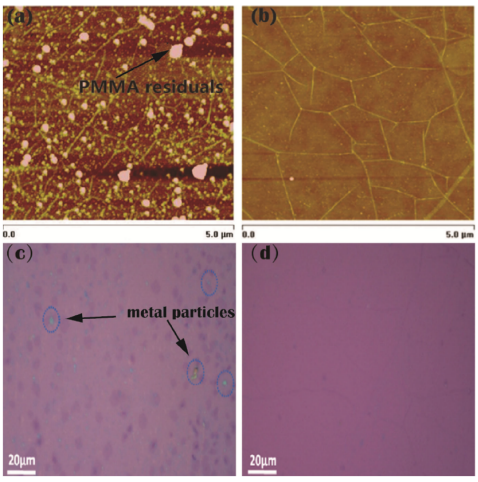


Figure 2.17: AFM images after removing PMMA using (a)Traditional methods, (b)Improved method using acetone and annealing, (c)before and (d)after the RCA cleaning methods.[35]

Improper treatment of PMMA may leave residues of PMMA on the graphene and use of an improved method in which the PMMA is first treated with acetone vapor, then immersed in acetone for 2 minutes and then goes through 3 hours of annealing. The differences in using the traditional method of removal using acetone and the improved method can be seen in figure 2.17 (a) and (b). There may also be cases where the metal-substrate is not fully etched away before the transfer. And for removing the residue metal particles a cleaning method called "RCA clean"[35] is used to remove metal contaminants/residues. The differences with and without the RCA cleaning are shown in figure 2.17 (c) and (d).

2.3.2. Polymer free wet transfer

In this subsection, we look into a method to wet transfer CVD graphene on Cu without using any polymer layer as a supporting layer. A graphite holder is used as a confinement area for the graphene film and after the Cu-substrate was etched, the etchant is p umped out and water/Isopropyl Alcohol (IPA) is injected in at the same rate. The surface tension of graphene is controlled this way. After the etchant is completely replaced by the mixed solvents, some of the solution is pulled out using a syringe such that the graphene is lowered onto the substrate. The whole process is shown in figure 2.18.

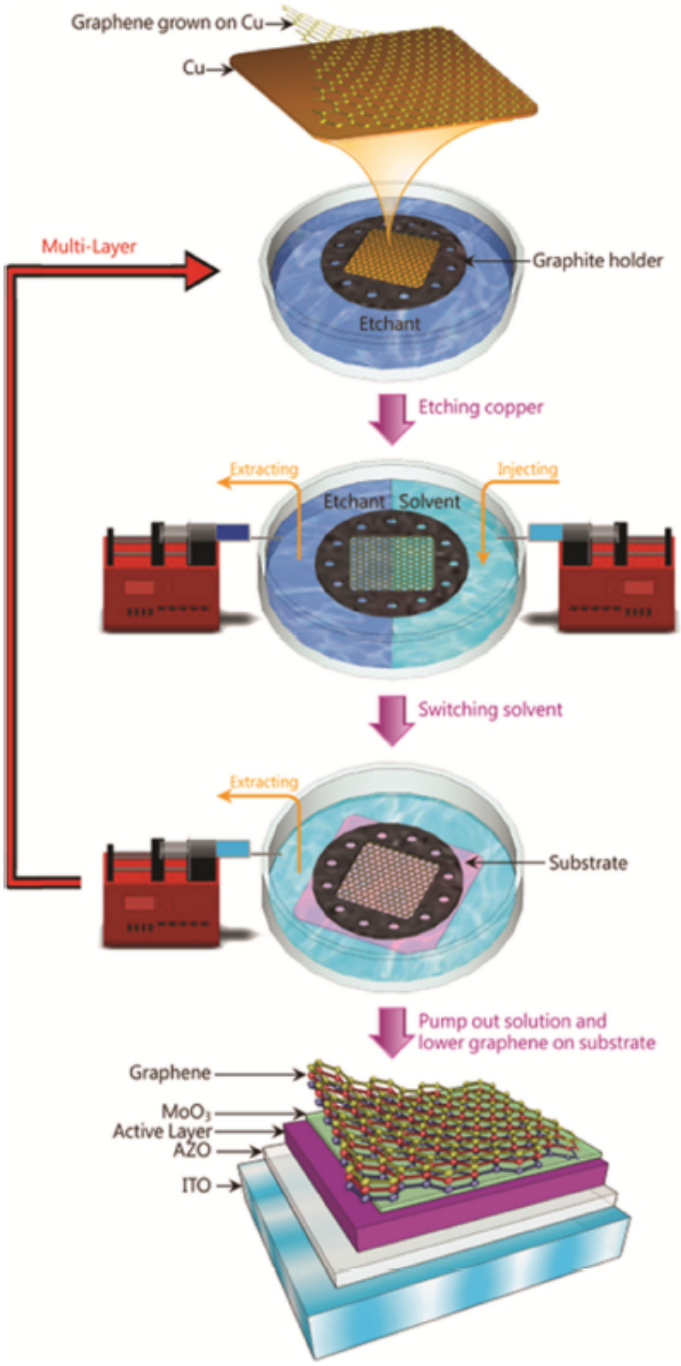


Figure 2.18: Schematic flow showing polymer free wet transfer of graphene onto a substrate.[35]

2.3.3. Electro-chemical Delamination

The traditional wet transfer methods which use etchants to etch metal growth substrates have their own disadvantages. The metal substrate used for growth cannot be used again as it is completely etched away, this increases the cost of the process in case of large scale production. The electrochemical delamination method allows for non-destructive transfer of graphene grown on both sides of the substrate if a foil is used and allows the reuse of the same substrate for future graphene production. The general steps for electrochemical delamination, as seen in figure 2.19, are as follows:

- Firstly, PMMA is coated as the protective layer for graphene.
- The PMMA/graphene/metal stack is set as the cathode electrode , glassy carbon is set as the anode electrode and both are inserted into an aqueous salt solution.
- A voltage is applied to the electrodes, and hydrogen bubbles start forming between the graphene/metal interface by electrolysis of water.
- Finally, the graphene is delaminated from the edges of the metal substrate and transferred onto a target substrate after removing the PMMA.

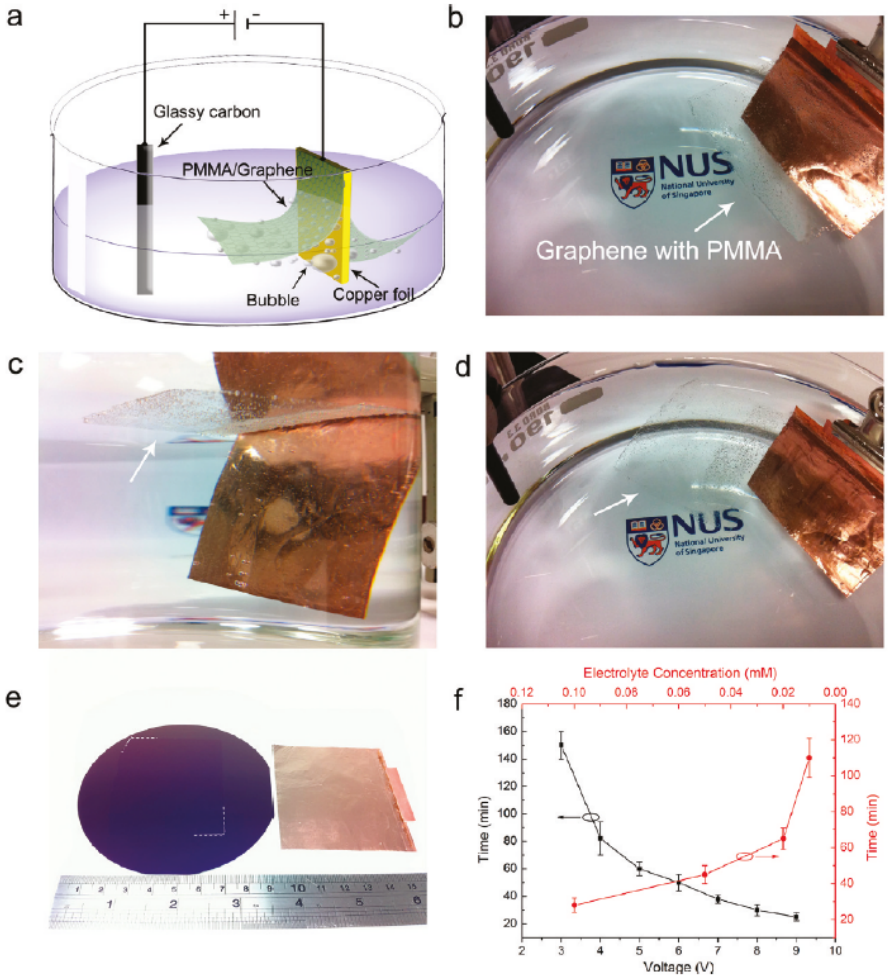


Figure 2.19: (a)Electrochemical delamination of Graphene films from Cu foil. (b)-(d)Images showing the whole film being delaminated in one piece. (e)The delaminated graphene transferred onto a 4-inch wafer. (f)Graph showing the time needed for complete delamination.[36]

In the above process, PMMA is used as a supporting layer which prevents the graphene layer from rolling or tearing into pieces. In case the delamintaion is done in the absence of the supporting layer, the delaminated graphene sheets are easily torn by the sheer forced exerted on them due to bubbling. The effect of not having

a supporting PMMA layer in graphene transfer is shown in figure 2.20. figure 2.20 (a) shows the graphene film being broken up into scrolled sheets. figure 2.20 (c) is the image of Cu foil showing the high density of crystal terraces and step edges and (d) is the Cu foil after one cycle of graphene growth. It can be seen that the surface becomes noticably smoother due to electrodeposition of Cu nanoparticles. The thickness of Cu is measured after the delamination and it is found that about 40 nm thickness of Cu film is etched for each cycle, which is why the same substrate can be used multiple times for deposition. The etching is limited only to less than 40 nm because of the Cu oxides that form on the foil during the electrolysis process, which end up passivating the surface which prevents more etching. figure 2.20 (e),(f) and (g) show the Raman comparison, Tafel plot and impedimetric curves of Cu and graphene with and without PMMA samples, which suggest that the graphene is more damaged if no PMMA is used when compared to that of the results when PMMA is used.

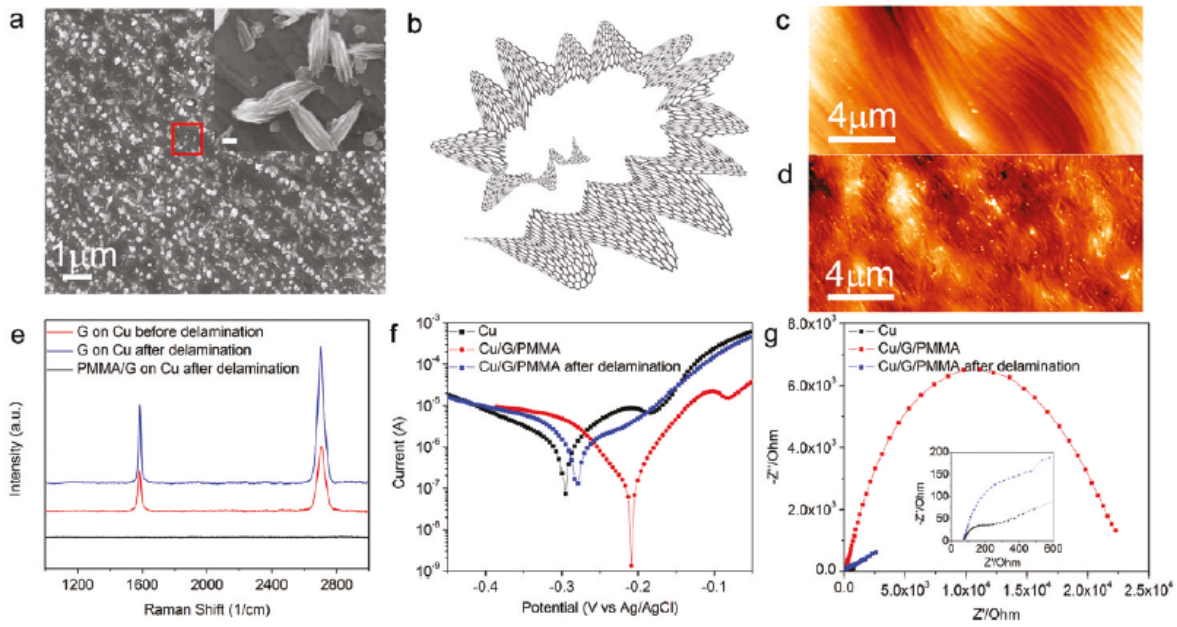


Figure 2.20: Role of PMMA.(a)SEM image showing graphene scrolls. (b)Schematic drawing of graphene scrolls seen in the inset. (c)AFM image of Cu/G surface, showing a high density of single crystal terraces and step edges. (d)AFM image of Cu growth substrate after one cycle of graphene growth. (e)Raman Spectra of the graphene. (f)Tafel plots and (e)Impedimetric curves for Cu with and without PMMA protection layer.[36]

Fig,2.21 (a) to (c) show the Cu foil after one , two and three delamination cycles respectively. We can see that graphene produced in the first cylce (G1) is characterized by a high-density of quasi-periodical nanoripples. The density of these nano-ripples get reduced for each cycle after the first deposition (G2 and G3). figure 2.21 (d) to (g) show the differences in electrical properties of the graphene deposited in each of the cycles one, two and three respectively. Similarly, other deformities like grain boundaries, terraces and step edges in the Cu foil smoothen out after each cycle of deposition and delamination. figure shows the surface reconstruction of the Cu substrate after three successive deposition and delamination cycles.
When noble metal substrates such as Ir, Pt and Au are used as the growth substrates for graphene, traditional wet transfer methods are not available for these substrates due to their inert nature. However, electochemical delamination can be used for such substrates. [37] uses this method to transfer graphene from a Pt substrate. The Pt/graphene/PMMA stack is used as the cathode electrode, similar to the process given above and the graphene layers were successfully delaminated and transferred.

2.3.4. Dry Transfer

As the name suggests, dry transfer of graphene onto the target substrate does not involve any solutions for the step after the graphene is released from the catalyst. Similar to the role of supporting layer played by PMMA in wet etching, Polydimethylsiloxane (PDMS) and TRT (thermal released tape) are used during the dry transfer process. Thermal treatment can be used to remove these supporting layers, after the transfer is done.

A "Roll to roll" method for synthesizing and transferring reported in [38] is discussed below.

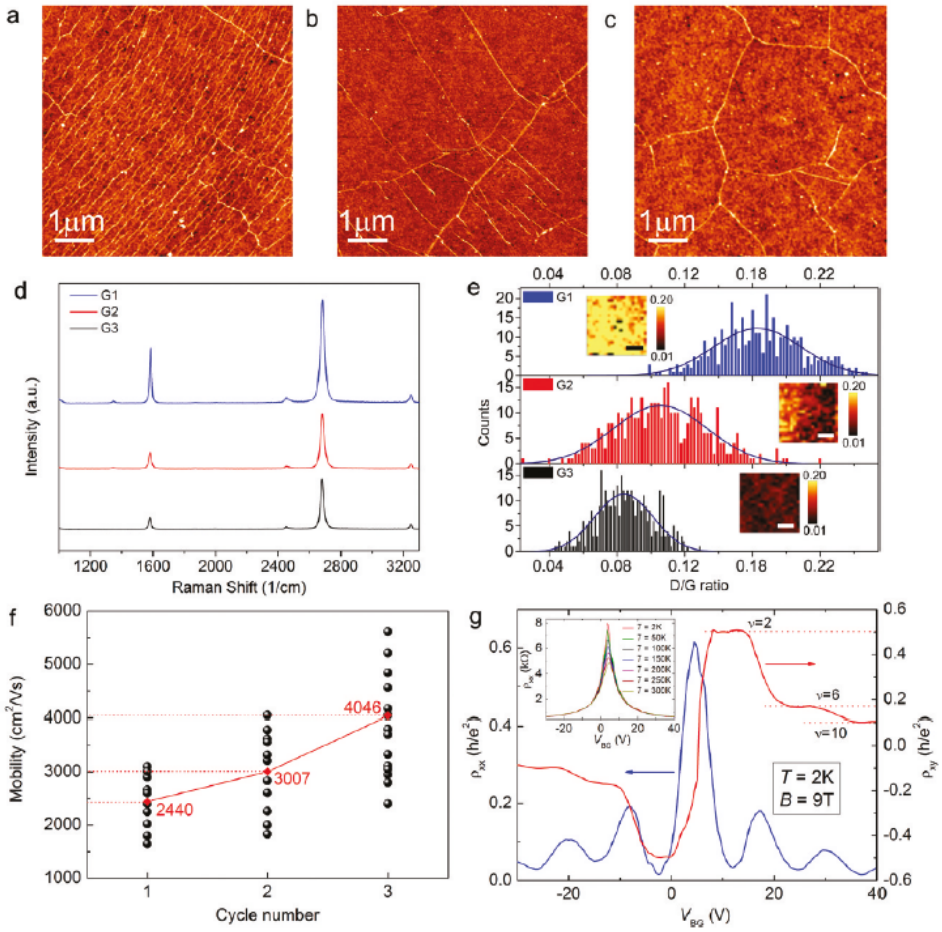


Figure 2.21: (a)-(c)AFM images of Cu foil after one, two and three cycles of graphene growth respectively (G1, G2 and G3). (d) Raman Spectra, (e)Statistical Histogram and (f)Carrier mobility of graphene layers grown in the first, second and third cycle respectively. (g)Quant um Hall effect measurement of G3 sample.[36]

- Firstly, two rollers are used to attach TRT to the graphene.
- Then the copper foil etched by using a copper etchant.
- Finally, the graphene is transferred onto the target substrate using two more rollers and the TRT was removed by mild heating.

The above process can be seen in figure 2.22 (a) and a similar process for Ni [39] for Ni substrate with EVA (ethylene-vinyl acetate) as the adhesion layer between graphene and target substrate is shown in (b). The "roll-to-roll" method is mainly suitable for flexible substrates as the substrate has to go through the rollers with the graphene films for good adhesion during the transfer process. However, mechanical defects can be easily formed in the graphene during the transfer process. It is found that, use of two hot pressing plates, as seen in figure 2.23 (a), decreases these mechanical defects. The process using hot press is as follows.

- After the removal of the Cu foil, the graphene with TRT as the support layer is inserted into two rollers to attach the target substrates.
- Then two hot metal plates were applied with controllable temeprature and pressure.
- The TRT loses its adhesion force after 10 seconds of hot pressing, then the graphene is transferred onto the target substrate.

This method can be used to trasfer graphene into both flexible and rigid substrates. figure 2.23 (b),(d) and (c),(e) show the defects in graphene before and after the use of hot press and it can be clearly seen that there

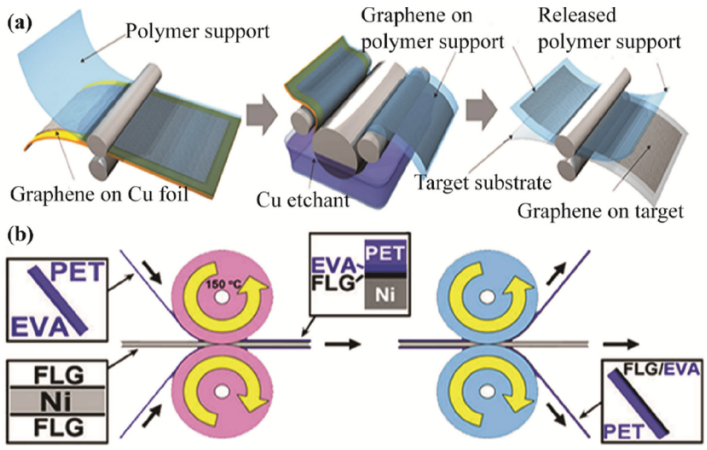


Figure 2.22: Two methods showing dry transfer of graphene films used in (a)[38] and (b)[39].[35]

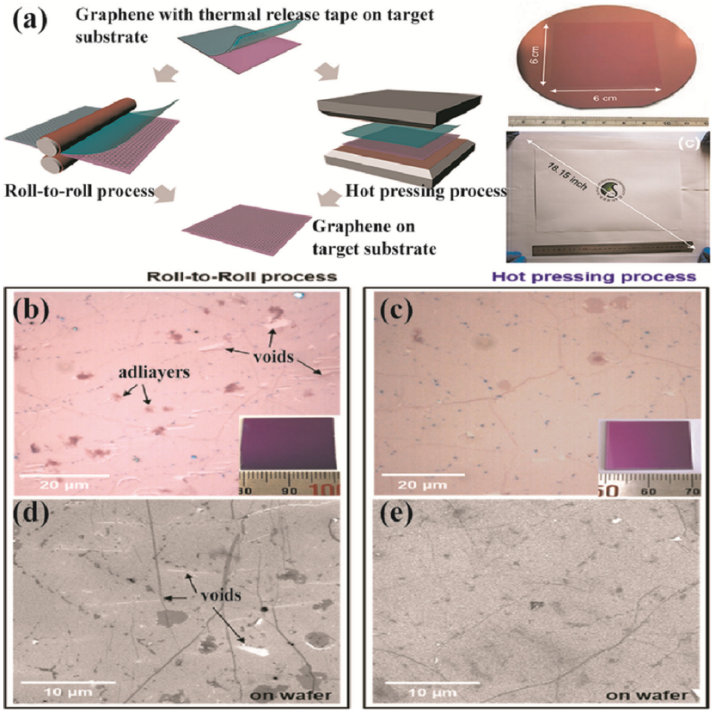


Figure 2.23: (a)Graphene dry transfer using hot-plates.(b),(c)Optical and (e),(f)SEM images of graphene showing differences when hot pressing is used.[35]

are lesser mechanical defects after the hot pressing process. Besides mainly using adhesives in the above processes, etchants have not been used (barring Copper) and dry transfer of high quality graphene films have been acheived.

2.4. Raman Spectroscopy

A key requirement in the research and applications in the carbon family is the ability to identify and characterize all the members of the said carbon family at both lab and mass-production scale. The characterization tool must be fast with high resolution and give maxim um electronic and structural information. Raman spectroscopy ticks all the boxes mentioned above and since graphene is one of the materials being researched in the carbon family, Raman spectroscopy can be used to characterize graphene.

Raman spectroscopy is a spectroscopic technique that is typically used to determine the vibrational modes of the molecules. It relies on the inelastic scattering of photons which is known as Raman scattering. Graphene consists of sp2 carbon hexagonal networks, in which strong covalent bonds are formed between two adjacent

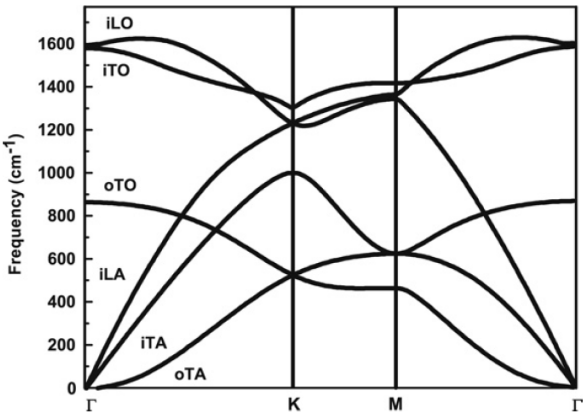


Figure 2.24: Phonon dispersion of graphene showing different branches[40]

atoms. Different peaks or bands can be seen in the spectroscopy results such as the D-band, G-band, D'-band and G'-band (also called 2D-band). D-band is observed due to the out of plane vibrations caused by the defects in the structure. The G-band is observed due to the in-plane vibrations of the sp2 bonded carbon atoms. The D' and G'-bands are the bands appearing in the spectra due to excitation. The G'-band frequency is approximately twice the frequency of the D-band spectrum, which is why some authors prefer to call it 2D-band. The unit cell of graphene consists two carbon atoms, A and B, and there are total six phonon dispersion bands with three of them being Acoustic branches (A) and the other three being Optic branches (O). The phonon dispersion bands can be seen in figure 2.24. "i" and "o" correspond to in-plane and out-of-plane phonon modes and "T" and "L" refer to tansverse and longitudinal vibrations, corresponding to the vibrations being perpendicular to or parallel to, respectively, the A-B carbon-carbon directions. Therefore, along the high symmetry Γ_K and Γ_M directions, the six phonon dispersion curves are assigned to LO, iTO, oTO, LA, iTA and oTA phonon modes. And Γ here is the zone center. The phonon modes in the vicinity of the K point are important as the D-band and G'-band are related to them. figure 2.25 shows the Raman spectrum of a graphene edge, the D, G and G'-bands taken with a laser excitation energy of 2.41 eV.

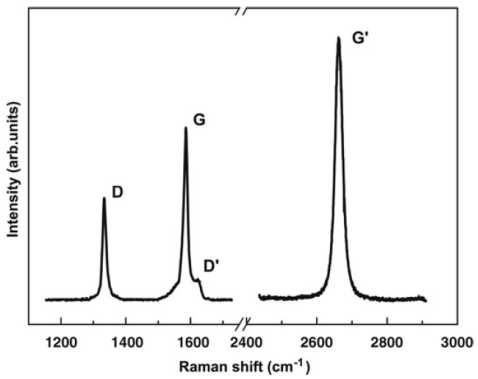


Figure 2.25: Raman spectrum of graphene edge showing different bands.[40]

The variations in the peaks on each of these bands for different reasons like defects in the film, number of layers, the influence of doping,etc and some of these will be looked into briefly in the subsections below.

2.4.1. G' band Raman spectra of single, bi and tri-layer graphene

Raman spectroscopy allows the measurement of the number of graphene layers on a Silicon dioxide substrate using the G' band peak of the Raman spectra. This peak is related to inter-valley double resonance Raman scattering. The shape, linewidth and peak position of the G' band changes when the number of layers changes. In [41], 7 laser excitation energies from 1.83 eV to 2.72 eV are used and the experimental spectra shown is normalized with the G band intensity for each laser energy.

The G' band of graphene that appears around 2650 cm^{-}1 is a two phonon double resonance Raman scattering process as seen in the figure 2.25. The G' band is an overtone of the D-band which consists of two inelastic scatterings, whereas the D band consists of one-elastic and one-inelastic scattering.

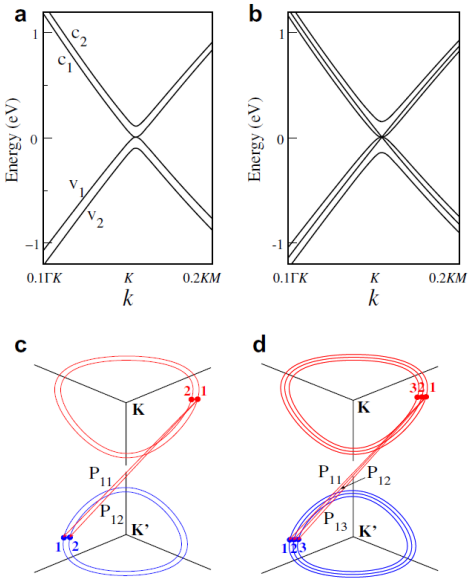


Figure 2.26: Electronic band structures for (a)double and (b)triple layer graphene. Equi-energy contours for (c)double and (d)triple layer graphene.[41]

For the bi and tri-layer graphene however, the two linear electronic bands around the fermi level for a single graphene layer, are split into two or three energy bands according to the inter-layer interaction between the layers. The band structure is shown in figure 2.26. The terms $P_1$1, $P_1$2, etc indicate the peak component for the G' band optical processes and the number subset "12" correspond to the process "1->2" and so on. Some of these processes may be degenerate and can share the same band line. The excitation energy, the theoretical and calculated energy dispersion of the G' band for 2L and 3L are shown in figure 2.27(a) and 2.28(a). The theoretical and calculated band line shapes for 1L and 2L graphene is shown in figure 2.27(b) and (c). The theoretical and experimental band line shapes for 3L graphene and the dependence of G' band intensity for the energy of laser of 2.41 eV, as a function of the number of layers is shown in figure 2.28(b) and (c).

As seen in the figure 2.27 the 2L graphene has two processes(21 and 12) that are degenerate with each other, which is why we see only 3 peaks in the band line shapes. Similarly in figure 2.28, 3L graphene has 4 processes that are degenerate (21+12, 22+13+31 and 23+32) which is why we only see 5 peaks in the band line shapes. The calculated peak intensity of the G' band decreases with increasing laser energy in figure 2.29 and 2.30, while irregular behaviour is observed in the experimental results for both 2L and 3L graphene. After assessing the figures, it can be said that the G'-band intensity should depend on the laser excitation energy.

2.4.2. Quantifying defects in Graphene

In graphene with zero-point like defects, the distance between the defects, L_D, is a measure of the amount of disorder. In [42] to fully accomplish the protocol for quantifying the point-like defects in graphene using Raman spectroscopy (or L_D), different excitation laser lines in ion-bombarded samples were used and the D to G peak intensity ratio was measured. It is found that for a given L_D, the I_D/I_G ratio increases, as the excitation laser energy increases as seen in figure 2.31. figure 2.32 shows the Raman spectra of five SLG samples exposed to different ion bombardment doses in the range of $10^1$1 to $10^1$5 Ar^+/cm^2 and it can be observed that higher the bombarding dose, the lower the D peak falls and D',G' peaks rise. The samples are first cultures using mechanical exfoliation and then bombarded with with the ions. figure 2.33 shows the relation between L_D and I_D/I_G which follows the relation given in [42].

A few other uses for Raman Spectrography in graphene applications can be seen in [43] and [44].

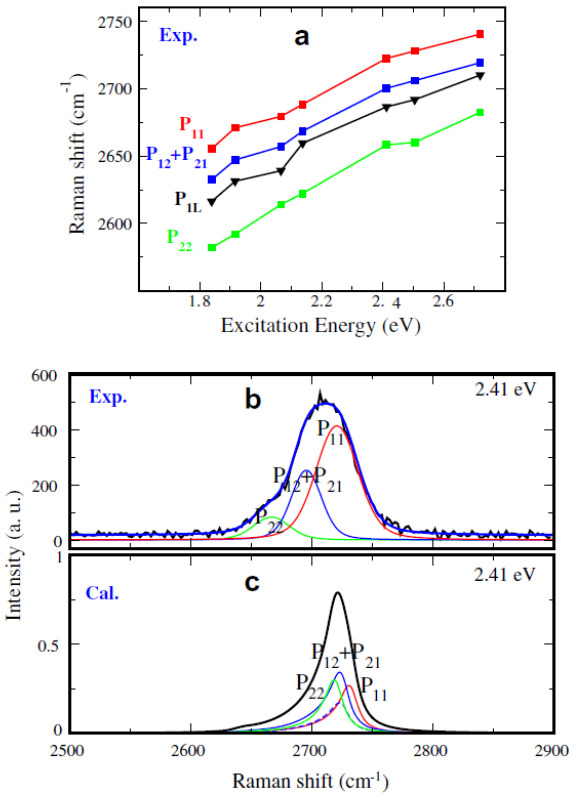


Figure 2.27: (a)Experimental energy dispersion of G'band as a function of excitation for 1L and 2L graphene. (b)Fittings of the 2L graphene G0 line shapes with three Lorentzian components at EL ¼ 2:41 eV. (c)Calculated peaks from each contribution to the 2L G' band intensity.[41]

2.5. Graphene Applications

After looking into some reliable ways to produce and transfer graphene and into some properties of graphene, now we will discuss a few applications of graphene. As mentioned previously, there are many publications regarding the applications of graphene, ranging from it being used in different kinds of sensors for sensor applications due to its good flexibility and electrical properties to different optical/photonic applications due to its controllable and variable reflectivity. A few of these applications will be discussed below briefly.

2.5.1. Sensor Applications

Multiple properties of graphene can be manipulated and controlled for it to be used in alot of sensor applications. It can be used in chemical sensors by exploiting its good surface to vol ume ratio, and due to this chemical detection can be done by making use of the change in conductivity of graphene when gas molecules adsorb on the graphene's surface and act as donors and acceptors of electrons [45]. The changes in resistivity for few gases is shown in figure 2.34.

It can be used in electro-chemical sensors in an electrolytic gated configuration as it was observed that an increasing pH shifted the dirac points of graphene FET in the positive direction as seen in figure 2.35.

The 2D geometry of mono-layer graphene, it naturally being thin and showing high mobility, it can be used to make graphene hall elements (GHE's) [figure 2.36][46]. The carrier density of graphene can also be easily modified by an electric field, making it suitable for use as an electric field sensor. Graphene also shows a hall resistance of ~1kOhm/T compared to 358 Ohm/T, which suggests that it can be used for magnetic field (Hall) sensor applications. Mass sensors can also be fabricated using graphene membranes and cantilevers by monitoring the vibrating graphene molecules, which absorb and desorb from its surface, which inturn changes the resonant frequency. The change in electrical conductivity based on the amount of strain suggests that graphene can also be used for strain sensor applications[4].

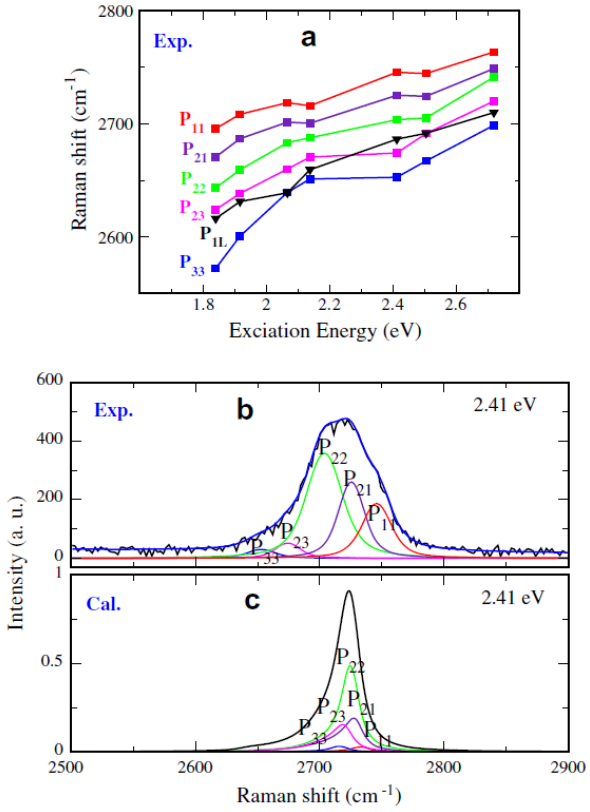


Figure 2.28: (a)Experimental energy dispersion of G'band as a function of excitation for 1L and 3L graphene. (b)Fittings of the 3L graphene G' line shapes with three Lorentzian components at EL ¼ 2:41 eV. (c)Calculated peaks from each contribution to the 3L G' band intensity.[41]

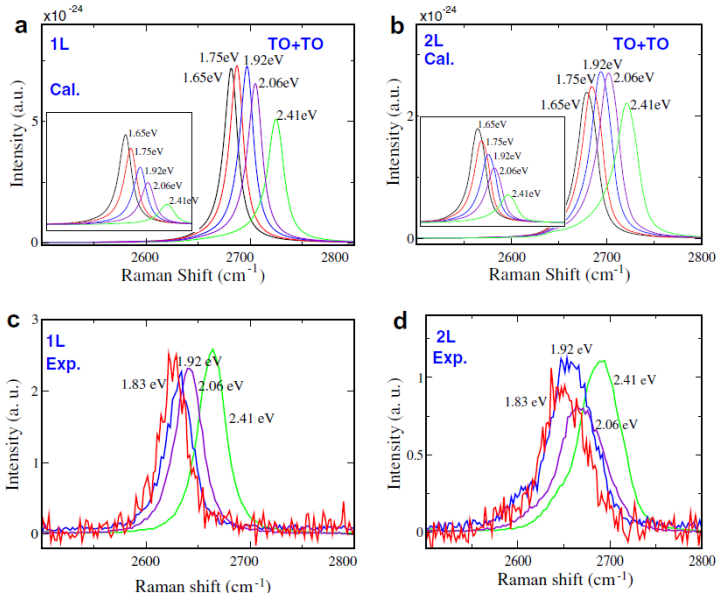


Figure 2.29: Theoritical and Experimental band line shapes for 1L(a),(c) and 2L(b),(d) graphene[41]

Figure 2.30: Theoritical(a) and Experimental(b) band line shapes for 3L graphene. Theoritical(c) and Experimental(d) dependence of G'-band line on the number of layers.[41]

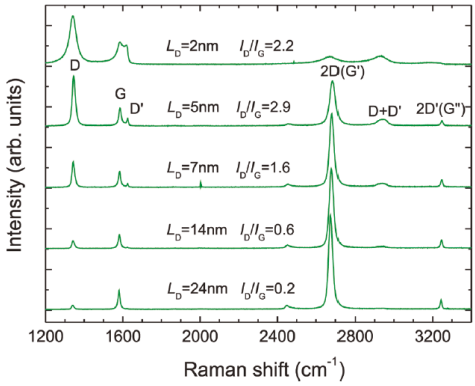


Figure 2.31: Raman spectras for different L_D.[42]

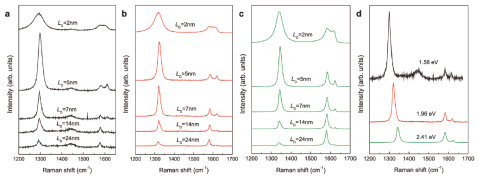


Figure 2.32: Raman spectra of five ion-bombarded SLGs measured with EL =1.58 eV (L =785 nm), EL =1.96 eV (L =632.8 nm), and EL =2.41 eV (L =514.5 nm), respectively. (d) Raman spectra of an ion-bombarded SLG with LD = 7 nm obtained using these three excitation energies.[42]

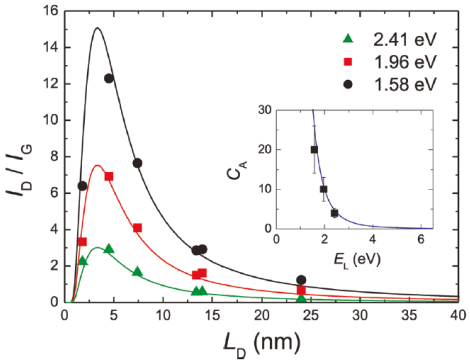


Figure 2.33: Intensity ratio vs L_D.[42]

2.5.2. Electronic Applications

As seen in the properties section, graphene exhibits excellent and unique electrical properties which would enable applications in the electronics field. A few of the published applications are briefly looked into, below.

Graphene FET's

Figure 2.37 shows the structure of a bilayer graphene FET. figure 2.37 (b) shows the three dimensional structure and (c) shows the layer structure with the channel region. The bilayer graphene is sandwiched between the top and bottom gates. The bottom gate is an SiO2 film that is 300 nm thick. The top gate is a dielectric stack that consists of first 9~12 nm of organic seed layer made from a polymer followed by a 10~11 nm film of HfO2.

The transport characteristics and transfer characteristics of the FET at RT and at 10 different temperatures can be seen in figure 2.38 and 2.39. Based on the observations made in [10][11], it was concluded that the bilayer graphene, at an average electrical displacement of 2.2 V/nm had an electrical badngap of >130 eV, ass uming the Schottky barrier height is about half of the electrical band gap which results in a large transport band gap.

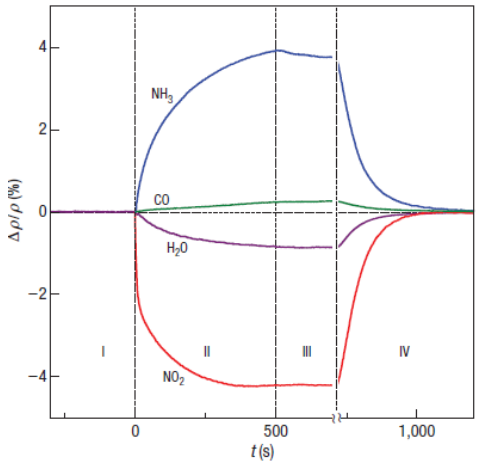


Figure 2.34: Differences in change in resistivities for different gases.[45]

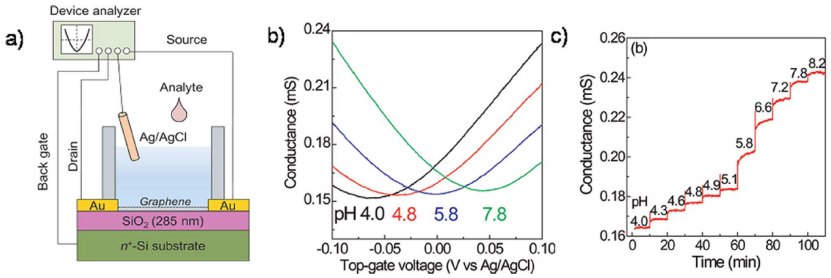


Figure 2.35: (a)Apparatus for the electro-chemical sensor. (b)Shift in conductance due to change in pH. (c)Conductance as a function of time.[4]

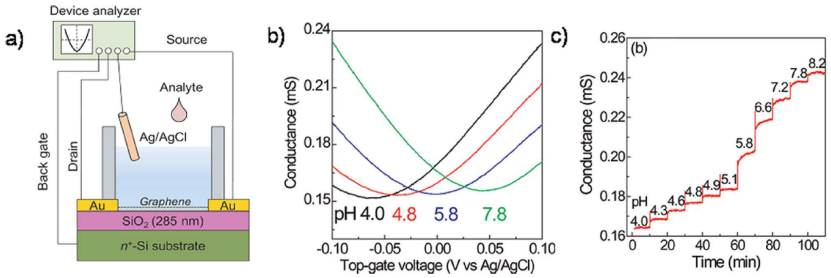


Figure 2.36: (a)Optical and (b)SEM image of GHE's. (c) Hall Voltage vs magnetic field and (d)Linearity error of GHE's in current mode.(e) Hall Voltage vs magnetic field and (f)Linearity error of GHE's in voltage mode.[46]

Photodetectors based on Graphene Schottky junctions

[47] shows a metal-semiconductor-metal(MSM) photodetectors where graphene plays the role of the metal. The schematic of the fabrication process is shown in figure 2.40. figure 2.40(f) shows the Raman spectrum of graphene transferred onto SiO2, measured at a laser wavelength of 632 nm. The strong peaks in D and G-bands show the good quality of graphene and the I'_G/I_G indicate the monolayer structure of the graphene. The voltage-current characteristics of the device and the energy band diagrams are shown in figure 2.41 and 2.42,and these are used to extract the Schottky barrier voltage, Φ B. A zero-bais fermilevel E_F of -0.25 eV and Schottky barrier height of 0.48 eV is obtained.

To characterize the photoresponse of the graphene MSM photodetectors, they were ill uminated with He-Ne laser (633 nm wavelength) at room temperature. The photocurrent and the dark current were observed(figure 2.43). From the figure, we can see that the device current increases close to five orders of magnitude at 5V bias under laser ill umination. The Responsivity and NPDR(Normalized photocurrent to dark current ratio)

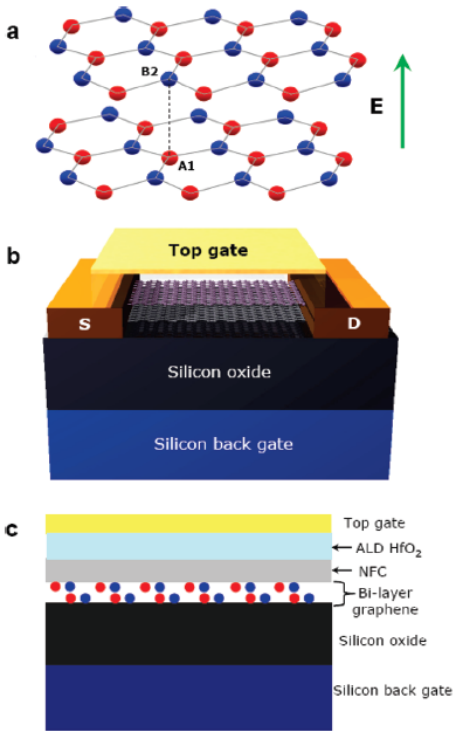


Figure 2.37: (a)Structure of bilayer graphene. (b)Graphene FET structure. (c)Cross-section of graphene FET.[46]

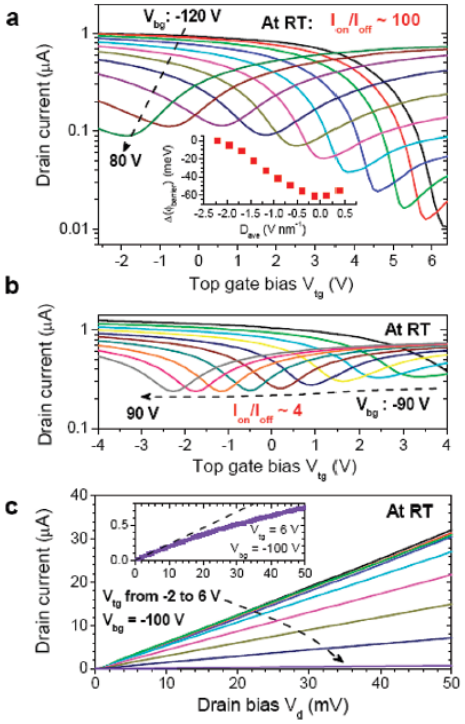


Figure 2.38: Transfer characteristics of (a)dual gate bi-layer graphene FET and (b)dual gate single layer graphene FET with varying V_bg at RT. (c)Transfer characteristics for graphene FET at fixed V_bg and varying V_tg.[10]

of the device at 5 V were calculated to be 0.11 A/W and 4.55 $mW^{-}1$ which are larger values when compared to the carbon nanotube film- Si MSM photodetectors.

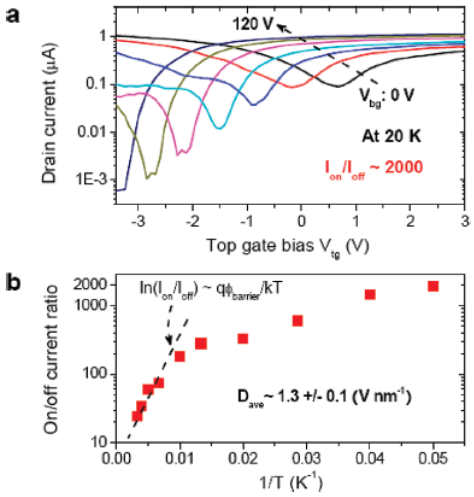


Figure 2.39: (a)Transfer characteristics of graphene FET varying temperatures. (b)The device on/off ratio vs temperature.[10]

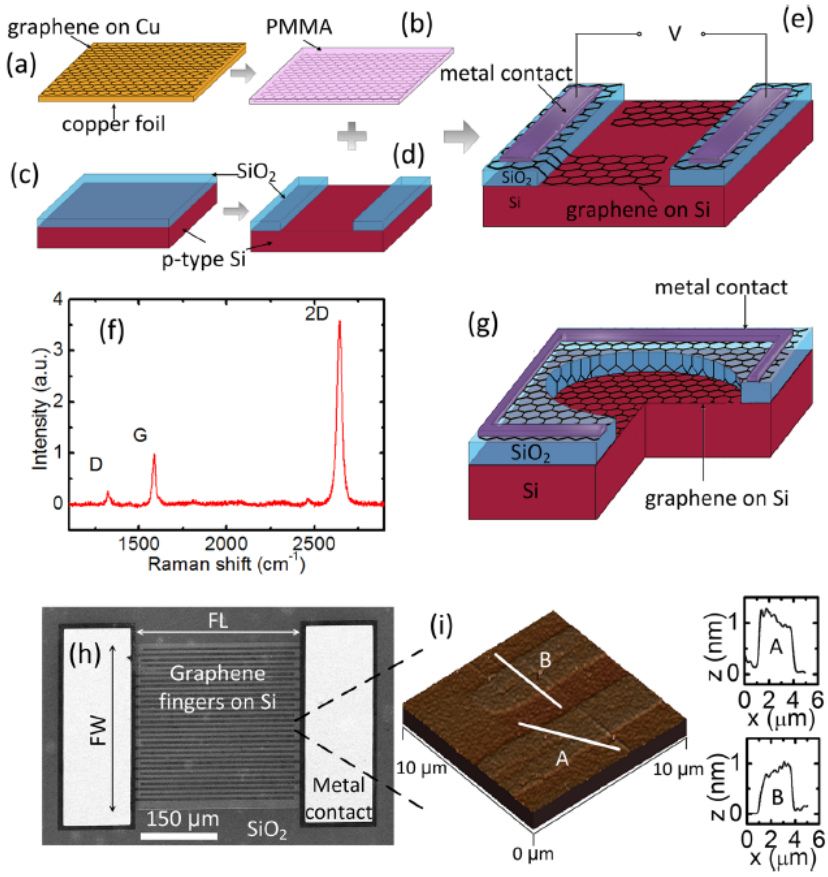


Figure 2.40: (a)-(e)Fabrication flow for graphene Schottky junctions. (f)Raman spectrum of graphene transferred onto SiO_2. (g)Cross section of the graphene Schottky junction. (h)-(i) Images of the fabricated Schottky junction.[47]

2.5.3. Optical applications

In photonic integrated ciruits, modulation of light is one of the key operations and a few papers have been published discussing how graphene can be used for the modulating light. The general schematic for light modulation is given in figure 2.44. Modulation of guided light is achieved by altering specific properties such as amplitude, phase and polarization.

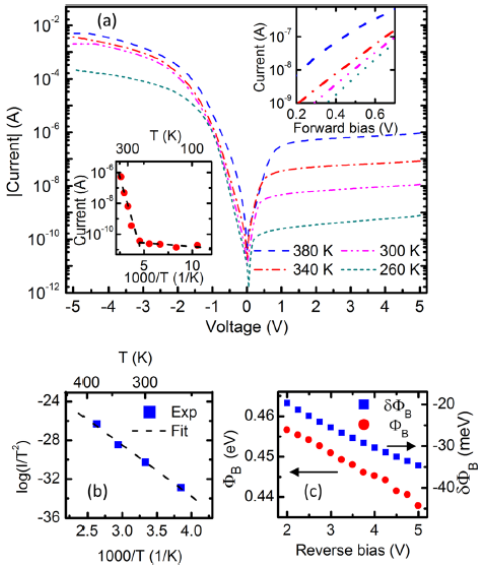


Figure 2.41: (a)Current Voltage characteristics of the Graphene Schottky Junction. (b) Richardson plot and (c)Experimental calculation of the Schottky barrier height.[47]

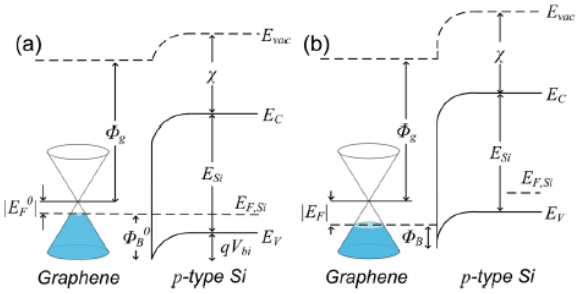


Figure 2.42: Energy band diagram at (a)thermal equilibri um and (b)Reverse bias voltage.[47]

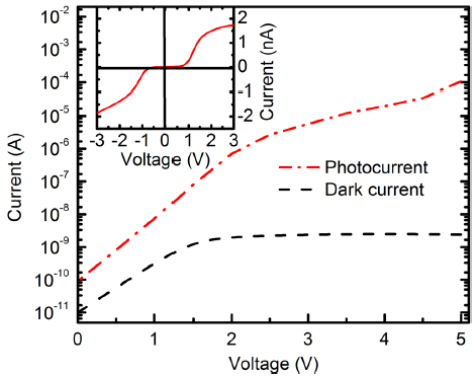


Figure 2.43: Photo current and Dark current as a function of bias voltage.[47]

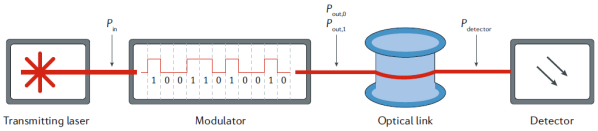


Figure 2.44: General schematic for light modulation.[8]

d

As a consequence of the lack of bandgap, SLG is a broadband absorber with 2.3% absorption for any wavelength of light at normal incidence, which is also mentioned in the optical properties in the above sections. So,superimposing SLG on a silicon wave-guide, it is possible to enhance the interaction of SLG with light. The absorption significantly increases from ~0.1 dB at normal incidence to thousands of dBcm^{-}1 when the light propagates along the wave-guide.

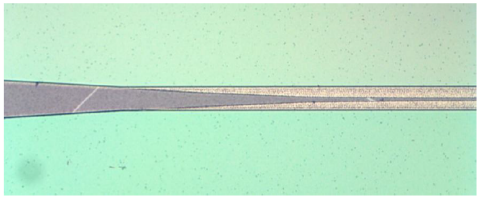


Figure 2.45: A taper in a waveguide.[9]

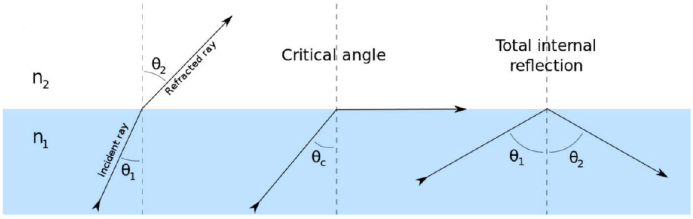


Figure 2.46: The phenomena of Total internal reflection.[8]

To understand how graphene interacts with the light propagating in the wave-guide, we first look into how light propagates in the wave-guide. Firstly, to make the connections between the light source and the wave-guides easier, a taper as shown in the figure 2.45 is used. After entering the wave-guide, light propagates in the wave-guides using the phenomena called Total internal Reflection (TIR). TIR occurs when the core's refractive index is greater than that of the cladding's refractive index in the wave-guide and when the angle of incidence of light in the wave-guide is greater than the critical angle whos equation is given in [9]. The phenomena of total internal refection is shown in figure 2.46 . As, the light propagates through the wave-guide, it hits the surface of the wave-guide at multiple points throughout its path. However, due to the wave-particle duality of light, an evanescent field(figure 2.47) is seen at these points of reflection. . This evanescent field can be absorbed using different materials, such as graphene, to alter the properties of the light propagating through the waveguide.

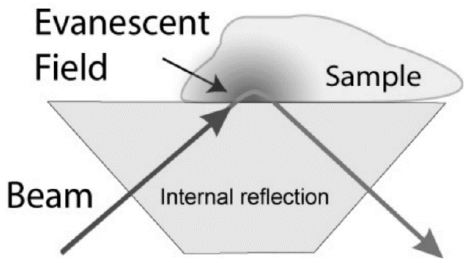


Figure 2.47: Evanescent field observed at the point of reflection, absorbed using an external material (Graphene in our case).[5]

The absorption of graphene can be reduced or be completely cancelled, by shifting the fermi energy of the SLG band. When the fermi energy of the SLG is larger than that of the propagating photons, SLG is more transparent as a result of Pauli blocking and the index of refraction changes. Defects in the graphene layer may also results in further background losses. To shift the fermi energy E_F, of the graphene that is superimposed on Si based wave-guides, a voltage is applied to the Si-insulator-SLG capacitor. Carriers get acc umulated in the SLG and the underlying Si wave-guide and as a result of plasma dispersion, the carriers in the Si wave-guide cause absorption. Therefore, even if the carriers make the SLG transparent for the high carrier concentration n_s ($E_F > 0.5$), they also make the Si opaque. Whereas for low carrier concentration n_s ($E_F < 0.4$), absorption

is mainly due to the interband transitions in the SLG as the losses due to Si are negligible. The absorption vs the carrier concentration graphs for different scattering times τ can be seen in figure 2.48(b). The scattering time here accounts for the presence of defects that affect the intraband transitions. Similar results(figure 2.48(d)) are seen for a double SLG configuration who's structure, along with that of the SLG-insulator-Si is shown in figure 2.48(a),(c). The curves follow a similar trajectory for all three scattering times. The curves are minim um in the range 10^-2 - 10^-3 for E_F = 0.5-0.6 eV and then increase due to the interband transitions. The losses in Si however, increase monotonically with n_s. This results in a wave-guide that is never transparent. For, double SLG configuration the losses decrease, when compared to that of the single SLG configuration. If n_s is further increased, (E_F > 0.6), losses increase again due to the interband transitions. Hence, electro-absorption modulators can be obtained by varying the absoption between $|E_F| < E_p h/2$ and $|E_F| > E_p h/2$ for both the single and double SLG configurations. The process flow to fabricate the single SLG configuration, electro-absorption modulator is shown in the figure .

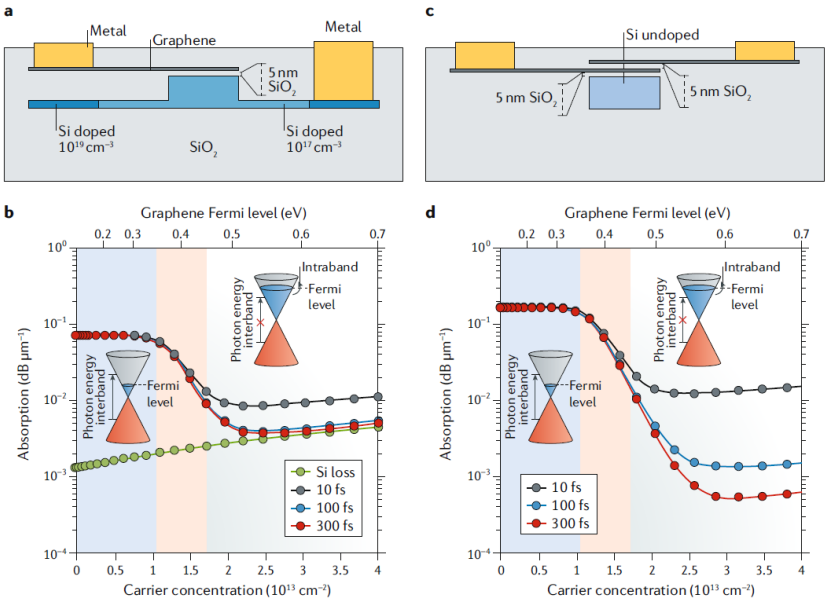


Figure 2.48: (a)Single SLG and (c)Double SLG on Si waveguide configuration and their absorption vs carrier concentration graphs(b),(d).[5]

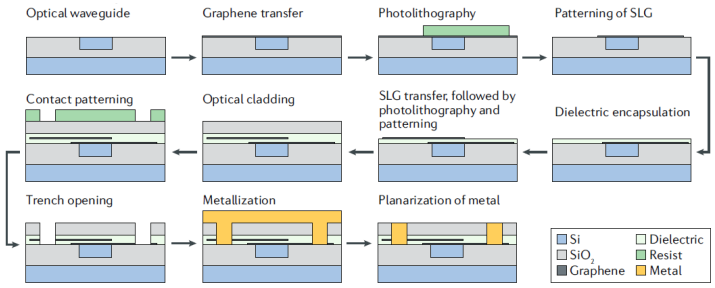


Figure 2.49: Fabrication flow for the graphene electro-absorption modulator.[5]

A similar kind of electro-refractive modulator (figure 2.50) is discussed in [6] which uses a single SLG configuration albeit on two arms, with different lengths of SLG to introduce a biased phase difference in the balanced interferometer structure for characterization process. The quality of the graphene films used for each of the arms is checked using Raman spectrography and the spectra shows a negligible D to G intensity ratio which suggests no significant degradation and/or defects have been introduced in the films during the fabrication. The Electro-optical bandwidth, the eye-diagram and the transmission measurements corresponding to the modulator are shown in figure 2.51 and 2.52. And it is observed that the modulator demonstrates a good modulation depth of 35dB and a modulation efficiency of 0.28 Vcm, outperforming the state of the art SIS-capacitor based modulators and Si-based pn-junctions. The modulator also operates at 10 Gbit/s show-

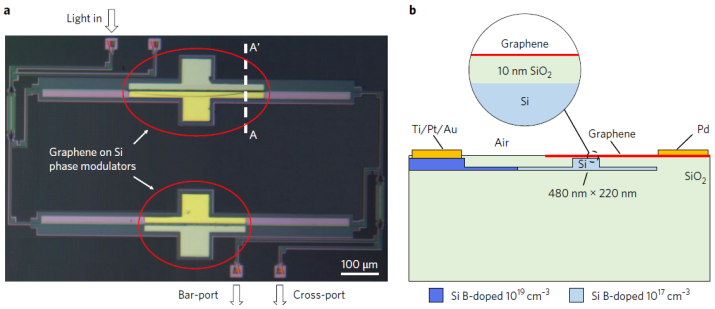


Figure 2.50: (a)Optical Image of the MZI modulator. (b)AA' Cross section of the MZI modulator.[6]

ing error-free transmission over 50km SME and an open-eye diagram. The results suggest the realization of graphene modulators for wide range of applications.

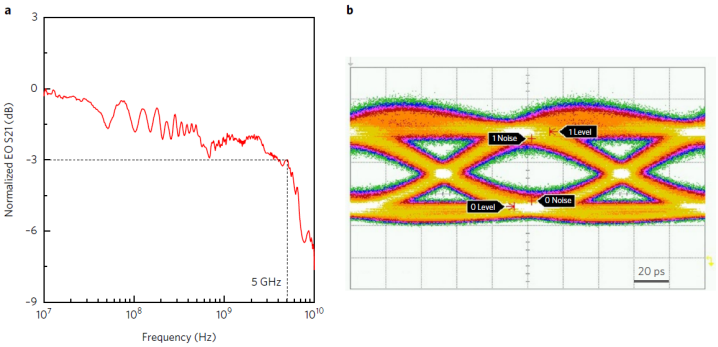


Figure 2.51: (a)Optical Bandwidth and (b)Eye diagram corresponding to the MZI modulator.[6]

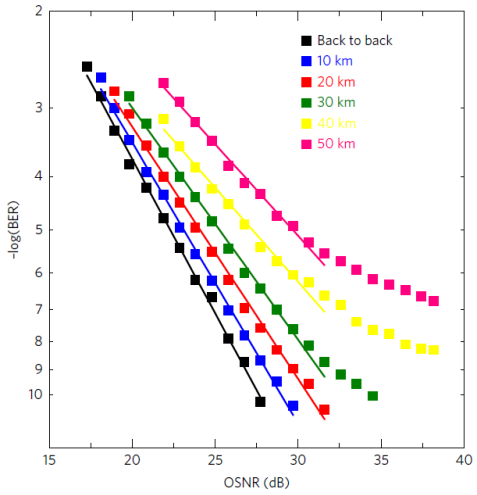


Figure 2.52: Transmission measurements of the MZI modulator.[6]

2.6. Contacting graphene

In this section, we look into a method to contact graphene [48] while keeping the contact resistance minimal. Figure 2.53(a) shows a fabrication flow for contacting graphene. And as seen in the flow, lithography is used in atleast one of the process steps in the common contacting techniques. However, the use of a lithographic process without treatment results in ρ_c values $> 10^{-5}\ \Sigma\text{cm}^2$. This is due to the fact that the residual photoresist from the lithography process is left untreated as revealed by X-ray photo-electron spectroscopy (XPS). figure 2.53(b) shows the poor interface between the graphene and the metal. XPS graphs of pristine graphene is

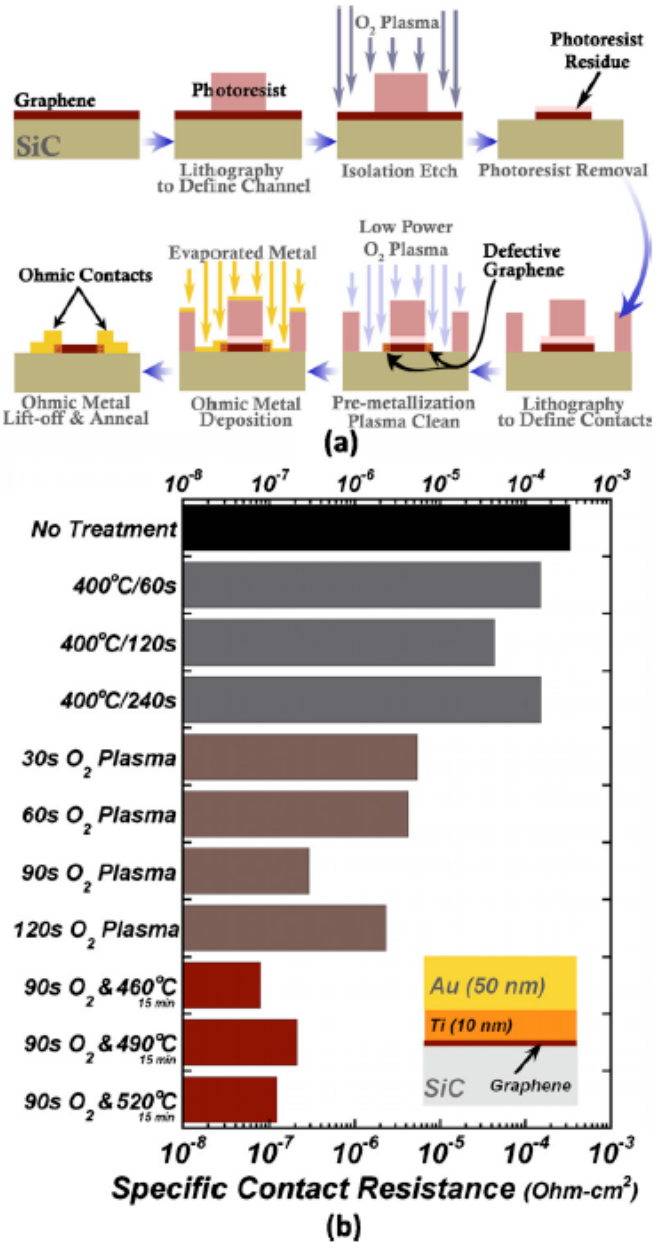


Figure 2.53: (a)Fabrication flow for contacting graphene. (b)Measured contact resistances for different methods.[48]

shown in figure 2.54 and it can be seen that there is no evidence of carbon-oxygen bonding. However, carbon-oxygen boding can be found upon checking the graphene post-metalization which suggests that the graphene is still covered with photoresist residue. Intitally, rapid heat treatments were used which did decrease the contact resistance, but value still stayed above 10^{-5} Ωcm^2. So, a low-power O2 plasma (O2 ash) treatment is utilized prior to metal deposition and this provides superior contact resistance. And as seen in figure 2.53(b), the use of O_2 ash results in the removal of the residue photoresist which can be seen by the decreasing 2D band peak. It is known, that the defectiveness of graphene grows upon O2 exposure and hence the exposure to O_2 ash needs an optimum time to get the best results. It is found that as the plasma treatment time increases from 30-90s, the contact resistance decreases and starts increasing, once the treatment time reaches 120 s and this increase in contact resistance correlates with the severe degradation of graphene and can be seen in the Raman spectroscopy results of figure 2.54(c). It is also found that the graphene that is used for the metal contacts gets degraded, but the graphene between the metal contacts remains untouched which is confirmed by the hall effect measurements, which show no degradation in graphene carrier mobility. Post-processing

heat treatments after the O2 plasma treatment, further improve the contact resistance. This suggests that the furnace anneal is a multi-functional process that improves the contact resistance and simultaneously removes the contaminants prior to the further device processing.

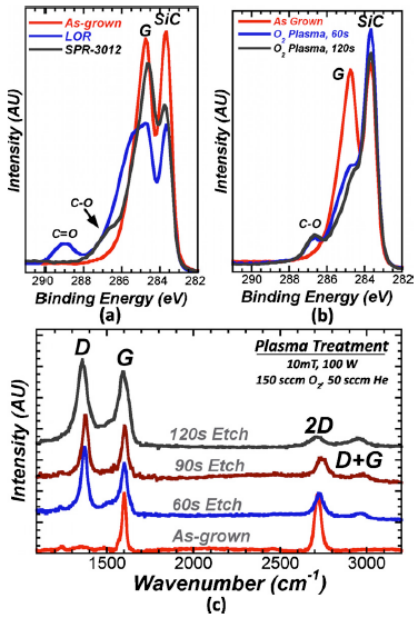


Figure 2.54: XPS of the contact (a)before and (b)after the O_2 Plasma treatment. (c)Raman Spectrascopy of the graphene on the device before and after the plasma treatment.[48]

The specific contact resistances for different materials can be seen in figure 2.55(a). A high work function difference between the graphene and the metal contact can results in problems which is why, when aluminium is used for the metallization, delamination occurs at the points of contact, as seen in figure 2.55(b).

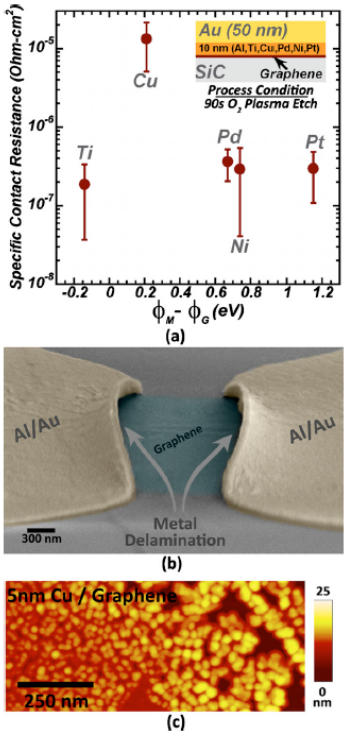


Figure 2.55: Correlation between specific contact resistance and work function for different metals. (b)Delamination of contacts. (c)agglomeration of Cu films.[48]

3

Simulations

As mentioned previously, ANL is interested in knowing the properties and behavior of the graphene films fabricated by them. The fabrication of hall-bars already has a known process flow, but there are still some unknowns when it comes to the fabrication of the electro-optical modulators. We need to find out the dimensions of the Silicon waveguides in the modulators and the thickness of the oxide on top of the waveguide (cladding). And further optimize these dimensions according to our requirements. The analysis is done by simulating the waveguide structures in BeamLab and COMSOL and comparing the results.

For the testing of optical properties, a 1320 nm SLED is used as the light source for the optical modulators. We initially use the dimensions of 1 um width (minimum dimensions that can be fabricated in a controlled method) and 350 nm height (thickness of the upper Silicon layer in the Silicon on Insulator (SOI) wafer) a start point for the waveguide and then optimize such that the 1320 nm wavelength propagates through the waveguide without any drastic losses and produces an acceptable intensity of evanescent field (around the order of 10^7 V/m for our simualtions) which is to be absorbed by graphene for the optical modulation. Varying widths of the waveguide are simulated and we check if light propagates through the waveguides without any losses. Varying thickness' of the oxide layer on top of the waveguide (cladding) are also simulated to check how the evanescent field changes with respect to change in thickness of the oxide. The simulations for the varying width and varying oxide (cladding) thickness are done to check how the profile of the electric field intensity at the air oxide interface (the evanescent field), for the graphene to absorb, changes with respect to a change in width or thickness. It is expected that as the width of the waveguide increases, the intensity of the evanescent field decreases as the intensity is more evenly divided across the larger volume of the waveguide. Similarly, as the thickness of the cladding increases, the intensity of light reaching the air-oxide interface decreases. The parameters such as thickness, width and intensity mentioned above are quite important when designing the optical modulator. As, we need sufficient evanescent field intensity for absorption by graphene such that a noticeable change is observed at the detector and also sufficient cladding thickness is also needed such that TIR occurs without any significant losses.

3.1. Simulations using BeamLab

BeamLab is a set of simulation tools for beam propagation through optical devices and waveguides in MATLAB® environment. Initially, BeamLab was used to simulate the varied waveguide dimensions and oxide thickness', due to its alternative (COMSOL) taking a lot more computational time and memory. The simulations for the waveguide widths being varied from 1 um to 10 um with increaments of 0.5 um while keeping the oxide thickness constant are done. An example of the input waveguide structure is shown in the figure 3.1. And the simulations results for the electric field intensity profile for a few of the simulated waveguides is shown in the figure 3.2. It is to be noted that, the length of the waveguide is along the z-axis, which cannot be seen. A length of 8000 um (8 mm) was set for the simulations, which is about the size of the waveguides that we would be fabricating.

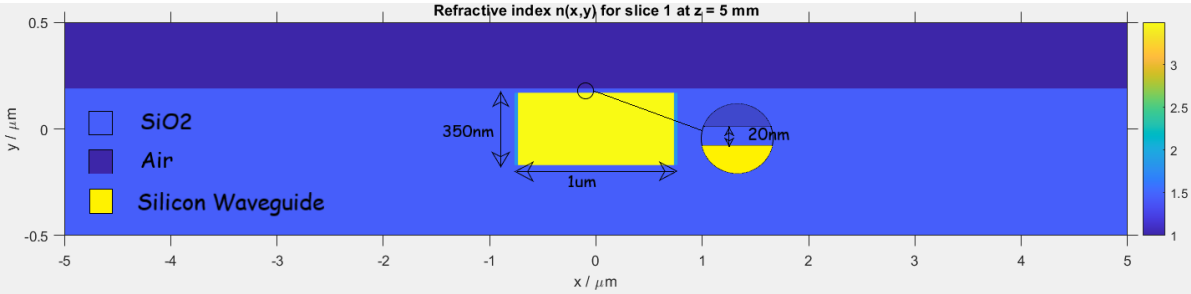
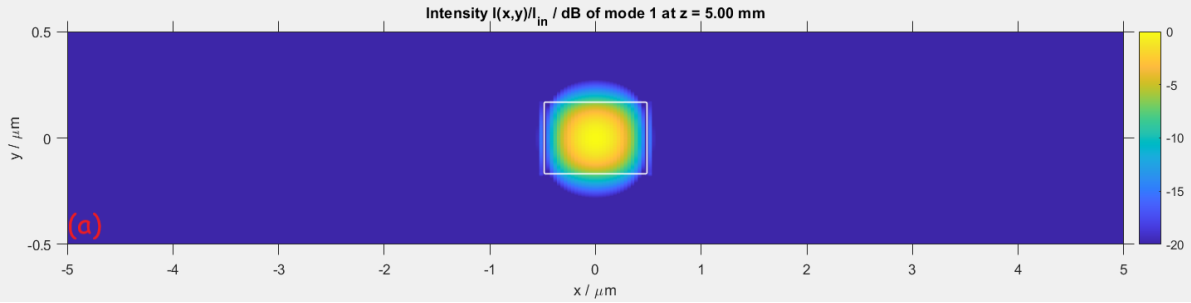
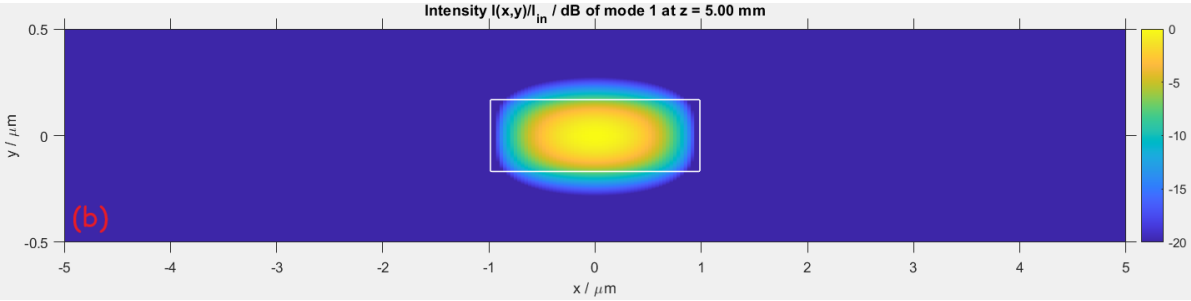
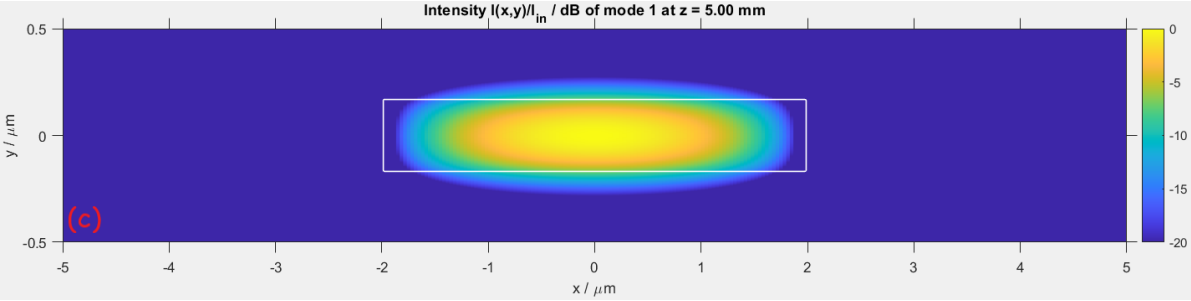


Figure 3.1: An example of the wave guide structure used as the input for simulations







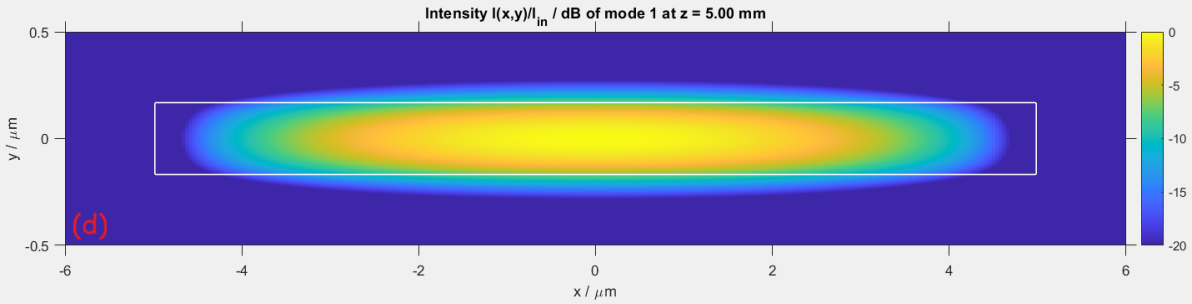
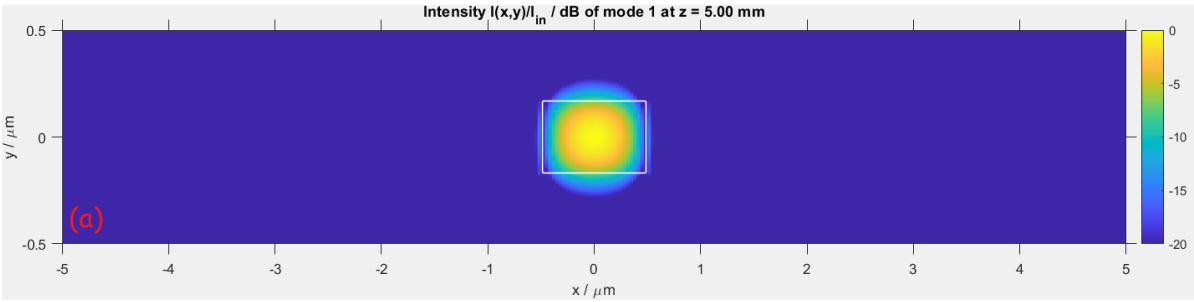


Figure 3.2: Electric field intensity profile simulations where the width of the waveguide simulated is (a)1 um, (b)2 um, (c)4 um and (d)10 um

In the figure 3.2, what we see is the distribution of E-field intensity of the light propagating through the waveguide for different widths of the waveguide at 5 mm, which is where the light exits or is detected. This first confirms that the light propagates through the waveguide and reaches the end without any significant losses. And as expected, majority of the light intensity (represented by yellow color) is within the waveguide. However, there is a small amount of light observed outside the waveguide (represented by light blue color), which is the evanescent field that we hope to absorb using graphene and modulate the signal. But, we cannot tell for sure if the evanescent field reaches the oxide-air interface (where graphene in present) or even the value of the intensity of light reaching the oxide-air interface in BeamLab simulations due to the limitations of the software. Which is also one of the reasons why we switch to COMSOL, whose simulations are seen in the next section.

Now, the thickness of the oxide sitting on top of the waveguide (cladding) varying from 5 nm to 50 nm is simulated which can be seen in the figure 3.3. As mentioned above, the oxide here acts as the cladding for the waveguide and the cladding is the reason why the propagation of light through the waveguide is possible using Total Internal Reflection (TIR). A varied cladding thickness is simulated to find the optimal thickness for the device. A thinner oxide results in higher amount of evanescnent field at the oxide-air interface, which is absorbed by the graphene to cause modulation, but during fabrication it is not easy to control the process to get a thickness of 5 nm. The length of the waveguide was set as an arbitrary value of 5000 um and the height of the waveguide stays constant at 350 nm in the simulations. The height of the waveguide is unchanged at 350 nm due to the specifications of the Silicon-on-Insulator wafers (SOI wafers) provided by Else-Kooi Lab (EKL lab) for the fabrication of the said waveguides. The specifications are that the thickness of the Silicon on the insulator is ~350 nm and hence the maximum height of the waveguide achievable during fabrication is 350 nm. As stated above, the range of the width in the simulations is set as 1um and 10 um. The lower limit of 1 um is set because fabricating structures with dimensions <1 um using the available resources in the EKL lab becomes more and more complex to be achieved. Whereas, the upper limit of 10 um is set because the e-field intensity distributed inside the waveguide increases as the width or volume of the waveguide increases, which results in insufficient intensity of evanescent field formed that is to be absorbed by the graphene film. When it comes to the oxide thickness we have more control in achieving oxide thickness' in the nm scale due to the process of thermal oxidation being slower. The oxide acts as the cladding for the waveguide and the range of 5 nm to 50 nm is set so as to optimize the amount of evanescent field reaching the graphene for the modulation. Lower thickness naturally results in more evanescent field at the air-oxide interface than thicker oxide. But, we need to have enough oxide for TIR to occur as well.



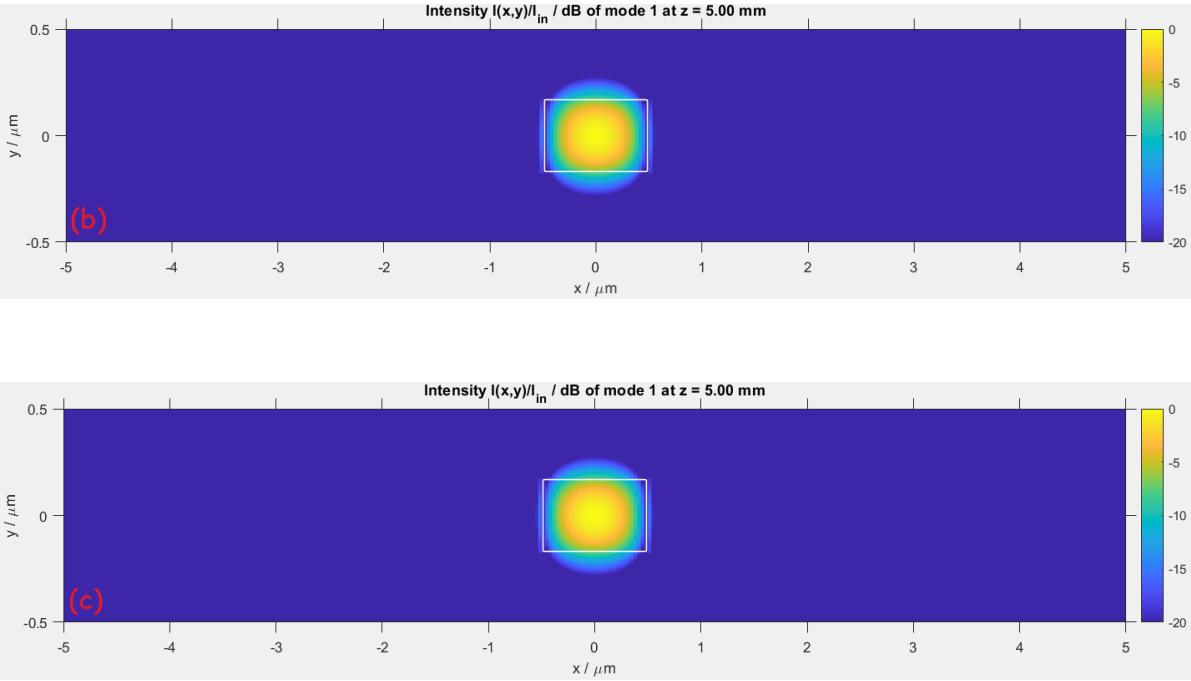


Figure 3.3: Electric field intensity profile simulations with varying oxide thickness where the dimensions of the waveguide kept unchanged at 1umx350 nm. (a)10 nm, (b)20 nm and (c)50 nm

Similar to the simulations seen in figure 3.2, in figure 3.3 we see that majority of the light is distributed inside the waveguide (Yellow) and some evanescent field is seen outside the wavguide (light blue). And even in these simulations, we can't see if the evanescent field reaches graphene which is checked in the COMSOL simulations to make further decisions.

Analysing the simulation results in the figure 3.2, we can see that light propagates without extreme losses starting from the lowest width of 1um. So, during the fabrication, we have to set the minimum width of the waveguide as 1 um which is also the minimum length dimension that can be fabricated in the EKL lab.

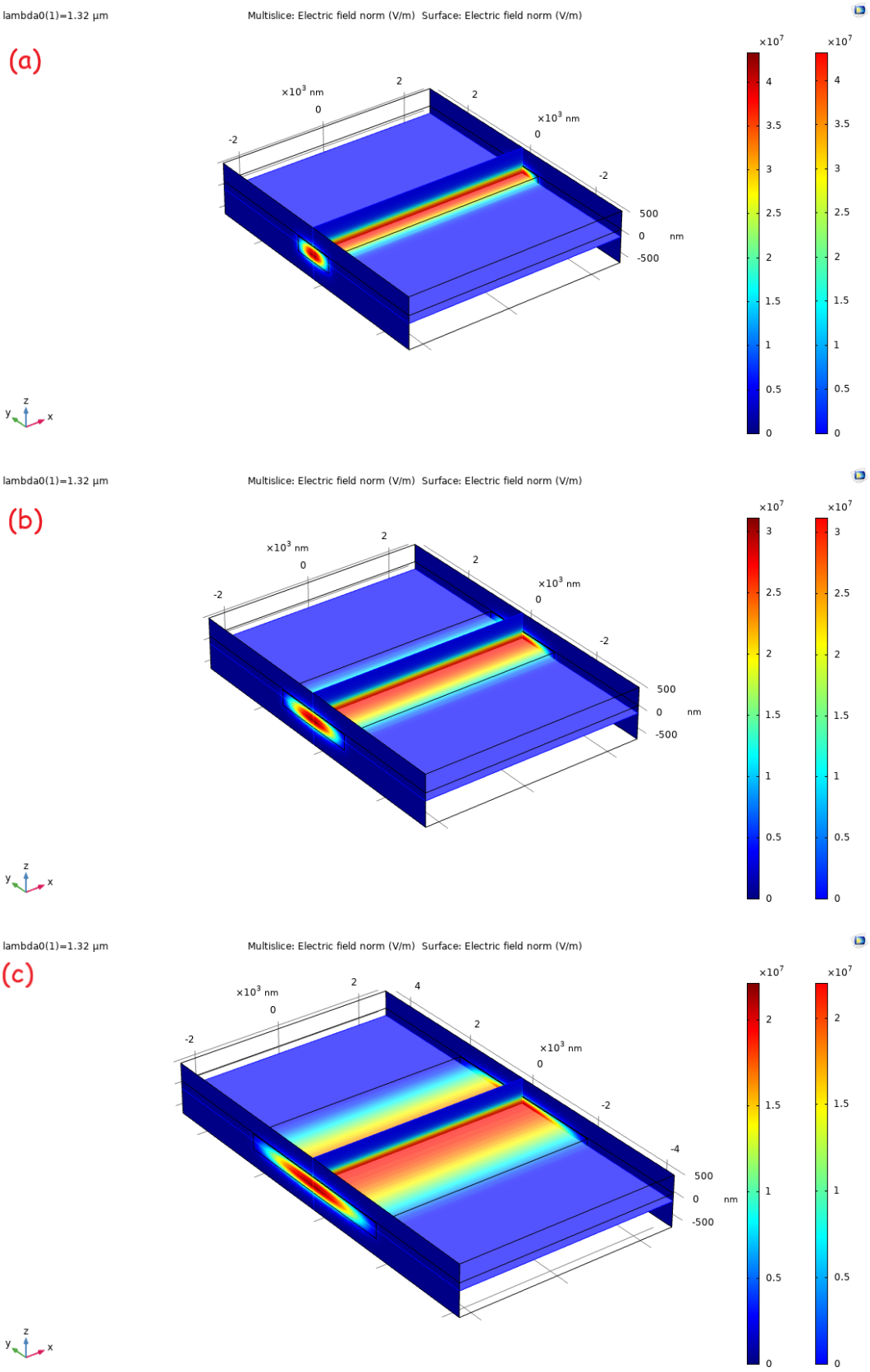
Now, when we look into the varying oxide thickness simulations in figure3.3, all the images pretty much show the same amount of evanescent fields. And even if there was any change in field, it is hardly noticeable in the simulations. A thickness of ~20 nm is expected to be used for our fabrication. However, we do need to verify if this thickness is suitable for the wavelength of light we're using and also check for the optimal width of the waveguide before the fabrication. For the verification of the parameters stated above, we need to know the absolute value of the electric field intensity at required points (namely the oxide-air interface). Upon further testing of the software, we could not find the absolute value of the electric field at a particular point in the simulations done using BeamLab. Additionally, the minimum wavelength of light that can be simulated in BeamLab is 1360 nm, which is slightly higher than our wavelength of light, 1320 nm, which might cause a slight deviation in expected results. Hence we switch to COMSOL and try the waveguide simulations there for better analysis.

3.2. Simulations using COMSOL

COMSOL Multiphysics is a cross-platform finite element analysis, solver and multiphysics simulation software. We use the "Beam Envelope" physics to simulate the optical waveguide in COMSOL.

3.2.1. Waveguide Simulations for varying widths and oxide thickness

Similar to the simulations done in BeamLab, a range of 1um to 10 um for the width of the waveguide and a thickness range of 5 nm to 50 nm (while keeping the thickness of constant at 10 nm) for the oxide while keeping the height constant at 350 nm and length constant at 5000 um, is simulated in COMSOL and a few of the results can be seen in figure 3.5.


lambda0(1)=1.32 µm
Multislice: Electric field norm (V/m) Surface: Electric field norm (V/m)
(a)
(b)
(c)
×10^3 nm
×10^3 nm
500
0
-500
nm
×10^7
z
y
x

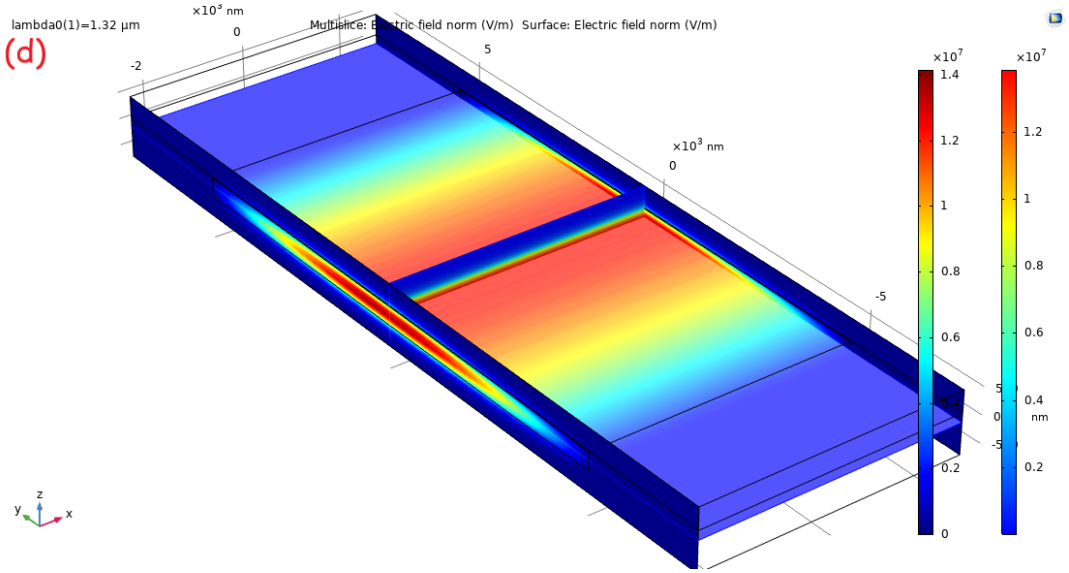
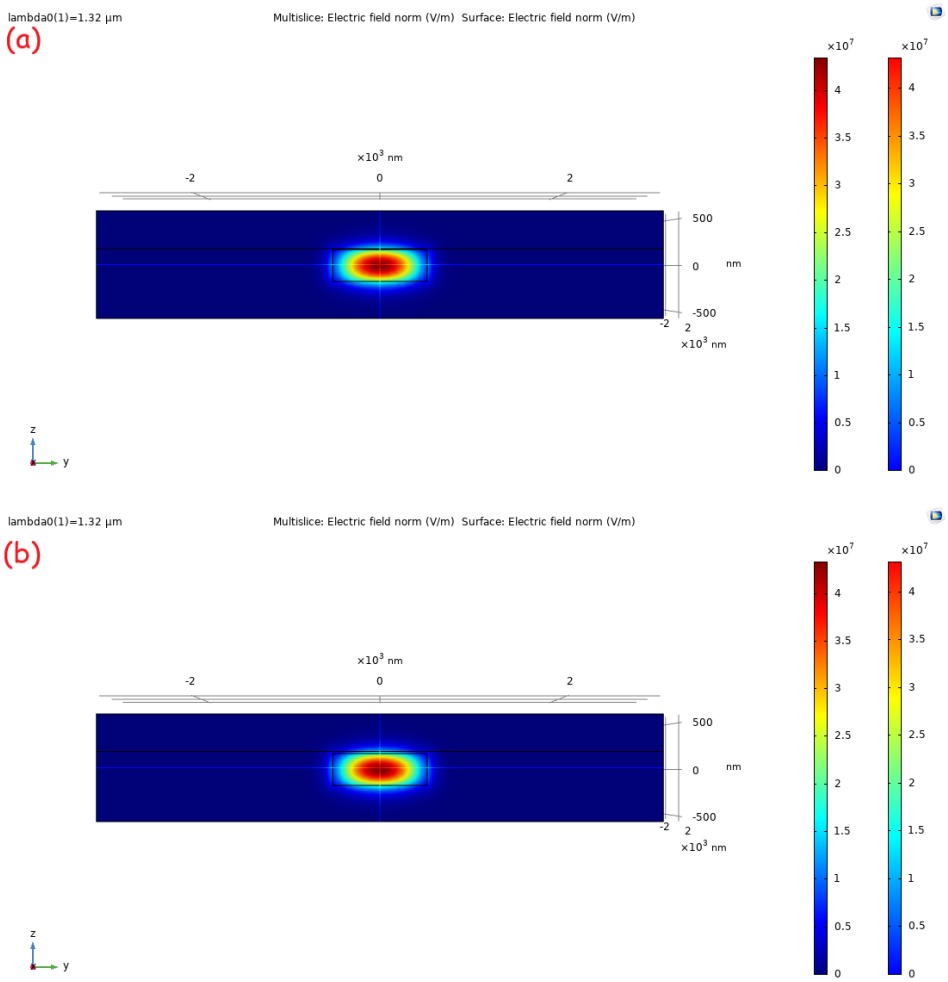


Figure 3.4: Electric field Intensity simulations where the width of the waveguide simulated is (a)1 um, (b)2 um, (c)4 um and (d)10 um



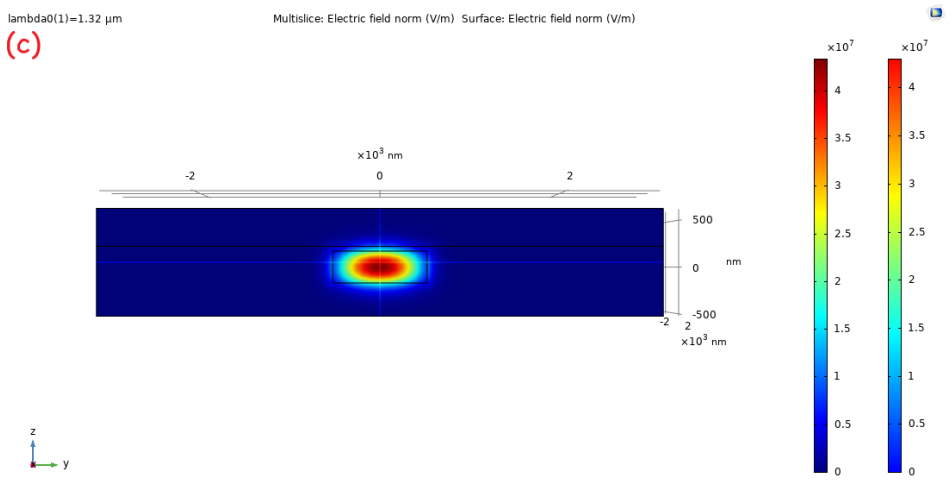


Figure 3.5: Electric field Intensity simulations where the thickness of the oxide simulated is (a)10nm, (b)20nm and (c)50nm

From the figures, the following information can be extracted. Firstly, we do observe an evanescent field around the waveguide and we do see that the light reaches the oxide-air interface, which allows the graphene to absorb it for optical modulation. Secondly, we see that light propagates through the whole waveguide structure without any significant losses. However, we do need to measure the magnitude of E-field reaching the oxide-air interface, to decide for the optimum dimensions of the waveguide structure. So, we use evaluation point simulations to find out the intensity of the evanescent field on the air-oxide interface. The observation of the evanescent fields also suggests that the range of widths and thickness' more or less lies within the working conditions of the optical modulator. The working condition here refers to the need of sufficient evanescent field intensity for absorption by graphene such that a noticeable change is observed at the detector and also sufficient cladding thickness needed such that TIR occurs without any significant losses.

3.2.2. Evaluation Point Simulations

Now that we have an acceptable working waveguide simulation, we can start optimizing the width and thickness by measuring and comparing the Electric field at certain set points. COMSOL has an option to put an evaluation probe point at any point in the structure to measure any required parameters at that particular point after the computations. This can be used to measure the electric field at the required points for further analysis of the simulations.

Width(um)	Electric field intensity(V/m)	Width(um)	Electric field intensity(V/m)
1	1.57E+07	6	6.55E+06
1.5	1.29E+07	6.5	6.29E+06
2	1.12E+07	7	6.05E+06
2.5	1.01E+07	7.5	5.86E+06
3	9.20E+06	8	5.68E+06
3.5	8.53E+06	8.5	5.45E+06
4	7.93E+06	9	5.34E+06
4.5	7.52E+06	9.5	5.15E+06
5	7.18E+06	10	5.14E+06
5.5	6.86E+06		

Table 3.1: Evaluation Point Simulations for varying widths

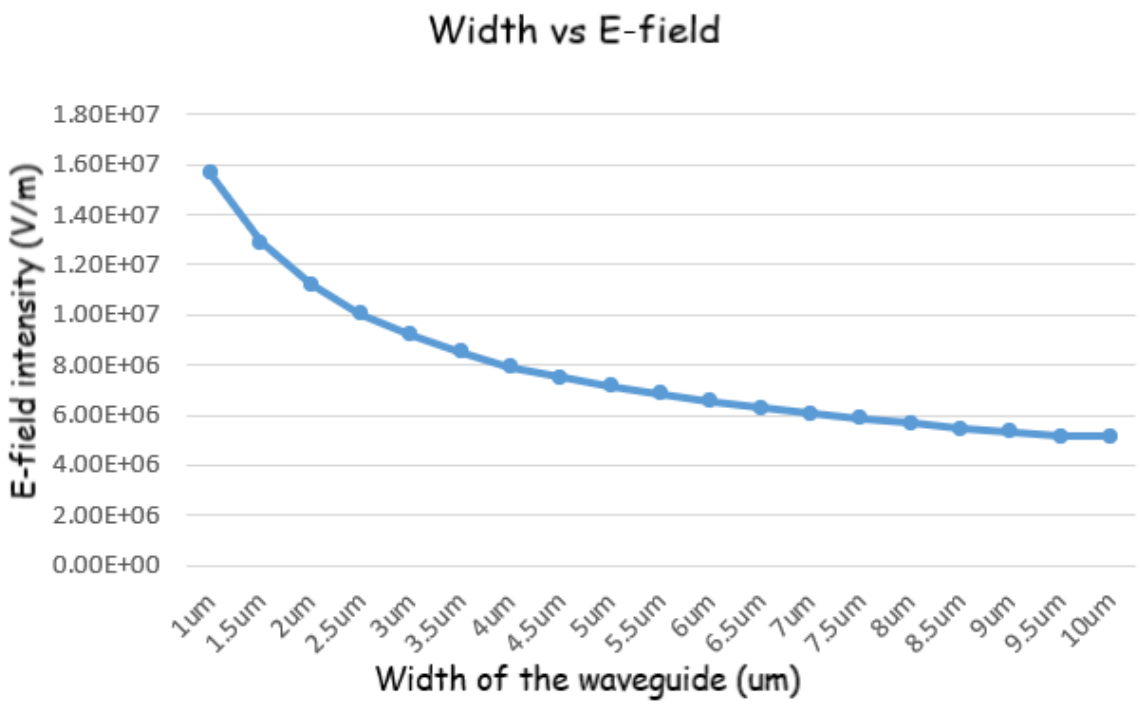


Figure 3.6: Graph showing the variation in the electric field intensity at the oxide-air interface for a change in the width of the waveguide

Firstly, we measure the electric field at the oxide-air interface at the centre of the waveguide (i.e at (0,0,(height of waveguide/2 + thickness of oxide)), which is where the monolayer graphene film would be during our fabrication or in our final device for absorbing the evanescent field. This measurement is done for varying widths of the waveguide while keeping the thickness of the oxide constant at 20 nm and height of the waveguide constant at 350nm. The length of the waveguide is also set at an arbitrary value of 5000 um like in the previous simulations. Table 3.1 shows the Electric field measured at the set evaluation point for their respective widths and figure 3.6 shows the plotted values of the table.

Oxide Thickness(um)	Electric field intensity at the air oxide interface(V/m)
5	1.66E+07
10	1.56E+07
15	1.46E+07
20	1.37E+07
25	1.29E+07
30	1.21E+07
35	1.13E+07
40	1.05E+07
45	9.85E+06
50	9.09E+06

Table 3.2: Evaluation Point Simulations for varying thickness'

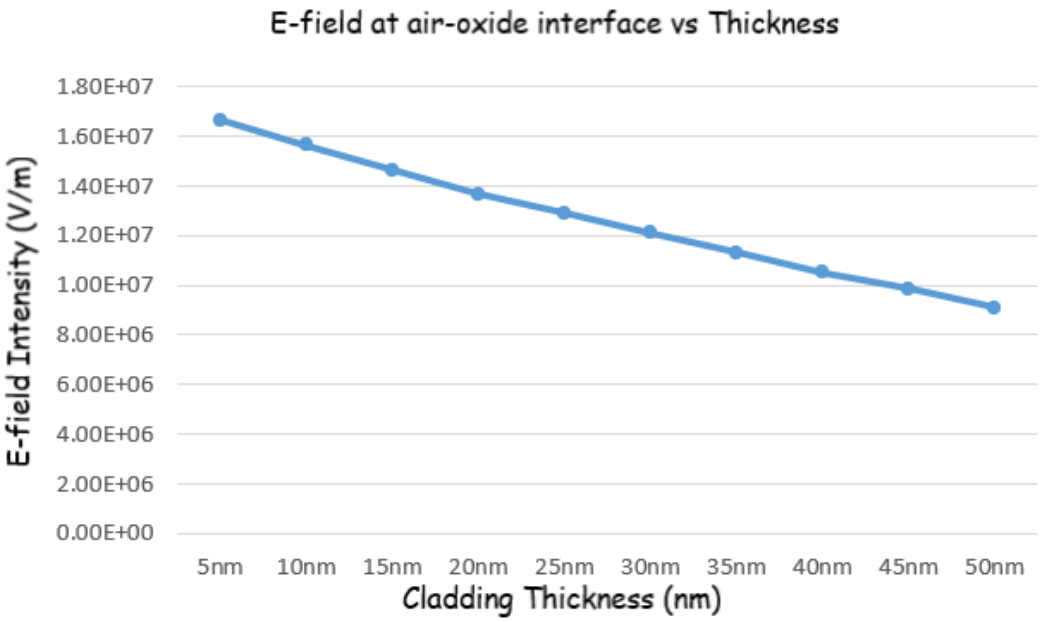


Figure 3.7: Graph showing the variation in the electric field intensity at the oxide-air interface for a change in the thickness of the oxide

Now, we keep the width of the waveguide constant as 1 um, the height as 350 nm, the length as 5000 um and vary the thickness of the oxide on top of the waveguide or the cladding thickness, and measure the electric field again at the oxide-air interface (i.e at (0,0,(height of waveguide/2 + thickness of oxide)) using the probe point evaluation. Table 3.2 shows the electric field measured at the set evaluation point for their respective widths and fig shows the plotted values of the table. Upon analysing the results from tables - and figures, we have decided to use widths ranging between 1um and 4um as the final set width of our waveguide. This range is selected because we want the E-field at the oxide-air interface closer to the order of 1E+07, and the value goes well into the 1E+06 starting from 4.5um. Similarly, a cladding thickness of 20 nm is selected for fabrication so that one, the cladding is not too thin or thick and two, the E-field intensity stays around the value of 1E+07 for all widths.

3.2.3. Simulation of the actual waveguide configuration

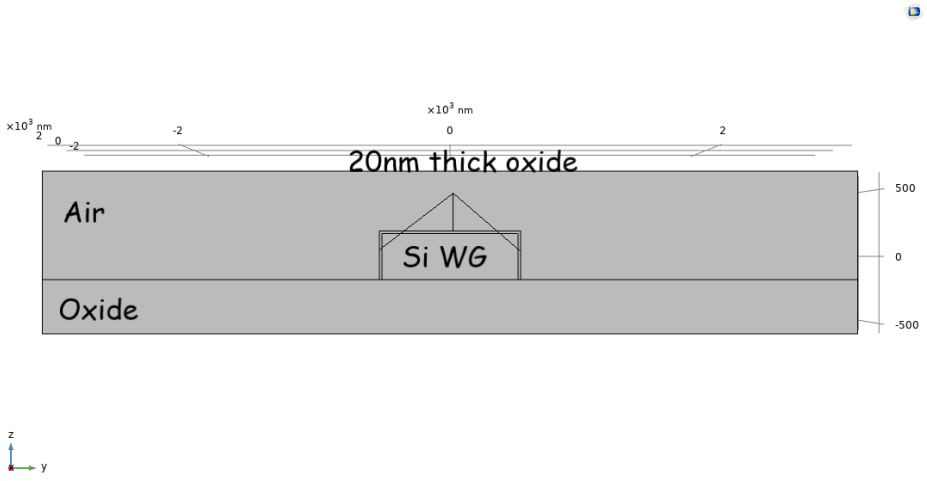


Figure 3.8: COMSOL simulation of the actual waveguide configuration

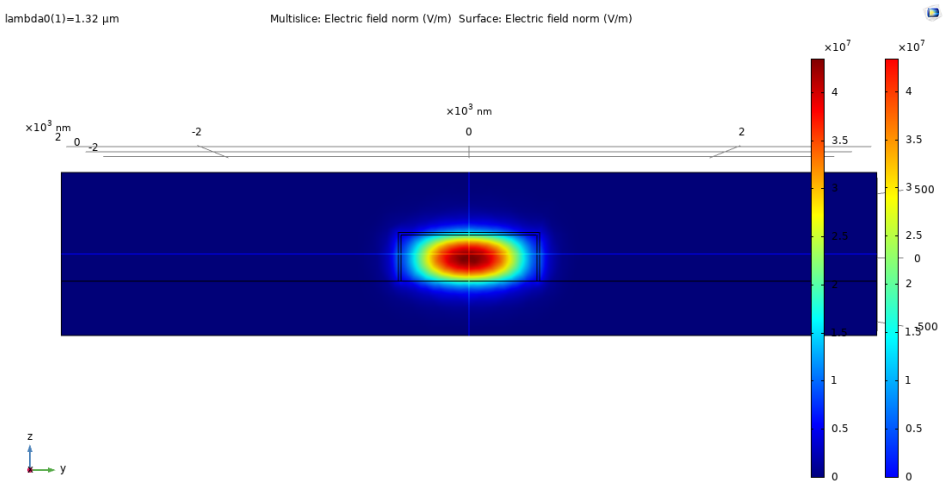


Figure 3.9: COMSOL simulation of the Electric field intensity of the actual waveguide configuration

When we try to fabricate the waveguide structure, during the oxidation process its not easy to control the process flow such that we have thick oxide on the sides of the waveguides and a few tens of nm of oxide on the top of the waveguide. And we need oxides on all the sides of the waveguide, so that there are no leakages during the propation of light. Hence, we first etch the waveguide structures, then thermally oxidze these waveguides structures such that a few tens of nms of oxide is on all sides of the waveguide as seen in the figure.3.8. The structure of the waveguide simulated in the above two subsections is close to what the actual structure of the waveguide and the simulation results would be more or less the same for the simulated structure and the actual structure. However, we do need to verify if the actual structure of the waveguide is compatible for light propagation and we do need to check if evanescent fields are indeed produced when light propagates through it. Which is why we simulate the actual structure for verification purposes for the following specifications. A waveguide with a width of 2 um, height of 350 nm, length 5000 um and an oxide of 20 nm thickness on the top and sides of the waveguide is simulated and the results are shown in figure. 3.8 and 3.9.

Figure 3.8 shows the waveguide configuration where the oxide present around 3 of the 4 sides of the waveguide are only 10nm thick. Also, from the figure 3.9, we can verify that the results are similar (an electric field intensity of about 1.42E+07 V/m is observed) to simulation results in the previous subsections (3.1 and 3.2 and hence verify that the actual configuration does work according to our requirements.

3.3. Waveguide Taper Simulations

As we know, we use the 1320 nm SLED as the light source in our experiment. The diameter of the optical fiber through which the SLED exits is 10 um and we need to guide this light into the waveguide with a minimum width of 1um. And as shown in figure 2.45, a taper can be used to make the connection between the light source and the waveguide easier.

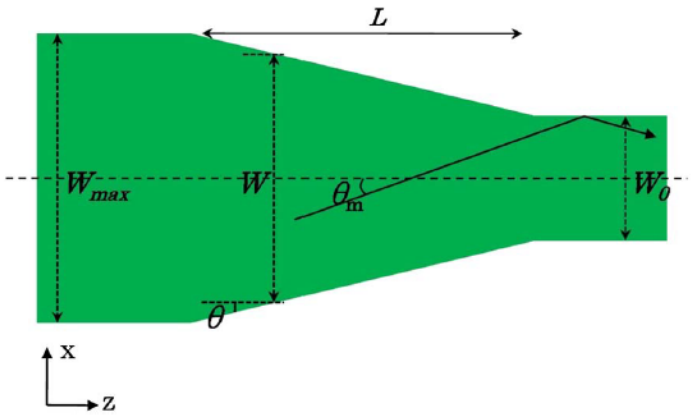


Figure 3.10: Top view structure of a linear waveguide taper [49]

The equation to calculate the maximum taper angle for which the light propagates through the taper without prominent losses as seen in [49] is given below. where θ is the local half angle of the taper at the point z, λ_0 is the wavelength in vacuum, n_{eff} is the effective index of the mode, α is a constant that was calculated to be between 1 and 1.4 and W is the local full width of the taper at point z, as shown in figure 3.10.

$$\theta = \alpha \frac{\lambda_o}{2W n_{eff}} \tag{3.1}$$

Using equation , we calculate the maximum angle for which light propagates without losses as ~1deg taking the Width W as the maximum value, 10 um. Hence, we set the taper length as 500 um, which gives a taper angle of 0.5 degree, which is lower than the calculated maximum taper angle and simulate it in COMSOL. However, COMSOL faces difficulties in meshing the taper structure, which ultimately prevents the computation of the electric field. Therefore, we again switch to BeamLab, as this particular simulation only needs to verify if the calculated taper length or angle is enough for light propagation from 10 um (Light source diameter) to 1 um (waveguide width).

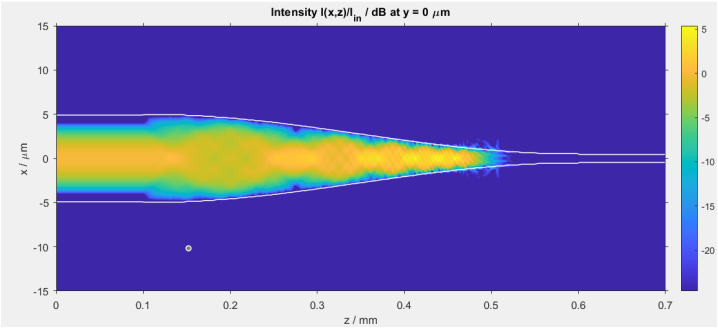


Figure 3.11: BeamLab simulation of a 10 um to 1 um taper waveguide with taper length 500 um

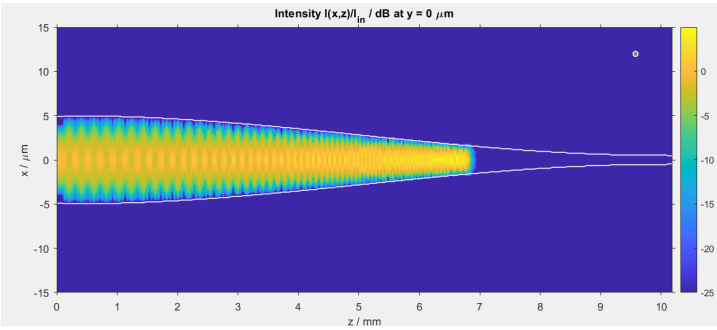


Figure 3.12: BeamLab simulation of a 10 um to 1 um taper waveguide with taper length 10mm

The simulation of a taper from 10 um to 1um with a taper length of 500 um is shown in the figure 3.11. It is to be noted that the height of the waveguide is constant at 350 nm throughout the whole waveguide structure, including the taper part. As seen in the figure 3.11, light does not fully propagate through the taper. This can be due to insufficient taper angle or taper length. Now, we try to simulate the maximum possible length of the taper that can be used in our case, 10 mm. The dimensions of the die that the waveguides are fabricated in is 10 mm x 10 mm. The device needs to be confined with in the die and cannot extend into the next die .Due to this a maximum value of 10 mm is set. The simulations for the same are shown in figure 3.12.

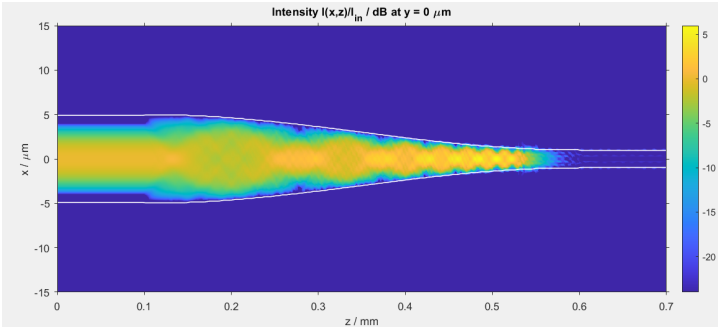


Figure 3.13: BeamLab simulation of a 10 um to 2 um taper waveguide with taper length 500 um

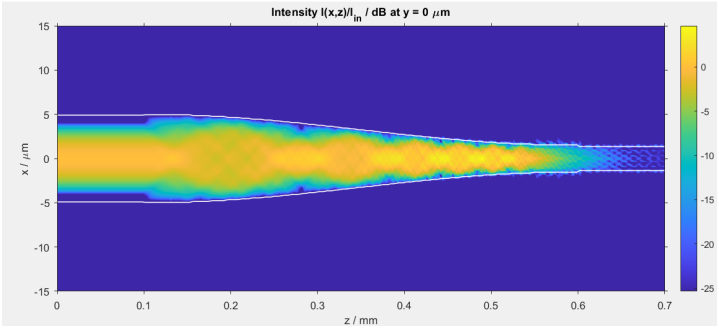


Figure 3.14: BeamLab simulation of a 10 um to 3 um taper waveguide with taper length 500 um

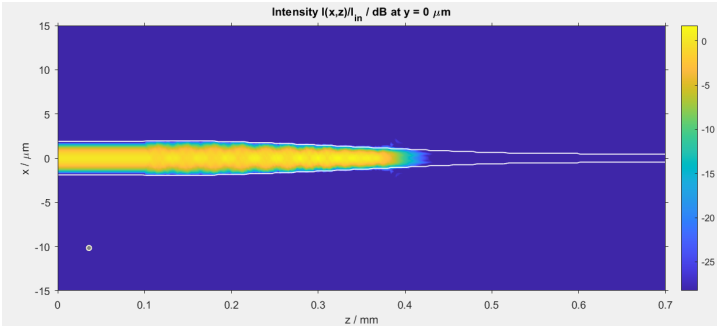


Figure 3.15: BeamLab simulation of a 4um to 1um taper waveguide with taper length 500 um

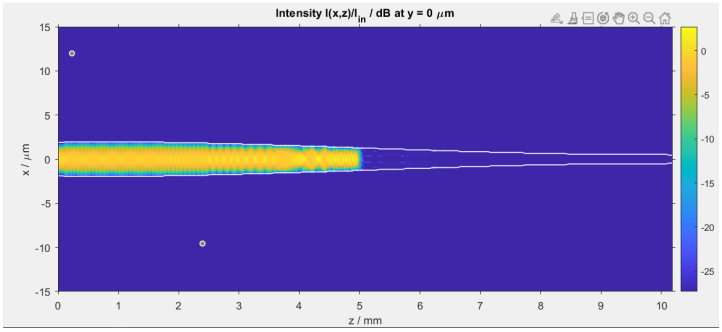


Figure 3.16: BeamLab simulation of a 4um to 1um taper waveguide with taper length 10mm

The simulations from figure 3.11 tell that even a taper length of 10 mm isnt enough for successful propagation of light from the source into the waveguide. This suggests that we either have an issue with the propagation of light, or an issue with the software, as tests done in [49] suggests the angle/taper length calculated using the equation 3.1 does indeed work for proper transmission. But for now we assume that there is an issue with the light propagation and try to implement other methods to achieve successful light propagation from the source to the waveguide. One such method that I designed which might result in successful transmission of light from the source to the waveguide is using a step configuration. The way the step configuration is designed is that, first light is propagated through a 10 um to 4um taper followed by 4 um to 3 um taper and 3 um to 2 um taper and finally end the step taper with a 2 um to 1 um taper. This configuration makes sure that light propagating through the taper doesnt experience a single harsh step-down from 10 um to 1 um, but rather faces multiple smaller step-downs. The taper lengths in all of the above mentioned tapers is 500 um and sections of 100 um of rectangular waveguide after each of the tapers is used. We arrived at this design due to the fact that the tapers for 10 um to 4 um, 4 um to 3 um, 3 um to 2 um, etc when simulated individually result in successful transmission of light as seen in the figure 3.17 to 3.20, and because the propagation of light from 10 um to 2 um, 10 um to 3 um and 4 um to 1 um tapers is unsuccessful as seen in figures 3.13 to 3.16.

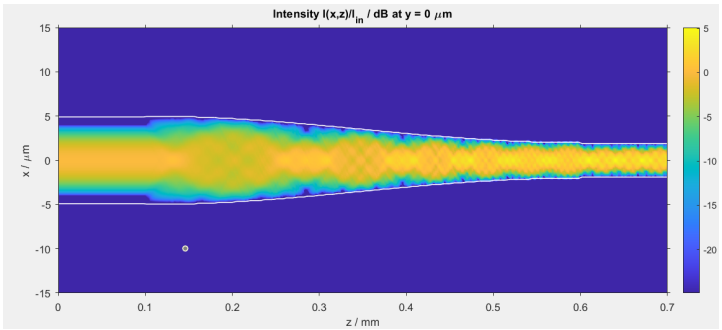


Figure 3.17: BeamLab simulation of a 10 um to 4 um taper waveguide with taper length 500 um

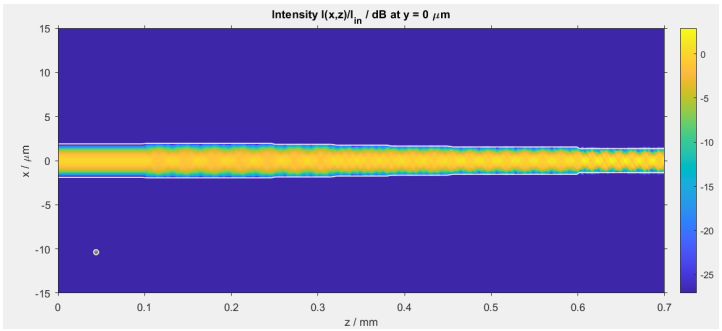


Figure 3.18: BeamLab simulation of a 4 um to 3 um taper waveguide with taper length 500 um

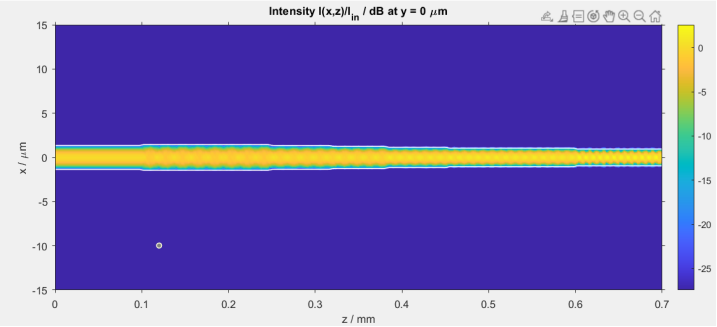


Figure 3.19: BeamLab simulation of a 3 um to 2 um taper waveguide with taper length 500 um

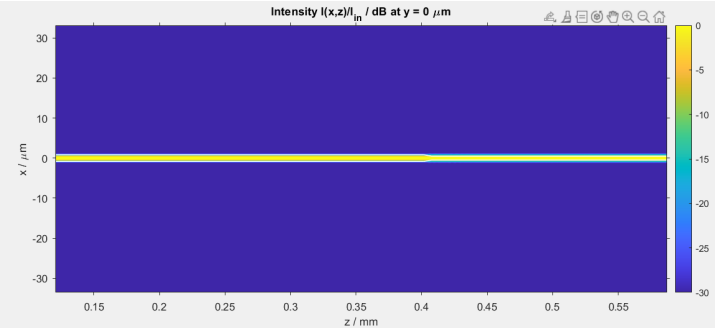


Figure 3.20: BeamLab simulation of a 2 um to 1 um taper waveguide with taper length 500 um

The final design simulation for the step configuration achieved by combining all the tapers simulated above is shown in figure 3.21. Unfortunately, as seen in the figure, the step configuration doesn't result in successful transmission of light.

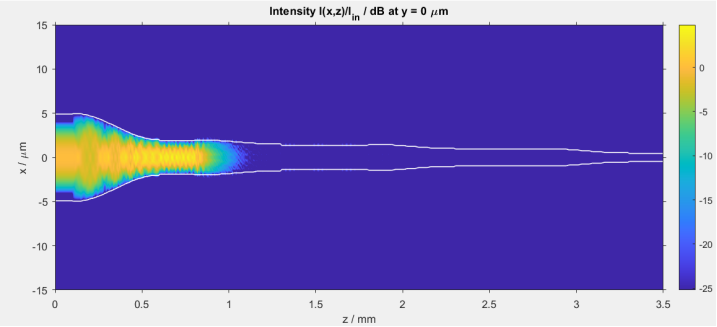


Figure 3.21: BeamLab simulation of a Step taper waveguide

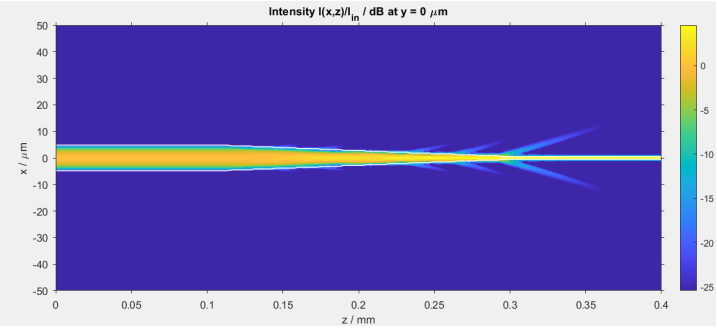


Figure 3.22: Working BeamLab simulation of a 10 um to 1 um taper waveguide with taper length 500 um

However, upon further tinkering with the software/ MATLAB code, changing the number of grid points in which the result is plotted, from [30 30] to [50 50], shows successful transmission of light when 10 um to 4um taper with a taper length of 500 um as shown in the figure 3.22. The reason for this is however unknown. Also, taking the results from the simulations above into consideration, it can be seen that there are some defects in the software. Therefore, due to the unreliability of the software, the simulation results can't be taken as a concrete simulation result when designing the final taper. Which is why Dr. Gregory Pandraud, an expert in waveguide optics, was consulted regarding the taper angle/taper length and based on his experience, he suggested using a taper angle <0.1 degrees, as anything above that would be too harsh of an angle for light transmission. Using this taper angle, a taper length of 2.57 mm is calculated. Rounding it up to prevent irregularities, we decided to use a taper length of 2.6 mm for our devices.

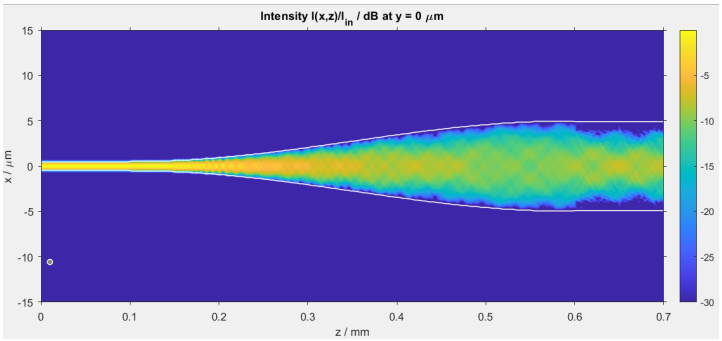


Figure 3.23: BeamLab simulation of a 1 um to 10 um taper waveguide with taper length 500 um

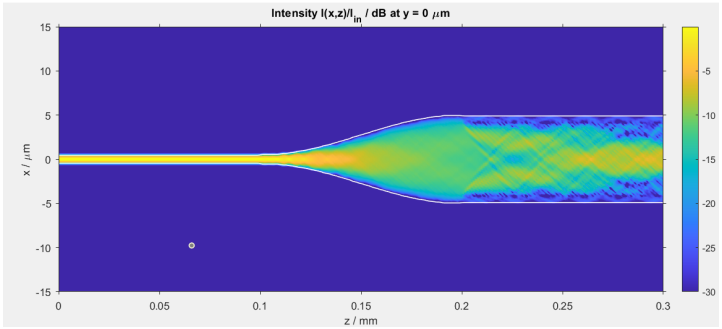


Figure 3.24: BeamLab simulation of a 1 um to 10 um taper waveguide with taper length 100 um

All the information above is for the taper at the source side of the waveguide. For the taper on the receiver side however, taper angle doesn't play as big a role as it does for the taper at the source side as the angle of reflection for the light propagating through the waveguide stays greater than the critical angle, which results in uninterrupted TIR and hence lossless transmission. We use a taper length of 300 um to make more space in the die for other components, and the simulation for this is shown in the figure 3.23 and 3.24.

3.4. Simulation of the extensions for metal contacts

Since we are fabricating an optical modulator, the Silicon waveguide and the graphene need to be contacted using metals so that a voltage biasing can be applied to the device. However, if we contact the waveguide on the path of light as shown in the figure , then this might result in obstruction of the path or might even cause losses which might result in irregular measurements at the source. Hence, we need to extend a part of the waveguide as shown in figure 3.25, for contacting purposes. To, check whether these extensions affect the propagation of light in the waveguide, the said extension is simulated in BeamLab which is seen in figure .

From the simulation, it can be seen that the said extension does not affect the propagation of light through the waveguide. Therefore, this structure can be used for contacting the waveguides in our devices.

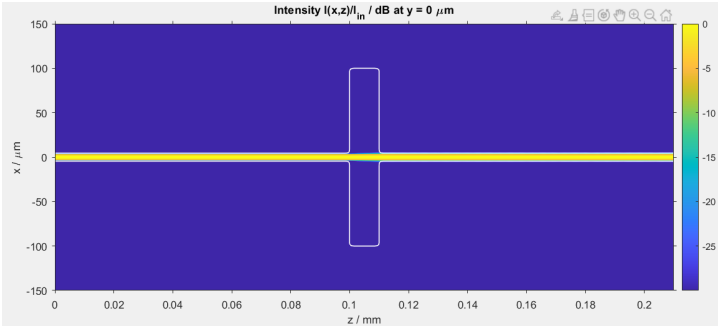


Figure 3.25: BeamLab simulation of a Metal Extensions

3.5. Summary of the Designs

Now to summarize this chapter, we first looked into the simulations done for varying widths of the waveguide in both BeamLab and COMSOL. Upon analysing the results by taking the set minimum required E-field intensity at the oxide-air interface into consideration, a range of 1 um to 4 um was selected for fabrication. Similarly, a cladding thickness of 20 nm was selected for fabrication.

Then we calculated and simulated different taper structures and taper lengths. And a taper length of 2.6 mm was selected for fabrication.

Lastly, we looked into the working simulations of the actual waveguide configuration and also simulated the extensions for metal contacts.

4

Device Fabrication

This chapter deals with the information related to the fabrication of devices, ranging from the process flow used for fabrication, brief explanation of a few sub-processes and the difficulties faced during the actual fabrication of the devices.

Firstly, we look into the mask that we designed, which was used for the fabrication of optical modulators.

Then, we discuss process flows for the fabrication of the Hall devices and the optical modulator are briefly explained. The process flow includes steps like oxidation, lithography, metallization, etc. We also briefly look into the different methods used for each of the step and the various components/techniques for different process steps.

Thirdly, we briefly discuss some electronic test structures included in the optical modulator mask, that would be used to test different materials, structures and properties in the die.

Lastly, we look into some difficulties faced during the fabrication process.

4.1. Designing the Mask to be used in the Lithography Process Steps

Lithography is a really important sub-process in the process flow for fabricating devices. Lithography is used prior to etching or deposition steps, so that the desired patterns are etched or deposited. As seen in figure 4.3 in the electrical components process flow and 4.4 in the Optical Modulator process flow, lithography process is used multiple times for patterning an metallization. The overview of a lithography process is given below.

- Firstly, Photo-resist is coated on the substrate.
- Followed by exposing a pattern onto the photo-resist through masks using a Stepper.
- Finally, the substrate is developed to finish making the patterns.

In a device fabrication process flow there are multiple lithography steps as it is not possible to make parts like the different structures, interconnects, etc. at the same time. Each type of pattern or structure need their own individual mask. The masks required to fabricate the devices required to test the electrical properties are readily available in the EKL lab. However, the masks required for the Optical Modulator need to be specifically designed according to the specifications that have been determined through the simulations done in chapter 3. The Mask design of the final layout of the die is shown in figure 4.1 and a closeup showing the structure of the optical modulator is shown in the figure 4.2.

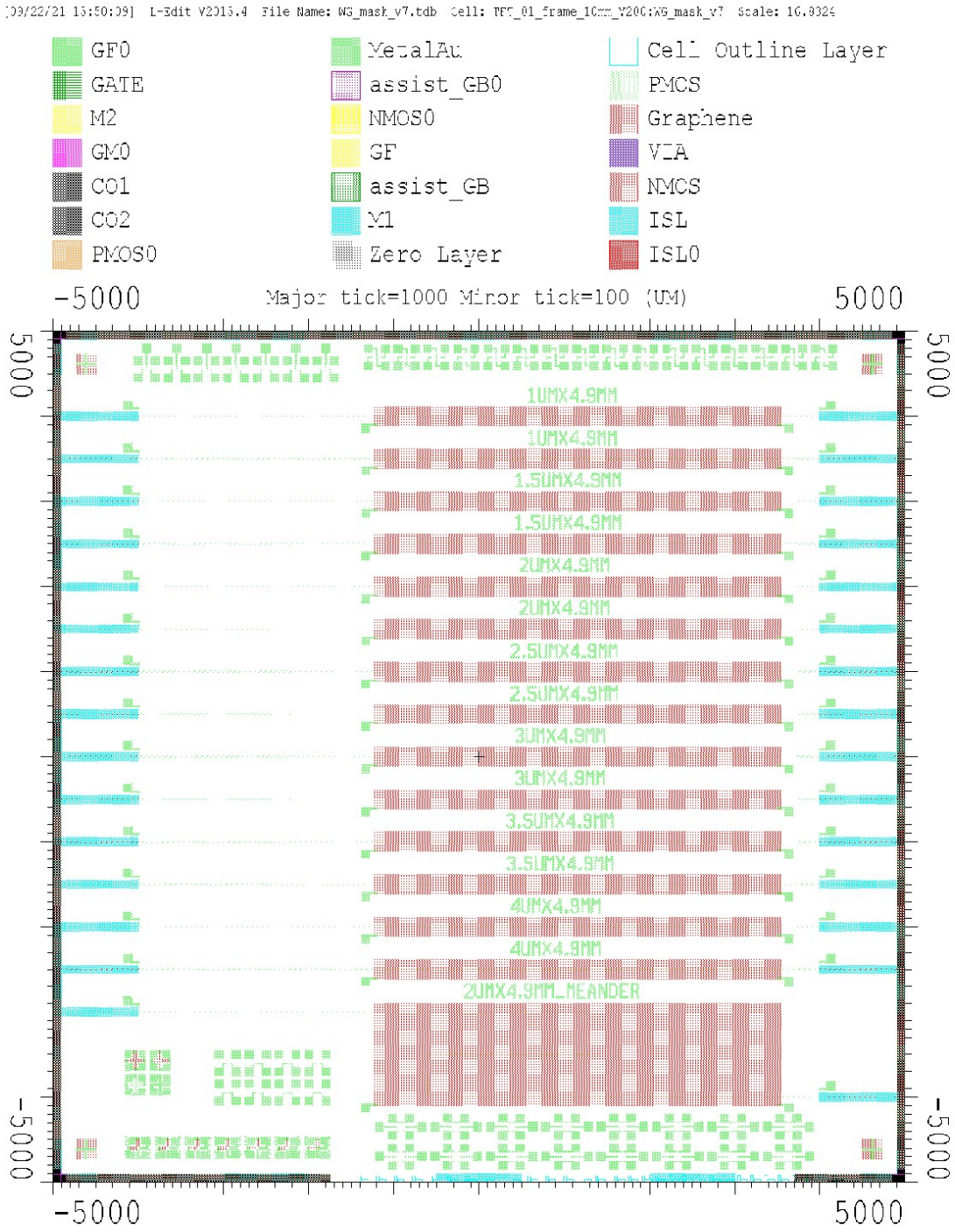


Figure 4.1: Mask designed for the fabrication of Optical Modulators

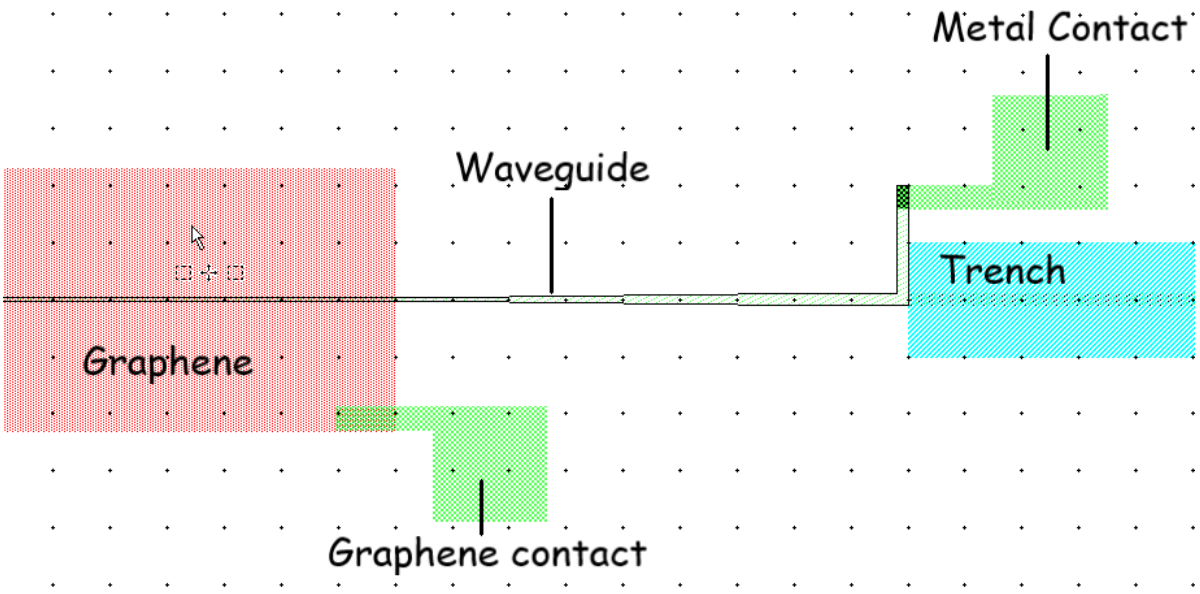


Figure 4.2: Closeup of the mask showing the structure of the Optical Modulator

Components in the mask and their descriptions:

- Silicon waveguides with widths ranging from 1um to 4um and an addition meander waveguide with width 1um. Different waveguide widths are implemented to compare results of the modulation for differing widths.
- Waveguide tapers with taper length 2.6 mm that gives a taper angle of ~0.1 ° on the source side and tapers with taper length 300um and taper angle of ~1 ° on the receiver side.
- Monolayer graphene strips on top of the waveguides that are used for the modulation.
- Contact openings for contacting the Silicon waveguide.
- Metal contact pads for contacting devices.
- Grooves on the sides of the side at the source and receiver sides to make it easier to place and couple the source and receiver optical fibers with the waveguides.
- Grooves on the perimeter of the die to make it easier for the dicing of the wafer.
- Some Electrical devices and test structures such as Hall bars, Hall Elements, Van der Pauw (vdp) structures, etc. are also included. The hall bars and hall elements are used to mimic and test the biasing of the graphene. And the vdp structures are used to measure the resistances of different materials on the wafer such as the silicon substrate, graphene and the interconnects.

The whole mask layout is then further divided into individual masks so that they can be used in their particular steps

4.2. Process flows for device fabrication

The fabrication of devices on wafers, be it Silicon wafers or Silicon-on-oxide wafers is a complicated process and involves several processing steps. The process flow for the Electrical components is shown in figure 4.3 and the process flow for the Optical Modulator is shown in figure 4.4.

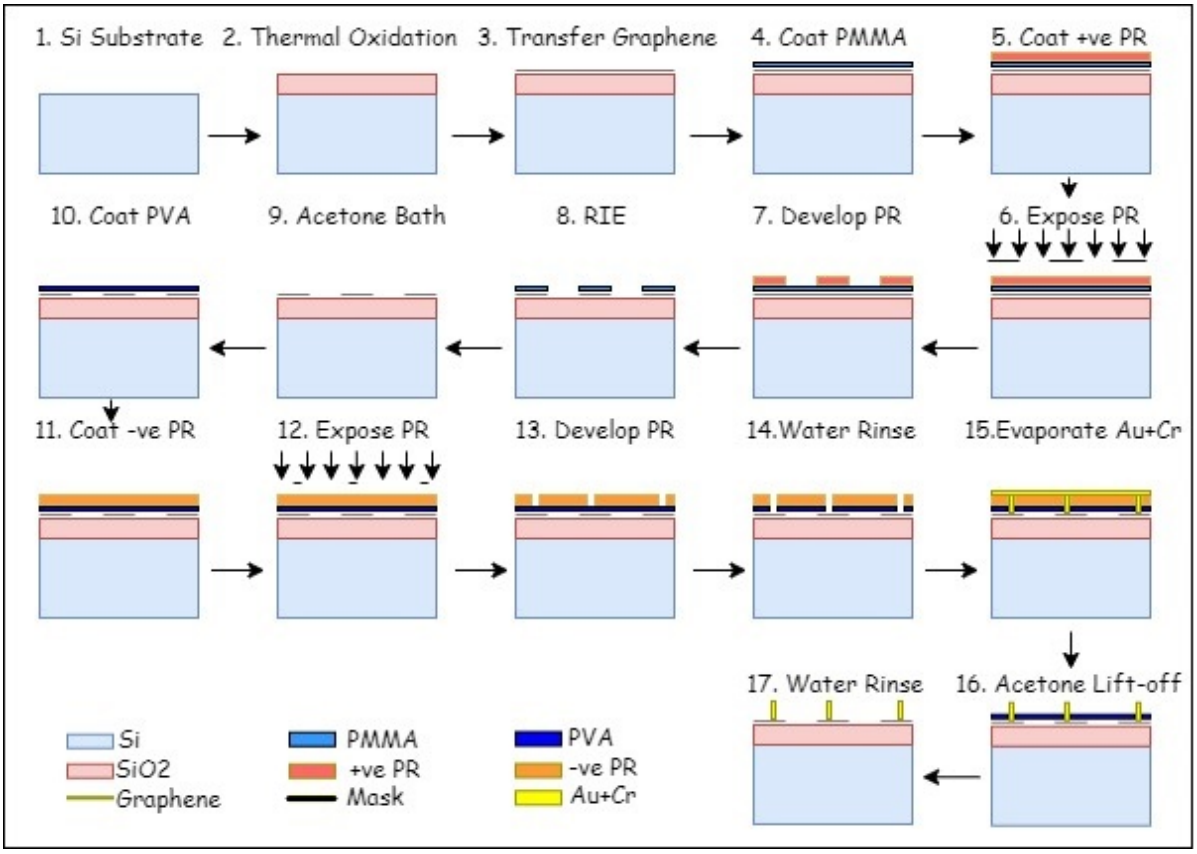


Figure 4.3: Process flow for fabricating Hall devices

A brief explanation of the process flow for the fabrication of Hall devices is given below:

- We start with a Silicon substrate wafer (p-type doped with Boron) and oxidize the substrate for about 285nm thick Silicon oxide using thermal oxidation. The type of oxidation done is dry oxidation, whether the substrate is oxidized without the presence of water. The time for oxidation is calculated using Deal-Grove model, and for 285nm the oxidation time is calculated as 4hours 32 minutes at 1100 $^{\circ}$C. The value of 285nm is selected as it is easiest to see the near transparent graphene for this said thickness.
- Now, the mono-layer graphene is transferred onto the substrate by ANL.
- Then the polymer PMMA is coated as a polymer support layer at 1k rpm for 1 minute then baked at 130 $^{\circ}$C for 5 minutes. Photo-resist degrades the quality of graphene when it comes in contact with it and the support layer protects the graphene films from the photo-resist but preventing contact between them.
- Then a positive photo resist called SPR3012 is coated for about 1.4 um thick, exposed with the graphene pattern masks with an energy of 140mJ/cm^2 and then developed.
- After the required patterns are developed, graphene is etched away using oxygen plasma in Reactive Ion Etching (RIE) from the areas where the PR was not exposed forming the required graphene patterns.
- Then the wafer is put into an acetone bath at 50 $^{\circ}$C for 10 minutes, to dissolve PMMA and the photo-resist, leaving just the patterned graphene on the oxidized wafer.
- Now, another polymer called PVA is coated onto the wafer at 1k rpm for 1 minute then baked at 130 $^{\circ}$C for 5 minutes. PVA is coated for the same reason as PMMA was coated in one of the previous steps. Why PVA is used instead of PMMA in this step, is discussed in section 4.2.
- A negative photo resist called AZ NLOF 2020 is then coated for about 3.5 um thick, exposed with the metal contacts mask with an energy of 55mJ/cm^2 and then developed.

- Then Gold (100 nm thick) is evaporated onto the wafer using Chromium (10 nm thick) as the adhesion layer, for the metal contacts.
- Finally, the wafer is submerged in an acetone bath at 50 $^{\circ}$C to lift-off the excess metal, leaving just the metal contacts. This process also dissolves the photo-resist used for patterning the metal contacts.
- And then the wafer is cleaned using IPA and water at 80 $^{\circ}$C to dissolve and remove the PVA, leaving the devices without any unwanted residues.

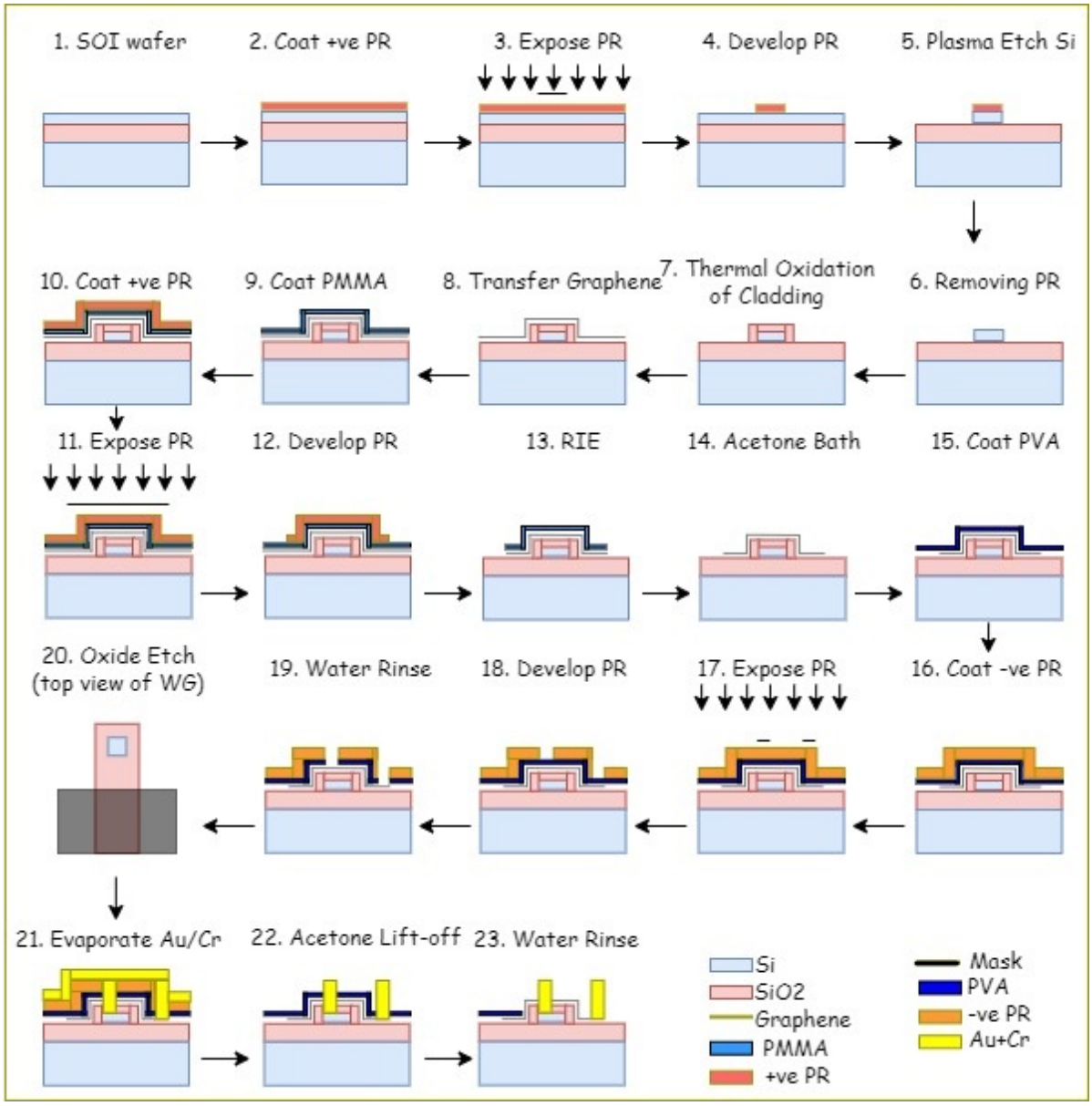


Figure 4.4: Process flow for fabricating the Optical Modulator

Similarly, a brief explanation of the process flow for the fabrication of the optical modulator is given below:

- We start with a Silicon-on-Insulator (SOI) substrate wafer. The structure of the SOI wafer is as follows, Silicon substrate on the bottom, 400 nm thick Silicon Oxide on top of it and 340 nm thick Silicon on top of the oxide.
- A +ve photo resist called AZ3027 is coated for a thickness of 3.1 um, exposed with the waveguide pattern masks with exposure energy 240 mJ/cm^2 and then developed.

- Then Silicon is etched away (about 340 nm) using Hydrogen Bromide and Chlorine gases with Plasma etching, from the area where the PR was not exposed forming the required waveguides.
- The left-over PR is then removed using hot acetone (50°C) and the wafer is then cleaned with 99% HNO3 to remove any other residues.
- (optional)Now the wafer is coated with a positive photo-resist called 12XT for a thickness of 8 um, exposed with trenches mask with an exposure energy of 140 mJ/cm^2 and then developed.
- (optional) The trenches are then etched (about 65 um) into the wafer using plasma etching. The top Silicon substrate (340 nm) is etched with RIE using chlorine and hydrogen bromide. Then bulk oxide (400 nm) is etched using plasma etching using a plasma mitxure of CF4 and CHF3 gases. And finally, the bottom Silicon substrate (about 64um) is etched with Deep reactive ion etching (DRIE) method using SF6 and the teflon coating deposited in between cycles is removed with oxygen plasma.
- Now, the silicon substrate is oxidized for about 20 nm using thermal oxidation, to make the cladding layer and the wafer is later put into hot acetone to remove the remaining photo-resist followed by the standard cleaning in 99% HNO3 and boiling 66%HNO3 baths. The oxidation is done using the dry oxidation method at 800 $^\circ$C for an oxidation time of 35 minutes.
- mono-layer graphene is then transferred onto the top Silicon substrate by ANL.
- Then the polymer PMMA is coated as a polymer support layer at 1k rpm for 1 minute then baked at 130 $^\circ$C for 5 minutes which results in the polymer layer being a few hundreds of nm thick. As mentioned in the Hall bars process flow, PMMA protects the graphene from the photo-resist, which is to be coated in the next step.
- A positive photo resist called SPR3012 is coated for a thickness of 1.4 um, exposed with the graphene pattern masks with an exposure energy of 140 mJ/cm^2 and then developed.
- After the required patterns are developed, graphene is etched away using RIE from the unexposed areas forming the required graphene patterns.
- Then the wafer is put into an acetone bath, to dissolve PMMA and the photo-resist, leaving just the patterned graphene on the oxidized wafer.
- Now, PVA is coated onto the wafer at 1k rpm for 1 minute then baked at 130 $^\circ$C for 5 minutes, to protect the wafer from the photo-resist. This results in the polymer layer being a few hundreds of nm thick.
- A negative photo resist called AZ NLOF 2020 is then coated for a thickness of 3.1 um, exposed with the metal contacts mask with an exposure energy of 55 mJ/cm^2 and then developed.
- Now, the oxide present at the metal contact openings for contacting the top silicon substrate is etched using BHF (1:7) solution for 12 seconds (SiO2 etch rate of 1.3 nm/s), such that a good contact can be made with the said silicon substrate.
- Then Gold (100 nm thick) is evaporated onto the wafer using Chromium (10 nm thick) as the adhesion layer, for the metal contacts.
- Finally, the wafer is submerged in an acetone bath at 50 $^\circ$C to lift-off the excess metal, leaving just the metal contacts. This process also dissolves the photo-resist used for patterning the metal contacts.
- And then the wafer is cleaned using IPA and water at 80 $^\circ$C to dissolve and remove the PVA, leaving the devices without any unwanted residues.

As seen above there are multiple steps involved in the process flows for both the fabrication of the Hall devices and the optical modulators. And fabrication of these devices often includes a few hurdles. Some of these hurdles encountered are discussed in the next section.

Another thing that is observed in the process flows is that, different photo resists such as SPR3012, AZ3027, AZ NLOF 2020 and 12XT are used in different lithography steps. This is because the choosing of the required photo-resist depends on various reasons. Such as, whether a positive or a negative photo-resist is required

or what thickness of photo-resist is required (As different photo-resists have different viscosities, only a certain range of thickness' can be achieved with each of them). And based on our requirements, the suitable photo-resist is selected.

4.3. Electrical test devices included in the Optical Modulator mask

As seen in section 4.1, a few electrical devices were included in the mask designed for the fabrication of optical modulators. These devices include, Van der Pauw structures, top gated Hall bars, back gated hall bars, etc. These devices are briefly discussed in the subsections below.

4.3.1. Van der Pauw structures

Van der Pauw structures are used to measure the square resistance of different materials on the die and to check if they are conducting or not. The vdp structure in the mask is shown in the figure. 4.5.

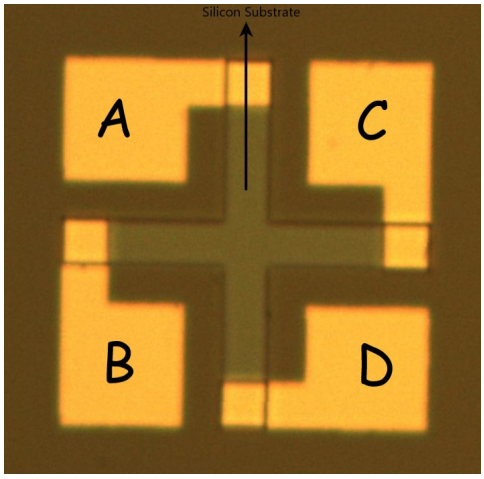


Figure 4.5: Van der Pauw Strcture that is measured

In the vdp structure, a current is applied from point A to B. Lets label this current as I_{AB}. The current is applied by setting A to a certain voltage (V_force) and B to ground. The applied current is calculated to be I_Sense. Then the voltage drop at point C and D is calculated as V_CD or V_diff. Now, using V_diff and I_sense, we calculate the square resistance as follows,

$$R_{AB,CD} = \frac{V_{diff}}{I_{sense}} \tag{4.1}$$

$$R_{square} = \frac{\pi}{ln2} R_{AB,CD} \tag{4.2}$$

The equation 4.2 is the resistance of a material for a single square. This can be multiplied by the number of squares in a structure, to calculate the resistance it.

4.3.2. Top gated Hall bars

Top gated hall bars are used to bias the graphene and measure/calculate parameters such as channel resistance, dirac point of the graphene, resistivity, etc. The top gated hall bars in our design with the points of contact during measurements is shown in figure 4.6 and its cross section is shown in the figure 4.7.

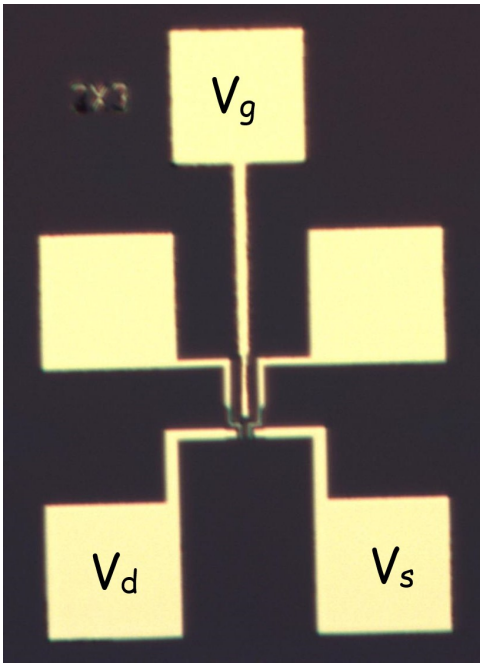


Figure 4.6: Graphene Hall bars with top gate.

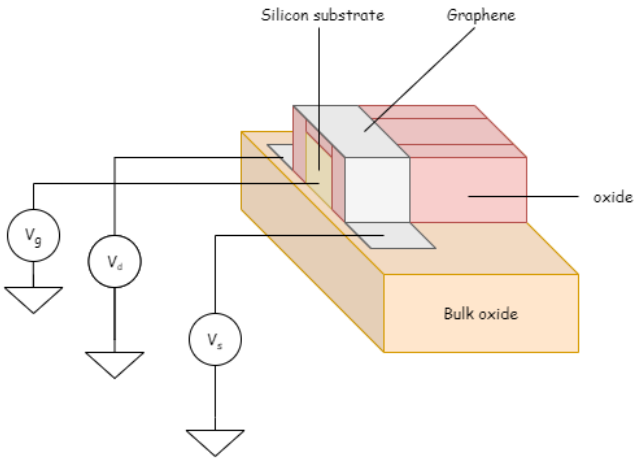


Figure 4.7: Cross section of the top gated graphene Hall bars

V_g here is the gate voltage, that is applied to the top silicon substrate. V_d and V_s are the drain and source voltages. Now, to find the dirac point of the graphene film, a constant current of voltage can be applied to the drain-source terminal and the gate voltage can be swept. From the I_d - V_g plot, the dirac voltage can be measured. Where dirac voltage is the point at which the dirac point is reached. Now, the voltage drop between V_h and V_l can be calculated and divided by the drain current to give the channel resistance. Then the resistivity can be calculated using the channel resistance.

4.3.3. Bottom gated Hall bars

Bottom gated hall bars have the same function that top gated Hall bars do. The only difference between them is where the gate voltage is applied. As the name says, bottom gated Hall bars are biased using the bottom silicon substrate. The steps to measure dirac voltage, channel resistance and resistivity is exactly the same as it is for top gated Hall bars. The designed device and their cross section is given below.

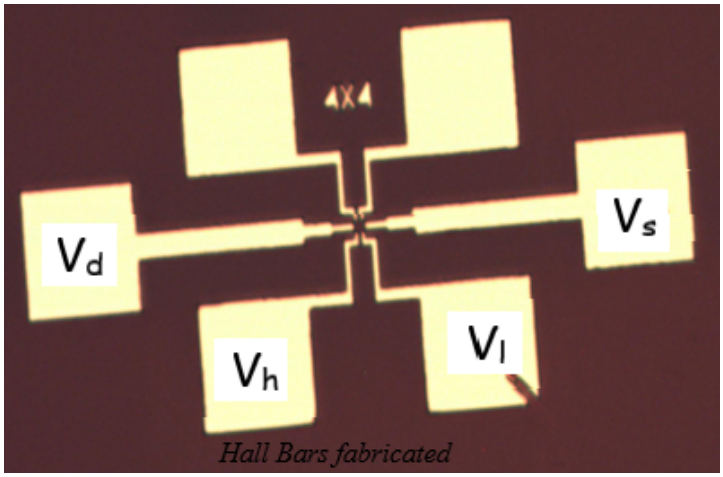


Figure 4.8: Graphene Hall bars with bottom gate.

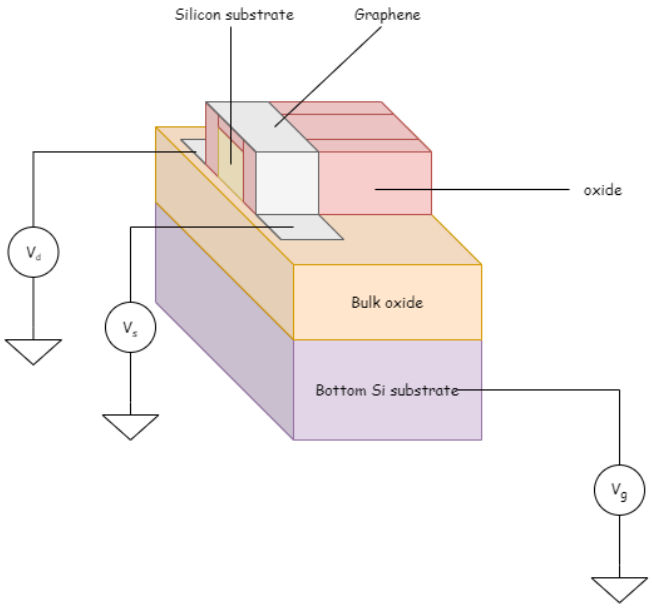


Figure 4.9: Cross section of the bottom gated graphene Hall bars

4.4. Hurdles encountered during fabrication

4.4.1. Choosing the right concentration of PVA between 10% by weigth and 20% by weight.

Poly-Vinyl Alcohol (PVA) is a polymer support layer used as an alternative for PMMA during the fabrication of both the Hall bars and Optical Modulators. PVA is coated (Step 10 in Hall bars and Step 15 in optical modulators fabrication) to protect the graphene film from the photo-resist when metal contacts are to be patterned, evaporated onto the wafer and then lift-off. One could say PMMA could do the same job of protecting the graphene films from the photo resist as it did in the previous lithography step. But during the metallization process, both the exposed PR and the polymer support layer, need to be removed at the metal contact openings, for a good contact. And to remove PMMA, acetone needs to be used. But using acetone to remove PMMA from the metal contact openings would also dissolve the PR, which would cause difficulties in patterning and lift-off, which also uses acetone. Which is why PVA is used as an alternative as it can be dissolved and removed using water before the metallization process, without affecting the PR patterns.

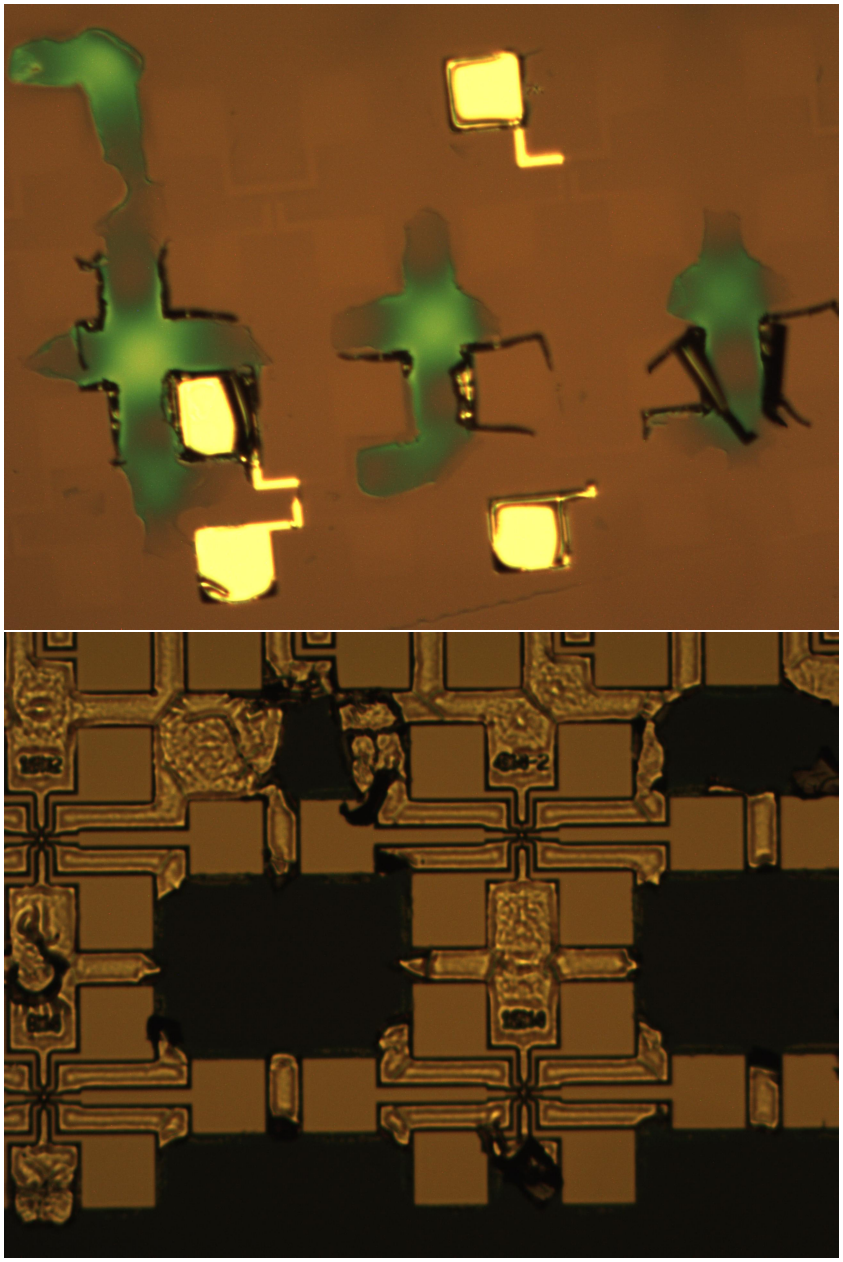


Figure 4.10: Unsatisfactory lift-off results when 20% PVA by weight is used as polymer support layer

The problem due to using PVA in the process flow is not with the polymer compound in itself, but the concentration of PVA solution used as the polymer support layer. Initially, a 20% by weight PVA solution was used as the polymer support layer. However, using this solution resulted in unsatisfactory lift-off results as seen in the figure 4.10. It is highly likely that the improper lift-off seen in the figure4.10 occurs due to not having the desired photo-resist profile. To better understand why the expected lift-off results weren't achieved the resist profile before the metallization process needs to be analyzed. The photoresist used in the lithography process in steps 11 and 16 in figures 4.3 and 4.4 is called AZ_NLOF_2020. It is a negative photo-resist, which means that the area of the resist that is exposed to light hardens and stays during the development process. Whereas, the unexposed area does not harden and is removed during the development process.

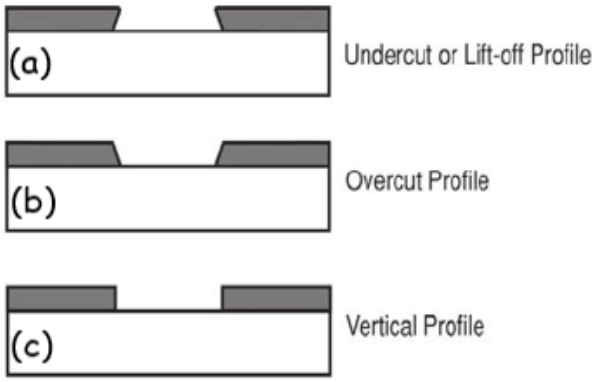


Figure 4.11: Different Photo-resist profiles that can be acheived [50]

There are different kind of resist profiles that can be achieved based on the resist and the exposure energy used. The different possible resist profiles and the desired resist profile for lift-off is shown in the figure 4.11. Since, we are using the NLOF photo resist, the acceptable exposure energy range lies between the range 40-75 mJ/cm^2 based on the datasheet of the PR. The energy range is decided based on the following requirements. To get an undercut profile, a lower energy range is needed, whereas a higher energy range is more likely to give an overcut or vertical profile. Also, the energy range used depends on the thickness of the PR to be exposed(3.1 um thick PR in our case) and the thickness of PVA underneath the PR, such that only the required amount of PR is exposed(Higher the energy, deeper the light penetrates into the PR, resulting in more defined/vertical structuers). And when this range is used, the profile (c) is expected from the figure 4.11. This said profile is called an undercut profile and having this profile makes it possible to do the lift-off process. Having an undercut profile prevents the side walls from being coated during the metallization process, and this in turn prevents cross-linking between structures. However, for vertical and overcut profiles, the sidewalls are also coated during the metallization process, which results in linking of the structures and leads to unsatisfactory lift-off results.

Initially, the energy used for exposure (50 mJ/cm^2) was suspected to be the cause for the improper lift-off due to it being insufficient to make the required profile. Therefore, we tried to check the resist profile when 20% by weight PVA solution is used as the polymer support layer, for exposure energies ranging from 40 to 75 mJ/cm^2. The SEM images of the profiles for different exposure energies is shown in the figure 4.12,4.13 and 4.14.

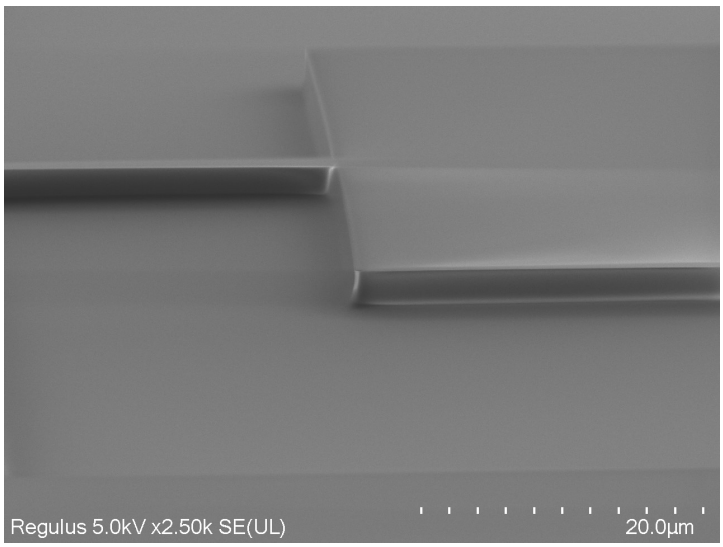


Figure 4.12: SEM image of the resist profile of NLOF PR for 40 mJ/cm^2 exposure energy with 20% PVA by weight as the polymer support layer

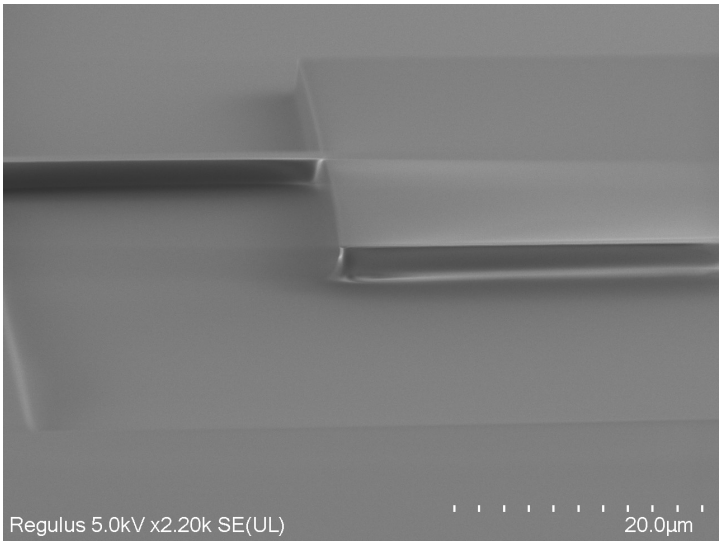


Figure 4.13: SEM image of the resist profile of NLOF PR for 50 mJ/cm^2 exposure energy with 20% PVA by weight as the polymer support layer

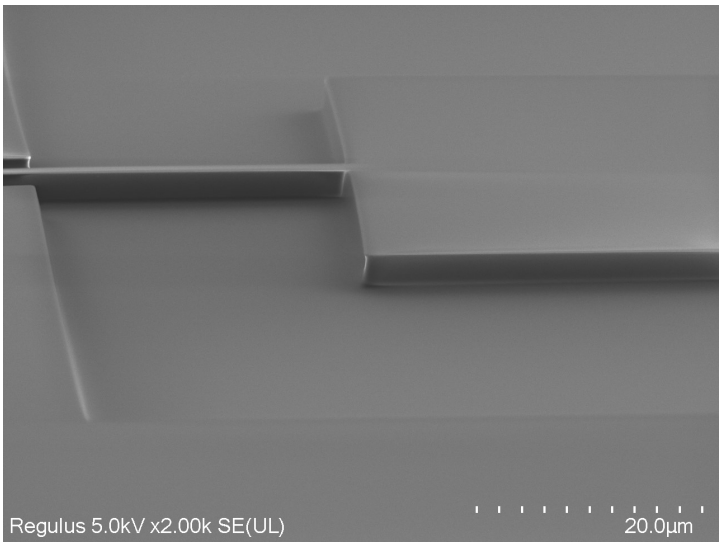


Figure 4.14: SEM image of the resist profile of NLOF PR for 75 mJ/cm^2 exposure energy with 20% PVA by weight as the polymer support layer

As seen in the figures, all of the exposure energies give more or less the same resist profile which is the vertical or over-cut profile and none of the exposure energies in the acceptable range give the desired undercut profile. This explains why unsatisfactory results for the lift-off process were achieved and also confirms that the exposure energy is not the culprit for not achieving the desired resist profile, but that PVA that is underneath the PR is the reason. It is suspected that this can be due to the difference in thickness' of the PVA support layer. If the same spinning speeds are used during the coating, 20% PVA would result in a higher thickness due to its higher viscosity, wheras the 10% PVA would result in a lower thickness due to its lower viscosity. The thickness of the polymer layer matters because, when the PR is being exposed with the mask, the light first goes through the PR, then through the PVA layer, then through the oxide of the wafer reflects back and goes through the PVA and PR again, to finally form the pattern. So, a change in thickness of the PVA, would probably need different exposure settings or use different spin speeds to get the same results as the 10% PVA does.

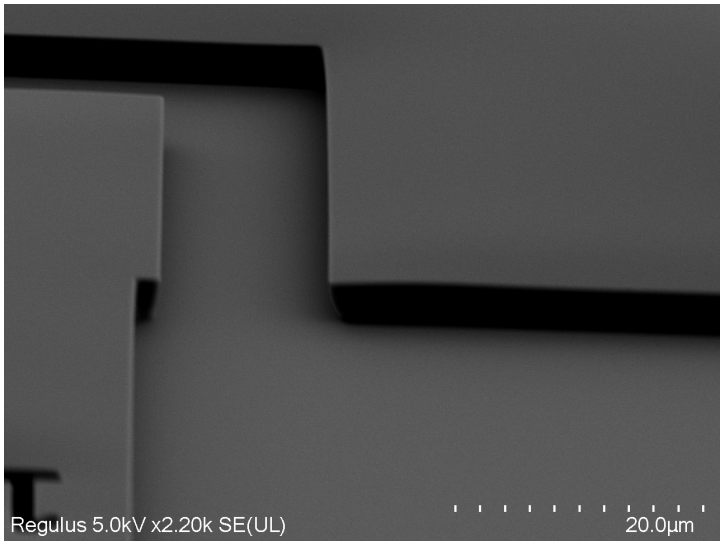


Figure 4.15: SEM image of the resist profile of NLOF PR for 40 mJ/cm^2 exposure energy with 10% PVA by weight as the polymer support layer

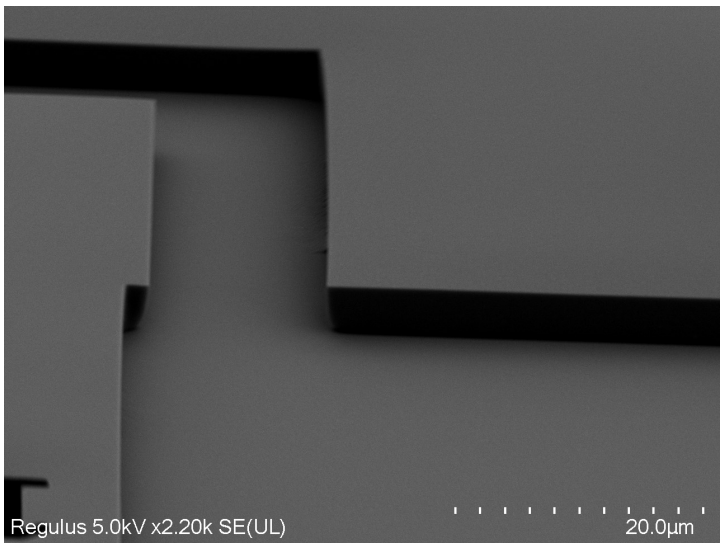


Figure 4.16: SEM image of the resist profile of NLOF PR for 50 mJ/cm^2 exposure energy with 10% PVA by weight as the polymer support layer

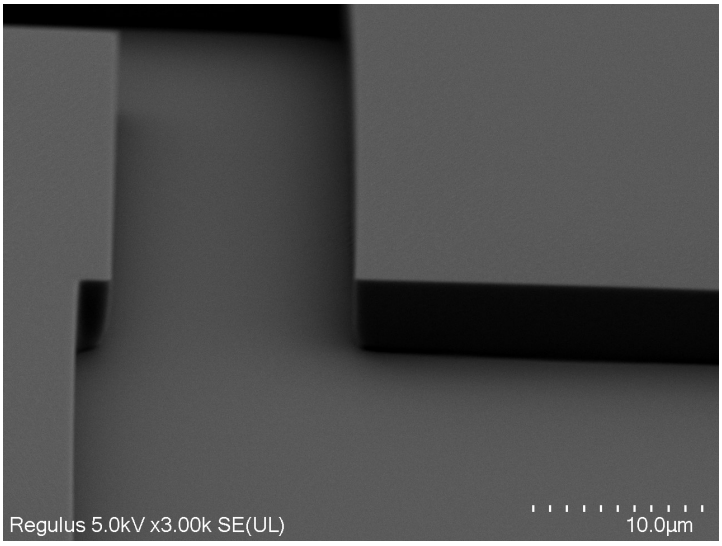


Figure 4.17: SEM image of the resist profile of NLOF PR for 75 mJ/cm^2 exposure energy with 10% PVA by weight as the polymer support layer

Now, 10% PVA by weight solution is used as the polymer support layer instead of 20% by weight PVA solution. The 10% concentration was selected based on the documentation provided by ANL. The same coating speed used for 20% PVA (1krpm for 1 minute) is also used for 10% PVA, which would result in a samller thickness due to its lower viscosity. The resist profile pertaining to 10% by weight PVA is shown in figure 4.15,4.16 and 4.17 for exposure energies ranging from 40 to 75mJ/cm^2. From the figures, we can see that the expected undercut is attained after the photoresist development when 10% PVA is used, the best being around 45-55 mJ/cm^2 exposure energy. This hints that more satisfactory lift-off result could be achieved if 10% PVA is used. The wafer now goes through the metallization and the lift-off process and the results are shown in figure 4.19. It can clearly be seen that, much better lift-off has occurred when compared to 20% PVA by weight. Hence, we decide to go forward with using 10% PVA solution for our processing based on the experimental results.

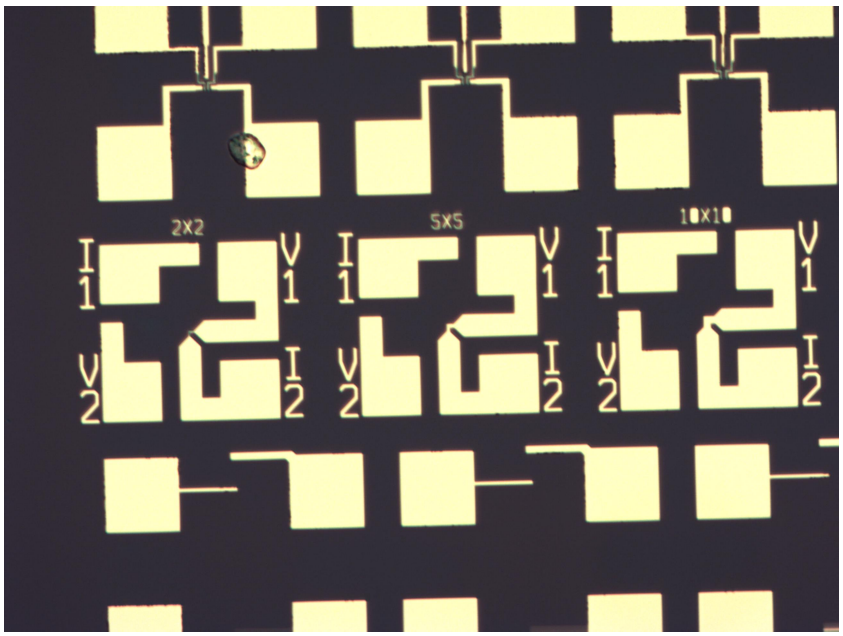


Figure 4.18: Lift-off results when 10% PVA by weight is used as the polymer support layer

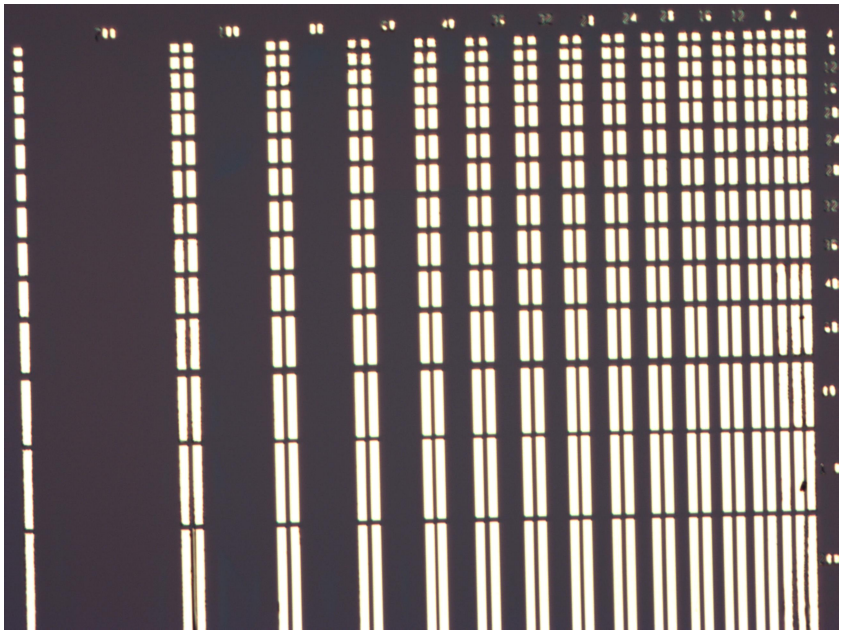


Figure 4.19: Lift-off results when 10% PVA by weight is used as the polymer support layer

4.4.2. Delamination of graphene after etching contact openings in BHF(1:7)

During the fabrication of the optical modulators, one of the processing steps involves etching the cladding layer or the oxide in the contact openings completely(as seen in step 20 in 4.4), so that the silicon waveguide underneath the cladding is contacted properly. The contact to the silicon waveguide is crucial as the biasing of the graphene in the optical modulator is done relative to the bias applied to the waveguide. However, the same mask is used for contacting the waveguide and the graphene. So, when you etch the cladding to contact the silicon waveguide, the graphene and the bulk oxide underneath the graphene is also exposed to the etchant (1:7 BHF is the etchant we use for etching oxide), and too much etching of this bulk oxide can result in the graphene delaminating from the substrate which might lead to problems while contacting graphene. This again would pose problems when biasing the graphene in the optical modulator as there wouldn't be an effective contact to graphene.

If we consider the etch rate of Silicon dioxide with BHF (1:7) to be ~1.3 nm/s and a cladding thickness of ~20 nm. So, that would be an etch time of about 15 seconds plus a few seconds of over-etch to passivate the Silicon surface, to prevent the formation of native oxide if required, which would result in the etching of about a few 10s of nms of the bulk oxide underneath the graphene. This is a considerable amount of bulk oxide etched which might result in delamination of the graphene. There is also another variable that might play a huge role in the delamination, which is the adhesion of graphene onto the substrate it's transferred to. The adhesion of graphene is something that is completely unpredictable and it changes batch to batch or even for different patterned parts of the same film. If the graphene adheres well to the substrate, it is less susceptible to delaminate from the substrate as easily and scroll. The delamination is not just limited to the cladding oxide etching, but can also happen during any of the process steps in the process flow.

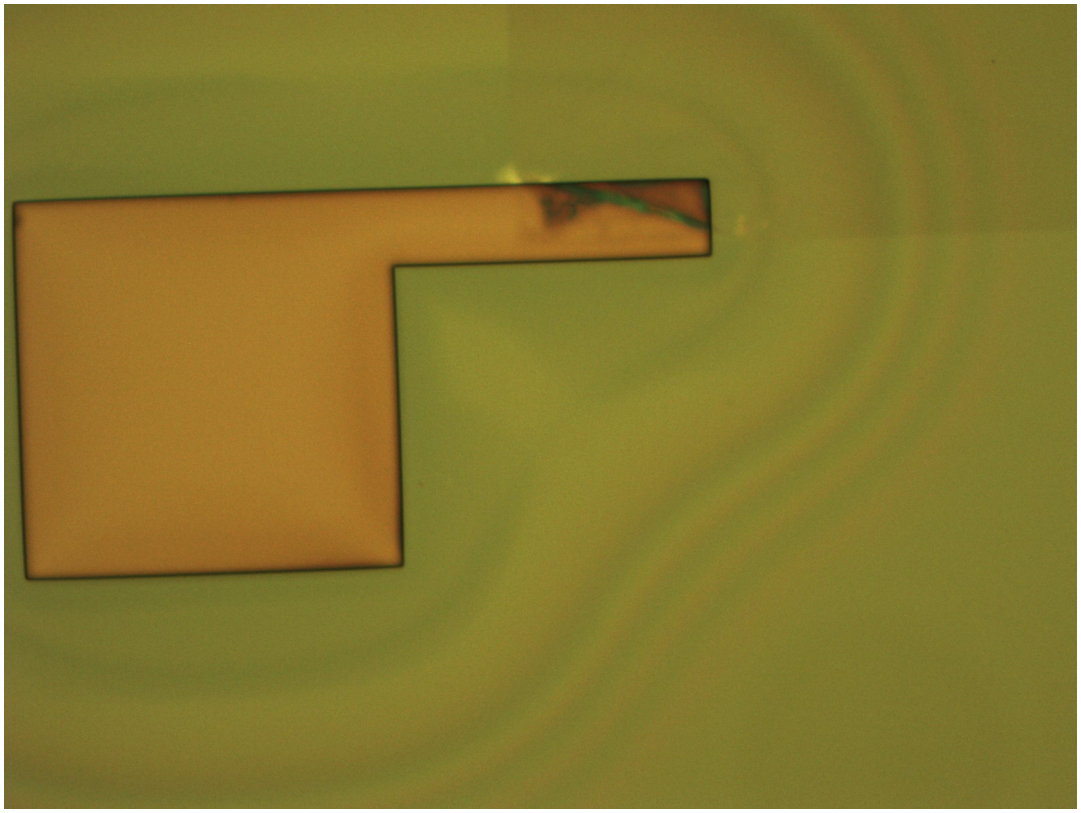


Figure 4.20: Fully delaminated graphene on an Silicon substrate at the contact openings after 18 seconds etch in BHF (1:7)

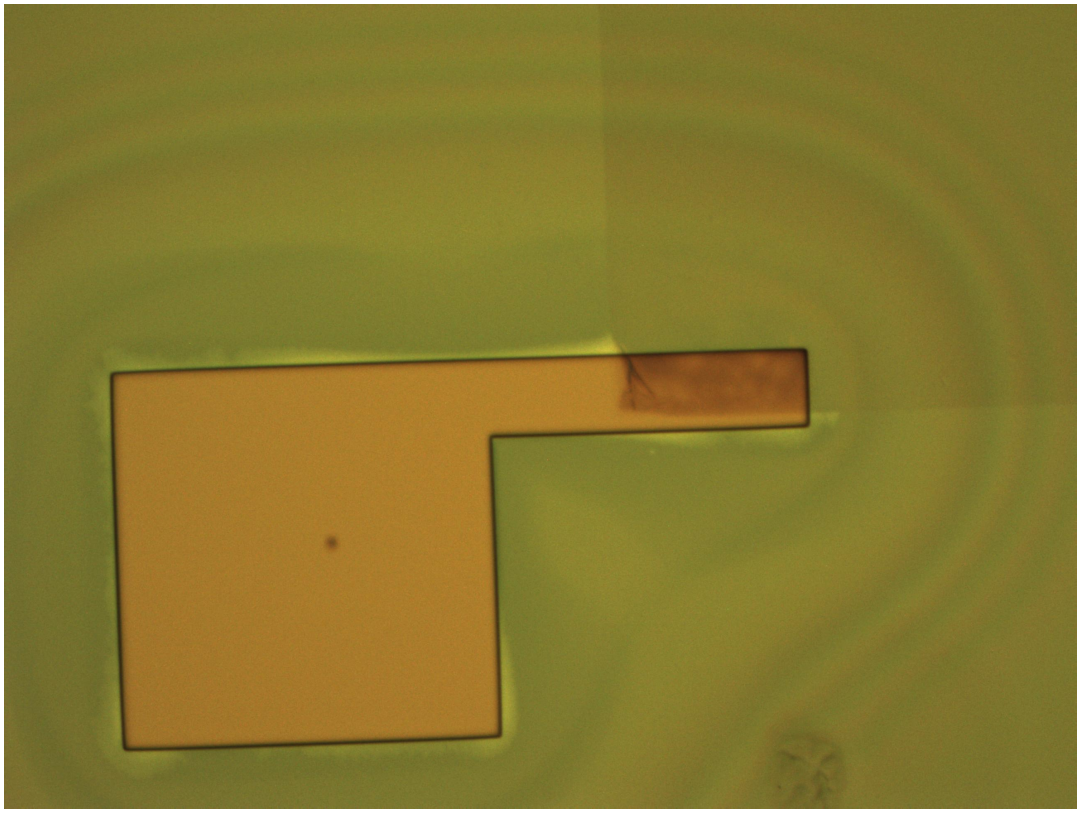


Figure 4.21: Partially delaminated graphene on an Silicon substrate at the contact openings after 18 seconds etch in BHF (1:7)

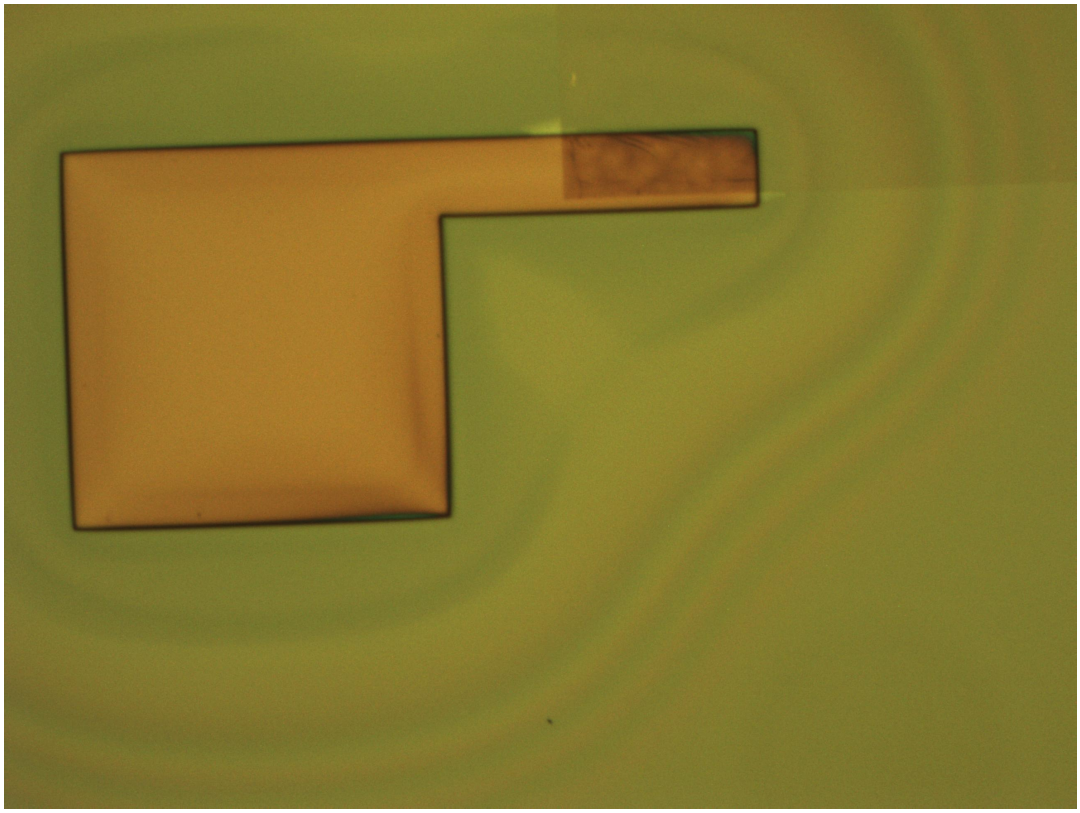


Figure 4.22: Fully intact graphene on an Silicon substrate at the contact openings after 18 seconds etch in BHF (1:7)

Figures 4.20, 4.21 and 4.22 show the graphene contact openings on the same silicon substrate test wafer that has been etched for 18 seconds in BHF (1:7) solution. Almost full delamination and scrolling of graphene is seen in figure.4.20. Figure.4.21 shows the graphene being slightly delaminated but still intact and figure.4.22 shows the graphene being fully intact. The delaminated graphene would probably result in a very bad contact to the graphene as a very small area in the contact opening would be contacted by the metal. The slightly delaminated graphene might still have a decent contact as majority of the graphene patch would still be contacted by the metal and the fully intact graphene pattern might have the best contact as the whole graphene patch would be in contact with the metal.

As mentioned previously, the adhesion of the graphene is quite random and to our convenience, graphene adhesion to the SOI substrate after 18 seconds of BHF (1:7) oxide etch, turned out to be more consistent (when compared to the results of the test wafer) and almost no delamination was observed in the metal contacts with majority of the graphene contact openings looking like in the picture seen in figure.4.23. The graphene film is in not quite clearly visible when compared to the graphene in figures. 4.20 to 4.22 due to the thickness of the oxide its sitting on being only 20 nm. Graphene is best visible when the oxide its sitting on is 285 nm thick or 60 nm thick.

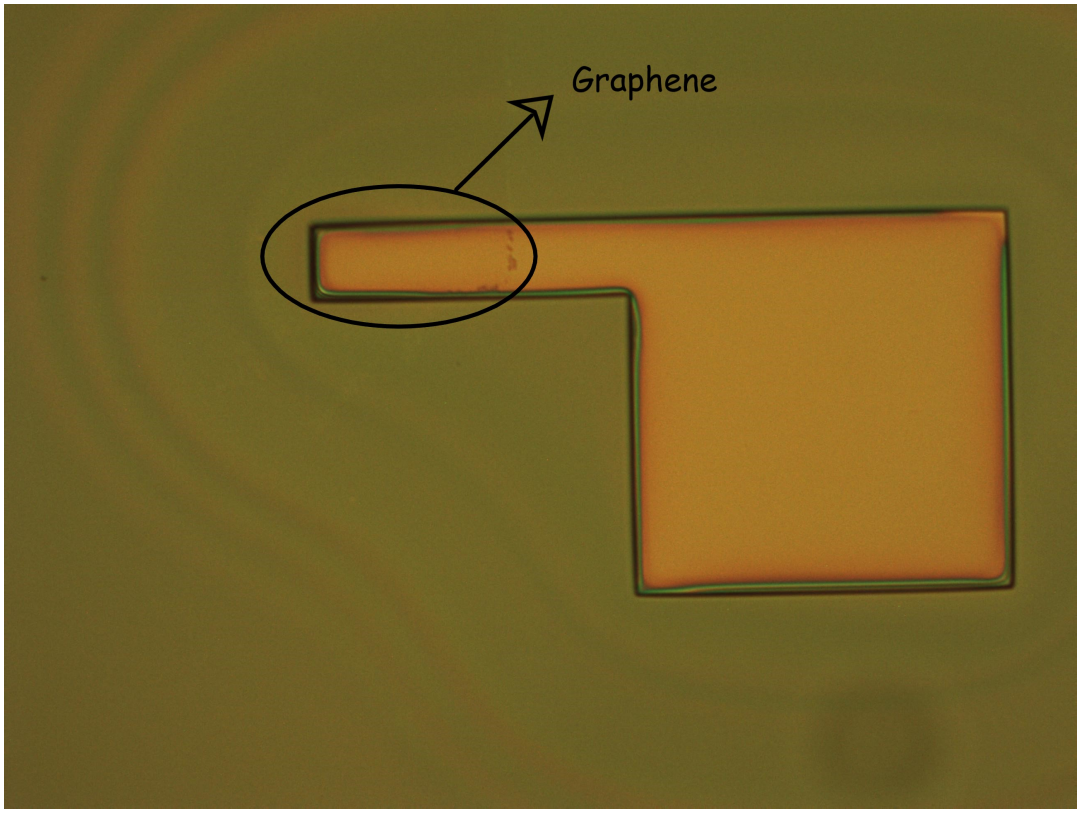


Figure 4.23: Fully intact graphene on an SOI substrate at the contact openings after 18 seconds etch in BHF (1:7)

4.4.3. Widening the Trenches to fit the optical fiber

During the fabrication of the optical modulator, an optional step was stated. This optional step was the etching of trenches into the wafer/die which help with aligning the waveguide and the core of the optical fibers that are used to input light into the waveguide at the input side and detect the light that propagated through the waveguide at the output side. How the alignment looks like is shown in the figure.4.24.

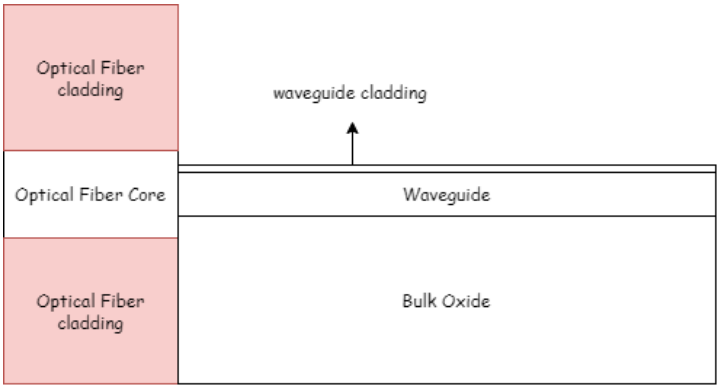


Figure 4.24: Aligning Optical fiber with the waveguide

The optical fiber that is available to us is the Thorlabs-P5-SMF28-FC-2 - SM Fiber Patch Cable. The same fiber is used for both transmission of light from the light source to the waveguide entrance and from the waveguide exit to the detector. It has a core diameter of 10 um and a cladding diameter of about 127 um. However, the mask designed for patterning the trenches that the fiber is gonna sit had a trench width of 100um and were designed for fibers whose diameters were <= 100 um. This would mean that the fibers available wouldn't fully fit in the trenches and hence cannot be properly aligned with the waveguide. Due to time constraints, designing and ordering a new mask with bigger trenches is not an option. So, we need to find a way to make

~127um wide trenches using the mask for 100 um wide trenches.

The solution to the above statement is rather simple. Since a positive photo resist (AZ_12XT) is used for patterning the trenches, the same resist can be exposed twice. Once, but shifting the mask by +15 um in the y direction and once by shifting the mask by -15 um in the y direction, adding a total of 30 um to the final width of the trench. The use of positive PR plays an important role here because, during the developement process of the PR, the part of the PR which is exposed by light is removed for positive PR. So even if part of the PR(about 70um wide) is exposed twice, it gets removed during the developement process. The theory behind double exposed PR pattern is shown in the figure 4.28.

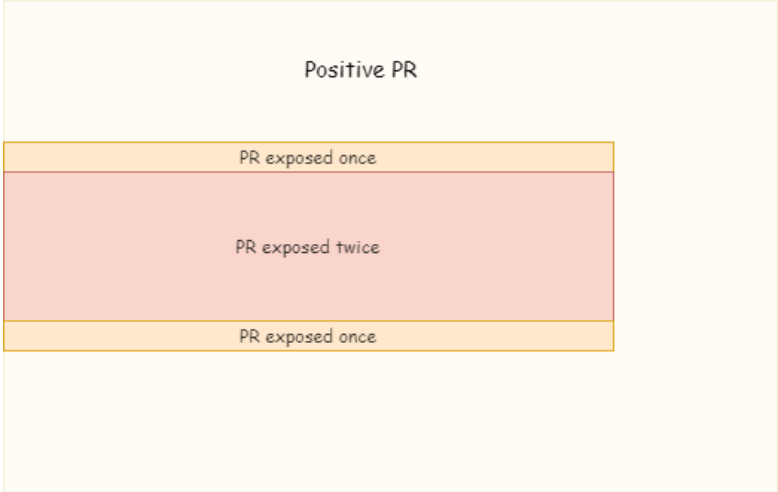


Figure 4.25: Photo resist exposed twice with shifted trench mask to form wider trenches on a test wafer

The above solution was tested using a test wafer. The patterns developed after exposing the PR with a +15 um and a -15 um shift is shown in the figure. 4.26. As, seen only a width of 120um is observed, instead of the expected 130 um. This difference of ~10um is probably due to the difference in focus of the lens in the stepper, while exposing the mask. To fix this difference of ~10um, a shift of +22 um and -22 um in the y-direction was used instead on the non-test SOI wafer which had the waveguides on it. The pattern developed and the width of the trenches after etching and removal of PR is seen in figures. and . As seen in the figures, the trench pattern developed is about 143 um wide and the trenches are about 144 um wide, which should comfortably fit the optical fibers in them.

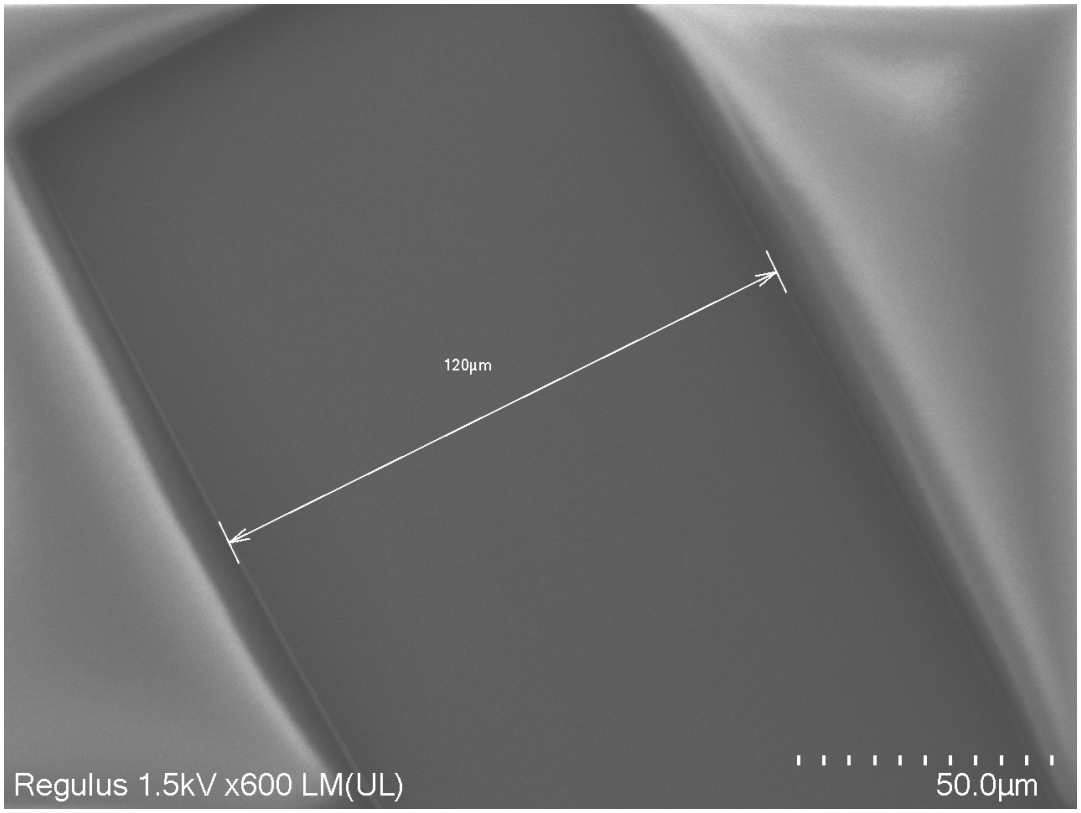


Figure 4.26: 120 um wide trench pattern on test wafer

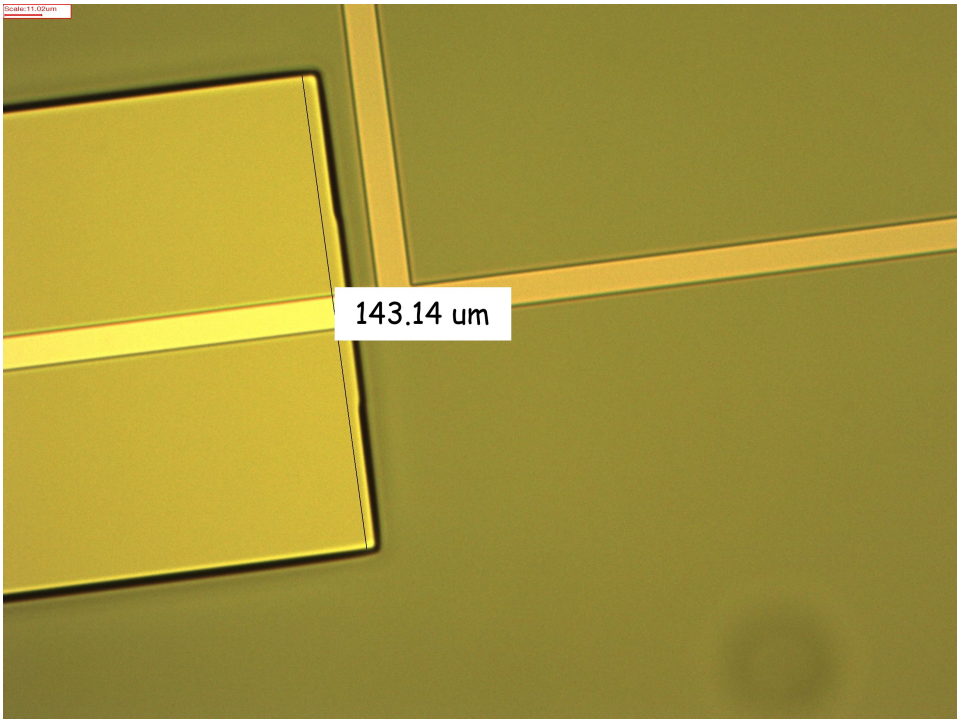


Figure 4.27: 143 um wide trench pattern developed

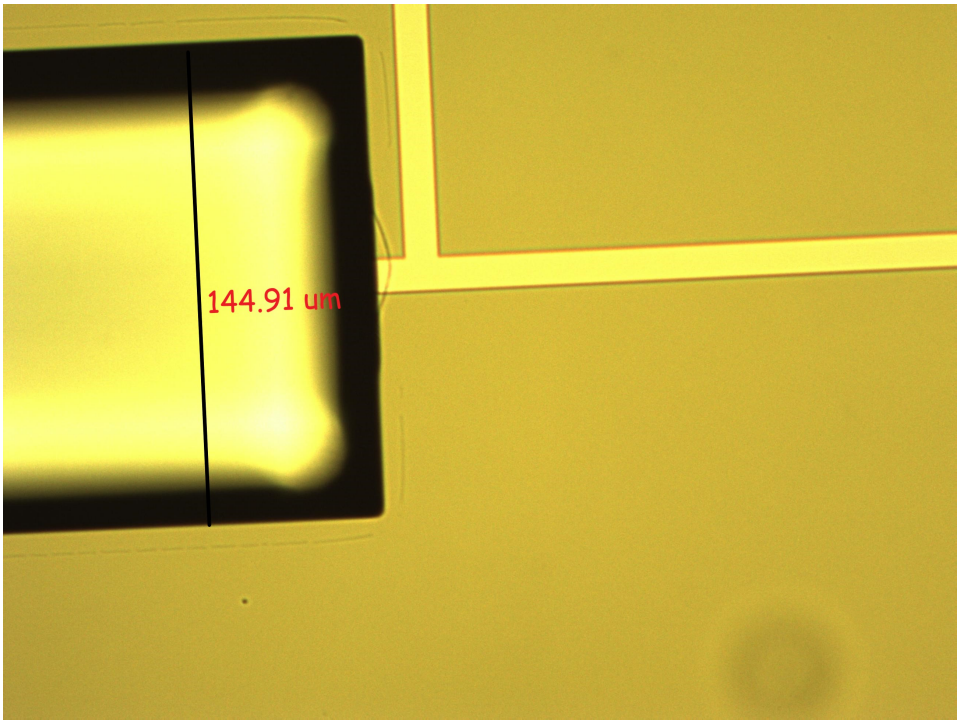


Figure 4.28: 144 um wide trench etched into the wafer

4.4.4. Finding the recipe for consistent etching rates of Silicon

Based on the simulations done in chapter 3, a range of 1 um to 4 um was selected for the width of the waveguides in the optical modulator. To make waveguides of these widths, the excess silicon around the structures needs to be etched away. As explained, we use lithography process to make the required patterns of the waveguide, use the PR as a blocking layer and etch the excess silicon substrate away using Reactive Ion Etching (RIE) with plasma. The plasma that etches the silicon is made using a combination of Hydrogen Bromide (HBr) and Chlorone (Cl_2) gases. The plasma made from this combination of gases, etches both Si and SiO2, albeit at different etching rates due to selectivity. When patterning the waveguide structures, we need to etch only the silcon, but not the bulk oxide underneath it. Which is why we need a consistent recipe for etching the silicon, such that only 340nm of the silicon substrate is etched(which is equal to the thickness of the Silicon substrate). Ideally, no bulk oxide being etched would be preferred, but since these processes are only controllable until a certain degree, a leeway of ~5 to 10 nm overetch of the bulk oxide underneath it is set as the limit. Further etching of the oxide might lead in losses of light propagating through the waveguide or formation of larger topographies which would affect the transfer of graphene and adhesion of the graphene onto the substrate.

Recipe	Etch time(s)	Depth Etched(nm)	Etch rate(nm/s)
Recipe 1	114	240	2.1
Recipe 1	162	150	0.92
Recipe 1	162	252	1.55
Recipe 1	162	234	1.44
Recipe 1	120	230	1.91
Recipe 1	180	280	1.55
Recipe 1	220	246	1.11
Recipe 2	60	554	9
Recipe 2	38	380	10
Recipe 2	35	340	9.3
Recipe 2	38	345	9.1

Table 4.1: Si Etch rates for different recipe's

Initially, a recipe with 80 sccm Cl_2 and 40 sccm HBr at a pressure of 60mTorr and temperature of 20 $^{\circ}$C was used. However, the etch rates weren't consistent enough to calculate an etching time for 340nm etch of silicon, as seen in the table 5.4. Then, a recipe that is generally used to etch poly-silicon was tried to check if it gave any consistent results. This recipe number 2 used 30 sccm Cl_2 and 40 sccm HBr at a pressure of 5mTorr and a temperature of 25 $^{\circ}$C. Recipe number 2 gave much more consistent etch rates, as seen in the table 5.4. An etch rate of ~9.3 nm per second was observed for recipe number 2 which gives an etching time of ~38 seconds to etch 340nm. When we look at the etch rates for recipe 1, we see a variation upto 100% between the tests, which is negligible for recipe 2. Hence, recipe number 2 was chosen for processing the SOI wafers to pattern the waveguides.

4.4.5. Contacting the Silicon waveguides

As mentioned in the subsection 4.3.2, having a good contact with the waveguides is crucial for biasing the graphene film. Before metallizing the contacts in the SOI wafer, a wafer from one of the earlier batches was etched for 17 seconds in the BHF (1:7) (etch rate of 1.3 nm/sec which should theoretically remove the 20 nm cladding oxide) bath to remove the cladding oxide in the contact openings for the waveguide and then was immediately metallized after rinsing, followed by the excess metal being lift-off using hot acetone. To test the contact, the vdp structure which is contacted to the silicon substrate as shown in the figure.4.5, is measured. The vdp measurement results are shown in the plot.4.29. A square resistance in the order of giga ohms is calculated for the silicon substrate, when the expected value for the substrate is in the order of mega Ohms. This means its likely there is still silicon oxide present between the metal and the Silicon substrate, and the oxide present is the native oxide that is formed between the oxide etch and the metallization. Due to this a tunnel barrier is formed because of the insulator, which results in a bad contact due to increase in the resistance. It is to be noted that it is expected that the voltages measured during the vdp measurements are quite random as we're measuring the resistance of a semi conductor. We're only interested in the magnitude of the current measured, using which we calculate the approximate resistance of the Silicon substrate.

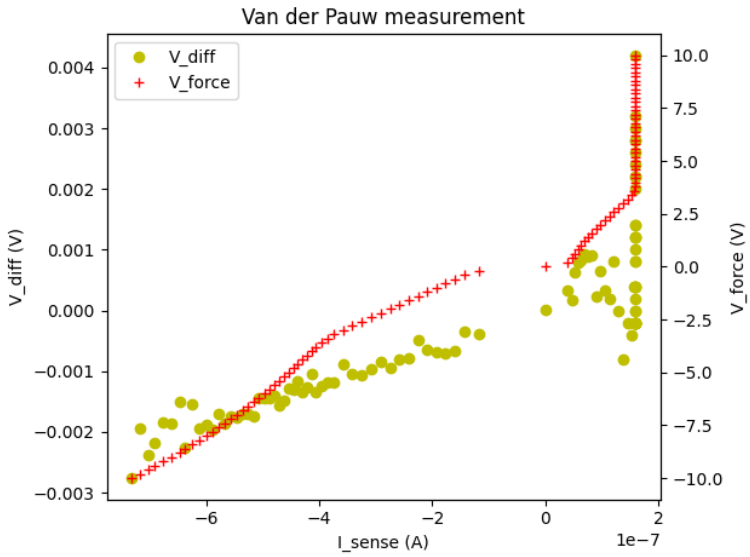


Figure 4.29: Van der Pauw measurements of Silicon substrate contacts

So, to prevent the formation of the suspected native oxide, the silicon substrate contacts must be passivated after etching the oxide away, such that no native oxide is formed before the metallization process. The passivation is done by leaving the wafer in the BHF (1:7) bath for an extra 30 ~ 45 seconds. To check if this passivation technique works, a few test Silicon substrate wafers were oxidized with 20 nm oxide layer, patterned with the metal contacts mask and then etched for 18 seconds and 45 seconds respectively, before metallization and lifting of the excess metal. The vdp structures were measured for both the wafers and their results can be seen in figures.4.30 and 4.31.

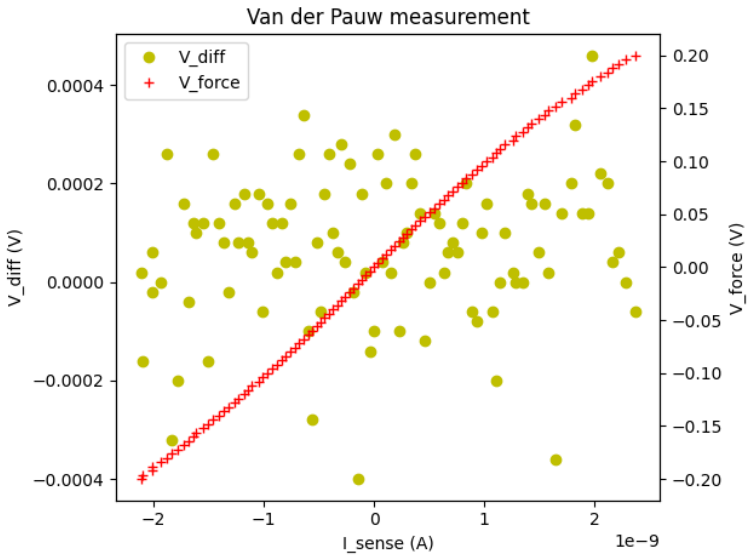


Figure 4.30: Van der Pauw measurements test wafer etched for 18 seconds

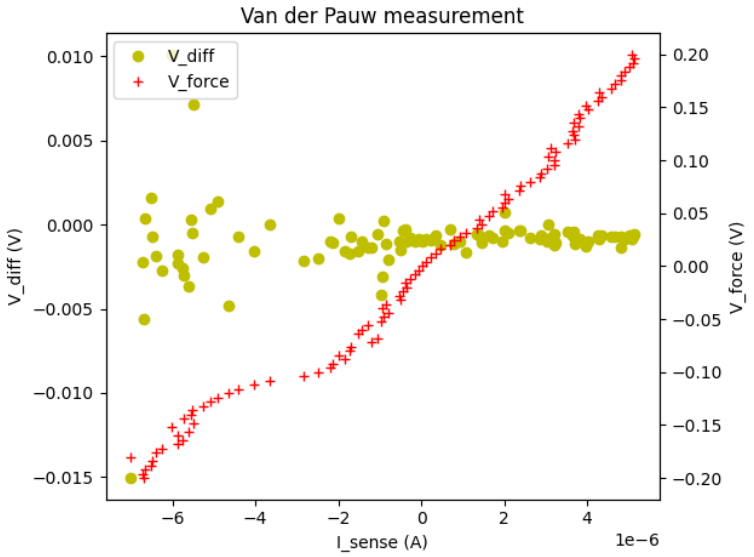


Figure 4.31: Van der Pauw measurements of test wafer etched for 45 seconds

It can be seen that the resistances calculated are in the order of mega ohms for 18 seconds etch and kilo ohms for the 45 second etch, which would mean that the passivation technique worked and no native oxide was formed before the metallization process.

4.4.6. Gold deposits at the entrance and exit of the waveguide

During the fabrication of the optical modualtors, the final steps involve metallizing the wafer and then lifting off the excess metal using acetone. Sometimes, not all the excess metal is removed during the lift-off procedure. One such case is observed near the entrance and the exit of the waveguides as seen in the figure.4.32 . It can be seen that excess gold is still deposited on the waveguide nearby the entrance/exit, which would result in bad coupling of the optical fiber and also block the light from entering the waveguide which could pose a problem.

As explained in the section 5.2.4, one of the wafers is specifically used just to test the waveguides and we

don't need contacts on that said wafer. So this makes the solution to the above problem rather simple as we don't have to selectively remove the gold from the dies. We can remove/etch away all the gold from the wafer by using a Potassium Iodide(KI) solution, which etches gold at the rate of 0.5 ~ 1 um per minute. And the results of this etch are seen in the figure 4.33.

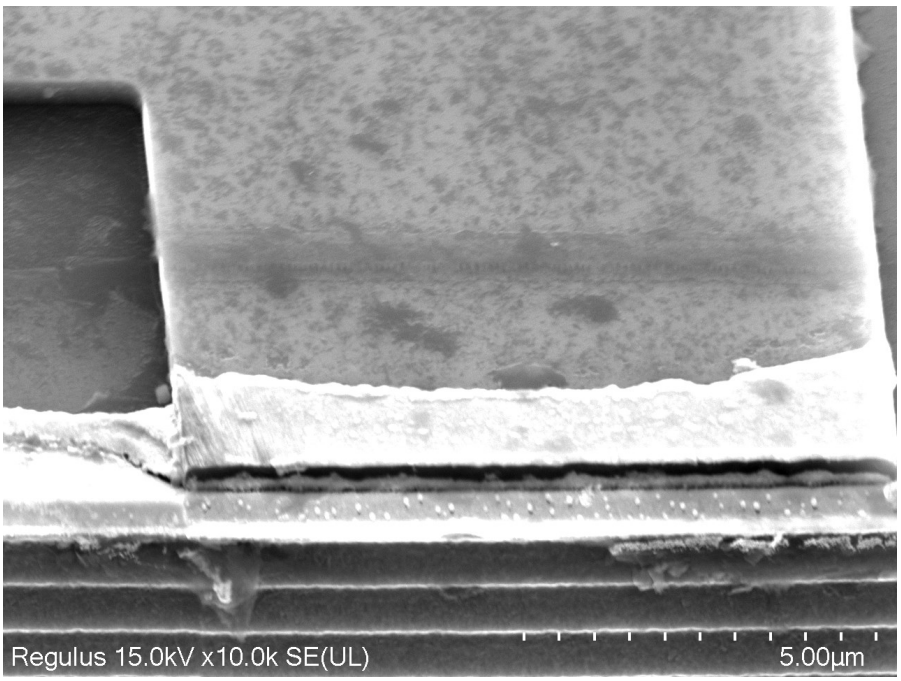


Figure 4.32: Gold deposited on the entrance/exit of the waveguide

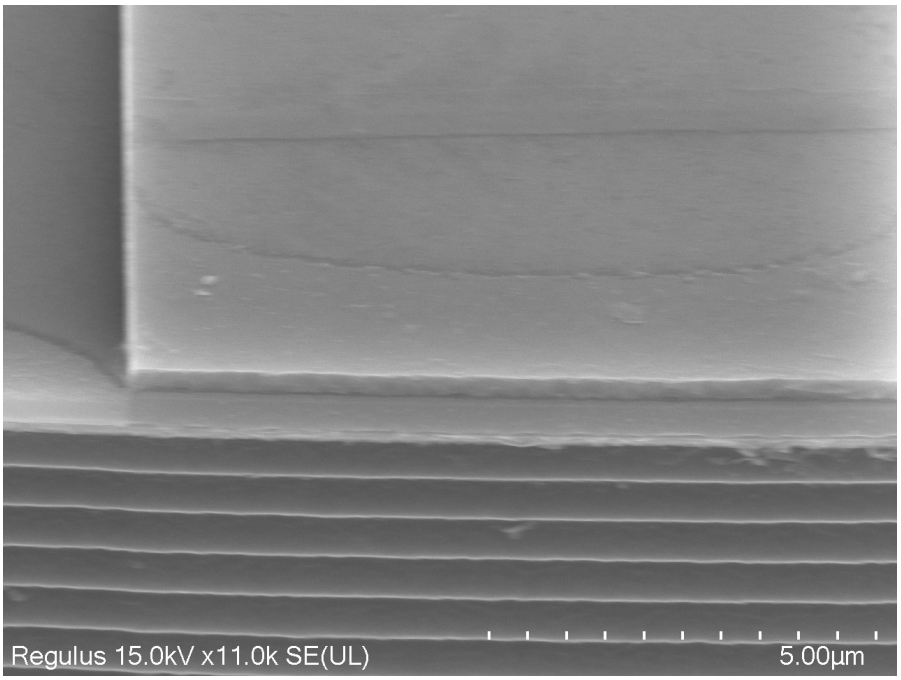


Figure 4.33: Gold deposits after etching the wafer with KI solution

5

Fabrication and Measurement Results

In this chapter we look into the fabrication results and measurement results of the devices fabricated. Firstly, we'll look into the fabrication results related to Hall devices where we measure the channel resistance exhibited by the graphene film. Then, we use the channel resistance plots to calculate the mobility and resistivity of graphene using the Drude Model.

Then we look into the CV-measurements of the oxide and calculate the value of the charge trapped in the oxide using the CV plots and use this charge trapped to calculate the shift in voltage measurements caused by it, and check if it is significant.

Finally, we look into the optical modulator. We discuss the fabrication results, then check if light successfully propagates through the waveguide, followed by if graphene can be biased and then the working of the optical modulator.

5.1. Hall Devices Results

In this section we look into the fabrication and measurement results of Hall devices.

5.1.1. Fabrication results

A wafer with 50 dies is processed with about 16 hall devices in each die. The images of all the hall devices in one of the dies are shown below. As seen in the figure 5.1, each of the devices are labelled in the form of "a x b". Here the a and b are the dimensions or the length and width of the graphene in that particular device whose channel resistance will be measured. The graphene patch and its dimensions are shown in the figure 5.2. The scratches on the metal pads seen occurred when the probes came into contact with the metal pads during the measurements. Different dimensions of the graphene films are fabricated to measure and check if there are any correlations between the dimensions of the graphene patch and the properties it exhibits. Out of the 16 devices, 8 devices(2 um x 2 um, 4 um x 2 um, 6 um x 2 um, 8 um x 2 um, 10 um x 2 um, 6 um x 6 um, 8 um x 6 um, 10 um x 6 um) are there present 1 time and 4 devices (4 um x 4 um, 6 um x 4 um, 8 um x 4 um, 10 um x 4 um) are present 2 times.

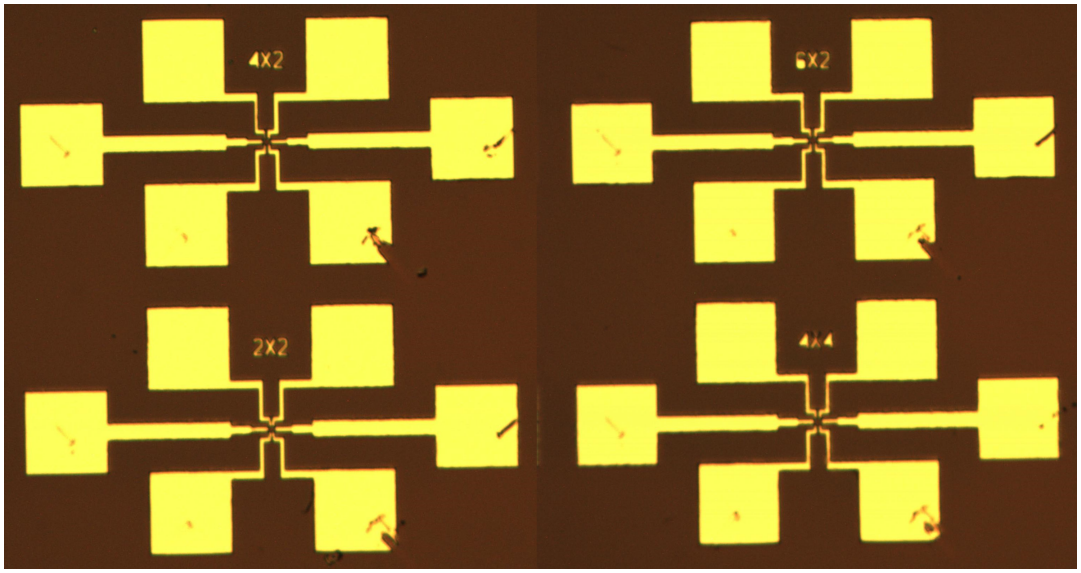


Figure 5.1: Hall Devices

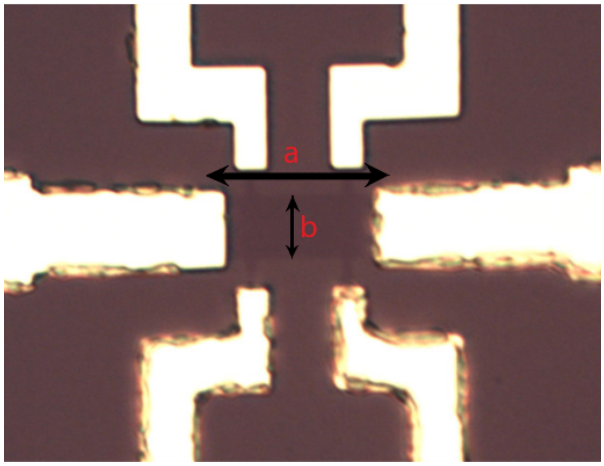


Figure 5.2: Dimensions of the graphene patch whose channel resistance is being measured

From the images it can be seen that the lift-off process was successful and the metallic contacts look defined and good. Whether the hall bars work as intended or if the devices just work in general is another story as several factors can affect the working/performance. The working can be affected if the graphene film is not contacted well or if it is delaminated or if there are defects in the films, etc. And some of these things cannot be clearly seen through the microscope but can only be verified by electrically measuring them.

The channel resistance of the hall bars is sweeped using the Cascade Microtech which can be seen in the figure.5.3, to check if the graphene is still intact. The probes that come in contact with the devices in the measurement tool are shown in figure 5.4. If a channel resistance in the order of kΩ is measured, it would mean the graphene is still intact. If resistances in the order of MΩ or GΩ are measured, that would mean that the graphene has defects or delaminated. As mentioned previously, there are 16 total devices with graphene patches of different dimensions in each die. So, 8 devices (2 um x 2 um, 4 um x 2 um, 6 um x 2 um, 8 um x 2 um, 10 um x 2 um, 6 um x 6 um, 8 um x 6 um, 10 um x 6 um) with a particular dimension is measured 50 times, 4 devices (4 um x 4 um, 6 um x 4 um, 8 um x 4 um, 10 um x 4 um) are measured 100 times and a total of 800 devices are measured for their channel resistance, and the results for number of working devices and their average channel resistances at the dirac point is shown below in the table 5.1. The dirac point is the voltage at which the carrier concentration for both the electrons and holes is the same. And at this voltage the resistance observed is the highest as there are no carriers to transport the current. The average dirac voltages

are also shown in the 5.2.

Device dimensions(W um x L um)	Total devices	Working Devices	Average Channel Resistance(kΩ)	Standard deviation of Channel Resistance(kΩ)
2x2	50	36	6.74	0.693
4x2	50	29	13.27	0.88
6x2	50	29	17.1	1.9
8x2	50	35	21.6	1.139
10x2	50	33	27.1	2.46
6x6	50	31	6.14	1.9
8x6	50	25	8.5	2.4
10x6	50	25	8.6	1.8
4x4	100	60	7.3	1.94
6x4	100	61	8.9	1.75
8x4	100	49	12	1.96
10x4	100	55	13.9	2.47

Table 5.1: Number of working Hall bars and their average channel resistances at the dirac point.

About 50 ~ 70% of the devices fabricated are still working and the devices that weren't working either had the graphene delaminated, the graphene damaged or the graphene with a lot of residues(which affects its properties). And upon comparing the relation between dimensions and the channel resistance, the relation follows the equation 5.1, which is to be expected. The relation is almost completely linear, the slight deviations are due to some stray measurements which were too high or too low than the majority of the measurements, which contribute in driving the average up. The resistivity of graphene calculated from these values of channel resistance is seen in 5.2 and their comparisons are discussed in the next subsection.

$$R_{channel} \propto \frac{L}{W} \tag{5.1}$$

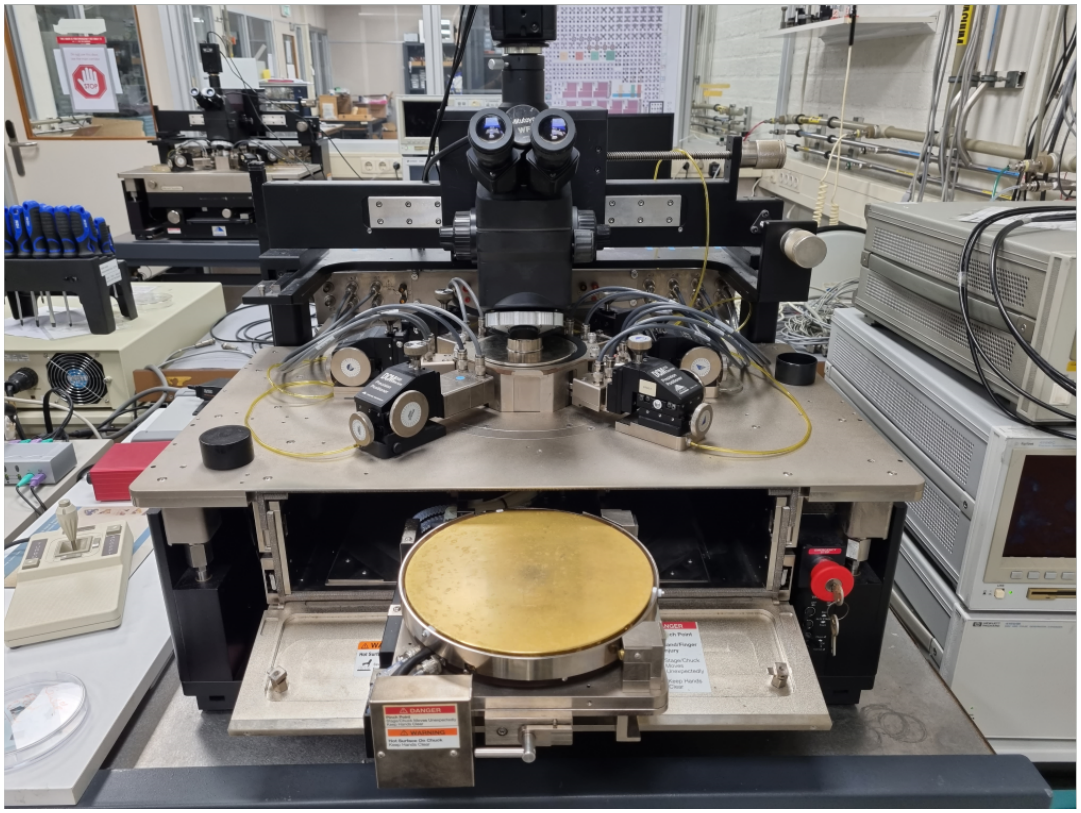


Figure 5.3: Cascade Microtech measurement tool

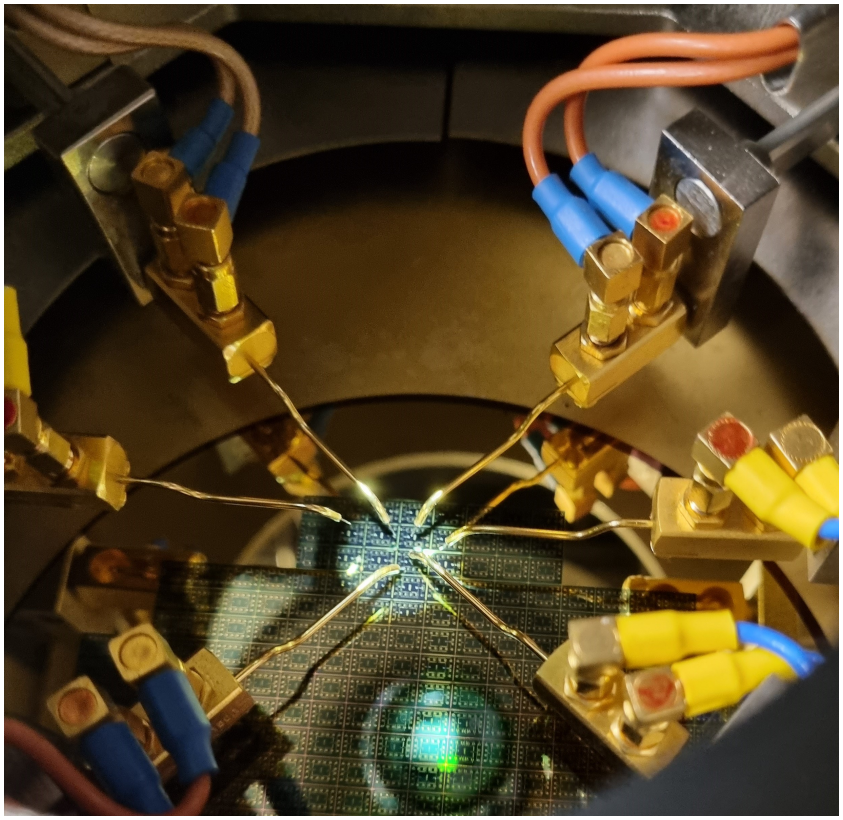


Figure 5.4: The probes in the Cascade Microtech measurement tool.

5.1.2. Calculating electrical properties

The electrical properties we are interested in are the mobility and resitivity exhibited by graphene films. These properties are not something that can be directly be measured by connecting the fabricate device to a mutlimeter and forcing some current or voltage to get a value. Rather, they're properties which are calculated or derived from the channel resistance plots of graphene film channel used in Hall bars/devices. So, we use the channel resistances of the Hall device. As mentioned previously, the measurements are done using Cascade Microtech measurement took and the points at which the probes in the tool are placed during the measurement are shown in the figure 5.5.

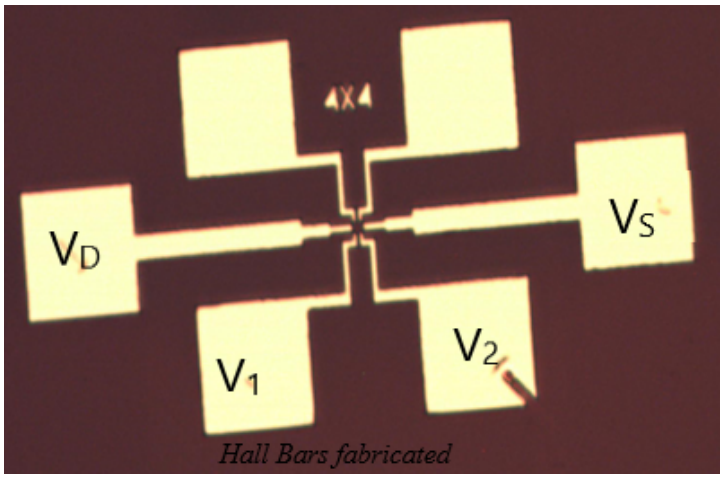


Figure 5.5: Points of contact of the probes during measurement

V_D and V_S are the contacts for drain and source respectively, and these two points are used to force a current of 10 uA at all times and their voltages are changed accordingly. V_1 and V_2 are the points where the voltage drop between the channel is measured. There is another point of biasing, which can't be seen in the picture, that is used during the measurements. It is the voltage applied to the bulk using the chuck of the measurement tool. This voltage is the gate voltage V_G and this is the voltage varied during the measurement. A change in V_G changes the channel resistance of the graphene film and we plot the change in channel resistance for a varying V_G and use this plot to calculate the mobility and resistivity. The channel resistivity plot is shown in figure.5.6 for a graphene film of dimensions 6 um x 4 um.

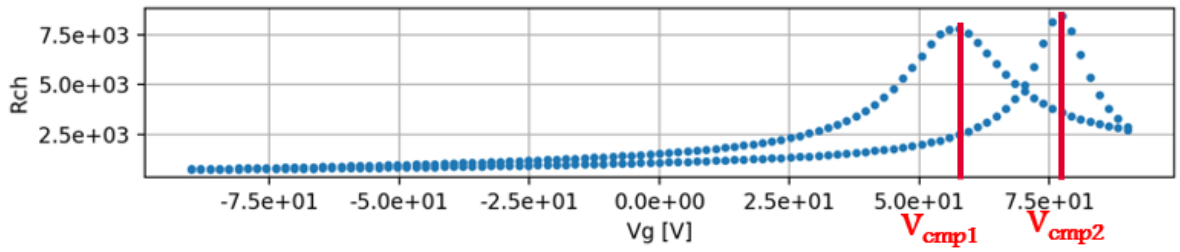


Figure 5.6: Channel resistance vs V_G plot

In the plot, two peaks are observed, one from when the gate voltage is swept from -90 V to +90 V(Left peak) and the other when the gate voltage is swept from +90 V to -9 0V(Right peak). And these peaks are observed when we reach the dirac points in the band strucutre. The voltages at which these peaks are observed are called V_{cmp1} (Left peak) and V_{cmp2} (Right peak). Ideally, both the peaks should appear at the same voltage, but 2 different peaks are observed due to some residues at the contact points of the graphene, which dope the contacted part of the graphene affecting the measurements from being accurate. Now, we use the Drude model to calculate the mobility of the graphene film. First, we calculate the resistivity of the graphene film using the equation 5.2 and calculate the conductivity using the relation given in equation 5.3. We calculate

the above values for a gate voltage of 45V. The value of 45 V is just an arbitrary value chosen for the sake of calculation.

$$\rho = R_{ch}\frac{W}{L} \tag{5.2}$$

$$\sigma = \frac{1}{\rho} \tag{5.3}$$

where R_{ch} is the channel resistance from the plot at the gate voltage of 45 V. W and L are the width and length of the graphene strip. All these values for both the peaks are then substituted into Drude Mobility equation which is given below.

$$\mu_{Drude} = \frac{\sigma}{C_{ox}}\frac{1}{|V_g - V_{cmp}|} \tag{5.4}$$

The resistivities were found to be 3190.37 Ω and 1184.02 Ω. And the mobilities were found to be 2053 cm^2/Vs and 2142.63 cm^2/Vs. And we average them out to get an average resistivity of 2779 Ω and average mobility of 2097.81 cm^2/Vs, which are along the lines of the values expected by ANL.

Similarly, we can calculate the mobility and the resistivity for any of the devices at any required voltage, except for the voltage at the dirac points as then, the denominator in the equation 5.4 becomes 0. The average dirac voltages which could be used to calculate mobility, for different dimensions of graphene films in the devices is given in the table below. For ease of calculation, only the first peak is used to calculate the average value as the 2nd peak frequently went past the used maximum voltage of 90 V. The average resistivity and mobility at 45 V calculated using the values in table 5.2 are shown in the table 5.3

Device dimensions(W um x L um)	Maximum Dirac Voltage(V)	Minimum Dirac Voltage(V)	Average Dirac Voltage(V)	Standard deviation of dirac voltage(V)
2x2	62	95	75.9	8.99
4x2	50	93	73.8	8.72
6x2	59	95	73.3	8.52
8x2	55	90	71.8	9.55
10x2	50	95	73.5	10.9
6x6	59	95	72.7	10.49
8x6	50	95	76.2	10.34
10x6	53	90	73.7	8.82
4x4	59	95	72	9.39
6x4	54	95	73.1	10.92
8x4	50	92	71.8	8.33
10x4	55	95	75.7	10.27

Table 5.2: Number of working Hall bars and their average channel resistances.

Comparing the values in the table, it can be seen that the average dirac voltage for all the devices lie close to each other i.e around 74 ∓ 3 V. Similarly, the average resistivity and mobility are also close to the each other and are close to the values calculated for V_{cmp1} in figure.5.6. The maximum dirac voltage and the minimum dirac voltage for all the devices have a difference of ~40 V. This high a difference is due to the differences in the amount of residues or defects in the patches. Further cleaning and removal of more polymer residues can result in the maximum dirac voltage as well as the average dirac voltage shifting down. Next, we check the charge trapped in the oxide and see how it affects the electrical measurements.

5.1.3. Calculating the charge trapped in the oxide

The metal contacts, oxide and the Silicon substrate together form a Metal-oxide-semiconductor (MOS) structure. The Silicon oxide insulator is a thermally grown oxide. And thermally grown oxides generally has trapped charge in the oxide due to improper bonding between the valence electrons in the Silicon substrate and the SiO_2 substrate. This trapped charge is usually negligible, but in case a significant amount of charge is trapped,

Device dimensions(W um x L um)	Average Resistivity at 45V (kΩ)	Average Mobility at 45V(cm^2/Vs)
2x2	1.7	1573.28
4x2	2.5	1147.84
6x2	2.06	1417.62
8x2	2	1541.87
10x2	2.4	1208.25
6x6	2.5	1193.42
8x6	2.25	1177.27
10x6	2.1	1371.24
4x4	2.8	1093.18
6x4	2.27	1295.63
8x4	2.25	1370.55
10x4	1.7	1583.53

Table 5.3: Number of working Hall bars and their average channel resistances.

the transfer characteristics of the device might be affected or shifted (A shift in the dirac point may be observed). The shift is observed due to the additional voltage biasing required to neutralize the trapped charge.

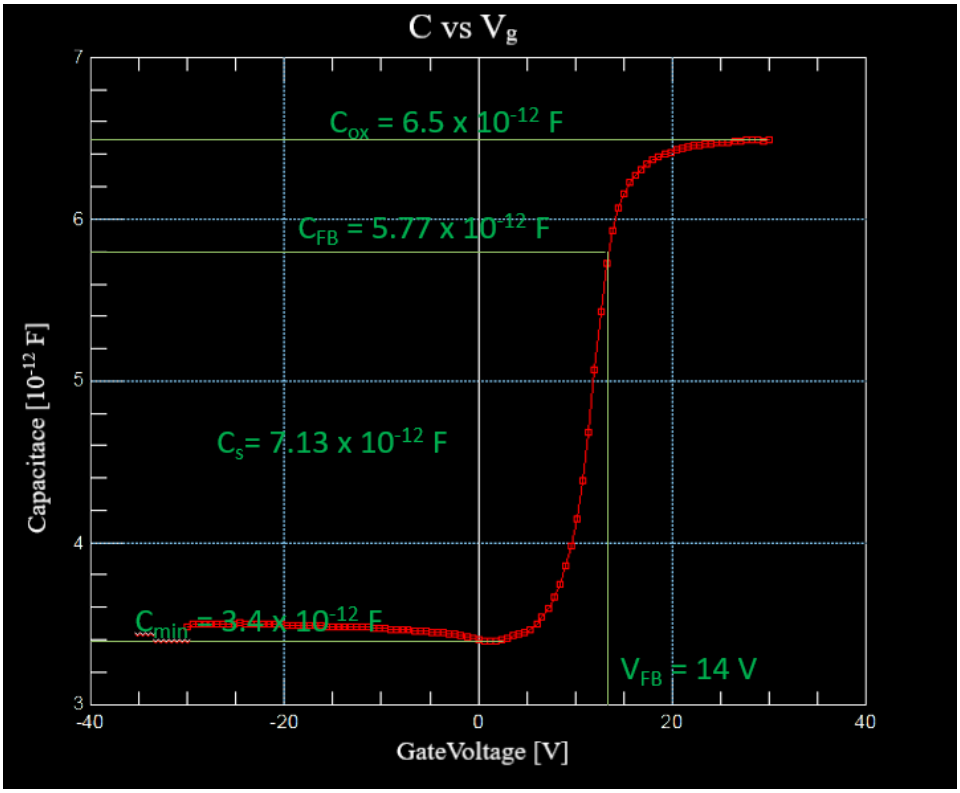


Figure 5.7: CV measurements of a MOS structure

To calculate the value of charge trapped in the oxide, we do CV measurements of the MOS capacitor and then use the plot and the flat-band condition to calculate the value. The measurements are done in different area's of the wafer, one of the plots is shown in figure. to , as the value of charge trapped is not usually uniform over the wafer. Then the trapped charge is calculated individually from each of these plots and then the value is averaged. The flat-band voltage condition is used for the calculations, which are shown below. The equations used below are taken from.

$$C_{ox} = \frac{\epsilon_o \epsilon_s A}{t_{ox}} \tag{5.5}$$

$$\frac{1}{C_s} = \frac{1}{C_{min}} - \frac{1}{Cox} \tag{5.6}$$

$$\frac{1}{C_{FB}} = \frac{1}{C_{ox}} + \frac{1}{2C_s\sqrt{ln(\frac{|N_A - N_D|}{n_i})}} \tag{5.7}$$

$$V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}} \tag{5.8}$$

Where $\epsilon_o = 8.85x10^{-12} F/m$ is electric permittivity of free space, $\epsilon_s = 3.9$ is the permittivity constant for Silicon dioxide, $A = \pi(120x10^{-6})^2 m^2$ is the Area of the measured capacitive device and $t_{ox} = 285x10^{-9} m$. Substituting these values into equation 5.5 gives $C_{ox} = 5.48x10^{-12} F$.

Now, substituting the values of C_{ox} and C_{min} from the measurement graphs into equation 5.6, we get the value of C_s which is the surface capacitance. And subsituting the value of C_s into equation 5.7, we can calculate the flat band capacitance C_{FB}. Here, N_A is the acceptor carrier concentration which lies between $4x10^{15} cm^3$ and $6x10^{15} cm^3$. Hence, we use the average of $5x10^{15} cm^3$ as the value of N_A. N_D is the donor carrier concentration and n_i is the intrinsic carrier concentration. n_i is a constant whose value is equal to $10^{10} cm^3$. N_D however is calculated from the equation:

$$N_D = \frac{n_i^2}{N_A} \tag{5.9}$$

Substituting all these values into 5.8 we can calculate the value of Flat band capacitance C_{FB}. Using C_{FB}, we obtain the flat band voltage V_{FB} from the measurement graphs and substitute the value in equation 5.8 to get the value of Q'_{ss} which is the trapped charge in the oxide. ϕ_{ms} in the equation is the metal semiconductor work function whose value is equal to 0.9V if gold is the metal layer. The calculated trapped charges for different zones on the wafer, and the average of all these values is given in the table below.

Position on the wafer	Charge trapped in the oxide(C)
Top Left	96.85x10^-12
Top Right	93.13x10^-12
Bottom Left	78.54x10^-12
Bottom Right	78.54x10^-12
Average	87.21x10^-12

Table 5.4: Calculated values of charge trapped in oxide in different zones

Now, we calculate the voltage shift the trapped charge causes using the equation 5.10.

$$V_{shift} = \frac{Q'_{ss}}{C_{ox}} \tag{5.10}$$

Substituting the average trapped charge from 5.4 and a C_{ox} of 5.48x10^-12 F, we get a value of -1.5 V. The value is pretty negligible and only accounts to ~1-2% of the V_{cmp} seen in figure 5.6, so the effect of trapped charge on the measurements can be neglected.

5.2. Optical Modulator results

In this section we look into the fabrication and measurement results of the optical modulator.

5.2.1. Fabrication Results

For the fabrication results, first lets look into the results of the waveguides. There were 15 waveguide structures in each of the dies, and a total of 50 dies in the wafer. The 15 waveguides are as follows, we have 2 waveguides each for 1 um, 1.5 um, 2 um, 2.5 um, 3 um, 3.5um and the 4 um wide waveguides. And 1 meander waveguide to add up to a total of 15 waveguides. Upon inspection, 2 of the 50 dies were damaged during processing which means about 720 waveguides are still intact. The waveguide structures(Top view) etched into the wafer are shown in the figure.5.8 and a close up of the 1 um wide waveguide is shown in figure.5.9 .

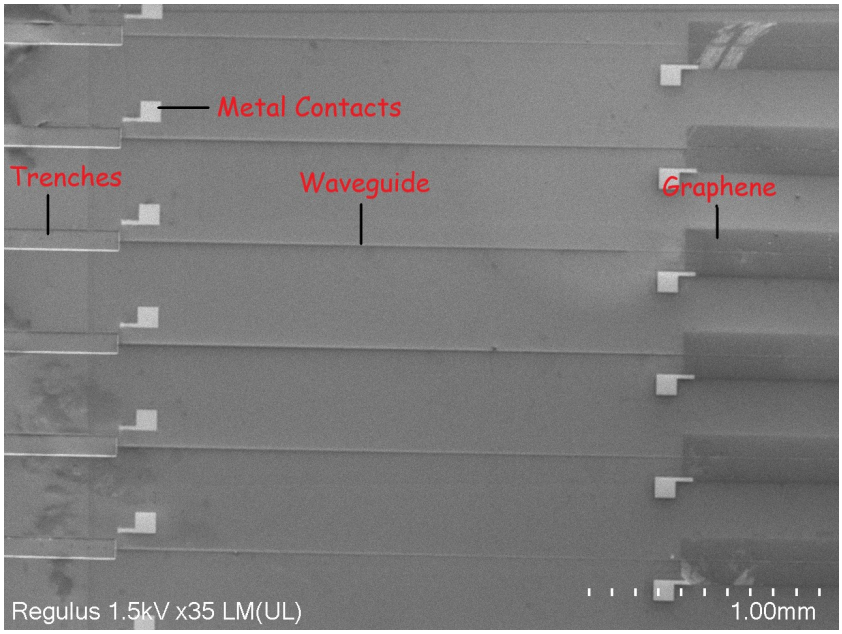


Figure 5.8: SEM image of Optical Modulators(Top view) fabricated on an SOI wafer die

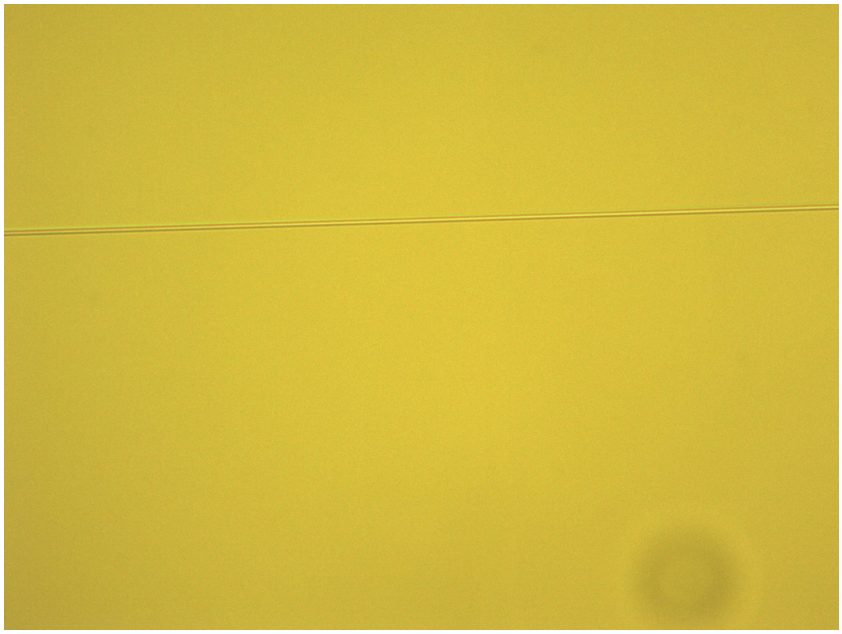


Figure 5.9: Close up of the 1um wide waveguide (20x magnification)

For good coupling between the optical fiber and the waveguide, the entrance/exit sidewalls of the waveguide needs to be smooth, such that majority of the light enters the waveguide. Reactive Ion etching with the recipe of Cl_2 at 30 sccm and HBr at 40 sccm with a pressure of 5 mTorr and a temperature of 25 $^{\circ}$C, is used

to etch the waveguide patterns onto the top Silicon substrate. RIE unlike Deep Reactive Ion Etching(DRIE) gives smooth side walls which can be seen in the entrance/ exit sidewalls of the waveguides(picture taken before metallization) in the figure.5.10 , and these smooth sidewalls, should result in good coupling with the optical fibers. The height of the waveguides was also measured using Dektak 8, and a height of ~340 nm was measured. This means that during the etching of the waveguides the right amount of time was used to etch the top silicon substrate and the etching was stopped exactly at the bulk oxide top silicon interface, with no extra oxide being etched.

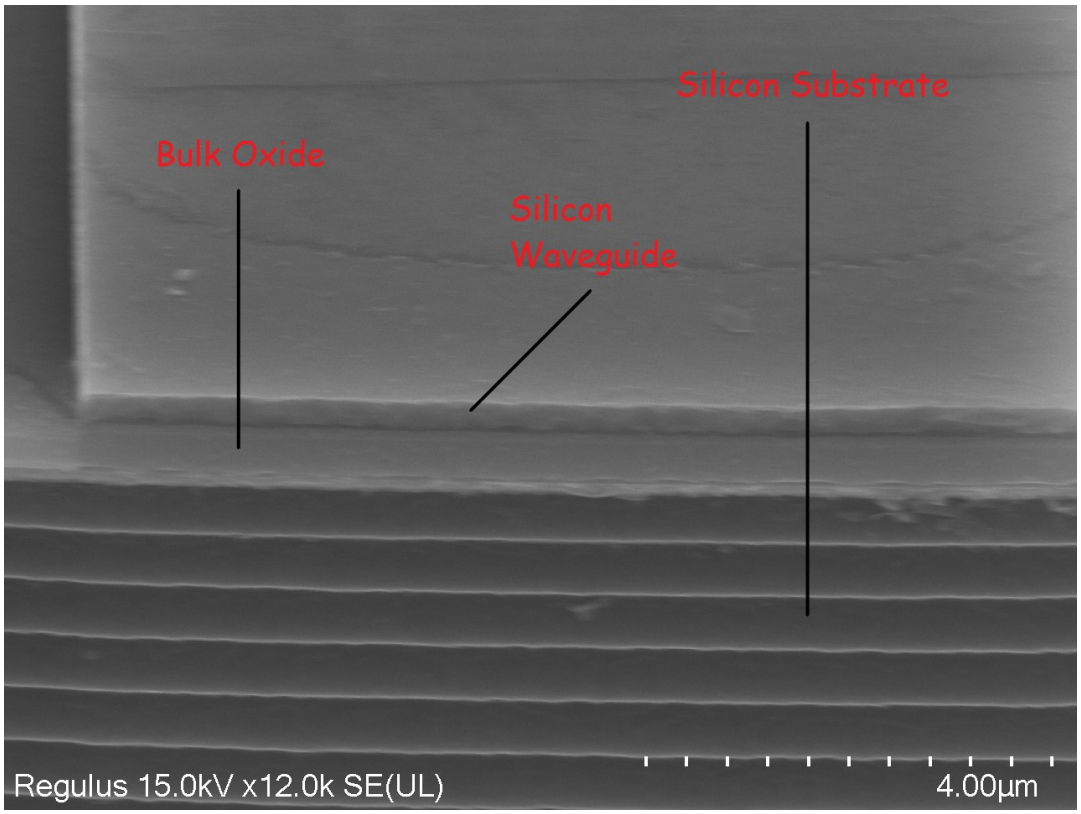


Figure 5.10: Sidewall entrace/exit of the waveguides

Now we take a look at the trenches etched into the wafer. In section 4.3, we say that the etching of trenches into the wafer is an optional step. As even without the trenches, the waveguides can be extended to the edges of the die and then be aligned with the optical fibers from the sides of the die. This could pose a problem as aligning the 10 um wide optical fiber core and a 340 nm tall waveguide would be really difficult. Not just the difficulties in alignment, but the sidewalls of the waveguides may not be as smooth when diced due to chiping at the edges, which could pose a problem for coupling the waveguide and the fiber. So trenches were etched into the wafer which help in both aligning the waveguides easily and having a smooth sidewall for good coupling. As mentioned in section 4.3, to etch the trenches into the wafer, we fist etch the top Silicon substrate with RIE, then the bulk oxide with plasma etching and the bottom Silicon substrate with DRIE. The results of the different kind of etching can be seen in figure 5.10. The top Silicon substrate and the bulk oxide have smooth surfaces due to normal plasma etching, but the bottom Silicon substrate has grooves, which is due to DRIE. We use DRIE for the bottom substrate instead of RIE like we did for the top substrate because the Silicon is etched much faster in DRIE and we dont really care about having a smooth surface for the bottom substrate. The trenches need to be > 67 um deep and > 130um wide for the optical fiber to fit in it. The depth was measured using Dektak 8 and found to be 69 um, which is along the lines of what we need. The width of the trench is measured to be around 140 um (seen in figure 5.11) which is again along the lines of what we need to fit the optical fiber.

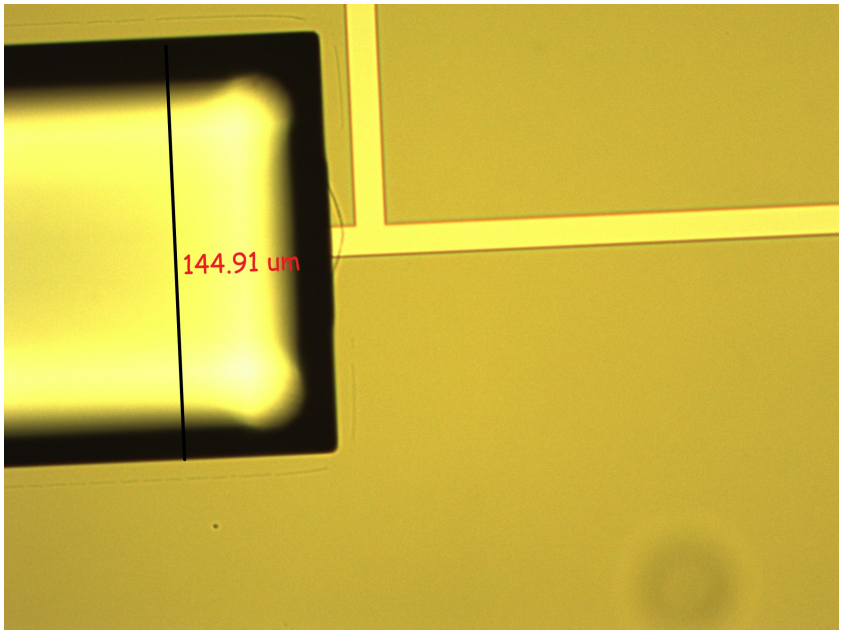


Figure 5.11: 144.91um wide trench etched into the wafer

5.2.2. Checking conductance of the graphene film and the waveguides

For us to successfully modulate the light propagating through the waveguide, we need both the waveguide and the graphene to conduct current so that we can bias them to reach the dirac point, where the Pauli-blocking occurs and the light is absorbed. To check whether the graphene film and the waveguide are conducting, IV measurements are done for the graphene films and the silicon waveguide. Then the resistance is roughly calculated to check if it is around the expected values. The IV measurement of the graphene film is given in the figure.5.12 and that of the silicon waveguide is given in figure.5.14. It is to be noted that it is expected that the voltages measured during the vdp measurements are quite random as we're measuring the resistance of a semi conductor. We're only interested in the magnitude of the current measured, using which we calculate the approximate resistance of the Silicon substrate.

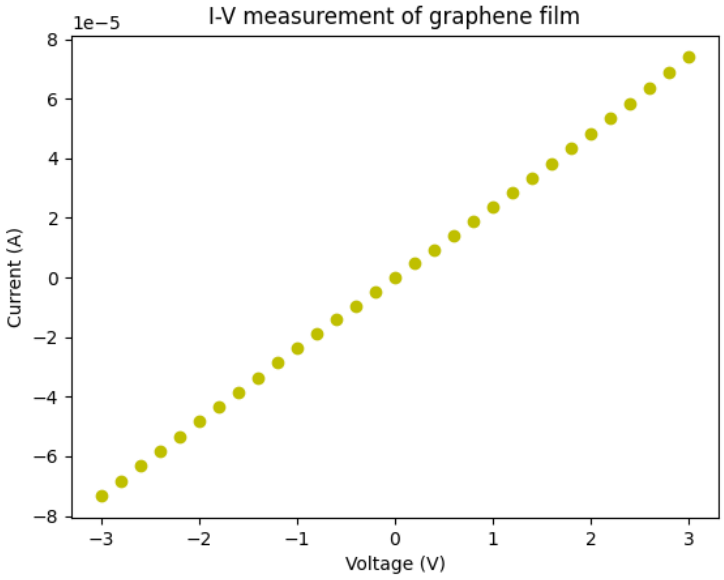


Figure 5.12: IV measurement plot of graphene film in an optical modulator

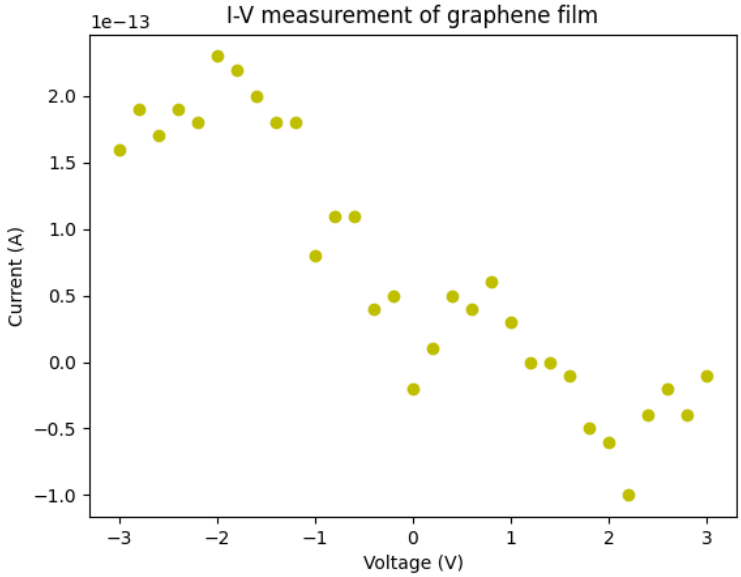


Figure 5.13: IV measurement plot of silicon waveguides in an optical modulator

In the IV measurements for graphene (figure 5.12), we see a current in the order of uA and calculate the resistance to be in the order of kilo ohms. As this is around what we measured in the section 5.2.2, we can conclude that the graphene is contacted well and is conducting.

Now, when we come to the IV measurements of the silicon waveguide (figure 5.13), we see a current in the order of fA and also that the current is negative for a voltage of 0 V. This could either mean that the waveguide is not conducting or the contacts to the waveguide are bad. We further do vdp measurements of Silicon substrate (5.14) to check if smaller dimensions Silicon substrate would conduction. But, again a current in the order of nA was measured which is still too low for the silicon substrate to be conducting (A current in the order of uA is expected).

Initially, it was assumed that the contacts to the waveguide are bad and hence we tested out a solution to get better contacts in section 4.3.4 and applied it to a new wafer. As mentioned in section 4.3.4 we need to passivate the silicon waveguide subsrtate from forming native oxide, before we metallize the contacts and we do this by leaving the waveguide in BHF(1:7) for an extra amount of time that exceeds the time required to etch away the cladding oxide in the metal contact openings.

So, the wafer was put in a BHF(1:7) bath for 18 + 42 seconds, adding upto a total of 60 seconds. The 18 seconds are for etching the cladding oxide away and the ~40 seconds are to passivate the surface from forming native oxide. Then the wafer was metallized and the excess metal was lift-off using hot acetone. The new wafer was used to measure the conductance of Si waveguides, but unfortunately the current measured was still in the order of nA as seen in the figure.5.15. This means that the problem is not with the contacts, but that the Si waveguides don't really conduct. And upon researching the properties of the SOI wafer, it was found that they have a resistivity of about 2 ~ 3e14 Ohms-cm. Which would mean that the 340 nm thick waveguides would have a resistance of about 0.5 mega ohms per square. If we translate that to the total length of the waveguide(A waveguide is about 12000 squares), we get the resistance of the waveguide to be in the order of hundreds of giga Ohms. This would mean that the waveguide doesnt conduct well and hence it's going to be very hard to bias the graphene using the top gate configuration. The top gate configuration mentioned here means that the graphene is biased using the the contact to the silicon that is on the top side of the wafer. There is however another configuration using which, the graphene can be biased. It is called the back gate configuration, in which we bias the graphene film using the back side of the wafer. The back gate configuration was already used for measureing the channel resistances in section 5.2.2. The different biasing configurations are shown in the figure.5.16.

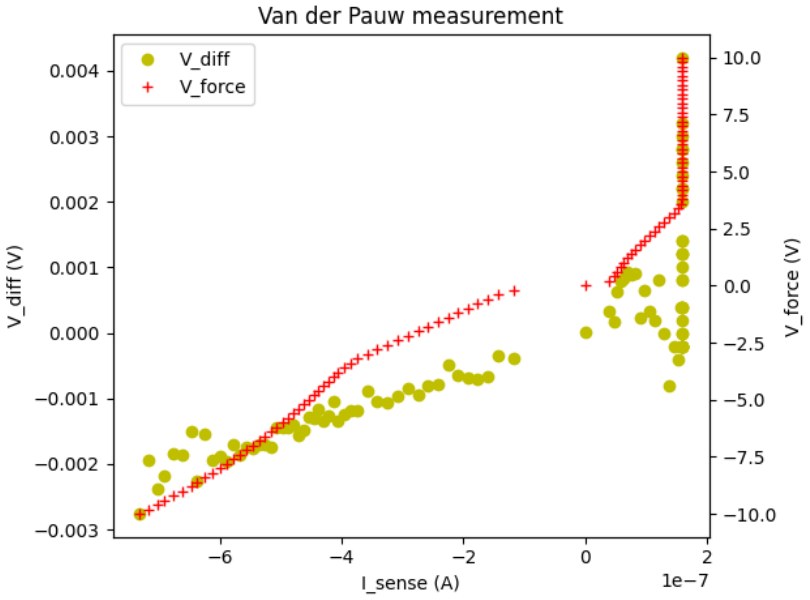


Figure 5.14: Van der Pauw measurement of the Silicon waveguides without passivating the Silicon substrate in the contact openings

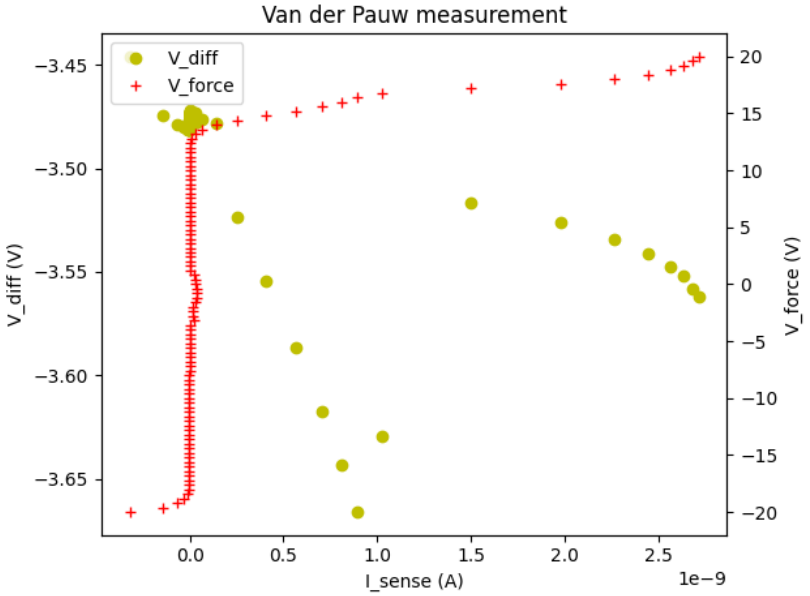


Figure 5.15: Van der Pauw measurement of the Silicon waveguides contacted after passivating the Silicon substrate in the contact openings

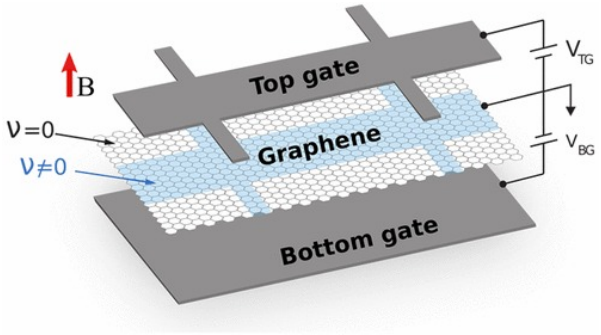


Figure 5.16: The top gate and back gate configurations to bias the graphene

5.2.3. Biasing the graphene on the optical modulator

As mentioned in the previous subsection, the resistivity exhibited by the silicon waveguide is really high and hence using the top gate configuration would be very difficult to bias the graphene. Instead, we need to use the back gate configuration for the biasing. To check if the back configuration is working, we use the hall devices on the die that are similar to the ones used in figure 5.5 and check if we can reach the dirac voltage. Unlike the constant current applied for measurements in section 5.1.1, we apply a constant voltage of 100 mV at the drain for dirac voltage measurements. And the gate voltage is applied to the bottom silicon substrate. One might wonder, if the resistance of the top silicon substrate is too high to conduct, why wouldn't the resistance of the bottom gate be too high to conduct? The answer to this is as follows. The waveguides patterned on the top silicon substrate are only 340 nm thick and a few micrometers wide. So the volume of Silicon left for the top substrate is very low. The resistance for the top substrate is high, as the number of free charge carriers available to conduct electricity is low, due to the low doping concentration. Now, the back gate is a few hundreds of um thick and the volume of silicon is significantly higher when compared to that of the top substrate. This means the amount of free charge carriers are higher compared to that of the top substrate. So the back gate is more likely to conduct electricity for biasing, when compared to the top gate for the current available wafer. The Id-Vg plot for one of the devices(2um x 2um) biased using the back gate is shown in the figure. 5.17. And the channel resistance is seen in figure 5.18.

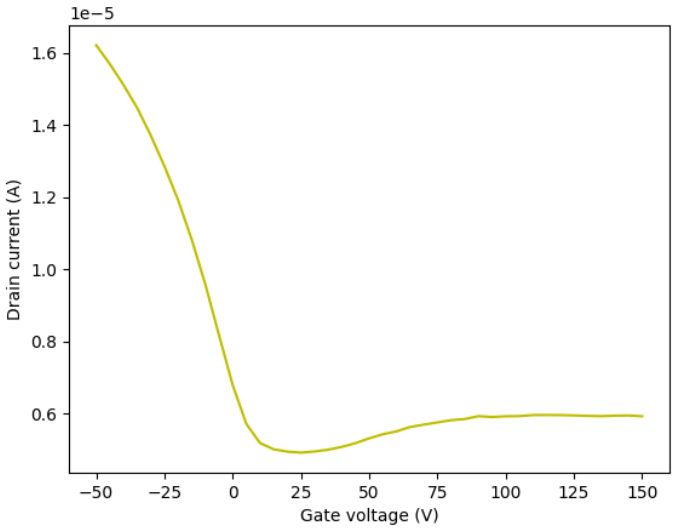


Figure 5.17: Id-Vg graph to check the dirac voltage for the back gate configuration for a contant V_{DS} of 100 mV

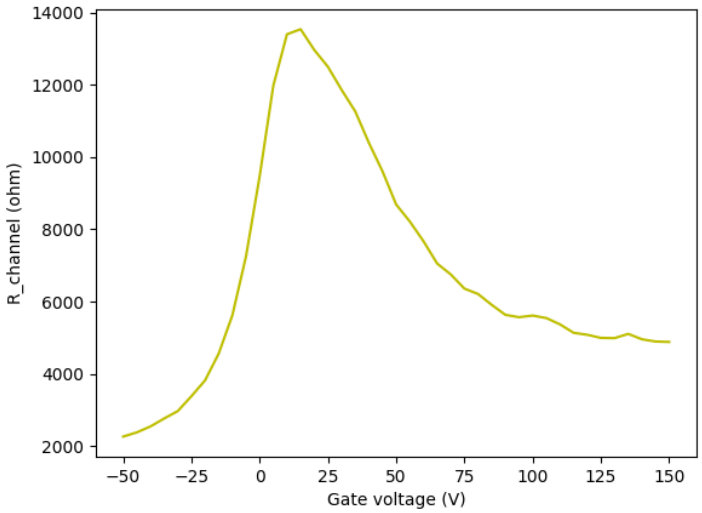


Figure 5.18: Id-Vg graph to check the dirac voltage for the back gate configuration for a contant V_{DS} of 100 mV

We can see that the transfer characteristics look more or less like we expected and it is comparable to the transfer characteristics seen in the figure. 2.2. The channel resistance plot is also comparable to the channel resistance in figure 5.6. The dirac voltage looks to be at around ~20V, but it does look like the device faces some troubles fully inverting after the dirac point and the current levels off instead of rising up again. This maybe due to some non-idealities in the graphene. The suspected reason for this behaviour is as follows. We know that the majority charge carriers in the graphene film to the right side of the dirac point are the electrons. So, when the graphene is past the dirac point towards the higher positive voltages, the graphene acts as if it is n-type doped. Now, there have been cases reported where the graphene films are doped by the metal contacts at the points of contact, Giovanetti et al.[51]. Lets say that at the metal contacts, the graphene is p type doped. This would create a configuration shown in figure 5.19. As seen in the figure, two junctions p-n and n-p are formed on the graphene film. Therefore, for the current to pass from drain to source in the hall bars, it needs to go through two diode like structures when in the electron regime, which might explain the unexpected behaviour of the devices. Furthermore, when the graphene is in the holes regime(bias voltage less than the dirac voltage), graphene behaves as if it is p-type doped. So, a p-p-p type configurations would be formed in the graphene films, and hence the device behaves as expected. Whether this actually happens or not is still unclear and further testing needs to be done to confirm this theory.

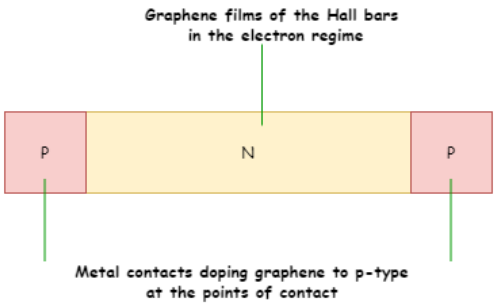


Figure 5.19: P-N-P configuration formed on the graphene film

Anyway, as the dirac voltage can be reached for the graphene films, it means that pauli blocking can occur, which would result in the graphene absorbing the light. Suppose we compare the dirac voltage measured here to the average dirac voltage measured for a 2 um x 2 um graphene patch in section 4.1.2, a difference of about 30V is seen. Ideally, when a graphene film is biased, it follows the relation given in equation.5.13, where

Vg is the gate voltage, C_{ox} is the oxide capacitance, ϵ_{ox} is the permittivity of the oxide and t_{ox} is the thickness of the oxide. It can be seen that the dirac voltage of the graphene is linearly proportional to thickness of the oxide between the gate and the graphene film due to device being similar to a MOS capacitor. Please do note that in the below equations, an approximation is made where V_g - V_t (threshold voltage of the MOS capacitor) is approximated to just V_g, since the value of V_t is negligible.

$$C_{ox}\frac{1}{Vg} \tag{5.11}$$

and

$$C_{ox} = \frac{\epsilon_o x}{t_o x} \tag{5.12}$$

combining the above two equations

$$t_o x \propto V_g \tag{5.13}$$

Now, for the measurements done in section 5.1.2, the oxide was about 285 nm thick. For the SOI wafer however, if the measurements are done using the back gate, the oxide thickness would be around ~420 nm. If we use the 5.13 to calculate the value of the dirac voltage, we get a value of around ~112 V. However, this value of 112 V is valid only if the same piece of graphene is biased through 440nm oxide. Since the properties of graphene changes from batch to batch or even from one spot in the same film to another spot, the dirac voltage of 40V is observed for the other device. Also, the difference in how clean the wafer is, might also affect the dirac voltage measured. So, this could mean the wafer measured in section 5.1.2 might still have some residues on it due to improper cleaning, which shifted the dirac point to ~70V. So, we can conclude that the measured dirac voltage of 40V is acceptable and that we can absorb light using this graphene film.

Similarly, more devices are measured to check the percentage of devices working and their dirac voltages. About 160 total devices are measured and out of those only 47 of the devices are fully working. That translates to about 30% of the devices working. This when compared to the number of devices working after the hall bar fabrication (5.1) is drastically low. The number of devices working for different dimensional devices is shown in table 5.5

Device dimensions(W um x L um)	Total devices	Working Devices	Average Dirac Voltage(V)	Standard deviation of Dirac Voltage(kOhms)
2x2	10	4	73.33	36.81
4x2	10	2	110	10
6x2	10	1	145	0
8x2	10	3	105	25
10x2	10	4	115	13.69
6x6	10	3	151.67	9.23
8x6	10	6	144	17.43
10x6	10	3	131.57	40.89
4x4	20	4	147	9.8
6x4	20	5	111	58.17
8x4	20	4	115	32.24
10x4	20	8	126.87	29.36

Table 5.5: Number of working Hall bars and their average channel resistances at the dirac point.

As seen in the table, the variance in the dirac voltages is quite high. This could be due to having a lower sample size. But, even for 8 devices measured for the 10 um x 4 um hall bar, a standard deviation of 29.36 is seen. This does suggest that there might be a high variance in the properties of the devices. The hall bars fabricated in the optical modulator dies, go through extra steps such as triton x100 rinse, cladding oxide removal in BHF (1:7) solution, extra water rinsing steps, etc, when compared to the hall bars in section 5.1.1. Therefore, the % of working devices and the high variance in the properties of devices could be due to the effect of process flow on graphene films.

5.2.4. Testing the propagation of light through the waveguides

Now that we have checked that the graphene can be baised to the dirac point, we move onto testing whether light successfully propagates through the waveguides. We use the optical setup shown in the figure.5.21. In the setup, the optical fiber on the left is connected to the light source, which is EXALOS EXS1320-2111 1320 nm wavelength SLED in our case (Nominal light output when directly connected to the detector - 1.4 mW). The optical fiber on the right is connected to the detector, Thorlabs S122C photodiode detector, which is connected to Thorlabs PM100D Optical power and energy meter that reads out the power of the light detected. Further, we see probes that can be used to bias the devices and a microscope which is used to align the fibers with the waveguide.

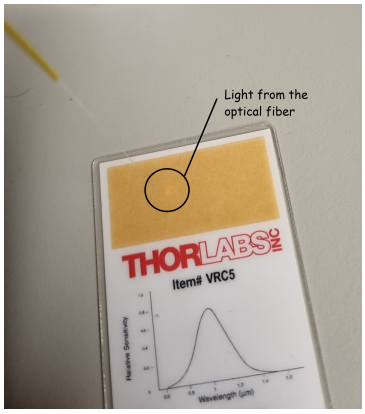


Figure 5.20: Light from the light source directed towards and IR paper

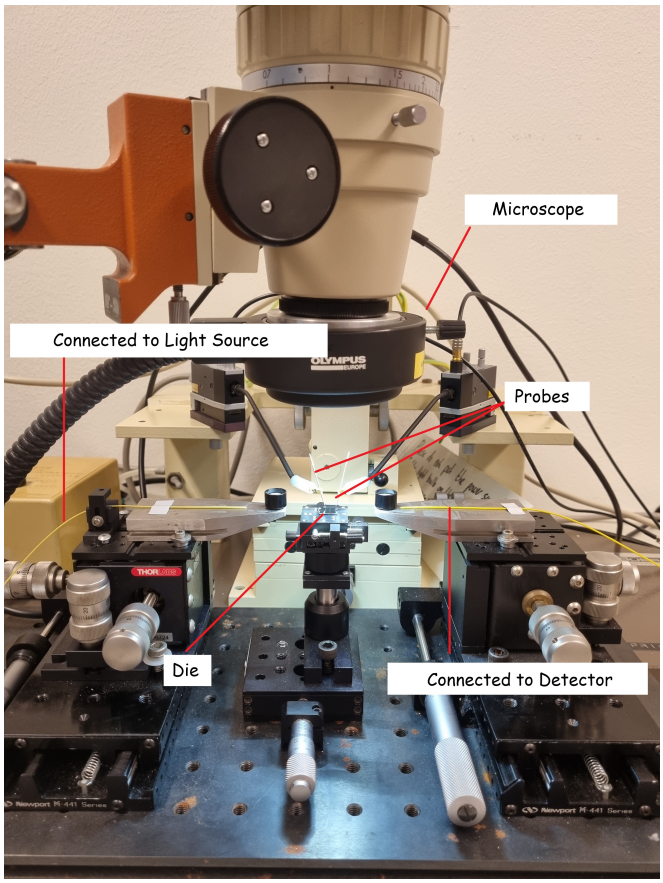


Figure 5.21: The setup used for testing the optical modulators

First, we need to test that the light source is working. This is done by shining the opening of the light source onto an IR paper rated for the working wavelength of the light (1320 nm in our case). This can be seen in the figure. 5.20. Then we need to test if the optical fibers are working. To do this we butt-couple two optical fibers, one connected to the light source and the other connected to the detector, switch on the power supply and measure the light detected at the detector. The butt-coupled configuration can be seen in the figure.5.22 and the detected power can be seen in the table.5.6.

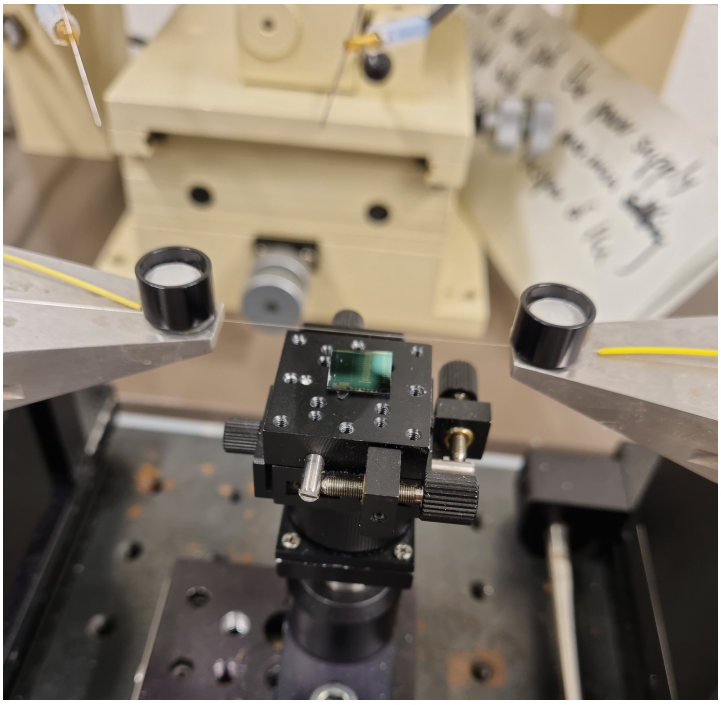


Figure 5.22: Optical fibers that are butt coupled to each other

Configuration number	Type of Setup	Power Measured(W)
Configuration 1 -	Butt coupled fibers	0.6 mW
Configuration 2	Fibers aligned and 2-3 mm away	0.1 uW
Configuration 3	Fibers aligned with the waveguide	0.8uW
Configuration 4	Fibers aligned with a broken waveguide	0.004 uW

Table 5.6: Power measured at the detector for different Setup configurations.

Another configuration where the butt-coupled fibers while still being aligned are moved away from each other for about 2-3 mm distance between one fiber to the other, is tested. This is done to check how close the fibers need to be, such that the light emitted from the fiber connected to the source is picked up by the fiber connected to the detector. This configuration is shown in the figure.5.23 and the power measured in this configuration is shown in the table.5.6. The next configuration is where we align and butt-couple the optical fibers connected to the source and detector, with the waveguide and measure the power detected at the exit of the waveguide. A few waveguidse were tested using this configuration and the average power measured is shown in the table 5.6. Then the last configuration is where we align the fibers with a broken waveguide and measure the power detected at the exit of the broken waveguide. These configurations can be seen in the figure.5.24. The broken waveguide that was tested can be seen in the figure.5.25.The values measured can be seen in table.5.6.
A power of 0.1 uW is observed when the aligned fibers are a few mm away compared to the 0.8 mW measured when they are butt-coupled. This means that measured power drastically falls off as the fibers move away

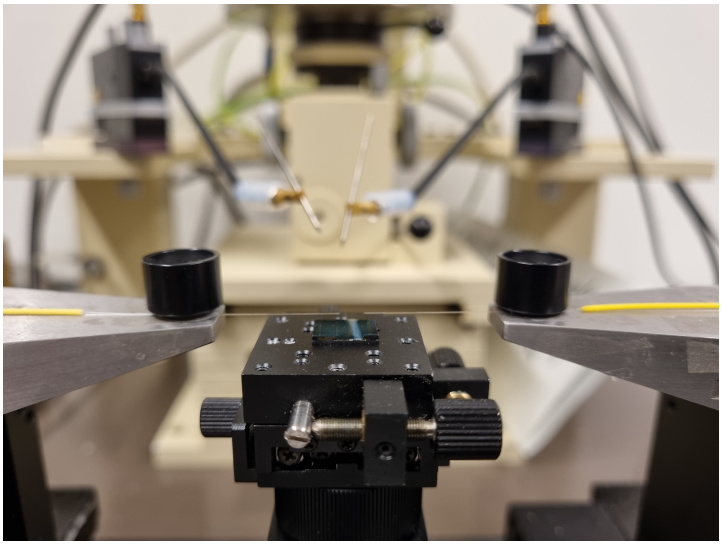


Figure 5.23: Optical fibers that are a few mm away from each other

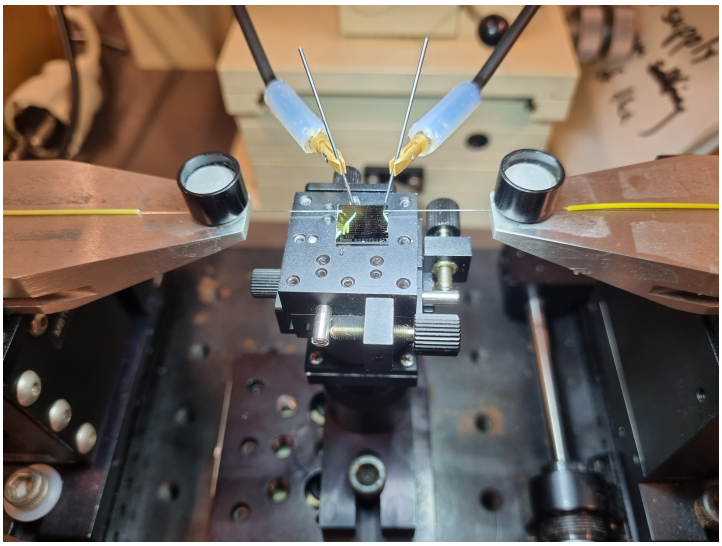


Figure 5.24: Optical fibers that put in the trenches and aligned with the waveguide

from each other. This also means that when the fibers are aligned with the waveguides and they are about 8 mm away from each other, the power detected would probably be from the light propagating through the waveguide. Hence, the 0.8 uW measured when the fibers are aligned with the waveguides, most likely is from the light propagating through the waveguide. The value is about 1000 times smaller than the power measured when the fibers are butt-coupled. There are a few reasons this case could be explained with. Firstly, the core of the waveguide has a diameter of 10um, and our waveguides are only 340 nm thick. So only a fraction of the light coming from the fibers enters the waveguide. Secondly, the fiber edges may not be cleaved properly and this might affect the coupling between the fiber and the waveguide. Thirdly, some of the light may be lost through the tapers due to the angle being too harsh. Fourthly, some of the light could be absorbed by the silicon waveguide itself. Lastly, there might be some reflections within the waveguide or to be more specific, light reflecting back inside the waveguide, instead of exiting it. Why this happens is explained below.

Figure 5.26 shows the different path that light takes within the waveguide. First, lets define the interfaces when refraction/reflection of light occurs. "A" is the interface between the silicon waveguide and the bulk oxide. "B" is the interface between the silicon waveguide and the cladding oxide and "C" is the interface between the cladding oxide and air. Now lets define the different angles seen in the figure. θ_0 is the angle of incidence at interface A. θ_1 and θ_2 are the angle of incidence and refraction for interface B. θ_3 is the angle

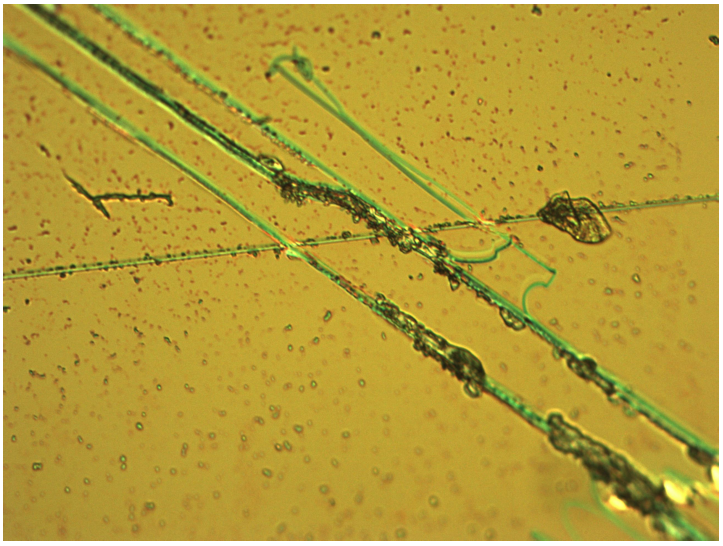


Figure 5.25: The broken waveguide that was measured in configuration 4

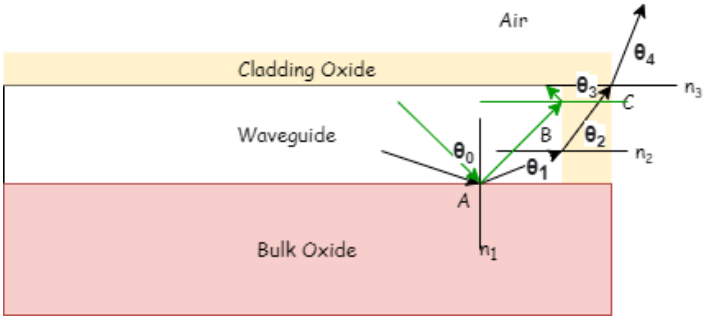


Figure 5.26: Schematic showing different paths of light in the waveguide

of incidence for interface C. When light enters the waveguide, different rays enter with a different incidence angle. Due to which the angle at which they reach the exit of the waveguide is not the same for all the light rays. For light to successfully exit the waveguide(the black ray), θ_3 needs to be less than the critical angle of interface C, i.e 40 degrees. θ_1 needs to be less than the critical angle of interface B, i.e 26 degrees. And θ_0 needs to be greater than the critical angle of interface A, i.e 26 degrees. For all these conditions to satisfy θ_0 is calculated to be between 73.4 degrees and 90 degrees. If θ_0 is less than 73.4 degrees, the light rays either get reflected back at interface B or C depending on the angle. Note that the critical angles used above are calculated using Snell's now. Since only a small range of angles would result in the light exiting the waveguide, majority of the light enterting the waveguide is lost due to reflections within the waveguide. This could also explain the low magnitude of light detected at the exit of the waveguide.

All these factors can add up, such that only a fraction of light emitted by the source is detected at the detector. To further support this claim, the power measured when a broken waveguide is measured is only about 0.004 uW. Which means majority of the light measured in configuration 3 is from the light propagating through the waveguide. Therefore, we can conclude that the waveguides ,although not perfect, are still working as intended.

5.2.5. Testing the Optical Modulator as a whole

In section 5.2.3, we have discussed how we can bias the graphene patch to reach the dirac point where the Pauli-blocking happens and in section 5.2.4, we have seen how light can successfully propagate through the waveguides. So, if we pass light through the waveguides and simultaneously bias the graphene on the optical modulator device to the dirac point, theoretically we should be able to absorb light and notice a change in light power detected when the biasing is at the dirac voltage and when its not. But, this is easier said than

done.

As we mentioned in section 5.2.2, the resistivity exhibited by the silicon waveguides is in the order of a few hundreds of giga ohms. This prevents us from biasing the graphene from the top gate, due to the poor conductance of the waveguide. Although, as discussed in 5.2.3, the graphene can be biased through the back gate, which was done then using the Cascade Microtech measurement tool. But, based on the current available measurement tools, it is not possible to bias the back gate of the die whilst it's in the optical setup, likewise it's not possible to use the optical setup while the wafer is being biased through the back gate. Therefore, for now, the optical modulator cannot be tested as a whole but only parts of it can be tested seperately. It is to be noted that, there was a hinderence while the testing of the propagation of light through the waveguides due to deposits of gold around the entrance and exit of the waveguide. Due to this, one of the processed wafers had the gold on it etch away using the method shown in section 4.3.6, such that it can be used for waveguide testing.

6

Conclusion

Graphene is a really interesting material that exhibits excellent properties and is touted to be the next big thing, not just in the world of electronics, but in many other fields. For this to be realised, reliable ways to manufacture and transfer wafer-scale graphene at a large scale, need to be developed. Applied Nano-Layers (ANL) is one such company that is trying to develop a reliable method to fabricate and transfer wafer-scale mono-layer graphene. The thing with graphene however is that, the properties of graphene films fabricated change with the fabrication and transfer method used [35]. Therefore, this thesis focuses on the analysing the properties and the behaviour of the monolayer graphene fabricated by ANL.

For this thesis, we are particularly interested in the electrical properties such as the resistivity, dirac voltage and mobility. And also in the optical behaviour of graphene, where the ability of graphene to absorb light at the dirac voltage, is analysed. The approach taken to extensively analyze the above said properties/behaviour of graphene, the results obtained and their conclusion is discussed below.

For the electrical properties analysis, firstly we develop and optimize a clean-room compatible process flow for fabricating Graphene Hall devices with differing dimensions. Secondly, we use the optimized process flow to successfully fabricate working graphene hall devices. 12 different dimensional devices were fabricated and measured. Lastly, the hall devices are extensively measured for the channel resistance and the dirac voltage. A total of 800 devices were measured out of which 468 devices were working as intended. The average channel resistance measured for the hall device with the graphene patch dimensions of 2 um x 2 um at the dirac point was calculated to be about 6.74 kΩ. Furthermore, the calculated average channel resistance for the remaining devices follow the relation given in equation 5.1 as expected. Similarly, the average dirac voltage for each device is calculated. Unlike the channel resistance, the dirac voltage for the graphene patches that went through the same process steps should roughly be equal or close together. And as expected, the dirac voltage for different graphene hall devices, is roughly the same, i.e 73 ∓ 3 V.

Now, using the channel resistance the resistivity of the graphene films is calculated. Followed by the calculation of the mobility of the graphene films, using the Drude mobility equation. Similar to the dirac voltage, resistivity and mobility of the device are independent of the dimensions of the graphene patches and should be roughly equal for graphene films that went through the same processing steps. As expected, the calculated average mobility and average resistivity were roughly equal for all the devices. An average mobility of 1330 ∓ 300 cm^2/Vs and an average resistivity of 2.1 ∓ 0.4 kΩ was observed. Now that we have measured the mobility, resistivity and dirac voltage for the graphene films, we can conclude that we successfully analysed the electrical properties. The voltage shift caused by the charge trapped in the oxide was also calculated to be 1.5 V, which accounted to 1 to 2% of the dirac voltage. So it can be concluded that the effect of trapped charge on the measurements is negligible.

For analysing the optical properties, firstly we design and optimize the waveguide to be used in the optical modulator, such that it is compatible with the parameters and components we want to work with. By parameters and components we mean, the wavelength of the light source to be used and the dimensions of the substrate that is to be used for fabricating the device. Different waveguide structures were simulated in

COMSOL and BeamLab. And waveguides of width 1 um to 4 um with steps of 0.5 um, and cladding thickness of 20 nm was decided for the optical modulator fabrication. The decision was made by assessing the amount of evanescent field observed on the air-cladding interface. Secondly, the waveguide design is implemented on a mask along with the optical modulator design. Thirdly, a cleanroom compatible process flow for the fabrication of theoptical modulator is developed and optimized. Fourthly, the optimized process flow is followed and the optical modulators are fabricated. About 8 different optical modulators per die, with varying waveguide dimensions were fabricated for testing. Lastly, the fabricated optical modulator is tested if it works as intended.

To test the optical modulator,

1. We couple light of known magnitude into the waveguide.

2. Absorb some of the light propagating through the waveguide by biasing the graphene thats sitting on top of the waveguide.

3. Detect the light reaching the end of the waveguide and estimate the amount of light absorbed by graphene.

A light of the magnitude 0.6 uW was measured when coupled with optical fibers connected to the source and detector compared to the 0.0006 uW measured when a broken waveguide is coupled. This concludes that light does propagate through the waveguide successfully. Now, to stop absorbing the light passing through the waveguide, the graphene needs to be biased to the dirac point. Both the top gate and back gate configurations were tested. Unfortunately the top gate configuration couldn't work due to the high resistivity exhibited by the top silicon substrate. But using the back gate configuration, graphene could be baised to the dirac point which was around 20V. To test the optical modulator as a whole, the light propagation and graphene biasing need to happen simulataneously. However, based on the available measurement tools back gate biasing the optical modulator while using the optical setup to couple light into the waveguides, is not currently feasible. Also, the presence of silicon waveguide between the graphene and the oxide in the optical modulators, might cause complications in the back gate biasing. But theoretically, the optical modulator should work if we combine the light propagation and the graphene biasing. Some solutions to workaround the limitation mentioned above is discussed in section 6.2.

So, lets see if we answered the sub-questions framed in chapter -1.

- A working process flow was designed for the graphene hall bars and back gate biased electro-absorption optical modulator. However, slight modifications could be made to the process flow designed for the optical modulator, such that it works for top gate biasing.

- The voltage shift caused by the charge trapped in the oxide was 1.5 V which accounted to 1 to 2% of the dirac voltage. Therefore, the effect is considered to be negligible.

- An optimized structure for a wafer-scale silicon waveguide for working waveglength of 1320 nm was designed using BeamLab and COMSOL.

- Albeit lot of losses, a measurable amount of light successfully propagates through the silicon waveguide.

- Light propagation and graphene modulation (biasing) were successfully achieved for the modulator. However, due to a few complications, light propagation and graphene modulation cannot be done simultaneously to test optical modulation.

- The effect of process flow on graphene and graphene devices was confirmed by comparing the % of working devices and the variance/change in properties of the device that went through two different process flows. The two process flows being 4.3 and 4.4. And based on the results (60% working for Hall bars fabrication and 30% for optical modulator fabrication) it can be concluded that, graphene gets more damaged as the number of process steps it goes though, increases. Likewise, the number of graphene devices working also decreases as the number of processing steps increases.

6.1. Recommendations and Future

Firstly, it is to be noted that, during the fabrication of the devices, the optimization of the process flow is done simultaneously with the process steps of the devices. Certain steps in the process flow are tested on several test wafers, before actually implementing them on the main device wafers. The solutions to the problems faced during the fabrication that needed to be fixed/optimized, were also discussed in this master thesis for future references.

In this thesis, the electrical properties of graphene were successfully analyzed. Whereas, the optical behaviour wasn't fully analyzed due to the limitation of not being able to back gate bias the graphene and couple light into waveguide simultaneously. To overcome this limitation, a small portable chuck that can fit in the optical setup, can be used to bias the die through the back gate or a PCB circuit can be used to bond the back side of the die to an interconnect which can then be used to apply a bias. However as mentioned above, the presence of silicon waveguides between the bulk oxide and the graphene might cause complications for full back gate biasing.

For the top gate biasing of the modulator, we saw that the problem arised from the resistance of the top silicon substrate being too high. To fix this, the resistance of the substrate has to be decreased, so that its conductance increases. This can be done using certain techniques. One such technique is to dope the substrate such that its resistance decreases. Doping the substrate can be done with multiple ways. One way is just directly using Ion Implantation. This could however damage the lattice structure of the substrate. Another way would be growing epitaxial Si of higher doping concentration, on the top silicon substrate and then annealing the wafer such that the doping becomes uniform in the substrate and the overall doping is increased. This method could also cause problems, as the height of the waveguide structure would change and this might affect the propagation of light through the waveguide.

Also, better methods to clean the graphene structures could be implemented such that multiple peaks during measurements aren't formed due to residues on the wafer. These methods could include overnight acetone cleaning of the wafers(since polymer residues dissolve slowly), annealing the graphene to remove defects, etc. Furthermore, other properties of graphene could also be tested. The chemical solubility of different gases can be tested by making gas sensors or the mechanical tensile strength of graphene could be tested by analyzing the fracture behaviour of graphene composites, etc.

Furthermore, improvements to the waveguides in the optical modualtor need to be made. Improvements here can mean further optimizing the structure or improving the process flow for fabricating the waveguides to mitigate the losses in the waveguide. In the waveguides we fabricated, cladding oxide was also present on exit of the waveguide which resulted in loss of light due to reflections within the waveguides. Using anti-reflecting coating on the exit sidewall, before oxidizing the waveguide can prevent the formation of oxide on the exit sidewalls. Optimizing the process flow, such that the trenches are etched after oxidizing the waveguide, could also help with the prevention of cladding oxide formation on the exit-sidewall. Theorectically, this could improve the amount of light detected at the exit of the waveguide.

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Appendices

BeamLab Simulations

Here, all the simulations done in BeamLab during the designing of the optical modulator, which weren't shown in chapter 3 are shown.

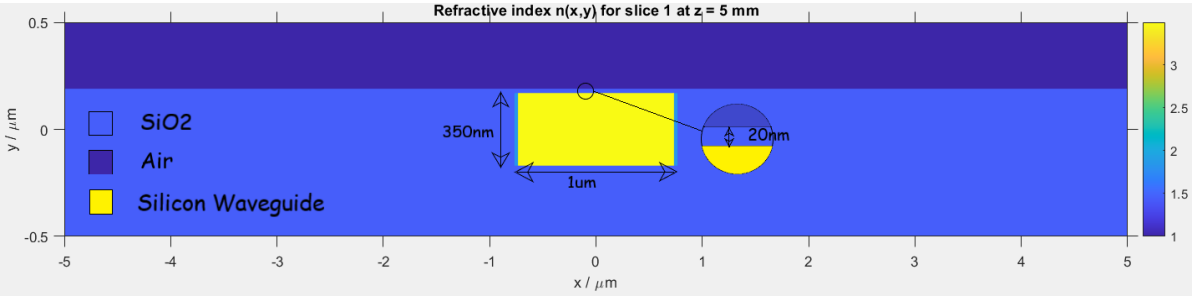

Figure 6.1: Input for waveguide simulations for a waveguide width of 1.5 um

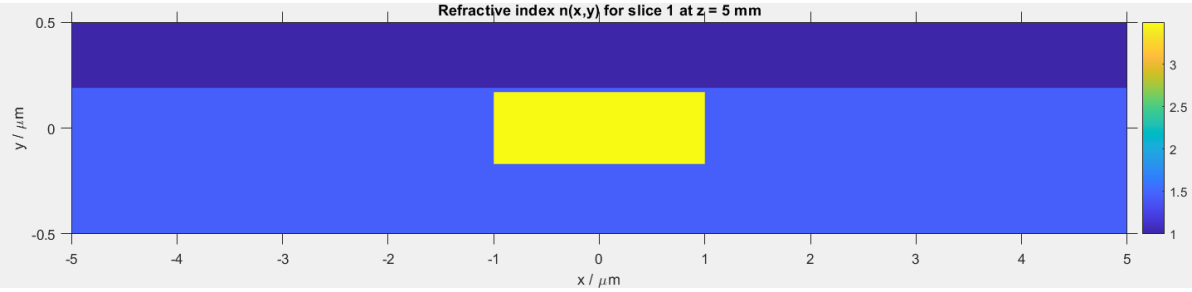

Figure 6.2: Input for waveguide simulations for a waveguide width of 2 um

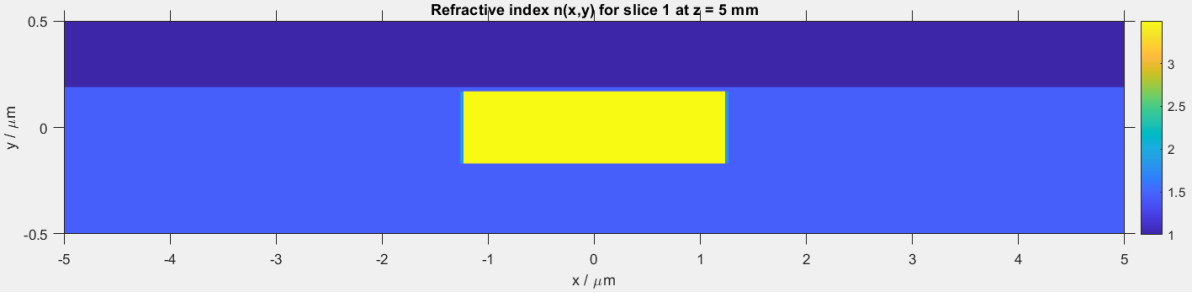

Figure 6.3: Input for waveguide simulations for a waveguide width of 2.5 um

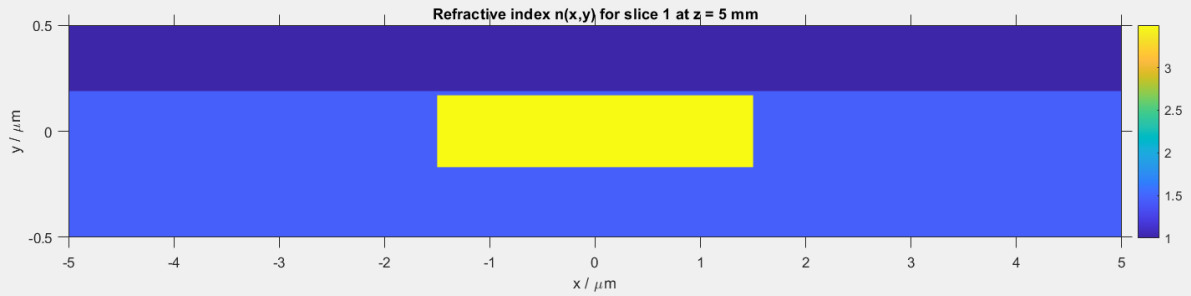

Figure 6.4: Input for waveguide simulations for a waveguide width of 3 um

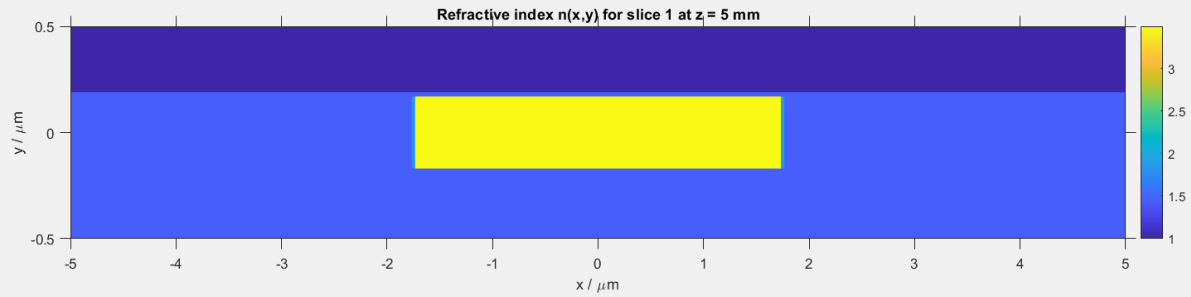

Figure 6.5: Input for waveguide simulations for a waveguide width of 3.5 um

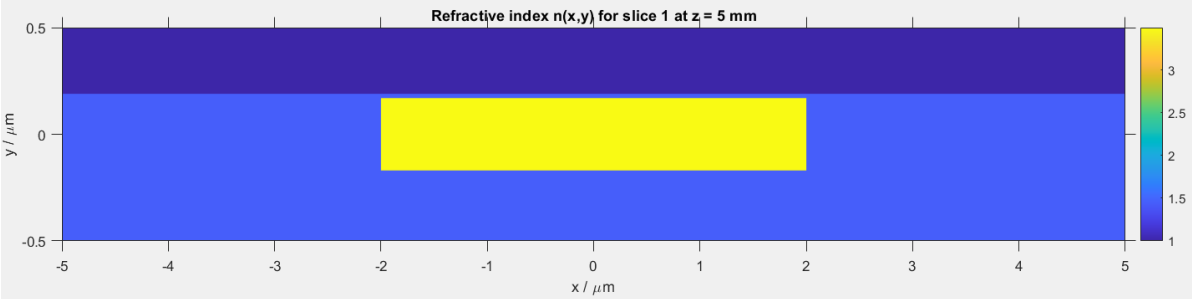

Figure 6.6: Input for waveguide simulations for a waveguide width of 4 um

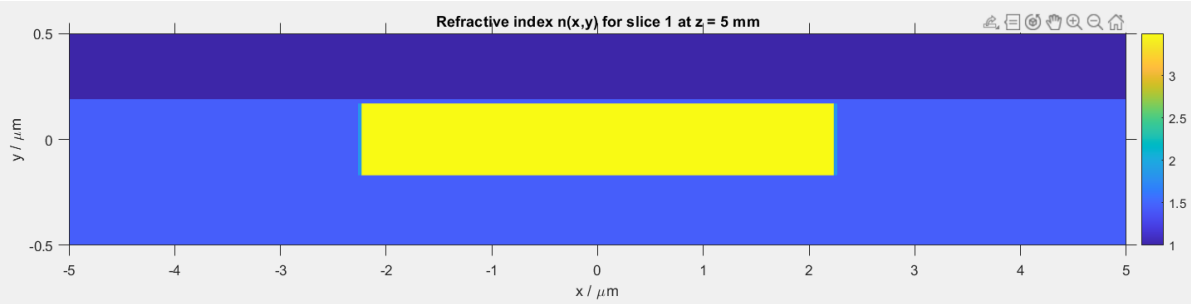

Figure 6.7: Input for waveguide simulations for a waveguide width of 4.5 um

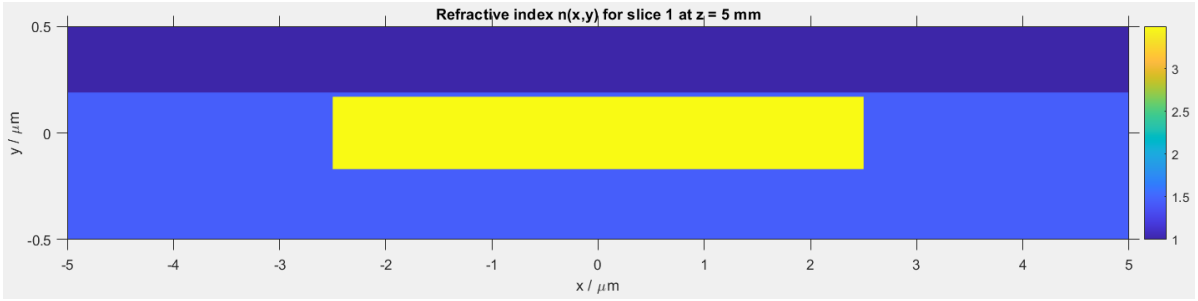

Figure 6.8: Input for waveguide simulations for a waveguide width of 5 um

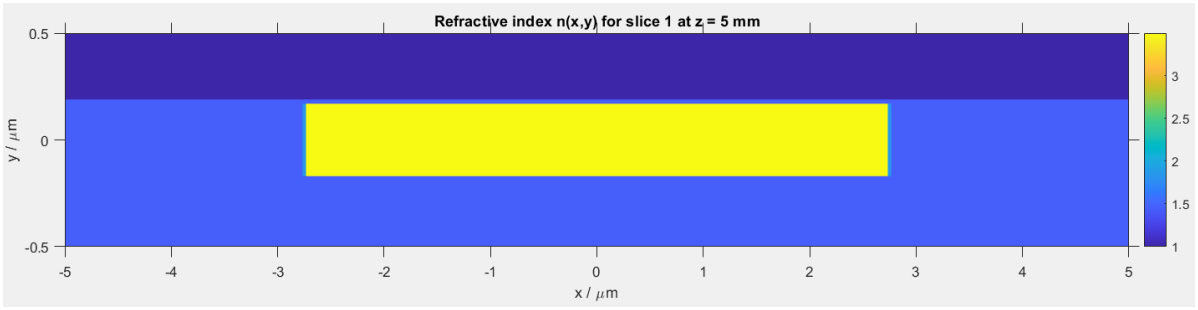

Figure 6.9: Input for waveguide simulations for a waveguide width of 5.5 um

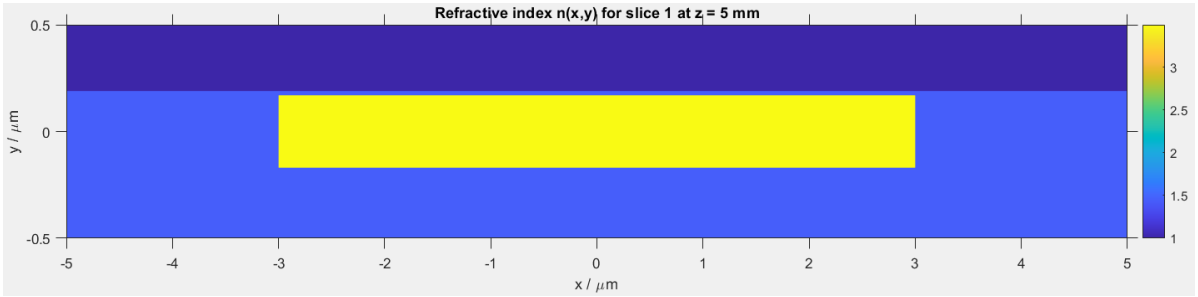

Figure 6.10: Input for waveguide simulations for a waveguide width of 6 um

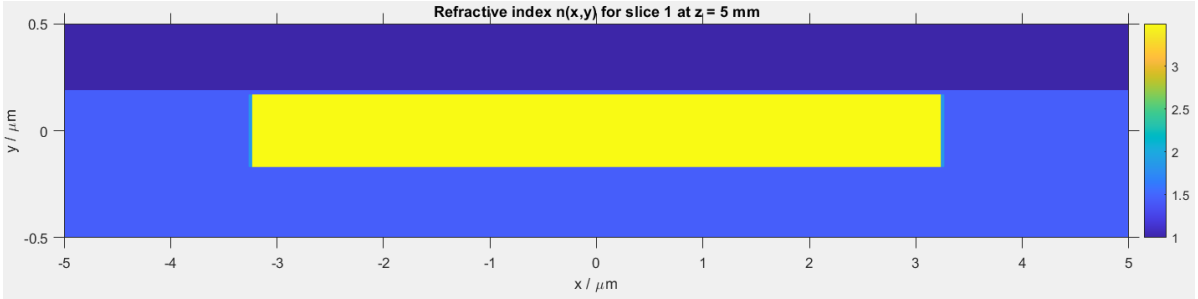

Figure 6.11: Input for waveguide simulations for a waveguide width of 6.5 um

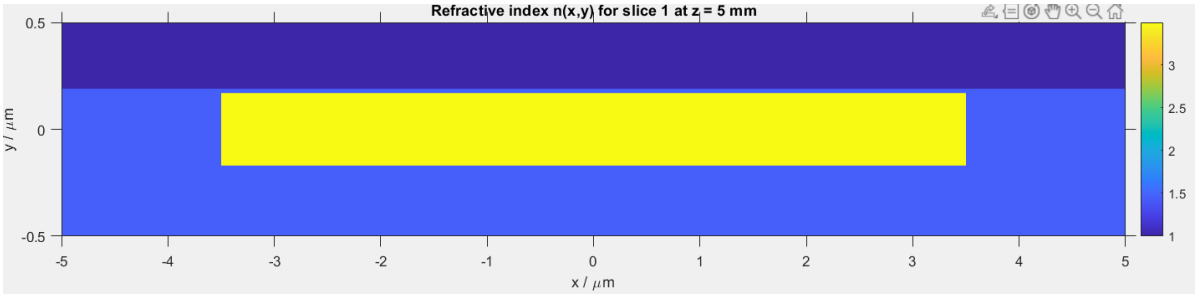

Figure 6.12: Input for waveguide simulations for a waveguide width of 7 um

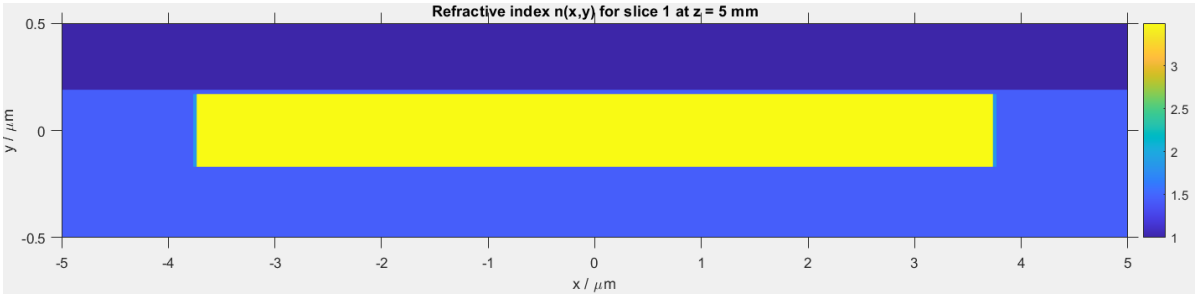

Figure 6.13: Input for waveguide simulations for a waveguide width of 7.5 um

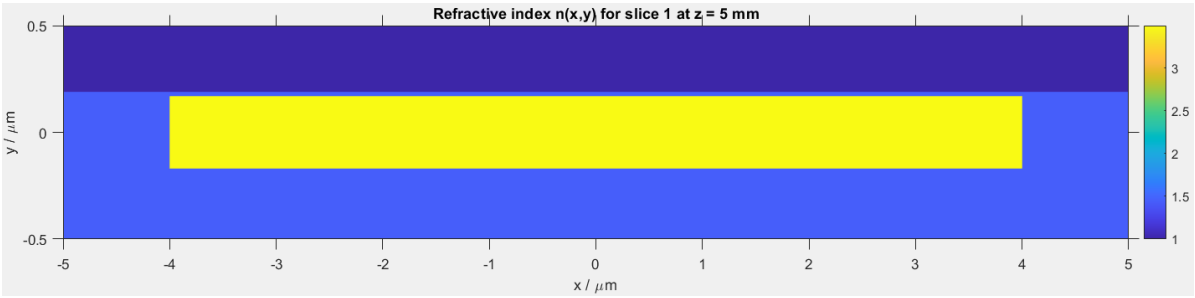

Figure 6.14: Input for waveguide simulations for a waveguide width of 8 um

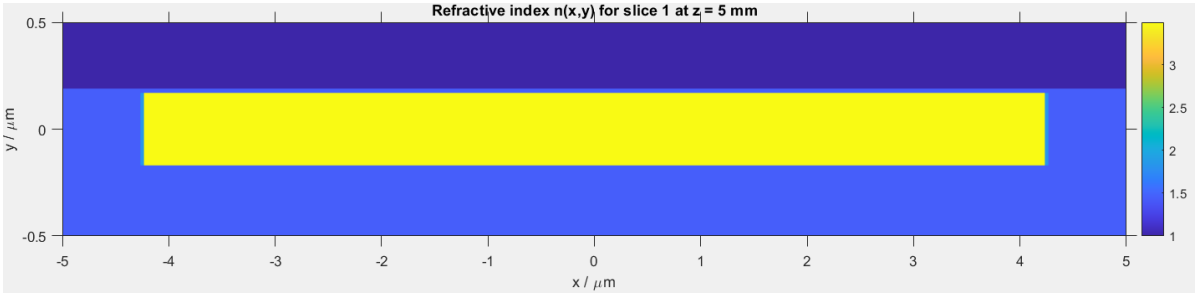

Figure 6.15: Input for waveguide simulations for a waveguide width of 8.5 um

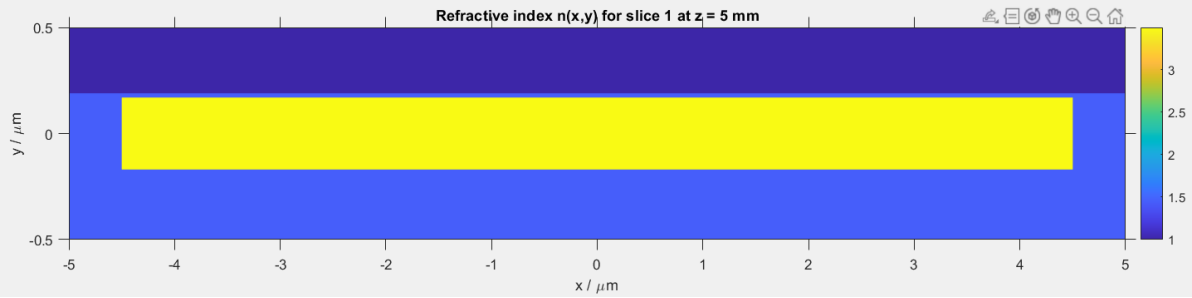

Figure 6.16: Input for waveguide simulations for a waveguide width of 9 um

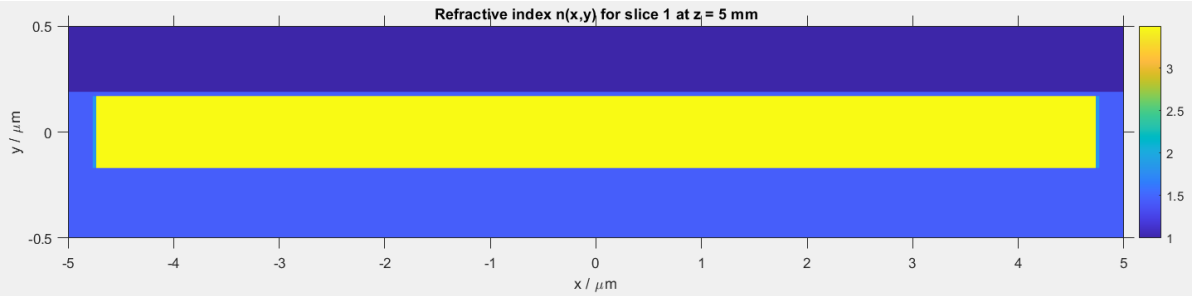

Figure 6.17: Input for waveguide simulations for a waveguide width of 9.5 um

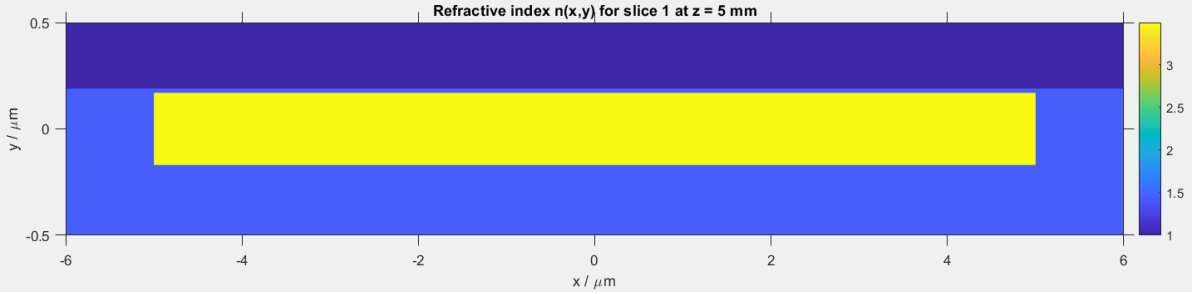

Figure 6.18: Input for waveguide simulations for a waveguide width of 10 um

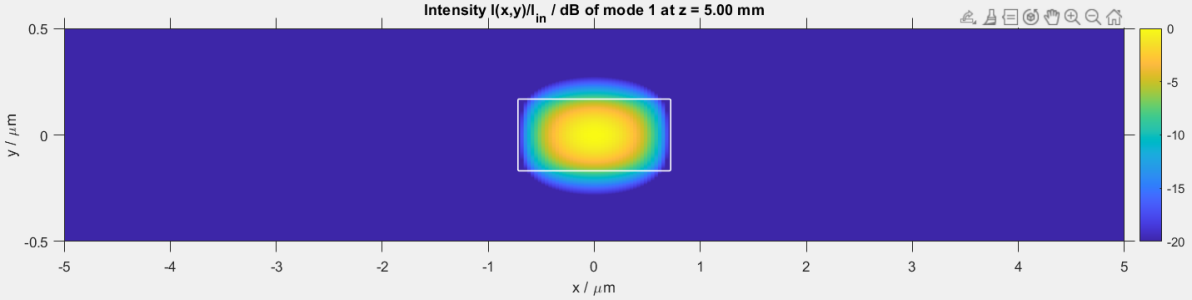

Figure 6.19: Electric field intensity simulations for a waveguide width of 1.5 um

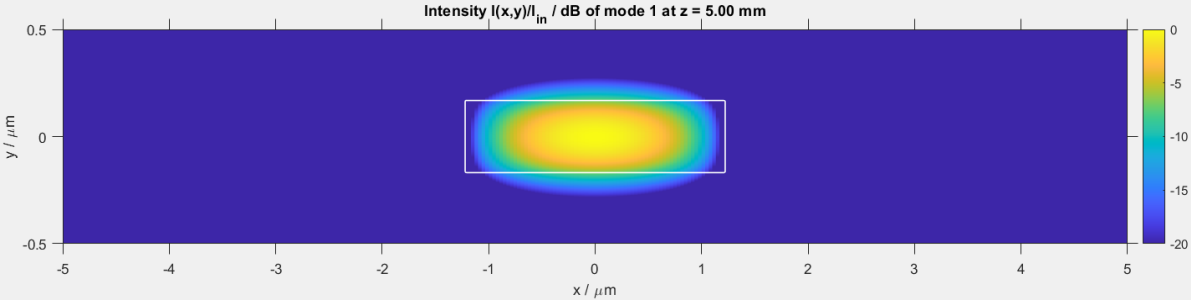

Figure 6.20: Electric field intensity simulations for a waveguide width of 2.5 um

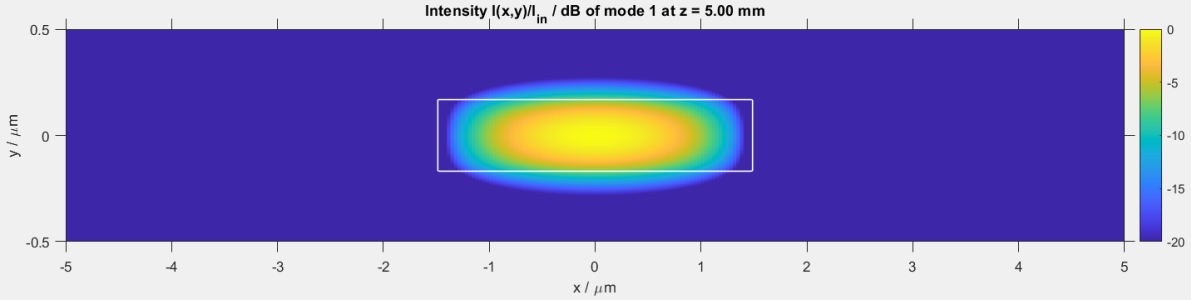

Figure 6.21: Electric field intensity simulations for a waveguide width of 3 um

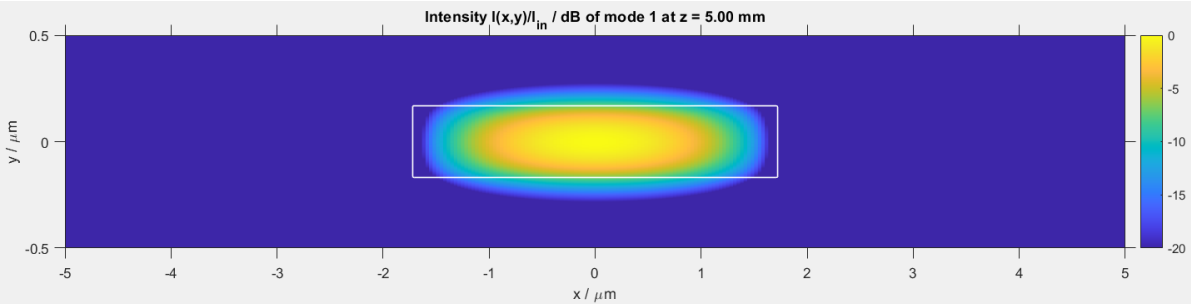

Figure 6.22: Electric field intensity simulations for a waveguide width of 3.5 um

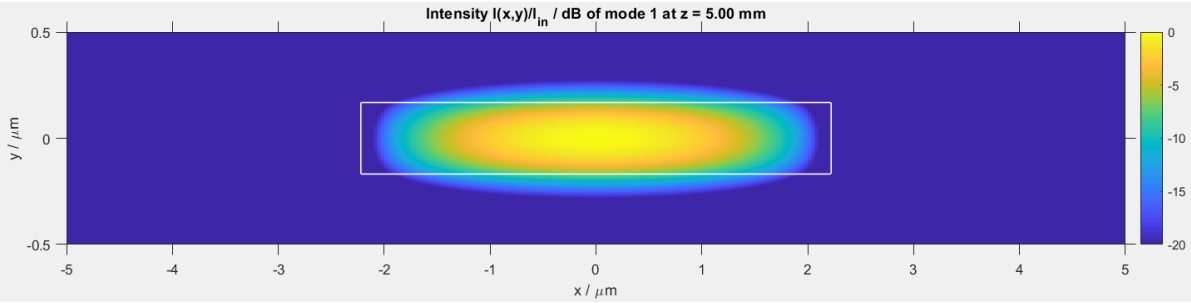

Figure 6.23: Electric field intensity simulations for a waveguide width of 4.5 um

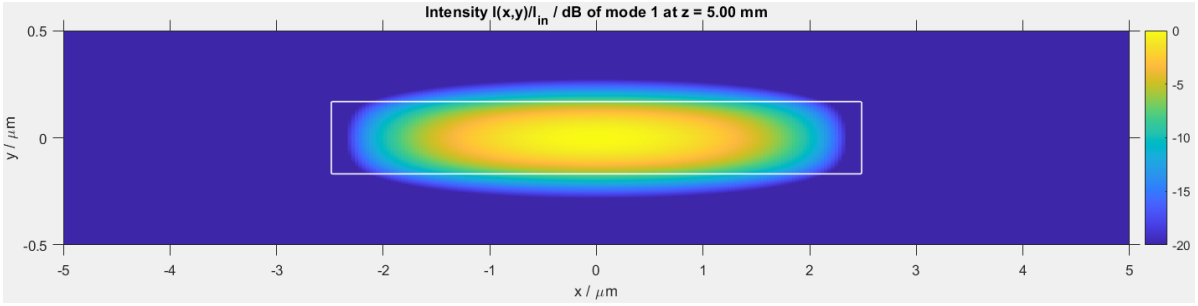

Figure 6.24: Electric field intensity simulations for a waveguide width of 5 um

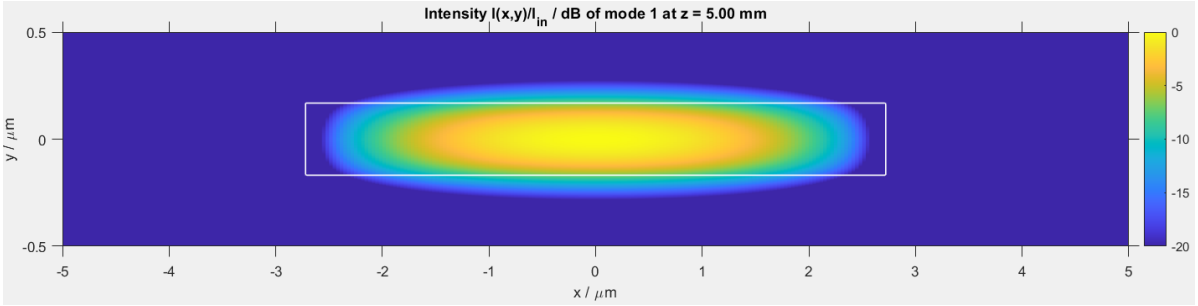

Figure 6.25: Electric field intensity simulations for a waveguide width of 5.5 um

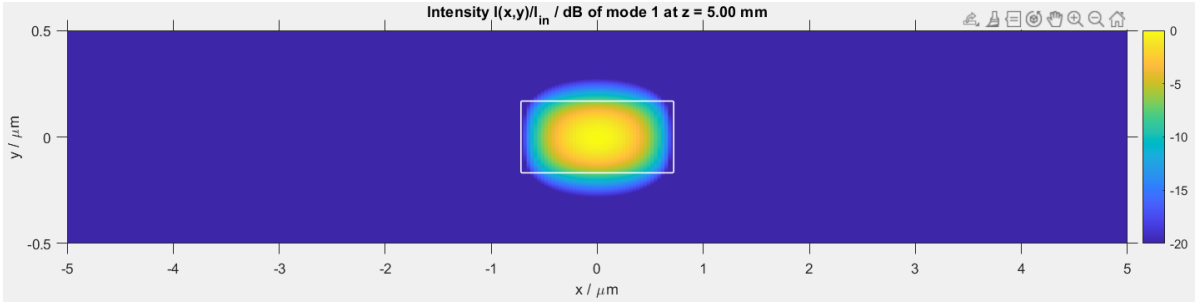

Figure 6.26: Electric field intensity simulations for a waveguide width of 1.5 um

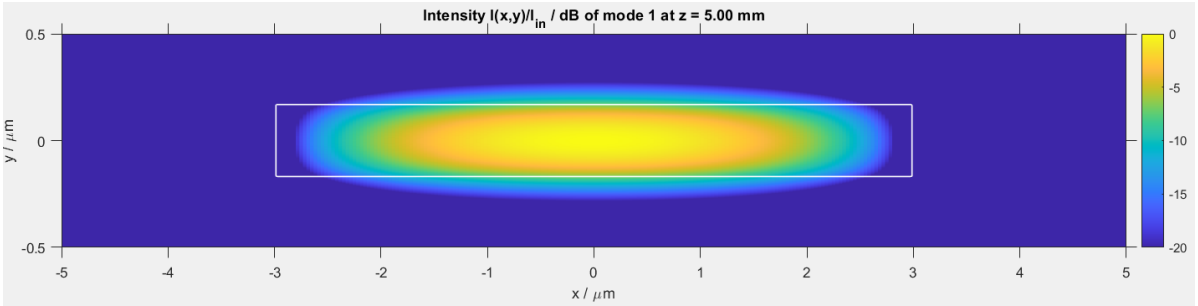

Figure 6.27: Electric field intensity simulations for a waveguide width of 6 um

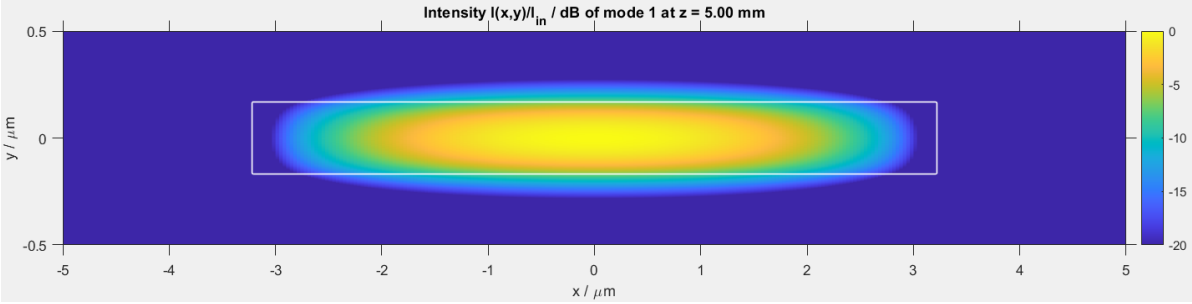

Figure 6.28: Electric field intensity simulations for a waveguide width of 6.5 um

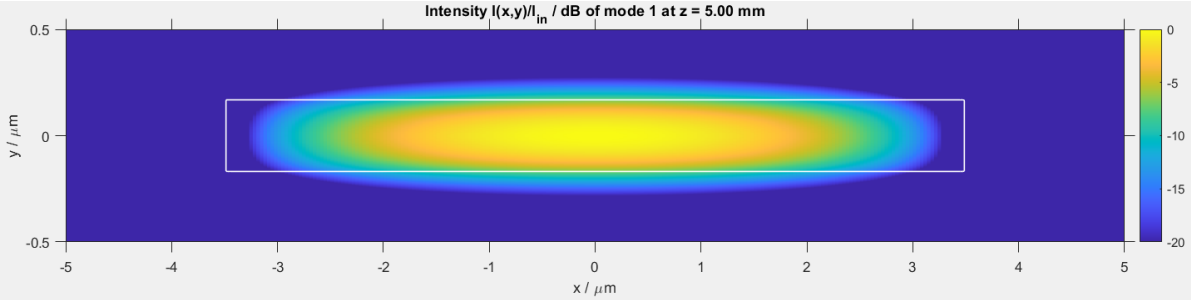

Figure 6.29: Electric field intensity simulations for a waveguide width of 7 um

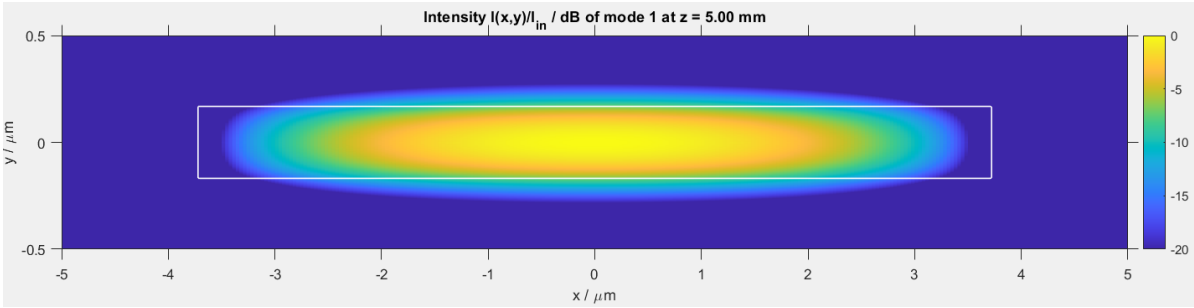

Figure 6.30: Electric field intensity simulations for a waveguide width of 7.5 um

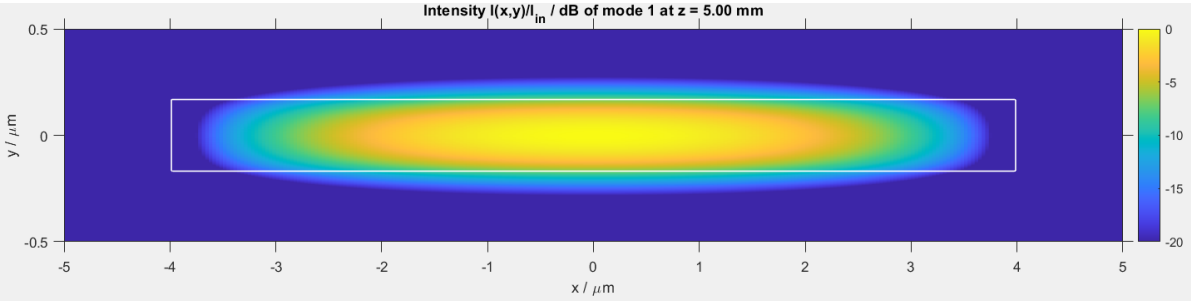

Figure 6.31: Electric field intensity simulations for a waveguide width of 8 um

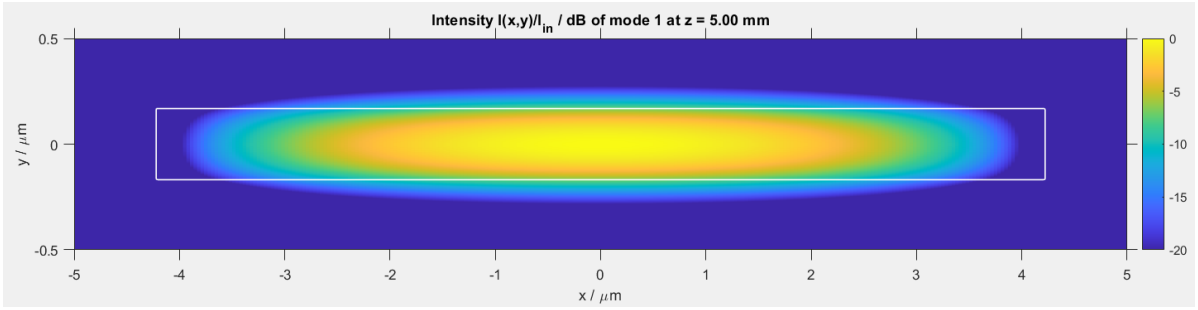

Figure 6.32: Electric field intensity simulations for a waveguide width of 8.5 um

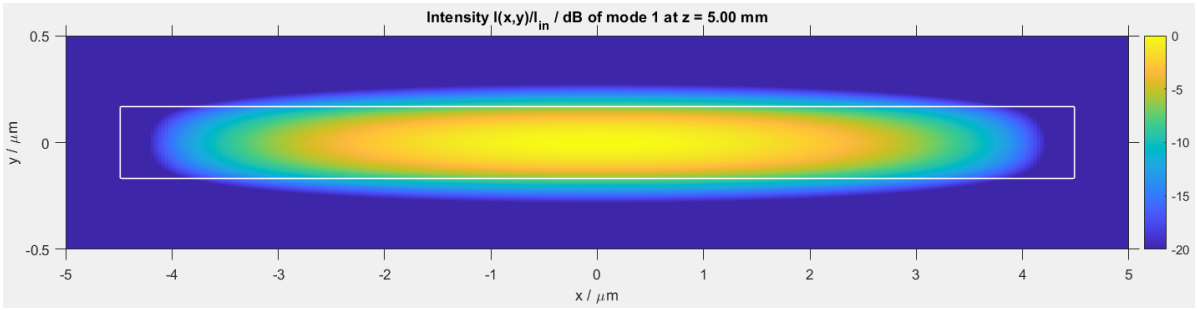

Figure 6.33: Electric field intensity simulations for a waveguide width of 9 um

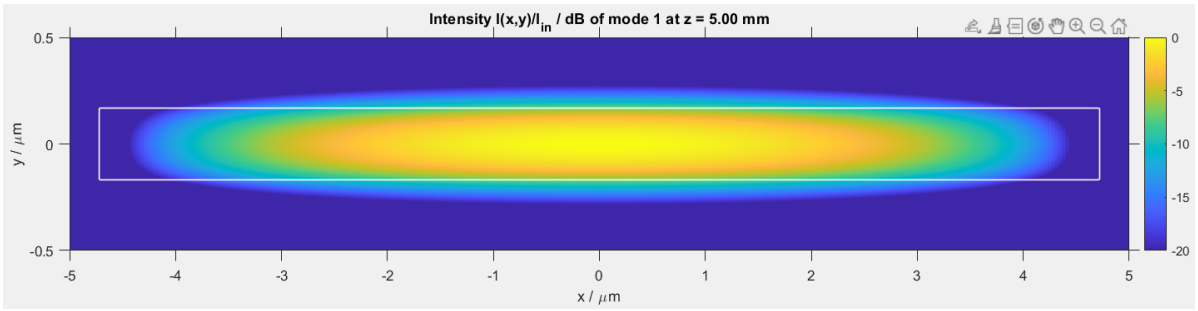

Figure 6.34: Electric field intensity simulations for a waveguide width of 9.5 um

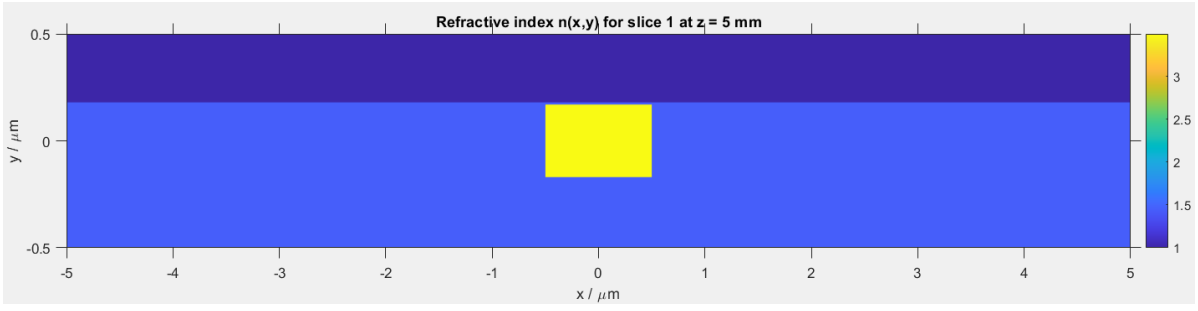

Figure 6.35: Input for waveguide simulations for a cladding thickness of 5 nm

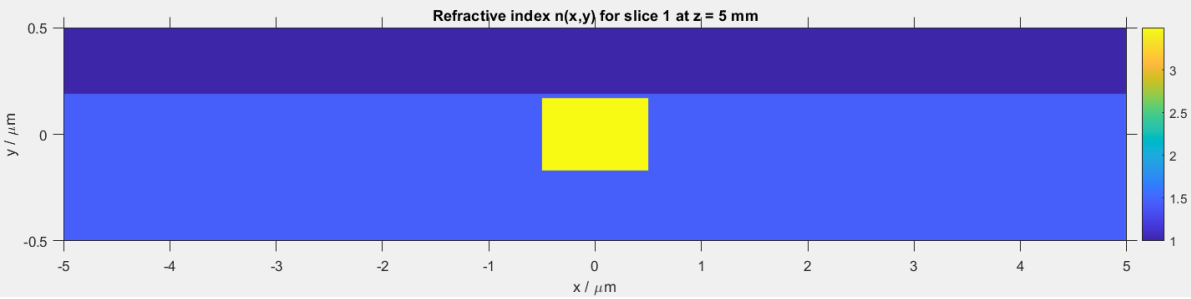

Figure 6.36: Input for waveguide simulations for a cladding thickness of 20 nm

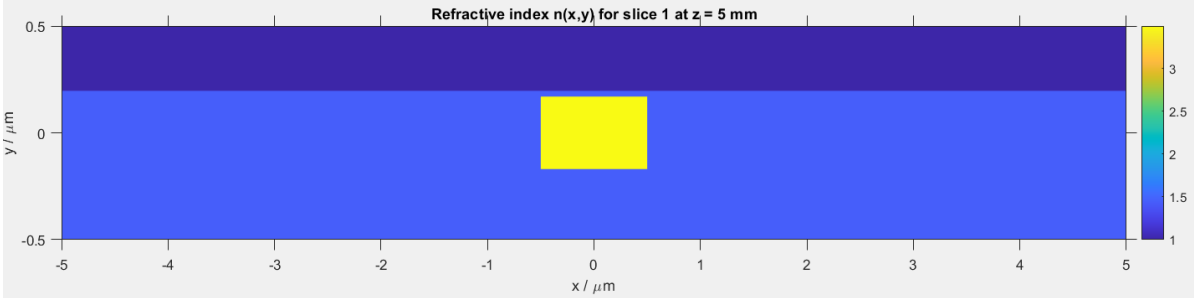

Figure 6.37: Input for waveguide simulations for a cladding thickness of 25 nm

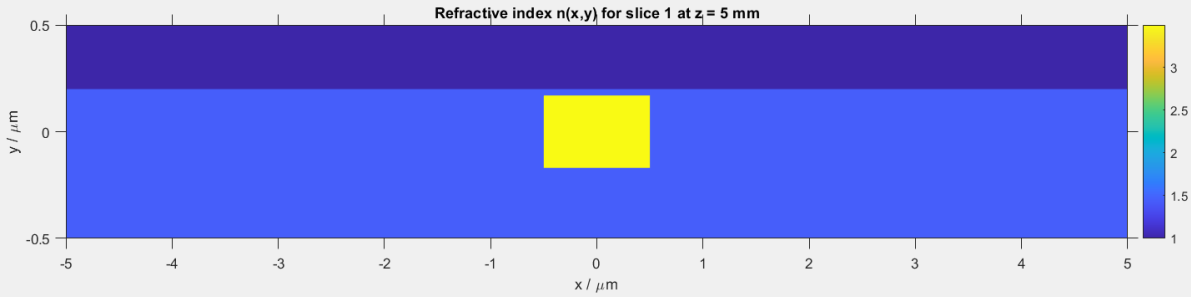

Figure 6.38: Input for waveguide simulations for a cladding thickness of 30 nm

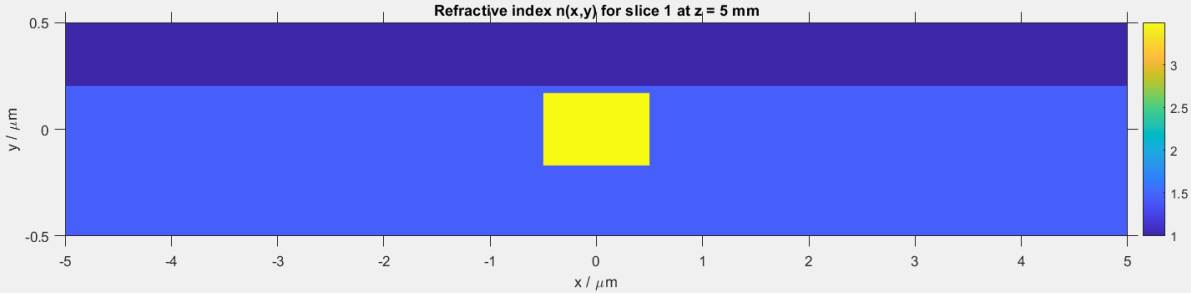

Figure 6.39: Input for waveguide simulations for a cladding thickness of 35 nm

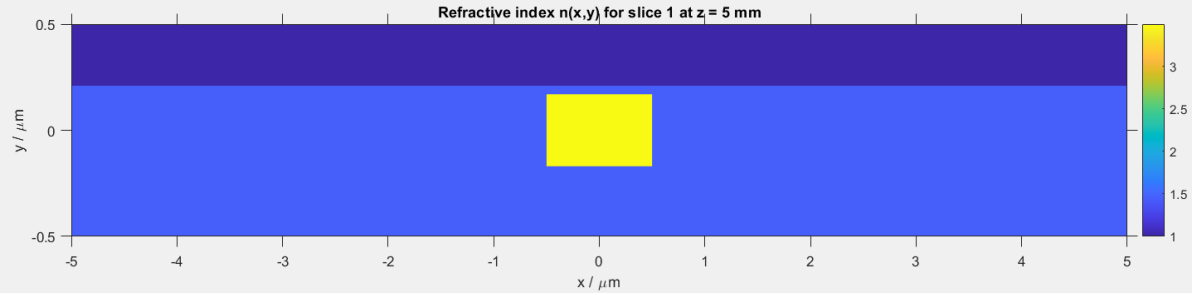

Figure 6.40: Input for waveguide simulations for a cladding thickness of 40 nm

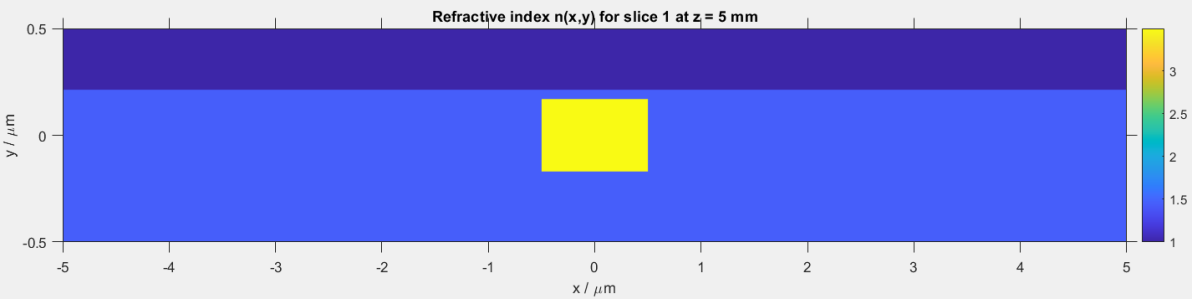

Figure 6.41: Input for waveguide simulations for a cladding thickness of 45 nm

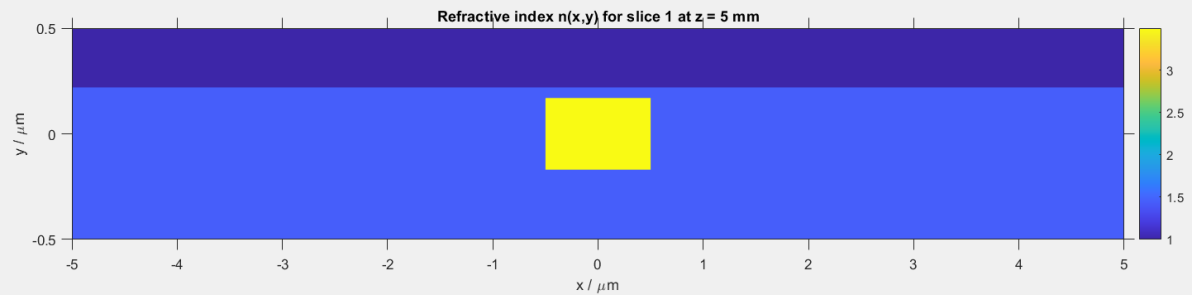

Figure 6.42: Input for waveguide simulations for a cladding thickness of 50 nm

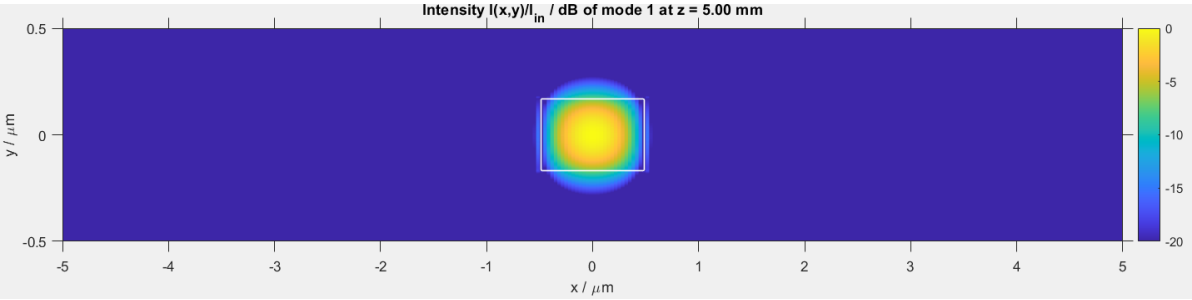

Figure 6.43: Electric field intensity simulations for a cladding thickness of 5 nm

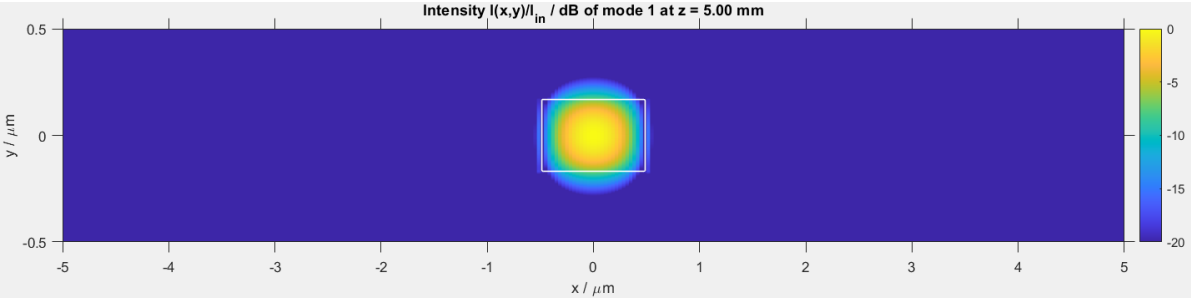

Figure 6.44: Electric field intensity simulations for a cladding thickness of 15 nm

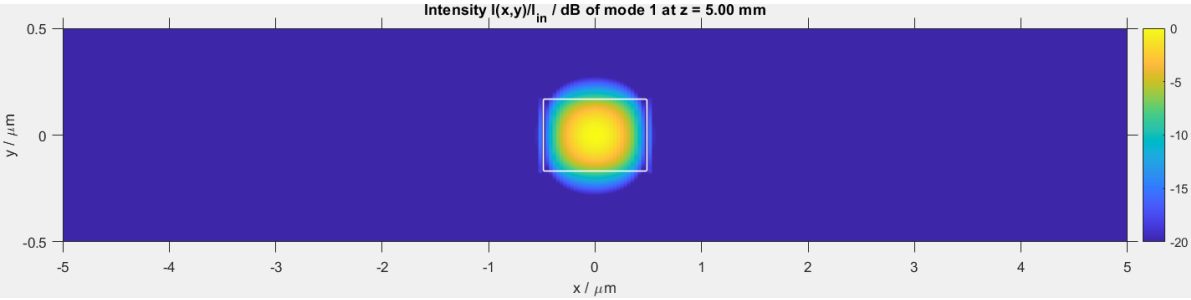

Figure 6.45: Electric field intensity simulations for a cladding thickness of 25 nm

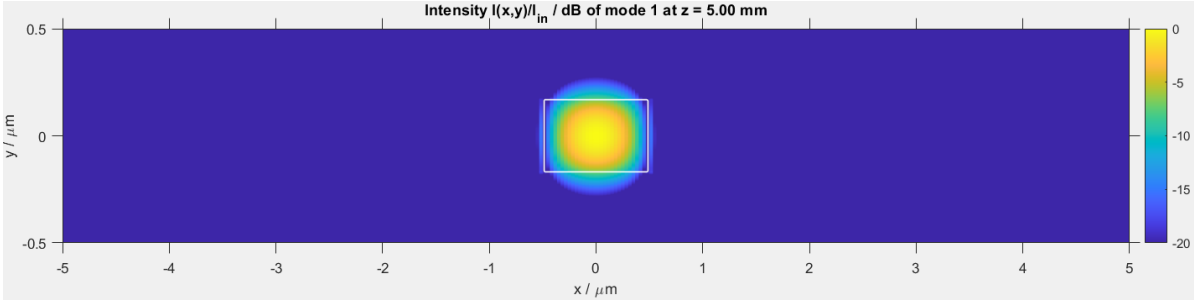

Figure 6.46: Electric field intensity simulations for a cladding thickness of 30 nm

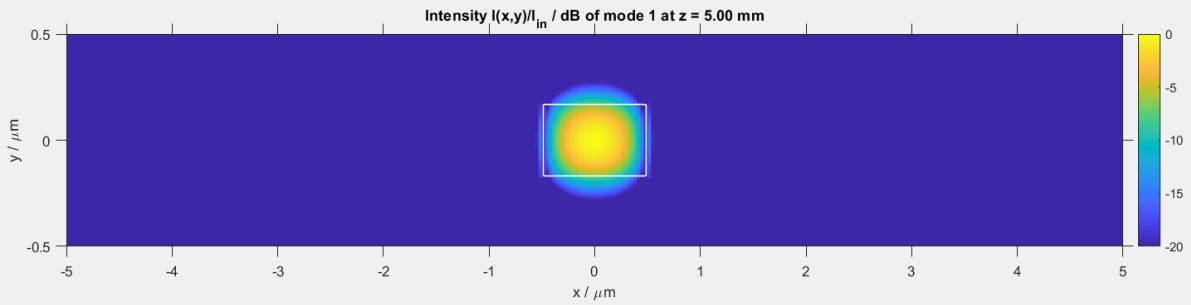

Figure 6.47: Electric field intensity simulations for a cladding thickness of 35 nm

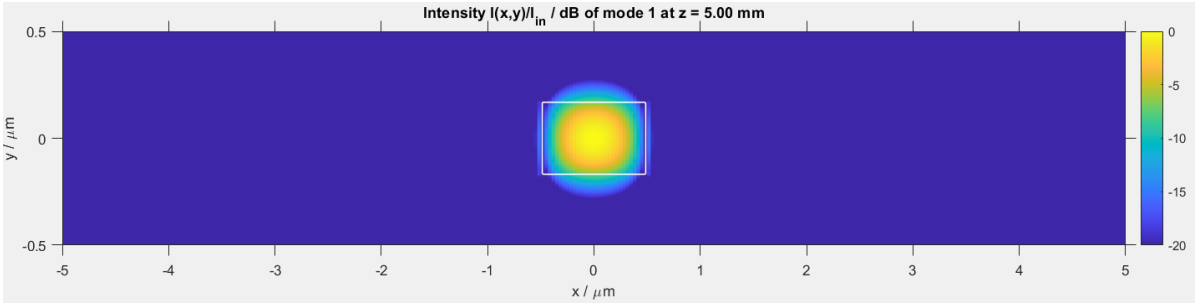

Figure 6.48: Electric field intensity simulations for a cladding thickness of 40 nm

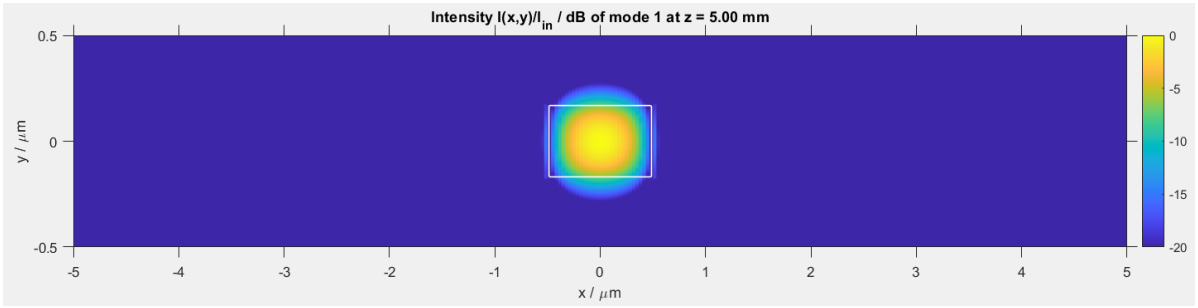

Figure 6.49: Electric field intensity simulations for a cladding thickness of 45 nm

COMSOL Simulations

Here, all the simulations done in COMSOL during the designing of the optical modulator, which weren't shown in chapter 3 are shown.

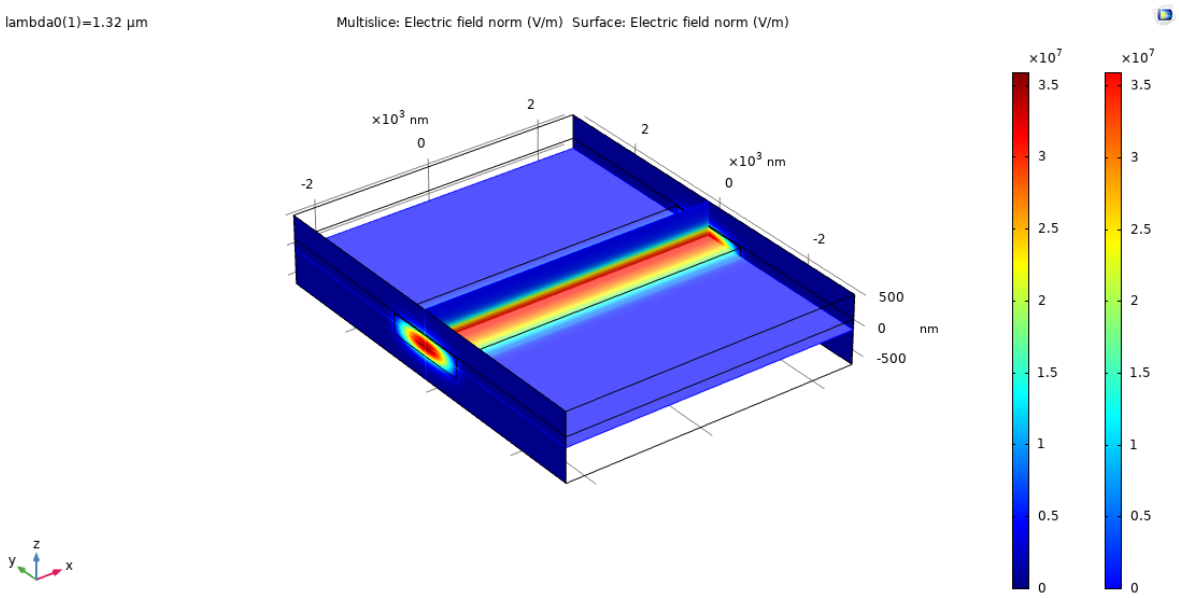

Figure 6.50: Electric field intensity simulations in COMSOL for a waveguide width of 1.5 um

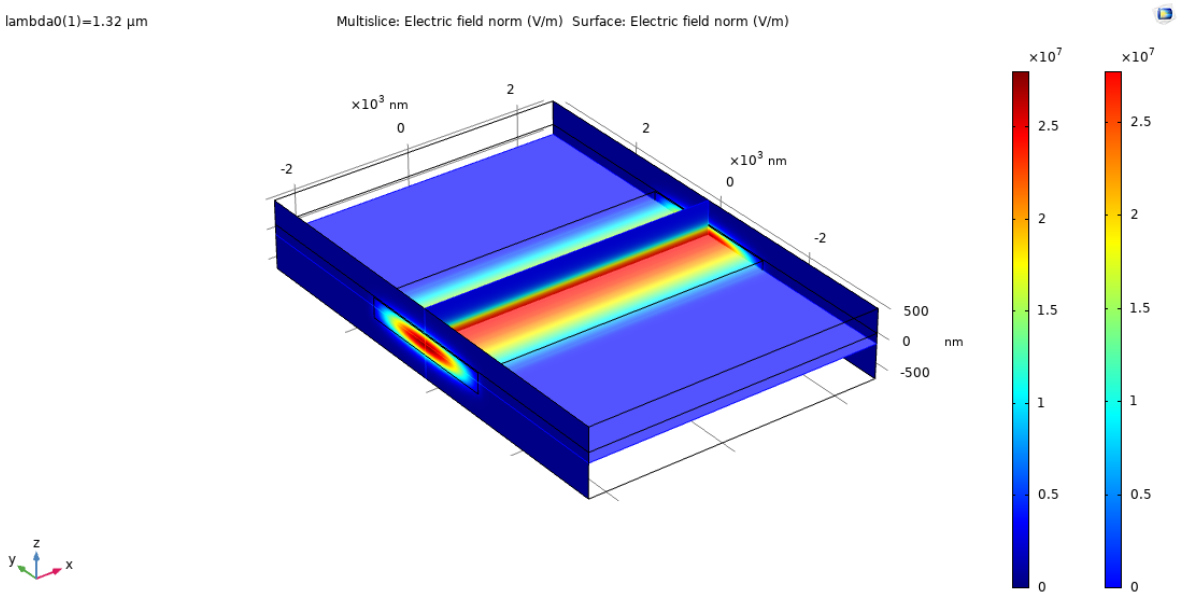

Figure 6.51: Electric field intensity simulations in COMSOL for a waveguide width of 2.5 um

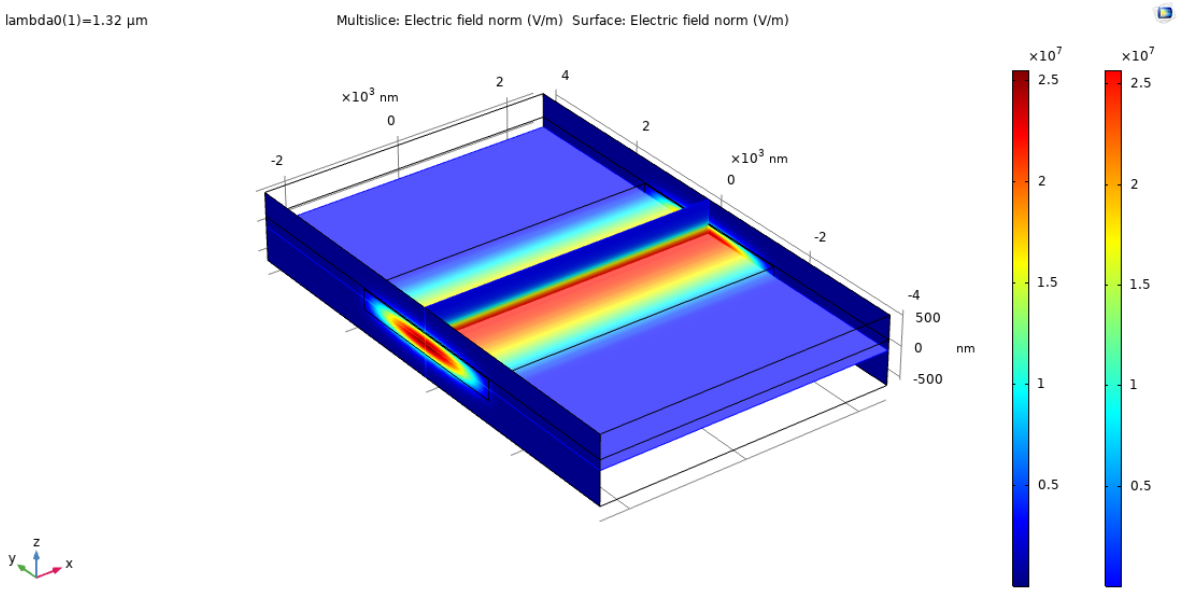

Figure 6.52: Electric field intensity simulations in COMSOL for a waveguide width of 3 um

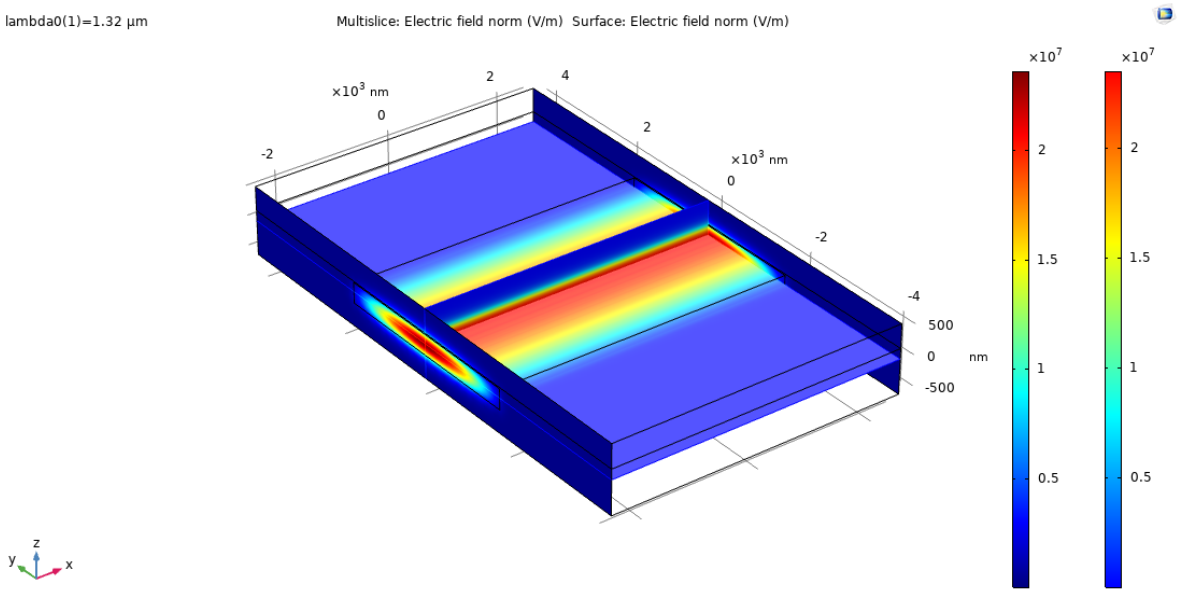

Figure 6.53: Electric field intensity simulations in COMSOL for a waveguide width of 3.5 um

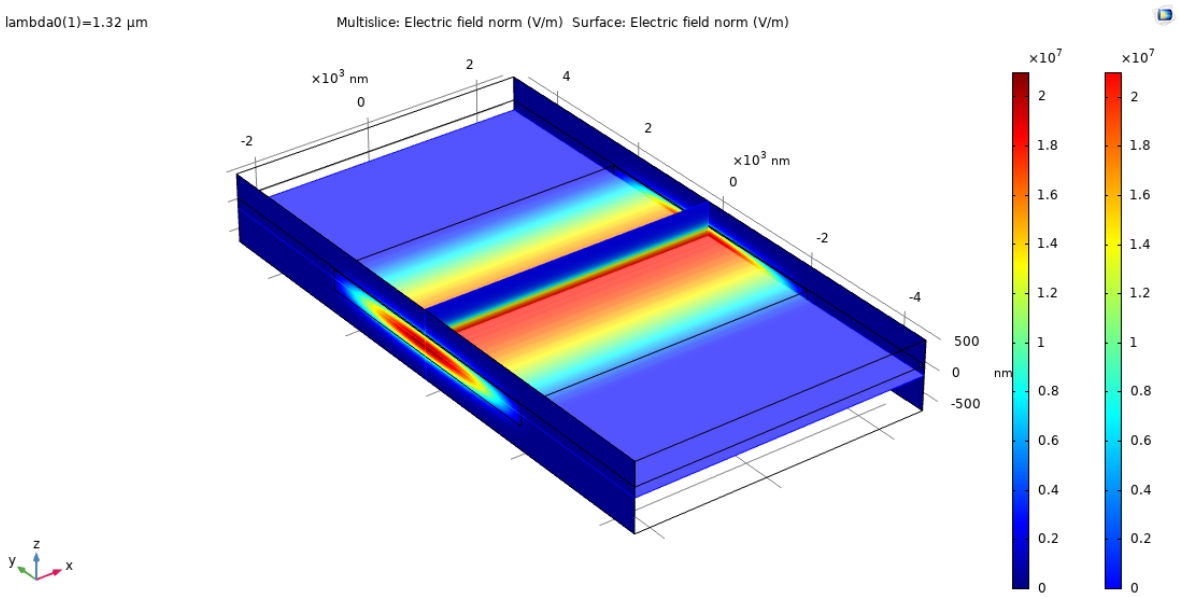

Figure 6.54: Electric field intensity simulations in COMSOL for a waveguide width of 4.5 um

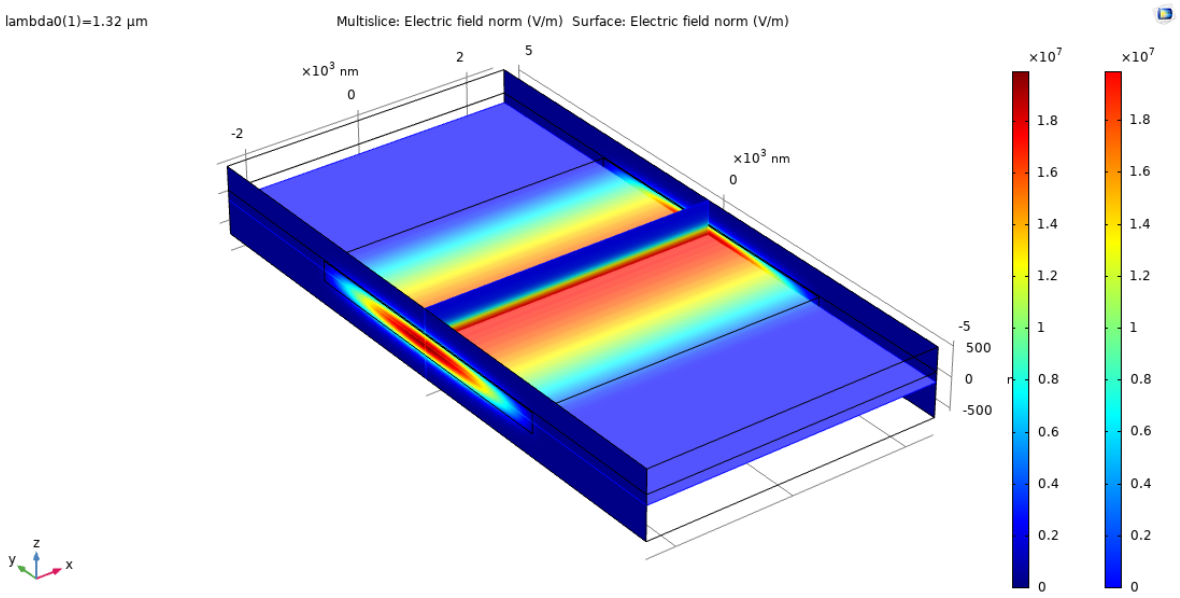

Figure 6.55: Electric field intensity simulations in COMSOL for a waveguide width of 5 um

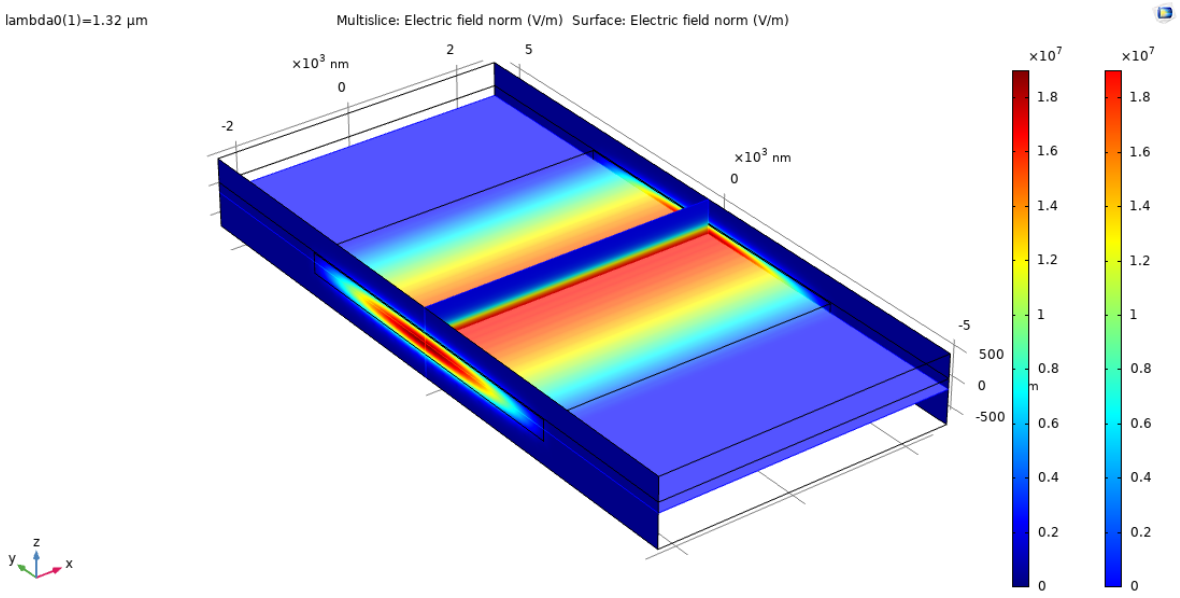

Figure 6.56: Electric field intensity simulations in COMSOL for a waveguide width of 5.5 um

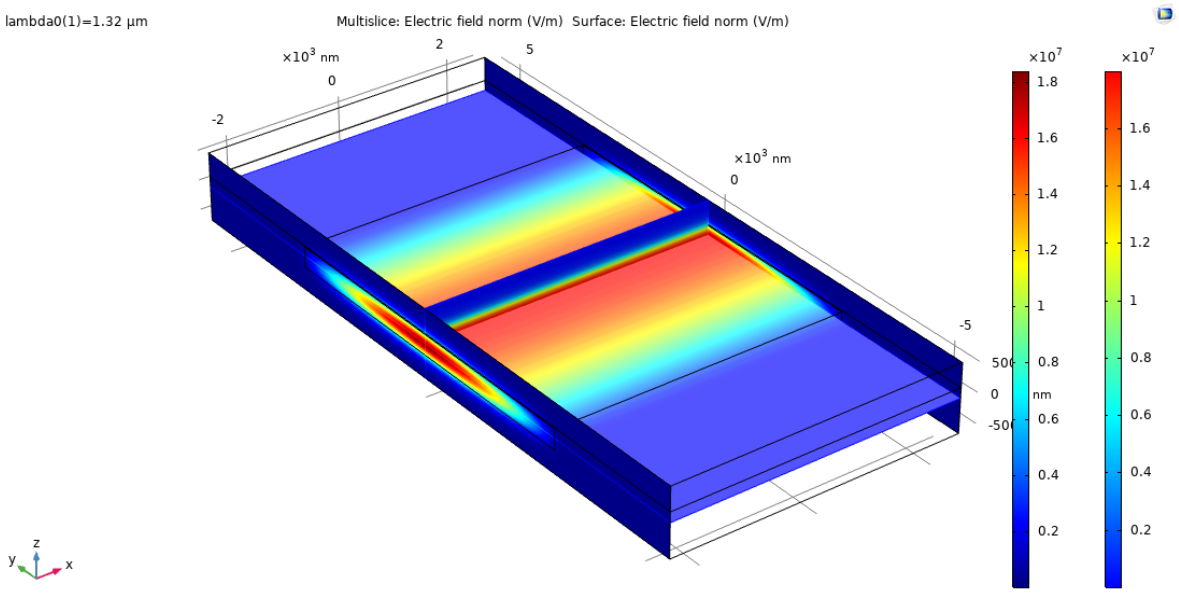

Figure 6.57: Electric field intensity simulations in COMSOL for a waveguide width of 6 um

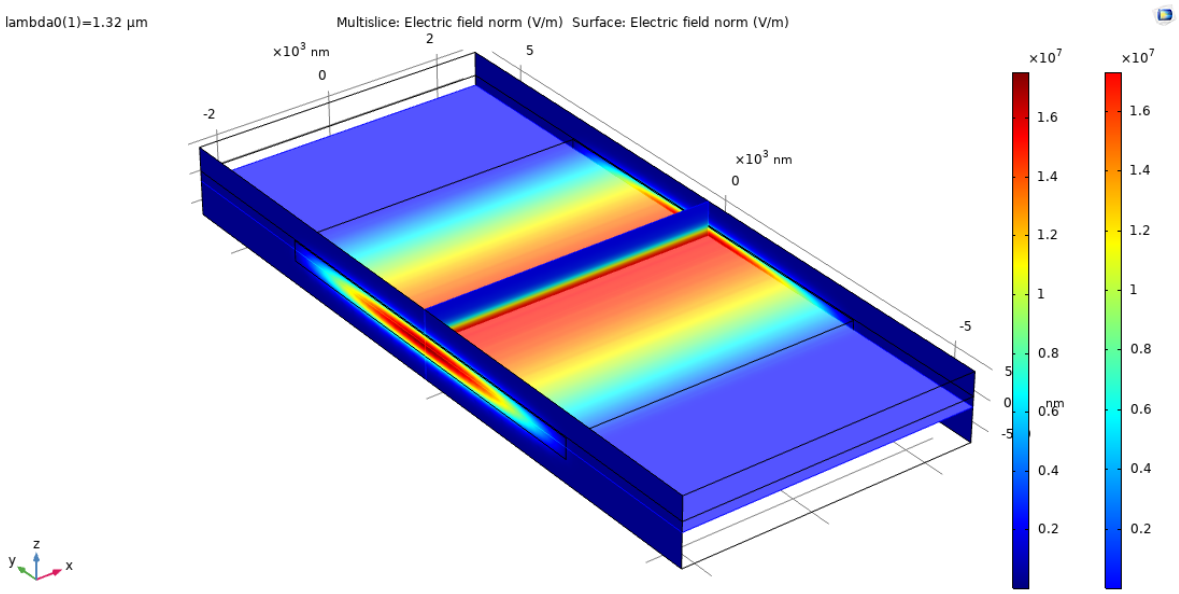

Figure 6.58: Electric field intensity simulations in COMSOL for a waveguide width of 6.5 um

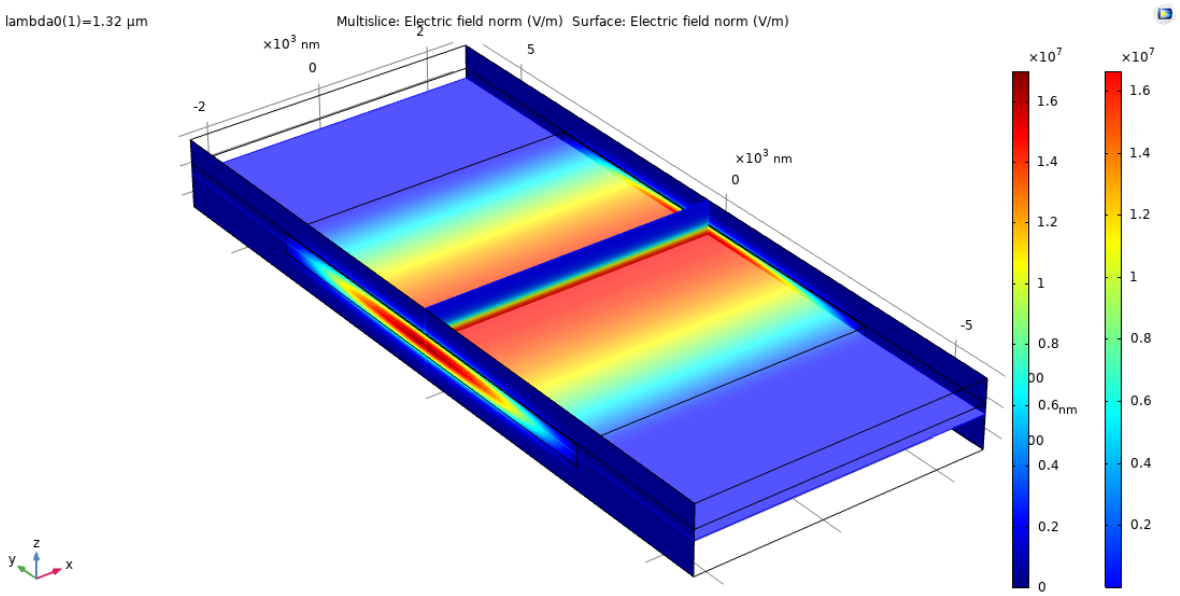

Figure 6.59: Electric field intensity simulations in COMSOL for a waveguide width of 7 um

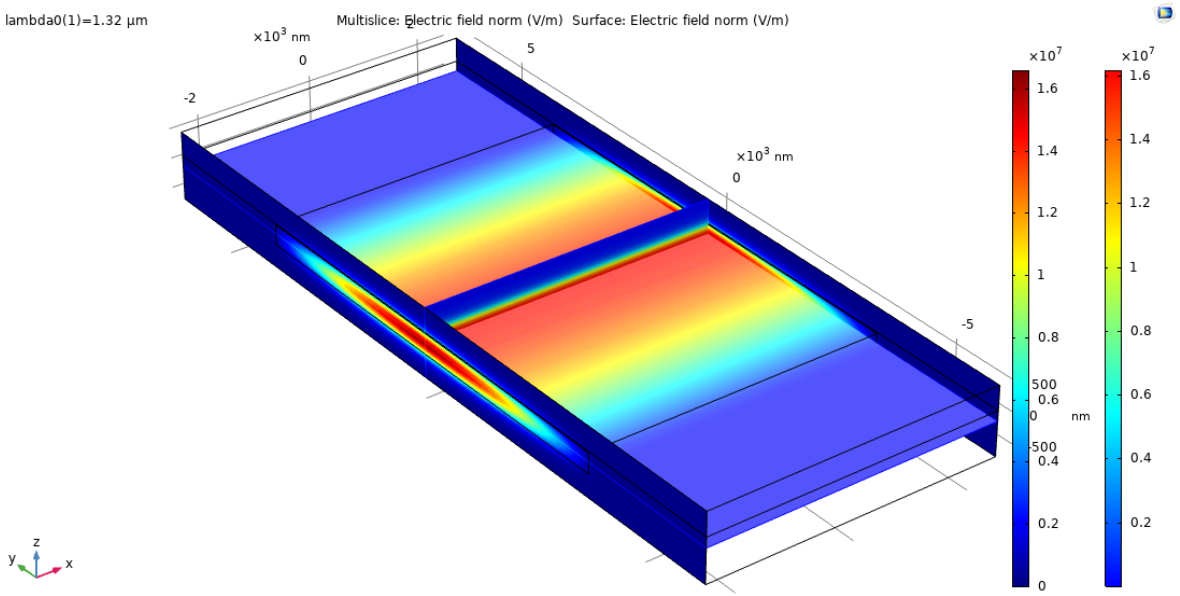

Figure 6.60: Electric field intensity simulations in COMSOL for a waveguide width of 7.5 um

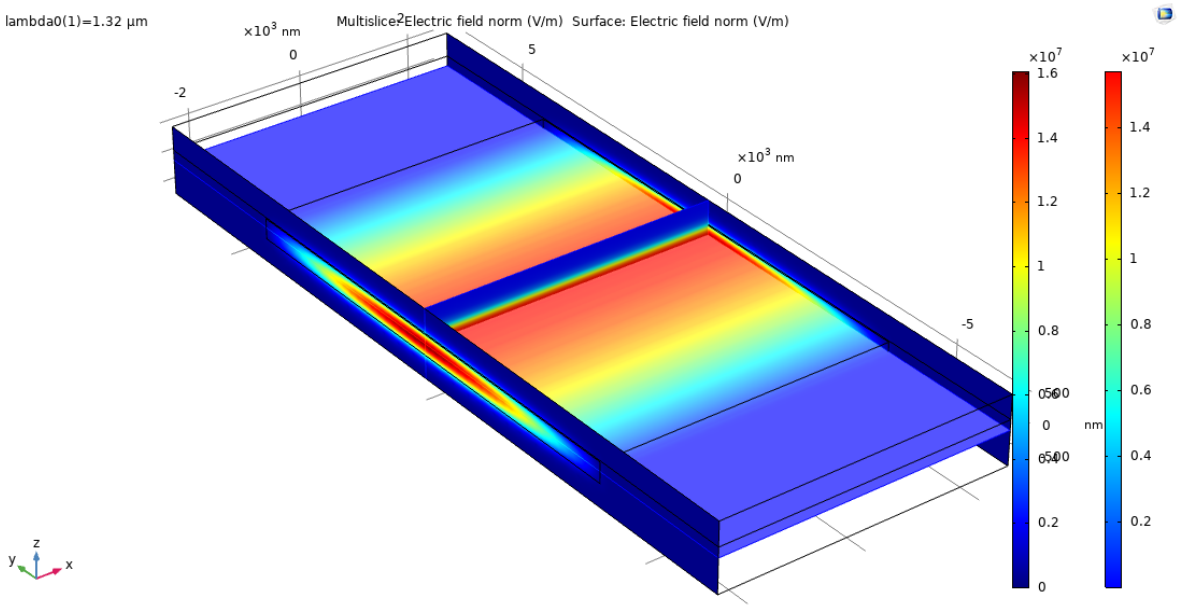

Figure 6.61: Electric field intensity simulations in COMSOL for a waveguide width of 8 um

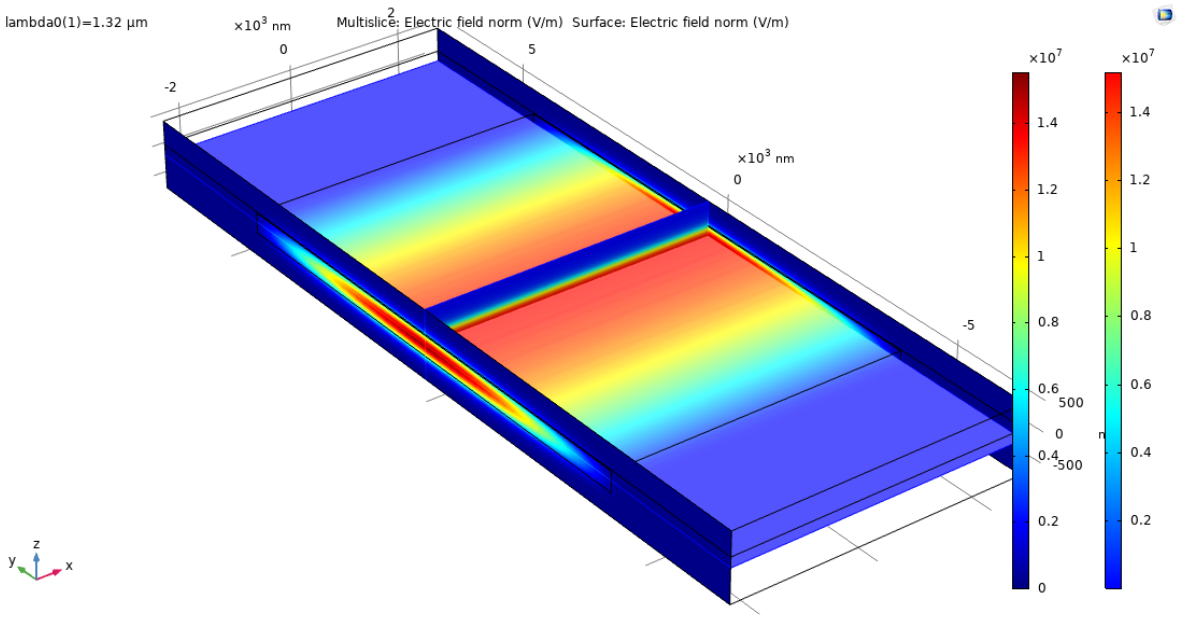

Figure 6.62: Electric field intensity simulations in COMSOL for a waveguide width of 8.5 um

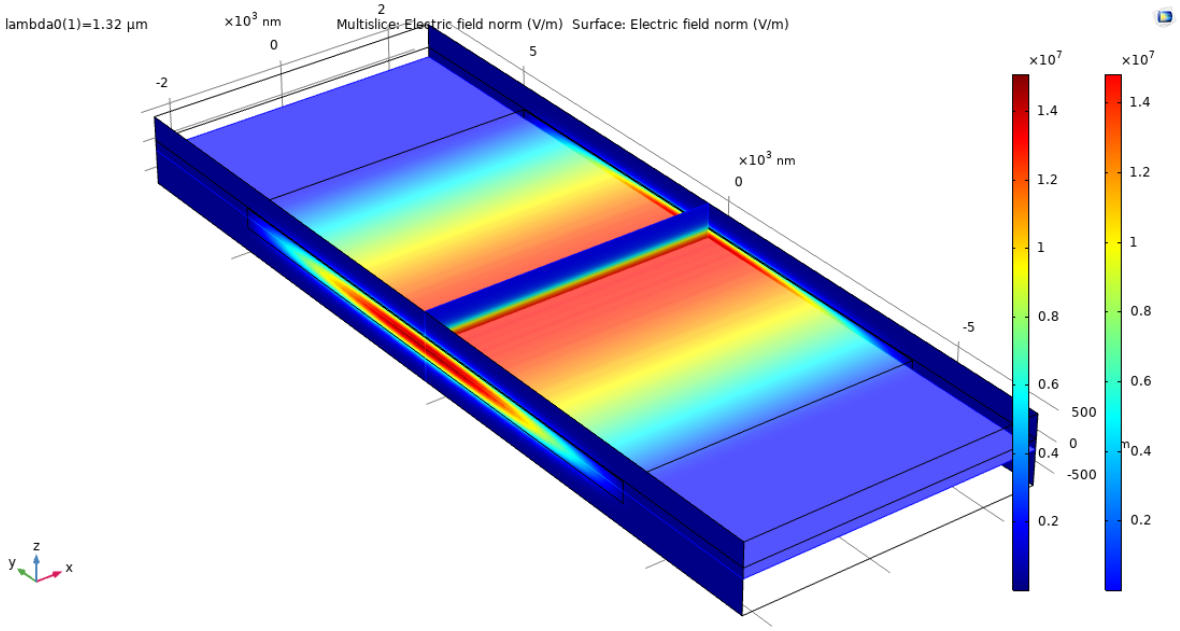

Figure 6.63: Electric field intensity simulations in COMSOL for a waveguide width of 9 um

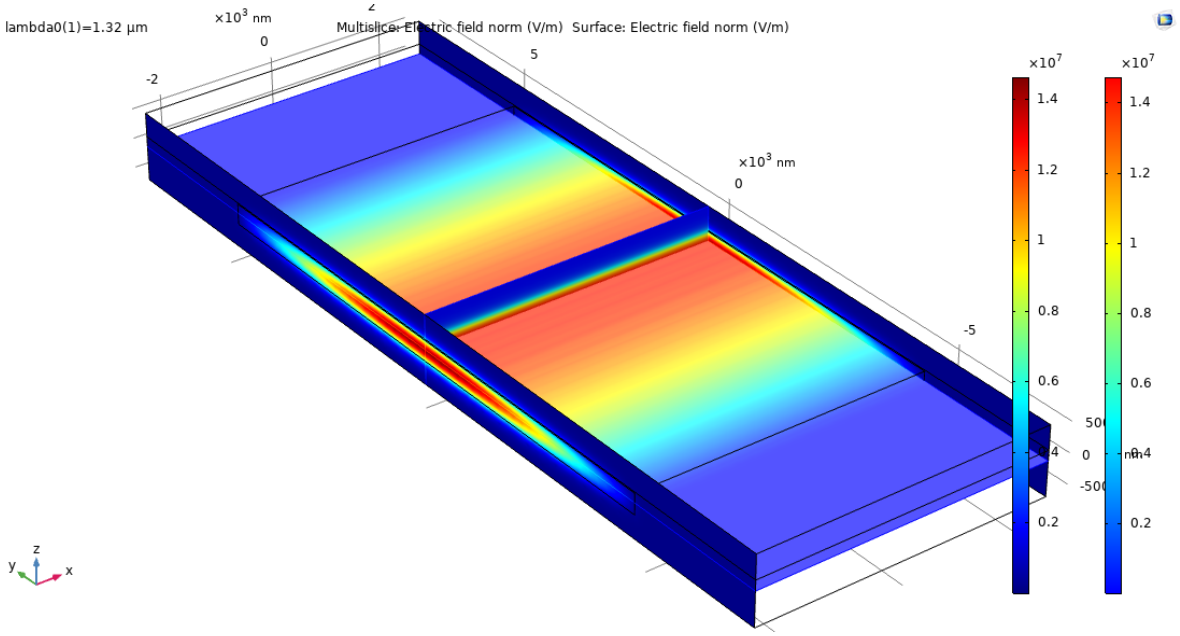

Figure 6.64: Electric field intensity simulations in COMSOL for a waveguide width of 9.5 um

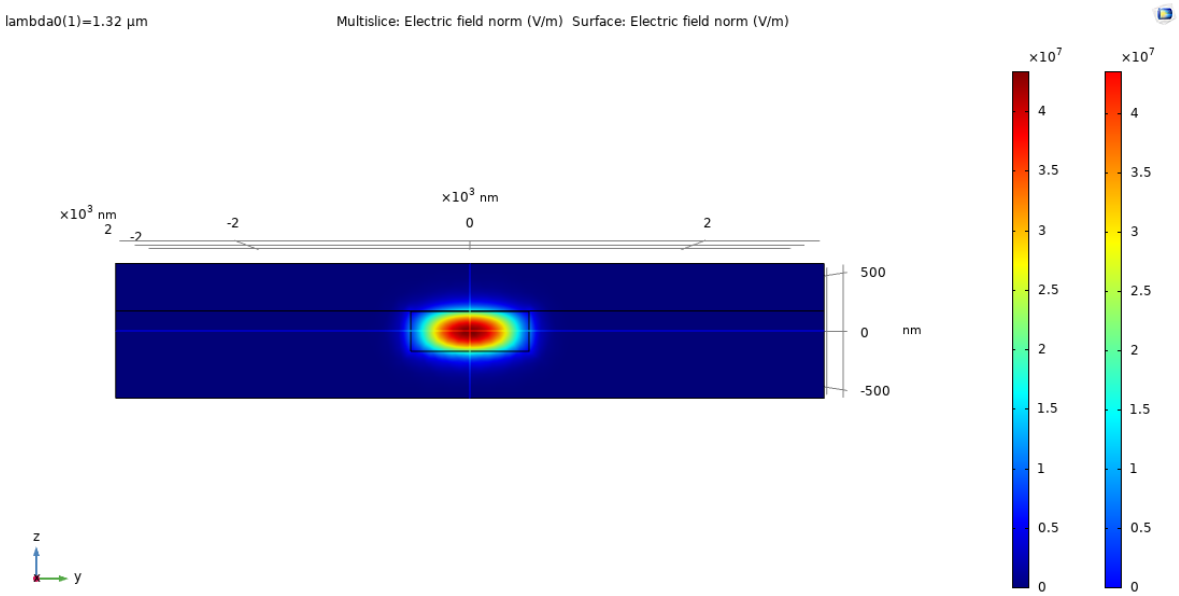

Figure 6.65: Electric field intensity simulations in COMSOL for a cladding thickness of 5 nm

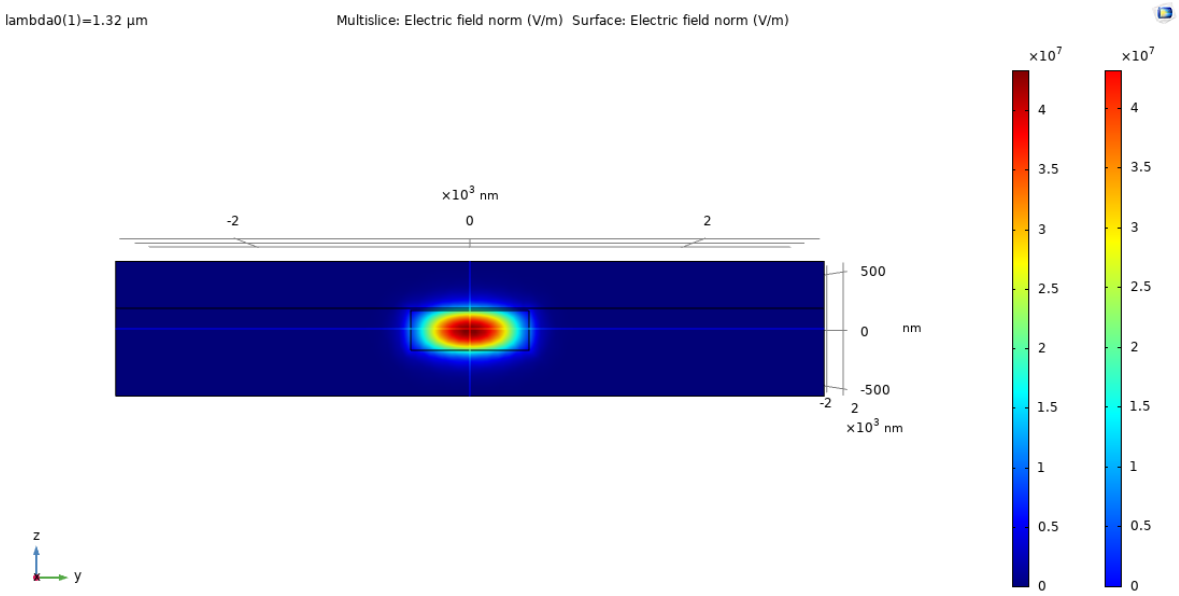

Figure 6.66: Electric field intensity simulations in COMSOL for a cladding thickness of 15 nm

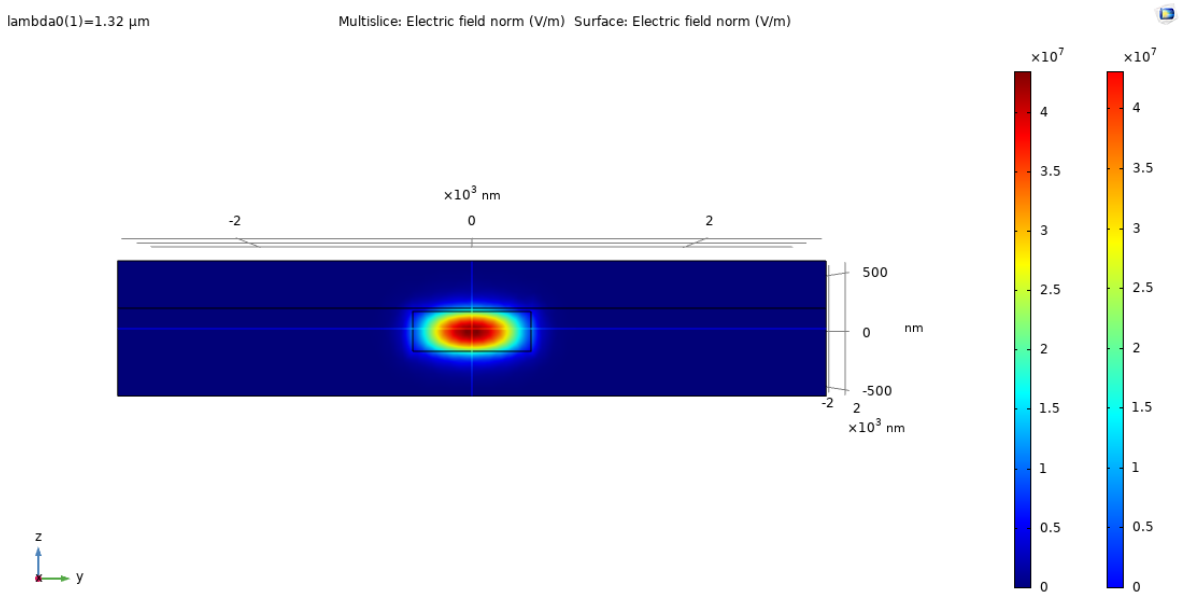

Figure 6.67: Electric field intensity simulations in COMSOL for a cladding thickness of 25 nm

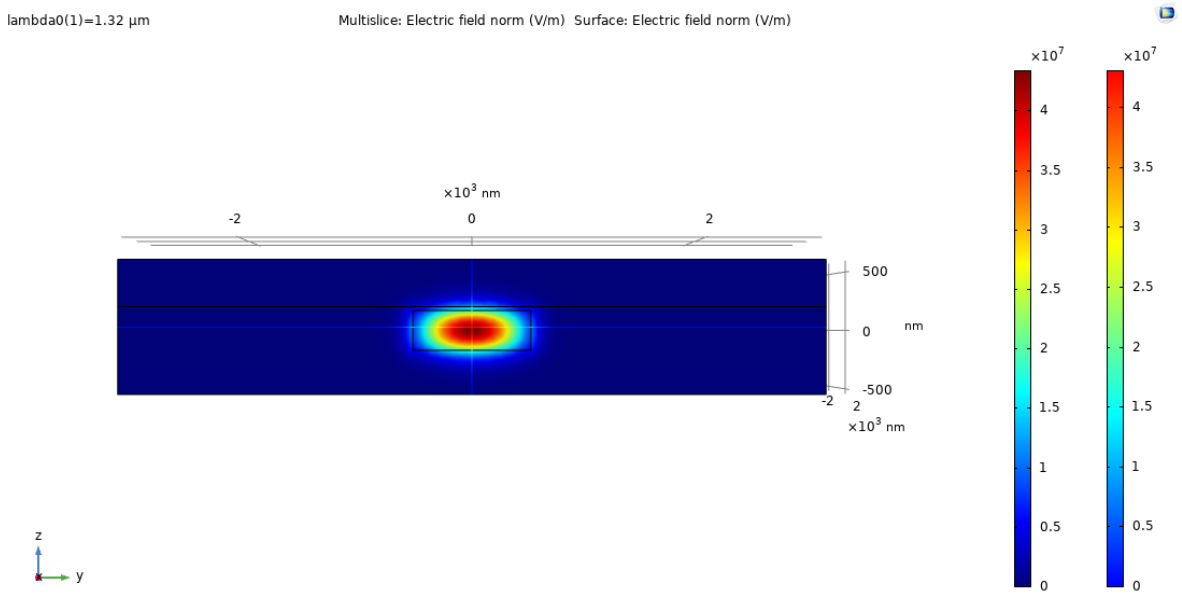

Figure 6.68: Electric field intensity simulations in COMSOL for a cladding thickness of 30 nm

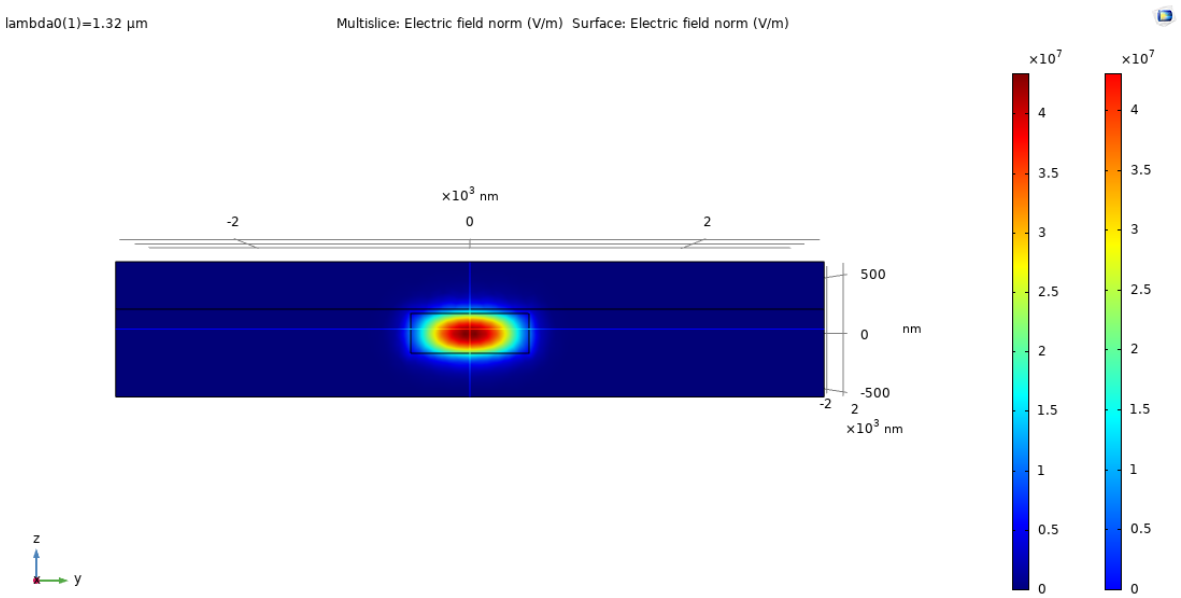

Figure 6.69: Electric field intensity simulations in COMSOL for a cladding thickness of 35 nm

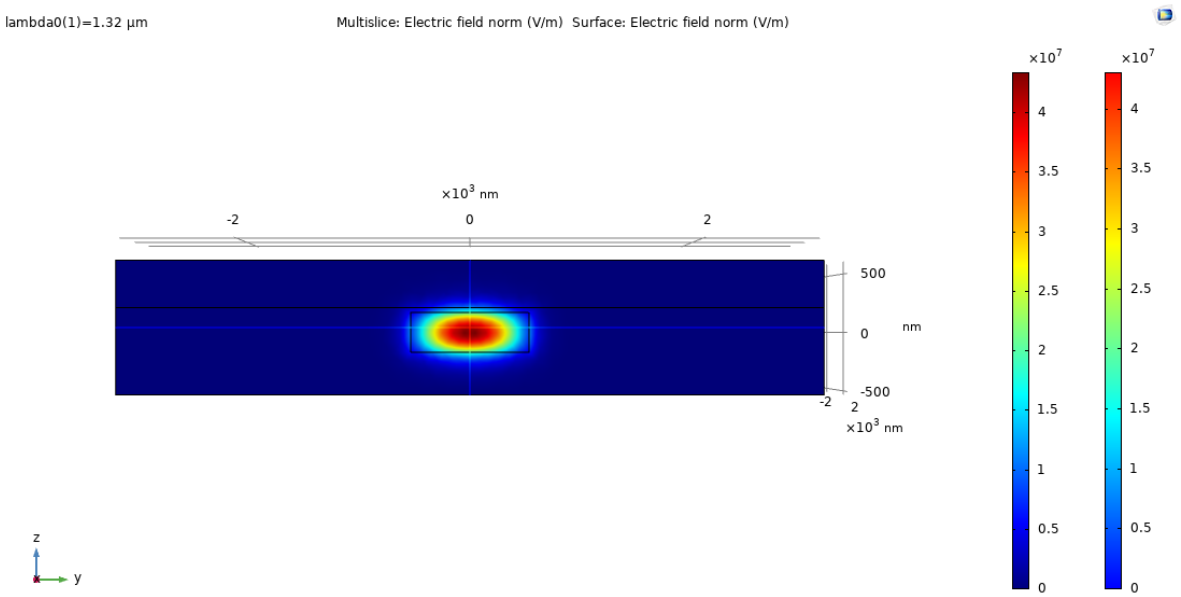

Figure 6.70: Electric field intensity simulations in COMSOL for a cladding thickness of 40 nm

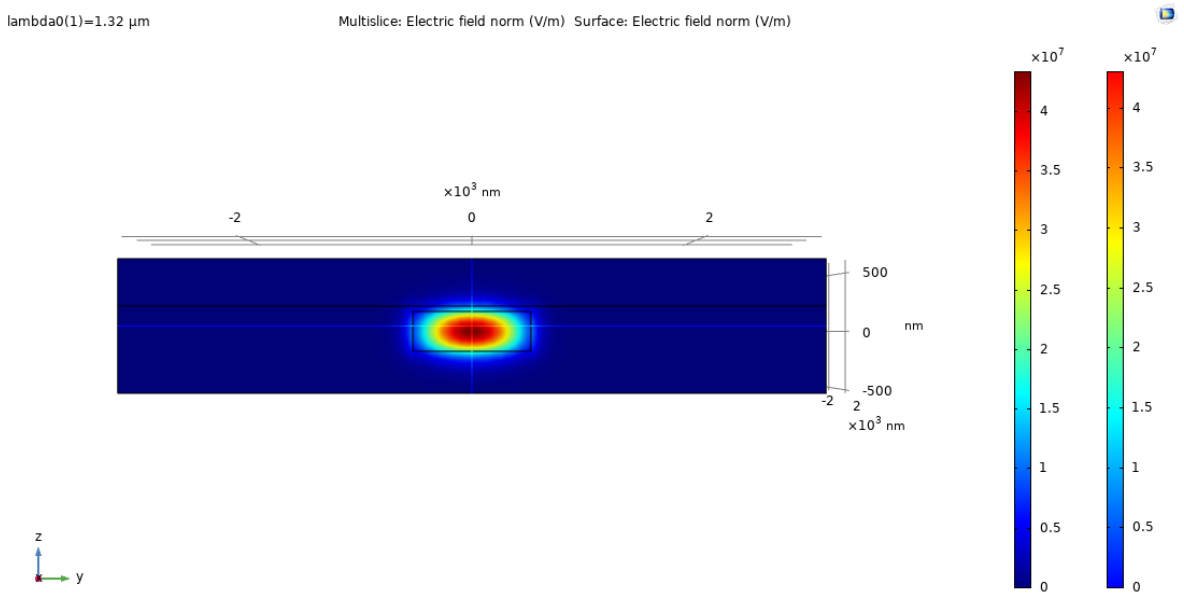

Figure 6.71: Electric field intensity simulations in COMSOL for a cladding thickness of 45 nm

SEM images

Here we show some SEM images taken during the testing of different PVA concentrations.

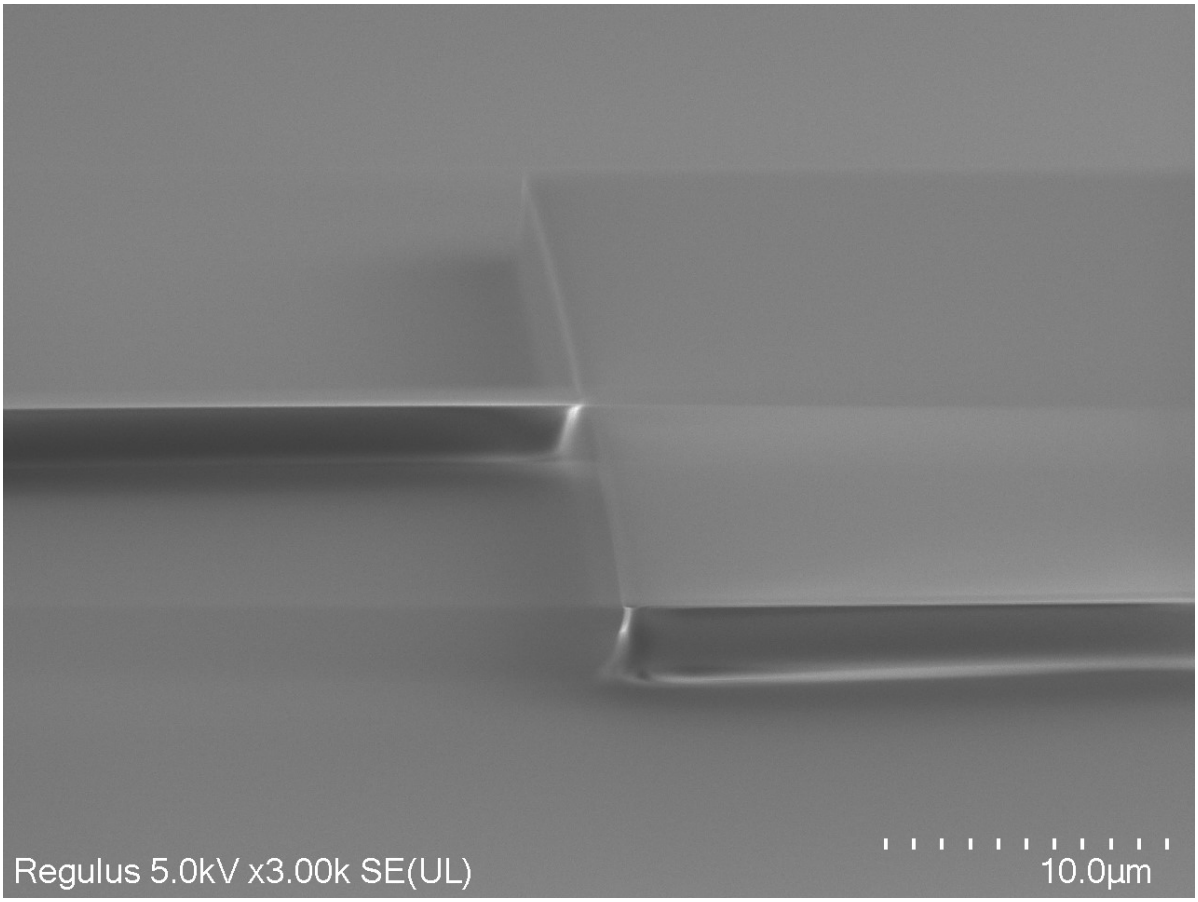

Figure 6.72: SEM images for the Photo-resist profile for 45mJ/cm^2 exposure energy when 20% PVA is used.

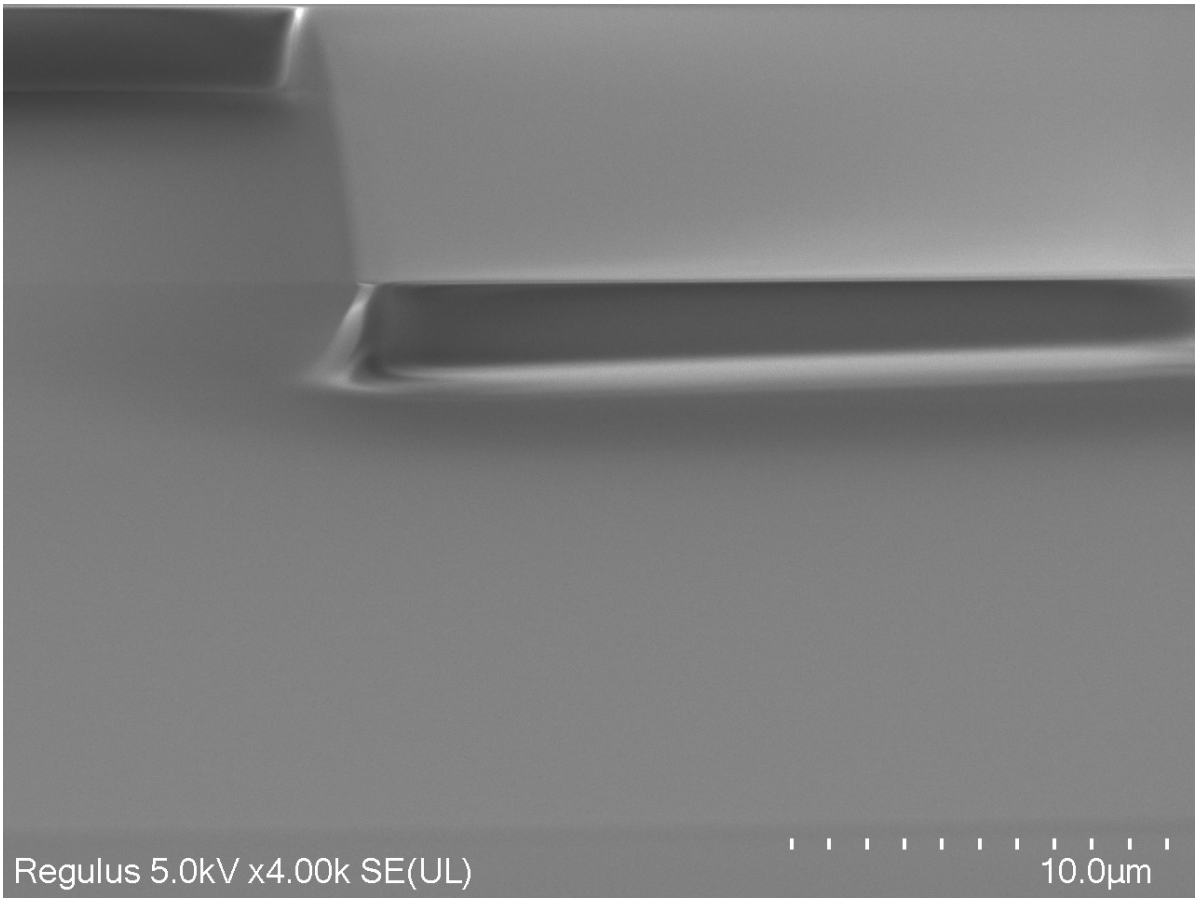

Figure 6.73: SEM images for the Photo-resist profile for 55mJ/cm^2 exposure energy when 20% PVA is used.

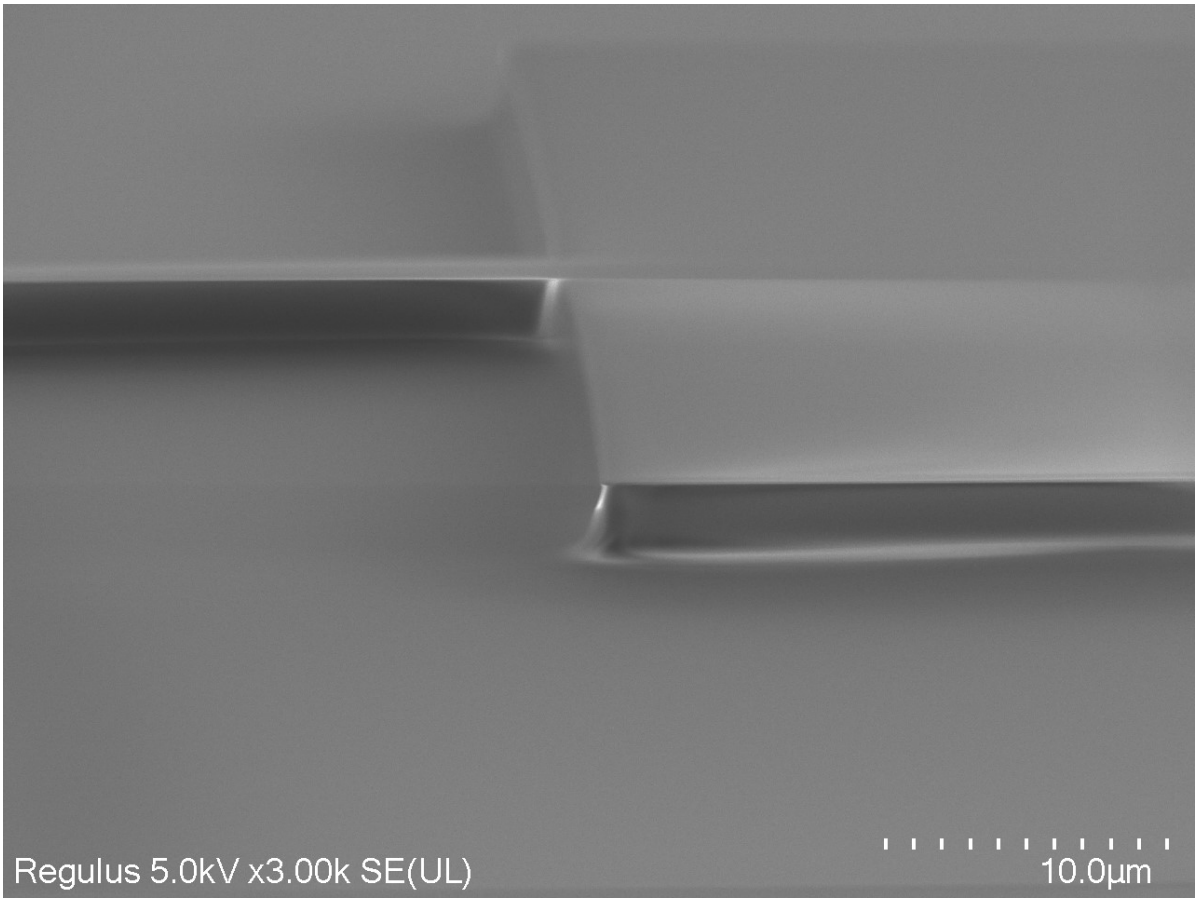

Figure 6.74: SEM images for the Photo-resist profile for 60mJ/cm^2 exposure energy when 20% PVA is used.

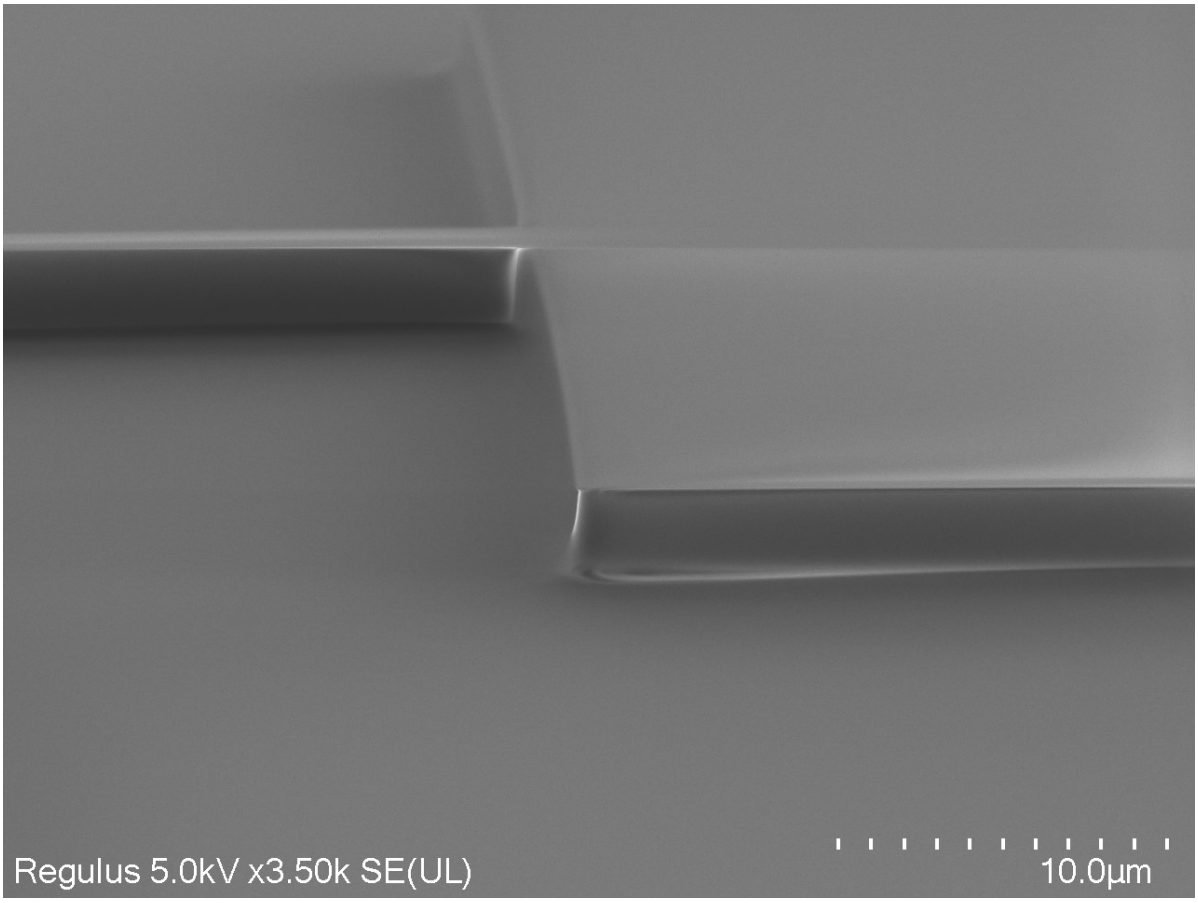

Figure 6.75: SEM images for the Photo-resist profile for 65mJ/cm^2 exposure energy when 20% PVA is used.

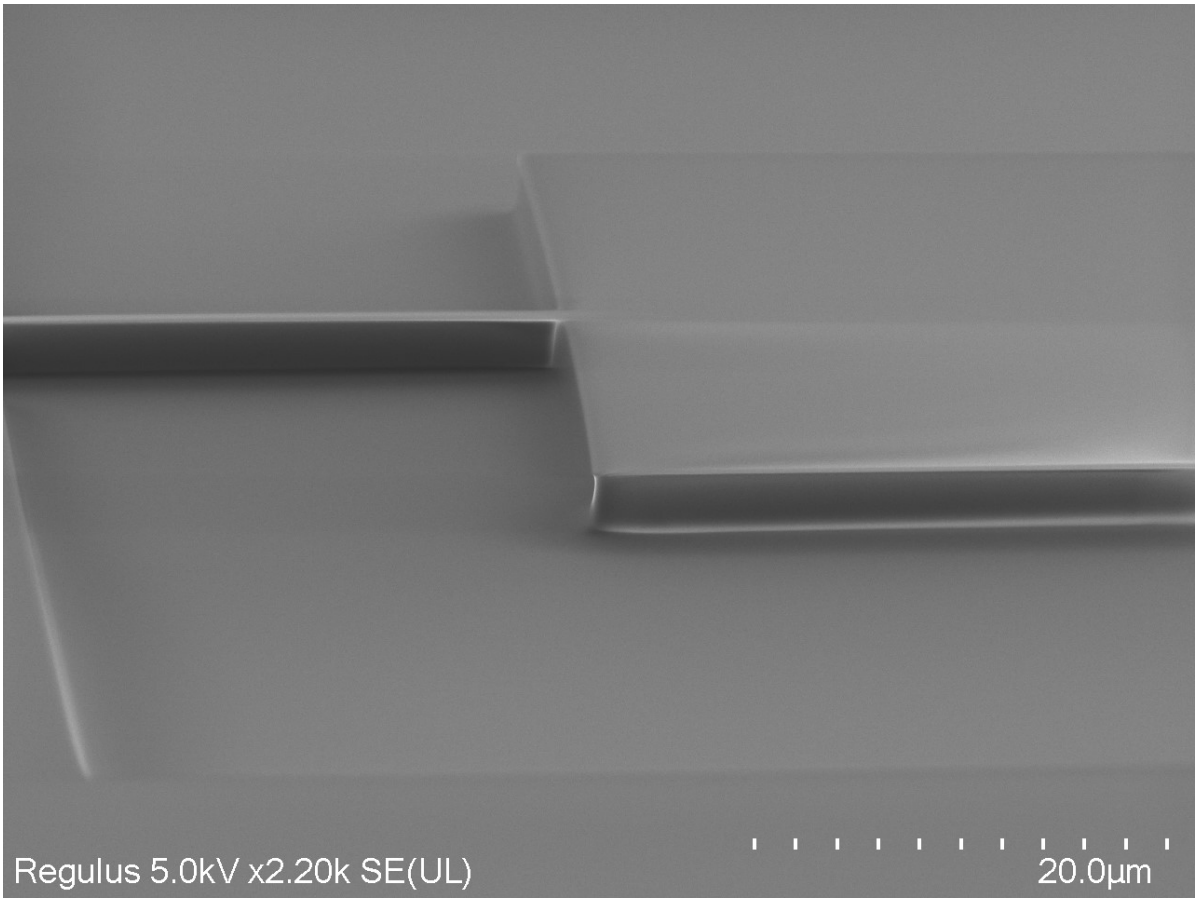

Figure 6.76: SEM images for the Photo-resist profile for 70mJ/cm^2 exposure energy when 20% PVA is used.

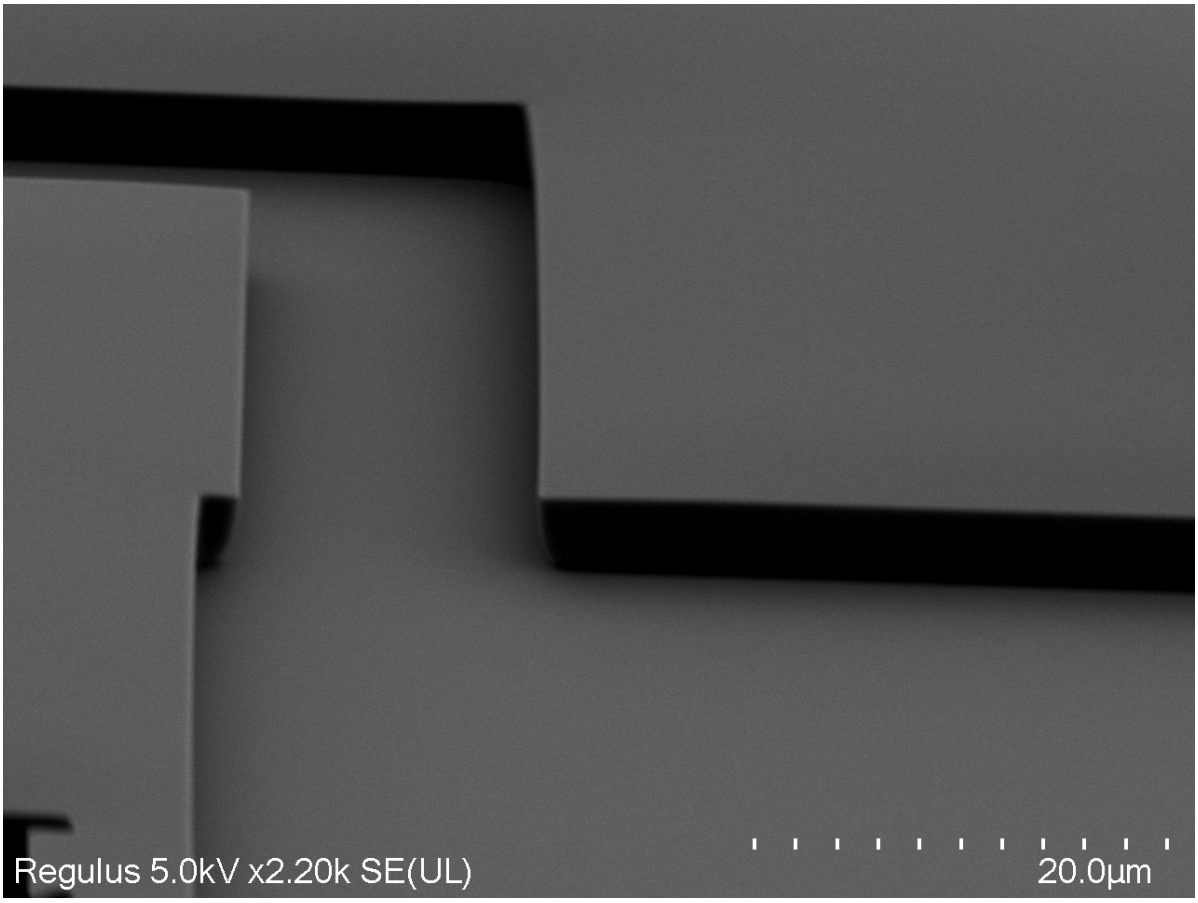

Figure 6.77: SEM images for the Photo-resist profile for 45mJ/cm^2 exposure energy when 10% PVA is used.

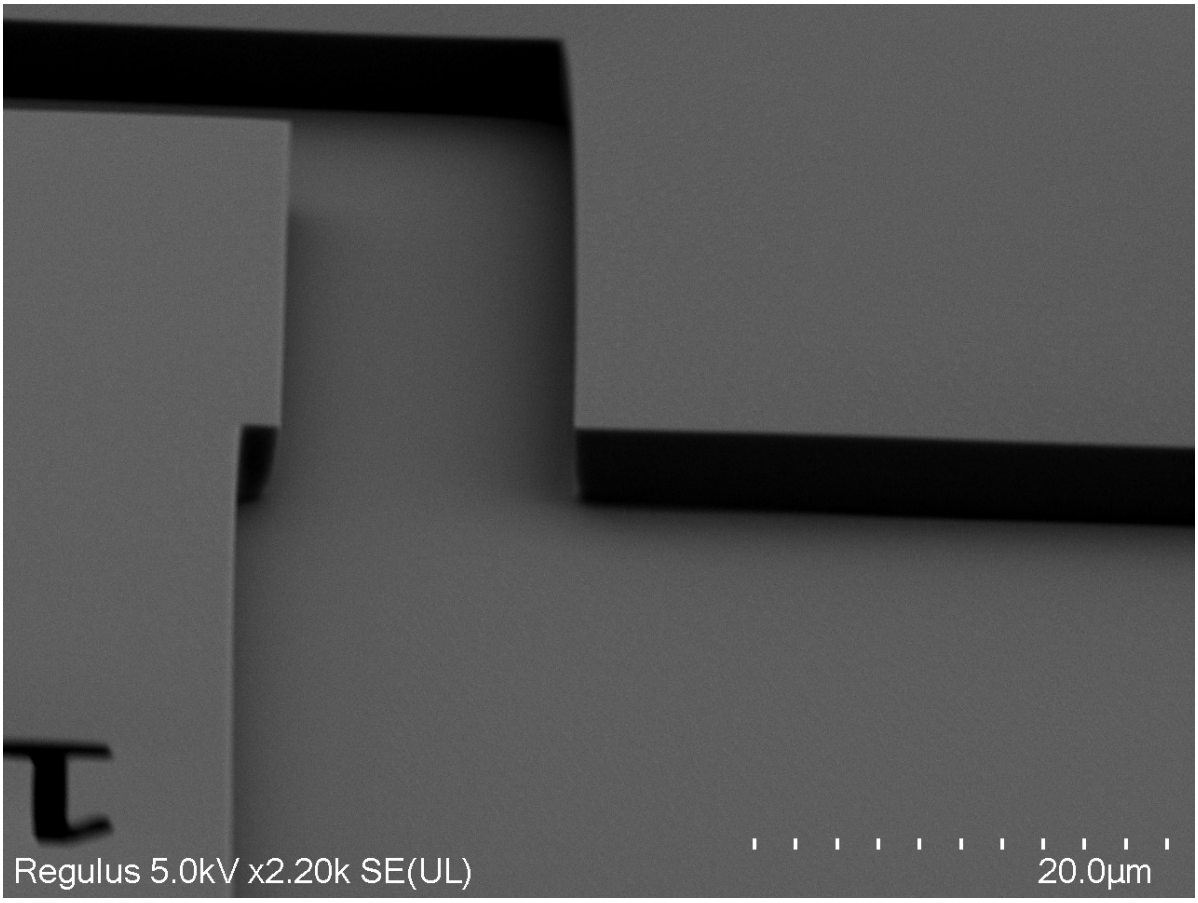

Figure 6.78: SEM images for the Photo-resist profile for 55mJ/cm^2 exposure energy when 10% PVA is used.

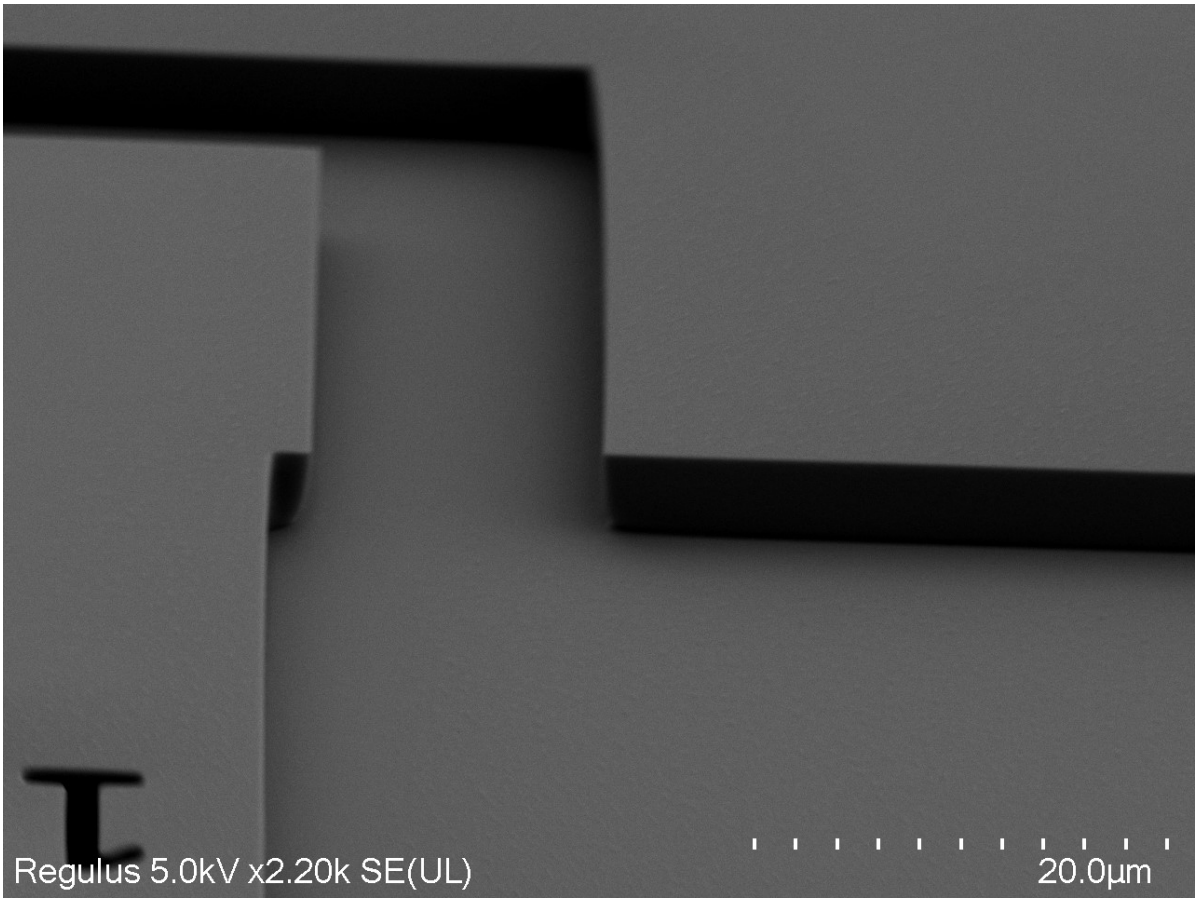

Figure 6.79: SEM images for the Photo-resist profile for 60mJ/cm^2 exposure energy when 10% PVA is used.

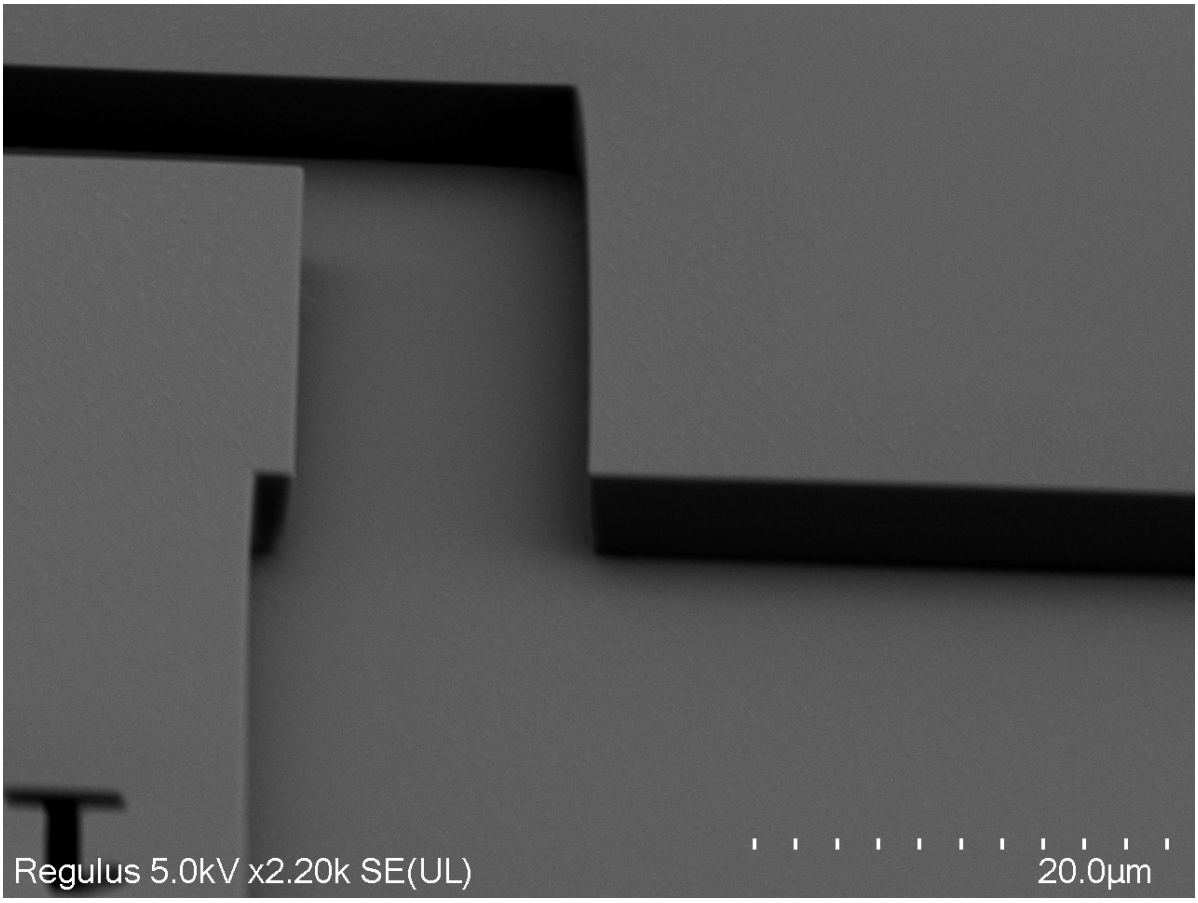

Figure 6.80: SEM images for the Photo-resist profile for 65mJ/cm^2 exposure energy when 10% PVA is used.

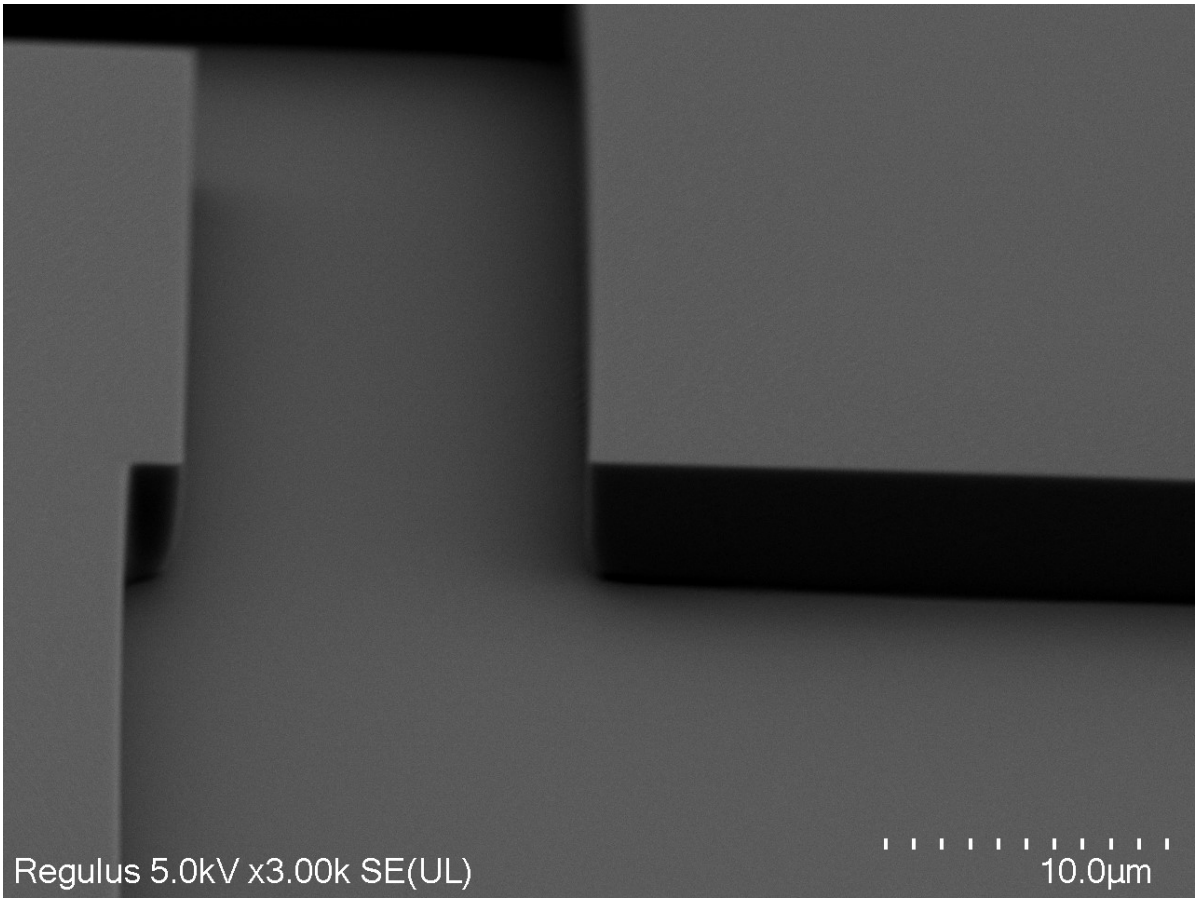

Figure 6.81: SEM images for the Photo-resist profile for 70mJ/cm^2 exposure energy when 10% PVA is used.