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Microstructure Analysis Based on 3D reconstruction Model and Transient Thermal Impedance Measurement of Resin-reinforced Sintered Ag layer for High power RF device

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Abstract—Resin-reinforced silver (Ag) sintering material is an effective and highly reliable solution for power electronics packaging. The hybrid material's process parameters strongly influence its microstructure and pose a significant challenge in estimating its effective properties as a thin interconnect layer. This research demonstrates a novel 3D reconstruction methodology for the microstructural investigation of the resin-reinforced Ag sintering material from OverMolded Plastic (OMP) packages. Based on the reconstructed models with different sintering parameters (temperature and time), the fraction of Ag and Resin volume distribution, the connectivity of silver particles, and the tortuosity factors were estimated. A 99% connectivity of sintered Ag particles was achieved with various sintering conditions, such as 200°C for 2 hours, 200°C for 4 hours, and 250°C for 2 hours. However, coarsening of Ag particles was promoted when sintered at 250°C. Increasing the sintering time at 200°C had insignificant changes. The estimated tortuosity factor also indicated that sintering at 250°C provides the shortest heat transport path between the semiconductor die and the package substrate. In order to quantify the microstructural findings, the OMP packages' thermal performance with different sintering conditions (temperature, time, and interconnect thickness) was experimentally assessed. Although the experimental measurements were less sensitive to the effective interface thermal resistances', the measurement results show a good correlation with the microstructural analysis. Sintering the Resin-reinforced Ag sintering material at higher temperatures (250°C) seems to improve the package thermal performance, and increasing the sintering time at 200°C has a negligible effect.

Keywords—Hybrid Ag Sintering, Pressureless Sintering, 3D Reconstruction, Microstructure Analysis, Tortuosity, Transient Thermal Impedance, LDMOS Body Diode Measurement

I. Introduction

The importance of package reliability for power semiconductor devices is becoming more critical than ever, and the choice of die-attach material plays a significant role [1, 2]. High-temperature Pb-rich solders were preferred for power electronics because they offer several advantages, such as high melting point (> 300°C) and relatively low stiffness (∼ 45 – 60 GPa). However, the toxicity of lead caused an increasing need for lead-free compositions. Sintering technology came up as an attractive alternative. Metal precursors in the form of pastes are fused under heat (and pressure), resulting in a significantly high melting point after processing (∼ 1000°C) and superior thermal properties. Despite its benefits, sintering materials are relatively stiff (∼ 80 – 130 GPa) and suffer from thermo-mechanical stresses. An overview of the current state-of-the-art sintering materials over traditional solders and a review of various sintering techniques are given in [3, 4, 5].

Resin-reinforced sintering material proposed by Sasaki et al. [6] is considered a promising strategy for maintaining favorable sintering properties with reduced stiffness. Thermoplastic resins added to the metal pastes occupy the porous regions during sintering, resulting in a relatively lower modulus [7]. However, the hybrid microstructure of this material makes it very different from traditional sintering materials. An indicative image of the resin-reinforced Ag sintering material is shown in **Figure 1**. Firstly, the composition is made of micro and nano-Ag particles surrounded by thermoplastic resin, which makes it difficult to judge to what degree the Ag particles have been sin-

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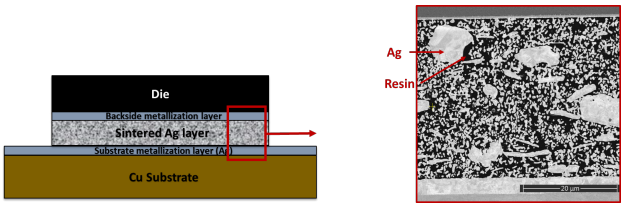
tered. Besides, the influence of process parameters (temperature and time) for resin-reinforced Ag sintering material has never been addressed. Furthermore, estimating thin interconnect's effective heat transport interactions toward the package's thermal performance remains challenging [8].



(a) (b)

Figure 1: (a). A cross-sectional schematic of a semiconductor die sintered to a copper substrate by resin-reinforced Ag sintering material is shown. The backside of the die and the topside of the substrate are metalized with silver to promote adhesion to the die-attach layer. **(b).** A zoomed-in SEM image of the resin-reinforced Ag sintering material is shown. The sintered layer composes of micro and nano-Ag particles surrounded by thermoplastic resin.

This research investigates the microstructure of resin-reinforced Ag sintering material under different processing conditions and its influence on the packaged device's thermal performance. In the next section, we discuss a 3D reconstruction technique to analyze the microstructure of the thin-interconnect material and an experimental methodology to analyze the packaged device's thermal performance. The subsequent section demonstrates the results of the microstructural analysis and transient thermal measurements. Both investigations concluded similar findings with key highlights on the sintering process parameter's influence on the resin-reinforced Ag sintering material's characteristics.

II. Methodology

A. Preparation of samples

Silicon-based Laterally Diffused Metal Oxide Semiconductor (LDMOS) high-power RF devices were assembled in Over Molded Plastic (OMP) packages. The semiconductor device's backside was metalized with Ag ($\sim 1\mu$m) to promote adhesion to the interconnect material as shown in **Figure 1**. Once metalized, the devices were sintered to a silver-metalized ($\sim 6\mu$m) copper substrate using resin-reinforced Ag sintering material. The complete stack is then wire-bonded and over-molded. To analyze the influence of sintering conditions, the devices were sintered with different processing parameters: **(i.)** Bond-Line Thicknesses (20μm & 60μm $\pm$ 10μm), **(ii.)** Sintering temperatures (200°C & 250°C), and **(iii.)** Sintering time (2 hours & 4 hours). All samples were sintered by a pressureless process under an air ambient.

B. FIB milling and 3D modeling

The workflow shown in **Figure 2** was followed to analyze the microstructure of the sintered interconnect layer. The OMP packages were dissected and potted with epoxy resin for polishing. After polishing, the sample was set in the Scanning Electron Microscope (SEM) vacuum chamber integrated with a Focused Ion Beam (FIB). The region of interest (ROI) was chosen, and a protective Pt layer of 1μm was deposited. Broad and deep U-shaped trenches were milled around the ROI with FIB currents up to 21nA. A reference mark on the ROI surface was made, and then the surface was milled at a fine pitch of 50nm to avoid missing tiny nano-particles. After every milling step, the sample surface was micrographed using SEM. The process described above is automatically implemented by Auto Slice & View 4 Software [9]. Accordingly, more than 200 steps of 50nm pitch were milled, and the micrographs obtained were transformed into a 3-dimensional model using AVIZO (A commercial software for data analysis) [10].

For image processing, the tilt of SEM images was corrected for alignment and a Gaussian filter was chosen to improve the SEM image contrast. The phase segmentation of the sintered Ag and the resin was implemented based on gray-scale thresholding. Finally, the rendered images were

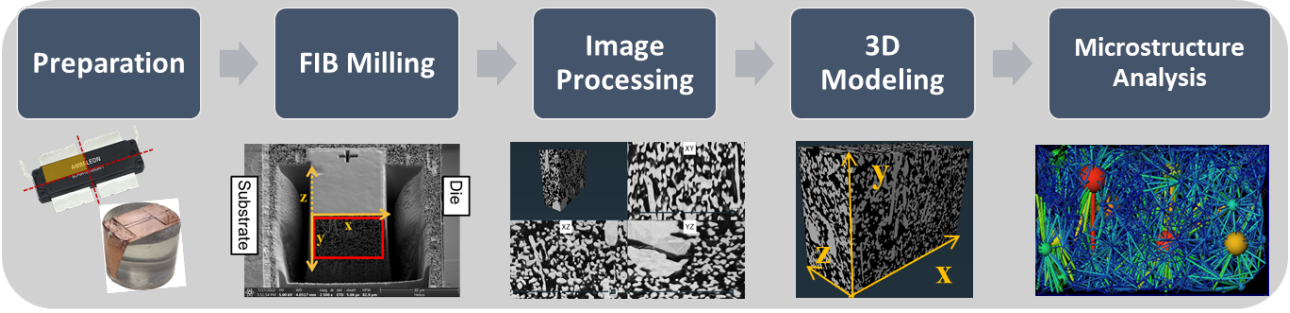
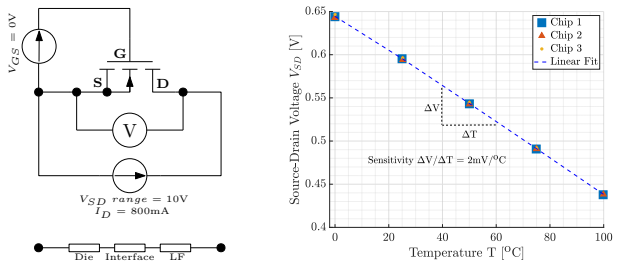


Figure 2: The workflow to obtain microstructure information on the resin-reinforced Ag sintering material is shown. The assembled OMP packages were first dissected, and a section of the sample was potted with an epoxy compound for polishing. A Region of Interest (ROI) was chosen in the second step. Broad and deep U-shaped trenches were milled around the ROI using FIB. Sequentially, the region of interest is micrographed using a scanning electron microscope. For each sample, over two-hundred steps of 50nm pitch were continuously milled and micrographed. Tilt correction and phase segmentation are carried out in the image processing step. Subsequently, the rendered images were stitched together to create a 3D geometry of this material. The last step involves identifying the particle volume and connection path based on Generate Pore Network Model (GPNM) in AVIZO for further microstructure analysis.

stitched together as a 3D model for further analysis. To understand the interconnecting network of silver particles, a Generate Pore Network Model (GPNM) was used to identify the particle connection and calculate the tortuosity factor (**Figure 2**). A similar 3D reconstruction method-based FIB-SEM for Ag sintering materials has been described in [11]. The microstructural analysis is further discussed in the results section.

C. Transient Thermal Impedance

To experimentally analyze the influence of different sintering conditions on the packaged device's thermal performance, the transient thermal impedance of the OMP packages needs to be measured. The transient thermal impedance is a measure of how effectively the packaging materials can dissipate heat. It is determined by measuring the change in the device junction temperature for applied input power. The sintering parameters such as temperature, time, and Bond-Line Thicknesses (BLT) can affect properties such as thermal resistance and diffusivity, thereby affecting the transient thermal impedance measurement. Hence, to analyze the influence of the sintering parameters, the Junction-to-Ambient transient thermal impedance of the OMP packages was determined by measuring the device junction temperature. Similar experiments for thermal resistance evaluation of Pb solders, Pb-free solders, and Ag sintering materials have been studied in [12].



(a) **(b)**

Figure 3: (a). The electrical circuit of the MOSFET connected with two source units and one measuring unit with 4-point Kelvin contacts is shown. The electrical resistance of the package is a summation of the semiconductor die, the interface, and the lead frame. The device was measured under reverse biased, i.e., V_{GS} = 0, V_{SD} = 10V range, and I_D = 1A. **(b).** The temperature dependence of the diode's voltage V_{SD} for three different LDMOS devices were measured and shown. A linear relation is observed with a sensitivity of ∼2mV/°C.

The semiconductor device's Temperature Sensitive Electrical Parameters (TSEP) enable measuring the device junction temperature by translating the electrical output to temperature readings. The device was connected with 4-point Kelvin contacts for accurate measurements, as shown in **Figure 3a**. An LDMOS is a voltage-controlled device (i.e.,) the device is forward-biased when a positive voltage is applied between the gate-source ($+V_{GS}$) and drain-source ($+V_{DS}$) terminals, reverse-biased when the gate is closed (V_{GS} = 0), and a negative voltage is applied between the drain-source terminal ($-V_{DS}$ = V_{SD}). When reverse-biased, the device operates through the intrinsic body diode (a PN Junction formed between the source and the drain terminals), which has higher sensitivity to the temperature. The effects of LDMOS body diode reverse bias have been studied in [13]. The temperature sensitivity of the diode voltage, i.e., the source-drain voltage (V_{SD}) has a linear response to temperature with a sensitivity of ∼2mV/°C (**Figure 3b**).

To determine the package's thermal impedance, the semiconductor device must be heated, and the junction temperature needs to be simultaneously measured. Hence, a continuous drain current I_D of 1A was supplied through the body diode for 1000 seconds, resulting in device heating. The changes in the diode voltage V_{SD} due to device heating were simultaneously measured at a very high sampling rate of 15μs per data point for 100 seconds and 1μs per data point between 100 and 1000 seconds. The device and the packaging materials reach a steady state during 1000 seconds of heating, which enables the extraction of the die-attach layer properties by deconvolution of the resistance against the capacitance network through the structure-function explained in [14, 15, 16]. For deconvolution and extracting the resistance-capacitance network, TDIM-Master software provided by JEDEC was used [17]. The experimental measurement results are further discussed in the subsequent section.

III. Results

A. Microstructure Analysis

A three-dimensional model was generated for each processing parameter based on the sequential FIB process and computational reconstruction methodology mentioned earlier.

- **Model 1** – 200°C sintering temperature and 2 hours of sintering time
- **Model 2** – 250°C sintering temperature and 2 hours of sintering time
- **Model 3** – 200°C sintering temperature and 4 hours of sintering time

It is assumed that BLT does not influence the material's microstructure because it is a dimensional parameter. Hence, the discussion in this section did not involve the BLT parameter. A Representative Volume Element (RVE) needs to be specified for further steps. The Ag volume fraction of all three models was observed to be stable when the total volume was greater than 4500 μm^3. Accordingly, the RVE of all three models was chosen for total volume in the range of 4500 μm^3, which results in 2.2×10^8 voxels for each model.

The volume fraction of silver and the resin was further determined. The proportion of sintered silver was less than 50% for all three models, which influences the effective

thermal properties. To identify the interconnecting network of silver particles, a 26-neighbor-connectivity criterion (6 faces, 12 edges, and 8 vertexes) was defined for the connection between voxels [18]. The results indicated that the connectivity of the silver particles was above 99% for all three models, which suggests that those seemingly separated particles in **Figure 1b** were connected in three-dimensional space. Subsequently, the particle volume distribution was obtained by separating the connected silver particles. The distribution is graphically shown in **Figure 4** along with a 3D-rendered volume of each model. The particle volume distribution results suggest that increasing the sintering time from two to four hours at 200°C has a limited promotion effect on the formation of larger silver particles. **Figure 4a** and **4c** indicate that the amount of small-volume particles ($\leq 0.6\mu m^3$) is much greater than that of large-volume particles ($\geq 5\mu m^3$) when sintered at 200°C. However, sintering at higher temperatures (250°C) for two hours significantly promoted the formation of large particles $\geq 5\mu m^3$ (**Figure 4b**) as compared to sintering at 200°C (**Figure 4a & 4c**).

To understand the Ag particle connectivity, the tortuosity factors of all three models were determined. The tortuosity factor is often used to describe the transport properties in porous materials. The Tortuosity factor τ is defined in equation **1**, where D is the intrinsic diffusivity of the conductive material, D_{eff} is the effective diffusivity of the hybrid material, and ε is the volume fraction [18].

$$\tau = \varepsilon \frac{D}{D_{eff}} \tag{1}$$

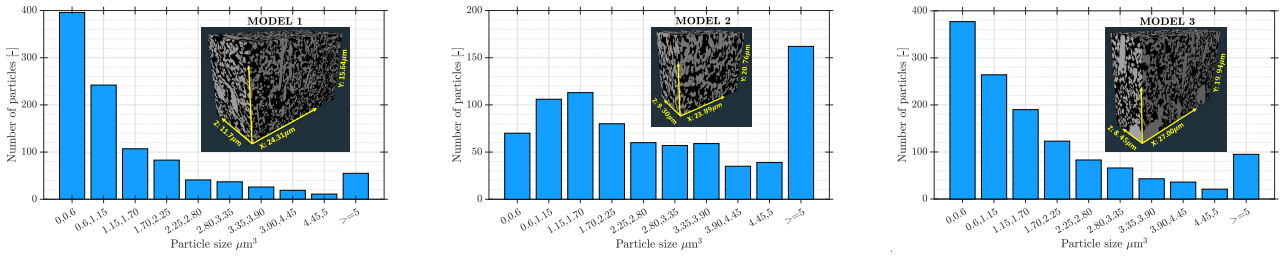
The tortuosity equation represents the diffusive flow of electrical current, heat transport, or mass transport in porous materials, which facilitates in determining the heat transport phenomenon of all three models shown in **Figure 4**. Using the Generate Pore Network Model (GPNM) in AVIZO, the tortuosity factor in all three principal directions (X, Y, and Z) were obtained through diffusion simulation, and the results are tabulated (**Table 1**). The tortuosity factor in the X-direction indicates heat transport along the die attach thickness (out-of-plane direction), and the YZ direction indicates the in-plane heat transport. Based on the estimated tortuosity factor, Model 2 indicates better thermal performance than Models 1 and 3.

The tortuosity factor in the X-direction for Model 2 (sintered at 250°C) is lower than Model 1 and 3 (sintered at 200°C), which suggests that the connection structure of silver particles in Model 2 has the shortest channel for heat dissipation along the die-attach thickness direction. Likewise, Model 2 also indicates the lowest tortuosity factor in the Y-direction. The tortuosity factor in the Z-direction, i.e., the milling direction exhibits a discrepancy as compared to the X and Y-direction, which can be due to insufficient length along the Z-axis. The anisotropy in the X, Y, and Z directions will not be addressed in this paper.

All microstructure findings are summarized in **Table 1**. The results indicate that all the aforementioned sintering conditions can achieve 99% connectivity of silver particles. However, sintering at 200°C does not lead to silver particles coarsening as observed from the particle volume distribution. Even prolonged sintering at 200°C has a limited effect in promoting silver particle growth. Sintering at 250°C for two hours results in silver particle coarsening, which was verified from particle volume distribution and

Table 1: The physical dimensions, the total volume, the fraction of Ag and Resin volume, the Tortuosity factor, and the Ag material's connectivity for all three models are tabulated below.

		Model 1 (200°C/2h)	**Model 2 (250°C/2h)**	**Model 3 (200°C/4h)**
Dimension (X × Y × Z) [μm]		24.3 × 15.6 × 11.7	23.8 × 20.7 × 9.3	27.0 × 19.9 × 8.4
Total Volume [μm^3]		4448.44	4613.38	4549.31
Ag Volume Fraction [%]		43.56	47.90	48.91
Resin Volume Fraction [%]		56.43	51.60	51.09
Tortuosity	**X**	1.79	**1.73**	1.77
	Y	1.77	**1.48**	1.62
	Z	1.51	1.70	1.50
Connectivity [%]		99.75	99.66	99.81



(a) **(b)** **(c)**

Figure 4: (a). The particle volume distribution is graphically shown with a 3D rendered volume of Model 1 (200°C sintering temperature and 2 hours of sintering time). A predominant amount of Ag particle volume is less than 0.6 μm^3. **(b).** The particle volume distribution of Model 2 (250°C sintering temperature and 2 hours of sintering time) is shown. When sintered at 250°C, the Ag particles coarsen, and a majority of the volume is more than or equal to 5 μm^3 **(c).** The particle volume distribution of Model 3 (200°C sintering temperature and 4 hours of sintering time) is shown. The Ag particle volume distribution for Model 3 shows similarities with Model 1.

tortuosity factor calculation. Model 2, representing 250°C for two hours sintering condition, has the lowest tortuosity factor along the interconnect thickness, indicating that it has the shortest heat transport channel between the die and substrate. To further quantify the results from the microstructural analysis, the transient thermal impedance of OMP packages with varying sintering conditions was experimentally measured, and the results are presented next.

B. Transient Thermal Impedance Measurement Results

As discussed in the methodology section, the device junction temperature of the various OMP packages fabricated with different sintering parameters was experimentally measured and shown in **Figure 5**. The differences in the steady-state temperature measured correspond to the variations in the packages. Normalizing the measured temperature with the applied input power provides the Junction-to-Ambient transient thermal impedance. However, the steady-state thermal impedance does not indicate the changes in the interface material (die and substrate metallizations + die-attach layer + contact interactions). Hence, the individual layer resistance and capacitance network were deconvoluted using TDIM-Master software and shown in **Figure 6a, 6b, & 6c**.

- **Figure 6a** indicates the cumulative resistance capacitance network of each layer measured for packages with different BLT but similar sintering temperature and time. The different layers in the packages are marked in the graph. The interface layer indicates a marginal increase in the effective thermal resistance for packages with 60μm BLT than with 20μm BLT.

- Likewise, **Figure 6b** indicates the cumulative resistance against the capacitance of each layer for packages with different sintering temperatures but uniform BLT and sintering time. It can be observed that the package sintered at 250°C has slightly lower resistance than the package sintered at 200°C.

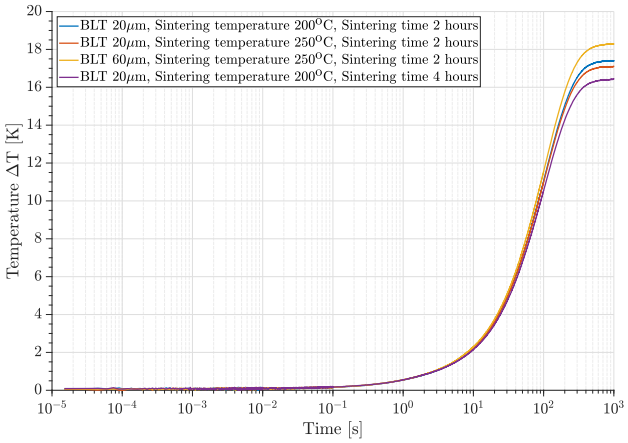
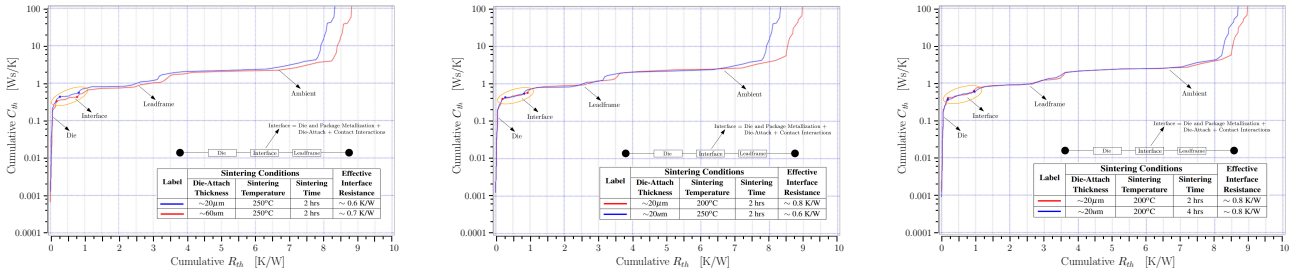


Figure 5: The device was heated by supplying continuous drain current I_D of 1A through the body diode for 1000 seconds and the change in device junction temperature ΔT was simultaneously measured at a very high frequency of 15μs for 100 seconds and 1μs from 100 to 1000 seconds. Normalizing the junction temperature with the input power provides the Junction to Ambient transient thermal impedance. The changes in the steady-state temperature observed are due to the overall packaging variations.

- Lastly, the effect of sintering time was analyzed and shown in **Figure 6c**, where the cumulative resistance-capacitance network for packages with different sintering time is shown. **Figure 6c** shows a more or less negligible difference between sintering at 200°C for two and four hours.

From **Figure 6**, the effective interface thermal resistance of different OMP packages was estimated by rounding off to its nearest decimal and the results are shown in **Table 2**. Assuming that the packages are identical except for their sintering parameters, the variation in the estimated thermal resistance values should correspond to different sintering conditions. The estimated interface thermal resistance from the high-frequency measurements shown in **Figure 5.** was very much repeatable provided the devices were measured in the same condition. However, for an average of two samples per type, the estimated effective thermal interface resistances were within ±0.2K/W, which is



(a) **(b)** **(c)**

Figure 6: (a). The cumulative resistance-capacitance network is deconvoluted for packages with different BLTs and shown. The highlighted region indicates that the package with a 20μm BLT has slightly lower interface resistance as compared to a package with a 60μm BLT. **(c).** The cumulative resistance-capacitance results for packages with different sintering temperatures are shown. The highlighted region indicates that the packages sintered at 250°C have slightly improved thermal performance than the packages sintered at 200°C. **(d).** The cumulative resistance-capacitance network deconvoluted for packages with different sintering time is shown. Negligible differences were observed for packages sintered between two and four hours.

Table 2: The effective interface resistance for different sintering conditions was estimated by rounding off to its nearest decimal. The thermal resistances mentioned are the effective heat transport property of the interface, which is cumulative of the semiconductor die's backs side metallization ($\sim 1\mu$m), Ag sintering material ($\sim 20/60\mu\text{m} \pm 10\mu$m), the metallization layer on the package substrate ($\sim 6\mu$m), and the contact heat transport interaction.

Sintering Conditions			Effective Interface Resistance
Bond-Line Thickness	Sintering Temperature	Sintering Time	
$\sim 20\mu$m	200°C	2 hrs	$\sim$ 0.8 K/W
$\sim 20\mu$m	250°C	2 hrs	$\sim$ 0.6 K/W
$\sim 60\mu$m	250°C	2 hrs	$\sim$ 0.7 K/W
$\sim 20\mu$m	200°C	4 hrs	$\sim$ 0.8 K/W

almost in the same range as the differences observed for various sintering conditions.

Although the transient thermal impedance methodology is less sensitive to quantitatively estimate the changes in the thin interconnect layer's thermal resistances due to different sintering conditions, the measurement results depicted in **Figure 6** correlate with the observations from the microstructural analysis. The packages sintered at 250°C have a slightly lower interface thermal resistance than the packages sintered at 200°C. The same applies also for packages with a thicker BLT ($\sim 60\mu$m) sintered at 250°C. As observed from the particle volume distribution (**Figure 4**), the experimental measurements shown in **Figure 6.** also indicates that varying the sintering time from two to four hours at 200°C does not cause any measurable differences in the interface layer. For future research, more samples are needed for larger data sets, and more sintering variations are recommended to quantify the results based on data distribution. Furthermore, the poor measurement sensitivity could be due to large thermal gradients on the die surface, which might require an active cooling block. However, considering that the experimental measurements and the microstructural analysis provide equivalent results suggests that sintering the resin-reinforced Ag sintering material at 250°C is more favorable for efficient package thermal performance.

IV. Conclusion

To realize high-efficiency-high-power electronic packages, novel materials such as resin-reinforced Ag sintering with favorable properties are needed to transition towards reliable lead-free solutions. However, the material's microstructure is strongly determined by its processing conditions. Besides, extracting the influence of a thin interconnect's thermal resistance from a packaged product remains challenging. Hence, a novel 3D reconstruction technique was implemented for microstructural investigation. Based on the 3D reconstructed models, Ag particles have 99% connectivity for all sintering conditions, i.e., 200°C for 2 hours, 200°C for 4 hours, and 250°C for 2 hours. The particle volume distribution indicated that the Ag particles coarsening is promoted when sintered at 250°C, and prolonged sintering time at 200°C had insignificant changes. The estimated tortuosity factor also suggests that sintering at 250°C provides the shortest heat transport path between the semiconductor die and the package substrate.

In order to quantify the microstructural findings, the transient thermal impedance of the over-molded packages with different sintering conditions was further measured. The transient thermal measurement methodology had low sensitivity in detecting changes to a thin interconnect layer's thermal resistance for different sintering conditions. However, the measurement results highlighted similar findings to the microstructural analysis, i.e., the packages sintered at 250°C seem to have lower thermal resistance than packages sintered at 200°C. Furthermore, the measurement results for packages sintered at 200°C for two and four hours had a similar thermal resistance, which also aligns with the microstructural investigation. The 3D reconstructed microstructural study and the transient thermal measurement analyses suggest that resin-reinforced Ag sintering material appears to have improved thermal performance when sintered at 250°C with two hours of sintering time. However, the obtained results need further validation. This research aimed to demonstrate new methodologies and understand thin interconnect's behavior on a packaged product. Such techniques are required to characterize the emerging novel materials for interconnect technology and to meet the needs of power device packaging.

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