A 117-dB In-Band CMRR 98.5-dB SNR Capacitance-to-Digital Converter for Sub-nm Displacement Sensing with an Electrically Floating Target

Jiang, Hui; Amani, Samira; Vogel, Johan G.; Shalmany, Saleh Heidary; Nihtianov, Stoyan

DOI
10.1109/LSSC.2019.2952851

Publication date
2020

Document Version
Final published version

Published in
IEEE Solid-State Circuits Letters

A 117-dB In-Band CMRR 98.5-dB SNR Capacitance-to-Digital Converter for Sub-nm Displacement Sensing With an Electrically Floating Target

Hui Jiang, *Student Member, IEEE*, Samira Amani, Johan G. Vogel, *Member, IEEE*, Saleh Heidary Shalmany, *Member, IEEE*, and Stoyan Nihtianov, *Senior Member, IEEE*

***Abstract*—This article describes a high-performance capacitance-to-digital converter (CDC) for sub-nm displacement sensing with an electrically floating target. Intended to be integrated into a displacement sensor probe, the CDC consumes only 560 μW. It achieves 98.5-dB SNR in a 1-ms conversion time. With a sensing $\emptyset$ 8-mm probe and a 25-μm stand-off distance from the target, it achieves 0.18-nm resolution. Moreover, it offers an in-band common-mode rejection ratio (CMRR) higher than 117 dB, providing decent electric field interference immunity.**

***Index Terms*—Capacitance-to-digital converter (CDC), chopping, electric field interference immunity, energy-efficient, readout, sub-nm displacement sensing.**

I. Introduction

Fully contactless displacement sensing with a sub-nm resolution is essential in high-precision mechatronic systems such as imaging systems with target on a moving chuck [1]. Conventionally, the displacement sensor is positioned and aligned manually, which is time-consuming and costly. It becomes more difficult if the sensor is located at an inaccessible location in the machine. Thus, a standalone displacement sensor with autonomously position and align capability is of great interest. A displacement sensor, consisting of a thermal stepper system and an eddy-current based displacement-to-digital converter (DDC), has been proposed [2], [3]. However, in order to mitigate the skin-effect and to attain sub-nm resolution within 1 ms of conversion time, a high excitation frequency (>100 MHz) was applied [3]. This resulted in relatively high-power dissipation (>10 mW) which can cause displacement errors due to self-heating, as the DDC has to be closely integrated with the eddy-current coil in the sensor head.

Capacitive DDCs are potentially more energy-efficient than eddy-current DDCs. However, conventional capacitive DDCs operate by connecting the target in a closed-loop configuration as shown in Fig. 1(a) [4]–[8]. This means that the target electrode must be connected to the same ground as the interface electronics, which is a major drawback compared to the eddy-current DDCs, as this makes the capacitive sensor not fully contactless. Even worse, the ground loop incorporating the target and the input of the electronic interface is susceptible to electromagnetic interference and acts as a source of parasitic capacitance, both of which degrade the sensor's performance.

To minimize the loop while offering fully contactless displacement sensing, readouts with electrically floating targets have been proposed [9], [10] [Fig. 1(b)]. The sensor readout employs two identical capacitive sensing electrodes, positioned close to the target electrode. This results in two capacitors in series ($C_{s1} = C_{s2} = C_s$), whose magnitudes equally vary with the distance, d, to the target. By exciting the capacitors with anti-phase voltages $\pm V_s$, the value of C_s can be obtained by measuring the charge Q_s. Compared to the conventional capacitive readout approach, it significantly reduces the area of the sensing loop and thus minimizes the error caused by the interfering magnetic fields [5]. However, such readouts with electrically floating targets are relatively power-hungry compared to conventional capacitive DDCs [7]. Moreover, any mismatch between the two sensing electrodes degrades the readout's common-mode rejection ratio (CMRR) and thus its electric field interference immunity [10]. To reduce the error caused by the misalignment of the probe and the target, the DDC needs a multichannel input to obtain an out-of-plane tilt angle.

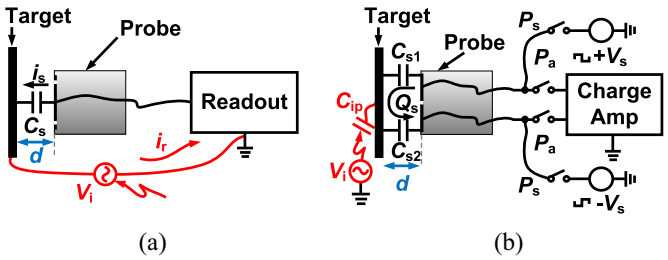


Fig. 1. (a) Conventional capacitive displacement sensing system. (b) Contactless capacitive displacement sensing with a floating target.

This article presents a three-channel capacitive DDC, with electrically floating target sensing capability [11], that overcomes these challenges while demonstrating an energy efficiency comparable to the state-of-the-art capacitive DDCs which do not support the use of electrically floating targets [4]–[8]. With a sensing probe size smaller than that in [3], it achieves a 0.18-nm resolution in a 1-ms conversion time, at a 25-μm stand-off distance to the target. Moreover, the interface consumes only 0.56 mW, which is 16 times lower than the state-of-the-art eddy-current DDC [3].

II. Operation Principle

A. Thermal Slider Actuator

To obtain an accurate displacement measurement, alignment of capacitive sensors is crucial. Self-alignment functionality integrated into the sensors reduces the cost of the conventional manual alignment, especially when they are installed at inaccessible locations in a machine. For this purpose, the thermal slider actuator (TSA) was developed [1].

Fig. 2(a) shows the actuator structure of the TSA. The position adjustment of the sensing probe is based on the thermal actuation of a number of fingers that clamp the probe. Fig. 2(b) shows an example of a thermal cycle of the fingers that leads to net displacement of the

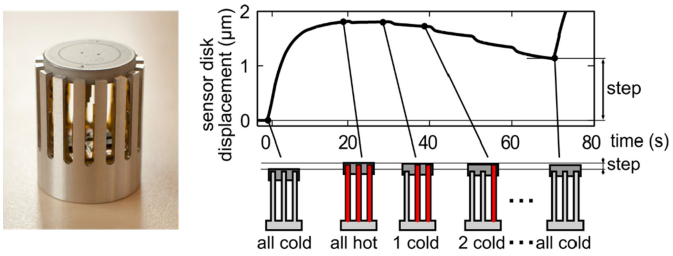
Manuscript received August 19, 2019; revised October 18, 2019; accepted November 1, 2019. Date of publication November 12, 2019; date of current version January 3, 2020. This article was approved by Associate Editor Nima Maghari. *(Corresponding author: Hui Jiang.)*

H. Jiang, J. G. Vogel, and S. Nihtianov are with the Department of Micro-Electronics and Computer Engineering, Technische Universiteit Delft, 2628 CD Delft, The Netherlands (e-mail: jianghuithu@gmail.com).

S. Amani is with the Business Development Department, Murata Electronics, 2132 JC Hoofddorp, The Netherlands.

S. H. Shalmany is with the Circuit Design Department, SiTime, 2612 PA Delft, The Netherlands.

Digital Object Identifier 10.1109/LSSC.2019.2952851



(a) (b)

Fig. 2. (a) TSA with 12 fingers. (b) Thermal cycle example and the resulting displacement profile [1].

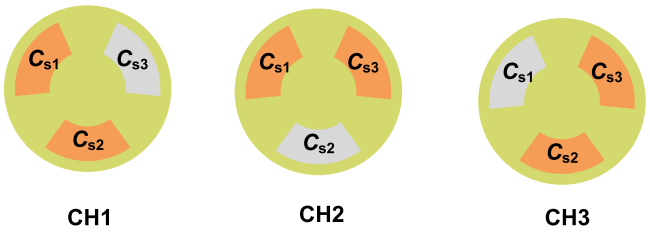


Fig. 3. Three electrode measurement for misalignment correction.

sensor probe. Heating of all elements together generates elongation by thermal expansion and moves the sensor probe to a new position. After that, the fingers are passively cooled one-by-one. When each finger cools, it slips over the probe surface, while the probe is kept in position by the other fingers. After the full thermal cycle, the probe has made a displacement step, while all fingers have cooled down and have returned to their original length. Because the actuation mechanism is fully switched off after positioning and the clamping is friction-based, the alignment obtained after actuation is maintained very stably [1].

B. Measurement Method for Misalignment Correction

Although the displacement with a floating target can be measured using two electrodes, misalignment of the probe and the target would lead to a sensing error. For this reason, a three-channel method is proposed. A third electrode is added to the probe (Fig. 3). Then, the probe capacitances can be measured through three channels CH: 1) CH1 ($C_{s1}+C_{s2}$); 2) CH2 ($C_{s1}+C_{s3}$); and 3) CH3 ($C_{s2}+C_{s3}$). As the tilt error causes mismatching errors among the measured results of CH1–CH3, the mismatching errors can then be used to minimize the tilt misalignment with the aid of self-alignment functionality of the TSA, matching the results of CH1–CH3.

III. Floating Capacitive Sensing Readout

In practical implementations, the parasitic capacitance between the floating target and its surrounding environment (C_{ip} up to 500 fF) introduces a major challenge. It forms a path for interfering electric fields, primarily created by mains lines (50/60 Hz). As shown in Fig. 1(b), the sensor front-end consists of a differential charge integrator with switched-capacitor excitation. C_{s1} and C_{s2} are periodically charged, delivering a signal charge $Q_s = (C_{s1} \cdot C_{s2}) \cdot (C_{s1}+C_{s2})V_{dd}$ to the integrator. An interfering signal V_i then couples into the target electrode via C_{ip}, resulting in a common-mode signal that will be rejected by the differential charge integrator.

However, a mismatch between the sensing electrodes ($C_{s1} \neq C_{s2}$), due to fabrication errors and/or alignment errors (θ), results in a deteriorated CMRR [10]. In this article, even with mismatched electrodes, a high CMRR is achieved by chopping the signal charge Q_i and

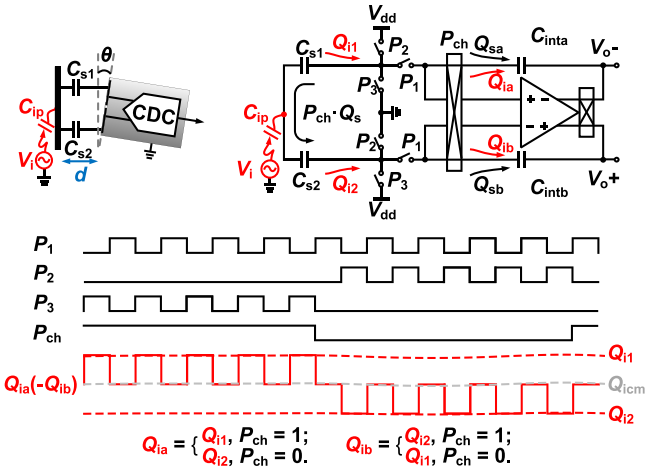


Fig. 4. Differential charge integrator with mismatched electrodes.

the integrating capacitors $C_{\text{int}a}$ and $C_{\text{int}b}$ (see Fig. 4). The input switches P_1–P_3 are controlled by the chopping signal P_{ch}, preserving the integration operation for C_s measurement. Due to the action of the input chopper, $C_{\text{int}a}$ and $C_{\text{int}b}$ continuously swap their position, such that $C_{\text{int}a}$ always accumulates negative charge (Q_{sa}), while $C_{\text{int}b}$ always accumulates positive charge (Q_{sb}). At the same time, the mismatched interference charges (Q_{i1} and Q_{i2}), as well as the offset and the $1/f$ noise of the integrator, are up-modulated to the out-of-band frequencies which will be filtered in digital domain.

In contrast to [10], which first converts Q_s into a proportional voltage and then digitizes it, this article directly embeds the charge integrator with sensing electrodes into a CDC, improving energy efficiency and reducing the number of potential error sources [5]. As shown in Fig. 5, the CDC is based on a second-order feedforward 1-bit sigma–delta modulator. The modulator's sampling frequency f_s is 1 MHz, enough to achieve the target resolution with an OSR of 1000, and the chopping frequency is set at 10 kHz to minimize quantization noise fold-back [12]. The differential signal charge Q_s is counterbalanced by a feedback DAC, in which C_{fb}=10 pF. Depending on the output bitstream, it delivers a charge of $\pm C_{fb}V_{dd}/2$. This charge-balancing results in an output bitstream with an average value of C_s/C_{fb}. To maximize the use of the CDC's available dynamic range, the modulator uses a programmable 5-bit trimming DAC to cancel the baseline capacitance, where $C_{T-\max} = 31$ pF.

As shown in Fig. 6, the first integrator is based on a folded-cascode OTA with an 84 dB dc gain and a transconductance about 1 ms to ensure the stability and accuracy for the worst case when the baseline cancelation capacitance is fully used. To achieve a lower intrinsic $1/f$ noise corner frequency for lower chopping frequency, pMOS input pairs have been chosen. The biasing circuitry and common mode feedback circuitry are not shown for simplicity. A passive summation network at the input of the quantizer combines the outputs of second integrator with that of the first integrator via the feedforward capacitors as shown in Fig. 5. The quantizer is implemented as a dynamic latch proceeded by two preamplifiers. Each preamplifier provides a gain of 5 while consuming 3 μA.

IV. Measurement Results

The CDC is realized in the 0.18-μm standard CMOS process and tested with sensing electrodes designed on PCB. The chip occupies an active area of 0.5 mm^2 and draws 313 μA, dominated by the first integrator, from a 1.8-V supply (Fig. 7). For flexibility, the decimation filter and digital controlling are implemented off-chip.

Fig. 8(a) shows the power spectral density (PSD) of the output bitstream. The CDC is thermal-noise-limited up to 1 kHz and achieves

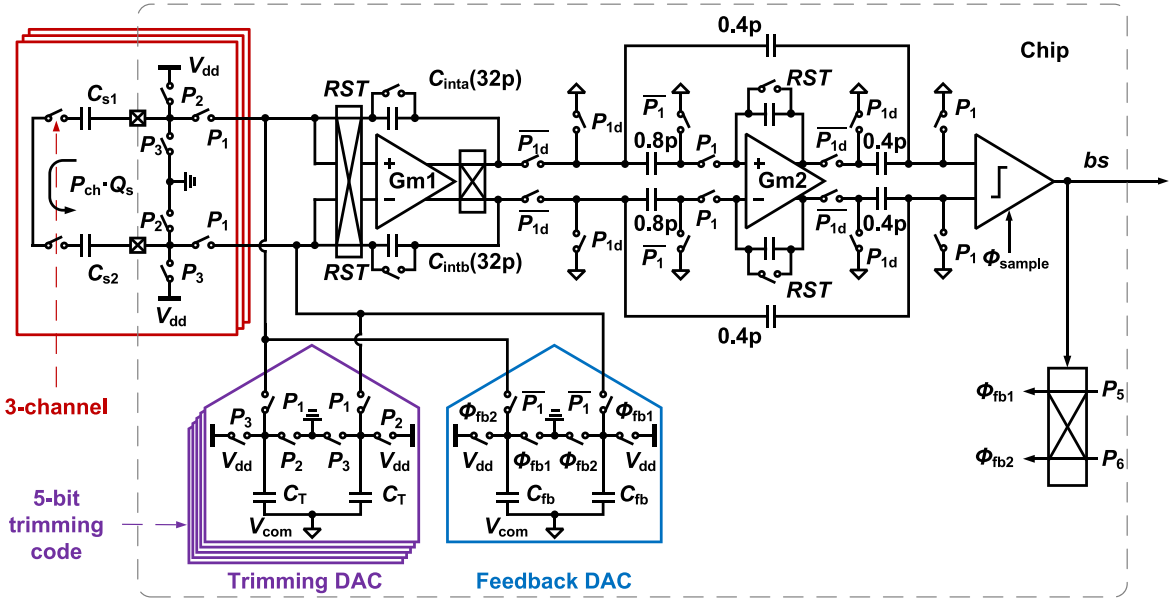


Fig. 5. Block diagram of the proposed three-channel CDC.

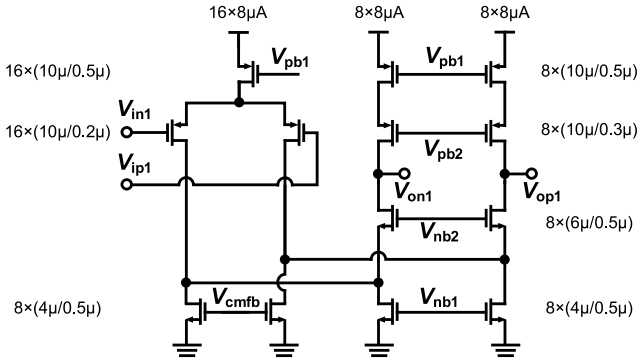


Fig. 6. Schematic of the first OTA and transistor-level parameters.

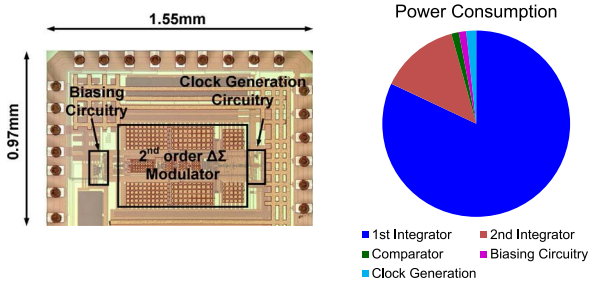


Fig. 7. Die micrograph of the CDC and power breakdown.

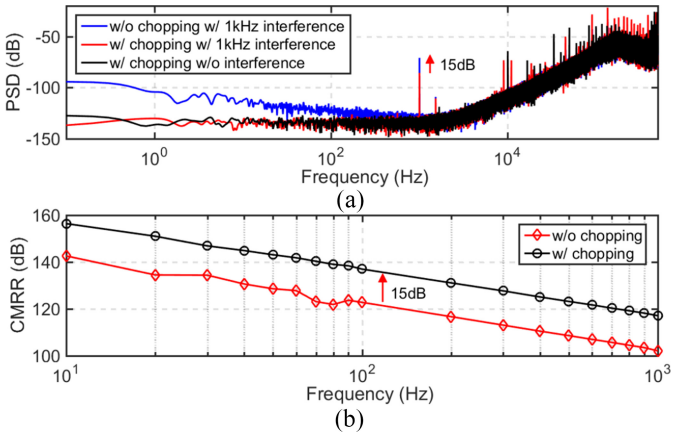


Fig. 8. (a) PSD of the CDC's bitstream. (b) Measured CMRR.

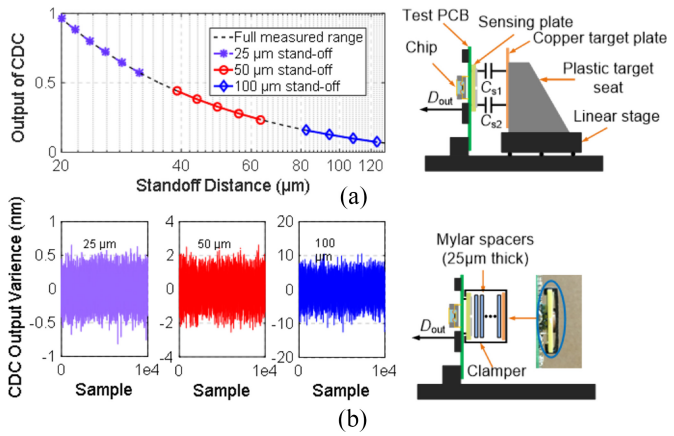


Fig. 9. (a) Measured displacement transfer characteristics. (b) Outputs of the CDC (10 000 decimated samples) with different stand-offs along.

42-aF resolution with a 10-pF dynamic range in a 1-ms conversion time. The electric field interference rejection capability is tested by injecting interferences of different frequencies into the floating electrode through a 10-pF capacitor (C_{ip} in Fig. 5) driven by a sinusoidal voltage of 20 Vpp. This is equivalent to injecting a 400 Vpp interference through a 500-fF capacitor, an order of magnitude larger than what is expected in practical applications. The CMRR, defined as the ratio between the power of the input interference signal and its power at the CDC output, is used to evaluate the interference rejection performance. As shown in Fig. 8(a), most of the interference power at 1 kHz is rejected by the differential architecture while chopping further suppresses the errors due to the mismatched electrodes ($< 1\%$), reducing the interference tone by 15 dB. As shown in Fig. 8(b), the in-band CMRR with chopping is more than 117 dB.

As shown in Fig. 9(a), an electrically floating target is moved relative to the probe, back and forth, over a number of logarithmically spaced steps between 20 and 130 μm in two cycles and

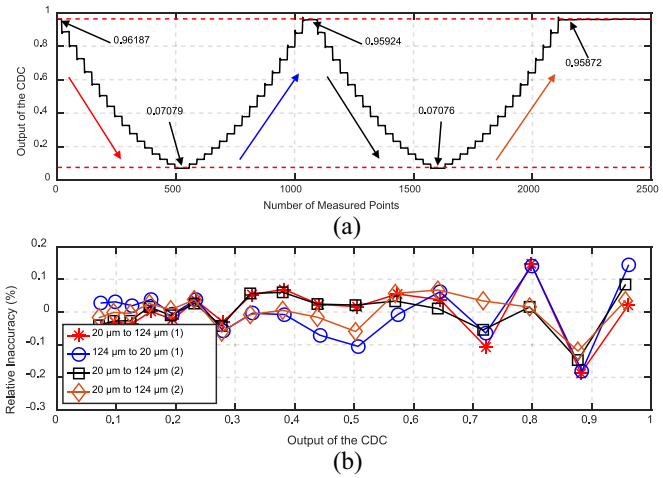


Fig. 10. (a) Real-time measurement. (b) Relative inaccuracy.

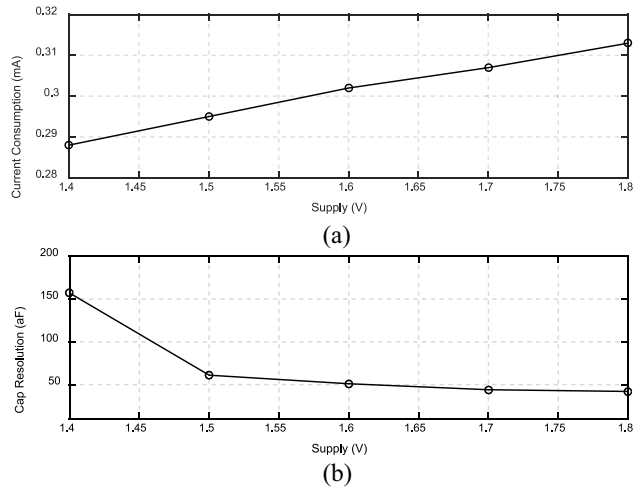


Fig. 11. (a) Current consumption versus supply. (b) Resolution versus supply.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This work	[5]	[6]	[7]	[8]	[10]
Technology (µm)	**0.18**	0.35	0.35	0.16	0.16	--
Floating target	**Yes**	No	No	No	No	Yes
Power (mW)	**0.56**	14.9	0.76	0.003	0.014	121*
Cap-range (pF)	**0-10**	8-12	6-22	0-3.8	0-8	0-10
SNR (dB)	**98.5**	84.8	102.6	114.6	80.9	81.3
Conversion time (ms)	**1**	0.02	10.5	100	6.86	0.1
FoM (pJ/Conv.-step)	**8.0**	20.9	74	0.76	10.4	369*

* Without considering the power consumption of the ADC.

the displacement transfer characteristic is measured. To evaluate displacement resolution, the target electrode is firmly positioned using a clamp and Mylar spacer foil to avoid mechanical interference. The displacement sensing resolutions, obtained from the standard deviation of 10 000 decimated samples, are found to be 0.18, 0.72, and 3 nm at standoffs of 25, 50, and 100 μm, respectively [Fig. 9(b)]. The real-time output of the CDC is shown in Fig. 10(a). The measured backlash of the system is below 0.4%. The relative inaccuracy is about 0.2% [Fig. 10(b)].

The current consumption of the CDC versus supply voltage is shown in Fig. 11(a). The CDC can work with a supply down to 1.5 V, achieving a capacitance resolution better than 61 aFrms, which is mainly limited by the kT/C noise [Fig. 11(b)].

Table I summarizes the performance of the CDC and the state-of-the-art. Compared to conventional CDCs [5]–[8], the proposed CDC offers floating target sensing capability, while achieving a similar energy efficiency. Moreover, compared to a state-of-the-art inductive DDC [3], it achieves 10× better resolution with 16× low-power consumption.

V. CONCLUSION

An energy-efficient CDC for a capacitive position sensor, with an electrically floating target, has been designed, implemented, and tested in a standard 0.18-μm CMOS technology. The interface embeds the push-pull principle in a second-order $\Sigma\Delta$ modulator. The experimental results show that it achieves a 98.5-dB SNR within 1-ms conversion time. The proposed CDC has an in-band CMRR higher than 117 dB and achieves comparable resolution FoM while being the only design offering floating target sensing capability.

REFERENCES

[1] O. S. van de Ven, J. G. Vogel, S. Xia, J. W. Spronck, and S. Nihtianov, "Self-Aligning and self-calibrating capacitive sensor system for displacement measurement in inaccessible industrial environments," *IEEE Trans. Instrum. Meas.*, vol. 67, no. 2, pp. 350–358, Feb. 2018.

[2] M. R. Nabavi, M. A. P. Pertijs, and S. Nihtianov, "An interface for Eddy-current displacement sensors with 15-bit resolution and 20 MHz excitation," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2868–2881, Nov. 2013.

[3] V. Chaturvedi, J. G. Vogel, K. A. A. Makinwa, and S. Nihtianov, "A 9.1 mW inductive displacement-to-digital converter with 1.85 nm resolution," in *Proc. Symp. VLSI Circuits*, Kyoto, Japan, 2017, pp. C80–C81.

[4] A. Heidary and G. C. M. Meijer, "Features and design constraints for an optimized SC front-end circuit for capacitive sensors with a wide dynamic range," *IEEE J. Solid-State Circuits*, vol. 43, no. 7, pp. 1609–1616, Jul. 2008.

[5] S. Xia, K. Makinwa, and S. Nihtianov, "A capacitance-to-digital converter for displacement sensing with 17b resolution and 20μs conversion time," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, 2012, pp. 198–199.

[6] R. Yang, M. A. P. Pertijs, and S. Nihtianov, "A precision capacitance-to-digital converter with 16.7-bit ENOB and 7.5-ppm/°C thermal drift," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 3018–3031, Nov. 2017.

[7] B. Yousefzadeh, W. Wu, B. Buter, K. Makinwa, and M. Pertijs, "A compact sensor readout circuit with combined temperature, capacitance and voltage sensing functionality," in *Proc. Symp. VLSI Circuits*, Kyoto, Japan, 2017, pp. 1–2.

[8] Y. He, Z.-Y. Chang, L. Pakula, S. H. Shalmany, and M. Pertijs, "A 0.05mm^2 1V capacitance-to-digital converter based on period modulation," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, 2015, pp. 1–3.

[9] "Capacitive sensor," Tech. Note, LT03–0022, Lion Precision, Oakdale, MN, USA, 2013.

[10] X. Guo and S. N. Nihtianov, "A capacitive sensing technique for measuring displacement with one floating target electrode," in *Proc. IEEE Int. Conf. Ind. Technol.*, Mar. 2010, pp. 1565–1570.

[11] H. Jiang, S. Amani, J. G. Vogel, S. H. Shalmany, and S. Nihtianov, "A 117DB in-band CMRR 98.5DB SNR capacitance-to-digital converter for sub-NM displacement sensing with an electrically floating target," in *Proc. IEEE Symp. VLSI Circuits*, Honolulu, HI, USA, 2018, pp. 159–160.

[12] H. Jiang, C. Ligouras, S. Nihtianov, and K. A. A. Makinwa, "A 4.5 nV/$\sqrt{}$Hz capacitively coupled continuous-time sigma-delta modulator with an energy-efficient chopping scheme," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 1, pp. 18–21, Jan. 2018.