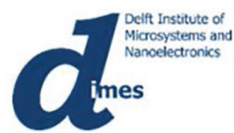
Development of Silicon Drift Detectors using Boron layer technology

Negin Golshani

Negin Golshani Development of Silicon Drift Detectors using Boron layer technology Delft 2015



Development
of
Silicon Drift Detectors
using
Boron layer technology

Negin Golshani

Development of Silicon Drift Detectors using Boron layer technology

PROEFSCHRIFT

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus Prof. ir. K. C. A. M. Luyben,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op

maandag 29 juni 2015 om 10:00 uur

door

Negin GOLSHANI

Elektrotechnisch ingenieur, Technische Universiteit Delft
Geboren te Uromieh, Iran

This dissertation has been approved by the
promotor: Prof. Dr. C. I. M. Beenakker and
copromotor: Dr. R. Ishihara

Composition of the doctoral committee:

Rector Magnificus	chairman
Prof. Dr. C. I. M. Beenakker	promotor
Dr. R. Ishihara	copromotor

Independent members:

Prof. Dr. G.Q. Zhang	EWI TU Delft
Prof. Dr. E. Charbon	EWI TU Delft
Prof. Dr. Ir. H. van der Graaf	Nikhef Amsterdam/TNW TU Delft
Prof. Dr. Mutsuko Hatano	Tokyo Institute of Technology, Japan

Other member:

Dr R. Woltjer	Novioscan, Nijmegen

Negin Golshani,
Development of Silicon Drift Detectors using Boron layer technology,
Ph.D. Thesis, Delft University of Technology,
with summary in Dutch.

The research presented in this thesis was financially supported by NanoNextNL, a micro and nanotechnology program of the Dutch Government, and 130 partners. Project number 09A.03.

Keywords: X-ray detector, Silicon drift detector, Thin entrance window SDD, PureB SDD, continuous SDD, constant field SDD, boron layer, dual PureB layer, ZrN diffusion barrier, PureB high-Ohmic resistor, silicon interposer package, on-chip front-end electronics, PureB JFET.

ISBN: 978-94-6186-497-0

Copyright © 2015 by Negin Golshani
Cover design: Negin Golshani

All rights reserved. No part of this publication may be reproduced, stored in a retrieval system, or transmitted in any form or by any means without the prior written permission of the copyright owner.

To Hedayat, Ferangiz

Jaber, Ouldouz and Mohammad

Contents

1 Introduction **1**

1.1 X-Ray detectors 1

1.1.1 Gas-filled detectors 1

1.1.2 Scintillation detectors 2

1.1.3 Semiconductor detectors 3

1.2 Silicon X-Ray detectors 4

1.2.1 PIN Diode 4

1.2.2 Silicon Lithium detector 5

1.2.3 Silicon strip detector 6

1.2.4 Silicon pixel detector 7

1.2.5 Charge coupled devices (CCD) 8

1.3 Silicon Drift Detectors (SDDs) 8

1.3.1 Circular silicon drift detector 9

1.3.2 SDD droplet (SD^3) 10

1.3.3 Multichannel SDDs 11

1.3.4 3D detector 12

1.4 Outline of the thesis 13

2 Pure boron layer properties and applications **15**

2.1 Introduction 15

2.2 Pure Boron layer with CVD deposition 16

2.3 Pure Boron diodes 18

2.4 High-Ohmic Pure Boron resistors 19

2.5 Protection, functional and diffusion barrier layers for PureB detectors 26

2.5.1 PureB and Ti/TiN layers as a diffusion barrier 27

2.5.2 ZrN as a diffusion barrier between boron layer and pure Al 30

2.5.3 Functional and protection layers 33

2.5.4 Lift-off process for PureB diode fabrication 34

2.6 Lower leakage current by double boron layer deposition 35

2.7 Conclusions 36

3 Designing Silicon Drift Detectors using PureB layer **39**

3.1 Introduction 39

3.2 Working principles of PIN and silicon drift detectors 39

3.3 Design considerations for silicon drift detectors 43

3.3.1 Selection of starting material 43

3.3.2 Entrance window 45
3.3.3 Biasing potential 46
3.3.4 Leakage current components in SDD 47
3.3.5 Sink Anode 50
3.3.6 Optimizing the detector size 50
3.3.7 Optimizing the drift field 51
3.3.8 Spatial spread in the pocket width of carriers 52
3.3.9 Pitch of drift rings 53
3.3.10 Integrated voltage divider 53
3.3.11 Minimizing capacitances. 54
3.3.12 Guard ring 54
3.4 Applications of PureB in silicon drift detectors 55
3.4.1 SDD entrance window using boron layer 55
3.4.2 Comparing potential distribution in PIN detector and SDD 56
3.4.3 Voltage divider using boron layer and implantation 57
3.4.4 Potential distribution in continuous SDD using one boron layer. 59
3.4.5 Potential distribution in constant field SDD using dual boron layers 66
3.5 Overview of designed SDDs using the boron layer 69
3.6 Conclusions 70

4 Integrating on-chip electronics and multi-guard rings in PureB-SDDs 73

4.1 Integrating n-channel JFET and reset devices in SDDs 73
4.1.1 Introduction 73
4.1.2 Noise considerations in SDDs 75
4.1.3 Choice of the front-end transistor. 78
4.1.4 Reset mechanisms 80
4.1.5 Designed on-chip JFET and reset devices in boron layer technology. 82
4.2 Multi-guard ring structures for SDDs 86
4.2.1 Introduction 86
4.2.2 Multi-guard ring design 88
4.2.3 Fabrication process 91
4.2.4 Identifying the breakdown mechanism 93
4.2.5 Breakdown voltage measurement in a bulk PN diode 94
4.2.6 Electrical measurements of multi-guard ring structures 97
4.3 Conclusions 100

5 Fabrication and characterization of PureB-SDDs 103

5.1 Introduction 103
5.2 Fabrication process flow of PureB-SDDs 103
5.2.1 Single PureB-SDD process flow. 103
5.2.2 Dual PureB-SDD process flow. 106
5.2.3 Dual PureB-SDD process flow with on-chip electronics 108
5.3 Characterization of fabricated SDDs 112
5.3.1 Starting materials 112

5.3.2 Electrical measurements setup 112
5.3.3 Extracting doping profile of high resistivity silicon wafers 113
5.3.4 Extracting generation life time and surface generation velocity 115
5.3.5 High-Ohmic PureB resistors as a voltage divider for SDDs 117
5.3.6 Electrical measurement of high-Ohmic resistors in SDDs 119
5.3.7 Leakage current measurement setup 121
5.3.8 Impact of passivation layer thickness on leakage current 123
5.3.9 Impact of thermal annealing on leakage current 124
5.3.10 Influence of field plate on measured leakage current 125
5.3.11 Influence of two times boron layer deposition on leakage current. 127
5.3.12 Comparing leakage current of fabricated PureB-SDDs 127
5.3.13 Characterization of on-chip amplifier (JFET) 129
5.4 A novel silicon interposer for SDD measurement 130
5.4.1 Fabrication process 131
5.4.2 Measurement results 133
5.5 Conclusions 134

6 Conclusions and recommendations 137
6.1 Conclusions 137
6.2 Recommendations 141

Bibliography 143

List of symbols and abbreviations 153

Summary 157

Samenvatting 167

List of publications 177

Acknowledgments 183

About the author 185

Chapter 1

Introduction

1.1 X-Ray Detectors

Radiation detectors are used in a large variety of fields such as medicine, security, defense, geophysics, industry and physics. They have been developed to detect the energy or position of radiation or charge particles. In this chapter different types of X-ray detectors, their operation principles and performance will be studied briefly. X-ray detectors can be divided into three categories: gas-filled detectors, scintillation detectors and semiconductor detectors.

1.1.1 Gas-Filled Detectors

In gas-filled detectors, X-ray photons ionize inert gas atoms such as Argon or Xenon into positive ions and free electrons. The typical ionization energy required to eject an outer electron is 30eV. An incoming photon can create a number of electron and ion pairs proportional to its energy. An electric field across the gas chamber separates the electron and ions. The electrons are collected at a thin wire anode inside of the chamber. Depend on the applied voltage and the geometry of the chamber a few types of detectors exist. In the ionization chamber a low electric field of about 100V/cm extracts all ions and electrons before they recombine. In a proportional counter the electric field near the anode is high enough for electrons to create an avalanche effect. In the Geiger-Mueller counter, the electric field is even higher so that UV-photons are created. Generated UV photons can start new avalanches and make the signal very strong. The main advantage of the gas-filled detector is the possibility of charge gain, thus a high value for the signal to noise ratio (SNR). The main disadvantage of the gas

detector is a very low density of the gas that results in low efficiency for X-ray detection [1]. Figure 1.1 illustrates a schematic of gas filled detectors.

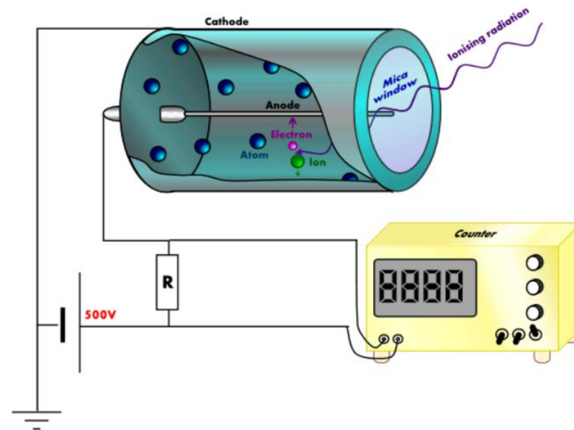


Figure 1.1: Schematic of gas-filled detectors consisting of a glass tube with a wire anode and metal tube as the cathode [2].

1.1.2 Scintillation Detectors

In scintillation detectors, X-ray photons are converted into an electrical signal in two steps. X-ray photons collide with the scintillator and a photon in UV or visible light is released when an excited electron in the scintillator returns to its ground state. The produced photons will be converted into an electrical signal in the photomultiplier tube (PMT) or photodiode. There are two types of scintillators: organic and inorganic scintillators. The scintillation mechanism is different for these two types. Using a large area of a scintillator coupled to a large number of photodiodes, a high efficiency image detector can be obtained for medical applications. The main disadvantage of scintillation detectors is their poor energy resolution, because of a large amount of loss, and the relatively high ionization energy such as 20-500eV [1]. Figure 1.2 displays basic principle of the scintillation detectors showing loss in scintillation material.

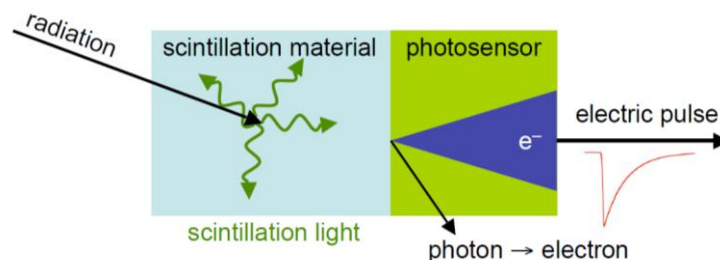


Figure 1.2: Basic principle of scintillation detectors [3].

1.1.3 Semiconductor Detectors

Semiconductor detectors are the most common radiation detectors because they have not only higher energy resolution than scintillators, but also higher density and higher interaction than gaseous detectors. In semiconductor detectors, charge carriers are electron-hole pairs which are created at a much lower energy than gas counter ionization energy. With semiconductor detectors it is possible to measure the simultaneous precise position and energy of the radiation. Accurate position measurement with high read out speed, integrating detector and readout electronics on a common substrate are other advantages of the semiconductor detectors over other types of detectors [4]. The disadvantage of semiconductor detectors is that they do not have any gain. There is no intrinsic amplification mechanism. Therefore they need an amplifier to amplify the small signal. This will be discussed in more detail in Chapter 4. Table 1.1 summarizes the physical properties such as density (ρ), atomic number (Z), band gap energy (E_g), ionization energy (E_{ion}) and mobility (μ) in different semiconductors.

Table 1.1: Comparison of properties of popular semiconductors for X-ray applications [5,6,7].

Semiconductor		Si	Ge	GaAs	SiC	CdTe	Diamond
Atomic number Z		14	32	31/33	14/12	48/52	6
Density ρ	g/cm^3	2.33	5.33	5.32	3.21	6.20	3.5
Band gap E_g	eV	1.12	0.66	1.42	3.0	1.44	5.5
Ionization energy E_i	eV	3.65	2.85	4.2	8.5	4.7	~13
Electron mobility μ_e	cm2/Vs	1500	3900	8500	1000		1800 (crystal)
Hole mobility μ_h	cm2/Vs	450	1900	400	100		1200 (crystal)
Minority carrier lifetime τ	s	2.5×10^{-3}	10^{-3}	10^{-8}	10^{-6}		
Intrinsic resistivity	Ωcm	2.3×10^5	47	10^8	$>10^{12}$		$>10^{11}$
Intrinsic carrier con.	cm^{-3}	1.45×10^{10}	2.5×10^{13}	1.8×10^6	10^{-6}		

In this table, density (ρ) and atomic number (Z) are interesting parameters in absorption efficiency. In order to obtain a large absorption probability or higher absorption efficiency, density and atomic number should be as large as possible. Band gap energy is another important parameter to be considered. Lower band gap is good for resolution, although detectors made with lower band gap material will have higher leakage current at room temperature and cooling will be needed. For instance, SiC detectors, with 3.0eV band gap energy, have the leakage current of $1pA/cm^2$ while detectors made with Si have $1nA/cm^2$ leakage current. Mobility is another important parameter in detectors. As it can be observed from Table 1, GaAs has electron mobility almost 6 times higher than Si, which enables it to be

one of the fast detectors. Figure 1.3 plots absorption efficiency of different semiconductors. It shows that GaAs with a higher density and atomic number has higher absorption efficiency than Si. Moreover, a thicker substrate has higher absorption efficiency [8,9,4].

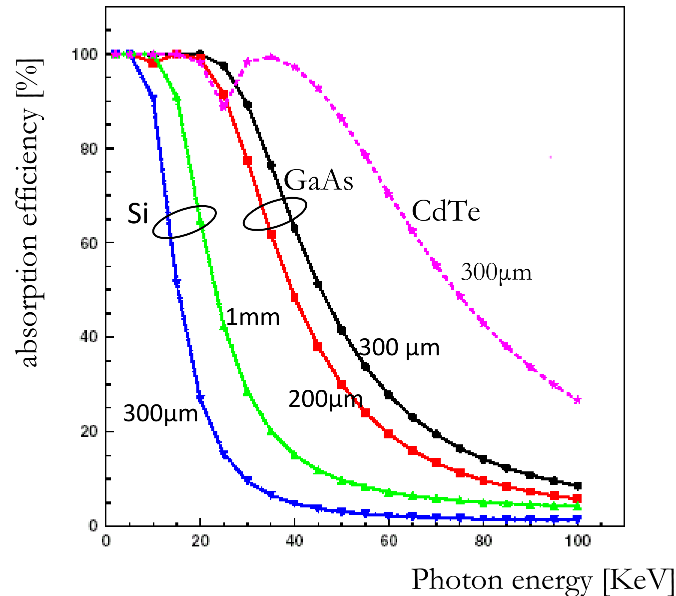


Figure 1.3: Photon absorption efficiencies for different Z and thickness of semiconductors [8].

1.2 Silicon X-Ray Detectors

Different criteria are applied in choosing the detector material such as properties of the intrinsic semiconductor, technological facilities, economic considerations and integration of electronics possibility. Between semiconductors, Silicon does not have exclusive properties for radiation detection, but Si detectors can be fabricated by common IC processing making integration of electronics possible [4]. Here some Si detectors are mentioned with the exception of Silicon Drift Detectors, which are discussed in detail in the next section.

1.2.1 PIN Diode

The simplest semiconductor radiation detector is the PIN photodiode biased in the reverse region. Figure 1.4 shows a PIN diode as a radiation detector made in an n-type high resistivity silicon wafer. The three regions, n^+, Intrinsic and p^+, are

shown. One side of the detector is an n^+n junction which provides good ohmic contact, and on the other side there is a p^+n junction as a rectifying junction. The guard ring is necessary to prevent current generated at the edge of the detector from being collected, which would increase the noise. The potential difference applied to the contacts should be high enough to deplete the complete thickness of the substrate in order to obtain the best detection efficiency [9,10,11]. When the detector is illuminated, the energy absorbed in Si creates pairs of electrons and holes. Generated electron-hole pairs will be extracted by the electric field and moved toward the electrodes. The number of electron-hole pairs is equal to $\frac{E}{E_i}$ where E is the absorbed energy and E_i is equal to the effective ionization energy, which is 3.6eV for Si. In The PIN diode, for minimum ionizing particles the typical signal charge is 3.5fC (22000 electrons) and the typical transit time is 10-20ns for a 300μm-thick Si wafer. The resolution for the 5.9 keV peak of ^{55}Fe is reported to be 145 eV FWHM to 230 eV FWHM depending on the detector type and shaping time constant [12,13,14].

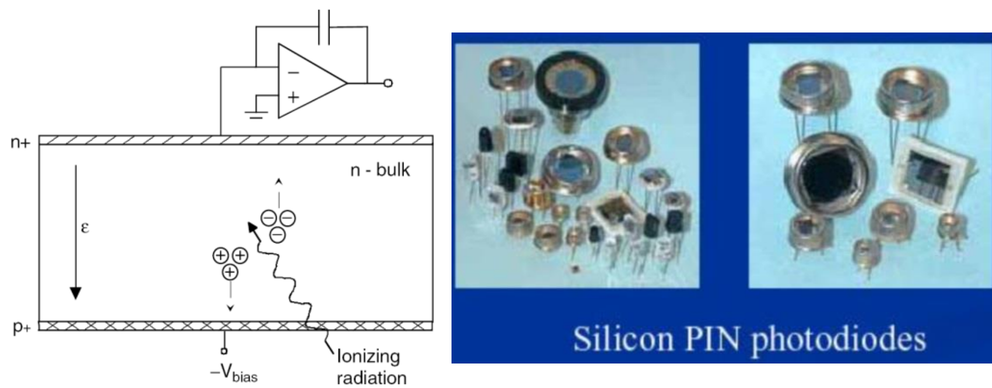


Figure 1.4: Basic structure of a PIN diode and working principle [1,15].

The PIN detectors are inexpensive with a small transition time. However, since they have a large anode area, the result is a large output capacitance with a high noise. To reduce the noise either the detector size should be small or the structure should be changed.

1.2.2 Silicon Lithium Detector

The first Ge(Li) and Si(Li) detectors were produced in the early 1960s.They offered much higher energy resolution than gas detectors and scintillators. Ionization energy in semiconductors is lower than in gases detectors. Therefore

in the semiconductor detectors, more charge is generated. Furthermore, higher charges allow direct measurement by low noise electronics [1]. The structure of a Silicon Lithium Si(Li) detector is the same as the PIN detector. Figure 1.5 shows a schematic of a Si(Li) detector with a thick Si crystal and gold contacts at its ends. Very low doped silicon with around 1cm thickness is required for this detector. For this purposes the lithium drifting process is used to create a near intrinsic silicon region with a thickness of a few mm up to 1cm and typical bias voltages of 500 - 4000V [12,16]. Lithium acts as a donor to compensate the acceptor ions to obtain a concentration level as low as 10^9 cm^{-3}. The main disadvantage of Si(Li) detectors is their need for liquid nitrogen cooling to prevent redistribution of lithium ions.

Energy resolutions for Si(Li) detectors with active areas of 10, 30, 50, 80 (mm^2) have been reported 127, 133, 139, 148 eV FWHM at 5.9 KeV Mn Ka.[17]. Depending on the thickness, Si(Li) detectors are usually used for detection of X-rays with energy up to 60 keV.

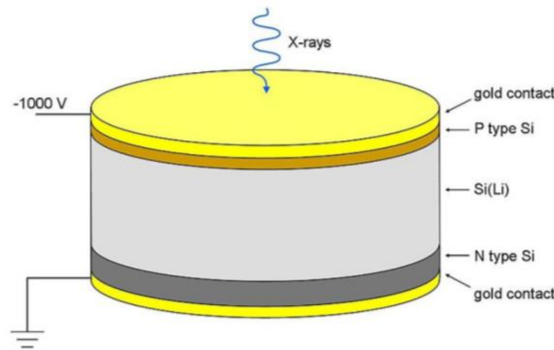


Figure 1.5: Silicon Lithium Si(Li) detector [17].

1.2.3 Silicon Strip Detector

In order to obtain a position sensitive detector, it is possible to divide a p^+n junction of a large PIN diode into many small (strip or pixel-like) regions and connecting them to readout electrodes separately as illustrated in Figure 1.6 The strips are typically 8-15 µm wide with 25-50µm pitch and can be 5-8cm long. The potential applied to all strips is the same and the detector is fully depleted. After ionization, created electron-hole pairs move toward the electrodes. The holes will be collected in one or more p^+ strips. In this way a 1D position sensitive detector is obtained. A 2D position sensitive detector can be realized by dividing the n^+n

junction on the other side of the detector as shown in Figure 1.6, where electrons are collected [18].

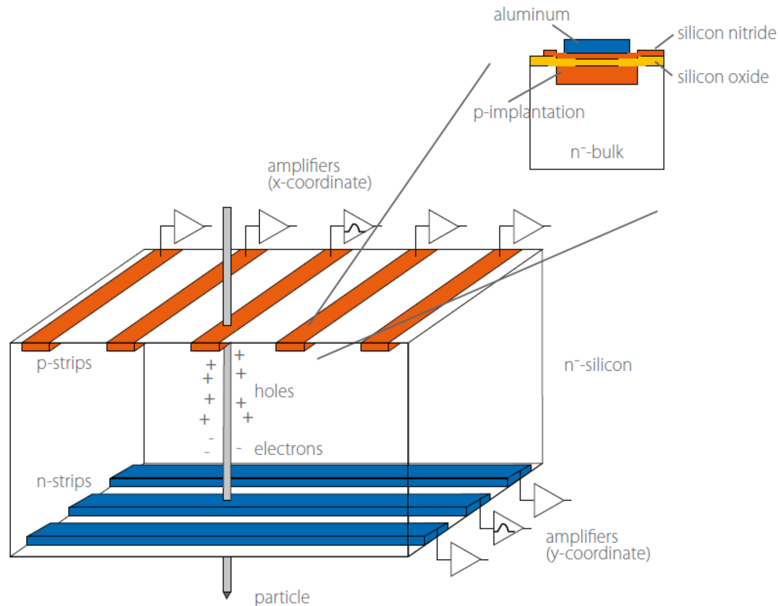


Figure 1.6: Schematic of double sided strip detector [18].

1.2.4 Silicon Pixel Detector (SPD)

A pixel detector is a 2D position sensitive detector. The main advantage of this detector is patterning a p^+n junction only in one side of the detector. This simplifies fabrication and mounting of an electronic silicon chip on the detector. Pixels with dimensions of 50×400 μm² have been reported [19]. For each pixel an electronic readout is attached with a bump solder bonding technique to amplify the signal as shown in Figure 1.7 [20,4]. In this detector, resolution is determined by pixel dimension and is typically similar to a strip detector.

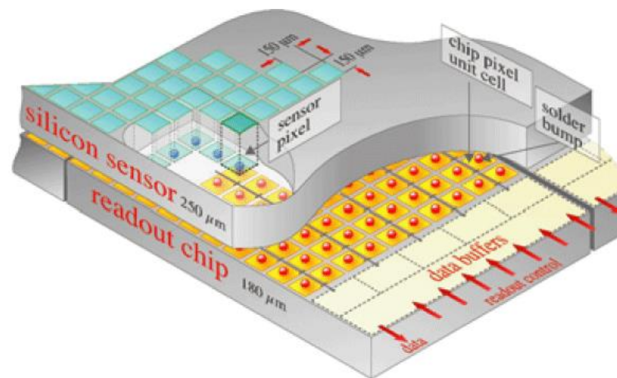


Figure 1.7: Schematic of silicon pixel detector [20].

1.2.5 Charge Coupled Devices (CCD)

Charge Coupled Devices (CCDs) were invented by W. Boyle in 1970 [21]. They have been used for several years in electronic devices as optical image sensors, charge storage devices and particle detectors. For different applications, there are different kinds of CCDs such as MOS, buried- channel and p-n CCDs.
For particle detection p-n CCDs are being used which is shown in Figure 1.8. The operation is similar to SDD where the drift function is carried out by reverse and forward biases of pn-junctions in periodic cycles by external pulses to act as a series of shift registers and push the electrons toward the anode. The location of minimum potential can be adjusted by biasing. Typical depletion voltage on the backside is −150V [1].

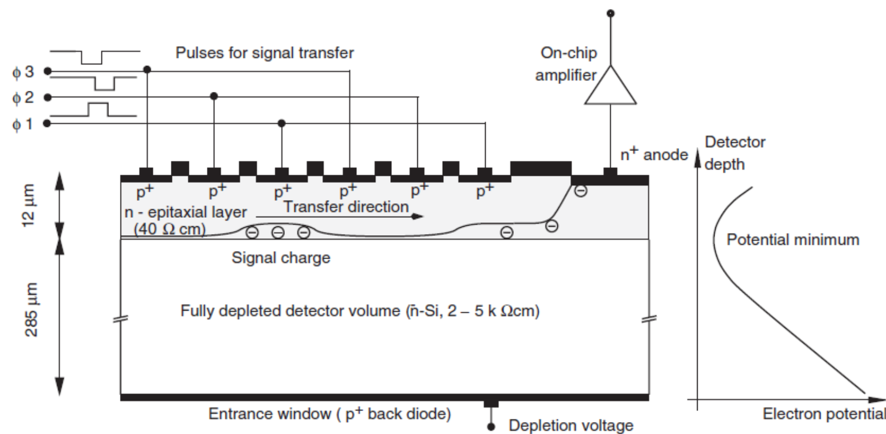


Figure 1.8: Schematic and principle working of pn-CCDs for particle detectors [1].

These types of detectors have been developed for astrophysics experiments in space, material analysis and experiments at synchrotron radiation facilities. Typical pn-CCD detectors can deliver position accuracy in the order of tens of microns, energy of about 140eV (FWHM at 6 keV), and high quantum efficiency above 90% at soft and medium energy X-rays from 0.5KeV to 10KeV. The low energy response is given by the very shallow implant of the p+ in the back contact resulting effective “dead” layer of 200Å [1].

1.3 Silicon Drift Detectors (SDDs)

The silicon drift detector, which was introduced by E.Gatti and P.Rehak in 1983, is a detector with very low anode capacitance [22]. This detector has a low electronic noise and it is one of the high energy resolution detectors. Silicon drift detectors can be used as a position sensitive or energy dispersive detector as well.

SDDs are well suitable for high resolution, high count rate X-ray spectroscopy [23], and they are used in electron microscopy (SEM-EDS) [24], and X-ray fluorescence analysis (XRF) [25].

1.3.1 Circular Silicon Drift Detector

In the conventional circular silicon drift detector, the p^+ junctions on the front (device) side of the detector are defined in such a way that an electric field parallel to the surface is created to drift the electrons toward the small sized collecting anode. An integrated voltage divider is used to bias the drift rings so that only the innermost and the outermost rings are biased externally [26]. On the back side (entrance window) of the device, a non-structured shallow implanted junction gives a homogeneous sensitivity over the whole detector area [27]. Moreover, using the back side as an entrance window has a self-shielding effect because the radiation sensitive components are placed on the device side and can only be hit by hard X-rays (> 10keV), whose intensity is reduced by the absorption of the silicon bulk [23].
The back contact is kept at a constant negative potential to fully deplete the detector and creates an electric field component perpendicular to the detector surface [28,29]. Figure 1.9 shows a schematic of a circular SDD. Capacitance of the SDD is very low typically in the range of 60fF and it is independent of the active area [30].

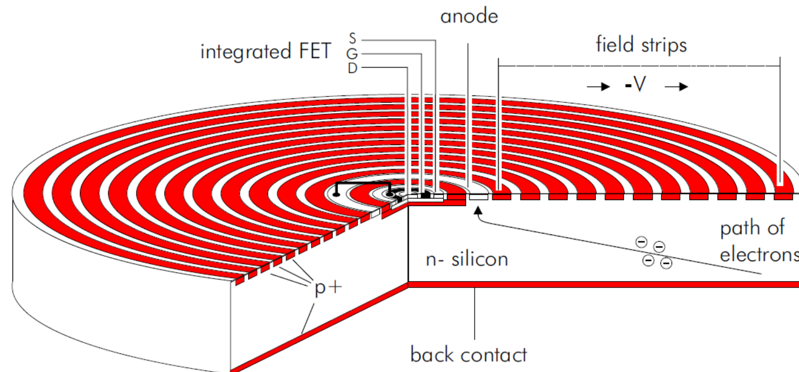


Figure 1.9: Schematic diagram of a conventional SDD. The silicon is completely depleted and therefore sensitive to incoming photons. In the center of the SDD, the integrated JFET can be seen [28].

The main advantages of the SDD are high resolution and short shaping time, which are due to the low output capacitance of the detector. Therefore the readout capacitance must be kept as small as possible. The readout capacitance in the SDD consists of the detector's output capacitance, preamplifier's input

capacitance and stray capacitance of the connection between the detector and amplifier [31,32]. Contribution of the SDD to the total readout capacitance is minimized by the small size of the anode. More reduction of the output capacitance is possible by integrating the first transistor of the amplifying electronics on the detector chip, as illustrated in Figure 1.9 [33].

An example of an integrated transistor is a nonconventional n-channel JFET, which is designed to be operated on a fully depleted n-type high resistivity silicon (HRS) wafer [31,34].

The integrated transistor is designed inside the ring shaped anode. A narrow metal strip connects the anode to the floating FET gate. When electrons are being collected in the anode, the anode voltage changes this can be easily measured as a modulation of the transistor current [23]. The transistor region is separated from the collecting region by a circular deep p-implantation which is biased through a guard ring. The transistor works in a source-follower configuration with an external current supply connected to the source [1,23]. In this structure the on-chip FET has an internal, self-adapting discharging mechanism; therefore there is no need for an externally clocked reset pulse. The integration of the first FET not only minimizes the total capacitance but also reduces noise which is induced by mechanical vibration [35].

Here is one example of a fabricated SDD which works at room temperature. The energy resolution at the MnKa line (5.898keV) is 176eV FWHM at room temperature and 142eV FWHM at -10°C, measured with a 0.5μs shaping time. Moreover, the SDD is the fastest X-ray spectroscopy detector when compared with conventional systems such as Si(Li), Ge and PIN diode [36].

Table 1.2 compares the SDD and Si(Li) as radiation detectors [37].

Table 1.2: Comparison of the SDD and Si(Li) detectors.

Feature SDD S(Li)	SDD	Si(Li)
Resolution	Excellent (>123eV)	Very good (>128eV)
Peak/Bgnd	Very good (7 – 15k)	Excellent (12 – 25k)
High energy efficiency	Moderate (75% at 13.5keV)	Very good (75% at 30keV)
Count rate capability	Excellent (>several hundred kcps)	Moderate (almost 100 kcps)
Light element detection	Very good (Beryllium/Boron)	Excellent (<Beryllium)
Ease of use compact	Compact, electrically cooled	LN cooled

1.3.2 SDD Droplet (SD^3)

In the Silicon Drift Detector Droplet (SD^3), the anode and integrated transistor are moved to the margin of the structure where they can be shielded from direct radiation by a proper collimator as shown in Figure 1.10 (left). In direct radiation

of the readout structure (circular SDD) signal of the electrons are partially lost to the integrated JFET [23]. This has a significant effect on the low energy background in the SDD. Therefore with the SD^3 the peak/background ratio is increased from 3000 to 5000.
Since in the SD^3 the electrons reach the anode from a given direction instead of from all directions, the anode can be designed in different shapes and sizes thereby reducing the total capacitance from 200fF to 120fF. The result is an improvement in energy resolution from 147eV to 128eV FWHM at 5.9 keV, -10°C. Figure 1.10 (right) shows comparison of ^{55}Fe spectra recorded with two SDDs, conventional circular SDD and SD^3. In the spectrum the Mn Kα (5895 eV) and Mn Kβ (6492 eV) lines can be seen [1,23].

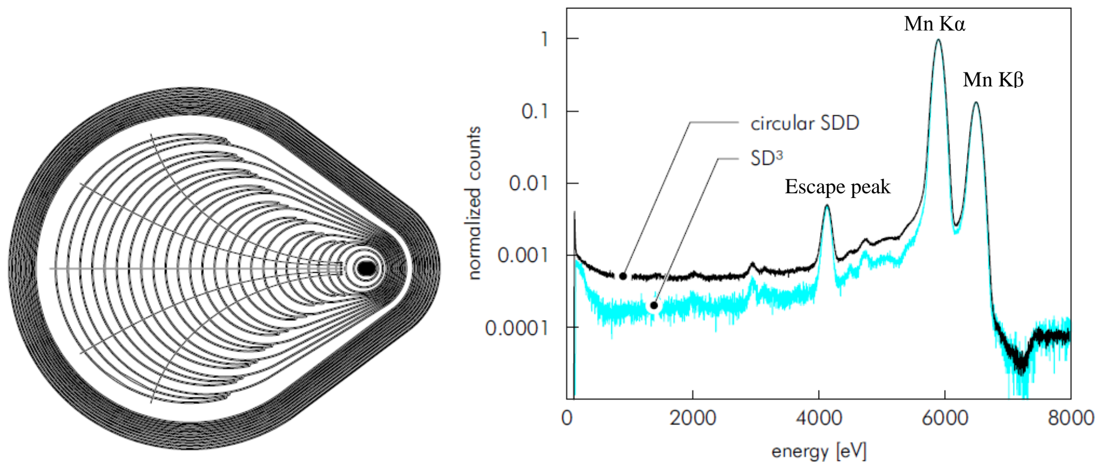


Figure 1.10: Silicon drift detector droplet (SD^3); readout structure is out of the active area resulting a higher peak to the background in the SD^3 [23].

1.3.3 Multichannel SDDs

The multichannel SDD is a radiation detector with a given shape and a large sensitive area, up to a few cm^2, that does not lose the energy resolution or count rate capability of the single SDD. Figure 1.11 shows some examples of multichannel SDDs. They consist of several SDDs with individual readout, but with a common voltage supply, entrance window, and guard ring structure [1,23,38].

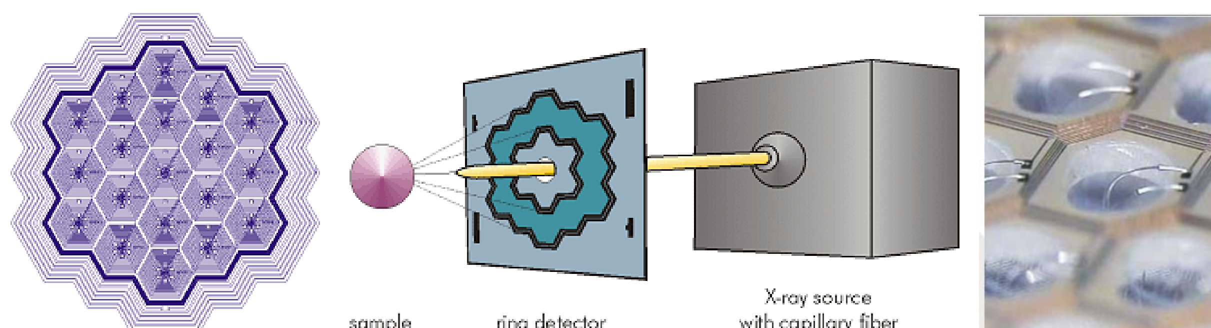


Figure 1.11: Typical multichannel SDD (left); one of the applications of a multichannel SDD in a highly intensive microbeam XRF system (middle) and detailed image of a 5cm^2 detector for gamma ray imaging (right) [39].

Typical parameters for multichannel SDDs are shown in Table 1.3.

Table 1.3: Typical parameters for a Multichannel SDD [39].

Active area	40mm^2 - 5cm^2
Sensitivity	>90% from 200eV to 15KeV
Maximum count rate	Up to 10^7 cps
Energy resolution	128eV – 145eV FWHM @ MnK_a at -20°C
Peak to background	2000 – 10000 @ MnK at -20°C

1.3.4 3D Detector

3D detectors were proposed by S.I. Parker and C.J. Kenney in 1994 [40]. In planar detectors, electrodes are fabricated on wafer surface by implantation while in 3D detectors a three-dimensional array of electrodes penetrate into the detector bulk and are filled with doped material [41]. In this type of the detector p^- and n^- columnar electrodes with the typical 300μm height and 10μm diameter have been fabricated in alternative rows with 50μm distance as shown in Figure 1.12.

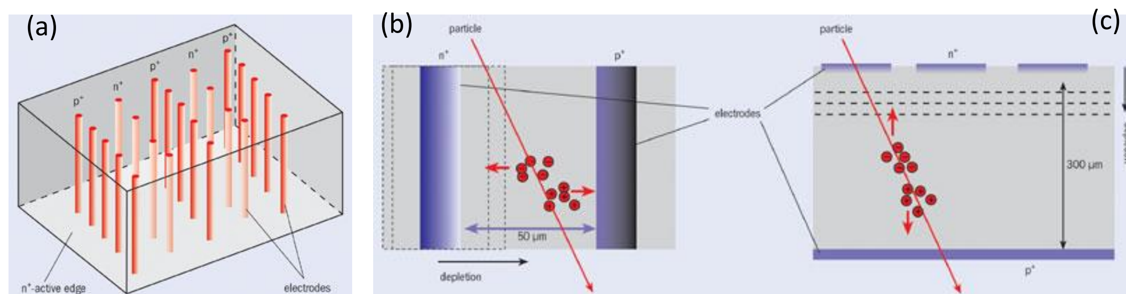


Figure 1.12: Schematic of 3D detectors where the electrodes and the active edges are fabricated inside the detector bulk and filled by n- and p-doped materials (a); 3D detector (b) compared with a standard planar detector (c) [42].

In the 3D detector, collection distances and times are about one order of magnitude less than planar strip and pixel detectors and the depletion voltage is about two orders of magnitude lower. With this specific geometry 3D detectors have a high electric field, fast charge collection and high radiation tolerance. Another advantage of the 3D detector over a planar one is its use of active edges which reduce the dead region from 500μm to less than 10μm. The main disadvantage of 3D detectors is that they require a more complex fabrication process [40,41,43,44,45].

1.4 Outline of the Thesis

This thesis focuses on the integration of the PureB layers in silicon drift detectors for use in SEM systems. In this thesis, novel PureB-SDDs are developed to create a thin-entrance window, low leakage current and uniform electric field with a continuous rectifying junction on the both sides of the SDD. Moreover, a PureB-JFET is developed for the integration of front-end electronics as an amplifier for silicon drift detectors. These are treated in the following chapters as follows:

In Chapter 2 PureB technology and its different aspects which make it suitable for detector are introduced. In particular reactively sputtered ZrN is studied as a diffusion barrier between the PureB and pure Al. The nm-thin ZrN enhances the quality of the detectors without any influence on the electrical parameters of the devices and is compatible with detector fabrication flowcharts. Moreover, high-Ohmic PureB resistors with low TCR and linear behavior are developed to be used in the SDD as a voltage divider.

In Chapter 3 the working principle of a SDD is reviewed and a general guideline for designing the SDDs based on the literatures is reported. The PureB-SDD designs are presented. Several novel SDDs are studied such as a continuous SDD using a boron layer as a voltage divider and a SDD with a dual Boron layer. The SDDs with continuous rectifying junctions on the both sides have low leakage current. The dual Boron layer-SDD with a special design and fabrication, which is also a continuous SDD, has a uniform electric field in the drift region.

In Chapter 4 different aspects of the integrated on-chip amplifier such as noise, transistor selection and designing the JFET and reset mechanisms are discussed. On-chip front end electronics are chosen from the literatures and adapted with the PureB technology. Furthermore, PureB-multi guard ring structures for the SDD are designed and studied.

In Chapter 5 the fabrication process flows for PureB-SDDs are summarized. Then the results of electrical characterization of fabricated SDDs are presented namely characterizing wafer quality, characterizing integrated high-Ohmic resistors in SDDs, influence of different design and process options on leakage current and characterizing an on-chip JFET. Moreover, a novel silicon interposer is designed which enables measurement of double sided contact pads in a conventional probe station.

Finally, Chapter 6 provides the main conclusions of this research and gives recommendations for future work.

Chapter 2

Pure Boron Layer Properties and Applications

2.1 Introduction

A pure boron (PureB) layer is a CVD layer with nanometer thickness which creates a shallow junction p^+-n diode suitable for low-energy electron and X-ray detectors. Nanometer boron layer thickness enables higher detecting responsivity for lower electron or X-ray energies. However, higher sheet resistance of the deposited PureB layer increases the series resistance of the detector. Therefore a mesh or net of µm-thin metallic layer such as Al is required to lower the series resistance while keeping the exposed boron area as much as possible free of Al to detect the incoming radiation with a higher fill factor. The second important parameter in the detectors is capacitance of the diodes which is reflected in the response time of the detector. Lower capacitance is better for fast readout. The Junction capacitance of a diode is a function of the substrate doping, hence to obtain lower capacitance, a high Ohmic wafer is required. In low energy electron detectors, however, a high Ohmic substrate will increase the series resistance of the detectors. One solution is thinning down the wafer to achieve lower resistances, although this requires complex processing and may cause breaking thin, brittle dies. Another way of keeping low RC is to use a 40µm-thic lightly-doped epitaxial silicon grown on a low Ohmic substrate. In this case lower resistance and lower capacitance can be obtained simultaneously. Incoming low energy electrons will be detected in the depletion region in the epi layer of the p-n diode [46]. In X-ray silicon detectors the full thickness of silicon is depleted and used to detect the radiation, thus a high resistivity silicon substrate is used. The boron layer can act as a shallow junction for the entrance window and in the drift side can act as a resistor to divide the electric field between the drift rings with lower surface leakage current.

Many different aspects of boron layers have been extensively discussed and documented in several PhD theses during the last few years. Here are some important achievements which are demonstrated in different PhD theses.

1. Deposition of a shallow junction boron layers, nm-thin p^+ doping, at the interface with the silicon substrate.
2. Suppression of minority carrier injection from the substrate in PureB junction diodes.
3. Selective deposition on clean Si so that the photosensitive junction area can be patterned by thermal oxide.
4. Ability to vary the sheet resistance from a few Ωcm to 10^5 Ωcm.
5. Uniform deposition of a nm-thin boron layer over a large area.
6. Stability in the vacuum environment with electron radiation.
7. PureB as a diffusion barrier layer between Si and Al.
8. ZrN as a diffusion barrier layer for PureB detectors (this thesis).
9. Demonstration of double PureB layer deposition (this thesis).
10. Two distinguished boron layers either on one or on both sides of the device with different controlled properties (this thesis).
11. Landing on PureB on both sides of the detector using a wet etching solution (this thesis).
12. High-ohmic resistors (this thesis).
13. On-chip amplifier (JFET) using a boron layer for the SDD (this thesis).
14. Development of SDD using PureB layers (this thesis).

For an in-depth study regarding properties 1-4 and 5-7 the reader is kindly referred to the PhD theses of F. Sarubbi and A. Sakic, respectively [46,47]. The objective of this thesis is to continue research on items 7 and develop items 8-14.

2.2 Pure Boron Layer with CVD Deposition

Boron layers are deposited on a silicon surface in an ASM Epsilon One reactor by chemical vapor deposition (CVD) with various conditions for Diborane (B_2H_6) and Hydrogen as a dopant gas and carrier gas, respectively. Deposition is performed at either atmospheric or reduced pressure with temperature ranging from 500°C to 700°C. The thickness and quality of the layer can be controlled by

changing the deposition conditions such as gas flow rate, pressure, temperature and deposition time. The standard PureB, which is used as an entrance window in the radiation detectors, is deposited at 700°C with a 490 SCCM flow rate of B_2H_6 at atmospheric pressure (760 Torr) for a 7min deposition time resulting in a 2-3nm thick layer (deposition rate is equal to 0.4nm/min) [47]. The obtained doping in c-Si is 2×10^{19} cm^{-3} and diffuses only nanometers away from the surface [46]. It is proven from TEM investigations that the PureB layer is a layer stack of amorphous boron (α-B) and a boron-silicon compound (B_xSi_y) as shown in Figure 2.1a [48]. SIMS analysis shows doping of underling crystalline silicon (c-Si) to depths below 10nm up to the solid solubility of boron by thermal diffusion (Figure 2.1b) [48]. By reducing the deposition temperature to 500°C as can be seen in Figure 2.1c, the boron layer is not a uniform layer and has high roughness [49].

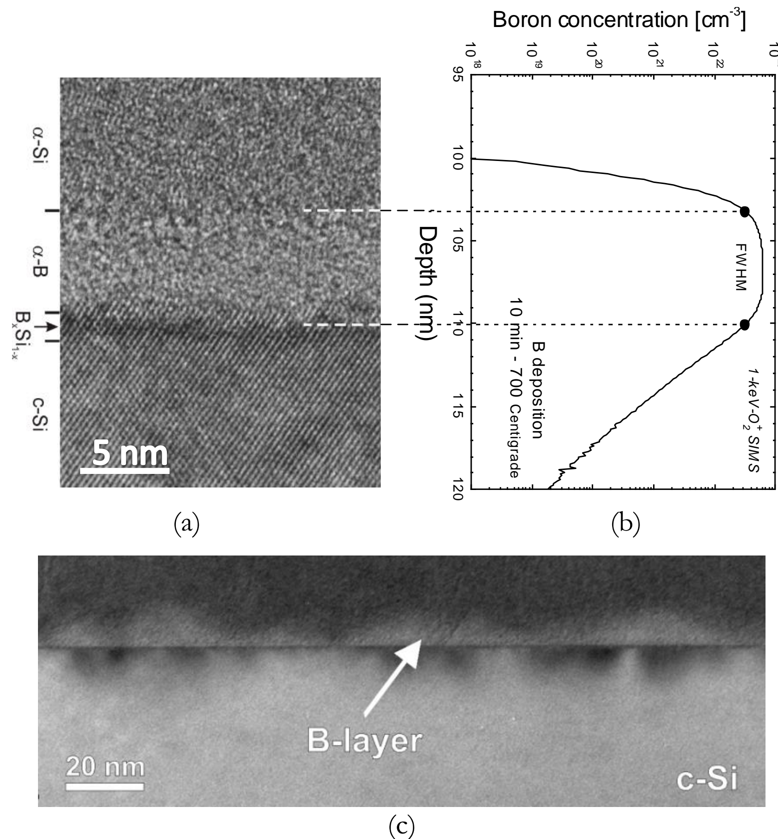


Figure 2.1: a) HRTEM of the PureB layer deposited at 700°C for 10min on a <100> silicon substrate; (b) SIMS profile of the corresponding sample; (c) Boron layer formed after a 10min exposure to B_2H_6 at 500°C [48,49].

2.3 Pure Boron Diodes

Boron atoms are not absorbed as a distinct layer on SiO_2. A patterned SiO_2 layer is used as a hard mask for selective B-deposition, and it is important to provide an oxide-free Si substrate for the boron layer deposition. This is achieved by HF (0.55%) dip-etching, Marangoni drying and an in-situ thermal baking step at 800°C in H_2 ambient beforehand to ensure removal of native oxide residues from the surface of the target area before the PureB deposition. Figure 2.2 shows a schematic of the p-n diode using the boron layer as the p^+ layer.

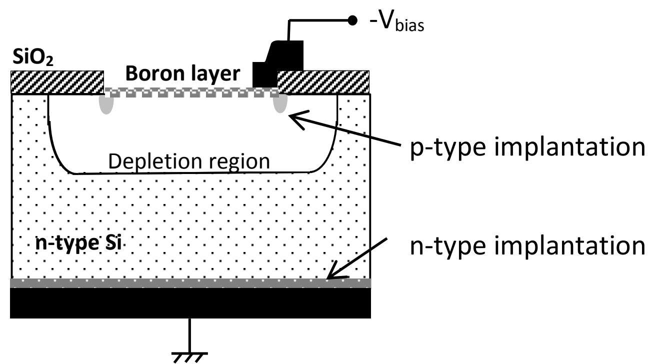


Figure 2.2: Schematic of p^+-n diode using boron layer.

The forward bias characteristics of fabricated p-n junction diodes with different PureB layer thicknesses deposited at 500°C and 700°C are plotted in Figure 2.3 and compared with a Schottky diode.

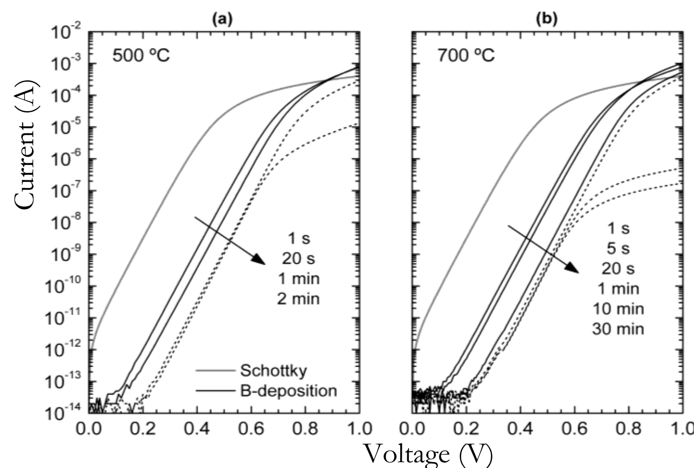


Figure 2.3: IV curve of a pn-diode in forward bias with different boron thicknesses and deposition temperatures of 500°C and 700°C [49,50].

PureB diodes behave like a conventional deep p^+-n junction with near ideal ideality factors lower than ≈ 1.02, and low saturation current. It can be observed that the series resistance of diodes becomes dominant when using a thicker boron layer. Moreover, PureB deposited in 500°C gives a similar IV curve as the 700°C one [49,50].

Another advantage of using a boron layer is the very low leakage current of diodes in the reverse bias region. The amorphous boron layer prevents minority carrier current (holes in the n-type) from flowing from the n-region to the p-type region, showing suppressing minority carrier current. Figure 2.4 shows the leakage current of a typical boron layer made diode and compares it with a commercial product [47].

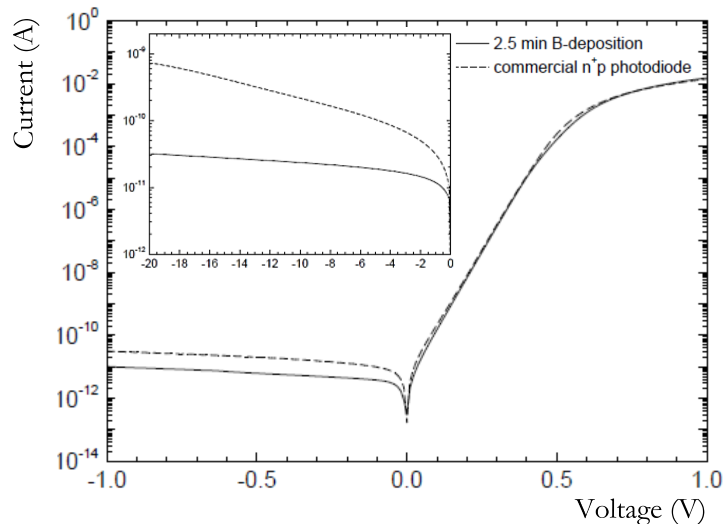


Figure 2.4: Forward and reverse I-V characteristics of a 2.5min as-deposited B-diode compared to a state-of-the-art n^+p photodiode. The active area is 10.75 mm² [47].

2.4 High-Ohmic Pure Boron Resistors

In silicon integrated circuits, resistors are often implemented as implanted p-type regions that are junction isolated by reverse biasing to the n-well in which they are embedded. The sheet resistance of the p-region together with the device dimensions and series resistance of the contacts determine the value of the resistor. This gives a straightforward, flexible way of integrating resistors since already available process steps can be used [51,52]. However, the use of a p-n

junction as isolation has two drawbacks. For one thing, the depletion over the p-n junction is bias dependent and the resistance value will increase with increasing reverse biasing. The p-n junction depletion also constitutes a parasitic capacitance. For resistors in the mega-ohm range, 100 kΩ/□ sheet resistance values are needed to keep the resistors compact enough to have low parasitic capacitance values [53]. To alleviate the junction depletion effects, one solution has been to use polysilicon resistors on oxide isolation [54]. However, these must preferably be heavily doped to assure sufficient dopant activation for good repeatability and reliability of the resistor values. For both lightly doped poly-resistors and diffused c-Si resistors, charging/discharging of the defect states, in the latter case mainly oxide interface states, leads to variable resistance values.

In this thesis, for the first time, we introduce PureB resistors. The pure boron layer can be used as a new material for integrating resistors. They prove to have excellent performance also for sheet resistance values in the 100kΩ/□ range. Sheet resistance of PureB is dependent on the deposition time and temperature. Figure 2.5 illustrates the reduction of sheet resistance of PureB layers with either an increasing deposition temperature or time consistent with a diffusion rate of the boron layer into the silicon. The maximum boron concentration is limited by the solid solubility [47].

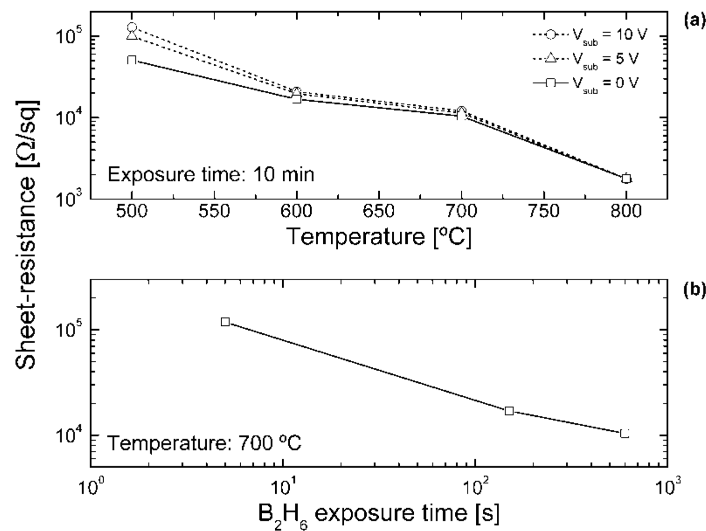


Figure 2.5: Sheet resistance measurement of PureB layers deposited on Si as a function of (a) temperature and substrate biasing, and (b) deposition time. The p-substrate doping is about 10^{15} cm^{-3} [49,47].

For many analog integrated circuits it is vital to have reliable operation over a wide range of temperatures. Having a temperature-stable resistor can therefore be crucial [51]. The important qualification parameters in this respect are the resistor tolerance, i.e., the deviation from the nominal value at 25°C, expressed as the change with applied voltage VCR (voltage coefficient of the resistor) and with temperature TCR (temperature coefficient of the resistor) [55]. Several circuit techniques have been proposed to minimize the TCR by using combinations of negative and positive TCR resistors. For example, resistors made in c-Si generally have a positive TCR while poly-resistors show negative TCR behavior [51]. However, such compensation techniques are often tedious low-yield solutions due to process variations in both materials. In contrast, the PureB technology is shown here to offer a reliable solution for fabricating low TCR, IC-compatible resistors that also can be realized with well controlled high-Ohmic sheet resistances.

The resistors studied here are specifically being developed for use in circuits containing PureB photodiode detectors where the bare PureB layer is used as the entrance window for the light to be detected. To achieve a low capacitance, the photodiodes are fabricated on high-resistivity Si (HRS) <100> wafers and are n-type, phosphorous-doped to 2-10 kΩ-cm. The resistors are also placed directly in the HRS so that the associated depletion layers are tens of microns wide even at 0 V biasing. Thus the voltage dependence of the resistance value is negligible.

The basic PureB-resistor fabrication process is illustrated in Figure 2.6. First a dry oxidation at 1050°C was used to grow a 200nm thick, gate-quality thermal silicon dioxide. The p-type contact regions were then defined by boron implantation and annealed at 1000°C for 35min. The region for PureB deposition was defined by patterning and etching the oxide to the Si. After cleaning, the wafers were dipped in diluted 0.55% HF for 4min followed by Marangoni drying. Thus the Si surface was hydrogen passivated to prevent native oxide formation. As an extra precaution, in the epi-reactor a prebaking step at 800°C in a H_2 atmosphere was also performed. The PureB layer was then deposited at either 700°C or 500°C. The thickness of the resulting layer was measured on the mm-large photodiode surfaces by Ellipsometry. It varied from 2.3nm to 3.5nm, depending on the exact

geometry. This is due to a loading effect that means that a thicker layer is deposited in windows surrounded by large areas of oxide. For small windows the large oxide-to-Si ratio promotes the growth of a thicker boron layer [56]. Immediately after this measurement, the wafers were placed in a metal sputtering system to deposit 1000nm pure Al at 350°C. The Al was etched in two steps. First 800nm was plasma-etched and the remaining Al was wet-etched selectively to the PureB in diluted HF. Finally, an alloying step at 400°C for 30min in forming gas was performed to H-passivate the interface and improve the metal contacts to the Si and PureB. After the formation of the PureB layer, any further temperature processing must be limited to either the 700°C or 500°C deposition temperature. Therefore, if the layer is to be introduced in an integration process such as CMOS, it must happen at a late stage but before the metallization. For further processing it is possible to cover the PureB with a protective dielectric layer without changing the sheet resistance.

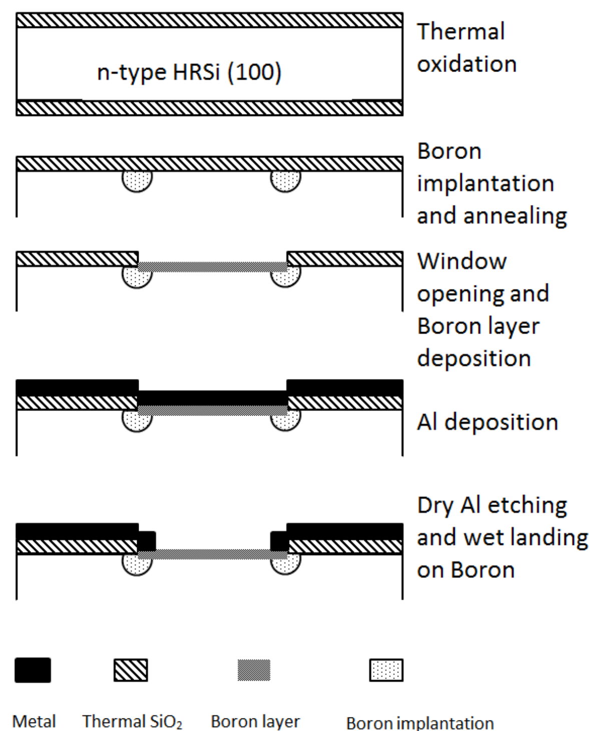


Figure 2.6: Schematic of the basic process flow for the PureB-resistor fabrication.

In Figure 2.7 the ring-shaped test structures with constant perimeter and width but different lengths of the structures (spacing from 5 to 14µm) are shown to measure the sheet resistance of boron layer [57]. With those design considerations

impact of geometrical aspects such as perimeter can be eliminated. Since the contact pads are the same for all test structures, the contact pad resistance can be cancelled using differential electrical measurements. The sheet resistance values extracted from differential electrical measurement of the ring structures are $2.5\times10^4\Omega/\square$ for a 7min 700°C deposition and $3.8\times10^5\Omega/\square$ for a 20min 500°C deposition.

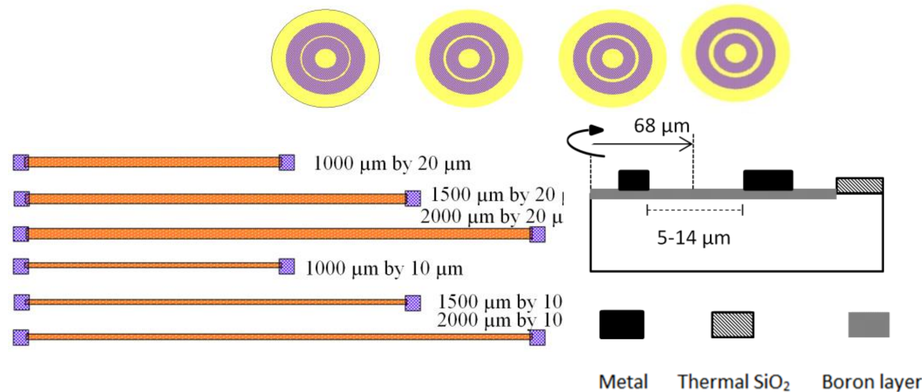


Figure 2.7: Layout and cross-section of ring shaped structures for measuring the PureB layer sheet resistance (top) and some examples of resistor dimensions (bottom).

Figure 2.8 shows the SEM images of the fabricated test structures used to extract the sheet resistance of the PureB layer. As can be seen in this image, the width of the boron layer increases from left to right. The black rings correspond to the boron layer and the white rings are Al pads. With measuring resistance between aluminum rings in this design, it is possible to extract the sheet resistance of the PureB layer [57].

Figure 2.8: SEM images of test structures to calculate the sheet resistance of PureB.

In Figure 2.9 the I-V characteristics are shown for one of the 700°C resistors when sweeping voltage from 10V to 100V reverse bias and varying the temperature from 15°C to 95°C. The resistor has high linearity in this voltage range and the resistance is stable under temperature cycling.

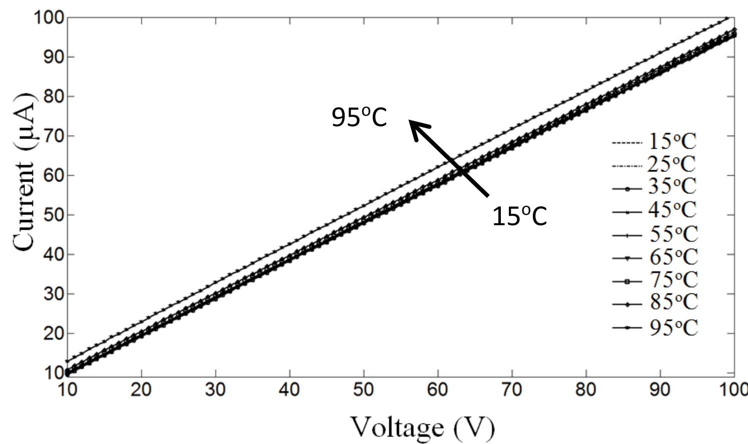


Figure 2.9: I-V characteristics of resistors fabricated at 700°C as a function of measurement temperature.

In Figure 2.10 the resistance is displayed for a 700°C resistor and 500°C resistors with different length/width ratios. The measurement temperature is varied from 15°C to 95°C. In all cases, from 85°C to 95°C the resistor value decreases slightly.

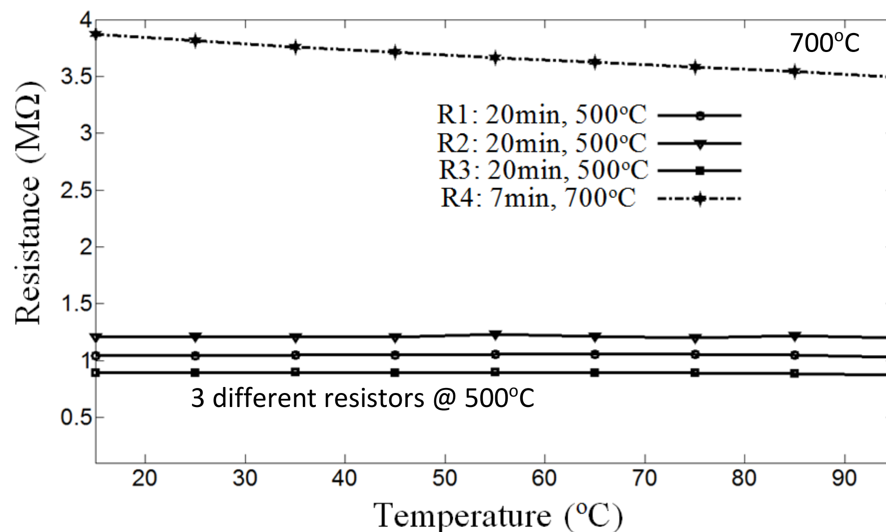


Figure 2.10: Resistance value of several different resistors measured as a function of temperature.

The TCR is calculated as [58]:

$$TCR\left(\frac{ppm}{oC}\right) = (10^6)\frac{R-Ro}{Ro(T-To)} \qquad (2.1)$$

where TCR is the temperature coefficient of the resistor in ppm/°C units, R is the measured resistance at temperature T in °C and Ro is the measured resistance at To in °C.

The absolute value of the calculated TCR is plotted in Figure 2.11 for two of the 500°C and 700°C samples. The 500°C resistors have a TCR of less than 200ppm/°C up until a measurement temperature of 70°C after which it increases to around 1000 ppm/°C at 95°C. The TCR of the 700°C sample has an almost constant value of less than 400 ppm/°C over the whole measurement temperature range.

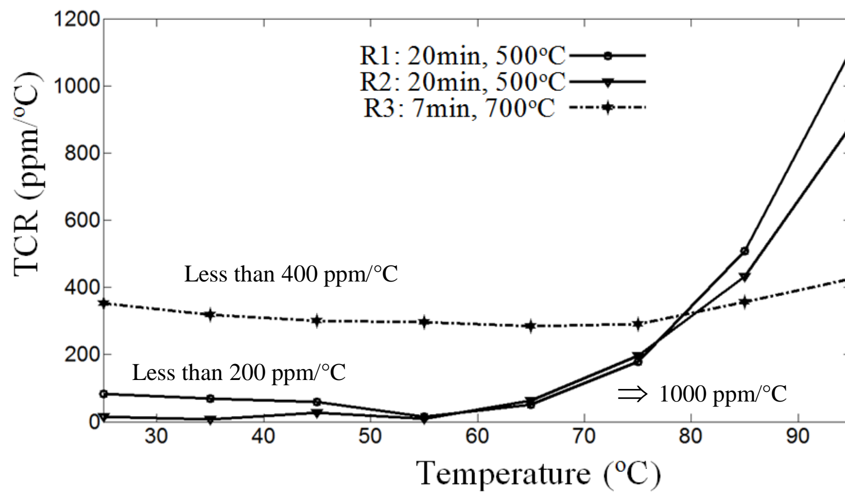


Figure 2.11: Absolute value of calculated TCR as a function of temperature for the resistors made at 700°C and 500°C.

The fabricated resistors have a very good repeatability over 100mm wafers containing 12 dies. This is in accordance with the fact that PureB deposition has been developed to have a very high uniformity over the whole wafer [56]. Moreover, the leakage current is in all cases less than 1nA/cm^2 at a 10V reverse bias which has been demonstrated repeatedly for this process [59,60]. In Table 2.1 a few examples are given of the resistance of the fabricated resistors along with the average values and calculated tolerances over three sampled dies. The tolerance is calculated using the following equation:

$$TR(\%) = \frac{Ri-Rav}{Rav} \times 100 \qquad (2.2)$$

where TR is the resistor tolerance, Rav is the average resistance value, and Ri is any resistor which has a maximum resistance deviation with respect to the average value.

TABLE 2.1: Examples of the tolerance of the fabricated resistors

Boron layer deposition temperature	500°C			700°C			
R(Ω)/Die	R1 (kΩ)	R2 (MΩ)	R3 (MΩ)	R4 (kΩ)	R5 (kΩ)	R6 (kΩ)	R7 (MΩ)
Die 1 (north)	20	1.023	1.45	23	307	872	3.82
Die 5 (center)	21	1.11	1.59	23.1	308	874	3.78
Die 12 (south)	20	1.09	1.49	23	304	875	3.87
Average	20.3	1.07	1.51	23.03	306	873.6	3.82
Tolerance	3.2%	3.3%	5.3%	0.3%	0.7%	0.2%	1.2%

Fabricated high ohmic PureB resistors can be used in several applications such as silicon drift detectors where a voltage divider is used to assign a voltage to the drift rings. In Chapter 5 details of the design will be discussed. Furthermore, this table shows a comparison between resistors fabricated at 500°C and 700°C and their corresponding tolerances. Resistors fabricated at higher temperatures demonstrate lower tolerances in accordance with the TEM images of Figure 2.1. In general with an increasing sheet resistance of the layers the tolerance of fabricated resistors will increase [4].

2.5 Protection, Functional and Diffusion Barrier Layers for PureB Detectors

Depending on the target application of the final device, a barrier, functional or protection layer is required to enhance the performance of the device enabling the fabrication process flow in a way that the final device can be realized in a proper way. In some applications such as silicon drift detectors (SDD) the ability of the detector to detect the lower energies is an important and challenging figure of merit. Conventionally the entrance window in a SDD is often made with ion implantation which limits the detection range of low energy radiation, while the CVD of the PureB layer offers a few nm junction-depth diodes, enabling lower energies detection capabilities. Furthermore, a diode made with PureB has very low leakage current compared to an implanted diode because the PureB layer suppress the minority carriers' current (holes) from the n-region to the boron

layer in reverse bias, resulting in low leakage current (dark current) for the detector [50]. Depending on the application, in the process of PureB detectors after boron layer deposition, some optional layers are directly deposited on top of the PureB. In this chapter, deposition and removal of SiO_2, TiN, ZrN, AlSi(1%) and Pure Al directly on top of the PureB deposited either at 500°C or 700°C, are discussed.

2.5.1 PureB and Ti/TiN Layers as a Diffusion Barrier

The Al layers are been used in the semiconductor industry as a metal layer to contact the pre-defined oxide openings. When Al is in contact with silicon it will try to be incorporated with some Si causing spiking, which dissolve silicon in Al. This will short the shallow junction contacts to the substrate. To avoid the spiking obstacle, Al/Si(1%) is commonly used for metallization. This will solve the spiking phenomena, but it will also introduce a new challenge which is the reverse of the spiking. The Al will sputter its surplus Si, hence accumulation of silicon in the interface of Al and the substrate will occur. Therefore Si precipitations will grow on the Si surface below the Al, resulting in high contact resistance especially for n-doped Si and small contacts [61]. If we use an AlSi (1%) metal layer directly on the boron layer and try to etch it with HF 0.55% solution to expose the boron layer, silicon dots will be left on top of the active region of the detector, as shown in Figure 2.12a. An alternative is to deposit Ti on the boron layer and then AlSi. However, as the optical image of Figure 2.12b shows, silicon dots can still be observed. Silicon dots will create dark spots on the image. A diluted HF solution does not attack the boron layer. To clean the surface one can use polysilicon etchant (HF, HNO_3, CH_3COOH and H_2O) for 30sec to remove the remaining silicon dots. However, this solution may remove the boron layer hence AlSi is not a good option to deposit on top of PureB for metallization.

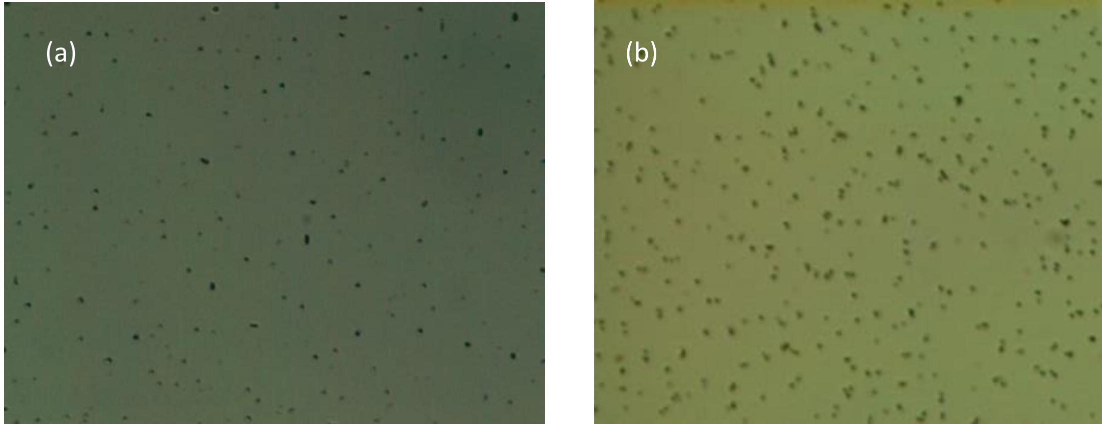


Figure 2.12: Optical image of (a) a wafer with a boron layer deposited at 700°C followed by 100nm AlSi and 875nm pure Al layers and (b) a wafer with a boron layer at 700°C followed by 40nm Ti and 875nm AlSi.

By using a thin layer of Ti/TiN as a diffusion barrier layer between Si and Pure Al, the spiking problem can be solved. However, if Ti/TiN is used as a barrier layer in PureB photodiodes, removing this layer from the top of few nm thin Boron layer in the entrance window is very difficult and is a challenge. Figure 2.13 shows removal of the Ti/TiN layer from the top of few nm thick PureB layer. As it can be seen Al metal layers are over-etched while there is a still Ti layer left on the active area of the detector. Therefore Ti on the boron layer is not a good option for a diffusion barrier layer.

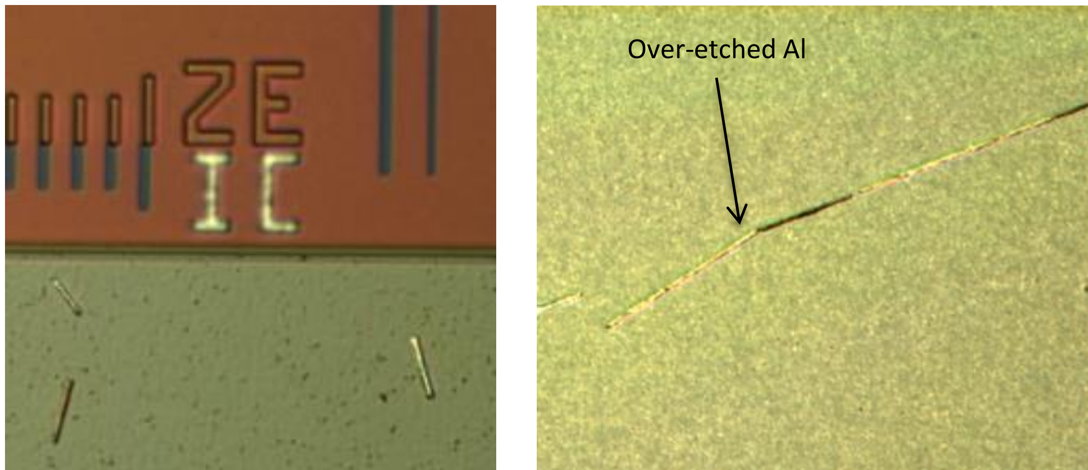


Figure 2.13: Ti layer cannot be selectively etched from the top of the PureB layer.

It has been shown that a thick boron layer can act as a diffusion barrier between silicon and Al [47]. However, the boron layer, which is used as an entrance

window in the radiation detectors, should be as thin as possible to enable detection of low energy radiations by a very shallow junction p-n diode. Figure 2.14a shows SEM images of the silicon surface for a sample which has contact holes with and without boron layer deposition followed by pure Al deposition, 20min alloying at 400°C and selective removal of the aluminum.

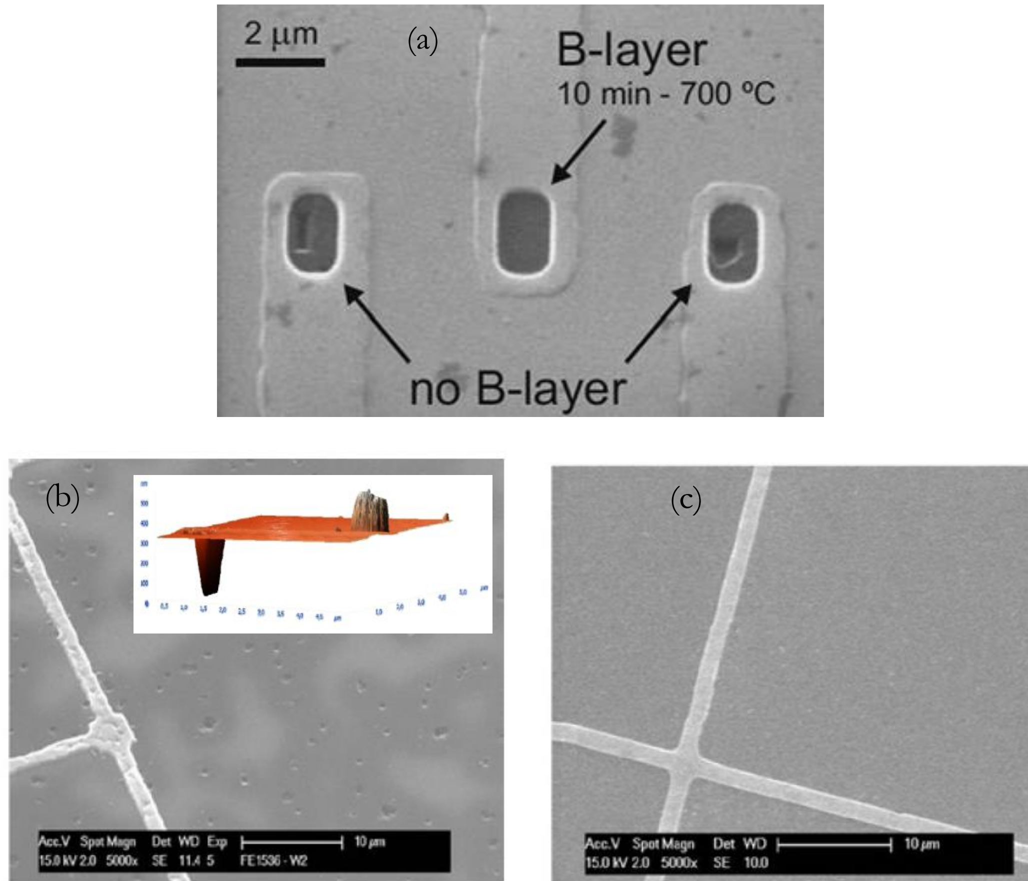


Figure 2.14: Different boron layer thicknesses as a diffusion barrier between Al and Si followed by pure Al deposition, alloying at 400°C, and selective removal of the aluminum: (a) a sample with 10 min boron deposition at 700°C shows a good barrier layer in the regions with the boron layer; (b) 2min 40s boron layer with voids and spikes (boron layer is not enough to act as a barrier); and (c) 6min deposited boron layer has a better barrier [47,62].

It can be observed (from Figure 2.14a) that the thick boron layer can act as a diffusion barrier and prevents spiking problem of Al. The large thickness of the boron layer (~5nm), which is deposited for 10min at 700°C, forms a barrier between Si and Al [47]. Figure 2.14b shows a sample with a 2min 40sec deposition time (~1.8nm average thickness) which shows after Al wet etching, in some points of the silicon surface spiking and precipitates can be seen, which was

confirmed by AFM analysis. Figure 2.14c shows the sample with a 6min boron deposition time (~ 3nm), which is uniform enough to act as a diffusion barrier between Si and Al without any spikes or pinholes [62].

2.5.2 ZrN as a Diffusion Barrier between Boron Layer and Pure Al

It has been mentioned that before boron layer deposition a 0.55% HF dip for 4min is done to ensure the removal of any native oxide layers. However, this cleaning does not remove the possible particles or defects already existing in the epi or silicon layer in the active area of the diodes. Therefore on defective regions, the boron layer will not be deposited. Furthermore, PureB deposition at low temperatures such as 500°C results in a non-uniform layer [47] with some pinholes in PureB. After pure Al deposition it reacts with silicon in the areas where there is no boron layer. Difficulty arises in removing Al from voids inside of the nm-thin PureB surface, while at the same time the above-deposited pure Al layer is preserved, as shown in Figure 2.15. In this SEM image some Al dots or residuals are observed after wet Al etching. These Al dots might create dark spots on the final image of the detector.

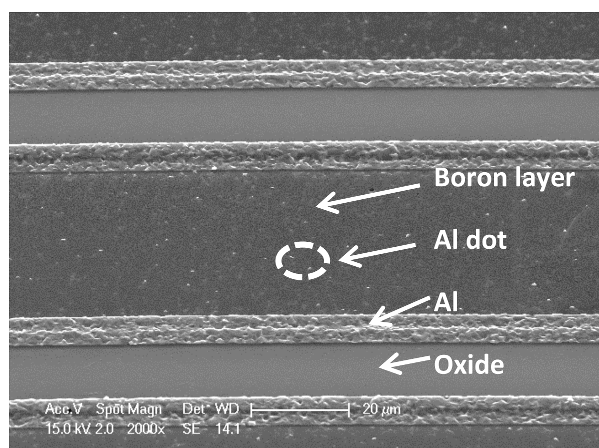


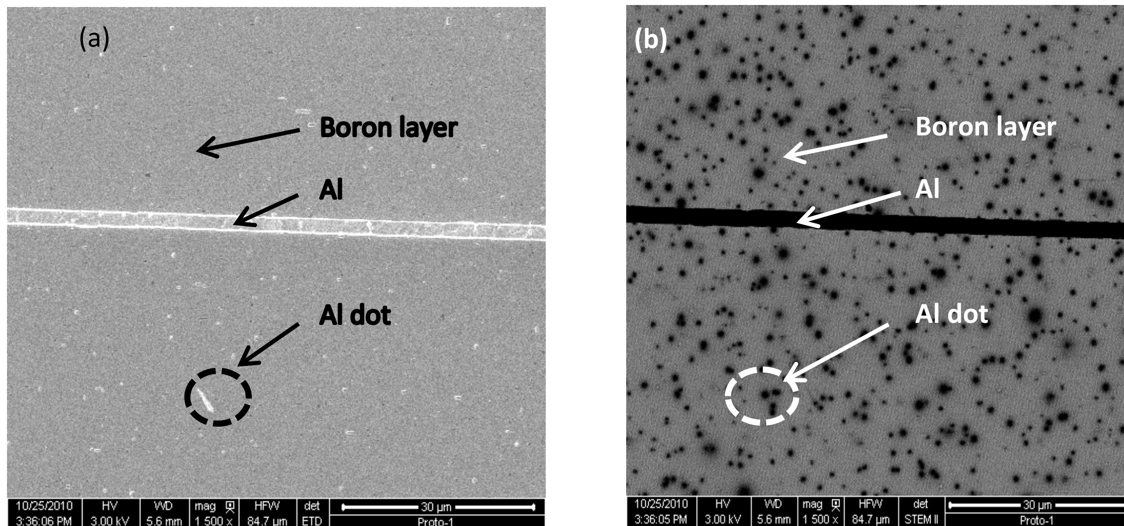
Figure 2.15: Top view SEM image after Al wet-etching from the boron layer deposited at 500°C.

The mentioned results show that the processing of the wafers should be either very clean or plasma cleaning should be done before boron layer deposition to remove any particles or defects from the active region. However, plasma cleaning might damage the surface of silicon resulting into high leakage current for the

detectors. Using a thin barrier layer on top of the boron layer before pure Al deposition might passivate the silicon surface possibly solving the problem. Different barrier layers such as TiN, AlN and ZrN were examined. Using AlN as the barrier layer increases the series resistance of the diodes and might have an impact on the performance of the fabricated detectors. This effect is more pronounced in devices with a very small area. It is mentioned that removing TiN is very difficult from a nm-thick boron layer selectively.

In Figure 2.16(a,b) electron optical inspection in combination with EBIC (Electron Beam Induced Current) imaging displays an unexpectedly high number of pits in the surface of the active area of the detector if Al residuals exist on the surface. Those dark spots lead as dead regions for the detector, which is an undesired effect.

Figure 2.16(c,d) illustrates the entrance window of the detector fabricated using PureB layer followed by few nm thin ZrN layer as a barrier layer. The surface of the detectors was observed in the SEM and EBIC. Images show no dark spot when using a ZrN layer on top of the PureB resulting in a significantly reduced dead region.



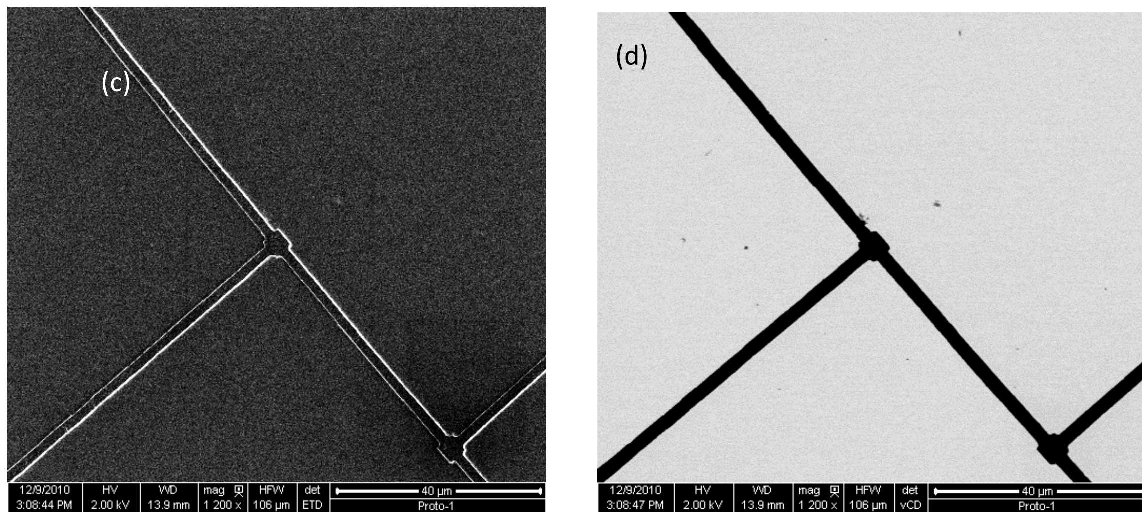


Figure 2.16: SEM and EBIC images of the detector surface, the boron layer was deposited at 700°C and the Si surface was defective before boron deposition: (a,b) samples without a ZrN layer, then high number of unwanted Al dots is seen; (c,d) samples with few nm-thin ZrN layer as the diffusion barrier between the Al and PureB shows no Al dots and no dark spots as the dead layer.

Figure 2.17 shows two SEM images of the detector surface with a boron layer deposited at 700°C and 500°C followed by 10nm ZrN and 875nm pure Al. As can be seen there are no Al dots or any defects on the boron layer.

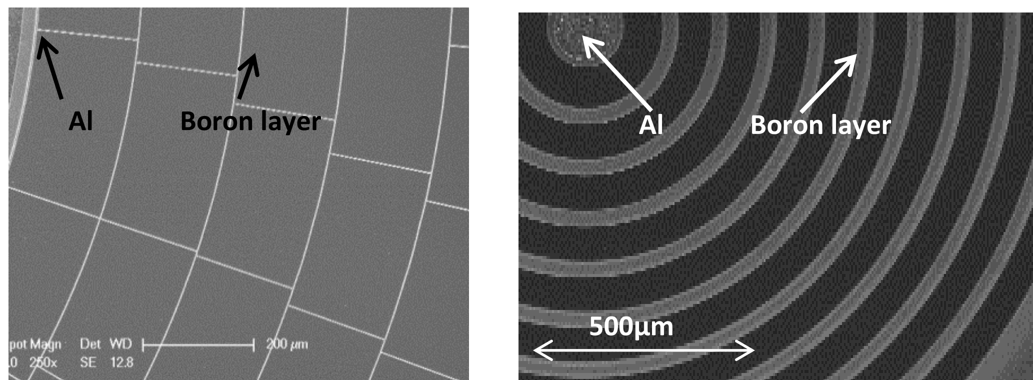


Figure 2.17: Defect-free surface achieved using 10nm ZrN as a barrier layer on top of PureB deposited at 700°C (left) and 500°C (right).

Figure 2.18 is an IV and CV plot of a detector with a large area showing no significant increase in the series resistance when using ZrN as the diffusion barrier between the boron layer and pure Al.

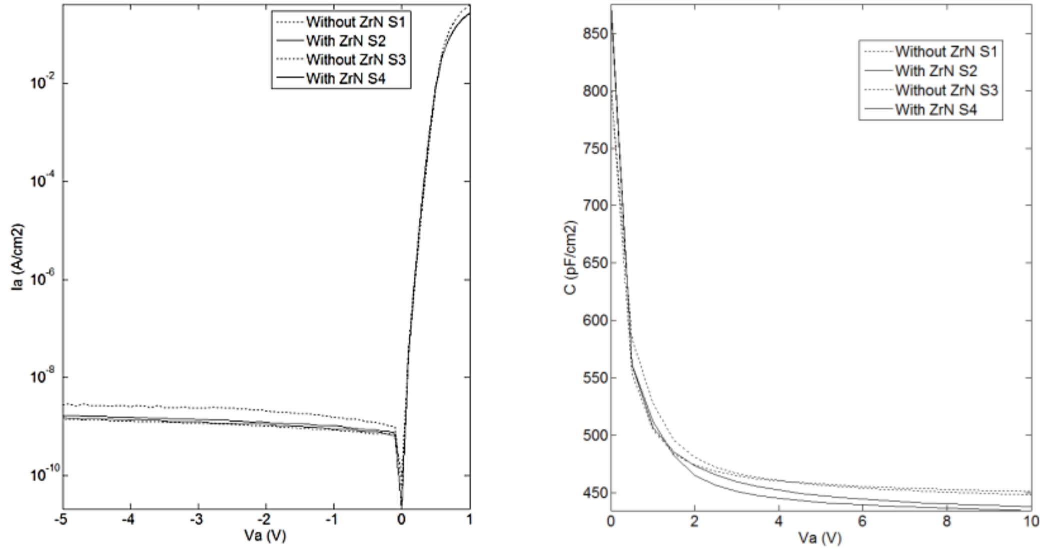


Figure 2.18: Impact of ZrN as the barrier layer on an IV and CV curve of diodes.

Another advantage of using ZrN is the fact that the etch rate of ZrN is lower in comparison with the Al layer in a 0.55% HF solution. Thus any possible Al residuals on the surface can be removed by longer wet etching in a HF solution while the PureB layer is protected by a barrier layer with slower etch rate.

2.5.3 Functional and Protection Layers

In some applications, protection or functional layers are required for optimum efficiency of the photodiodes. Examples of functional layers are PECVD oxide for DUV detectors (where with the optimum thickness of the oxide layer, higher quantum efficiency/responsivity can be obtained), ZrN as a filter for VUV detectors, and SiN as a filter for infrared wavelengths [63]. Other layers such as amorphous silicon, LPCVD oxide and thermal oxide on top of a PureB layer has been examined [64]. Metal layers such as Ti and Zr can be used as protection layer for some applications such as EUV detectors.

The challenging processing step is to deposit and pattern the PECVD oxide on top of the boron layer deposited at lower temperatures. As mentioned before, a boron layer deposited at 500°C has a non-uniform surface, thus if deposition follows the oxide layer, an adhesion problem might result. Different thicknesses of PECVD oxide and TEOS layers were examined to find the best layer. In general, all wafers with deposited PureB at 700°C showed good adhesion without

any problem during oxide patterning and Al deposition. However, wafers with a PureB layer deposited at 500°C had weak adhesion to the PECVD oxide. TEOS deposited wafers had better adhesion than oxide. Figure 2.19 displays wafers with 600nm PECVD TEOS (a) and oxide layers (b,c) on top of PureB deposited at 500°C. The sample with 500°C PureB, as can be observed in the images in (b,c) has a non-uniform boron layer resulting in an oxide layer with high roughness and very poor adhesion to the PureB layer. The oxide layer can be easily peeled off during further processing steps such as a HF dip before Al deposition. The possible cause can be oxide growing under a porous boron layer (deposited at 500°C) during PECVD oxide deposition which will lead to under-etching of oxide and peeling off of the boron and oxide layers when doing a HF dip step before Al deposition. Unlike the 500°C sample, the 700°C PureB sample showed a very uniform oxide layer with good adhesion to the PureB layer.

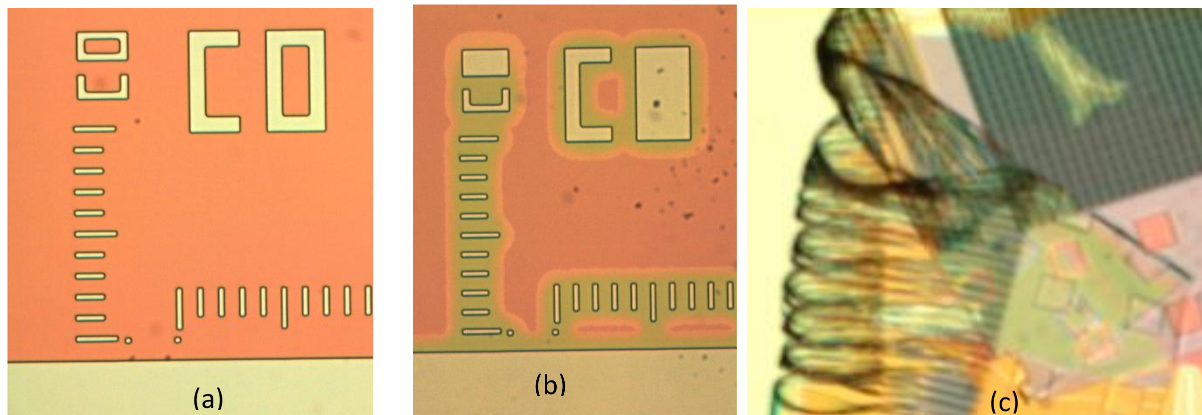


Figure 2.19: Optical images of deposition/patterning of PECVD TEOS (a) and oxide layers (b,c) on 500°C PureB layers. Wafer (a) with TEOS layer had good adhesion while wafer (b) with PECVD oxide had under-etching with delamination of the PECVD oxide and PureB layers during the HF dip step before Al deposition.

2.5.4 Lift-off Process for PureB Diode Fabrication

In order to have a clean surface without Al residuals for the entrance window of the detector, one can use a lift-off process to eliminate any Al contact to the radiation entering area. After PureB layer deposition at 700°C or 500°C, a negative photoresist (AZ®nLOF) was applied and patterned followed by a 400nm thick

Al layer deposition by evaporation. The resist was stripped in an acetone or NMP solution in an ultrasonic bath. For both PureB layers deposited at 700°C or 500°C, the lift-off process was successfully performed as shown in Figure 2.20. There was no adhesion problem nor any Al dots observed on the surface of the detectors. The challenge for this process is limitation of the Al layer thickness maximum to 400nm.

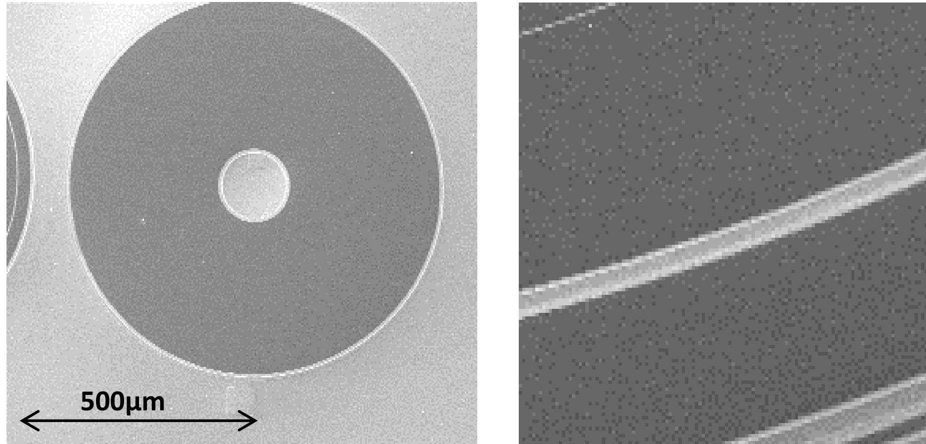


Figure 2.20: SEM image of samples with the lift-off process on 700°C (left) and 500°C (right) PureB layers.

2.6 Lower Leakage Current by Double Boron Layer Deposition

In the next chapter the designed SDDs will be discussed in detail. In some structures of silicon drift detector, combination of two different boron layers is required to obtain different sheet resistances on the different region of the detector. With this unique design the electric field can be made uniform over the drift region of the silicon drift detector. Moreover, photodiodes fabricated with a double boron layer show extremely low leakage current (less than 60 times) compared to conventional PureB photodiodes as reported in Table 2.2.

Table 2.2: Comparison of the dark current of photodiodes when using single or double PureB layers.

Sample (fabricated in the test wafers)	Dark current	Active area (cm^2)	Dark current per unit area (nA/cm^2)	Perimeter of active area (μm)
S1 (B700°C)	~1.7nA	A= 0.58182331	1.7187	P= 42919.4
S2 (B700°C)	3.8nA	A=0.43750989448	8.6855	P=26552.034
SDD(700+5Ann+700)	8.8pA	A=0.30857652955	0.0285	P=26297.591
SDD(700+10Ann+700)	16.4pA	A=0.30857652955	0.0531	P=26297.591

2.7 Conclusions

In this chapter the different aspects of the PureB layer were discussed in detail. Boron layer has many advantages when used in different applications such as detectors and resistors. This layer being a few nm thick creates shallow junction diodes with a very low dark current, allowing it to be suitable for low energy electron and X-ray detectors where the responsivity can be gained significantly. On the other hand the boron layer offers high ohmic resistors with very low TCR and tolerances specifically designed and fabricated for silicon drift detectors. The sheet resistance values extracted from measurement of the ring structures are 2.5×10^4 **Ω/□** for a 7min deposition at 700°C and 3.8×10^5 **Ω/□** for a 20min deposition at 500°C. The fabricated resistors show high linearity in voltage ranges between 10V and 100V and are stable in temperature ranges from 15°C to 95°C. The resistors deposited at 500°C had a TCR (temperature coefficient of the resistor) of less than 200ppm/°C up to a measurement temperature of 70°C after which it increased to around 1000ppm/°C at 95°C. The TCR of the 700°C sample had an almost constant value of less than 400 ppm/°C over the whole measurement temperature range. The calculated tolerance of several resistors made in different ranges by 500°C boron and 700°C boron layer showed less than 1% for the 700°C, and around 3% for the 500°C deposited boron layer. The measured leakage current was less than $1nA/cm^2$ at 10V reverse bias over all dies of the 100mm wafer.

Furthermore, it was shown that 10nm sputtered ZrN can enhance the quality of the detectors without any influence on the electrical parameters of the devices and is compatible with the boron layer process. Optical and SEM inspections showed a defect-free surface of detectors when using 10nm ZrN between the Al and

boron layer for both the 700°C and 500°C deposited layers. As an alternative, a lift-off process was developed to avoid any Al residuals on the boron layer. For both PureB layers deposited at 700°C or 500°C the lift-off process was successfully performed. However, the limitation of the Al thickness and deposition method (evaporation) can be a challenge for some applications.

Moreover, for the low temperature deposited PureB layer it was shown that PECVD TEOS has better adhesion than PECVD oxide to the porous boron layer.

Finally for the first time a double boron layer was introduced and developed where two different sheet resistances of the boron layers are required to achieve a uniform drift field in silicon drift detectors with extremely low leakage current. The detail will be explained in the next chapter.

Chapter 3

Designing Silicon Drift Detectors using PureB layer

3.1 Introduction

In this chapter after the working principle of silicon drift detectors have been reviewed, different aspects of SDDs such as the starting materials, entrance window, full depletion bias, leakage current sources, sink anode, detector size, drift field, spatial spread of the carrier packet, pitch of the drift rings, voltage divider, minimizing output capacitance and guard ring will be explained in details. Then the application in a SDD structure of a boron layer as a voltage divider in the drift area with higher yield and low leakage current in the entrance window for low energy detection will be explained with calculations and simulations. At the end a novel double boron layer as a radial uniform electric field will be introduced.

3.2 Working Principles of PIN and Silicon Drift Detectors

The silicon drift detector (SDD) was proposed by Gatti and Rehak in 1983. SDDs have been developed in many different versions, depending on the application [22,29].

The main advantages of SDDs are a high count rate and better energy resolution with respect to other X-ray detectors thanks to the extremely small anode area and output capacitance. Figure 3.1 illustrates typical SDD structures such as the Multi-Linear Silicon Drift Detector (ML-SDD), Circular SDDs with and without an on-chip amplifier, and Droplet and Multichannel SDDs. All are commercially available and used for different applications.

In order to introduce the working principle of the silicon drift detectors, the simplest semiconductor radiation detector - the PIN photodiode - which is biased in the reverse region, will be discussed. In PIN photodiodes the entire thickness of the silicon wafer is used to detect the X-ray. Figure 3.2a shows the schematic of the planar p-n diode for X-ray detection applications. It consists of a p^+ region where radiation enters the detector (called the entrance window) and an n^+ region for electrical connection. Radiation creates electron-hole pairs (EHPs) in the depletion region where external reverse bias separates the EHPs, and then holes and electrons drift to the p^+ and n^+ regions, respectively.

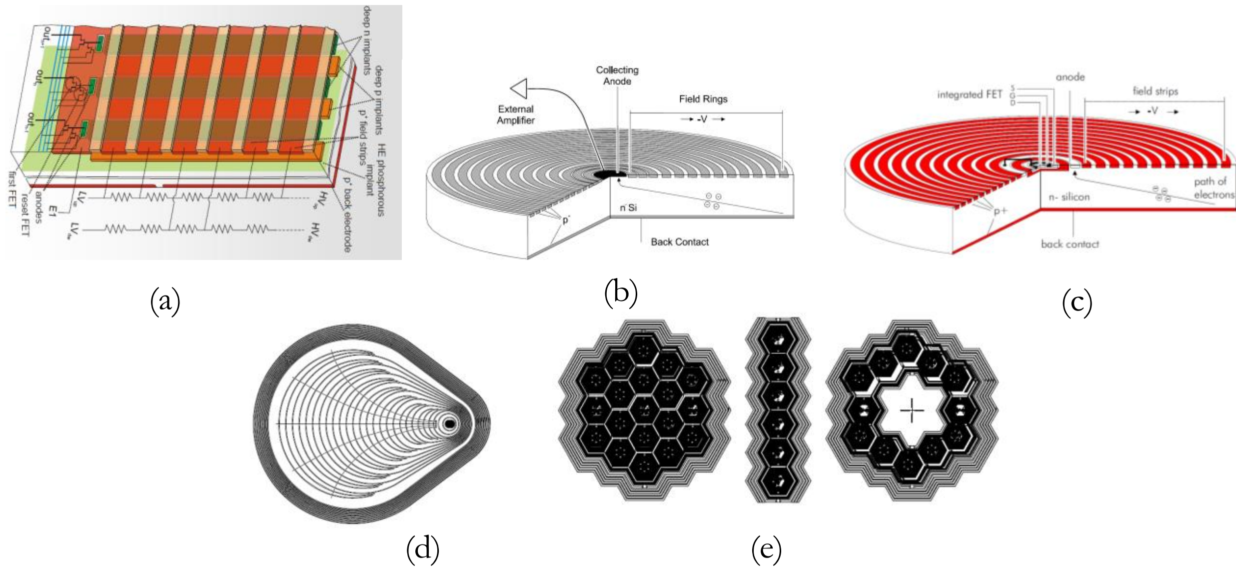


Figure 3.1: Different kinds of silicon drift detectors for different applications: a) ML-SDD; b) Circular SDD; c) Circular SDD with on-chip amplifier; d) Droplet SDD; and e) Multichannel SDDs [Figures from 23,65,66].

Since the entire thickness of the wafer is used for the radiation detection, the device should be fully depleted. The full depletion voltage of a bulk diode can be calculated from the depletion region width:

$$d = \sqrt{\frac{2\epsilon_{si}(V_o - V_r)}{q.N_d}} \cong \sqrt{\frac{2\epsilon_{si}(V_{dep})}{q.N_d}} \quad => \quad V_{dep} = \frac{q.N_d.d^2}{2\epsilon_{si}} = \frac{d^2}{2\epsilon_{si}.\mu_n.\rho} \tag{3.1}$$

where d is the wafer thickness; N_d is the bulk doping concentration; ε_{Si} is the dielectric permittivity of silicon (1.05×10^{-12} F/cm); μ_n is the majority carrier mobility of the bulk; ρ is the bulk resistivity; V_o is the built-in potential of the diode; V_r is the applied voltage; and V_{dep} is the full depletion voltage.

Note that the applied external voltage is much higher than the built-in potential of the diode, thus V_o can be ignored. From this equation it can be seen that the depletion voltage has a linear relation with the doping concentration of bulk silicon and a square relation with the thickness of the wafer. Figure 3.2b illustrates simulation results for the voltage distribution over the wafer for a PIN diode.

Capacitance measurements are typically used to find the full depletion voltage of the detector. The capacitance per unit area is:

$$C(V) = \varepsilon_{si}\frac{1}{d} = \sqrt{\frac{q\varepsilon_{si}N_d}{2V_r}} \Rightarrow \frac{1}{C^2} = \frac{2V_r}{q\varepsilon_{si}N_d} \qquad (3.2)$$

Figure 3.2c shows a plot of the square inverse of the capacitance versus the applied voltage. The capacitance of the detector has a linear relation with the applied voltage up to the full depletion voltage, at which point it will be constant by further increasing the applied voltage.

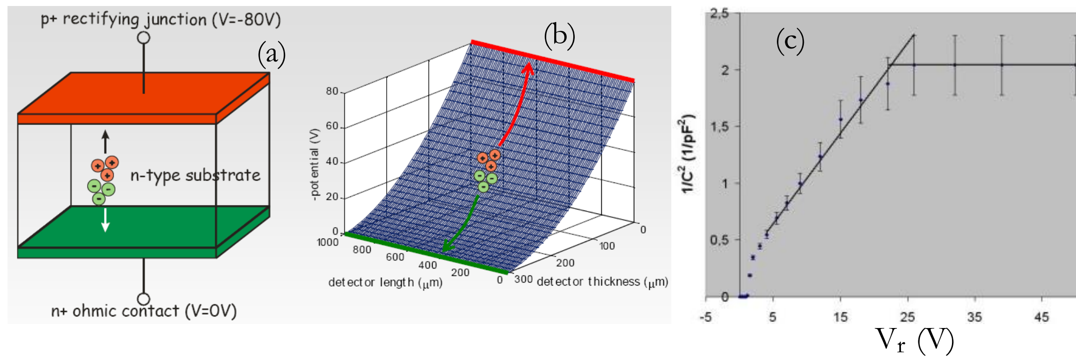


Figure 3.2: a) Schematic of PIN detector and carriers movement in the reverse biased region; b) voltage distribution over the detector thickness; c) corresponding capacitance for the PIN diode [66].

To improve the energy resolution and count rate of an X-ray detector, the capacitance of the detector has to be minimized. For PIN photodiodes,

capacitance is related to the detector size and the thickness of the silicon wafer ($C_{det} = \frac{\varepsilon_{Si} A}{d}$) which will result in very high capacitance for larger detectors.

To maintain minimum capacitance, one can use sideward depletion [29] where the detector capacitance is minimized without changing the size or thickness of the detector. As shown in Figure 3.3 the Ohmic n^+ contact can be small and placed anywhere on the un-depleted bulk. In this configuration on both sides of the wafer, p-n diodes can be made. By applying a small voltage to the n^+ electrode, two separated depletion regions will be created. By increasing the applied voltage these two space charge regions will reach each other and there will be a small un-depleted bulk region around the n^+ electrode. When the detector is fully depleted, the minimum potential distribution for electrons will be in the center of the wafer.

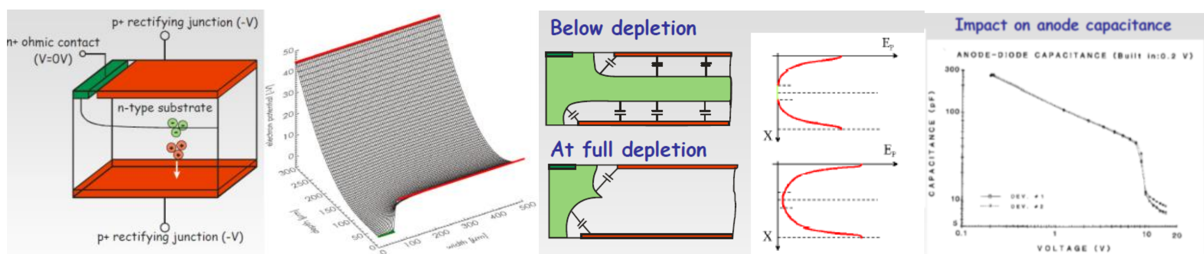


Figure 3.3: Minimizing the anode capacitance by use of the sidewall depletion idea [66].

After X-ray radiation, generated holes inside the depletion region will be drifted to the p+ contacts while electrons inside the potential valley will move toward the anode slowly with the diffusion mechanism. If there is an electric field parallel to the detector surface, electrons will drift faster to reach the n^+ anode contact. This can be done by dividing the p^+ junctions into p^+ strips where their external voltage will gradually be more positive to the anode in order to drift the electrons. Finally electrons will be collected in the anode. A schematic of the multi-anode SDD is shown in Figure 3.4.

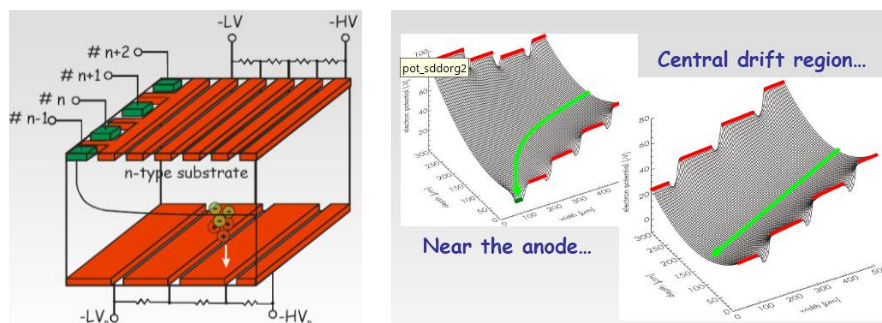


Figure 3.4: Multi-anode SDD and calculated potential distribution [66].

In the ultimate case the anode area can be a small n^+ region such as a point like a junction to collect the generated electrons. With this type of SDD, the anode capacitance is extremely small with values typically between 100fF to 200fF. The depletion region will be created by bias voltages applied to both sides of the detector. In the first generations of the SDD as shown in Figure 3.4, although there were p^+ rings in the entrance window, positive charges were accumulated in the oxide between the drift rings resulting into a pocket-like potential distribution between the rings where generated electrons from radiation could be captured and trapped. Therefore it was the idea to have a continuous shallow junction in the backside of the wafer with continuous p^+ back contact acting as the entrance window. Typically the entrance window is created by shallow implantation which will lead to dead layer of at least 40nm. By optimizing the doping profile it is possible to minimize the charge loss and enhance the quantum efficiency.

3.3 Design Considerations for Silicon Drift Detectors

In this section a general guideline for designing SDDs based on the available literatures will be presented. Then the application of PureB in creating novel SDD structures will be discussed. Design considerations such as pitch and the width of the drift rings, optimizing the anode capacitance, size of the detector, wafer thickness and resistivity, X-ray energy range, noise considerations, sink anode and voltage dividers such as implanted resistors, MOS structures and punch through mechanism will be discussed in detail.

3.3.1 Selection of Starting Material

In X-ray detectors, high-Ohmic silicon wafers are used because they have a better carrier lifetime in the order of milliseconds and a smaller voltage required for full depletion. Wafer quality is very important and has significant impact on the performance of the final device. In silicon drift detectors since it is based on full thickness depletion, any doping variations in the wafer, can distort the drift path and change the position resolution of the detector. Hence a very homogeneous material in terms of doping impurities is required. Among different wafer

preparation methods, for SDD applications usually Neutron Transmutation Doped (NTD) wafers are used where uniformity of the phosphorus doping is achieved by exposing an ingot of high purity silicon to a uniform flux of thermal neutrons. One isotope of silicon absorbs a neutron, and the following β decay converts it into phosphorus which is an n-type material with donor impurities. The resulting uniformity of the donors is superior to that achievable by adding phosphorus during the growing phase of silicon ingots [28].

At higher the X-ray energy, the more the X-ray detection efficiency of the SDDs is limited by wafer thickness. As plotted in Figure 3.5, for specific energy above 10keV thicker wafers offer higher quantum efficiency. For example for typical 300μm thick wafers, quantum efficiency is about 90% at 10keV and 50% at 15keV [1]. Therefore depending on the application, the wafer thickness can be selected. For higher energies a thicker wafer is required.

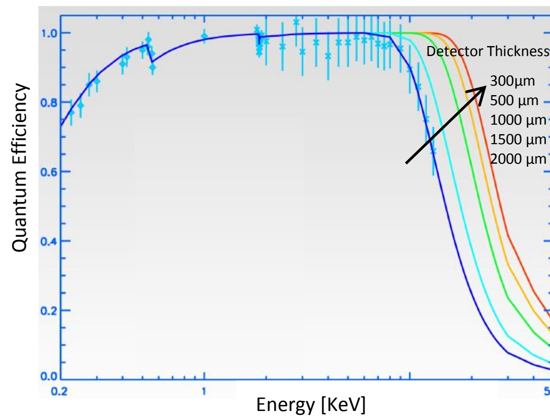


Figure 3.5: Quantum efficiency versus energy for different silicon thicknesses [66].

In the field of X-ray spectrometry, high energy resolution and low energy detection capabilities are basic requirements [67]. For low energy detection, silicon wafer orientation of <100> is preferred to have higher charge collection efficiency (CCE) for soft X-rays (below 200nm wavelengths) as shown in Figure 3.6. CCE can be maximized further by realizing a shallow junction p^+ region. Furthermore wafers with a <100> orientation have lower surface leakage current compared to <111> orientation.

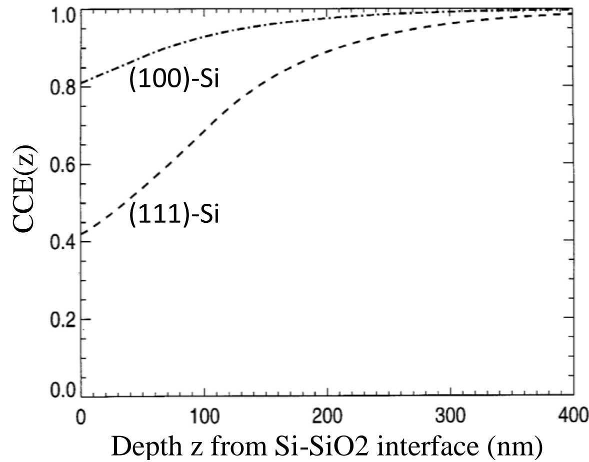


Figure 3.6: Wafer with <100> orientation is preferred for detectors to maximize the charge collection efficiency (CCE) for soft X-rays [68].

3.3.2 Entrance Window

In the low X-ray energy range (100eV–1keV), the detection efficiency is generally limited by the absorption in the window material of the instrument. The window provides a barrier to maintain the vacuum within the detector while being as transparent as possible to low energy X-rays. There are two main types of window materials. Beryllium (Be) is highly robust, but strongly absorbs low energy X-rays meaning that only elements from sodium (atomic number = 11) can be detected. Polymer-based thin windows can be made much thinner than Beryllium windows and therefore are transparent to much lower energy X-rays, many allowing detection of X-rays down to 100eV. In instruments that operate under very high vacuum conditions, for example TEMs, it is possible to use windowless detectors which allow for even more sensitivity to light elements [69].

Another limitation factor for the detection efficiency is the absorption in the dead layer of the detector. In order to reach a good response in the low energy range (a few hundred eVs) a very shallow implantation of the P^+ back contact that acts as a radiation entrance window is needed [1].

In order to improve the quantum efficiency of the detectors for very low energy ranges (a few hundred eVs) special care has to be considered in the design and fabrication steps such as implantation of the entrance window and annealing to

minimize charge loss in the dead layer or non-sensitive area in the p^+ region of the entrance window. Figure 3.7 shows attenuation length versus energies in the silicon, boron, silicon dioxide, Al and ZrN layers [70]. It can be seen that lower energies have a shorter attenuation length. Therefore detecting lower energies with higher quantum efficiency or higher responsivity requires a shallow junction p-n diode. Furthermore, it can be seen that a boron layer of a few nm on silicon will not attenuate the incoming radiation energies. For typical implanted junctions, the obtained minimum junction depth is at least 40nm, which can act as dead layer for lower energies. This means lower radiation energies will create electron holes in the dead layer, not in the depletion layer.

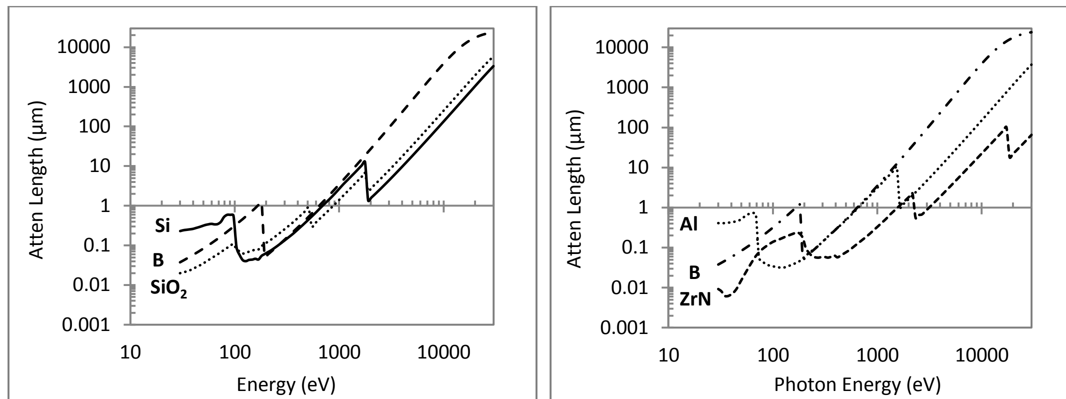


Figure 3.7: Attenuation length versus energy. Lower energies generate electron hole pairs near the surface requiring shallow junction p-n detectors. Attenuation length is simulated using reference [70].

3.3.3 Biasing Potential

In order to prevent any loss of electrons at the surface of the detector, the potential difference between the front (device side) and back side (entrance window) has to be equal to or less than the required depletion voltage. Any increase of this potential would lead to a reach-through condition with a large current flowing between the p^+ regions at both sides [71]. In the front side and center of the detector, which is the anode, the potential is zero. To keep full depletion in the center of detector, the entrance window will be biased at V_{dep} which corresponds to the depletion voltage of the full wafer thickness. In the outer drift ring the applied voltage is equal to $2V_{dep}$ to ensure enough drift potential for the electrons toward the anode. Therefore the maximum applied

voltage is limited to two times the depletion voltage ($V_{bias} \leq 2V_{dep}$) to prevent any reach-through condition that would lead to high current flow.

3.3.4 Leakage Current Components in SDD

The leakage current of a radiation detector is an important parameter that creates white noise in the detector. In a radiation detector there are one or more p-n junctions which have specific leakage currents. Those leakage currents (I_L) generate a parallel white noise current source with a noise power density qI_L. Then contribution of the leakage current to the total ENC (Equivalent Noise Charge) can be derived:

$$ENC_L = \sqrt{A_3(qI_L)\tau} \qquad (3.3)$$

where A_3 is a shape factor and τ is the time parameter of the shaping filter [72,73].

In a p-n junction, leakage current consists of three components as illustrated in Figure 3.8:

bulk generation current I_{bulk}, diffusion leakage current I_{diff} and surface generation current I_{surf}.

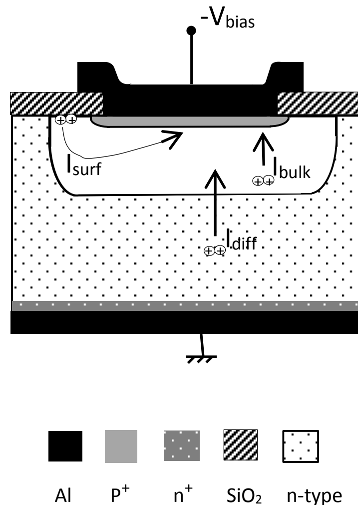


Figure 3.8: Three components of leakage current in a p-n junction.

Bulk Generation Current

In a depletion region of a diode, thermally generated electron-hole pairs form bulk generation current. This current can be written [74]:

$$I_{bulk} = q\frac{n_i}{\tau_g}AW_{depl} \qquad (3.4)$$

where n_i is the intrinsic carrier concentration, τ_g is the generation lifetime of the electron-hole pair, and W_{depl} is the width of the depletion region (W_{depl}= $\sqrt{2\varepsilon_{si}\frac{(V_{bias}+V_{bi})}{qN_D}}$). According to (3.4), a greater depletion width, higher intrinsic carrier concentration and larger diode lead to higher leakage current. For a given $A\times W_{depl}$, the bulk generation current can be controlled by a generation lifetime which is a reflection of wafer quality.

Since n_i (T) and τ_g (T) are temperature dependent, the bulk generation current is strongly related to temperature [12]:

$$I_{bulk}\infty T^2 e^{\frac{-E_g}{2kT}} \qquad (3.5)$$

where E_g is the band gap energy (1.12eV for silicon).

It can be seen that to minimize the bulk contribution to leakage current one can reduce the temperature of the detector (with a Peltier cooler) and select high quality wafers to fabricate the detectors.

Diffusion Leakage Current

The diffusion leakage current results from the diffusion of charge carriers from un-depleted regions of the detector to the depleted region. Usually it is well controlled and has less contribution to the total leakage current of the SDD. Diffusion leakage current can be derived from [74,75]:

$$I_{diff} = qn_i^2 A\left(\frac{D_{n^+}}{N_{D^+}d_{n^+}} + \frac{D_{p^+}}{N_A d_{p^+}}\right) \qquad (3.6)$$

where D is the diffusion constant for the minority carriers, N is the doping concentration for the donors and acceptors and d is the depletion region width in the n- and p-regions. The temperature dependence of I_{diff} can be written as [12]:

$$I_{diff} \propto T^3 e^{\frac{-E_g}{kT}} \quad (3.7)$$

Therefore both bulk and diffusion leakage currents can be minimized by cooling the detector.

Surface Generation Current

The last component of leakage current is surface generation current. The main sources of surface generation current are surface defects generated during processing (such as scratches or any contamination on the surface) and energy levels or interface states generated in the bandgap region near the surface by abrupt discontinuity in the silicon interface. The surface generation current can be written as [74,75]:

$$I_{surf} = qn_i s_g A_s \quad (3.8)$$

where s_g is the surface generation velocity and A_s is the area.
Surface generation current can be the dominant contributor in the total leakage current. There are some design and fabrication considerations when reducing the surface leakage current. For example in the fabrication of the detectors, dry thermally grown SiO_2 is preferred to passivate the silicon surface. Moreover, wafers with <100> orientation have fewer interface states in comparison to <111> oriented wafers. There are several other design tricks to reduce the surface leakage current which will be discussed below.

The temperature dependence of I_{surf} can be derived as [12]:

$$I_{surf} \propto T^2 e^{\frac{-E_g}{2kT}} \quad (3.9)$$

Cooling the detector will decrease the surface leakage current similar to other components.

3.3.5 Sink Anode

A sink anode is a structure to reduce the surface leakage current. This structure is used to provide a path to drain away the surface electrons through the p^+ field electrodes. The idea is to extend the Al metal, which is connected to the drift rings, to create overlap with the oxide. This configuration is similar to a MOS transistor which has the gate shorted to the source acting as a diode as illustrated in Figure 3.9. In this structure the MOS gate is connected to the inner neighboring ring which is more positive than the outer ring. Therefore as can be seen from Figure 3.9 we have $V_S > V_D$ thus an electric field will be created under the gate between the rings creating an electron accumulation layer. Using a narrow interrupt between each ring, accumulation layers of all rings will be connected to the clear pad [26,76]. The advantage of this structure is that the detector is less sensitive to radiation damage at the Si-SiO_2 interface as well. However, in this type of detector, some part of the signal charges are lost to the sink anodes [28,76,77,78].

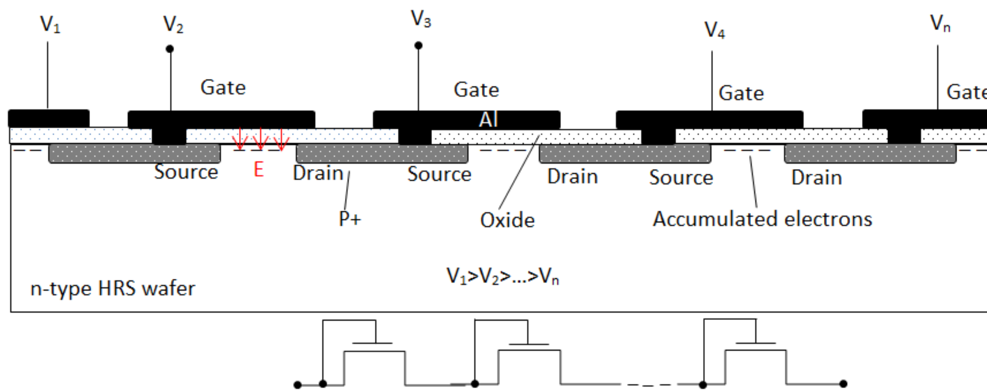


Figure 3.9: Cross-section and equivalent circuit of a sink anode used to collect the surface charges and guide them to clear contact.

3.3.6 Optimizing the Detector Size

The maximum collection efficiency can be achieved by maximizing the detection size [79]. Depending on the application of the detector, the required size can be calculated to meet maximum collection efficiency and drift time requirements in

a specific geometry of the system. The relation between the detector size and given maximum drift time can be calculated as

$$R_{\det} = \sqrt{2V_{dep.}\mu_n.t_{drift}^{\max}} \tag{3.10}$$

We have:

$$v_{drift} = \frac{x_{drift}}{t_{drift}} \quad \text{and} \quad v_{drift} = \mu_n \times E_{drift} \Rightarrow \quad x_{drift} = \mu_n \times E_{drift} \times t_{drift}$$

$$E_{drift} = \frac{V_{bias}}{x_{drift}} \quad \Rightarrow \quad x_{drift}^2 = \mu_n \times V_{bias} \times t_{drift}$$

$$V_{bias} \le 2V_{dep.} \quad \Rightarrow \quad x_{drift}^2 \le 2V_{dep.}\mu_n.t_{drift}$$

$$x_{drift}^{Max.} = \sqrt{2V_{dep.}\mu_n.t_{drift}^{\max}} \quad \Rightarrow \quad R_{\det} = \sqrt{2V_{dep.}\mu_n.t_{drift}^{\max}}$$

where $V_{dep.}$ is the full depletion voltage; μ_n is electron mobility; v_{drift} is the drift velocity; E_{drift} is the drift field; x_{drift} is the drift distance; t_{drift} is the drift time; and $R_{\det}$ is the maximum radius of the detector.

Therefore the maximum radius of the detector has a square root relation with the maximum drift time. A shorter drift time means a smaller detector. Hence in some applications instead of using a big detector, many small segmented detectors can be used to have a shorter drift time and large area for detection.

3.3.7 Optimizing the Drift Field

The minimum required drift field can be calculated from the Gaussian spread of the signal in the time domain (σ_t). The equation for the minimal drift field requirement for the given σ_t reported as $E_{drift}^{\min} = \left[\frac{1}{\left(\mu_n\sigma_t^{\max}\right)^2} 2L\frac{kT}{q}\right]^{1/3}$ in [80]. This equation is calculated here:

$$\sigma_t = \frac{\sigma_x}{v_{drift}} \Rightarrow \sigma_x = v_{drift}.\sigma_t$$

$$\nu_{drift} = \mu_n . E_{drift} \quad \Rightarrow \quad \sigma_x = \mu_n . E_{drift} . \sigma_t$$

$$\left.\begin{array}{l} \sigma_x(t) = \sqrt{2D.t} \quad \Rightarrow \quad \sqrt{2D.t} = \mu_n . E_{drift} . \sigma_t \quad \Rightarrow \quad 2D.t = \mu_n^2 . E_{drift}^2 . \delta_t^2 \\ \nu_{drift} = \dfrac{x_{drift}}{t_{drift}} \quad , \quad \nu_{drift} = \mu_n . E_{drift} \quad \Rightarrow \quad t_{drift} = \dfrac{x_{drift}}{\mu_n . E_{drift}} \end{array}\right\}$$

$$2D.\frac{x_{drift}}{\mu_n . E_{drift}} = \mu_n^2 . E_{drift}^2 . \delta_t^2$$

$$\frac{D}{\mu} = \frac{kT}{q} \quad \Rightarrow \quad \frac{2kT}{q} . \frac{x_{drift}}{E_{drift}} = \mu_n^2 . E_{drift}^2 . \delta_t^2 \quad \Rightarrow \quad E_{drift}^{min} = \left[\frac{1}{\left(\mu_n \sigma_t^{max}\right)^2} 2L \frac{kT}{q} \right]^{1/3} \tag{3.11}$$

where σ_x is the spatial electron cloud spread; σ_t is the Gaussian spread of signal in the time domain; D is the diffusion coefficient or diffusivity (m^2/s) ; and L is the maximal drift distance.

Therefore the minimum required drift field has inverse relation with the time domain spread of the signal.

3.3.8 Spatial Spread in the Packet Width of Carriers

The spatial growth of the signal charge packet (either electrons or holes) as it drifts down the detector is governed by diffusion. At room temperature, the rms of spatial spread in the packet width, σ(x), can be given by [81]:

$$\sigma(x) = \sqrt{2D.t} = \sqrt{\frac{2kT\mu}{q} \frac{x_0}{\mu . E}} \quad \Rightarrow \quad \sigma(x) = 0.228\sqrt{\frac{x_0}{E}} \quad \text{(cm)} \tag{3.12}$$

where x_o is the distance (in cm) of the location of the generated carriers from the collecting anode, and E is the applied vertical electric drift field (in V/cm), which is independent of any material properties. For example for a 520μm silicon wafer, if the generated electrons are in the middle of the wafer under anode, and the applied depletion voltage is 300V, then σ(x) is around 2μm. As can be seen from the equation, $\nu_{drift} = \mu_n . E_{drift}$, the speed of the signal charge packet movement is dependent on the mobility of the carriers, then for a p-type substrate is μ_h/μ_e times slower than a n-type substrate [81].

3.3.9 Pitch of Drift Rings

Drift rings are used to divide the applied potential between outer and inner rings uniformly. To achieve a sufficiently uniform drift field, in the central part of the SDD, the pitch of rectifying strips must be less than half of the wafer thickness [28]. For 520μm wafer thickness, the pitch of the rings has to be less than 260μm.

$$\frac{Pitch\ of\ rectifying\ strips}{wafer\ thickness} < \frac{1}{2} \tag{3.13}$$

3.3.10 Integrated Voltage Divider

In order to drift generated electrons toward the anode, external voltages have to be applied to all drift rings, which will require a lot of wire bonding. Another way is to make integrated voltage dividers in the SDD structure. With this technique only the first ring next to the collecting anode and the last one at the edge of the detector has to be contacted in order to bias all rings. Several methods have been developed to realize the voltage divider in the SDDs:

a) Each p^+ ring is connected to the contiguous one by an implanted layer [28].

b) Each p^+ ring is connected to the neighboring one by a polysilicon layer [81,82].

c) Each p^+ ring is connected to the next one by punch through mechanism where suitable distance and substrate doping define the punch though between two neighboring p-rings [82].

d) Each p^+ ring is connected to the contiguous one by a p-channel MOSFET transistor; in this case a metal gate is connected to the corresponding drain. Applied voltage between the outer and inner rings has to be more than the threshold voltage of one MOSFET multiplied by the number of interstices between the rings [26,76].

3.3.11 Minimizing Capacitances

In order to improve the energy resolution as much as possible, all capacitances including the anode capacitance and stray capacitance (connection path to the external circuit), have to be minimized and carefully designed. Furthermore, in order to minimize the Equivalent Noise Charge (ENC), the capacitance of the externally integrated JFET has to be matched by the capacitance of the detector [83]. Details will be discussed in the next chapter. For more information regarding calculation of the ENC the reader is kindly referred to the lecture notes of the C.Guzzoni [72]. By minimizing ENC^2 one can find the optimum value for the external circuit by taking the derivative of ENC^2 and then finding the required capacitance of the external circuit [35,76,84]:

$$\left.\begin{aligned} ENC_{opt}^2 &= \sqrt{A_1 A_3}\,\sqrt{2kTq}\underbrace{\sqrt{\frac{\alpha}{\omega_T}}}_{FET}\underbrace{\sqrt{C_{Det} I_L}}_{detector}\underbrace{\left(\sqrt{\frac{C_G}{C_{Det}}}+\sqrt{\frac{C_{Det}}{C_G}}\right)}_{matching} + ENC_{1/f}^2\left(C_T^2\right) \\ ENC_{opt} &= \sqrt[4]{\frac{2kTq}{\pi}} \times \sqrt[4]{\frac{I_{Leak}.C_{\det}}{f_T}} \times \underbrace{\sqrt{\sqrt{\frac{C_{\det}}{C_i}}+\sqrt{\frac{C_i}{C_{\det}}}}}_{matching} \end{aligned}\right\} C_{FET} = C_{detector} \qquad (3.14)$$

where A_1 and A_3 are shape factors; C_G is the gate capacitance; C_{det} is the detector capacitance; $ENC_{1/f}^2$ is ENC in presence of 1/f noise and/or dielectric losses; and C_T is capacitor dielectric losses.

3.3.12 Guard Ring

The breakdown voltage is an important parameter in designing X-ray detectors such as silicon drift detectors. In SDDs complete thickness of the wafer has to be depleted to enable detecting different energies of X-rays. A high voltage is required to have a fully depleted region while keeping leakage current at lower values. Multi-guard ring structures are designed to meet both lower leakage current and higher breakdown voltages using deposited PureB layers. These structures will be discussed in details in the next chapter.

3.4 Applications of PureB in Silicon Drift Detectors

In this section the advantages of using a boron layer in silicon drift detectors will be discussed in more detail. Below are the topics where a boron layer can improve the performance of the SDDs.

1. PureB nm-thin front entrance windows for sensitivity down to 100 eV X-rays.
2. Using a boron layer with high sheet resistance as a voltage divider between implanted rings in the device side of conventional circular SDDs.
3. Replacing p^+ implantations of drift rings with a boron layer in conventional circular SDDs to lower the leakage current.
4. Continuous SDD structure using a boron layer to reduce surface leakage current.
5. Continuous SDD structure using a double boron layer to obtain a radial uniform electric field for drift rings and lower leakage current at the same time.

3.4.1 SSD Entrance Window Using Boron Layer

Detectors were fabricated in high resistivity wafers with <100> orientation since a <100> oriented wafer has higher charge collection efficiency (CCE) (higher quantum efficiency) than a <111> oriented wafer in soft X-rays. Furthermore, the absorption in a dead layer of the detector is an important parameter that limits the detection of low energy X-rays. In order to reach a good response in the low energy range (a few hundred eVs), what is needed is a very shallow implantation of the p^+ back contact that acts as a radiation entrance window [1]. In order to enhance the quantum efficiency and obtain a good response in soft X-rays down to a few hundred eV, an entrance window can be fabricated with a few nanometer boron layer which limits the insensitive area or dead layer.

The PureB technology is used in silicon drift detectors (SDDs) for the detection of X-rays down to energies as low as 100eV [85]. This corresponds to soft X-ray

wavelengths around 10nm, for which range PureB p^+n photodiodes have already proven their worth in extreme-ultraviolet (EUV) detectors for 13.5nm advanced lithography systems. Moreover, they now also have wide application as low-energy electron detectors for commercial scanning electron microscope (SEM) systems. For successful implementation of PureB front entrance windows in silicon drift detectors, several aspects are taken into consideration. Processes have developed for the fabrication of the entrance window where the dead layers (optically absorbing layers) are formed by only a 2-nm-thick pure boron layer under which a comparable thickness of p^+-doped silicon is created to form the junction to the photosensitive depleted n-region. However, the exact design of the p^+-region perimeter, i.e., the oxide isolation and guard ring design, is decisive for the detector leakage and breakdown voltage. Guard ring design will be discussed in the next chapter in detail.

3.4.2 Comparing Potential Distribution in PIN Detector and SDD

In this thesis devices were fabricated in 500µm-thick, high resistivity silicon wafers of 2-10 kΩcm, corresponding to a bulk doping concentration of 2.2×10^{12} - 4.4×10^{11} 1/cm^3, which resulted in the required 420-84V depletion voltage, respectively (according to $V_{dep} \cong \frac{q.N_D.d^2}{2\,\varepsilon_{Si}}$).

Figure 3.10 schematically illustrates the planar p-n detector and simulation results for voltage distribution over the wafer. The bulk doping of the wafer is assumed to be constant in the whole volume of the detector.

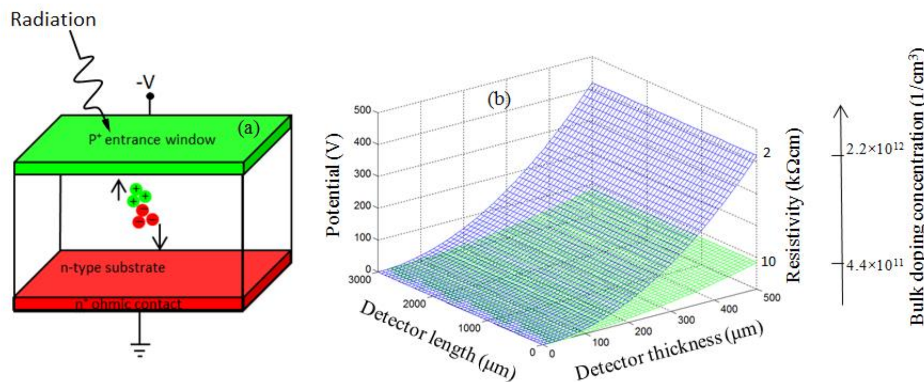


Figure 3.10: a) Schematic of a PIN detector and carriers movement in a reverse bias region and b) voltage distribution over the detector thickness for different resistivity of the wafers.

Figure 3.11a illustrates a conventional SDD with concentric p^+ junctions, anode and integrated JFET on the device side and continuous p^+ junction as the entrance window on the back side. The p^+ rings in the device side are biased with increasing potential toward the anode. With these strips we can obtain a nearly uniform drift field parallel to the surface where electrons are focused in the center of the wafer and are transported at a constant velocity towards the readout anode. The circular SDD can be realized with and without an integrated amplifier. Typically a JFET is placed in the center of the detector with a direct connection between the anode and JFET gate. Integration of readout electronics will be discussed in the next chapter in detail. In Figure 3.11b calculated potential distribution is shown for wafers with 2 and 10 kΩcm resistivity. As can be seen for the same design, detectors fabricated in the lower resistivity wafer require a higher depletion voltage and drift field. This means that the drift time will be lower for low resistivity wafers.

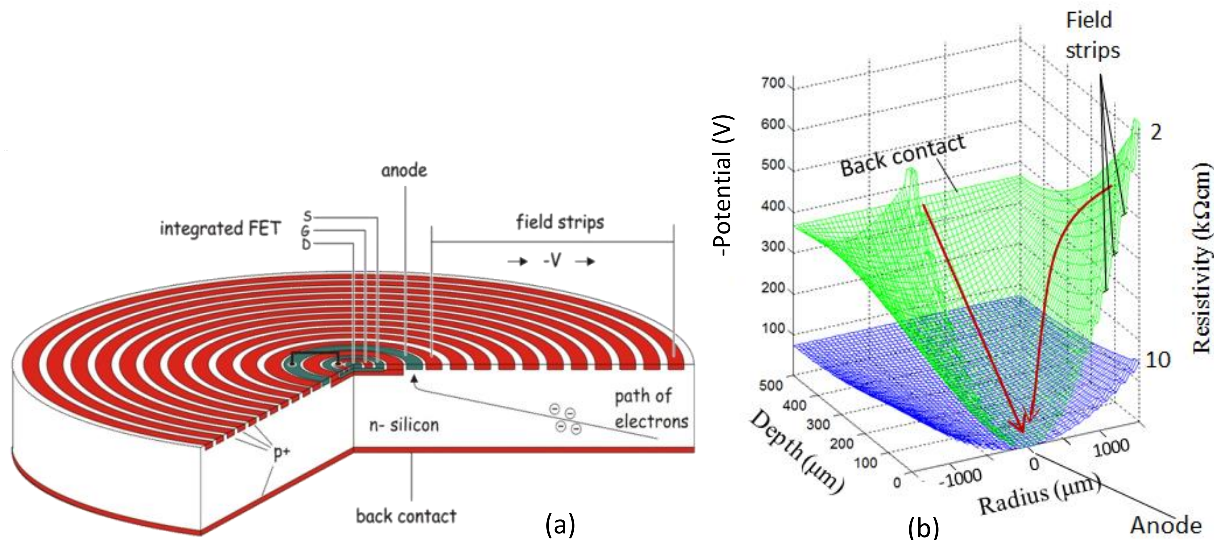


Figure 3.11: a) Circular silicon drift detector [28]; and b) calculated potential distribution.

3.4.3 Voltage Divider Using Boron Layer and Implantation

In the designed SDDs different integrated voltage dividers were used to connect to neighboring p+ rings such as the implanted layer, boron layer or punch

through. All rings are biased by applying voltage to the first ring near the anode and the last one at the edge of the detector.

Implanted Layer

Typically in SDDs, each p^+ ring is connected to the neighboring ring using an implanted layer. Figure 3.12 illustrates the designed layout of the SDD structure with implanted voltage divider as a reference to compare with other divider methods. Resistance between the rings depends on the sheet resistance, width and length of the implanted layer. In order to have low power consumption, this resistance should be high. If one uses layers with low sheet resistance then long and meandering resistors are necessary to obtain high resistance values (more than 100 kΩ). However, if layers with high sheet resistance (~10 kΩ/□) are used, design is easy but the drawbacks are nonlinear behavior of resistance with bias, and poor doping reproducibility. In this thesis boron implantation is used with 180keV energy and 10^{13} 1/cm^2 dose which creates the low doped p^- layers with sheet resistance in the range of ~1.8 kΩ/□.

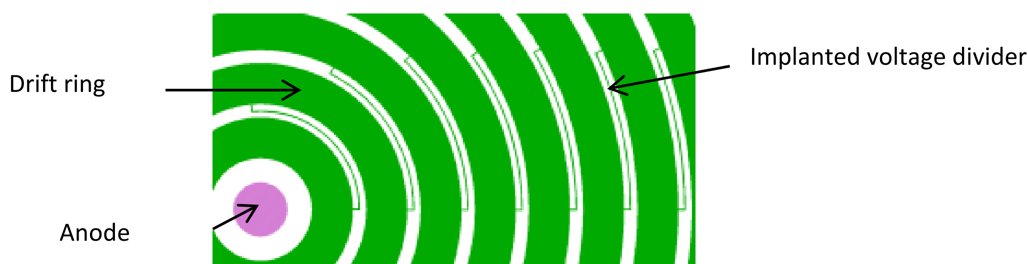


Figure 3.12: Designed layout of SDD with implanted voltage divider.

PureB Resistor

High Ohmic PureB resistors were introduced in Chapter two. In this thesis, for the first time we employ the PureB resistors in silicon drift detectors to divide the drift voltage between drift rings. SDD structures have designed with resistors made with PureB layers deposited at 500°C and 700°C. The designed SDD using a PureB layer as a voltage divider is displayed in Figure 3.13. In this design the PureB layer is placed between the inner and outer ring in a continuous form and

intersects the implanted drift rings. Experimental results of high-Ohmic PureB resistors as a voltage divider for SDDs will be discussed in Chapter 5.

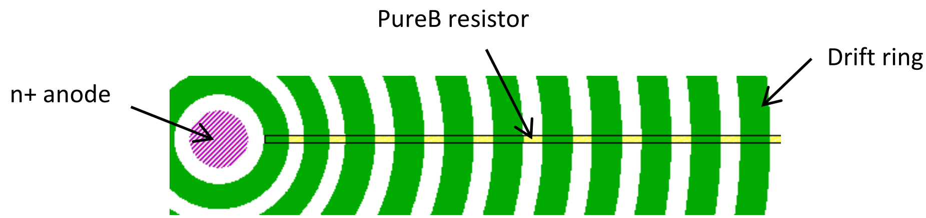


Figure 3.13: Layout design of the SDD using a PureB voltage divider. The implanted drift rings and PureB voltage divider are seen in this figure.

Pinched Resistor

One of the common solutions for high Ohmic integrated resistors is pinched resistors. They have sheet resistance values around 30kΩ/□, with a small parasitic junction capacitance. However, pinched resistors are bias dependent. This kind of the resistor was used in the SDDs structures. Figure 3.14 shows a schematic of pinched resistor.

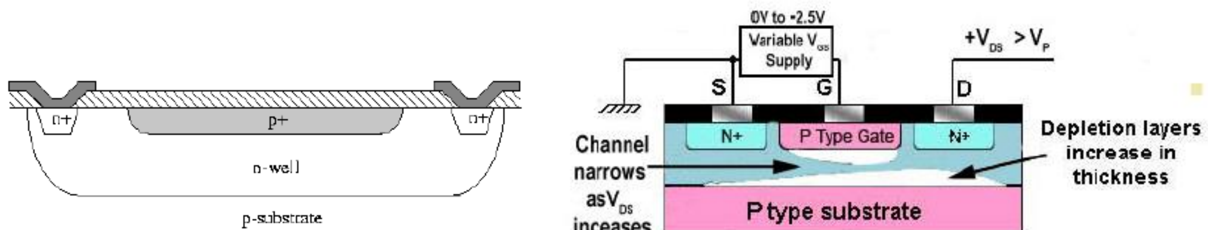


Figure 3.14: Schematics of Pinched resistors [86,87].

3.4.4 Potential Distribution in Continuous SDD Using One Boron Layer

One of the challenges in the SDD is high surface leakage current generated at the Si-SiO_2 interface between p^+ drift rings. One possible way to eliminate this surface leakage current is using a sink anode as described above. However, when using a

sink anode structures, some part of the radiation created electrons will be lost in the sink anode [78].

In this thesis for the first time we introduce a new kind of silicon drift detector using a deposited pure boron layer. This layer at the same time acts as distributed biased resistance to drift the electrons toward the anode and a shallow junction p-n diode with a very low leakage current. Since in this structure there is no oxide layer in the drift region, the leakage current will be lower and stable over time. The designed layout of the continuous silicon drift detector is shown in Figure 3.15, where the anode has been placed in the center of the detector and drift region is a continuous-area with a ~3mm radius, which is covered by an amorphous boron layer as distributed resistance. Guard rings, which will be discussed in detail in the next chapter, are designed to reduce the leakage current of the detector and prevent any possible voltage breakdown in the detector. On the opposite side of the detector the entrance window is covered by a high performance shallow junction p^+ layer, PureB, acting as the entrance window confined by p^+ guard rings. A 3D schematic diagram of whole design is illustrated in Figure 3.15.

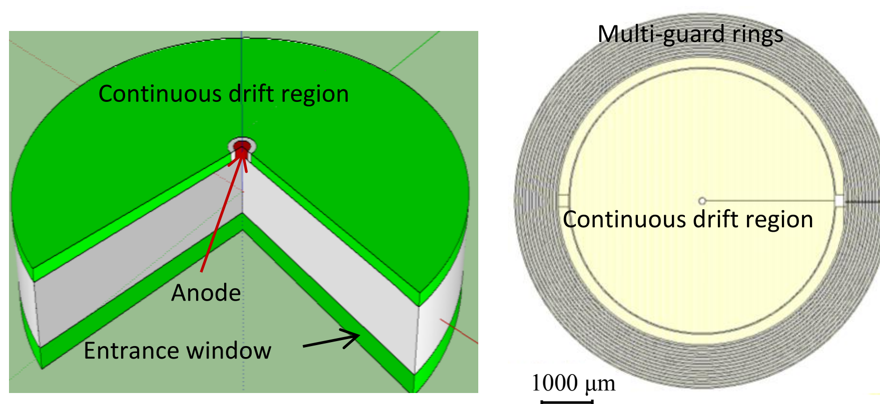


Figure 3.15: Designed layout of continuous SDD (right) and 3D schematic diagram of the designed continuous SDD (left).

Calculation of Electric Field in a Continuous Design

In the continuous drift design concept, resistance between the inner and outer contact pads is not uniform. It can be shown that the resistance of a ring shaped

area has the following relation with the layer sheet resistance, width and length of the ring as illustrated in Figure 3.16 [57]:

$$R_{ij} = R_{sh} \frac{L_{ij}}{2\pi r_g} \ (\Omega) \tag{3.15}$$

where L_{ij} is length, $2\pi r_g$ is the width of the resistance, and R_{sh} is the sheet resistance of the layer.

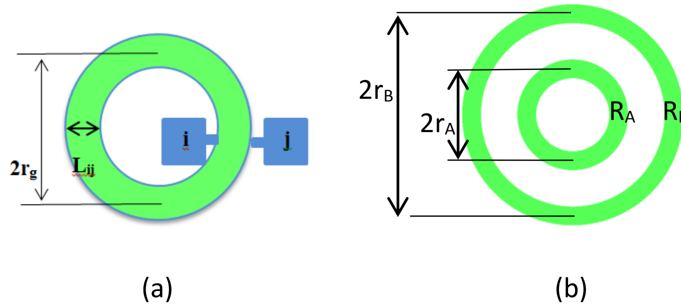


Figure 3.16: Calculation of resistance of a ring shape structure.

In a continuous SDD structure, the drift region is a ring shaped resistor; the resistance over the drift region can be calculated with the formula above. As Figure 3.16b shows for the same length, the resistance near the anode, $R_A = R_{sh} \frac{L}{2\pi \times r_A}$, is much higher than the resistance in the outer part, $R_B = R_{sh} \frac{L}{2\pi \times r_B}$, of the drift region. Therefore there is non-uniformity in the resistance distribution from the anode to the edge of the detector. The calculated resistance distribution over the drift region of the continuous design using the above formula, is shown in Figure 3.17 where the resistor value drops in the outer areas significantly. This plot shows that the resistor value close to the inner ring is 30 times more than at the outer ring. For our designed detector with an inner radius of 135µm and outer ring radius of 3135µm using a boron layer with a sheet resistance value of $10^5\Omega/\square$, the total resistance between the contact pads is equal to 50kΩ.

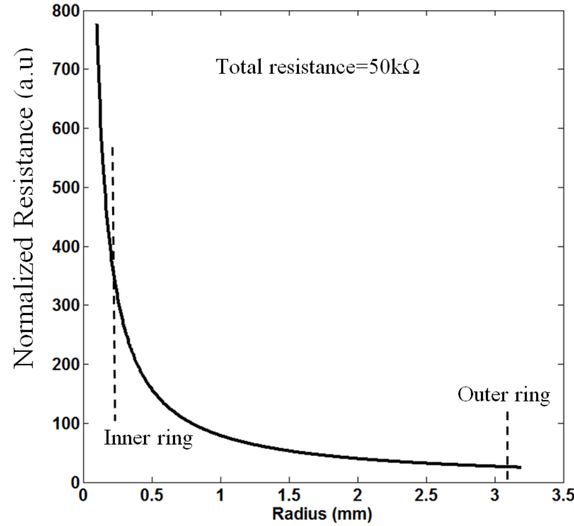


Figure 3.17: Calculated resistance distribution over the drift region of the continuous structure.

This non-uniformity in the resistance over the drift area results in a non-uniform electric field.

From the calculated resistance as a function of the detector radius, the potential can be written using Ohm's law as:

$$V(r) = \left(\frac{\Delta V}{R_T}\right) R(r) \qquad \text{(V)} \qquad (3.16)$$

where V(r) is the voltage at the radius r; R(r) is resistance over the drift area as a function of the detector radius; R_T is the total resistance from the inner ring to the outer ring; and ΔV is the applied external voltage between the inner and outer rings. The electric field can be derived from the voltage:

$$E(r) = -\frac{\partial V(r)}{\partial r} \qquad \text{(V/cm)} \qquad (3.17)$$

The electric field can be plotted for a specific applied voltage along the detector radius. In Figure 3.18 the electric field is plotted for applied external voltages of 40, 80, 120 and 160V in both the linear and log scales. It can be seen that electric field is around three orders of magnitude less in the outer ring, thus it is only effective at the inner side of the detector as there is not enough electric field to move the electrons toward the anode in the outer sides of the detector.

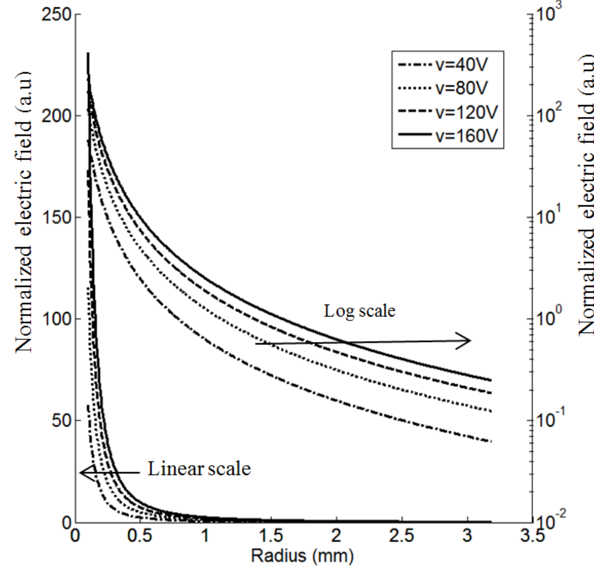


Figure 3.18: Calculated electric field of the continuous SDD; as a function of the detector radius in the linear and log scales for different applied external drift voltages.

One can calculate the electric field over the drift area from Poisson's equation as well:

$$\nabla^2\Phi = \frac{dE}{dX} = -\frac{\rho}{\varepsilon_0\,\varepsilon_{Si}} \qquad (3.18)$$

where Φ is the potential distribution, E is the electric field over the drift area, and ρ is the charge density in the silicon bulk.

In cylindrical coordinates the Laplacian operator can be written as:

$$\nabla^2\Phi = \frac{1}{r}\frac{\partial}{\partial r}\left(r\,\frac{\partial\Phi}{\partial r}\right) + \frac{1}{r2}\frac{\partial^2\Phi}{\partial\theta^2} + \frac{\partial^2\Phi}{\partial z^2} \qquad (3.19)$$

Assuming the simple case of one directional voltage distribution only in the r direction, this equation can be written as:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\,\frac{\partial V}{\partial r}\right) = -\frac{\rho}{\varepsilon_0\,\varepsilon_{Si}} = -q\,\frac{N_D}{\varepsilon_0\,\varepsilon_{Si}} \qquad (3.20)$$

The electric field can be derived as:

$$E(r) = ar + \frac{b}{r} \qquad (V/cm) \qquad (3.21)$$

where a and b are constants and can be extracted from boundary conditions of the potential distribution. Plotting this formula will give a similar curve as Figure 3.18.

In order to calculate the electric field and voltage distribution along the detector thickness one can use the following equation. Since complete thickness of the detector is fully depleted by biasing the entrance window, the following formula can be written from the depth of the depletion region of a p^+n junction diode:

$$V_{dep} \cong \frac{q.N_D.d^2}{2\,\varepsilon_{Si}} \quad (V) \qquad (3.22)$$

where V_{dep} is the depletion voltage of the silicon wafer; q is the elementary charge; N_D is the donor concentration in the n-type high resistivity silicon wafer; d is the detector thickness; and ε_{si} is silicon permittivity.

Figure 3.19 illustrates the calculated potential distribution of a continuous SDD structure over the depth and radius of the detector for different bias voltages. The back side or entrance window is kept at -80V, which corresponds to the full depletion voltage for a 10kΩcm high resistivity wafer with 500μm thickness. The front side or drift region is biased with -10V in the inner ring and -50V or -170V in the outer ring. It can be seen that the electric field, the slope of the voltage distribution at the surface of the detector, is very small at the edge of the detector. Electrons will then be accumulated in the gutter, the minimum of the potential energy, and will be moved slowly to the anode. At 160V drift voltage, the slope along the detector surface is lightly sharper than the 40V case but still too small to drift the electrons toward the anode. There are limits to how much one can vary the potential along the detector. The potential at the edge of the detector is limited to two times the depletion voltage. Any increase of this potential would lead to a reach-through condition with a large current flowing between the p^+ regions at both sides [71].

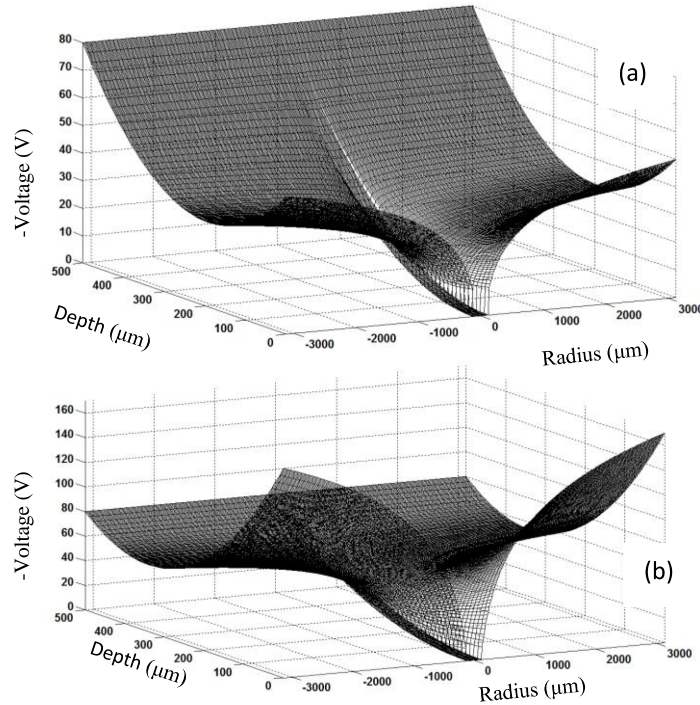


Figure 3.19: Calculated potential distribution of the continuous SDD as a function of the detector thickness and radius for two different drift voltages (40V and 160V). The entrance side is kept at 80V, which corresponds to a full depletion voltage for a 10kΩcm silicon wafer.

Figure 3.20 plots the calculated results for the drift time for electrons. Assuming high mobility for electrons in the low doped silicon bulk under the above-mentioned external field, one can calculate the drift time from the following formula:

$$t = \frac{d}{v} = \frac{d}{\mu E} \quad , \quad t = \int_{r=r2}^{r=r1} \frac{r}{\mu E(r)} dr \qquad (3.23)$$

where t is the drift time; d is distance; v is the velocity; and μ is the mobility of the electrons. For small ranges of r_1 and r_2 we can plot drift time versus radius as shown in Figure 3.20. This plot shows drift time is around 4 order of magnitudes longer for the electrons generated at the edge of the detector than those generated close to the anode. This observation shows that a continuous layer of resistor is not efficient for drifting the electrons toward the anode with a reasonable drift time.

Based on the above-mentioned calculation results, the continuous SDD, although offering lower leakage current, have a non-uniform electric field, which is also very small at the edge of the detector creating longer drift time for electrons. It can be seen that around 80% of drift area has almost zero electric field. In order to have an acceptable drift field and time, either detector size should be very small or the structure should be changed.

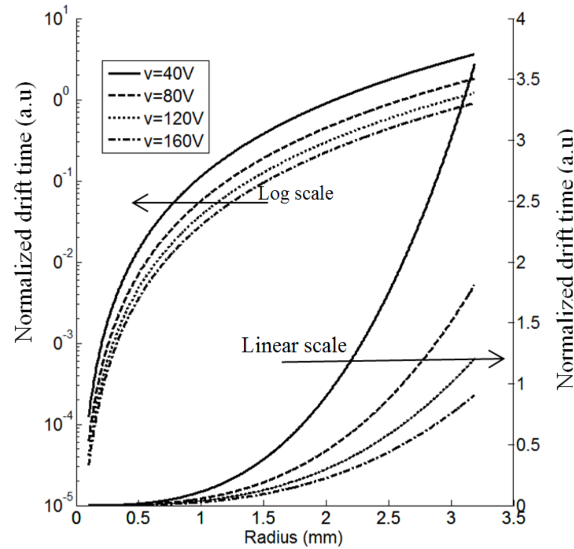


Figure 3.20: The calculated drift time of continues SDD, as a function of detector radius in linear and Log scales for different applied external drift voltages.

3.4.5 Potential Distribution in Constant Field SDD Using Dual Boron Layers

As mentioned above, the goal is to design a detector with low leakage current and a uniform electric field. A continuous PureB layer with specific sheet resistance cannot maintain a uniform electric field. This is due to different resistor values in different radiuses over the drift region. Uniform resistance can be obtained by using two different sheet resistance layers and a suitable design. Two different sheet resistance layers can be achieved by combination of two boron layers deposited at different conditions, i.e. temperature and time. In this design, the drift region is continuous and is divided into several rings with different lengths.

In order to have the same voltage drop in each pitch, all pitches must have same resistance. By knowing the sheet resistance values and number of drift rings, the pitch and length of each ring can be extracted to have similar resistance in each pitch. The first and last pitches of the drift region are illustrated in Figure 3.21.

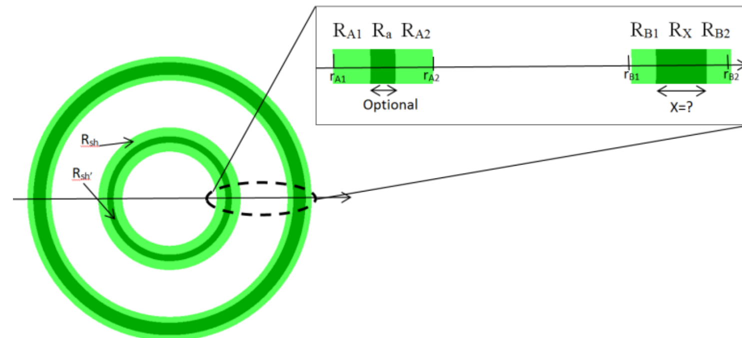


Figure 3.21: Designing width and pitch of each drift ring to obtain similar resistances for all rings.

It can be seen that each pitch has three components containing two regions with low sheet resistance and one region in the middle with high sheet resistance. With changing length of the high resistance region of the first pitch and taking into consideration equal resistance value for all pitches, lengths of the remaining regions can be calculated using formula 1. In the calculated structure, the contribution of the lower sheet resistance layer is high near the anode region, while at the edge of the structure, contribution of the higher sheet resistance layer is more the other one to maintain similar resistance for all drift rings. In the designed SDD, the drift region is divided into 144 pitches. With 100KΩ/□ and 1MΩ/□ sheet resistances for the two boron layers, a total resistance value of 150KΩ was obtained for the complete drift region.

Figure 3.22 illustrates the designed layout of the SDD with dual boron layers to have a radial uniform electric field and continuous drift structure. In this design the whole surface has been covered with a boron layer to have minimum leakage current. It can be seen that low sheet resistance layer is denser near the anode.

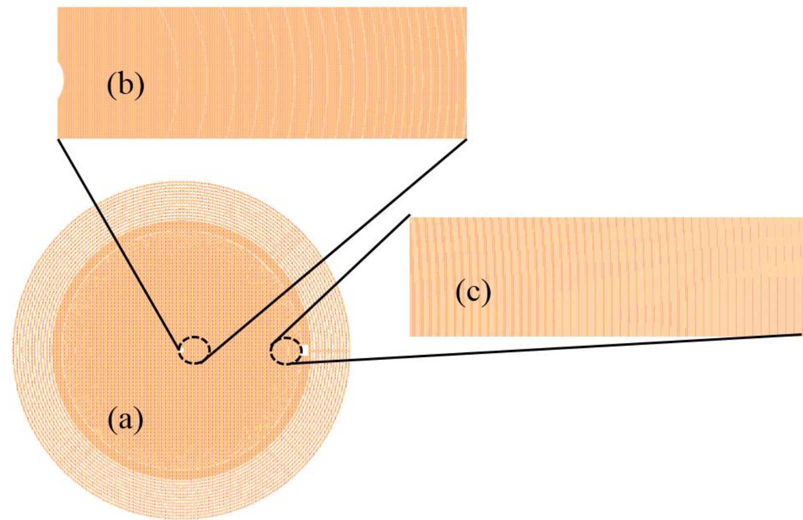


Figure 3.22: (a) Snapshot of the designed layout of the SDD using dual boron layers, (b) highlighted inner part and (c) outer region of the drift area.

Figure 3.23 displays 3D calculated potential distribution of the constant field SDD structure over the depth and radius of the detector for a 10kΩcm high resistivity wafer and two biased drift voltages at -40V and -160V with an entrance window biased at -80V. It can be observed that the voltage slope at the surface of the detector is much sharper with respect to the continuous SDD and it is constant which means a constant electric field is maintained. Electrons generated in the bulk drift to the minimum value of the potential and then to the anode due to the drift fields maintained by the rings and entrance window bias.

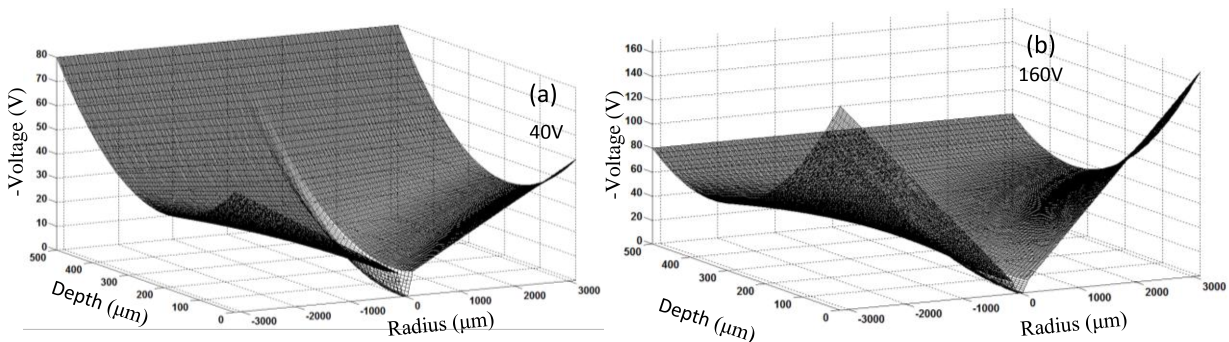


Figure 3.23: Calculated potential distribution of the constant field SDD structure with 40V and 160V drift voltages. Potential slope is constant in the drift region.

Figure 3.24 illustrates the cross-section and potential distribution along the electron transfer direction for three different kinds of SDDs. In a conventional circular SDD (Figure 3.24a) there are drift rings (p^+ implants) separated by an oxide layer creating a drift electric field with several steps. Because of the presence of oxide the surface leakage current will be high. The continuous SDD structure (Figure 3.24b) with one layer of PureB, has a non-uniform electric field and slow drift time but a lower leakage current. The SDD with two layers of boron and constant electric field (Figure 3.24c) has the advantage of both lower leakage current and constant drift field.

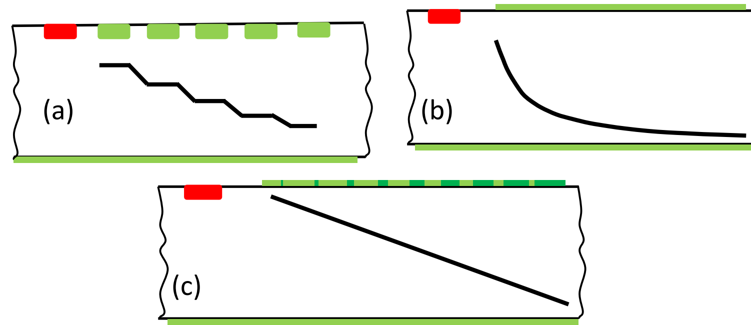


Figure 3.24: Cross-sections and potential along the transfer direction for (a) a conventional circular SDD using implanted rings, (b) a continuous SDD using a PureB layer, and (c) a continuous SDD using dual PureB layers.

3.5 Overview of the Designed SDDs Using the Boron Layer

In this project different circular SDD structures have been designed and fabricated. The active area of all SDDs is the same (with a radius of $R_{Active\ area}$= 3135μm). The entrance window of SDDs has been made with either the ultra-shallow PureB or implanted layer for comparison. For both sides of the detectors, multi-guard ring structures have been designed. In two SDD structures different on-chip electronics have been integrated. Guard rings and on-chip electronics will be discussed in the next chapter. Detectors with different pitches of drift rings have been designed to study the influence of them on the parameters of SDDs. The drift rings have been fabricated either with PureB or an implanted layer. Different Field Plates (FP) have been used in some of the structures. The voltage

divider between the drift rings have been designed either with PureB or an implanted layer. In one of the designed structures drift rings are connected by punch through phenomenon. Finally a novel structure has been designed to obtain a radial uniform electric field for drifting the produced charges. Table 3-1 shows a summary of the different designed SDDs. In Chapter 5 the results of the electrical measurements will be reported.

Table 3-1: Details of the designed SDD structures

	R_{Active} (µm)	Anode (µm)	R_1 (µm)	$d_{Anode-R1}$ (µm)	Oxide (µm)	Ring (µm)	Pitch (µm)	$N_{drift\ ring}$	$V_{divider}$ (µm)	FP	On-chip electronics	Guard ring	n+ around guard (µm)
V7-1	3135	R=75	R=104	29	36	24	60	51	20×2980 PureB	+	–	N=13 R_{out}=4010	R_1=4160 R_2=4310
V7-2	3135	R=80	R=110	30	50	70	120	26	20×2900 PureB	+	–	N=14 R_{out}=4414	R_1=4714 R_2=4850
V7-3	3135	R=70	R=108	38	21	34	55	55	20×2940 PureB	+	–	N=19 R_{out}=4430	R_1=4650 R_2=4800
V7-4	3135	R=80	R=138	58	------	------	-----	------	---------	---	–	N=14 R_{out}=4414	R_1=4714 R_2=4850
V8-1	3135	R_1=37.5 R_2=47.5	R=83	35.5	6	24	30	102	10×3010 PureB	+	+	N=13 R_{out}=4010	R_1=4160 R_2=4310
V8-2	3135	R=50	R=95	45	25	75	100	31	2×320 imp.	–	–	N=14 R_{out}=4414	R_1=4714 R_2=4850
V8-3	3135	R=70	R=110	40	50	70	120	26	20×2900 PureB	±	–	N=19 R_{out}=4430	R_1=4650 R_2=4800
V8-4	3135	R_1=33.8 R_2=40.6	R=75	34.5	50	70	120	26	20×2936 PureB	+	+	N=14 R_{out}=4414	R_1=4714 R_2=4850

3.6 Conclusions

In this chapter after introducing the PIN and SDD structures, different aspects of designing SDDs were discussed in detail. Then the boron layer was introduced as an ultra-shallow junction entrance window for low energy X-rays and as a voltage divider in the drift side. Single and double boron layers were introduced to drift the electrons toward the anode while rectifying p-n junctions have very low leakage current. The reason is that there is no oxide present in between rectifying diodes, thus the surface leakage current is low.

Calculations and simulations showed that a single boron layer does not provide a sufficient electric field to drift the electrons toward the anode. The electric field was around three orders of magnitude less in the outer ring thus it is only effective at the inner side of the detector and there was not enough electric field to move the electrons towards the anode in the outer sides of the detector. The potential

distribution showed that at 40V applied voltage, electrons are accumulated in the gutter, the minimum of the potential energy, and are moved slowly to the anode. At 160V drift voltage, the slope along the detector surface was lightly sharper than the 40V case but still too small to drift the electrons toward the anode. Therefore around 80% of the drift area had an almost zero electric field. Using the double boron layer process with different sheet resistances and a special design, the electric field was constant over the drift region with very low leakage current. In this design a low sheet resistance layer was denser near the anode and high sheet resistance layer was present in the outer rings to produce a constant resistance and electric field over the drift area. At the end the details of the designed SDD structures were shown briefly.

Chapter 4

Integrating On-Chip Electronics and Multi-Guard Rings in PureB-SDDs

4.1 Integrating n-Channel JFET and Reset Devices in SDDs

4.1.1 Introduction

Unlike avalanche type of detectors where a multiplication mechanism amplifies the signal, there is no intrinsic amplification mechanism in silicon drift detectors. Therefore an amplifier is required to amplify the small ionization signals and increase the energy resolution performance of the detector. Since there is very close interplay between the detector and its external amplifier, both of them should be considered in the design of the detector [35,6,4]. The amplifier can be integrated on the detector chip (front-end electronics) or it can be an off-chip amplifier [65,66]. Using an integrated amplifier can prevent undesirable interference effects related to wire bonding such as stray capacitance and microphonic noise [90]. Therefore, this leads to minimum stray capacitance and better matching capacitances between the detector and input amplifier [91]. Since the input stage of the preamplifier (the first transistor) is the crucial element, it is integrated on the detector chip, normally on the opposite side of the entrance window [92]. Figure 4.1 illustrates an integrated n-type JFET on the silicon drift detector chip where the transistor is located inside the anode area on the device side of the detector. The drain is in the center, the gate is connected to the anode and the source surrounds the top gate of the transistor. Collected electrons in the anode increase the negative voltage on the p+ gate and deplete the transistor channel more and more. Therefore the transistor current (common source

configuration) or the source voltage (source follower configuration) drops. This change in current or voltage can be amplified and measured by an external circuit [93]. The p-type ring around the transistor acts as a guard ring between the transistor and the anode. The transistor area is separated from the detector bulk by a deep p-implanted well (Figure 4.1). This circular p-type area acts as a back gate for the JFET and prevents electrons from drifting toward the n-regions of the source and drain. A source-follower is the most used configuration where source is connected to an external current supply.

In order to discharge the accumulated charges (electrons) on the anode, different types of reset mechanisms are used [35].

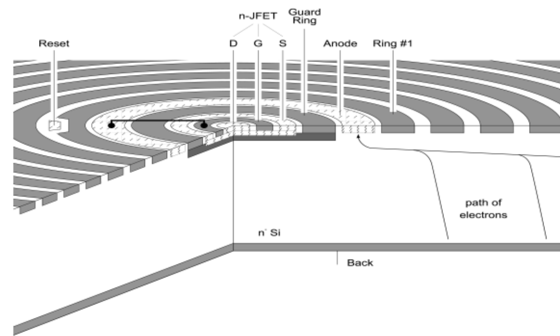


Figure 4.1: Central area of a cylindrical silicon drift detector with an integrated amplifier [90]. The entire silicon wafer is sensitive to radiation.

Following to the single transistor amplification, as shown in Figure 4.2, an external amplifier and integrator circuit using an operational amplifier is used. The signal pulses will be amplified and converted to voltage using this stage. The input stage of a charge amplifier is a low noise JFET with high open gain and low output impedance as a buffer to drive the next stage. Depending on the application, different types of amplifier configurations can be used. The charge-sensitive mode is used for low noise applications and the current-sensitive mode is used when high speed is required. The next stage is called the multichannel analyzer (MCA) where the analog signal is converted into a digital pulse, and a histogram of the energy of the detected photons is produced. The height of the pulse is proportional to the energy of the incoming X-ray. The MCA counts the number of pulses and converts the histogram into a curve which plots counts vs. energy.

The ability of the detector system to count photons in an efficient way is called sensitivity. At the end a computer processes the data and assigns elements to the different energy peaks as shown in the Figure 4.2 spectrum. The ability of the detector to distinguish between different energy levels is called resolution [91]. There are some commercial electronic circuits available with all describe blocks in one system. A power supply with different voltage levels is required to bias the detector and the Peltier cooler which are normally available in those systems [92].

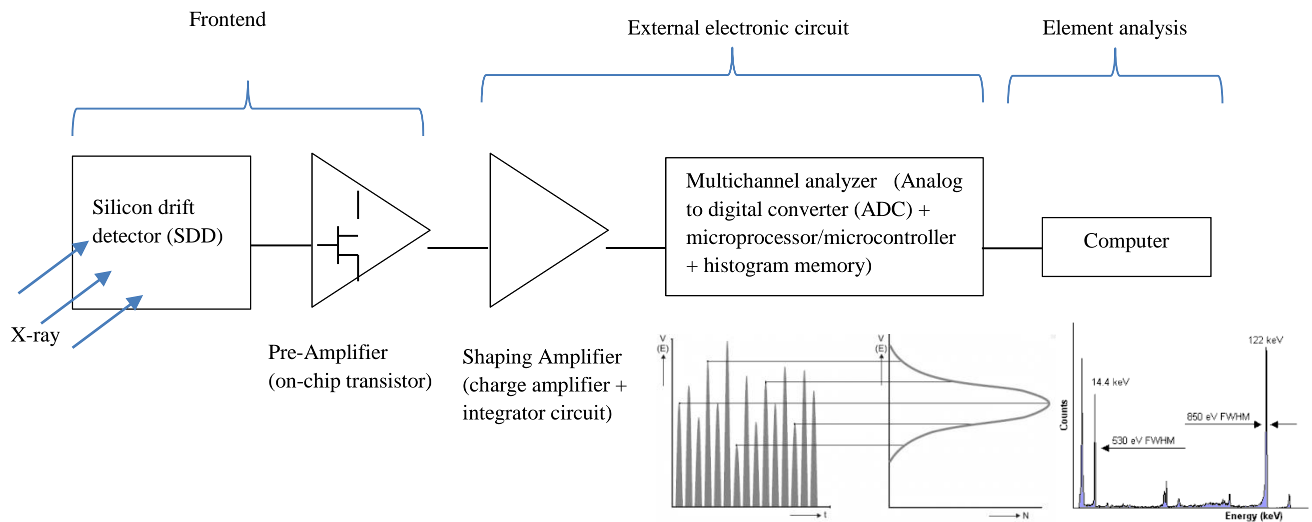


Figure 4.2: Block diagram of detector and post processing stages [Figures from 91].

4.1.2 Noise Considerations in SDDs

Amplifiers used in detectors generate two categories of noise: parallel noise coming from the dark current and biasing circuit, and series noise created from the amplifier [6]. The input stage of the preamplifier, which is the first transistor, is the crucial element in terms of noise consideration in the whole detector system [31].

The optimum resolution which can be achieved for a detector with a preamplifier followed by an optimum signal processor can be expressed, in terms of equivalent noise charge (ENC), as below [93]:

$$ENC_{opt} = (2qkT/\pi)^{1/4}.(I_l.C_d/f_t)^{1/4}.\left((C_d/C_i)^{1/2} + (C_i/C_d)^{1/2}\right)^{1/2} \quad (4.1)$$

where I_l and C_d are the detector leakage current and capacitance, and C_i and f_t are the capacitance and the bandwidth of the input device of the preamplifier, respectively. It can be proved that the best resolution is achieved when $C_i = C_d$ which means the capacitance of the preamplifier has to be matched to the output capacitance of the detector [93]. Since the output capacitance of the silicon drift detector is extremely low, in the order of 100fF and independent of the SDD area, potentially a high energy and position resolution can be achieved even at room temperature [94]. In order to match the impedances, the input capacitance and stray capacitances of the connection between the detector and preamplifier have to be kept as small as possible, and in the same order (around 100fF).

However, the gate capacitance of the external JFET used in the circuit is high (typically around 3pF) with additional stray capacitances for the connection (typically around 1-2pF) [31]. Therefore, in order to fully obtain the best characteristics of the detectors, direct integration of the front-end JFET into the detector is necessary. Additional small noise sources in the detector can be generated from each of the blocks presented in Figure 4.2. It can originate from the detector, on-chip JFET or external electronics circuit.

In terms of the total noise contributed by the detector, all leakage current components that exist in the detector (such as bulk and surface generation currents and diffusion leakage current) can add noise to the system. Moreover, low frequency noise (1/f noise) can be generated due to mobility fluctuations, series resistance and generation-recombination.

For the on-chip contribution to the total noise, 1/f noise of the JFET and thermal noise are the main components. In a JFET, thermal noise is due to channel resistance. The white noise of the transistor channel can be expressed as [4]:

$$\frac{d\langle \Delta I_D^2 \rangle}{df} = 4kT(g_{m1} + g_{m2}) \frac{\langle Q_C \rangle}{Q_C(y=0)} \quad (4.2)$$

where g_{m1} and g_{m2} are transconductances of the top and bottom gates of a JFET, respectively. This noise can be modeled by a white noise voltage source at the gate of the transistor using the following formula [4]:

$$\frac{d\langle v_n^2\rangle}{df} = 4kT\frac{2}{3}\frac{1}{g_m} \qquad \text{where} \quad g_m = g_{m1} + g_{m2} \tag{4.3}$$

In this equation it is assumed that the source and back gate contacts are connected to ground.

Generated noise from external electronic circuits is mainly low frequency voltage noise and shot noise. In most electronic devices there is a low frequency noise which is dependent on fabrication process technology and crystal defects. JFET and depletion mode MOSFETS show lower low frequency noise than other transistors. The noise power spectrum is described by [4]:

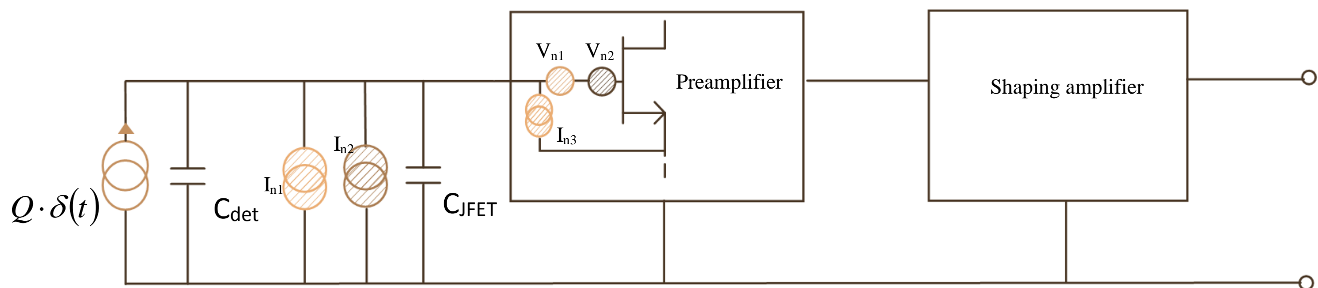
$$\frac{dU_n^2}{df} \approx \frac{A_n}{f^\alpha}, \quad \text{with} \quad \alpha \approx 1 \tag{4.4}$$

Thus the 1/f dependence is only a rough approximation.

Shot noise is another noise source in electronic circuits which is generated due to electric charges. Shot noise does not exist in MOSFETS and has a minor role in JFETs. It can be modeled as a current source with the frequency spectrum of the noise current below [4]:

$$\frac{d\langle i_n^2\rangle}{df} = 2Iq \tag{4.5}$$

Figure 4.3 summarizes different components of noise in different stages of a detector system.



Noise source	Leakage current feedback resistor	Capacitor dielectric losses	Gate current shot noise	White voltage noise	1/f voltage noise
Noise value	$qI_L + \frac{2kT}{R_f}$	$2kTC\tan(\delta)\omega$	qI_G	$2kT\alpha / g_m$	$\frac{\pi A_f}{\omega}$
Symbol in the figure	I_{n1}	I_{n2}	I_{n3}	V_{n1}	V_{n2}

Figure 4.3: Noise modeling in different stages of a detector system [72].

4.1.3 Choice of the Front-end Transistor

On-chip or front-end transistors used in silicon drift detectors have to be operational in high resistivity silicon wafers when the full thickness of the silicon wafer is depleted by detector biasing. Therefore design, fabrication process and implantation parameters for the transistors are not the same as in standard CMOS technology [31,95].

For silicon drift detector applications, JFETs have been preferred over MOSFETs and Bipolar transistors, because of noise considerations. Bipolar transistors are not selected due to their large shot noise. The base current of a Bipolar transistor adds parallel noise to the system which can degrade the resolution. However, they have been used in some special applications where fast shaping and low power consumption are required [12]. MOSFETs have a higher 1/f noise component (current flows in the surface in the interface between Si and oxide). Moreover they have lower resistance to radiation damage, thus they are not suitable for detector applications. JFET transistors have lower noise and are therefore suitable for low noise applications.

Designing JFETs for detector applications requires a tradeoff between minimum noise and minimum capacitance with higher transconductance (g_m). The gate capacitance of a JFET can be calculated from the sum of capacitances of the gate-drain and gate-source with the following equation [96]:

$$C_G = C_{GD(gate-drain)} + C_{GS(gate-source)} = \frac{2\times W\times L\times \varepsilon}{x} \qquad 4.6$$

$$x = \left[\frac{2 * \varepsilon}{q} \; * \; \left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V_{gs} \; + \; V_{gd})\right]^{1/2}$$

$$C_G = \frac{2 \times W \times L \times \varepsilon}{(\frac{2 * \varepsilon}{q} \; * \; \left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V_{gs} \; + \; V_{gd}))^{1/2}}$$

where L is the gate length, W is the gate width, x is the depletion region width of the gate, N_A and N_D are the acceptor and donor concentrations for the gate (boron implantation) and the S/D (arsenic, phosphorous implantation), and V_{gs} and V_{gd} are applied voltages to GS and GD. Implantation energy defines gate depth or channel location and the implantation dose defines N_A and N_D. Since JFETs contain two gates, two gate capacitances can be calculated. In order to reduce the gate capacitance the following parameters can be used:

1) Reduce length and width of the gate electrode. For a gate length lower than 1µm, short channel effects will limit L reduction. Gate width reduction is limited by the technology to define the drain area as shown in Figure 4.1.
2) Increase width of the depletion region by reducing doping concentrations (until pinch off limits) and increasing channel thickness with higher implantation energy.

On the other hand, to obtain higher gain for the on-chip JFET, it is desired to have a higher g_m or transconductance for the JFET. From the following formula, g_m can be calculated [96]:

$$g_m \propto \; G_o = q * \mu_n * N_D \frac{2 * a * W}{L} \qquad (4.7)$$

where a is the depth of channel, W is the width, L is the length and G_o is the conductance of the open channel which is the depletion width at the bias voltage equal to zero.
It can be seen from Equations 4.6 and 4.7 that reducing the length of the JFET improves both the g_m and the capacitance. However, since increasing the channel width (W) and the doping concentration of the channel (N_D) increases both g_m

and the capacitance, there is a trade-off between them. For better resolution, a lower capacitance and higher g_m are required.

A lower capacitance or higher cut-off frequency JFET will result in lower 1/f noise as well. Since n-channel JFETs have a higher cut-off frequency (because of higher carrier mobility) than p-channel JFETs, for low noise applications an n-channel is preferred [97]. It is possible to use a p-channel JFET with a width three times larger to obtain a similar g_m as an n-JFET, but the gate capacitance will be high and the cut-off frequency will drop by the same factor [16,35].

4.1.4 Reset Mechanisms

In order to discharge the leakage current of the detector and accumulated electrons from radiation on the anode, a reset circuit is required. Figure 4.4 shows a schematic of a SDD with reset and feedback capacitance. Reset can be done either in continuous or pulse form, depending on the application and available technology. Pulsed reset systems require additional electronic circuits for timing and pulses. It should be mentioned that in order to obtain minimum node capacitance for the anode, all devices connected to the detector including the reset device, feedback capacitance and JFET, should be integrated in the SDD chip [34,35,97,98].

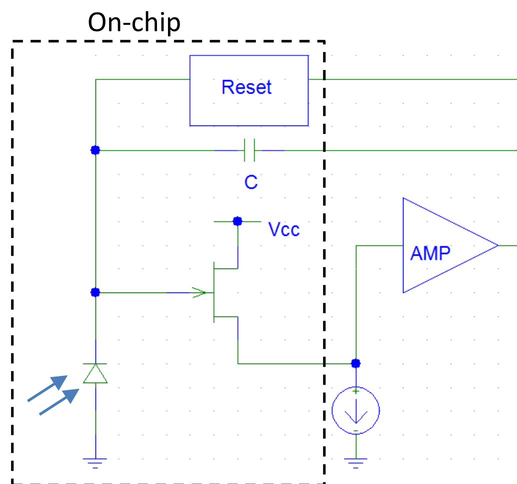


Figure 4.4: Schematic of a SDD with reset and feedback capacitance.

There are several mechanisms to discharge the collected electrons in the anode. A resistor is the simplest feedback element but passing detector leakage current

creates very high shot noise which disqualifies this element for the reset. Furthermore, fabricating such a big resistor (around 500MΩ) in a small area is extremely difficult. Using a diode as the reset device is not advised since it creates a voltage difference between the output and detector. Furthermore, fabricating a p^+ region near the anode and biasing the diode in the forward region may interfere with the electron collection by the anode and possibly cause a punch through current with the guard ring around the transistor [98]. Different types of transistors such as a JFET [34,35], MOSFET [97] and Bipolar transistor [89] have been used as a reset device in the detectors. Availability of technology and layout compatibility, minimum added noise and maximum linearity determine the choice of the reset transistor [99].

Figure 4.5a shows a pulsed reset system which uses an extra pMOS transistor to discharge the gate of the JFET (connected to the anode) by injecting holes from the source to drain of the MOSFET in the subthreshold region. The pMOS source is connected to the amplifier output as feedback; the drain is in the same region as the JFET gate which is biased at constant voltage [100]. Figure 4.5b shows continuous discharging by the gate-to-drain current of the on-chip JFET. In this configuration no extra device is used for reset. By increasing charges in the JFET gate, current passing through the gate to the drain increases, thus continuously discharging the anode charges [35]. In this configuration there is no need for an external reset pulse.

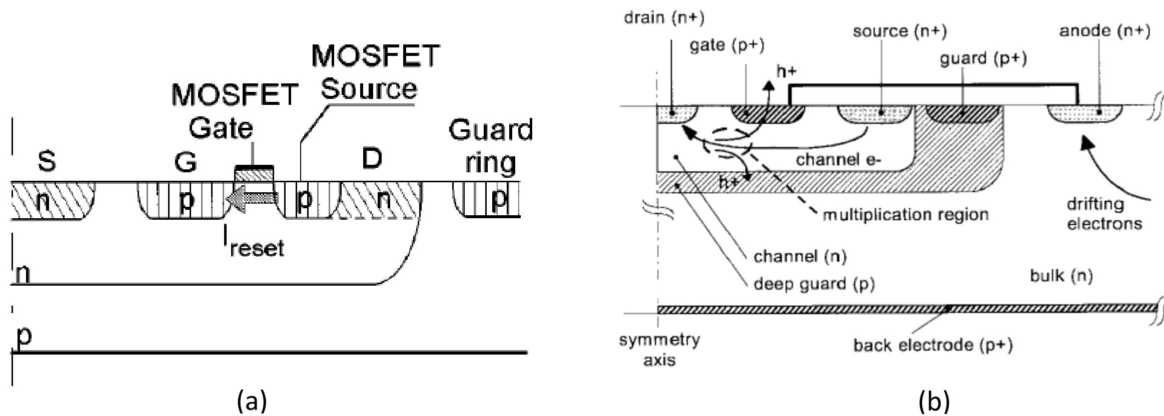


Figure 4.5: a) Pulsed reset system using a MOSFET [100]; b) continuous discharge by gate-to-drain current of an integrated JFET [35].

4.1.5 Designed On-Chip JFET and reset devices in boron layer technology

An on-chip front-end n-JFET transistor and two reset devices were adapted from literature-based studies using references [35,100]. For more information please refer to those papers. However, JFET dimensions and implantation parameters and fabrication were adapted to the boron layer technology flowchart for the final SDD device.

The designed n-JFET is a circular symmetry type transistor with a 4.5μm gate length located inside the n^+ anode ring and is isolated from the anode region by a reverse biased p-type guard ring. They are designed to operate in fully depleted high resistivity n-type silicon. To be compatible with the boron layer detector fabrication process, the doping of the transistor channel and the n-type electrodes were obtained by phosphorous implantation and the p-type electrodes by boron implantation plus boron layer deposition. As can be seen from the cross section shown in Figures 4.6 and 4.8, a circular deep boron implanted p-type layer separates the n^+ channel of the JFET from the fully depleted bulk underneath. Moreover, this p-type layer acts as a back gate for the transistor and it is biased through the p^+ guard ring.

Two types of on-chip JFET structures with different reset devices were designed for the SDDs shown in Figures 4.6 and 4.8. The reset devices are embedded either in the JFET or in the small anode region. In order to reset the accumulated charges on the anode, two mechanisms were used. The first one applies a positive voltage pulse to an n^+ implanted clear contact designed either in the anode ring or in the first p^+ ring of the drift region, as shown in Figure 4.6. The disadvantage of this method is the unavoidable dead time of the pulsed reset. The second reset mechanism shown in Figure 4.8 is a continuous reset using a p-MOS transistor. A continuous reset can be an additional noise source.

In both designed SDD structures there are no integrated capacitors. However, the parasitic capacitor between the detector anode and the transistor guard ring can act as a feedback capacitor.

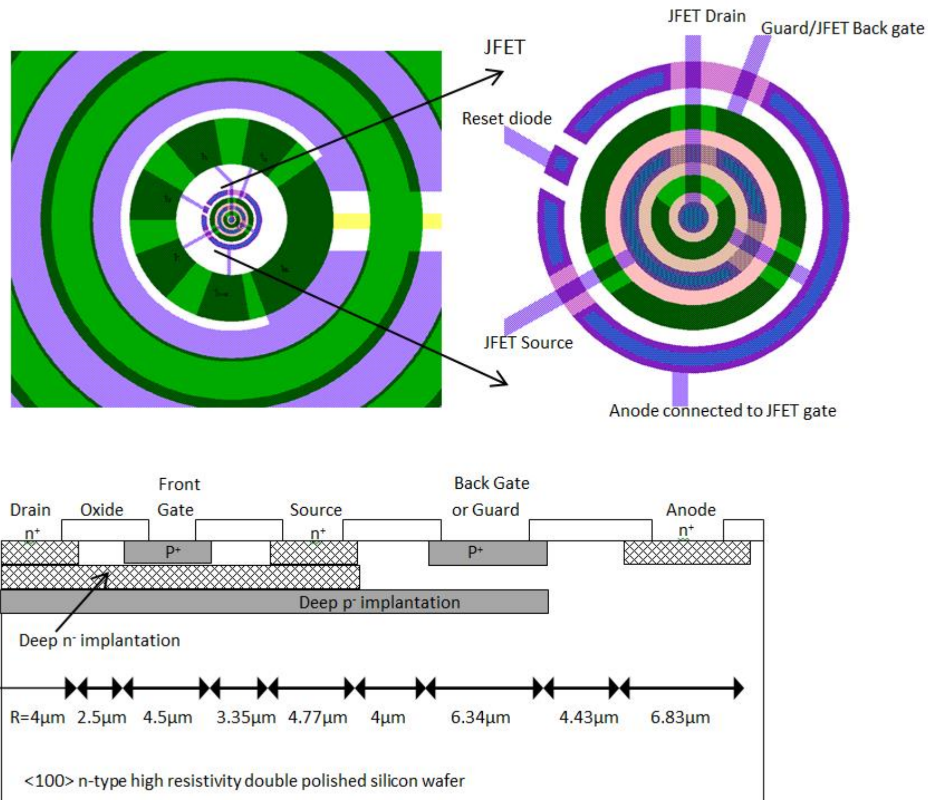


Figure 4.6: Designed layout and cross section view of an on-chip JFET with reset diode.

Figure 4.7 shows optical images of the structure with the on-chip JFET and reset diode. The reset diode is marked by a circle. Drift rings and the boron layer voltage divider are visible in these optical microscopic images.

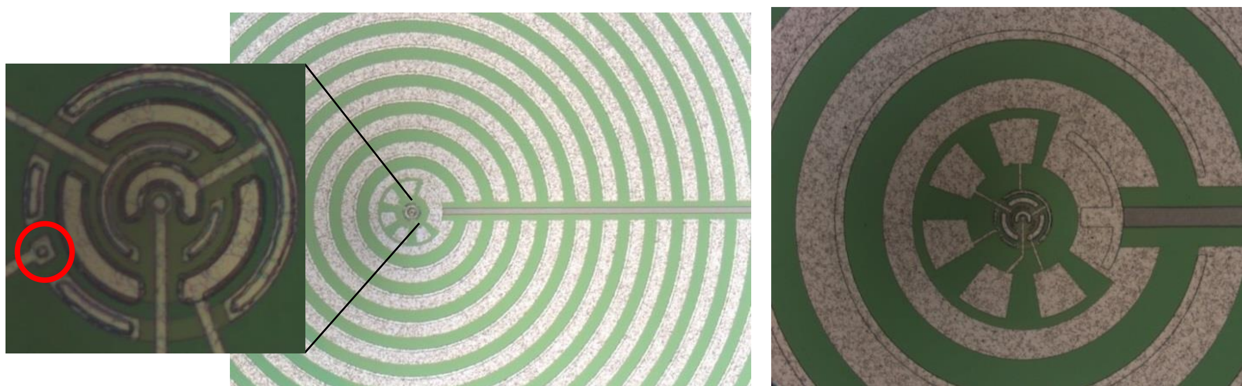


Figure 4.7: Optical images of the first SDD structure designed with an on-chip JFET and reset diode.

The second structure uses a pMOS transistor as the reset device, which was explained in Figure 4.5. This pMOS transistor works at the subthreshold region. A pMOS drain is connected to the JFET gate and the source/gate are connected to the output contact pads as shown in the layout and cross section of Figure 4.8.

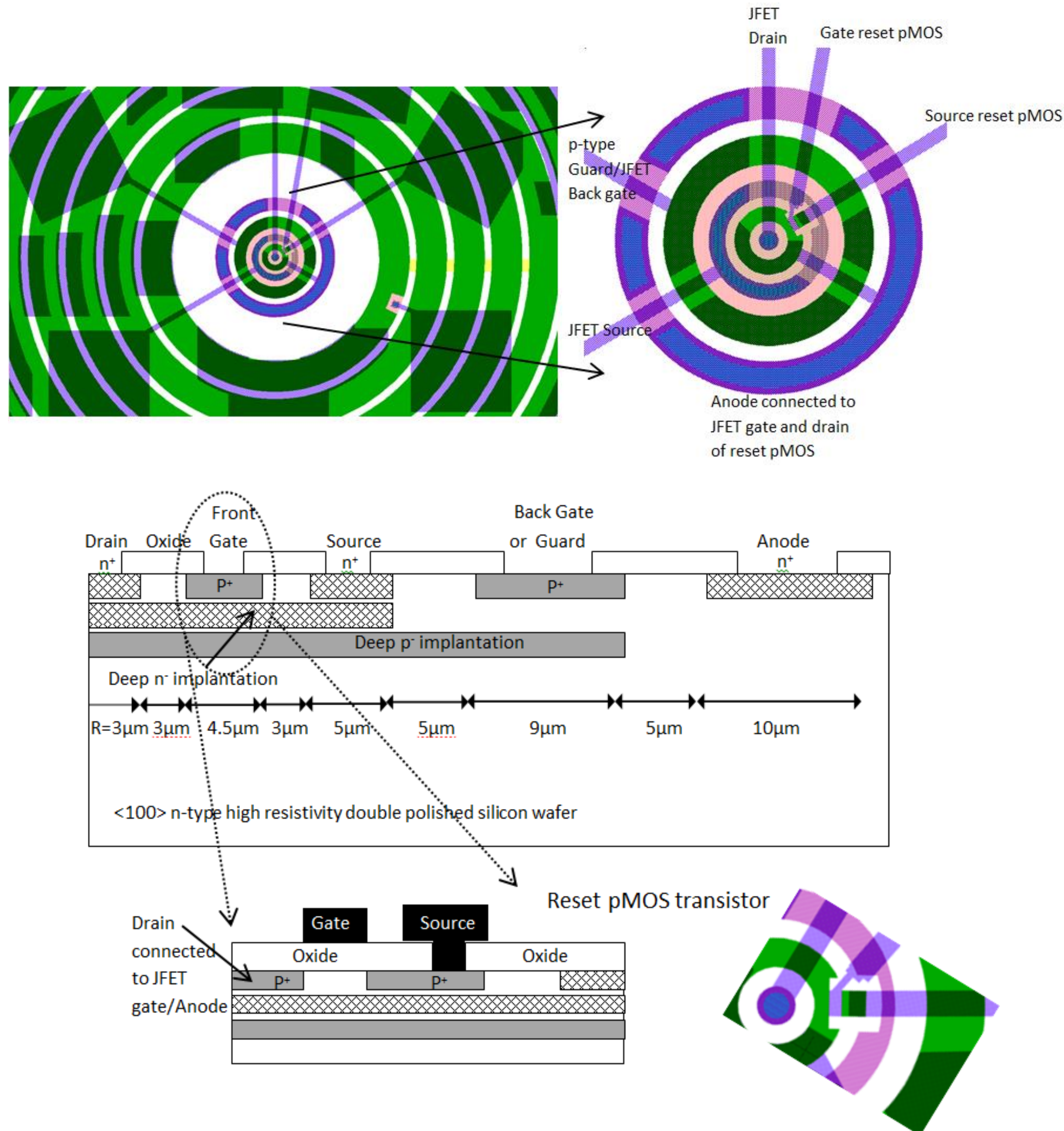


Figure 4.8: Designed layout and cross section view of the on-chip JFET with reset diode.

Figure 4.9 shows optical microscopic images taken from the SDD structure with continuous pMOS reset. Drift rings, a boron layer resistor as the voltage divider, the on-chip JFET and anode are visible in these images.

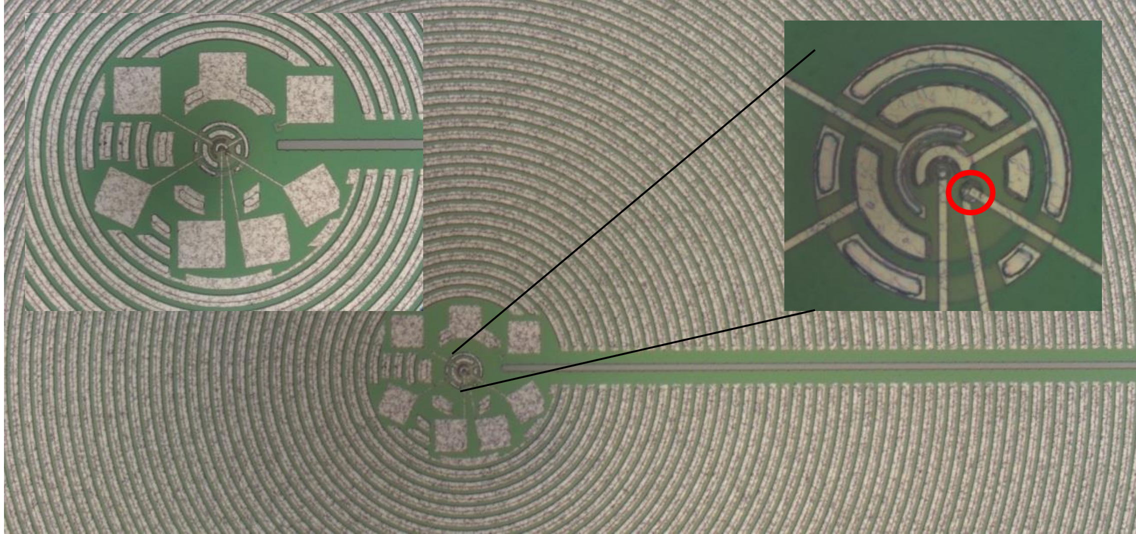


Figure 4.9: Optical images of the second SDD structure designed with an on-chip JFET and p-MOS reset device.

In order to see the influence of the JFET channel depth on the performance of the JFET we used the implantation parameters shown in Table 4.1. All implantation steps were performed through 30nm oxide. The expected depth for specific implantation energies are written in this table. Furthermore, the required resist thickness as a mask for implantation are reported in the table as well.

Table 4.1: Parameters of the ion implantations used for SDD fabrication flows: Implantation energies were performed through 30nm oxide.

		Dopant	Energy (KeV)	Dose (cm^{-2})	R_p (µm)	ΔR_p (µm)	Resist thickness	Boron layer
Source/ Drain (n^+)	Flowchart 1	P^+	100	1×10^{15}	0.1	0.05	3µm	-
	Flowchart 2	P^+ + As^+	500 100	1.4×10^{12} 5×10^{14}	0.65 0.05	0.15 0.02		
Gate (p^+)	Flowchart 1	B^+	30	5×10^{14}	0.1	0.04	3µm	yes
	Flowchart 2		20		0.05	0.03		
Deep n^-	Flowchart 1	P^+	220	3.5×10^{12}	0.3	0.09	3µm	-
	Flowchart 2		500	8.5×10^{11}	0.65	0.15		
Deep p^-	Flowchart 1	B^+	250	1×10^{12}	0.6	0.09	6µm	-
	Flowchart 2		500		0.96	0.1		

4.2 Multi-Guard Ring Structures for SDDs

The breakdown voltage is an important parameter in designing X-ray detectors such as silicon drift detectors (SDDs). In SDDs the complete thickness of the wafer has to be depleted to enable the detection of different energies of X-rays. A high voltage is required to have a fully depleted region while keeping the leakage current low. Multi-guard ring structures are designed to meet both a low leakage current and a high breakdown voltage using deposited PureB layers. To obtain a low leakage current, PureB layers were used. In multi-guard ring structures, parameters such as gap width, number of the rings and overlap of the metal field plate with the oxide have been designed to obtain higher breakdown voltage. Parameters such as gap size, oxide charge, bulk doping concentration and field plate design have an influence on the potential distribution of the guard rings. The designed structure works up to the limit of the measurement systems (1100V) with very low leakage current in the range of 1.5-3nA/cm^2 for the detector.

4.2.1 Introduction

Breakdown voltage determines the maximum voltage that can be applied to the p-n junction diode without any exponential (or rapid) increase in the current [101]. Typically a reverse biased p-n junction has a very small current which flows through the junction. When the reverse voltage is increased the current dramatically increases due to the dramatic reduction in dynamic resistance of the diode. There are two main mechanisms for reverse breakdown in a p-n junction: Zener and avalanche breakdown [101].

Zener breakdown is caused by quantum mechanical tunneling of the charge carriers through the junction. It occurs in junctions where both sides are heavily doped. Since the band gap decreases with increasing temperature, tunneling can occur at lower voltages leading to a negative temperature coefficient [102].

Avalanche breakdown is due to accelerated charge carriers in the high electric field at the junction hitting other charge carriers (impact ionization), which leads to carrier multiplication. Avalanche breakdown occurs in lightly doped p-n junctions

where the depletion region is comparatively long. The doping density controls the breakdown voltage. The breakdown voltage increases with rising temperature. This behavior is the reverse of tunneling diodes, which allows the two processes to be distinguished this way [102,103].

The above-mentioned breakdown mechanisms are not destructive. However, the heat generated by the large current flowing can cause damage to the crystal lattice. Therefore either the current must be limited and/or adequate heat sinking must be supplied [103,104].

Any defects such as grain boundaries in the material [105] or fixed charges in the oxide or oxide-silicon interface [106] can locally influence the breakdown voltages [107,108].
It should be mentioned that the value of the breakdown voltage diminishes in the edge of the structures. Different edge-termination methods such as field plate extensions [109], junction termination extensions (JTE) [110], high-resistivity implanted layers [111], and floating guard ring structures [112,113] have been used to minimize this effect and to increase the breakdown voltage.

One of the devices where breakdown voltage plays an important role is the silicon drift detector where a relatively high voltage is applied to ensure depletion over the full silicon thickness and drift of the electrons toward the anode with sufficient speed. A typical mechanism for breakdown in SDD detectors is avalanche breakdown. To improve the breakdown voltage of the detector and to keep low leakage currents, guard rings must be designed such that they provide a uniform potential distribution over the silicon surface, resulting in a higher breakdown voltage. In drift detectors, drift rings and entrance window are surrounded by guard rings at the minimum distance to reduce surface leakage current and electronic noise [114]. Furthermore, edge termination shields the sensitive region of the detector from the dicing line, resulting into a lower leakage current. This edge termination structure ensures that the depletion region of the detector does not reach the defective region of the dicing line.

The p^+ guard ring on the n-type substrate can be biased or can be kept floating. However, a single guard ring structure is sensitive to the surface charge density at

the oxide-semiconductor interface, which is dependent on the fabrication process and environmental conditions to which the detector is exposed. P^+ strips can be fabricated with deep diffusion of impurities [113], implantation, doped poly-silicon deposition, or it can be made from metal to semiconductor junctions such as the Schottky diode [114]. Moreover, between the last drift ring and guard ring structure there is an insulating ring [115].

To improve the breakdown voltage, multi-guard ring structures [116,117] can be used. The external voltage is applied to two ends of the multi-guard rings. The highest negative voltage is close to the active area of the detector. Voltage distribution over intermediate rings can be obtained by a resistor network or by a punch-through mechanism in between two p+ strips and the n-substrate [117,118]. The voltage in each ring of the guard structure is dependent on substrate doping, the gaps between the rings, oxide charges, bias voltage and field plates design [119]. Designing guard rings using field plates can offer a higher breakdown voltage. In a field plate design, a kind of MOS capacitor structure is used where the gate-to-drain or gate-to-source contacts are shorted. Obtaining an optimal field plate depends on wafer quality, passivation layer material and thickness, positive oxide charges, implantation depth and fabrication process [120,121]. Field extension causes the voltage over the oxide to be constant; therefore during irradiation there will be no drift of the guard rings voltages [117].

In this thesis, design of multi-guard ring structures with a field plate extension are optimized for boron layer technology and used as p^+ guard rings to obtain the highest breakdown voltage. Electrical measurements show one of the structures demonstrates a maximum breakdown voltage with low leakage current.

4.2.2 Multi-Guard Ring Design

Our silicon drift detector uses p+ drift rings and voltage divider layers fabricated in boron layer technology [122]. To compensate the existing high field at the edge of the p^+ rings, a low doped p-layer was added by implantation around the p^+ area. In order to improve the breakdown voltage of the detectors, multi-guard structures were used. Multi-guard ring structures surround the active area of the

SDD. They consist of a conventional large p-type guard, a series of intermediate concentric circular p-type guard rings (with different pitches and widths and metal overlap of the field plate) and a large n-type guard close to the scribing line. Details of multi-guard structures aimed at optimizing the layout of the floating rings can be found in the literature [117, 119,121]. The width of the large p-type guard ring should be at least equal to one quarter of the wafer thickness in order to shift the saddle point from the surface to depth to prevent any loss of charge carriers generated by radiation near the surface [115]. For the optimum spacing between the large guard and first p+ guard ring, the following equation can be used [123]:

$$\frac{W_S}{W_C} = \sqrt{\frac{BV_{FFR}}{BV_{PP}}} - \sqrt{\frac{BV_{FFR}}{BV_{PP}} - \frac{BV_C}{BV_{PP}}} \tag{4.8}$$

where W_S is the optimum distance from the edge of the main junction, W_C is the depletion width at breakdown for the main junction, BV_{FFR} is the reverse voltage applied to the main junction under the breakdown conditions, BV_C is the potential of the floating guard ring under the breakdown condition, and BV_{PP} is the breakdown voltage for the main junction.

Since an optimal guard structure is dependent on the fabrication process, materials and many other parameters, it is very difficult to drive an analytical formula for breakdown voltage. Therefore we performed a DOE (design of experiment) for the field plate structures.

Figure 4.10 illustrates a snapshot of the layout for the detector and the corresponding cross-section. In this picture the active region (entrance window) and the guard rings are visible. In the cross-sectional view, metal overlap or field plates are visible.

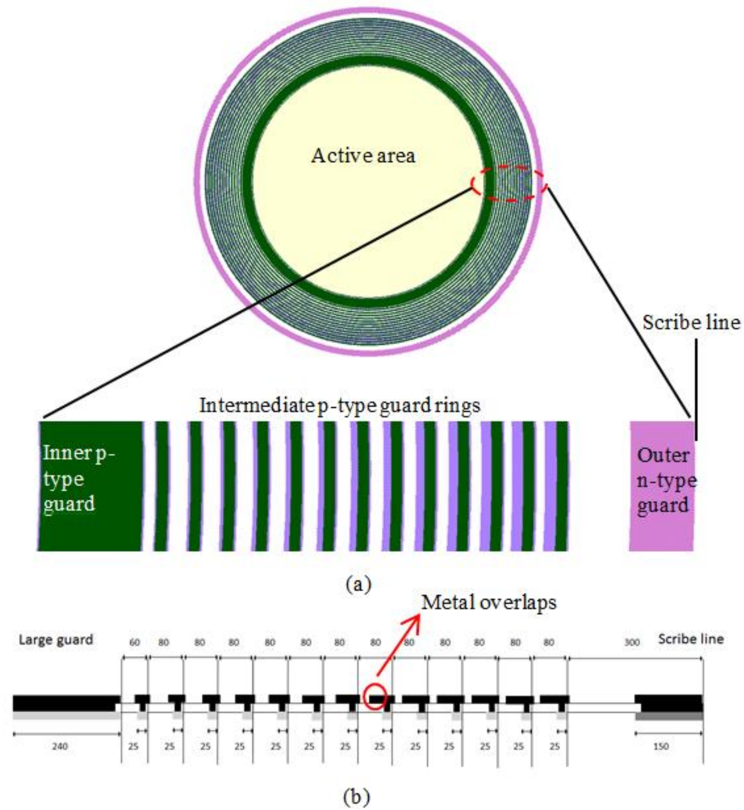


Figure 4.10: Designed layout of a detector consisting of an active region and surrounding guard rings (a), and cross-section of structure number 9 (b).

A multi-guard ring structure consists of a large inner p-type guard, several intermediate p-type guard rings and finally an outer n-type guard ring. The widths of inner and outer guard rings are fixed to 240μm and 150μm for all DOE, respectively. For the intermediate guard rings we performed a DOE to find the optimum structure for higher breakdown voltage. Guard rings have different pitches, widths and field plate overlap as described in Table 4.2. The last column shows the total distance between the active area and the scribe line for each structure including the main guard rings. In structure 1, the metal on the p+ rings does not have any overlap with oxide. In other structures the metal line is either inward or outward or it has symmetrical overlap with oxide to reduce the surface leakage current and improve the breakdown voltage.

Table 4.2: Specifications of the designed structures for intermediate p-type guard rings.

Structure	Number of rings (p-type)	Width of rings (µm)	Pitches (µm)	Field plate overlap (µm)			Distance between active area and scribe line (µm)
				Inward	Outward	Symmetrical	
1	12	20-35	40-70	-	-	-	1140
2	12	20-35	40-70	10-25	-	-	1140
3	12	20-35	40-70	-	10-25	-	1140
4	12	20-35	40-70	-	-	5	1140
5	6	20-35	80-140	40	-	-	1140
6	13	20-55	70-80	-	-	5	1570
7	12	40-55	80-110	-	-	5	1620
8	12	30-45	60-90	-	-	5	1380
9	13	25	60-80	5-30	-	-	1560
10	Spiral design						

In the cross-sectional view of Figure 4.10, structure 9 is displayed, which consists of 13 intermediate p^+ rings with an inward field plate.

4.2.3 Fabrication Process

In the next chapter the fabrication process will be discussed in detail. In summary, Figure 4.11 displays a flow diagram of the fabrication process.

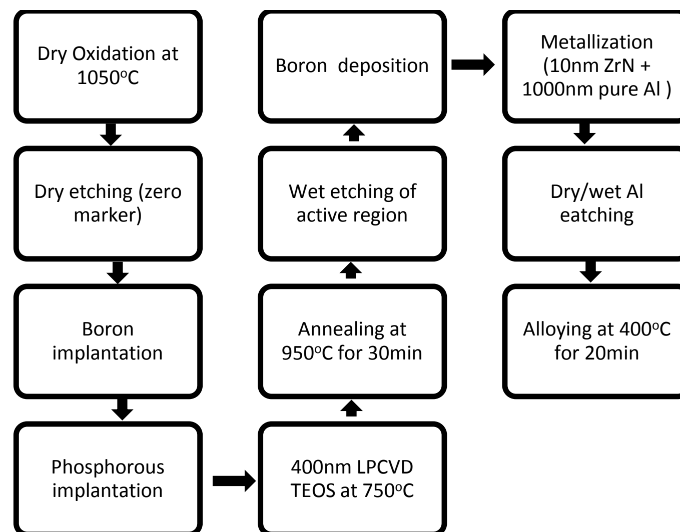


Figure 4.11: Flow diagram of the fabrication process.

SEM images of the fabricated devices are shown in Figures 4.12, 4.13 and 4.14. In the layout we had several p-n and SDD devices as test structures to study the different guard ring designs. Figure 4.12 shows two SDD devices with a single n-type guard ring with 6µm and 60µm spacing between the last drift ring and the single guard.

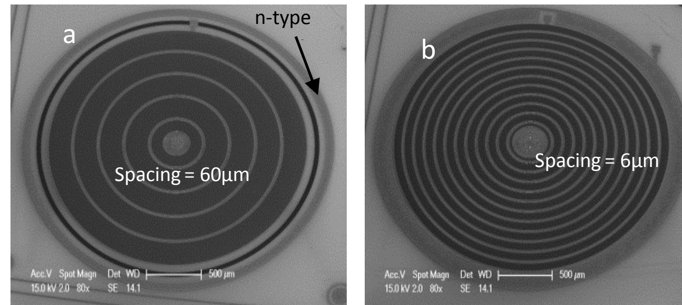


Figure 4.12: SEM images of single guard ring structures with a) 60µm and b) 6µm spacing between the last drift ring and n-type guard ring.

Figure 4.13 demonstrates two different guard ring structures where the connection between the guard rings is maintained by a resistor network fabricated in the boron layer [122]. In the spiral structure a large p-type guard is connected to the intermediate p-type rings with the boron layer as a resistor (Figure 4.13a). In Figure 4.13b, intermediate p-type guard rings are connected to the large p-type guard by the resistor network as a biasing circuit.

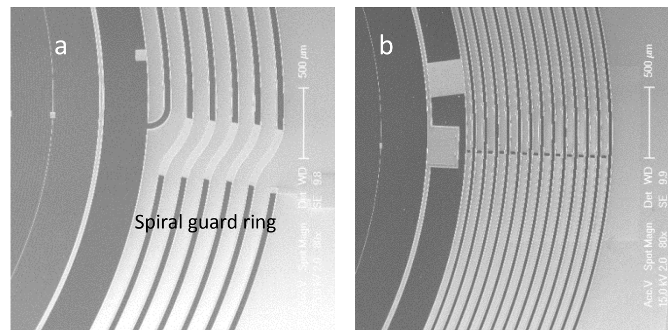


Figure 4.13: SEM images of the resistor connected and biased guard rings with a) spiral guard ring and b) multi-guard ring structures.

Punch-through biased multi-guard ring structures with different field plate overlap are shown in Figure 4.14. They all have similar large guard rings but different number of rings, width and field plate overlap. The exposed boron layer, large guard ring, intermediate p^+ guards and n^+ last ring are visible in these images.

All reported SEM images are taken from the device side where the anode is in the center of the SDD. The entrance window and all p^+ regions are formed by a deposited nm-thin boron layer [85,122,124].

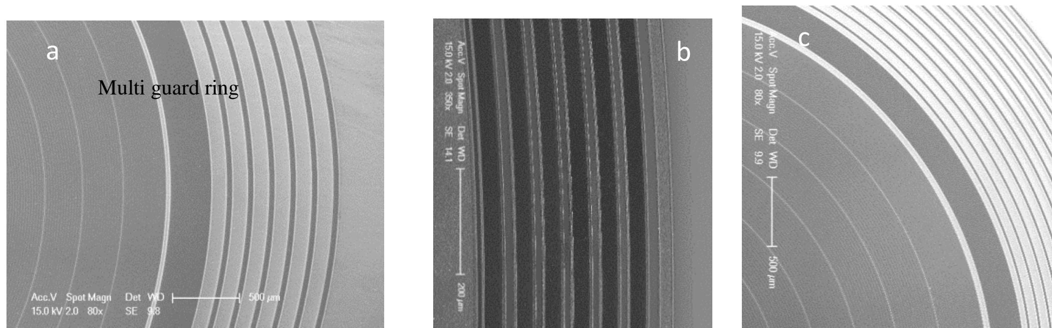


Figure 4.14: SEM images of different multi-guard ring structures with a different number of rings, width and field plate extensions. SEM image of structure number 9 is shown in c.

The quality of the silicon wafers has a significant influence on finding the optimum structure as a guard ring for the detectors. Furthermore, since silicon drift detectors work in the fully depleted condition, the doping uniformity of the wafer over the whole thickness is extremely important. In Chapter 5 the results of the doping profile measurement is reported.

4.2.4 Identifying the Breakdown Mechanism

In order to determine the type of breakdown, we measured the devices at different temperatures. As displayed in Figure 4.15, the breakdown voltage increases from 61V at -40°C to 65V at 50°C indicating a positive temperature coefficient for the breakdown voltage. The calculated value of $\partial Vbr/\partial T$ is equal to 0.044 V/K. This suggests that the breakdown mechanism is an avalanche type.

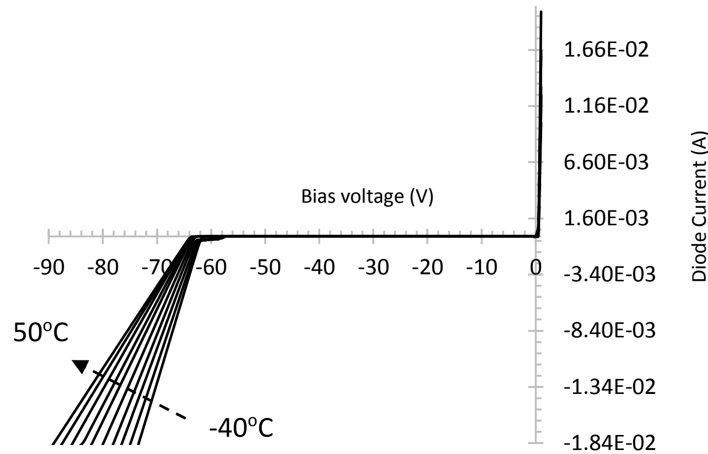


Figure 4.15: Temperature dependency of the breakdown voltage. The temperature coefficient $\partial Vbr/\partial T$ is 0.044 V/K. Positive coefficient of the breakdown voltage indicates an avalanche breakdown.

4.2.5 Breakdown Voltage Measurement in a Bulk PIN Diode

A bulk p-n diode is one type of X-ray detector where the full thickness of the silicon wafer is depleted to detect incoming radiation. As shown in the schematic of Figure 4.16 it has a p^+ region as the entrance window and a guard ring surrounding this area. Our first designed p-n test structure consists of a boron layer doped p^+ region as the entrance window with only p^- guard rings , metal contact on top and n^+ implanted contact at the bottom. The dc I-V measurement showed no breakdown voltage until the limitation of the measurement system (200V) was reached. The measured leakage current at -100V reverse voltage was 37.5nA/cm^2. One of the reasons for this higher leakage current can be a surface leakage current under the passivation layer. Using extra guard rings and the metal field plate, this leakage current can be reduced. To study this effect we designed a second type of device with an n^+ floating guard ring and different gaps with respect to p^- guard rings as illustrated in Figure 4.16.

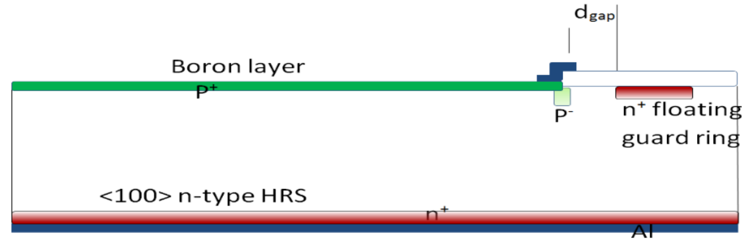


Figure 4.16: Schematic diagram of the PIN diode with single guard ring.

It is well known that adding an n^+ guard ring around the p-region reduces the leakage current significantly and makes segmentation of diodes possible for multi-segment types of detectors [60]. The function of the n+ guard ring is to shield any existing positive charges in the oxide and prevent extension of the depletion region toward the dicing line which causes leakage current to drop significantly. Table 4.3 summarizes the measured breakdown voltages and leakage current for different gaps.

Table 4.3: Impact of adding an n^+ guard on leakage current and breakdown voltage of the p-n diode.

Gap between n^+ and p^- (d_{gap})	Leakage current	Measured breakdown voltage
No n^+ guard	37.5nA/cm² at 200V	>200V
6μm	3.5nA/cm² at 67V	67V
38μm	17.4nA/cm² at 200V	>200V

It can be seen that adding an n+ guard ring reduces the leakage current, although for a 6μm gap the breakdown voltage is too low (67V). As mentioned above, wafer doping uniformity plays an important role in the breakdown voltage of devices. Figure 4.17 shows I-V plots of several measurements of p-n diodes with a 6μm gap between the p^+ ring and n^+ floating guard for the devices fabricated on the front side, with an average N_D equal to 10^{12} 1/cm³, and backside of the wafer with an average N_D equal to 10^{11} 1/cm³. It can be seen that p-n diodes made on the front side all show relatively a higher breakdown voltage (around 75V) compared with devices made on the backside of the wafer (around 60V). These measurements were repeated for several dies and wafers and they all had similar behavior.

Furthermore, the breakdown voltage of a p-n diode which has only an n^+ floating guard ring can be calculated with the following formula [118,122]:

$$V_{BD} = \varepsilon_C W_{gap} - \frac{1}{2}\frac{qN_D W_{gap}^2}{\varepsilon_s} \quad (4.9)$$

where W_{gap} is the gap between the p^+ and n^+ implants, q is the electron charge, N_D is the substrate donor density, ε_S is the silicon dielectric constant and ε_C is the critical field given by the following equation [118,122]:

$$\varepsilon_C = 4010 N_D^{1/8} \quad (4.10)$$

Calculations for 6μm spacing show breakdown voltages equal to 76V and 57V, for the front side and backside, respectively, which are in good agreement with the measurements.

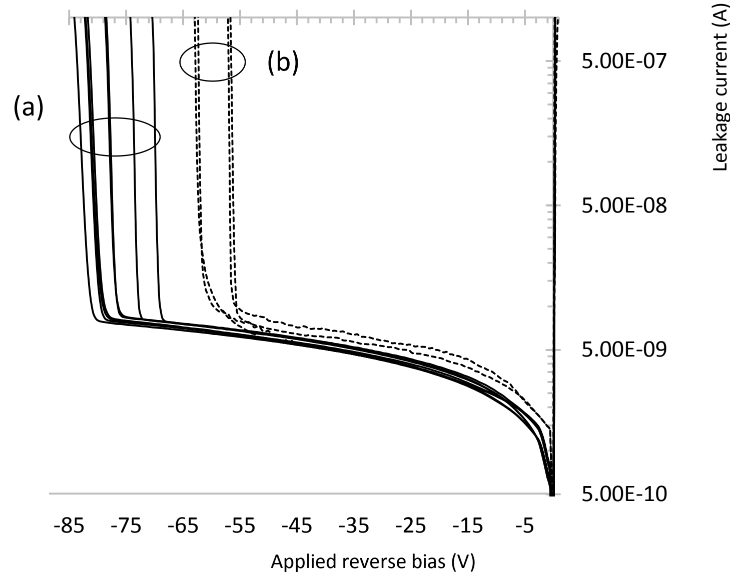


Figure 4.17: Measured breakdown voltage for several p-n diodes with an extra n+ guard ring with a 6μm gap fabricated in a) the front side b) back side.

For some low voltage applications such as low energy electron detectors and EUV detectors, this gap (6μm) sufficiently reduces the leakage current [60,63]. However, for high voltage applications such as X-ray detectors, the breakdown voltage has to be much higher while at the same time maintaining a low leakage current. For this kind of application the gap has to be increased. In the design with a 38μm gap, the leakage current was 17.4nA/cm² and breakdown was not observed until the system limitation of 200V was reached. The conclusion is that

for specific detector applications, based on the maximum feasible leakage current and the minimum breakdown voltage, the distance between the n^+ floating guard and p^+ region can be optimized.

4.2.6 Electrical Measurements of Multi-Guard Ring Structures

Another way of designing the guard rings is by adding p^+ strips in between the p^+ region and n^+ guard ring so that the potential distribution can be smoothly lowered from high voltage to ground at the edge of the detector. Intermediate guard rings are biased by the punch-through mechanism. All p^+ guard rings and the entrance window were realized with boron layer technology which offers few nanometer shallow p-n junctions.

Since in multi-guard ring structures the breakdown voltage is higher than the limitation of the measurement tool, we used the Keithley measurement system which is able to operate up to 1100V.

Figure 4.18 illustrates the measured breakdown voltages on different structures (shown in Table 4.2) on two wafers. The measured values are the average over several samples from each structure.

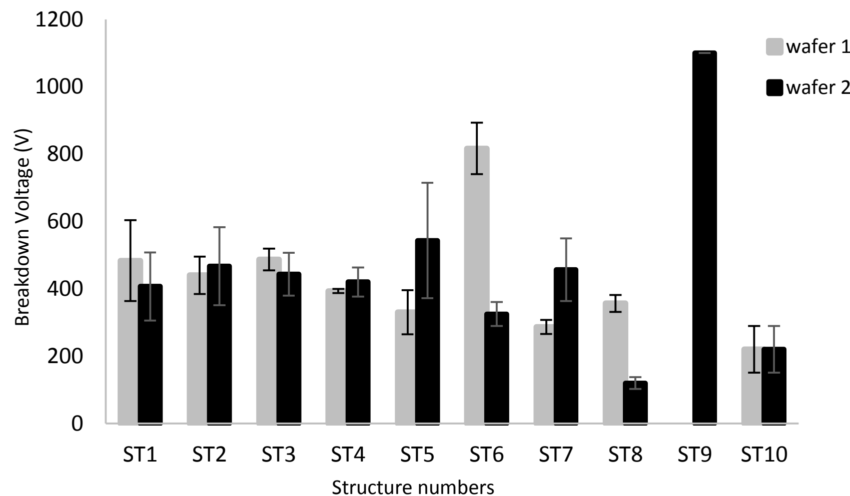


Figure 4.18: Measured average and STDEV of breakdown voltage on two wafers over 10 different structures.

Among 10 different designs, structure number 9 shows a breakdown voltage higher than 1100V, which was the limitation of the measurement system. In this structure the width of the guard rings was 25µm, the first gap (between the large guard and first intermediate guard ring) was 35µm, and the pitch was 80µm for the rest of the rings, with an inward field plate extending 5-30µm. Other structures show a roughly 400V breakdown voltage.

Since the surface leakage is blocked by the guard structures and scribe line, the leakage current is not collected by the main diode. Therefore the total leakage current of the main p-n diode is reduced significantly. The leakage current varied between 1.5-3nA/cm^2 on different structures.
Figure 4.19 shows measurement results of the breakdown voltage on structures with gaps (between the large guard and first ring of the multi-guard) varying from 20-60µm. According to this measurement, a roughly 40µm gap is an optimal value for the distance between the large guard and first ring of the multi-guard structure. In structure 9 this gap was 35µm, which is consistent with the results of Figure 4.19.

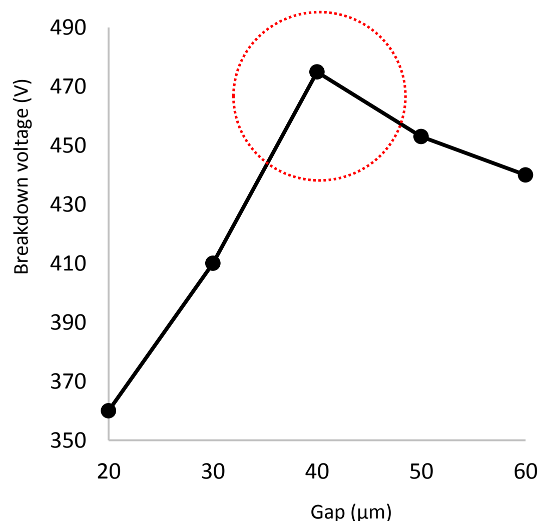


Figure 4.19: Breakdown voltage as a function of the gap between the large guard and first ring of the multi-guard structure. The 'sweet spot' is highlighted by a circle.

The overlap value and direction of the field plate have significant influence on the breakdown voltage as well. Figure 4.20 displays the extracted breakdown voltage from the measurement for the inward (where the extension is positioned in the large guard direction) and outward design. It can be seen that a field plate in the inward direction offers a higher breakdown voltage because of charge shielding.

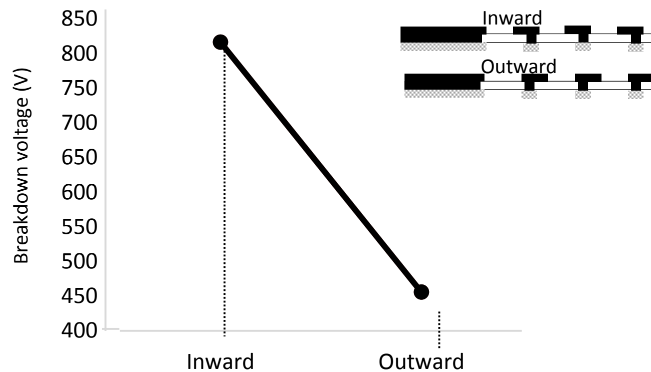


Figure 4.20: Breakdown voltage in structures with inward and outward field plate design.

In the multi-guard ring design the voltage drop is reduced smoothly from a negative high voltage near the large guard to ground near the last ring. Therefore any generated electrons under the guard area (p^+ strips) is drifted toward the outer n+ guard ring. These electrons can be collected by individual ground which is separated from the main detector ground to reduce any unwanted noise coupling. Figure 4.21a shows the measured voltage drop on intermediate p-type guard rings when applying -100V to the large guard. It can be observed that the potential drops almost exponentially around 0V in guard number 4. This measurement suggests that having three guard rings is sufficient to maintain the function of the multi-guard ring structure when applying 100V to the large guard. It is expected that more guard rings will be needed when applying higher voltages because of depletion region expansion. With re-plotting the measured values versus the detector radius, Figure 4.21b is obtained where a large guard and intermediate guard rings radius is shown. The total length of the large guard and the first three intermediate guards is 460µm.

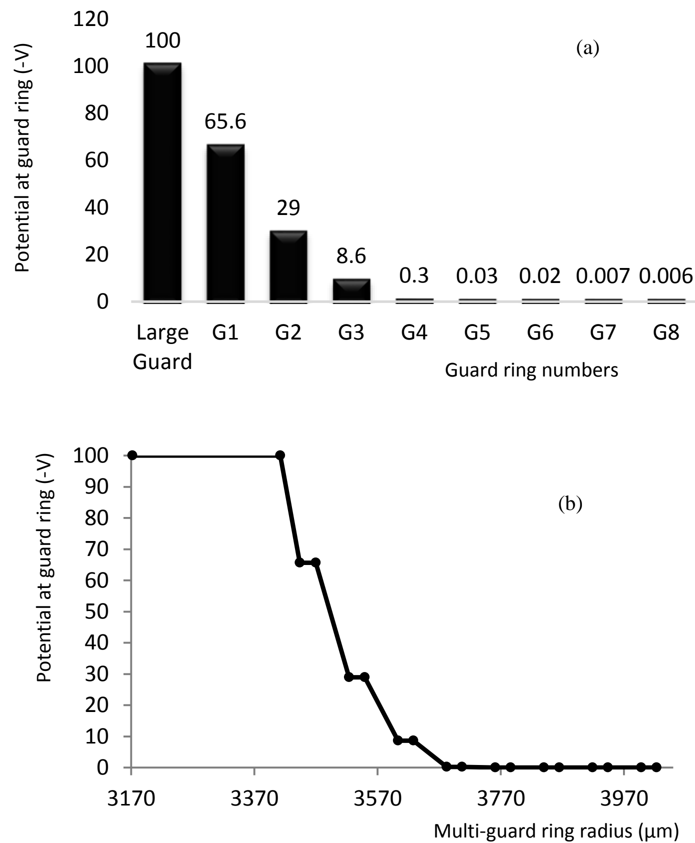


Figure 4.21: a) Dropped voltage on rings of the multi-guard ring structure with voltage applied to the large guard; b) dropped voltage measured as a function of the device radius.

4.3 Conclusions

Integrating an on-chip amplifier can improve the performance of SDDs in terms of noise and resolution. To select the type of transistor for the SDD, a JFET is preferred because of noise considerations. Bipolar transistors have higher shot noise while CMOS transistors have a higher 1/f noise component. In designing the JFET there is a trade-off between obtaining minimum noise and minimum capacitance while keeping the transconductance (g_m) as high as possible. The gate capacitance plays an important role in this trade-off. Since mobility of an nFET is higher it offers a higher cut-off frequency than a pFET. For optimum SDD resolution, the input capacitance of the JFET is equal to the capacitance of the detector. In a SDD, typically the JFET is placed inside the anode which is isolated

by a p-type region from the anode. Two different JFET transistors designed with a 4.5µm gate length together with reset mechanisms (MOS and reset diode) were discussed in detail. The electrical performance of the fabricated JFETs is discussed in Chapter 5.

Electrical measurements showed that the positive coefficient of the breakdown voltage corresponds to avalanche breakdown for the fabricated devices. Using a single n^+ guard ring for the p-n diode detector could significantly lower the leakage current. However, the breakdown voltage was also reduced in the best case to 85V. To maintain the lower leakage current and to obtain a higher breakdown voltage a multi-guard ring structure was used. Among 9 different multi-guard ring designs, one of them works up to the limit of the measurement systems (1100V) with very low leakage current in the range of 1.5-3nA/cm^2 for the detector. In this structure the width of the guard rings was 25µm, the first gap (between the large guard and first intermediate guard ring) was 35µm, and the pitch was 80µm for the rest of the rings, with an inward field plate extension of 5-30µm. Other structures show a breakdown voltage of around 400V. According to the measurements of different designed guard ring structures, a roughly 40µm gap is an optimal value for the distance between the large guard and first ring of the multi-guard structure. Moreover, it was found that a field plate in the inward direction offers a higher breakdown voltage because of charge shielding. The measured voltage drop over the guard rings showed an exponential reduction of the negative voltage and ground potential in 4th guard ring.

Chapter 5

Fabrication and Characterization of PureB-SDDs

5.1 Introduction

In this chapter, a fabrication flowchart of a conventional SDD along with single and double boron layer SDDs with and without on-chip electronics, will be reported. Then quality of wafer will be characterized by doping profile and gated diode test structures. The influence of the passivation layer, annealing, field plate and boron layer on the leakage current of fabricated SDDs will be investigated in detail. Moreover, a novel interposer which enables measuring of "double-sided contact designs" in conventional single-sided probe stations will be introduced.

5.2 Fabrication Process Flow of PureB-SDDs

5.2.1 Single PureB-SDD Process Flow

The PureB-SDD process is a double-sided process for the fabrication of SDDs aiming for a thin entrance window SDD with a continuous p-n junction on both sides of the SDD with an acceptable level of leakage current [this thesis]. The major fabrication steps are listed in processing order in Table 5.1. This process flow consists of 14 mask steps. The process flow with on-chip readout electronics, i.e. the JFET amplifier, MOS injector, reset diode and MOSFET will be explained later.

As can be seen from this table, the process flow starts with dry oxidation followed by the guard ring and anode implantations by boron and phosphorous dopants, respectively. The next step is TEOS oxide deposition and annealing. Then the

oxide layer is etched to open the regions for boron deposition to create p^+ regions. Boron deposition is selective, which means it deposits only on silicon. Aluminum metallization on both sides is the next step. In order to etch Al and expose the boron layer, a combination of dry (keeping the dimensions the same as the design) and wet etching in diluted HF (to land on the boron layer without damaging this layer) was performed. Alloying in forming gas is the last step to create ohmic contact of doped silicon with Al.

All the mentioned processing steps are done on both sides of the wafers, which added complexities to the process flow.

Table 5.1: PureB-SDD fabrication process flow.

Starting material	n-type FZ wafer, 500 μm, 2-10 kΩ.cm, (100)
Oxidation	D2, DryoxID, 200nm, 1050°C, 5hrs* D2, Gate oxide, 30nm, 850°C, 8hrs
P^+ implantation, front & back side	B^+, 180 keV, 10^{13} cm^{-2} * B^+, 40 keV, 10^{13} cm^{-2}
n^+ implantation, front & back side	P+, 180 keV, 5×10^{15} cm^{-2} * P+, 40 keV, 5×10^{15} cm^{-2}
TEOS deposition	LPCVD, E1, NEW TEOS 1, 400nm, 52 min
Annealing	C2, AnnealN1, 1000°C, 35 min
Window opening, front&back side	Plasma etching (Drytek 384T plasma etcher), plasmox + wet etching, BHF : 1 :7
Boron deposition, back side	BK 800 (4 min) - B 690C - 7m
Boron deposition, front side	BK 800 (4 min) - B 500C - 20m
Metallization, front&back side	10nm ZrN/Pure Al, 1075 nm, 350°C
Etching of Al, front & back side	Plasma etching (Omega), Al1m-350°C, system at 25°C
Etching of Al and exposing Boron layer, front side	Plasma etching (Omega), Al06 ts, system at 25°C + wet etching, HF 0.55%, 2 min
Alloying	C4, Alloy1

* Shows second option of the process.

Figure 5.1 shows two images of SDD wafers after oxide etching for boron layer deposition. The left image is with photoresist and the right image is after stripping the resist.

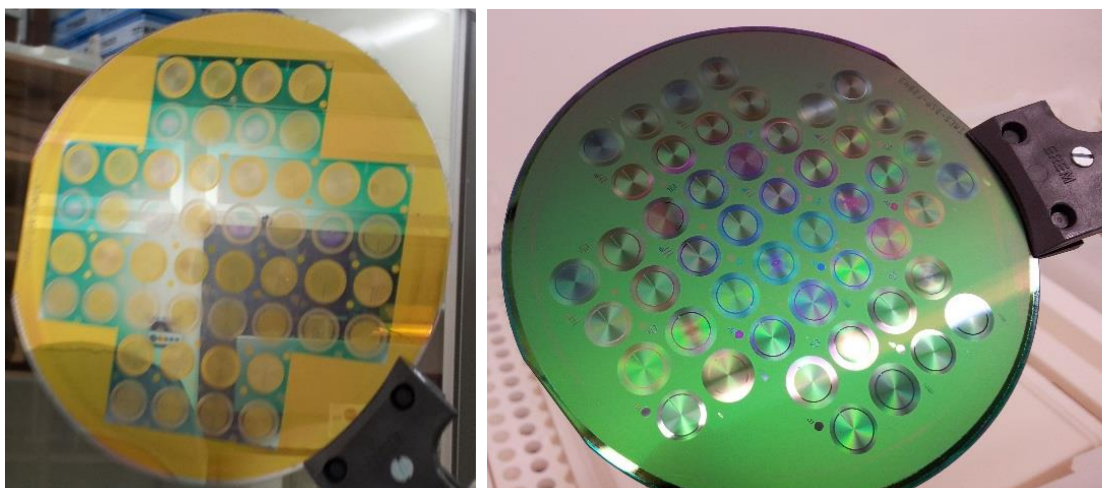


Figure 5.1: Oxide etching step on SDD wafers before resist strip (left) and after resist strip (right).

The first double-sided processing run showed some issues such as low breakdown in the SDD (around 57V) and a non-uniform electric field in the drift region of the continuous SDD. Wafers with 30nm oxide showed scratches caused by implantation, resulted in higher leakage current. A test run with 4 masks was done to determine the best design of the multi-guard ring structures, which was described in Chapter 4 in the breakdown section.

The other short loop test with 3 masks was done to define the best boron layer deposition conditions for a novel SDD designed with a continuous p-n junction on both sides and a uniform electric field in the drift region (Chapter 3).

Three test runs were done to expose the PureB layer on the entrance window of the SDDs. PureB layers with different deposition temperatures were tested (Chapter 2).

In order to quantify the high resistivity silicon wafer, p-n and gated diode test structures were measured to extract the doping profile, generation lifetime and surface generation velocity. These test structures together with process monitor test structures to monitor doping, sheet resistance of the boron layer, Al shorts and opens, were designed in SDD reticles.

5.2.2 Dual PureB-SDD Process Flow

The dual PureB-SDD process is a double-sided process developed for the fabrication of SDDs aiming for a thin entrance window SDD with a continuous p-n junction on both sides of the SDD with a uniform electric field in the drift region and with an acceptable level of leakage current [this thesis]. The major fabrication steps are listed in processing order in Table 5.2. This process was not optimized for the integration of readout electronics, but it was optimized for low energy X-ray detection.

Table 5.2: Dual PureB-SDD process flow.

Starting material	n-type FZ wafer, 500 μm, 2-10 kΩ.cm, (100)
Oxidation	D2, DryoxID, 220 nm, 1050°C, 5hrs 30 min
p+ implantation, front & back side	B^+, 180 keV, 10^{13} cm^{-2}
n+ implantation, back side	P+, 180 keV, 5×10^{15} cm^{-2}
n+ implantation, front side	P+, 500 keV, 1.4×10^{12} cm^{-2} + As+, 100 keV, 5×10^{14} cm^{-2}
TEOS deposition	LPCVD, E1, NEW TEOS 1, 400 nm, 50 min
Window opening, front side	wet etching, BHF, 8 min
Window opening, back side	wet etching, BHF, 8 min
Boron deposition, front side	BK 900 - B 690C - 8m Ann.(850°C, 10 min)
Boron deposition, back side	BK 700 (10min) - B 690C - 8m
Boron deposition, front side	wet etching, BHF, 10sec BK 700 - B 500C - 20m
Metallization, front & back side	Sputtering, ZrN, 10 nm Pure Al, 300 nm
Metallization, back side	Sputtering, Al/Si, 1475 nm, 350°C+RF
Window opening, front side	Plasma etching
Metallization, front side	Al/Si, 1475 nm, 350°C+RF
Etching of Al, front & back side	Plasma etching (Omega), 1.4μm AlSi+300 nm pureAl
Etching of Al and exposing Boron layer, front & back side	Plasma etching (Omega), 1.4μm AlSi+150 nm pureAl , + wet etching, HF 0.55%, 3 min
Alloying	C4, Alloy1

In this process flow two reticles (litho steps) are used before the boron deposition. Using the first litho step, oxide was etched in the drift region to leave a 30nm-thick oxide. In the second litho step, 30nm-thick oxide was etched from low sheet resistance areas. A low sheet resistance boron layer was deposited and followed by a 10sec BHF step to etch 30nm-thick oxide from the rest of the drift region. The previously deposited boron layer will not be attacked by this short BHF step.

At the end, a high sheet resistance boron layer was deposited. The double boron layer deposition process is summarized as follows:

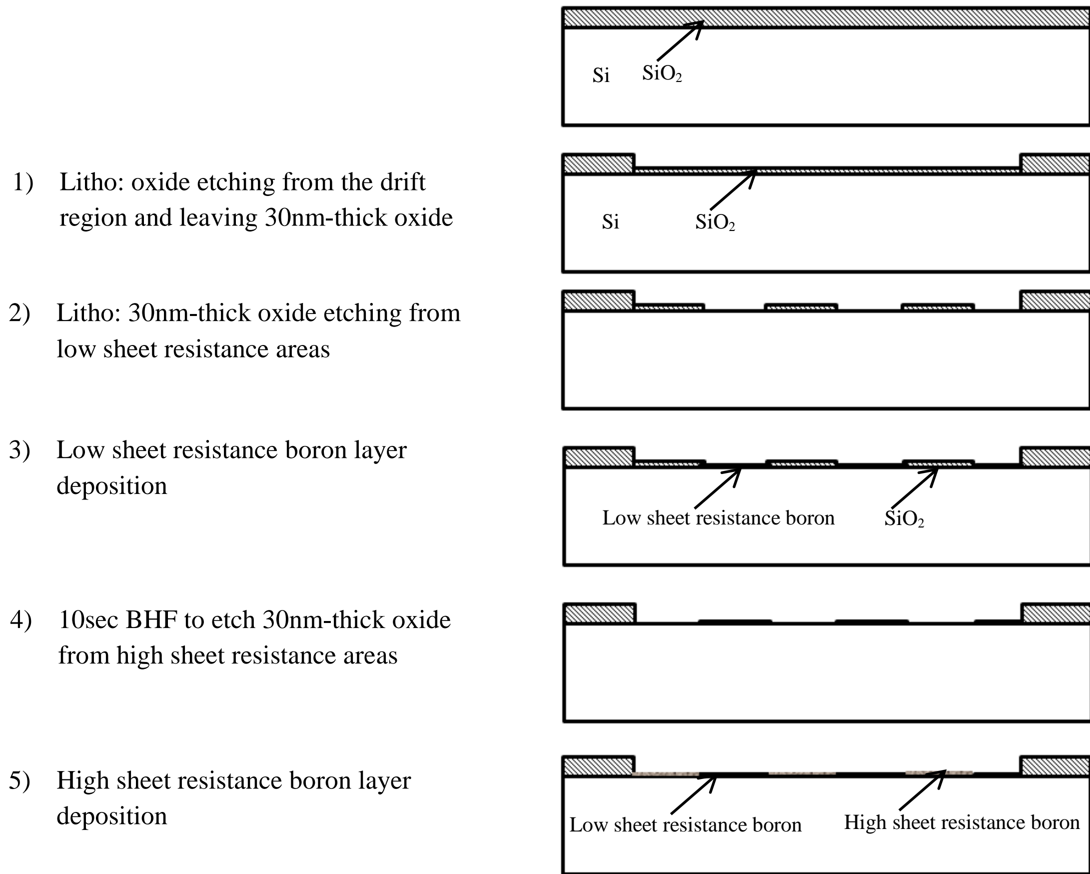


Figure 5.2 (left) shows a SEM image of the fabricated continuous SDD using one layer of boron with the anode in the center, the drift area with the boron layer and the guard rings. Figure 5.2 (right) shows the SEM images of the SDD using the dual boron layer. The insert illustrates both high and low sheet resistance layers.

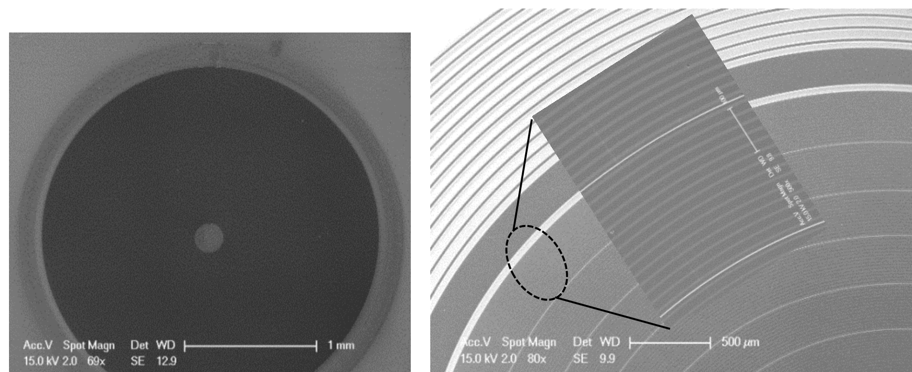


Figure 5.2: SEM images of fabricated continuous SDDs using one layer of boron (left) and using dual boron layer (right).

5.2.3 Dual PureB-SDD Process Flow with On-Chip Electronics

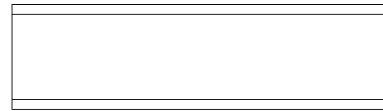
The process flow for PureB-SDD with on-chip electronics is a double-sided process developed for the fabrication of the SDDs aiming for thin entrance window SDDs with on-chip electronics with an acceptable level of leakage current [this thesis]. The process flow is similar to double boron process flow with extra implantation steps for the JFET and is listed as follows:

1. Starting material:

   n-type FZ wafer, 500 μm, 2-10 kΩ.cm,

   <100>

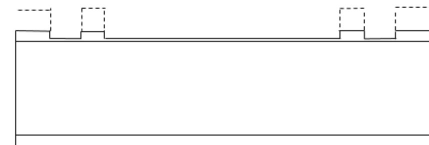
2. Dry oxidation, 220nm gate oxide
   at 1050°C, 5hrs 30 min, furnace D2



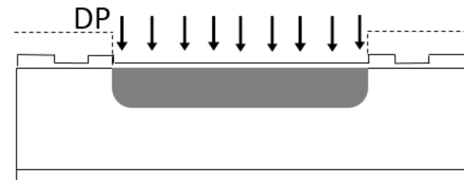
2a. Zero layer FS; Zero layer BS
(oxide wet etching: BHF 4min, 30sec;
Omega Si etching: LEON_1, at 20°C, 10-10-50 sec)

3. Wet etching of oxide back to 30nm on the FS,
   DP, DN and WN masks

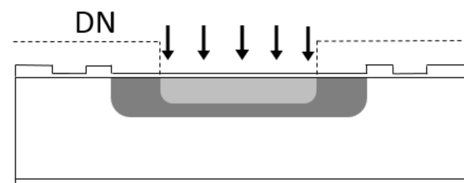
   Defines the JFET region



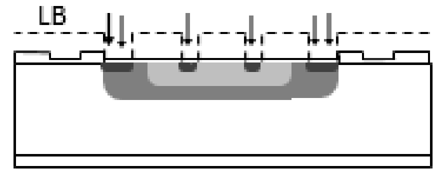
4. Boron deep-p implantation on the FS,
   DP mask, B^+, 250 keV, 1×10^{12} cm^{-2}



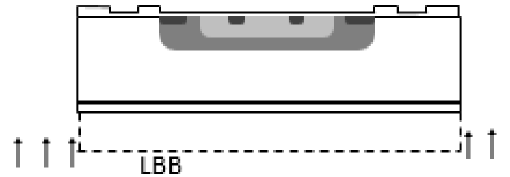
5. Phosphorous deep-n implantation on the FS,
   DN mask, Ph^+, 220keV, 3.5×10^{12} cm^{-2}



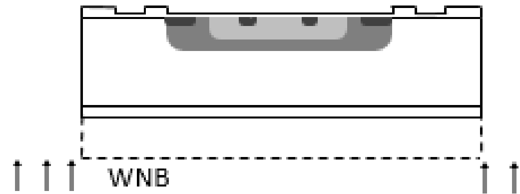
6. Boron implantation on the FS,
   LB mask, B^+, 30keV, 5×10^{14} cm^{-2}



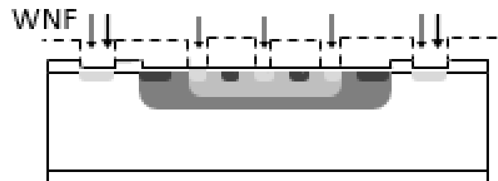
7. Boron implantation on the BS,
   LBB mask, 30keV, 5×10^{14} cm^{-2}



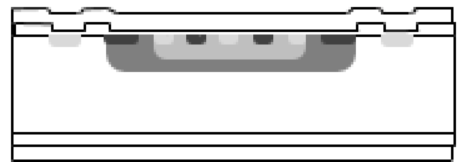
8. Phosphorous implantation on the BS,
   WNB mask, 180 keV, 5×10^{15} cm^{-2}



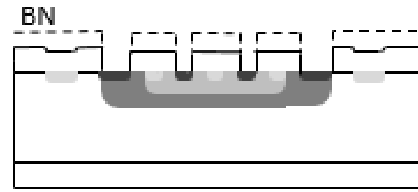
9. Phosphorous implantation on the FS,
   WNF mask, 100 keV, 1×10^{15} cm^{-2}



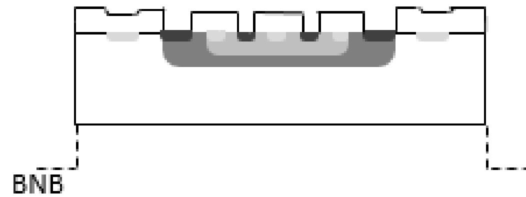
10. TEOS deposition, LPCVD,
    Furnace E1, 400 nm,



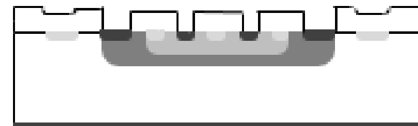
11. Annealing 950°C, 20 min in furnace C2



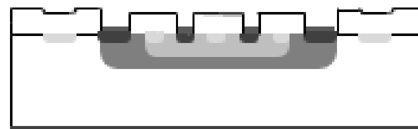
12. Wet etching of oxide on the FS, BN mask



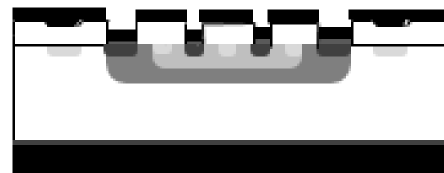
13. Wet etching of oxide on the BS, BNB mask



14. Boron deposition on the BS Marangoni cleaning,
    - BS: BK 800 - B 690C - 7m

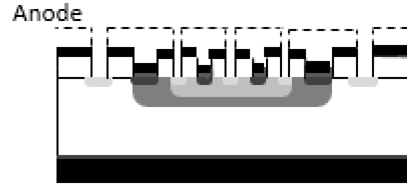


15. Boron deposition on the FS
    - FS: BK 700 - B 690C -7m

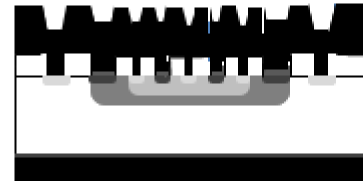


16. Metallization:
    - Sputtering of ZrN, 10 nm on the BS
    - Sputtering of ZrN, 10 nm on the FS
    - Sputtering of Pure Al, 300 nm on the FS
    - Sputtering of Pure Al, 300 nm on the BS
    - Sputtering of AlSi, 1475 nm on the BS

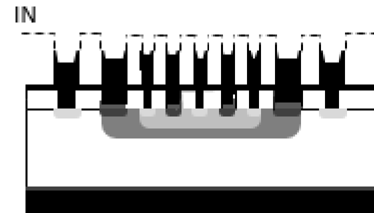
17. Plasma etching of Al, oxide and TEOS on the FS,
    Anode mask



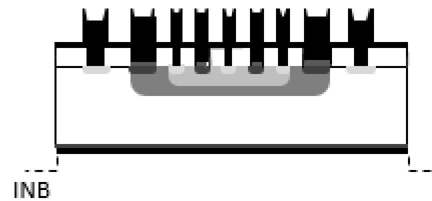
18. Metallization:
    - Sputtering of AlSi, 1475 nm on the FS



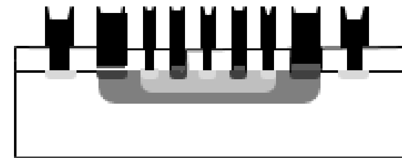
19. Plasma etching of Al back to 150 nm Pure-Al on the FS,
    IN mask



20. Plasma etching of Al back to 150 nm Pure-Al on the BS,
    INB mask



21. Wet etching of Al and landing on the boron layer on both sides (the FS and BS),
    HF 0.55% , 2-3 min



22. Alloying: Furnace C4, program: Alloy1

Figure 5.3 shows photos of SDD wafers during the last step of processing (alloying). Different SDD structures can be seen in the wafer.

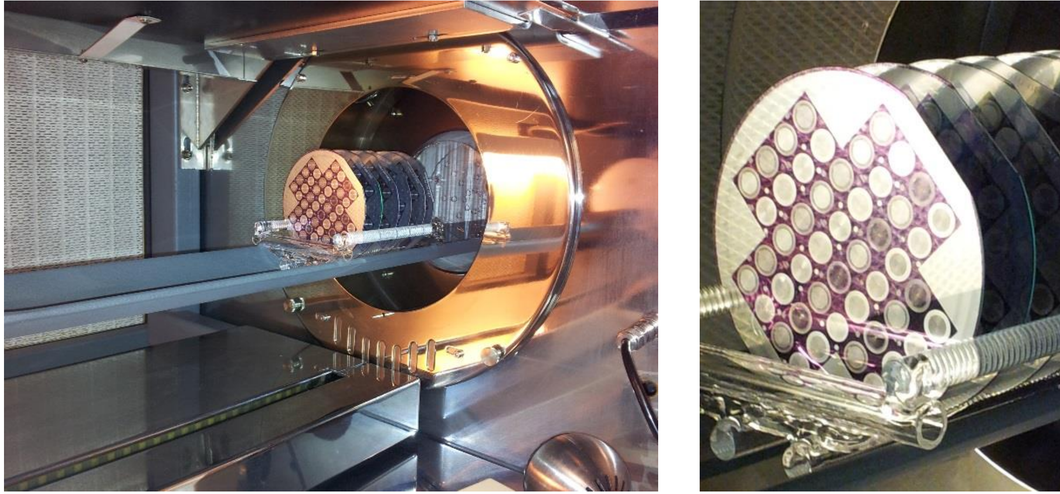


Figure 5.3: SDD wafers at alloying step in C4 furnace (last step of processing).

5.3 Characterization of Fabricated SDDs

5.3.1 Starting Material

In this thesis the detectors were fabricated on available wafers with following specifications:
4-inch diameter, FZ, double side polished, <100> silicon wafers orientation, resistivity of about 2-10kΩcm, n-type Phosphors doping and a thickness of 500±25 μm.

5.3.2 Electrical Measurements Setup

For the measurement of the devices, a Cascade Microtech Summit 12000 probe station was used. The DC measurements were performed on an Agilent 4156A/4156C parameter analyzer; for the CV measurements an HP 4284 LCR meter was used. For the high voltage IV measurements up to 1100V, a Keithley 2410 measurement system was used. Moreover, since the fabricated drift detectors have contact pads on both sides of the wafer, we developed a silicon

interposer package to transfer all connections to the top-side in order to be able to use the one-sided cascade measurement system [this thesis].This novel technique will be discussed in Section 5.4.

5.3.3 Extracting Doping Profile of High Resistivity Silicon Wafers

To verify the quality of high resistivity silicon wafers, a PIN test diode on both sides of the wafer was designed to extract the doping profile of the silicon wafer from the CV measurement.

To extract the doping profile from CV measurement, one can use the depletion region width formula as follows:

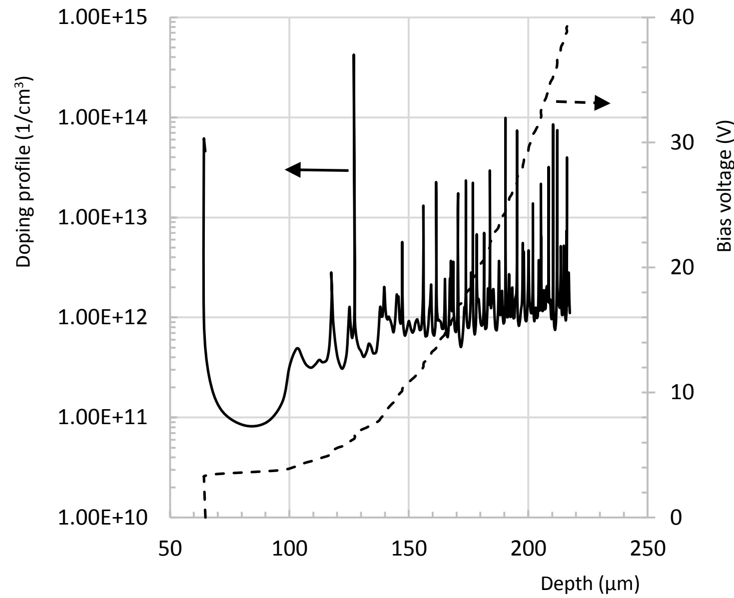
$$X_d = \left(\frac{2\varepsilon_o \varepsilon_r v}{qN}\right)^{1/2} \tag{5.1}$$

$$X_d = \frac{\varepsilon_o \varepsilon_r A}{C} \tag{5.2}$$

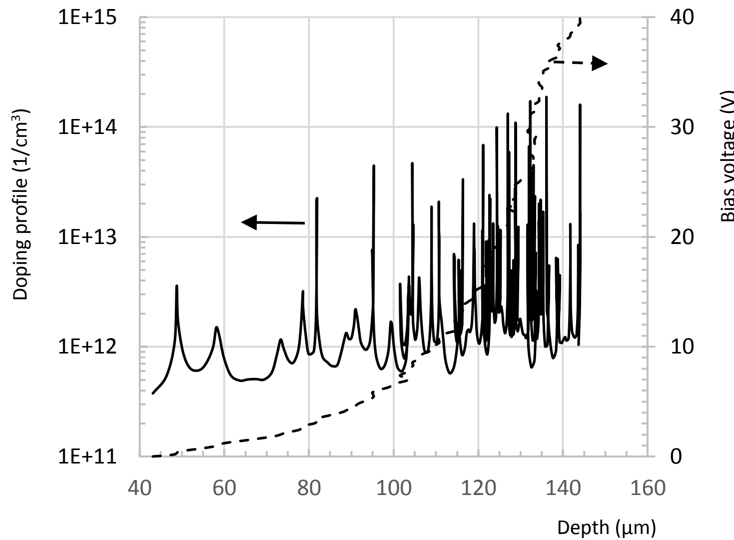
$$N = \frac{2}{q\varepsilon_o \varepsilon_r A^2}\left[\frac{d\left(\frac{1}{C^2}\right)}{dv}\right]^{-1} \tag{5.3}$$

where X_d is the doping depth, N is the doping, A is the diode area, and C is the measured capacitance.

The CV measurement system is limited to a maximum of 40V as reverse bias be applied to the p-n diode. The CV measurement was performed at both sides of the wafer. Thereafter the doping profile of the wafer was extracted using Equation 5.3 as a function of depth. Measurement and calculation resulted in 144.5μm and 217.5μm depletion depths on the entrance window side and device side of the silicon wafer, respectively. This measurement reveals that the entrance window (front side) of the wafer has lower resistivity than the device side (back side). Figure 5.4(a,b)illustrates the bias voltage and the extracted doping profile versus the depletion depth from CV measurements for the front side (a) and back side of the wafer (b).



(a)



(b)

Figure 5.4: Extracted doping profile (left) and bias voltage (right) of the wafer measured from (a) device side (back side); (b) entrance window side (front side).

From the measurements shown in Figure 5.4a, it can be calculated that the first 90μm of wafer thickness has a resistivity of 10kΩ-cm while it decreases to 2kΩ-cm in the middle depth of the wafer. However, the measurements depicted in Figure 5.4b and calculation of the resistivity show a resistivity that is twice as low, indicating poor quality of the wafer at the entrance window side. These

measurements reveal that the wafer doping uniformity over the whole thickness of the wafer is not symmetrical and uniform from the front side to the back side and implies that in the center of wafer around 140μm of the wafer thickness was not depleted. Therefore to fully deplete the thickness of the wafer, a higher bias voltage is required. However, in some of the designed structures, breakdown happens before full depletion of the wafer occurs.

5.3.4 Extracting Generation Lifetime and Surface Generation Velocity

Bulk generation lifetime (τ_g) and surface generation velocity (s_g) in high resistivity silicon wafers can be extracted from a family of measured I-V curves of a gated diode [126,127]. Knowledge of τ_g and s_g is essential for process control and radiation damage monitoring in radiation detectors [128].

A schematic cross-section of the fabricated gated diode structure is shown in Figure 5.5a. It can be considered a p-n diode where the p-region is separated into two sections by a circular gate. A metal gate is located between the diodes where all sides of the gate are surrounded by a diode. The major part of the diffusion current will be collected by the diode current [127]. A metal guard ring surrounds the outer diode edge. During gated diode measurement it is biased in a small accumulation (0.2V) and isolates the structure cancelling unwanted side effects from the substrate. Gated diode structures with different dimensions were tested. The gate area (A_g) is 0.3mm^2-1.5mm^2 with a gate length (L_g) of 95-470μm. During the measurement, the diode (inner diode + outer diode) was kept at a constant reverse voltage (V_d) while the changes of the diode current were monitored when the gate was swept from accumulation toward the inversion. Figure 5.5b shows a typical measurement result of the gated diode. The leakage current in the accumulation region is only the diode leakage current. By sweeping the gate voltage toward depletion, an increase in the leakage current was observed due to minority carriers generated at and beneath the gate surface. When the gate was biased further towards inversion, the volume of the depletion layer increased and

higher current was measured. At the point where inversion was reached, a drop in current occurred due to screening of surface traps by the inversion layer.

Figure 5.5: a) Schematic cross-section and b) typical measurement of a fabricated gated diode.

In the Figure 5.5b the Ig current is due to the bulk generation current beneath the gate area and I_s is related to the surface generated current at the gate area. I_g and I_s can be calculated with the following equations [127]:

$$I_g = q\frac{n_i}{\tau_g}A_g\left(W_g - W_{g0}\right) \qquad (5.4)$$

$$I_S = qn_is_gA_g \qquad (5.5)$$

where the depletion width is $W_g = \sqrt{2\varepsilon_{Si}(V_d + 2\phi_F)/qN_D}$, W_{g0} is $W_{g0} = \sqrt{2\varepsilon_{Si}2\phi_F/qN_D}$ and ϕ_F is $\phi_F = (kT/q)\ln(N_D/n_i)$.

In order to extract τ_g and s_g, an I-V measurement was done on 12 samples for each gate length. Figure 5.6 illustrates the average values of the bulk generation lifetime and surface generation velocity as a function of the gate length with error bars indicating one standard deviation. According to referenced literature and text books, a gated diode with a small gate length will give an accurate value for surface generation velocity while a gated diode structure with a large gate length will give an accurate value for a bulk generation lifetime [128]. Therefore the average value of the bulk generation lifetime is 40ms and surface generation velocity is 2.1cm/s for the fabricated wafers. The corresponding area of each structure is shown in the x-axis under the gate length.

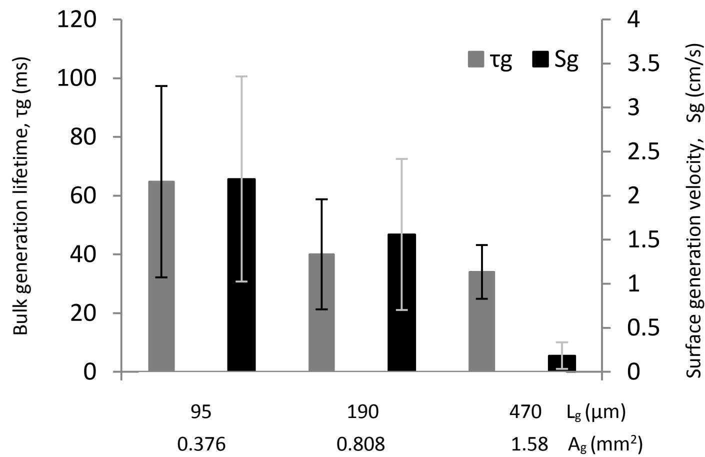


Figure 5.6: Average values of bulk generation lifetime (left y axis) and surface generation velocity (right y axis) as a function of gate length (L_g) and gate area (A_g) over 12 samples. Error bars represent standard deviation. Data is extracted from I-V measurement of gated diode structures.

5.3.5 High-Ohmic PureB Resistors as a Voltage Divider for SDDs

One of the applications for fabricated high-ohmic resistors is silicon drift detectors where on the device side, drift rings are connected via integrated resistors [124,132]. A schematic of the SDD with internal resistors is shown in Figure 5.7.

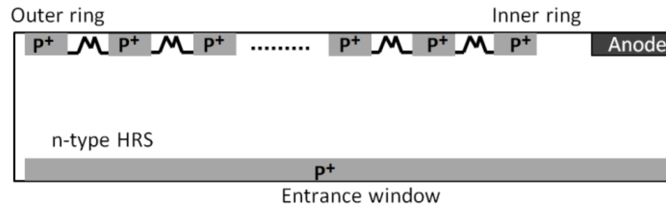


Figure 5.7: Illustration of silicon drift detector and integrated resistors as a voltage divider between the first and last drift rings.

In this configuration, resistors act as a voltage divider to divide the applied voltage between the inner and outer drift rings. It can be observed that linearity, TCR and uniformity of the resistors have significant influence on the generated electric field to push the electrons toward the anode.

We have designed several SDD structures with resistors made with ion implantation and PureB layers deposited at 500°C and 700°C. In the case of resistors fabricated by implantation we designed the resistors between the drift rings in such a way that there are equal resistor values from the inner to outer drift rings as illustrated in the optical image of Figure 5.8 (left). The inset shows part of the corresponding layout design. In the center of the structure the anode is visible. In Figure 5.8 (right) the SDD structure can be seen during electrical measurement. One probe is on the anode, the second one is on the first drift ring, and the third one (not shown here) is connected to the outer ring.

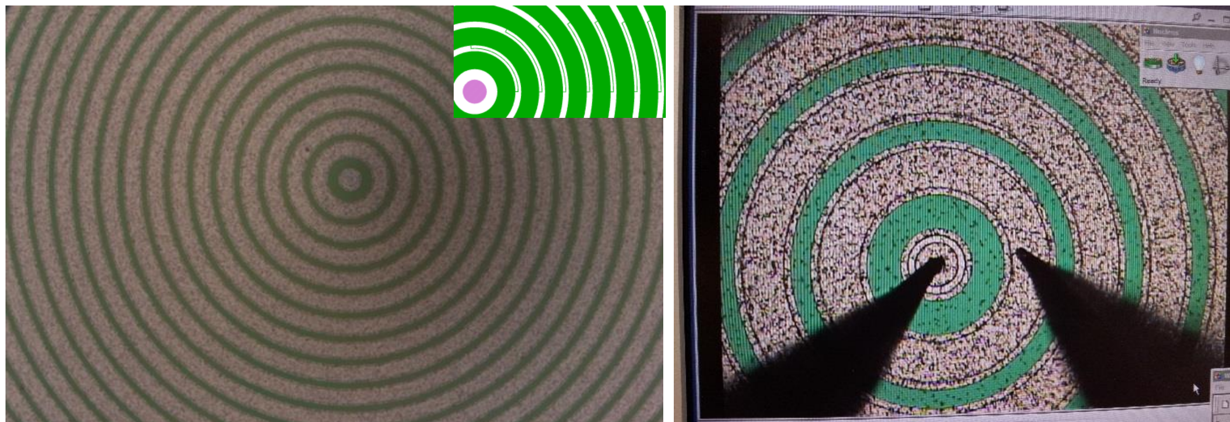


Figure 5.8: Optical images of the fabricated SDD with resistors made with implantation. The implanted areas between the rings have been highlighted in the inset from the layout design. Location of the electrical probes (on the anode and first drift ring) is shown in the right image.

The designed SDD using a PureB layer as the voltage divider is displayed in Figure 5.9. In this design the PureB layer is used to connect neighboring p^+ rings. Only the first and the last rings are connected to the external voltage in order to bias all the rings. The inset is shows the layout design. In the right image the SDD is shown during electrical measurement.

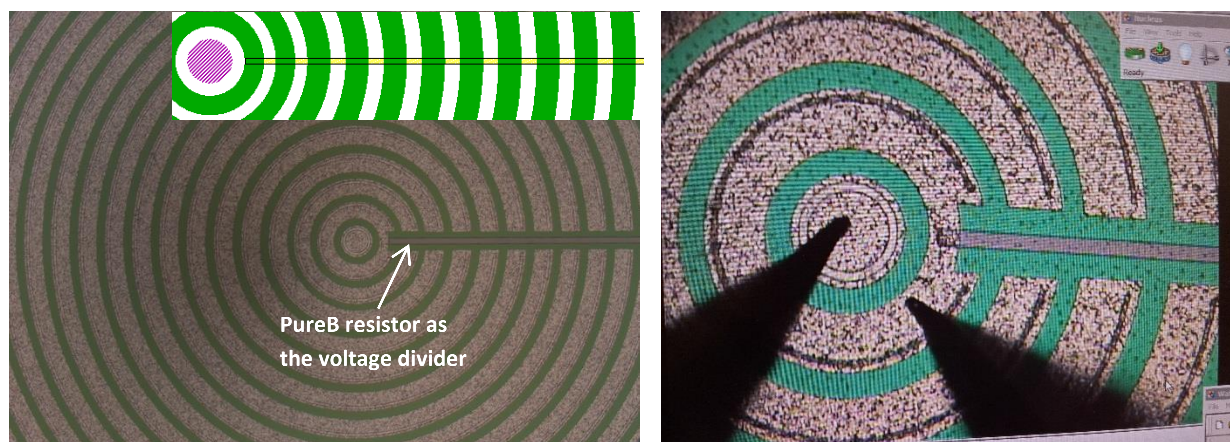


Figure 5.9: Optical image of the fabricated SDD with resistors made with the PureB layer. Implanted areas and deposited PureB layer have been highlighted in the inset from the layout design. Location of the electrical probes is shown in the right image.

5.3.6 Electrical Measurement of High-Ohmic Resistors in SDDs

The SDD structure was biased in such a way that the whole thickness of the wafer was fully depleted. The inner and outer rings were biased in suitable voltages to drift the electrons toward the anode. Current sources with zero Amp values were connected to the intermediate rings between the first and last rings, as shown in Figure 5.10a, to measure the potential of the drift rings. Figure 5.10b shows the monitored voltages over the drift region of the SDD using either PureB or implantation. According to this measurement, PureB made resistors have constant, similar values between consecutive rings. In contrast, for some of the samples which had resistors made with implantation, a deviation from the linear curve was observed. In the implanted samples, as shown in Figure 5.8, resistors were made from narrow lines (to meet the requirement of the resistor values), which makes them sensitive to process variations, especially CD variations in the lithography step. Among ten implantation samples, only one behaved similar to PureB (Sample 5). Other samples showed non-linear voltage distribution over the drift area (Sample 4).

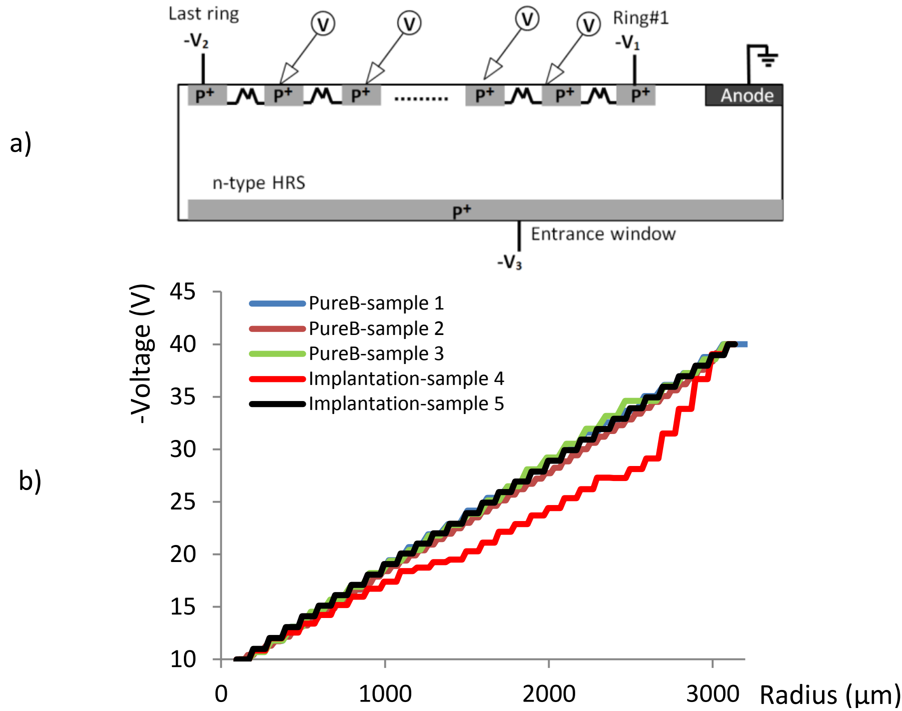


Figure 5.10: a) Measurement setup; b) measured voltage on all drift rings for PureB and implantation made samples.

The resistors between the outer and inner rings were measured in different SDD structures with resistors made with implantation and PureB layers deposited at low and high temperatures. Figure 5.11 compares the measurement results of resistors made with two types of PureB in three different locations on the wafers for different SDD designs.

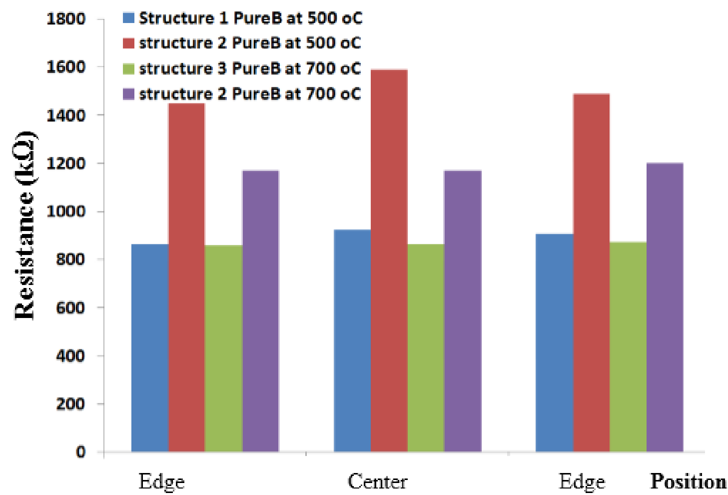


Figure 5.11: Comparison between two resistors made with 500°C and 700°C PureB layers over three locations on the wafer.

It can be seen that resistors made with 500°C and 700°C PureB layers are stable in different locations in the wafer with a maximum 1.7% tolerance over the wafer for high temperature samples compared to 4.9% for low temperature samples. However, in the silicon drift detector fabrication process it is recommended to keep the thermal budget as low as possible to obtain a higher lifetime for carriers and lower leakage current for the final device [9,12].

Figure 5.12 compares the resistors made with 500°C PureB and implantation in three locations on the wafer. Implanted resistors in general fluctuate more over the wafer. It should be mentioned that the plotted resistor values for implantation were the best values we could measure. These low yield resistors made with implantation were already reported in [129]. On the contrary, resistors made with a boron layer have better uniformity and yield. The calculated value of the tolerance for resistors made with implantation is 30% (only working devices were considered) while for resistors made with 500°C PureB it is only 4.9% (all devices were working). We conclude that PureB offers lower tolerances for the resistors.

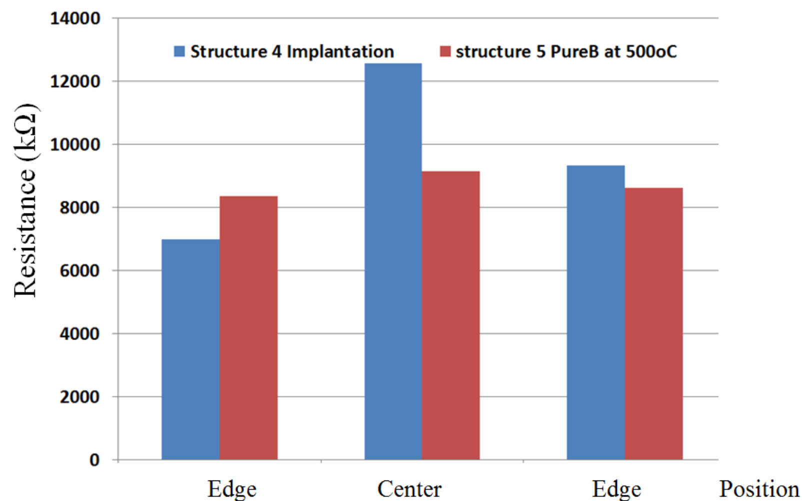
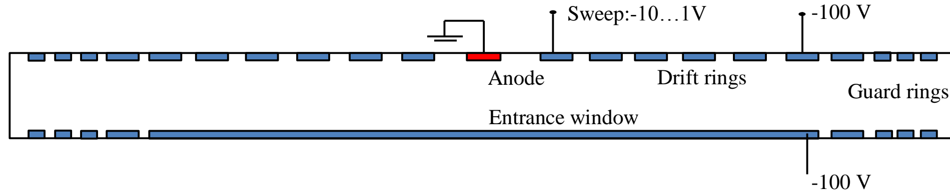


Figure 5.12: Comparison of resistors made with implantation and with 500°C PureB layer deposition.

5.3.7 Leakage Current Measurement Setup

The electrical measurement results of different SDD structures with different process flows will be shown in this section. The SDD structure was biased in such

a way that the whole thickness of the wafer was fully depleted. The inner and the outer rings were biased in suitable voltages to drift the electrons toward the anode. As shown in the drawing of Figure 5.13, the anode was kept at zero Volts during the measurement and the voltage was swept between -10V to 1V in the first drift ring to get the I-V curve of the rectifying diodes. Leakage current was measured in the anode. The multi-guard ring structures were biased similar to the drift rings to minimize the leakage current coming from non-active area of the detector [please refer to Chapter 4 section on multi-guard ring structures for SDDs]. In the optical image, electrical probing on the anode and first drift ring can be seen. Other probes are not visible in the image since they are far from the anode.



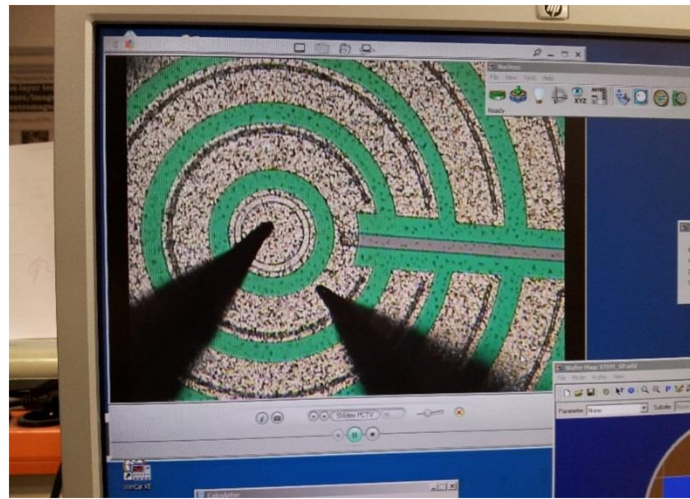


Figure 5.13: Electrical measurement setup.

First we characterize the continuous structure fabricated using one layer of PureB. This structure has a non-linear electric field over the drift region. The total resistance of the boron layer should preferably be high enough to enable us to apply a higher drift voltage between the inner and outer contact pads in the drift region. The measured leakage current was 815pA or 2.6nA/cm^2 at room

temperature at a 10V reverse bias voltage. Figure 5.14a shows the current-voltage measurement plots for a continuous non-uniform drift field structure with only one layer of boron.

Wafers with a double boron deposition have different I-V characteristics. As shown in Figure 5.14b and 5.14c both have lower leakage current (0.3nA/cm² at -1V) as compared to the structure in Figure 5.14a which has 1.29nA/cm² at -1V (thus 4 times less). Furthermore, the double boron layer shows higher built-in potential for the diode compared with the single layer of boron. The higher built-in voltage is probably due to the annealing step between the two boron depositions. The annealing activates the deposited boron atoms on top of the silicon of the drift region. This structure behaves similar to a conventional implanted diode. The second layer of boron deposition introduces a layer of holes in the top layer, which suppresses the minority carriers current resulting in a very low leakage current.

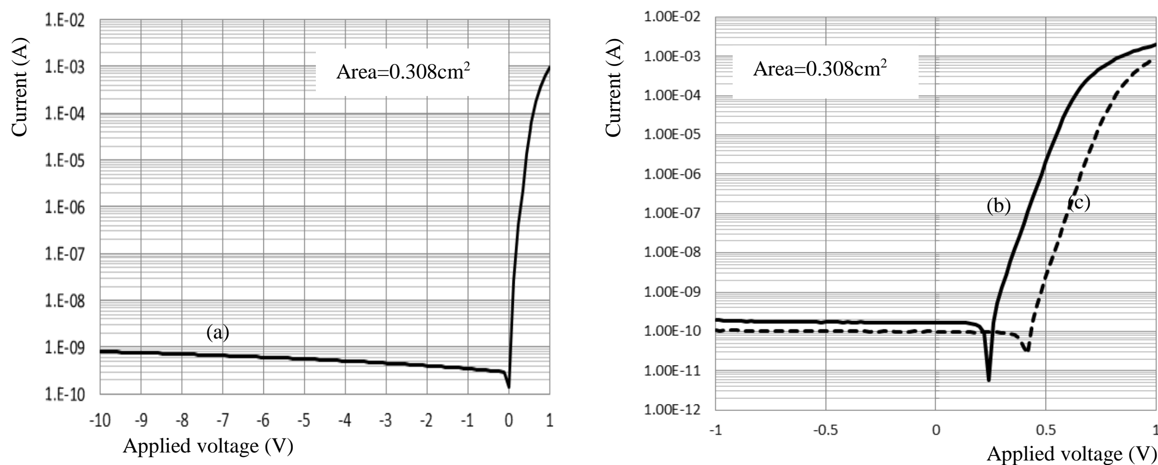


Figure 5.14: Electrical I-V measurement results of the drift region of a detector with a 0.308cm² area on a) one layer of boron on a non-uniform SDD structure, b) two layers of boron on a non-uniform SDD structure and c) two layers of boron on designed constant field SDD.

5.3.8 Impact of Passivation Layer Thickness on Leakage Current

In detector technology, wafers are passivated with a thermally grown oxide layer. This oxide layer protects the bulk material from contamination and mechanical

damage during the process. Usually implantations are done through this oxide layer. Since in an SDD the entire bulk of the device is used for radiation detection, the quality of the passivation layer is important. A dry oxide process (only O_2 gas at 1100°C) was used to grow the oxide layers and there was a cleaning step for furnace using dummy wafers before processing the device wafers. Figure 5.15 compares the average values of the measured leakage current as a function of oxide thickness for SDDs with conventional p-type implants or a boron layer for drift regions over 12 samples. It can be seen that the thicker oxide layer has lower leakage current in both designs. It was observed that during processing, especially implantation, wafers with thin oxide were damaged because of the implanter chuck which touches the other side of the wafer. This results in higher leakage current in the final device. Furthermore, it can be seen that the boron layer design and process have lower leakage current since the boron layer covers the drift region. Surface leakage current contribution is higher in the conventional SDD due to the presence of the oxide layer in between the p-type drift rings. The large spread in leakage current of the boron layer SDD is because of the boron layer deposition at 500°C which typically gives non-uniform boron layer thickness.

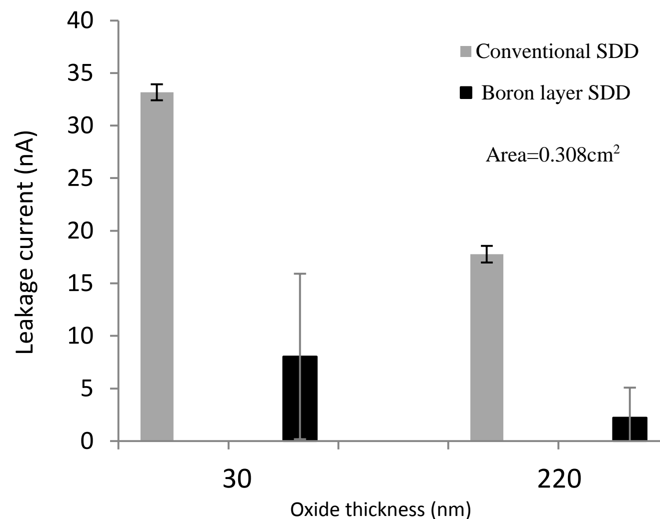


Figure 5.15: Average and standard deviation values of leakage current measured on conventional and double boron SDDs for different oxide thicknesses.

5.3.9 Impact of Thermal Annealing on Leakage Current

High temperature processing can cause higher leakage current in silicon drift detectors due to activation of unwanted impurities in the silicon wafer. Therefore it is recommended to have a high quality silicon wafer for the SDD and to avoid the high temperature processing steps in the SDD fabrication flow. However, activating atoms of implantation can be a challenge for low temperature processing. There are papers which show low temperature SDD processing with on-chip electronics at 600°C or 700°C for 30min have been used to partially recover the silicon lattice from ion implantation defects [7,130,131].

The successful baseline processing of the JFET at DIMES had annealing steps at 950°C-1000°C for 25-35min to activate the dopants. Therefore it was decided to merge this process with an SDD process flow. Figure 5.16 illustrates the leakage current measurement of the conventional SDD design with p-type drift rings either implanted or boron-layer deposited. It can be seen from the measurement shown in Figure 5.16 (left) that furnace annealing offers lower leakage current for the devices. Therefore Epsilon annealing is not sufficient to recover the lattice damages caused by ion implantation. Annealing boron deposited devices, on the other hand, shows similar leakage current for both furnace and Epsilon annealing as shown in Figure 5.16 (right). Epsilon annealing was done in an Epsilon reactor at 850°C for 10min as shown in Table 5.2. This measurement shows that Epsilon annealing can offer low thermal budget processing for boron made junctions.

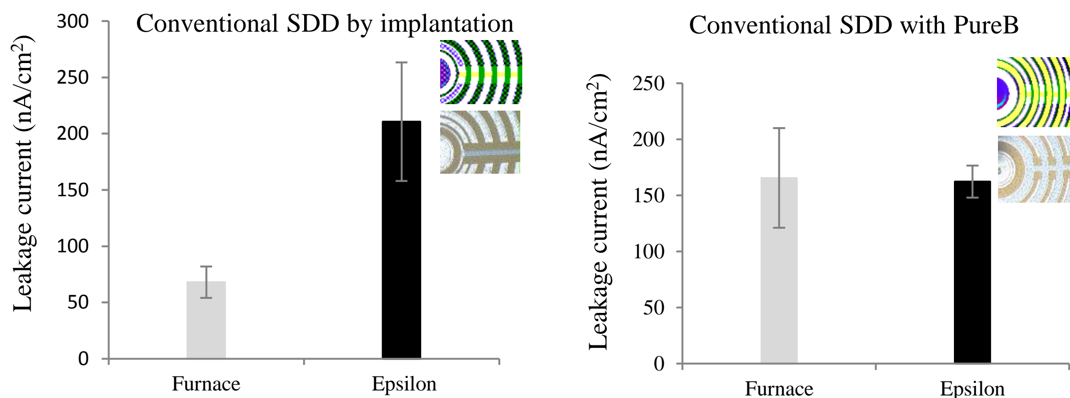


Figure 5.16: Influence of annealing in different systems on leakage current of a conventional SDD fabricated by implantation and a boron layer.

5.3.10 Influence of Field Plate on Measured Leakage Current

As discussed above, the presence of the oxide area between p^+ rings can increase the leakage current. In order to reduce surface leakage current, the oxide layers are covered with a metal layer to keep the electron accumulation layer stable in the conventional SDD terminated by a field plate [76], as shown in the Figure 5.17a. An Al metal layer covers drift ring and neighboring oxide. Figure 5.17b shows a design where only a 1µm overlap was considered. Therefore the oxide layer is not covered with metal. Figure 5.16c shows the effect of the field plate on the leakage current of the SDD. The experimental data are the average values obtained from 6 samples over the wafer for each structure, with error bars indicating one standard deviation. It can be seen that adding a field plate reduces the leakage current by a factor of two. In the SDD structure, the potential is derived from neighboring p+ ring and directly coupled to the adjacent MOS structure shielding the electrons which are accumulated in the vicinity of the SiO_2-Si interface, resulting in lower leakage current.

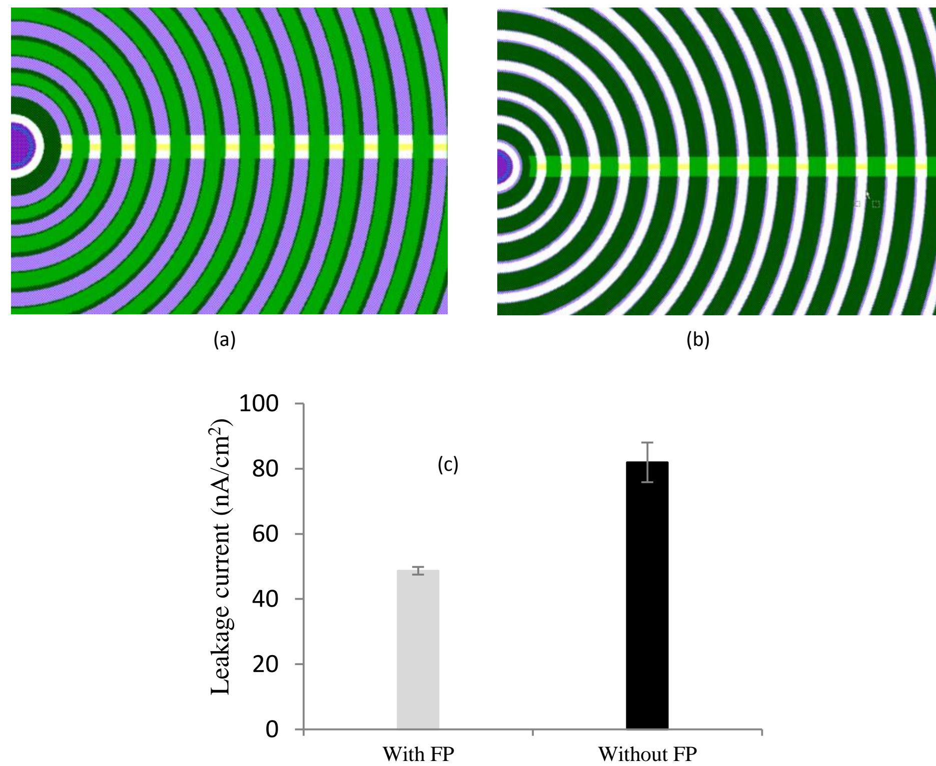


Figure 5.17: Conventional SDD a) with FP; b) without FP; and c) leakage current of fabricated SDD structures with and without field plate.

5.3.11 Influence of Two Times Boron Layer Deposition on Leakage Current (Constant Electric Field)

A double PureB process flow was developed for the first time in this thesis. This is a novel process flow for detector fabrication which offers extremely low leakage current. In this process the p-type implantation and furnace annealing steps were replaced with double boron layer deposition with annealing in the Epsilon for a very short time (5-10min) in between boron layer depositions [124]. Figure 5.18 compares the leakage current of different SDD structures fabricated with both a conventional process flow and our novel double PureB process flow. It can be seen that the average value of the leakage current is 5 times less when using two layers of boron.

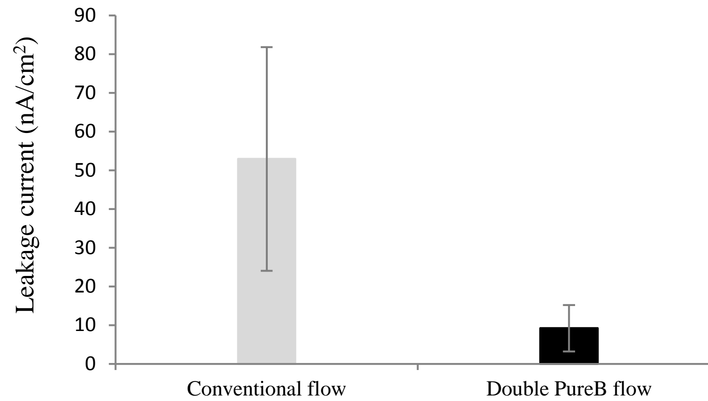


Figure 5.18: Double boron layer process flow reduced the leakage current of SDDs by factor 5 with respect to conventional flow.

5.3.12 Comparing Leakage Current of Fabricated PureB-SDDs

Figure 5.19 shows optical images of the front side (left) and back side (right) of fabricated SDD structures. Different structures such as the conventional SDD, continuous PureB SDD and constant field SDD were fabricated.

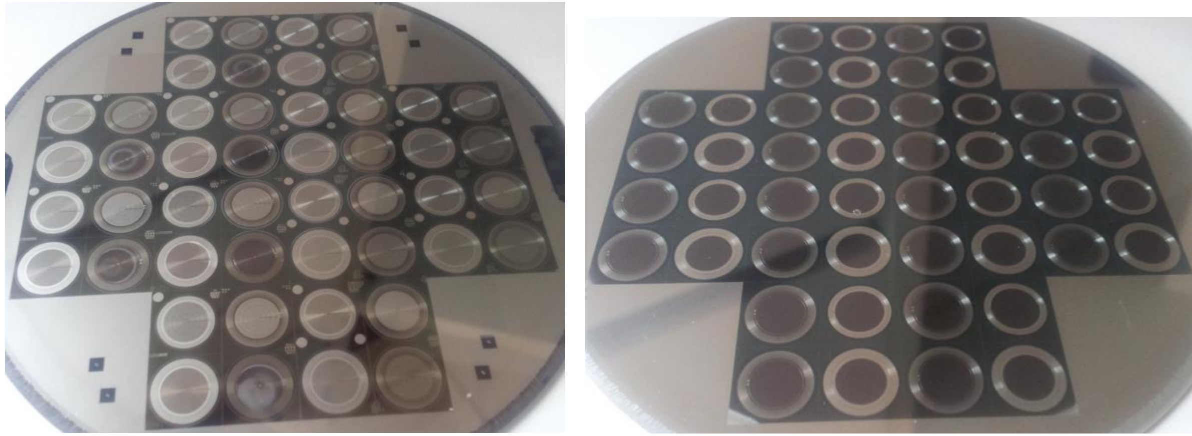


Figure 5.19: Front side (left) and entrance window side (right) of fabricated SDDs on a 4 inch high resistivity silicon wafer with 500µm thickness. SDDs have different designed structures.

Figure 5.20 shows the average values of the measured leakage current at a -100V reverse bias voltage for three SDD structures: conventional SDD with p^+ implanted rings without a sink anode and field plate, continuous boron layer SDD, and constant field PureB SDD over 12 samples. Leakage current was measured at the wafer level. It can be seen that fabricated SDDs using a continuous design and constant field design respectively have around 6 and 20 times less leakage current compared to conventional SDD.

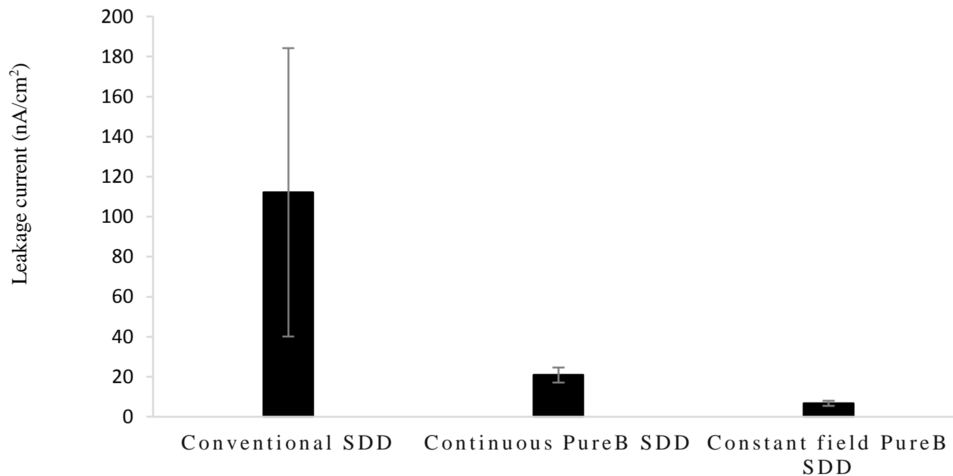


Figure 5.20: Average and STD values of leakage current measured at -100V for different structures.

5.3.13 Characterization of On-Chip Amplifier (JFET)

As discussed in Chapter 4, an on-chip JFET amplifier was embedded in the SDD structure. Two types of JFET structures with different implantation parameters were fabricated. Since measuring the JFET in a SDD structure is not possible (the gate is connected to anode) at the wafer level, individual JFET structures were placed in the layout with similar dimensions as SDD JFETs. One of the measured dc characteristics of the JFET is shown in Figure 5.21. This transistor corresponds to the structure shown in Figure 4.6 in Chapter 4. The S/D of this transistor had Phosphorous plus Arsenic implantations with a deeper version of implantations for deep n- and deep p-regions, as explained in Table 4.1 of Chapter 4. The length of the transistor is L=4.5µm and the width is W=48.5µm. Using the formulas discussed in Chapter 4, the saturation current is equal to 412.5µA, the transconductance (g_m) is 198.65µA/V at the drain voltage of 4V and the gate voltage of zero volts, pinch-off voltage is -4V, and gate capacitance is 71.48fF. Typically while the SDD running, the gate voltage is zero, which is connected to the anode; the drain is connected to a supply voltage of 4V. Any incoming radiation will create electrons which are collected in the anode, thus reducing the gate voltage or current. External electronics sense this current reduction and then reset the gate to zero.

These data are comparable with reports from different groups where fabricated JFETs with a 792µA saturation current and g_m value of 310µA/V have been reported [100].

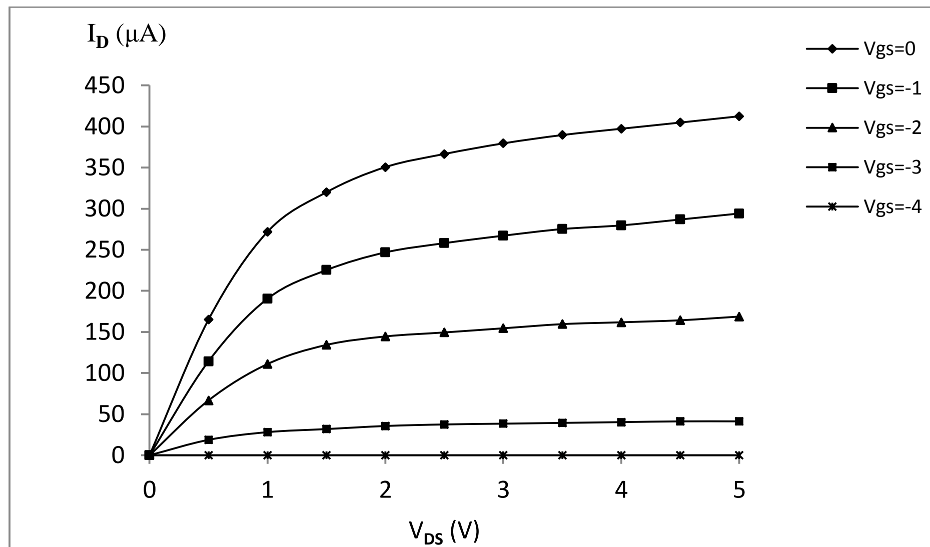


Figure 5.21: Family of Id-Vd curves for fabricated the n-channel JFET with L=4.5µm and W=48.5µm.

5.4 A Novel Silicon Interposer for SDD Measurement

As discussed, SDD characterization requires measurement of multiple contact pads on both sides of the wafer. Using a novel silicon interposer [125], all contacts are transferred to the same side of the wafer so that the measurement can be done using conventional probe stations for one-sided probing.
The idea is to glue the device under test (DUT) to this interposer and then wire-bond the front side and back side contacts to the interposer. The designed package is illustrated in Figure 5.22.

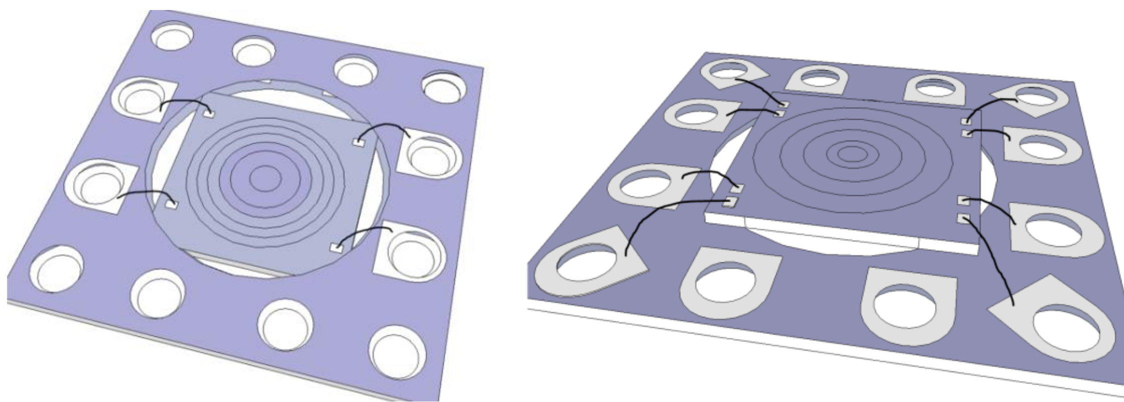


Figure 5.22: Illustration of the front and back side of the designed package for dies with two-sided contacts.

There are several advantages of using this package. First of all the package is made on silicon wafers using conventional integrated circuits fabrication methods which makes it compatible with CMOS processing. The formation of through silicon Vias (TSVs) is now well-developed in silicon technology which gives the possibility of designing packages with small dimensions. Moreover, this package has advantages such as thermal mismatch improvement, better thermal conductance and stability of dimensions because both the die and the package are made of silicon.

In some applications such as the electron and x-ray detectors, external circuitry is required to amplify the signal level. With this package it is possible to integrate some of the electronic devices such as JFETs and capacitors on the package itself. Therefore it would be possible to enhance the performance of the final product by using such a package.

5.4.1 Fabrication Process

For fabrication of such an interposer, a <100> double-sided polished wafer with a thickness of 560μm was used. After making alignment markers (zero layers) on the wafer, a 6μm-thick PECVD oxide was deposited on both sides of the wafer to act as a mask for silicon etching. Then using the designed via mask, we patterned the resist and then dry etched the oxide. To etch through the silicon we used a Bosch-process deep-reactive-ion-etching (DRIE) system called Adixen. The etching temperature was -10°C to have better oxide selectivity and we used a combination of O_2, SF_6 and C_4F_8 gases. Oxygen was used to make the profile similar to KOH wet etching. The optimized recipe gives an angle of around 60° for the etching profile. By adjusting the oxygen flow rate we can obtain different angles. Without oxygen the etching will proceed vertically straight down resulting in an angle of 90°. The etching time was 2 hours resulting in complete silicon etching and stopping on the oxide layer.

As shown in Figure 5.23, after through-silicon etching we removed the oxide mask in a BHF solution and then cleaned the wafer in a nitric acid bath for 10 min followed by DI water washing.

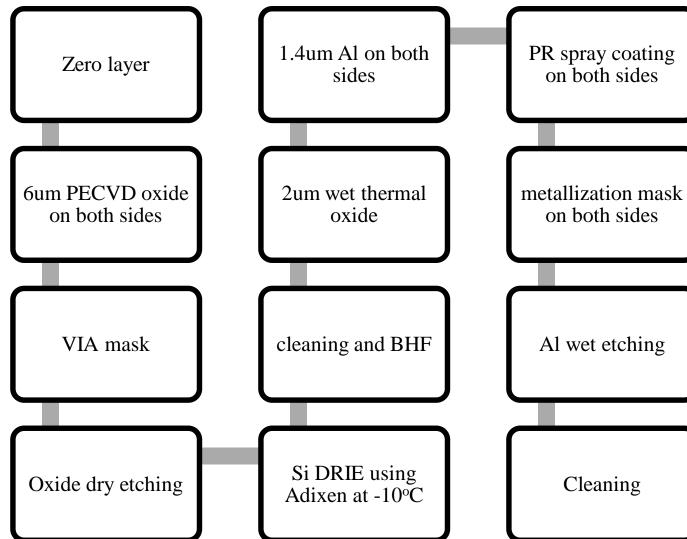


Figure 5.23: Process flow for fabricating the designed package.

The next step was to isolate the vias from the silicon package. We used wet oxidation for 9 hrs at 1100°C to achieve 2μm-thick oxide inside the holes. After

that 1.4μm Al was deposited on both sides of the wafer. For better step coverage and contact of the metal on both sides, we deposited the Al at 350°C using a pulsed DC sputtering system. Using the next mask we etched the Al. In this step photoresist had to be spray coated since we had holes in the wafer. We spray coated the resist on both sides of the wafer and then we did exposure using the same mask on both sides of the wafer. After developing and baking the resist, we used wet etching to remove the Al. The final step was a cleaning in acetone and nitric acid followed by DI water rinsing.

Photos with views of the top and back side of the fabricated wafer are displayed in Figure 5.24. The front side view of the vias, holes and contact pads is visible in this image. The DUT is to be placed in the middle of the big hole and glued to this side of the package. The location of the bond pads on the backside of the DUT has to be visible through the big holes so that wire bonding can be done through this hole. A special tool was made in order to wire-bond the contact pads through this hole. The whole package is isolated from the vias with the 2μm-thick thermal oxide.

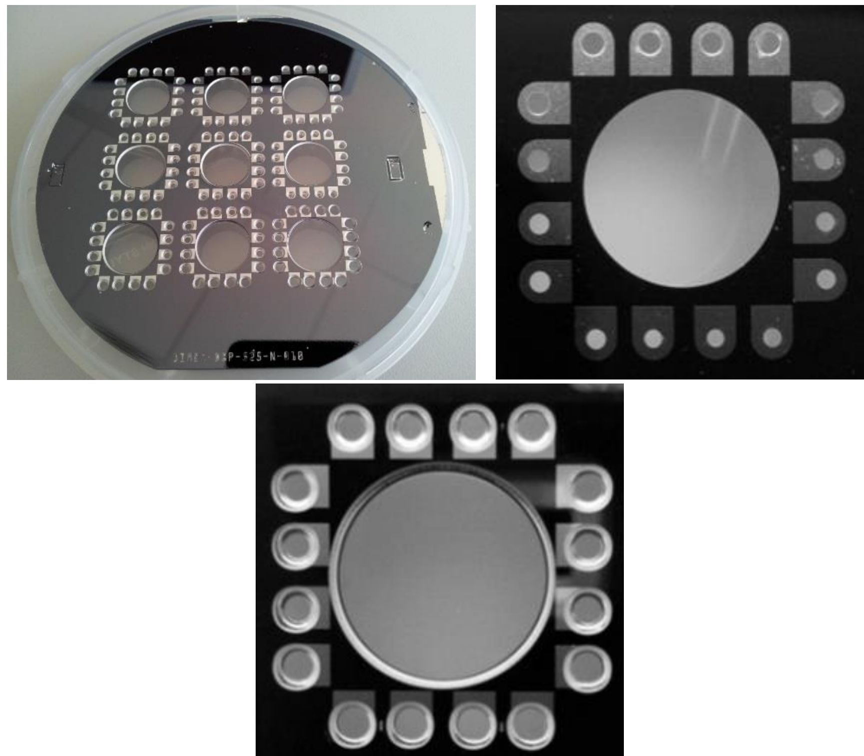


Figure 5.24: Front side and back side images of the fabricated silicon interposer.

SEM images of the front side and back side of the fabricated interposer are shown in Figure 5.25. The layer surrounding the hole is Al, which is extended for wire bonding and measurement needle purposes.

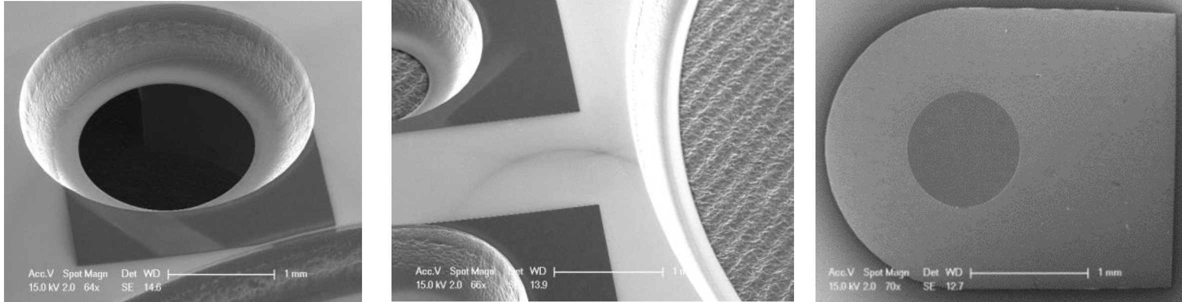


Figure 5.25: Front side and back side of etched holes.

5.4.2 Measurement Results

The final packaged SDD device is shown in Figure 5.26. We developed a Teflon container to prevent any damage to the back side wire bonds. All contact pads are available for measurement from the top side of the complete package. The device that we mounted on the silicon package/interposer had several bulk p-n diodes and SDDs with two contacts on the back side and several contacts on the front side of the wafer. Using this developed package we could do all DC and CV measurements on the probe station successfully.

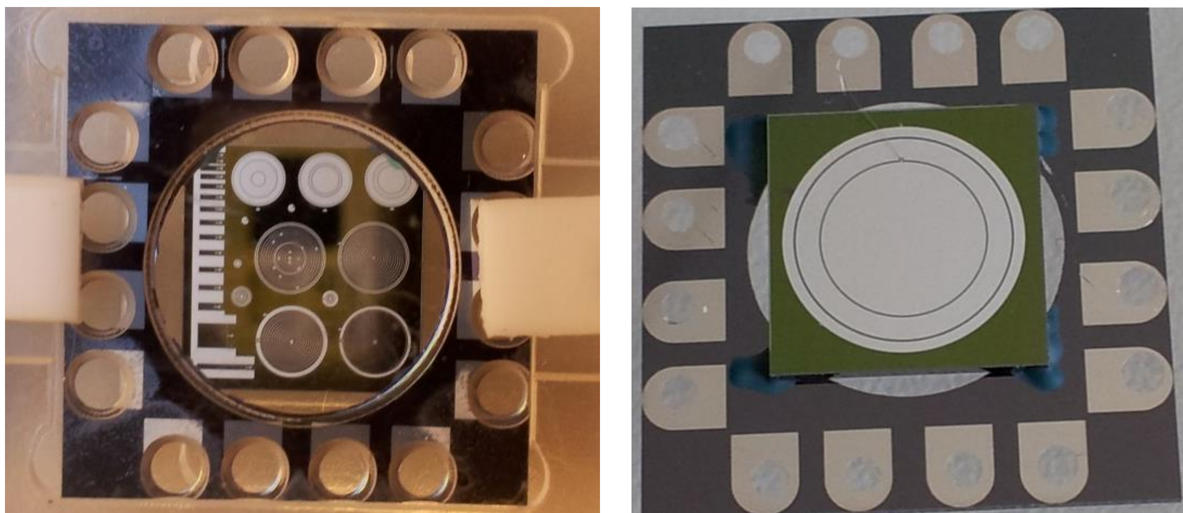


Figure 5.26: Mounted SDDs on the package with access to the front and back side contact pads.

Moreover, Figure 5.27 shows a DC current voltage measurement between two neighboring vias. As can be seen in this plot, even when applying a voltage of -100V between two neighboring contact pads in the package, there is no significant increase in leakage current between them (less than 100pA).

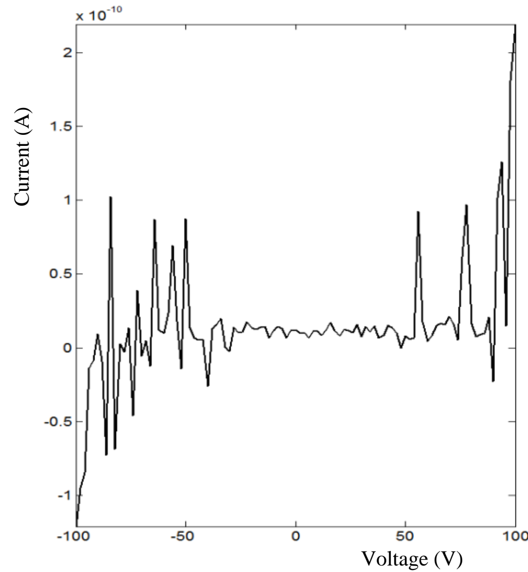


Figure 5.27: Electrical measurement of the isolation between two contact pads.

The measured resistance between the top and bottom contacts of one via was in the order of 0.8485m**Ω**, which is negligible compared to the series resistance found in most devices.

5.5 Conclusions

In this chapter, the complete fabrication process of SDDs with one layer of boron, double boron layers and an on-chip JFET were reported. Then the results of electrical measurements to characterize the fabricated devices were displayed. Using CV measurements, the doping profile of silicon wafers was extracted. According to measurements with 40V applied voltage 144.5µm and 217.5µm, depletion depths on the entrance window side and device side of the silicon wafer were calculated. This measurement reveals that the entrance window (front side) of the wafer has lower resistivity than the device side (back side). Using a gated

diode structure, the average value of the bulk generation lifetime was 40ms and surface generation velocity was 2.1cm/s for the fabricated wafers.

The fabricated PureB resistors displayed attractive electrical characteristics in many respects. For both low and high Ohmic sheet resistance values, the resistance has high linearity and the tolerance over the wafer remains within a few percent. Particularly the temperature performance is exceptional with temperature coefficients for mega-ohm resistors around 400ppm/^{o}C in the temperature range 15°C to 95°C. In this work a bare PureB layer was implemented because the resistor was fabricated together with the light-entrance window of low-energy electron photodiode detectors but it is also possible to cover the PureB with a dielectric layer for protection and/or increased integration compatibility. In general, resistors made with a 700°C PureB layer have better uniformity than 500°C. However, depending on the required range for resistor values and thermal budget of the process, 500°C resistors can be used as well. PureB made resistors have been employed in silicon drift detectors to divide the drift voltage between drift rings. Resistors made with PureB have a tolerance as low as 5% but resistors made with implantation show around a 30% tolerance if we consider only working implanted resistors.

Furthermore, it was found that in both conventional and boron layer SDDs, thicker passivation gave lower leakage current. Furnace annealing is necessary only in the case of implantation in order to recover the silicon lattice. Adding a field plate to the drift region reduces the surface leakage current, thus lower leakage current was obtained. A double boron layer process resulted in leakage current 5 times lower (9.18nA/cm^2) compared with conventional implanted p-type rectifiers for drift region.

Furthermore, the measured JFET showed saturation current of 412.5µA, and the transconductance (g_m) of 198.65µA/V at a drain voltage of 4V and gate voltage of zero volts, pinch-off voltage of -4V and gate capacitance of 71.48fF which are comparable with what is reported in the literature.

At the end of the chapter, a novel silicon interposer package was reported which transfers all contacts from one side of detector to the other side in order to measure the devices in conventional probe stations.

Chapter 6

Conclusions and Recommendations

6.1 Conclusions

The nanometer thick boron layer deposited by CVD offers a shallow junction p^+-n diode suitable for low energy electron and X-ray detectors. These detectors potentially enable higher detection responsivity for low energies. Employing boron layer technology in silicon drift detector structures requires careful designing of the drift region, guard rings, and entrance window. Calculations and simulations are required to make sure that from one point of view, the drift function of the boron layer can compete with the state of the art collection speed of SDDs, and on the other hand, can offer lower leakage current. Furthermore, designing guard ring structures using boron layer technology should be carefully performed in order to have low leakage current at higher bias voltages. Developing the fabrication process steps in both sides of the high resistivity wafer and introducing the double boron layer are other challenges. Optimizing implantation energies for the JFET, boron layer deposition temperature and time, in situ annealing and wet landing on the boron layer on both sides of the wafer was investigated. Finally characterization of fabricated devices with contact pads on both sides using high voltage power suppliers was achieved in this thesis. The main conclusions of this thesis are as follows:

- The boron layer has many advantages when used in different applications such as detectors and resistors. Since this nm-thick layer creating shallow junction diodes with very low dark current, it is suitable for low energy electron and X-ray detectors, and offers high responsivity.

- The boron layer offers high ohmic resistors with very low TCR (temperature coefficient of the resistor) and tolerances. PureB-layer resistors designed and fabricated for silicon drift detectors. The sheet resistance values extracted from measurement of the ring structures are 2.5×10^4 Ω/□ for a 7min 700°C deposition and 3.8×10^5 Ω/□ for a 20min 500°C deposition. Fabricated resistors showed high linearity in voltage ranges between 10V and 100V and they are stable in temperature ranges from 15°C to 95°C. The 500°C resistors had a TCR of less than 200ppm/°C up to a measurement temperature of 70°C which increased to around 1000ppm/°C at 95°C. The TCR of the 700°C sample had an almost constant value of less than 400 ppm/°C over the whole measurement temperature range. The calculated tolerance of several resistors made in different ranges by 500°C and 700°C boron layers showed respectively less than 1% for the 700°C, and around 3% for a 500°C deposited boron layer. The measured leakage current was less than 1nA/cm^2 at 10V reverse bias over all dies of the 100mm wafer. Resistor tolerance was in the range of 1% to 5% for both kΩ and MΩ values. PureB made resistors have been employed in silicon drift detectors to divide the drift voltage between drift rings. Resistors made with PureB have a tolerance as low as 5% but resistors made with implantation show around a 30% tolerance if we consider only working implanted resistors.

- It has been shown that 10nm sputtered ZrN can enhance the quality of the detectors without any influence on the electrical parameters of the devices and is compatible with the boron layer process. Optical and SEM inspections showed defect-free surface of detectors when using 10nm ZrN between an Al and boron layer for both 700°C and 500°C deposited layers. As an alternative, a lift-off process was developed to not have any Al residuals on the boron layer. For both PureB layers deposited at 700°C or 500°C, the lift-off process was successfully performed. However, the limitation of Al thickness and the deposition method (evaporation) can be a challenge for some applications.

- For the low temperature deposited PureB layer it was shown that PECVD TEOS has better adhesion than PECVD oxide to the porous boron layer.

- The boron layer was introduced to act as an ultra-shallow junction entrance window for low energy of X-rays and as a voltage divider in the drift side. Single and double boron layers were introduced to drift the electrons toward the anode, while the rectifying p-n junctions had very low leakage current. There is no oxide present in between the rectifying diodes, thus the surface leakage current is low. Calculations and simulations showed that a single boron layer does not provide a sufficient electric field to drift the electrons toward the anode. The electric field was around three orders of magnitude less in the outer ring, thus it is only effective at the inner side of the detector; there was not enough electric field to move the electrons toward the anode in the outer sides of the detector. Potential distribution showed that at 40V applied voltage, electrons are accumulated in the gutter, the minimum of the potential energy, and are moved slowly to the anode. At 160V drift voltage, the slope along the detector surface was lightly sharper than the 40V case but still too small to drift the electrons toward the anode. Therefore around 80% of drift area had an almost zero electric field. Using the double boron layer process with different sheet resistances and a special design, the electric field was radial and constant over the drift region and the SDD has very low leakage current. In this design the low sheet resistance layer was denser near anode and the high sheet resistance layer was present in the outer rings to produce constant resistance and an electric field over the drift area.

- Electrical measurements showed that the positive coefficient of breakdown voltage corresponds to avalanche breakdown for the fabricated devices. Using a single n+ guard ring for the p-n diode detector the leakage current could be lowered significantly. However, the breakdown voltage was reduced also in the best case to 85V. To maintain the lower leakage current and to obtain a higher breakdown voltage, a multi-guard ring structure was used. Among 9 different multi-guard ring designs, one of them works up to the limit of the measurement systems (1100V) with very low leakage

current in the range of 1.5-3nA/cm^2 for the detector. In this structure the width of the guard rings was 25µm, the first gap (between the large guard and first intermediate guard ring) was 35µm, and the pitch was 80µm for the rest of the rings, with an inward field plate extending 5-30µm. Other structures show around a 400V breakdown voltage. According to the measurements of different designed guard ring structures, a roughly 40µm gap is an optimal value for the distance between the large guard ring and first ring of the multi-guard structure. Moreover, it was found that a field plate in the inward direction offers a higher breakdown voltage because of charge shielding. The measured voltage drop over the guard rings showed an exponential reduction of the negative voltage, and ground potential in the 4th guard ring.

- Using CV measurements, the doping profile of silicon wafers was extracted. According to the measurements with a 40V applied voltage, 144.5µm and 217.5µm depletion depths on the entrance window side and device side of the silicon wafer were calculated. This measurement reveals that the entrance window (front side) of the wafer has lower resistivity than the device side (back side).

- Using gated diode structures the average value of the bulk generation lifetime was 40ms and surface generation velocity was 2.1cm/s for the fabricated wafers.

- It was found that in both conventional and boron layer SDDs, thicker passivation gave lower leakage current. Furnace annealing is necessary only in the case of implantation in order to recover the silicon lattice. Adding a field plate to the drift region reduces surface leakage current, thus lower leakage current was obtained. The double boron layer process resulted in leakage current (9.18nA/cm^2) 5 times lower compared with conventional implanted p-type rectifiers for the drift region.

- Integrating an on-chip amplifier can improve the performance of SDDs in terms of noise and resolution. To select the type of transistor for the SDD, a JFET is preferred because of noise considerations. Bipolar transistors

have higher shot noise and CMOS transistors have the higher 1/f noise component. In designing the JFET there is a trade-off between obtaining minimum noise and minimum capacitance while keeping transconductance (g_m) as high as possible. Gate capacitance plays an important role in this trade-off. Since mobility of the nFET is higher, it offers a higher cut-off frequency than the pFET. For optimum SDD resolution input capacitance of the JFET is equal to the detector's capacitance. In SDDs, typically the JFET is placed inside the anode which is isolated by a p-type region from the anode. Two different designed JFET transistors with a 4.5µm gate length together with reset mechanisms (MOS and reset diode) were discussed in detail. The measured JFET showed saturation current of 412.5µA, a transconductance (g_m) of 198.65µA/V at the drain voltage of 4V and the gate voltage of zero volts, a pinch-off voltage of -4V, and a gate capacitance of 71.48fF.

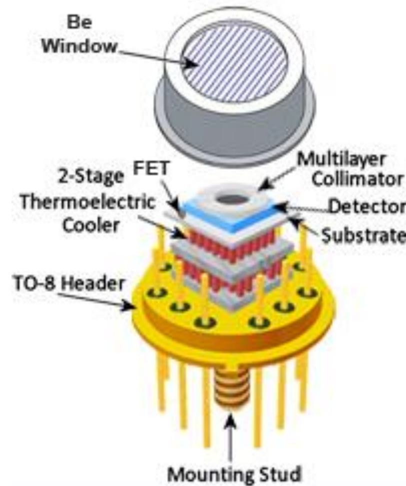
- Design and fabrication flow of a novel silicon interposer package were reported to transfer all contacts from one side of detector to the other side in order to measure the devices in conventional probe stations. In this interposer, the SDD device was mounted on the center hole; there are TSV-type connections in the periphery of the center hole. By wire bonding, contact pads are connected to the TSV connections to transfer all pads to one side.

6.2 Recommendations

In this thesis it was shown that a boron layer has many advantages when used in silicon drift detectors such as lower leakage current, an ultra-shallow junction in the entrance window, and uniform drift field using a double boron layer. Furthermore, the JFET integration process flow is compatible with the boron layer process enabling replacement of p-type implantations by the boron layer.

The following items are recommended for future work:

- Full ceramic packaging including a Peltier cooler, Collimator and external circuit to characterize the fabricated SDD devices under X-ray radiation. Here is one example from the AMETEK company:



- Using high quality SDD wafers with a 300µm or 500µm thickness. There are a few wafer manufacturers which produce high quality wafers for SDD applications.
- In this thesis it was shown that when using a boron layer, the leakage current can be very low. Using SiC wafers the leakage current can be reduced even more because the bandgap of SiC is higher. However, detecting lower X-ray energies with SiC SDDs might be a challenge. By combining the boron layer in SiC processing, lower energies can be detected as well.

Bibliography

[1] B. Beckhoff, B. Kanngießer, N. Langhoff, R.Wedell H.Wolff (Eds.), "Handbook of Practical X-Ray Fluorescence Analysis", F.Scholze, book chapter, "X-ray detectors and XRF detection channels", 2006.

[2] Berkeley lectures, "Gas-Detectors", available in: http://inst.nuc.berkeley.edu/NE104/Lectures/Gas-Detectors_NE104_Spring10.pdf

[3] Peter Dendooven, "Detection of energetic particles and gamma rays - Scintillation detectors", 2009-2010, available in: http://www.astro.rug.nl/~peletier/Bas Det Tech 2009 scintillators.pdf

[4] Book, "Semiconductor radiation detectors - device physics", Gerhard Lutz, 1999.

[5] W. Bencivelli, E. Bertolucci, U. Bottigli, A. Del Guerra, A. Messineo, W.R. Nelson, P. Randaccio, V. Rosso, P. Russo, A. Stefanini, "Evaluation of elemental and compound semiconductors for x-ray digital radiography", Nucl. Instr. & Meth. A, vol. 310, no. 1-2, pp. 210-214, Dec.1991. DOI: 10.1016/0168-9002(91)91028-T.

[6] Book, "Semiconductor particle tracking detectors", G.Hall, 1994.

[7] Tobias Eggert, "Semiconductor X-Ray Detectors", available in: http://wwwmayr.informatik.tu-muenchen.de/konferenzen/Jass04/courses/4/TobiasEggert/TalkIoffe.pdf

[8] Presentation by Rene Bellwied, "Silicon drift detectors: A novel technology for medical imaging", available in: rhic.physics.wayne.edu/~bellwied/medical/medical2.ppt

[9] E.A Hijzen: "Design and Fabrication of Silicon Drift Detectors" , Ph.D. thesis, Technical University Delft, The Netherlands, 1995.

[10] H.Sipila, "Energy resolution of the proportional counter", Nucl. Instr.and Meth., vol. 133, no. 2, p.p.251–252 March 1976. DOI: 10.1016/0029-554X(76)90616-9.

[11] F. J. Ramírez-Jiménez, L. Mondragón-Contreras and P. Cruz-Estrada, "Application of PIN diodes in Physics Research", AIP Conference Proceedings, vol. 857, no.2, p.p.395-406, 2006. DOI: 10.1063/1.2359424.

[12] J. Sonsky, "Multi-anode linear SDDs for high-resolution S-ray spectroscopy: Charge confinement and integration of read-out electronics", Ph.D. thesis, Delft university of technology, The Netherlands, 2002.

[13] Amptek Inc.: "X-ray detectors: XR-100CR", specification brochure. available in: http://www.amptek.com/pdf/xr100cr.pdf

[14] D. Renker , "New developments on photosensors for particle physics", Nucl. Instr. and Meth. in Phys. Res. A, vol. 598, p.p. 207–212, 2009. DOI: 10.1016/j.nima.2008.08.023.

[15] ppt, “Optical Receivers”, available in: http://opt.zju.edu.cn/eclass/attachments/2013-05/01-1369313883-194122.pdf

[16] A.Coche and P.Siffert, “Lithium drifted silicon and germanium detectors”, semiconductor detectors, 1968.

[17] Saleh Qutaishat, “Silicon Lithium Detectors for Synchrotron Energy Dispersive X-Ray Fluorescence Spectroscopy (SiLi for EDXRF)” , Conference: The tenth SESAME (Synchrotron-light for Experimental Science and Applications in the Middle East), Amman, Jordan, vol. 1, November, 2012.

[18] Silicon Strip Detectors, available in: http://hll.mpg.de/graphics/PDF_BrochArticle/MPI-HLL-brochure_5.pdf

[19] Book chapter, “Silicon Radiation Detectors”, Yu. K. Akimov, 2006.

[20] CERN, Silicon Pixels, available in: http://cms.web.cern.ch/news/silicon-pixels.

[21] W. S. Boyle and G. E. Smith, “Charge coupled semiconductor devices”, Bell System Technical Journal, vol. 49, no. 4, p.p. 587-593, 1970. DOI: 10.1002/j.1538-7305.1970.tb01790.x

[22] E. Gatti, P. Rehak, “Semiconductor Drift Chamber - An Application of a Novel Charge Transport Scheme”, Nucl. Instr. and Meth. A, vol. 225, pp. 608-614, 1984.

[23] P. Lechner, C. Fiorini, A. Longoni, G. Lutz, A. Pahlke, H. Soltau, L. Strüder, “Silicon drift detectors for high resolution, high count rate x-ray spectroscopy at room temperature”, International Centre for Diffraction Data, Advances in X-ray Analysis, vol. 47, p.p. 53-58, 2004.

[24] Dale E. Newbury and Nicholas W. M. Ritchie, “Elemental mapping of microstructures by scanning electron microscopy-energy dispersive X-ray spectrometry (SEM-EDS): extraordinary advances with the silicon drift detector (SDD)”, Journal of Analytical Atomic Spectrometry, vol. 28, no. 7, p.p. 973-988, 2013. DOI: 10.1039/C3JA50026H

[25] Amptek, “What is XRF?” available in : http://www.amptek.com/xrf/

[26] P. Lechner, L. Andricek, N. Findeis, D. Hauff, P. Holl, J. Kemmer, P. Klein, G. Lutz, N. Meidinger, E. Pinotti, R. Richter, L. Strüder, C. v. Zanthier, “New DEPMOS applications”, Nucl. Instr. & Meth. A, vol. 326, no. 1-2, p.p. 284 – 289, 1993.

[27] J. Kemmer, G. Lutz, E. Belau, U. Prechtel, W. Welser, “Low capacity drift diode”, Nucl. Instr. & Meth. A, vol. 253, no. 3, p.p. 378 – 381, 1987.

[28] Emilio Gatti , Pavel Rehak , “ Review of semiconductor drift detectors,” Nuclear Instruments and Methods in Physics Research A, vol. 541, no. 1-2, p.p. 47–60, 2005.

[29] Emilio Gatti, Pavel Rehak, Jack T. Walton, “Silicon drift chambers - first results and optimum processing of signals”, Nuclear Instruments and Methods in Physics Research Section A, vol. 226, no. 1, pp. 129-141, 1984.

[30] A. Vacchi, A. Castoldi, S. Chinnici, E. Gatti, A. Longoni, F. Palma, M. Sampietro, P. Rehak, J. Kemmer , “Performance of the UA6 large-area silicon drift chamber prototype”, Nucl. Instr. And Meth. A, vol. 306. No.1-2, p.p. 187-193, 1991.

[31] Veljko Radeka, P. Rahek, S. Rescia, Emilio Gatti, A. Longoni, M. Sampietro, G. Bertuccio, P. Holl, L. Struder, J. Kemmer, "Implanted silicon JFET on completely depleted high-resistivity devices", IEEE Electron Device Letters, vol. 10, no. 2, p.p. 91-94, 1989. DOI: 10.1109/55.32439

[32] M. Sampietro, L. Fasoli, P. Rehak, L.Struder, "Novel pJFET embedded in silicon radiation detectors that avoids preamplifier feedback resistor", IEEE Electron Device Letters, vol. 16, no. 5, p.p. 208-210, 1995. DOI: 10.1109/55.382242.

[33] Peter Lechner, Stefan Eckbauer, Robert Hartmann, Susanne Krisch, Dieter Hauff, Rainer Richter, Heike Soltau, Lothar Strüder, Carlo Fiorini, Emilio Gatti, Antonio Longoni, Marco Sampietro, "Silicon drift detectors for high resolution room temperature X-ray spectroscopy", Nucl. Instr. & Meth. A, vol. 377, no.2-3, p.p. 346 – 351, 1996.

[34] E. Pinotti, H. Bräuninger, N. Findeis, H. Gorke, D. Hauff, P. Holl, J. Kemmer, P. Lechner, G. Lutz, W. Kink, N. Meidinger, G. Metzner, "The pn-CCD on-chip electronics", Nucl. Instr. & Meth. A, vol. 326, no. 1-2, pp. 85-91, 1993.

[35] C. Fiorini, P. Lechner, "Continuous charge restoration in semiconductor detectors by means of the gate-to-drain current of the integrated front-end JFET", IEEE Trans. Nucl. Sci., vol. 46 , no. 3, pp. 761 – 764, 1999. DOI: 10.1109/23.774174.

[36] Paolo Leutenegger, Josef Kemmer, Peter Lechner, Heike Soltau, Ulrich Weber, Lothar Strüder, Antonio Longoni, Carlo Fiorini, "Silicon drift detectors as radiation monitors for x rays, gamma rays, and particles", Proc. SPIE, vol. 4012, p.p. 579-591, 2000. DOI:10.1117/12.391595

[37] SGX Sensortech, available in: www.sgxsensortech.com.

[38] Peter Lechner, Werner Buttler, Carlo Fiorini, Robert Hartmann, Josef Kemmer, Norbert Krause, Paolo Leutenegger, Antonio Longoni, Heike Soltau, Diana Stoetter, R. Stoetter, Lothar Strueder, Ulrich Weber, "Multichannel silicon drift detectors for X-ray spectroscopy", Proc. SPIE, vol. 4012, p.p. 592 – 599, 2000.
doi: 10.1117/12.391596

[39] PNSensor, available in: www.pnsensor.de.

[40] S.I. Parker, C. J. Kenney, J. Segal, "3D- A proposed new architecture for solid-state radiation detectors", Nucl. Instr. And Meth. A, vol. 395, no.3, p.p. 328-343, 1997.

[41] Christopher Kenney, Sherwood Parker, Julie Segal, and Chris Storment, "Silicon Detectors with 3-D Electrode Arrays: Fabrication and Initial Test Results", IEEE Trans. Nucl. Sci., vol. 46, no. 4, p.p. 1224-1236, 1999.

[42] CERN, Radiation hard silicon detectors lead the way, available in:
http://cerncourier.com/cws/article/cern/28790

[43] Sherwood I. Parker and Christopher J. Kenney, "Performance of 3-D architecture silicon sensors after intense proton irradiation", IEEE Trans. Nucl. Sci., vol. 48, no. 5, p.p. 1629-1638, 2001.

[44] C.J. Kenney, S.Parker and E. Walckiers, "Results from 3-D silicon sensors with wall electrodes: near-cell-edge sensitivity measurements as a preview of active-edge sensors", IEEE Trans. Nucl. Sci., vol. 48, no. 6, p.p. 2405 – 2410, 2001. DOI: 10.1109/23.983250.

[45] C. DaVia, J. Hasi, C. Kenney, A. Kok, S. Parker, "3D silicon detectors - status and applications", Nucl. Instr. And Meth A, vol.549, no. 1-3, p.p. 122-125, 2005.

[46] Agata Sakic, "Silicon technology for integrating high-performance low-energy electron photodiode detectors" Ph.D. Thesis, Delft University of Technology, 2012.

[47] Francesco Sarubbi, "Characterization of Pure boron depositions integrated in Silicon diodes for nanometer-deep junction applications" Ph.D. Thesis, Delft University of Technology, 2010.

[48] Lis K. Nanver, "PureB silicon photodiode detectors for DUV/VUV/EUV light and low-energy electrons", Workshop, Next Generation UV Instrument Technologies Enabling Missions in Astrophysics, Cosmology and Planetary Sciences, California Institute of Technology, August 2011.

[49] F. Sarubbi, T. L. M. Scholtes, and L. K. Nanver, "Chemical vapor deposition of a-boron layers on silicon for controlled nanometer-deep p+njunction formation," J. Electron. Mater., vol. 39, pp. 162-173,2010.

[50] F. Sarubbi, L.K. Nanver, T.L.M. Scholtes "High Effective Gummel Number of CVD Boron Layers in Ultrashallow Diode Configurations", IEEE Trans. Electron Devices, vol. 57, no. 6, pp. 1269-1278, 2010.

[51] N. Sadeghi and S. Mirabbasi, "A technique for implementing monolithic resistors with near-zero temperature coefficient", 24th Canadian Conference on IEEE Electrical and Computer Engineering (CCECE), p.p. 001292 – 001295, 2011. DOI: 10.1109/CCECE.2011.6030672.

[52] S. Raetzke1 and J. Kindersberger, "Resistance to high voltage arcing and the resistance to tracking and erosion for silicone/sio2 nanocomposites", Proc. 16th Intern. Symp. on High Voltage Engineering, SAIEE 2009, pp. 1-6, 2009.

[53] J. Ninkovic, L. Andricek, C. Jendrisyk, G. Liemann, G. Lutz, H.-G. Moser, R. Richter, F. Schopper, "The first measurements on SiPMs with bulk integrated quench resistors", Proc. 12th International Vienna Conference on Instrumentation, vol. 628, no. 1, pp. 407–410, 2011.

[54] Y.S. Ho, Y.L. Hsu, C.C. Lan, Y.J. Tsai, C.W. Chen, S.R. Horng, Y.K. Fang, T.C. Hu, C.P. Liu, J.J. Huang, W.K. Yeh, "Mis-matching characteristics study of P^{+}-poly-silicon resistor in newly CMOS process technology', IEEE Electron Devices and Solid-State Circuits, pp.1133-1135, 2007. DOI: 10.1109/EDSSC.2007.4450328

[55] Huang, C , Buisman, K, Nanver, LK, Sarubbi, F , Popadic, M , Scholtes, TLM & Schellevis, H, "Ultra linear low-loss varactor diode configurations for adaptive RF systems", IEEE Trans. Microwave Theory and Techniques, vol. 57, no. 1, pp. 205-215, 2009.

[56] V. Mohammadi, W.B. de Boer, T.L.M. Scholtes, L.K. Nanver, Pattern dependency and loading effect of pure-boron-layer chemical-vapor deposition, ECS Journal of Solid State Science and Technology, vol. 1, no. 1, pp. Q16-Q20, 2012. DOI: 10.1149/2.024201jss

[57] S. B. Evseev, L. K. Nanver, S. Milosavljevic, "Ring-gate MOSFET test structures for measuring surface-charge-layer sheet resistance on high-resistivity-silicon substrates" , Proc. IEEE International Conference on Microelectronic Test Structures (ICMTS), pp. 3 - 8, Austin, USA, 2006.

[58] Glossary of Resistor Terminology ,Version 2010, Token ElectronicsIindustry Co., Ltd., avalble in: www.token.com.

[59] L.K. Nanver, A. Sammak, V. Mohammadi, K.R.C. Mok, L. Qi, A. Sakic, N. Golshani, J. Derakhshandeh, T.M.L. Scholtes, W.D. de Boer, Pure dopant deposition of B and Ga for ultrashallow junctions in Si-based devices, ECS Trans. 2012, vol. 49, no. 1, pp. 25-33, 2012.

[60] Agata Sakic, Gerard van Veen, Kees Kooijman, Patrick Vogelsang, Tom L. M. Scholtes, Wiebe B. de Boer, Jaber Derakhshandeh, Wim H. A. Wien, Silvana Milosavljevic, and Lis K. Nanver, "High-Efficiency Silicon Photodiode Detector for Sub-keV Electron Microscopy", IEEE Trans. Electron Devices, vol. 59, no. 10, pp. 2707 – 2714, 2012.

[61] Spiking and Epitaxial Si in Contact Holes, Kiel University, Germany, avalble in: http://www.tf.uni-kiel.de/en

[62] A. Šakic, V. Jovanovic, P. Maleki, T.L.M. Scholtes, S. Milosavljevic, L.K. Nanver "Characterization of amorphous boron layers as diffusion barrier for pure aluminium" , MIPRO 2010, Croatia, pp. 52-55., 2010.

[63] L.K. Nanver, L. Qi, V. Mohammadi, K.R.M. Mok, W.B. de Boer, N. Golshani, A. Sammak, T.L.M. Scholtes, A. Gottwald, U. Kroth, F. Scholze, "Robust UV/VUV/EUV PureB Photodiode Detector Technology with High CMOS Compatibility", IEEE Journal of Selected Topics in Quantum Electronics, vol. 20, no. 6, pp. 1-11, 2014.

[64] P. Maleki1, T.L.M. Scholtes, M. Popadić, F. Sarubbi, G. Lorito, S. Milosavljevic, W.B. de Boer, and L.K. Nanver, "Deep p+ junctions formed by drive-in from pure boron depositions", International Workshop on Junction Technology (IWJT), Shanghai, China, pp. 1–4, 2010.

[65] P. Lechner, C. Fiorini, R. Hartmann, J. Kemmer, N. Krause, P. Leutenegger, A. Longoni, H. Soltau ,D. Stötter, R. Stötter, L. Strüder, U. Weber, "Silicon Drift Detectors for high count rate X-ray spectroscopy at room temperature", 11th international workshop on room temperature semiconductor x- and gamma-ray detectors and associated electronics, Vienna, October 11-15, 1999.

[66] Chiara Guazzoni, " Development of Silicon Drift Detectors and recent applications" , Workshop of the Technology and Innovation Group of the European Physical Society "Advanced Radiation Detectors for Industrial Use" , Nov. 2013.

[67] A. Castoldi, C. Fiorini, C. Guazzoni, A. Longoni and L. Strüder , "Semiconductor Drift Detectors: Applications and New Devices", X-ray Spectrometry, Vol. 28, no. 5, pp. 312-316, 1999.

[68] M. Popp, R. Hartmann, H. Soltau, L. Struder, N. Meidinger, P. Holl, N. Krause and C. von Zanthier, "Modeling the energy response of pn-CCDs in the 0.2-10 keV band", Nucl. Instr. Meth. in phys. res A , vol. 439, no. 2, pp.567-574, 2000.

[69] Oxford-instruments brochure, "Silicon Drift Detectors Explained", available in: http://www.uni-export.com.pl/files/Akcesoria_analityczne/SDD_Explained.pdf.

[70] The Center for X-ray Optics: CXRO, available in: http://www.cxro.lbl.gov/.

[71] P. Rehak, E. Gatti, A. Longoni, M. Sampietro, P. Holl, G. Lutz, J. Kemmer, U. Prechtel and T. Ziemann, "Spiral silicon drift detectors", IEEE Nucl. Science Sumposium, Nov. 1988.

[72] C. Guazzoni, "Front-end Electronics and Signal Processing – I", II Regional ICFA Instrumentation School – Istanbul, September 2, 2005. available in:
http://indico.cern.ch/event/a055742/material/0/1?contribId=s0t4&sessionId=s0

[73] G. Bertuccio, A. Pullia, A, "A method for the determination of the noise parameters in preamplifying systems for semiconductor radiation detectors", Review of Scientific Instruments, vol. 64, no. 11, pp.3294-3298, Nov. 1993.

[74]S.M. Sze: "Semiconductor devices- Physics and technology", Johan Wiley & Sons, New York, 1985.

[75] Amporn Poyai, E. Ratanaudomphisut, J. Supadech, N. Klunngien, C. Hruanan and S. Sophitpan, "Improving Sensitivity of p-n Junction Temperature Sensor by Carrier Lifetime Modification", Advanced Materials Research vols. 55-57, pp. 517-520, 2008.

[76] R. Hartmann, D. Hauff, S. Krisch, P. Lechner, G. Lutz, R.H. Richter, H. Seitz, L. Struder, G. Bertuccio, L. Fasoli, C. Fiorini, E. Gatti, A. Longoni, E. Pinotti, M. Sampietro, "Design and test at room temperature of the first silicon drift detector with on-chip electronics", IEEE Electron Devices Meeting (IEDM), p.p. 535 - 538, San Francisco, CA, USA, 94. DOI: 10.1109/IEDM.1994.383351.

[77] Pasi Kostamo, "Leakage current collection structure and a radiation detector with the same", Patent EP2677345 A2,

[78] W. Chen, H. Kraner, Z. Li, P. Rehak, G. Bertuccio, E. Gatti, A. Longoni, M. Sampietro, P. Holl, J. Kemmer, U. Faschingbauer, F. Hess, C. Jacob, A. Wörner, J.P. Wurm, R. Baur, A. Drees, P. Fischer, P. Glässel, T.F. Günzel, D. Irmscher, et al, "Performance of the multianode cylindrical silicon drift detector in the CERES NA45 experiment : first results", Nucl. Instr.and Meth. A, vol. 326, no. 1-2, p.p. 273-278, 1993.

[79] D.M. Schlosser, P.Lechner, G.Lutz, A.Niculae, H.Soltau, L.Struder, R.Eckhardt, K.Hermenau, G. Schaller, F.Schopper, O.Jaritschin, A.Liebel, A.Simsek, C.Fiorini, A.Longoni, "Expanding the detection efficiency of silicon drift detectors", Nucl. Instr. and Meth. A, vol. 624, p.p. 270–276, 2010.

[80] J.S. Iwanczyk, B.E. Patt, J. Segal, J. Plummer, G. Vilkelis, B. Hedman, K.O. Hodgson, A.D Cox, L.Rehn, J. Metz, "Simulation and modelling of a new silicon X-ray drift detector design for synchrotron radiation applications" , ELSEVIER, NIMA, vol.380, p.p. 288- 294, 1996.

[81] J.T. Walton, B. Krieger, D. Krofcheck, R. Odonnel, G. Odyniec, M. D. Partlan, and N.W. Wang, "P-Type Silicon Drift Detectors" , 7th European Symposium on Semiconductor Detectors, Germany, 1995.

[82] M. Krammer, "Silicon detectors", available in:
http://fisica.cab.cnea.gov.ar/particulas/html/icfa/wiki/images/3/32/Krammer02.pdf

[83] R.Alberti, S.Buzzetti, C.Fioni, C.Guazzoni, T.Klatka, P.Lechner, A.Longoni, L.Struder, "Advanced monolithic arrays of Silicon Drift Detectors for elemental mapping applications" , SNIC symposium,Stanford, California – 2006.

[84] C. Fiorini ,A. Longoni, "Semicon ductor drift detectors for X- and gamma-ray spectroscopy and imaging" , 9th European Conference on Accelerators in Applied Research and Technology, vol. 266, no. 10, p.p. 2173–2181, 2008.

[85] Negin Golshani, Jaber Derakhshandeh, Agata Sakic, Lis Nanver, "Silicon Drift Detectors for the detection of x-rays down to energies as low as 100 eV", Micro Nano conference, Ede, The Netherlands, Dec.2013.

[86] Learn about-Electronics-Transistors, available in: www.learnabout-electronics.org/fet_02.php

[87] VLSI design lectures, available in: http://www.eet.bme.hu/~benedek/Vlsi_Design/Lectures/

[88] A. Niculae, P. Lechner, H. Soltau, G. Lutz, L. Strüder, C. Fiorini, A. Longoni, “Optimized readout methods of silicon drift detectors for high-resolution X-ray spectroscopy”, Nuclear Instruments and Methods in Physics Research Section A (NIM A), vol. 568, no. 1, p.p. 336–342, 2006. DOI: 10.1016/j.nima.2006.06.025

[89] M. Sampietro, L. Fasoli, E. Gatti, C. Guazzoni, A. Fazzi, P. Lechner, J. Kemmer, D. Hauf, L. Struder, “Bipolar feedback transistor integrated on detector with JFET for continuous reset”, Nuclear Instruments and Methods in Physics Research. Section A, vol. 439, no. 2-3, P.P. 368-372, 2000.

[90] L. Strüder, N. Meidinger, D. Stotter, J. Kemmer, P. Lechner, P. Leutenegger, H. Soltau, F. Eggert, M. Rohde, T. Schulein, “High-Resolution X-ray Spectroscopy Close to Room Temperature”, journal of Microscopy and Microanalysis - Microsc Microanal., vol. 4, no. 06, pp. 622-631, 1998.

[91] Book: “Theory of XRF - Getting acquainted with the principles”, Peter Brouwer, 3rd edition, 2010, ISBN: 90-9016758-7.

[92] Amptek, “Silicon Drift Detector (SDD) XR-100SDD”, available in: http://www.amptek.com/pdf/sdd.pdf

[93] E. Gatti and P. F. Manfredi, “Processing the signals from solid-state detectors in elementary-particle physics,” Riv. Nuovo Cimento, vol.9, no. 1, 1986.

[94] E. Gatti, A. Longoni, and M. Sampietro, “New developments in solid state detectors,” in Solid State Devices, G. Soncini and P. V. Calzolari, pp. 497-509, Eds Amsterdam: North Holland, 1987.

[95] P. Rehak, S. Rescia, V. Radeka, E. Gatti, A. Longoni, M. Sampietro, G. Bertuccio, P. Holl, L. Strüder, J. Kemmer, U. Prechtel, T. Ziemann, “Feedback charge amplifier integrated on the detector wafer”, Nuclear Instruments and Methods in Physics Research Section A, vol. 288, no. 1, pp. 168-175, 1990.

[96] Book: “Solid state electronic devices”, Ben G. Streetman and Sanjay Banerjee, 5th edition, 2000.

[97] On-board electronics for X-ray detectors, available in:
http://home.deib.polimi.it/sampietr/Ratex/RATEX1.html.

[98] A. Fazzi, P. Jalas, P. Rehak, P. Holl, “Charge-sensitive amplifier front-end with an nJFET and a forward-biased reset diode”, IEEE Transactions on Nuclear Science, vol. 43, no. 6, pp. 3218-3222, 1996. DOI: 10.1109/23.552721

[99] C. Guazzoni, M. Sampietro, A. Fazzi, P. Lechner, “Embedded front-end for charge amplifier configuration with sub-threshold MOSFET continuous reset”, IEEE Transactions on Nuclear Science - IEEE Transactions on Nuclear Science, vol. 47, no. 4, pp. 1442-1446, 2000. DOI: 10.1109/23.872993.

[100] Marco Sampietro, Chiara Guazzoni, Hermes Cruciata, Peter Lechner, “Experimental behavior of a two-chip charge amplifier for high-stability spectroscopy systems”, IEEE Transactions on Nuclear Science, vol. 48, no. 4, pp. 1229-1233, 2001. DOI: 10.1109/23.958756.

[101] Kevin F. Brennan, “Introduction to semiconductor devices”, first edition, 2005, page 57.

[102] Marius Grundmann, “The physics of semiconductors: An Introduction Including Nanophysics and Applications”, 2nd Edition, 2010, page 455.

[103] Bart Van Zeghbroeck, "Principles of Semiconductor Devices", available in: http://ecee.colorado.edu/~bart/book/book/title.htm

[104] R. Victor Jones, "Electronic Devices and Circuits", available in: http://people.seas.harvard.edu/~jones/es154/lectures/lecture_2/breakdown/breakdown.html

[105] Otwin Breitenstein, Jan Bauer, Karsten Bothe, Wolfram Kwapil, Dominik Lausch, Uwe Rau, Jan Schmidt, Matthias Schneemann, Martin C. Schubert, Jan-Martin Wagner and Wilhelm Warta, "Understanding junction breakdown in multicrystalline solar cells", Journal of applied physics, vol. 109, no. 7, 2011.

[106] R. K. Willardson and Albert C. Beer, "Semiconductors and semimetals" , Volume 4, page 316, 1968.

[107] Sudha Mahadevan, S. M. Hardas and G. Suryan,"Electrical breakdown in semiconductors", phys. Stat. Sol., vol. 8, no. 2, page 335, 1971.

[108] Dominik Lausch, Kai Petter, Holger von Wenckstern and Marius Grundmann, "Correlation of pre-breakdown sites and bulk defects in multicrystalline silicon solar cells", physica status solidi (RRL)-Rapid Research Letters , vol.3, no. 2-3, pp. 70-72, 2009. DOI: 10.1002/pssr.200802264.

[109] Dragomirescu, G Charitat, "Improving the dynamic avalanche breakdown of high voltage planar devices using semi-resistive field plates", Microelectronics Journal, vol. 32, Issues 5–6, pp. 473–479, 2001.

[110] V.A.K. Temple, "Junction termination extension (JTE), A new technique for increasing avalanche breakdown voltage and controlling surface electric fields in P-N junctions", International Electron Devices Meeting (IEDM), vol. 23, p.p. 423 – 426, 1977. DOI: 10.1109/IEDM.1977.189277

[111] Dev Alok, B. Jayant Baliga, "SiC device edge termination using finite area argon implantation" IEEE Transactions on Electron Devices, vol. 44, no.6, p.p. 1013-1017, 1997. DOI: 10.1109/16.585559.

[112] Adler MS, Temple VAK, Ferro AP, Rustay RC., "Theory and breakdown voltage for planar devices with a single field limiting ring", IEEE Transactions on Electron Devices, vol. 42, no.2, p.p. 107-113, 1977. DOI: 10.1109/T-ED.1977.18688.

[113] B. Jayant Baliga, "Power semiconductor devices", PWS Publishing Company, 1995.

[114] Bradley E. Patt, Sherman Oaks; Jan S.Iwanczyk, Los Angeles; Carolyn R.Tull, Orinda; Gintas Vilkelis, WestlakeVillage, "Semiconductor radiation detector", Patent no. US 6,455,858 B1, 2002.

[115] Peter Lechner, Gerhard Lutz and Lothar Strueder, "Semiconductor detector with optimised radiation entry window", Patent no. US 7105827 B2, 2006.

[116] Jason Henning, Qingchun Zhang, Sei-Hyung Ryu, "Junction termination structures including guard ring extensions and methods of fabricating electronic devices incorporating same", Patent no. US 8803277 B2, Aug. 2014.

[117] M. Da Rold, N. Bacchetta, D. Bisello, A. Paccagnella, G.-F. Dalla Betta, G. Verzellesi, O. Militaru, R. Wheadon, P.G. Fuochi, C. Bozzi, R. Dell'Orso, A. Messineo, G. Tonelli, P.G. Verdini, "Study of breakdown effects in silicon multiguard structures", IEEE Transactions on Nuclear Science, vol.46, no.4, p.p. 1215-1223, 1999.

[118] B. J. Baliga, "Modern power devices", New York:Wiley, 1987, pp.62-100

[119] Berit Sundby Avseta, Lars Evensen, “The effect of metal field plates on multiguard structures with floating p+ guard rings”, Nuclear Instruments and Methods in Physics Research Section A, vol. 377, no. 2–3, pp.397–403,1996.

[120] A. Bischoffa, N. Findeis, D. Hauff, P. Holl, J. Kemmer, P. Klein, P. Lechner, G. Lutz, R.H. Richter, L. Struder, “Breakdown protection and long-term stabilisation for Si-detectors”, Nucl. Instrum. Methods Phys. Res., vol. 326, no. 1-2, pp. 27-37, 1993.

[121] L. Evensen and A.Hanneborg, “Guard ring design for high voltage operation of silicon detectors”, Nucl. Instrum. Methods Phys. Res., vol. A337, pp. 44-52, 1993.

[122] Negin Golshani, Jaber Derakhshandeh, C.I.M Beenakker, R. Ishihara, “High-Ohmic resistors fabricated by PureB layer for silicon drift detectors applications”, Journal of Solid-State Electronics, vol. 105, p.p. 6-11, 2015. DOI:10.1016/j.sse.2014.11.022.

[123] B. Jayant Baliga, “Closed-form analytical solutions for the breakdown voltage of planar junctions terminated with a single floating field ring”, Solid-State Electronics, vol.33, no 5, pp. 485–488, 1990.

[124] Negin Golshani, C.I.M Beenakker, R. Ishihara, “Manufacturing uniform field silicon drift detector using double boron layer”, accepted for publication in Nucl. Instr. and Meth. in Phys. Res. A, 2015.

[125] J. Derakhshandeh, N. Golshani, L.A. Steenweg, W. van der Vlist, L.K. Nanver, “A novel silicon interposer for measuring devices requiring complex two-sided contacting”, IEEE International Conference on Microelectronic Test Structures (ICMTS), Osaka, pp. 43-46, 2013. DOI: 10.1109/ICMTS.2013.6528143.

[126] G. Vanstraelen, K. De Backker, I. Debusschere, C. Claeys, G. Declerck, “Generation lifetime monitoring on high resistivity silicon using gated diodes” Nucl. Instr. and Meth. A, vol. 288, no. 1, p.p. 48-53, 1990.

[127] Dieter K.Schroder, “Semiconductor Material and Device Characterization”, John Wiley & Sons, New York, 1998.

[128] G. Verzellesi, G.-F. Dalla Betta, M. Boscardin, G.U. Pignatel, L. Bosisio, “Extraction of bulk generation lifetime and surface generation velocity in high-resistivity silicon by means of gated diodes”, Nuclear Instruments and Methods in Physics Research A, vol. 477, no.1-3, p.p. 220–225, 2002.

[129] “SDD laboratory measurement” availble in: http://ojs.ujf.cas.cz/~skushpil/measur.html

[130] lezioni_SDD.ppt, “A Silicon Microstrip System equipped with the RX64DTH ASIC PPT- The most complex Silicon Detectors: Silicon Drift! ”, available in: http://www.to.infn.it/~beole/ppt/lezioni_SDD.ppt.

[131] W. Chen, G.A. Carini, G.De Geronimo, J. Fried, J.A. Gaskin, J.W. Keister, Z.Li, B.D. Ramsey, P. Rehak, D.P. Siddons, “Development of Thin-Window Silicon Drift Detector for X-ray spectroscopy”, IEEE Nucl. Science Symposium Conference Record (NSS), vol. 3, p.p.1954 – 1959, 2007. DOI: 10.1109/NSSMIC.2007.4436537.

[132] N. Golshani, V. Mohammadi, S. Ramesh and L.K. Nanver, “High-Ohmic Resistors using Nanometer-Thin Pure-Boron Chemical-Vapour-Deposited Layers”, 43rd European Solid-State Device Research Conference (ESSDERC), Bucharest, Romania, pp. 210-213, Sep. 2013. DOI: 10.1109/ESSDERC.2013.6818856.

List of symbols and abbreviations

List of Abbreviations

BJT	Bipolar Junction Transistor
CCD	Charge Coupled Device
CCE	Charge Collection Efficiency
CPA	Charge sensitive PreAmplifier
ENC	Equivalent Noise Charge
FBJ	Forward Biased Junction
FWHM	Full Width at Half Maximum
FZ	Float Zone
EBIC	Electron Beam Induced Current
JFET	Junction Field Effect Transistor
LPCVD	Low Pressure Chemical Vapour Deposition
MLSDD	Multi-Linear Silicon Drift Detector
MOS	Metal-Oxide-Semiconductor (usually Silicon)
MOSFET	Metal-Oxide-Silicon Field Effect Transistor
NTD	Neutron Transmutation Doped
PECVD	Plasma Enhanced Chemical Vapour Deposition
RT	Room Temperature
RTA	Rapid Thermal Annealing
SDD	Silicon Drift Detector
SF	Source Follower
SNR	Signal to Noise Ratio
PMT	Photo Multiplier Tube
SPD	Silicon Pixel Detector
SEM	Scanning Electron Microscope
XRF	X-ray Fluorescence analysis
HRS	High Resistivity Silicon wafer
SD^3	Silicon Drift Detector Droplet
CVD	Chemical Vapor Deposition
HRTEM	High-Resolution Transmission Electron Microscopy
SIMS	Secondary Ion Mass Spectrometry
VCR	Voltage Coefficient of the Resistor
TCR	Temperature Coefficient of the Resistor
DUV	Deep-UV (350-190 nm)
EUV	Extreme-UV (100-10 nm)
VUV	Vacuum-UV (200-10 nm)
EHP	Electron-Hole Pairs
MCA	Multi-Channel Analyzer
TSV	Through silicon via
DRIE	Deep reactive ion etching
DUT	Device under test
BHF	Buffered hydrofluoric acid
ADC	Analog to digital converter
JTE	Junction termination extensions

List of Selected Symbols

Symbol	Description	Unit
ε_{ox}	SiO2 dielectric permittivity ($\varepsilon_{ox} = 3.4\times10^{-13}$ F/cm)	F/cm
ε_{Si}	Silicon dielectric permittivity ($\varepsilon_{Si} = 1.0\times10^{-12}$ F/cm)	F/cm
μ	Carrier mobility, channel carrier mobility	cm^2/(V.s)
v_{th}	Thermal velocity	cm/s
ρ	Silicon density (ρ = 2.33 g/cm^3)	g/cm^3
ρ_S	Sheet resistance	Ω/□
σ	Standard deviation of Gaussian shaped electron cloud	μm
τ	Time parameter of the shaping filter (usually equal to shaping time)	μs
τ_g	Generation lifetime of e-h pairs	ms
τ_r	Recombination lifetime of minority carriers	ms
A	Detector area	cm^2
$A1, A2, A3$	Shaping constants	
A_g	Gate area (MOS capacitor or gated diode)	cm^2
A_s	Surface area covered with oxide	cm^2
C_D	Detector capacitance	F
C_{GD}, C_{GS}	Gate-drain and gate-source capacitance	F
C_{fb}	Feedback capacitance	F
C_{FET}	JFET input capacitance	F
C_{stray}	Stray capacitance of connections	F
C_T	Total capacitance	F
d	Wafer thickness	μm
d_{ox}	Thickness of the SiO_2 layer	nm
E	Photon energy	eV
E_d	Drift field	V/cm
E_g	Bandgap energy ($E_g \sim 1.12$ eV for Si at RT)	eV
ENC	Equivalent noise charge	rms el.
f	Frequency	Hz
F	Fano factor	
$FWHM$	Energy resolution expressed as Full Width at Half Maximum	eV
g_m	Transconductance of the ideal JFET	mS
I_{bulk}, I_{surf}	Bulk and surface leakage current	A
I_{diff}	Diffusion leakage current	A
I_{gate}	Gate leakage current	A
I_L	Leakage current	A
k	Boltzmann constant ($k = 1.381\times10^{-23}$ J/K)	J/K
L	Channel length	μm
L_e, L_h	Electron and hole diffusion length	m
n	Electron distribution	cm^{-3}
n_i	Intrinsic carrier concentration	cm^{-3}
N_A	Doping concentration of the p-doped region	cm^{-3}
N_{ch}	Channel doping	cm^{-3}
N_D	Doping concentration of the n-doped region	cm^{-3}
N_{fo}	Density of fixed oxide charge	cm^{-2}
N_{it}	Concentration of surface trapping centers	cm^{-2}
N_{ox}	Oxide charge density	cm^{-2}
q	Elementary charge ($q = 1.6\times10^{-19}$ C)	C
R_{count}	Peak-to-background ratio	
R_{ch}	Channel resistance	Ω
R_L	Load resistance	Ω
s_g	Surface generation velocity	cm/s

List of symbols and abbreviations

Symbol	**Description**	**Unit**
t	Time	s
T	Absolute temperature	K
V	Potential	V
V_{bd}	Breakdown voltage	V
V_{bi}	Built-in potential	V
V_{GS}, V_{DS}	Gate-source and Drain-source bias	V
V_{fb}	Flat-band voltage	V
V_{sat}	Saturation voltage	V
W	Channel width	μm
W	Mean e-h pair creation energy, (W = 3.65 eV in Si at RT)	eV
W_{depl}	Thickness of the depletion layer	μm
Wg	Gate depletion width (MOS capacitor or gated diode)	μm

Summary

Development of Silicon Drift Detectors using Boron layer technology

Radiation detectors are used in a large variety of fields such as medicine, security, defense, geophysics, industry and physics. They have been developed to detect the energy or position of radiation or charge particles.

In **Chapter 1** several X-ray detectors were introduced briefly. In gas filled X-ray detectors, incoming photons ionize inert gas and create electron and ions which can be collected at a thin wire anode inside of the chamber. The advantage of this type of detector is the possibility to amplify the signal or charge, hence a high signal to noise ratio. However, they suffer from low efficiency for X-ray detection due to low density of the filled gas. In scintillation detectors, X-ray photons collide with the scintillator and create UV or visible light which can be converted into an electrical signal by a photodiode. The main disadvantage of scintillation detectors is their poor energy resolution due to a large amount of loss, and the relatively high ionization energy, i.e. 20-500eV. In semiconductor detectors, electron and hole pairs (EHPs) can be generated at much lower energies than gas filled detectors. The possibility to measure both position and energy of incoming radiation accurately is a unique property for semiconductor detectors. However, they do not have any intrinsic signal gain, as is the case in gas filled detectors. Therefore an integrated or external amplifier is required for this type of detector. When selecting semiconductor materials, higher density, a higher atomic number for better absorption efficiency, lower bandgap for better resolution, higher mobility for fast detection beside lower leakage current, and a thicker substrate should be considered. Among different semiconductor materials, silicon is an

interesting material for X-ray detectors because of the availability of fabrication process technology, lower cost and possibility to integrate advanced electronic circuits and further signal processing. PIN photodiodes made in a high resistivity silicon substrate are the simplest, cheapest, commercially available type of X-ray detectors where the full thickness of silicon is depleted by reverse bias to extract the generated EHPs with radiation. However, PIN detectors have a large anode area which makes the output capacitance so large that higher noise level in the output is the result. In Si(Li) and Ge(Li) detectors, crystals of silicon or germanium are used with thicknesses in the range of a few mm to cm. To obtain intrinsic material (concentration levels as low as 10^9 cm^{-3}) for complete thickness, a Li drifting process is used where Li acts as a donor to compensate acceptor ions. The typical biasing voltage is 500V to 4000V. In order to prevent redistribution of the Li atoms, the detector has to be kept at a low temperature with liquid nitrogen, which is the main disadvantage for this type of detector. Silicon strip detectors offer 2D position sensitive detection. They are similar to PIN diodes, but the p^+ region is divided into many strips on the front side to collect the holes, and the n^+ region is divided into many n^+ strips on the backside to collect the electrons. In silicon pixel detectors (SPDs) only one side of p^+n is patterned and every pixel has its own readout electronics attached to the pixel by solder bumping. In p-n CCDs the drift function is carried out by reverse and forward biases of p-n junctions in periodic cycles by external pulses acting as series of shift registers drifting the electrons toward the anode. Silicon drift detectors (SDDs) are detectors with an extremely small anode and low output capacitance, thus less noise and high energy resolution. In a circular configuration the p^+ drift rings create an electric field parallel to the surface to collect the electrons in the small anode region. Independent of the active area of the detector, a typical output capacitance of an SDD is in the range of 60fF. On-chip electronic devices are placed on the front side to amplify the signal. In the Silicon Drift Detector Droplet (SD^3) the anode and integrated transistor are moved to the margin of the structure where they can be shielded from direct radiation by a proper collimator. This has a significant effect on the low energy background in the SDD. With the SD^3 the peak/background ratio is increased from 3000 to 5000. Multichannel SDDs consist of many single SDDs with individual readout but a common

entrance window, guard ring and supply voltage where the sensitive area is very big, up to few cm^2, without losing the energy resolution and count rate capability of the single SDD. Finally in 3D detectors implanted electrodes of conventional SDD are replaced with a 3D array of p+ and n^+ electrodes inside the silicon. In 3D detectors collection distances and times are about one order of magnitude less than planar strips and pixel detectors, and the depletion voltage is about two orders of magnitude lower. However, the fabrication process is complex and expensive.

In **Chapter 2** the properties of the boron layer were described in detail. A boron layer is deposited in an ASM Epsilon reactor using Diborane (B_2H_6) and Hydrogen as a dopant gas and carrier gas at temperatures ranging from 500°C to 700°C. The typical thickness of the boron layer deposited at 700°C for a 7min deposition time is equal to a 2-3nm uniform layer. Deposition at lower temperatures results in a non-uniform boron layer which is confirmed by TEM analysis. Fabricated PureB diodes behave like a conventional deep p^+-n junction with near ideal ideality factors lower than ≈ 1.02, and low saturation current. Resistors are key elements in integrated circuits and can be made with a p-n junction or by poly silicon deposition. However, drawbacks for these two technologies are bias dependence, high parasitic capacitance for high Ohmic values in junction made resistors, and large variation and process dependency for poly-made resistors. The typical sheet resistance value of the deposited boron layer is in the 100k**Ω**/□ range which can be changed by deposition time, temperature and annealing. In this thesis, the photodiodes were fabricated on high-resistivity Si (HRS) <100> wafers, n-type phosphorous-doped to 2-10kΩ-cm. The resistors were also placed directly in the HRS so that associated depletion layers were tens of microns wide even at 0V biasing. Thus the voltage dependence of the resistance value is negligible. The fabrication process consisted of oxidation followed by etching, boron layer deposition and finally metallization. To remove Al from the top of the boron layer, a combination of dry etching and short wet etching in diluted HF was used. The sheet resistance values extracted from measurement of the ring structures are 2.5×10^4 **Ω**/□ for a 7min 700°C deposition and 3.8×10^5 **Ω**/□ for a 20min 500°C deposition. Fabricated resistors show high

linearity in voltage ranges between 10V and 100V and are stable in temperature ranges from 15°C to 95°C. The 500°C resistors have a TCR (temperature coefficient of the resistor) less than 200ppm/°C up to a measurement temperature of 70°C, then increasing to around 1000ppm/°C at 95°C. The TCR of the 700°C sample had an almost constant value of less than 400 ppm/°C over the whole measurement temperature range. The measured leakage current was less than 1nA/cm^2 at 10V reverse bias over all dies of the 100mm wafer. The measured resistor tolerance was in the range of 1% to 5% for both kΩ and MΩ resistors.
Since Pure Al can short the shallow junctions to bulk especially when the boron layer is deposited at lower temperatures (non-uniform boron layer) or when there is a defect on the substrate, an alloy of AlSi (1% Si) is used. However, removing AlSi with a wet process is not compatible with the boron layer process. Therefore it is better to add a diffusion barrier layer between the Al and boron layer. Among different studied diffusion barrier layers such as Ti, TiN, AlN and ZrN, only ZrN showed better process compatibility and no influence on the electrical performance of the detectors. Optical and SEM inspections show a defect-free detector surface when using 10nm ZrN between the Al and boron layer for both the 700°C and 500°C deposited layers. As an alternative, a lift-off process was developed to prevent any Al residuals on the boron layer. After PureB layer deposition at 700°C or 500°C, a negative photoresist (AZ®nLOF) was applied and patterned followed by 400nm-thick Al layer deposition by evaporation. Then the resist was stripped in acetone or a NMP solution in an ultrasonic bath. For both PureB layers deposited at 700°C or 500°C, the lift-off process was successfully performed. However, the limitation of Al thickness and the deposition method (evaporation) can be a challenge for some applications.

In **Chapter 3** the working principle of SDDs was reviewed. They have a higher count rate and better energy resolution with respect to other X-ray detectors. In order to have a successful working detector, different aspects of SDDs must be selected, designed and simulated carefully. The starting material for SDDs is high-Ohmic silicon wafers due to a better carrier lifetime (in the order of milliseconds) and lower required voltage for full depletion. To obtain better wafer uniformity typically wafers are made with the Neutron Transmutation Doped (NTD) method

where uniformity of the phosphorus doping is achieved by exposing an ingot of high-purity silicon to a uniform flux of thermal neutrons. For detection of higher energies, thicker wafers should be used. Furthermore, a <100> silicon substrate has a higher charge collection efficiency (CCE) of soft X-rays (below 200nm wavelengths) and has a lower surface leakage current compared to the <111> orientation. The entrance window of the detector determines the lowest energy the detector can detect. In SDDs the entrance window is kept in a vacuum by using Beryllium or polymer windows. Those windows can limit the lower range of detectable X-rays. In TEM systems a very high vacuum condition exists, thus those windows are not required. Therefore the lower detectable range can be reduced. In order to detect even lower X-rays energies (few hundred eVs), the dead layer of the p^+ region in the entrance window should be as thin as possible, i.e. a shallow junction is required. A typical dead layer of 40nm by implantation is reported. To keep full depletion in the center of detector, the entrance window is biased at V_{dep} which corresponds to a depletion voltage of the full wafer thickness. In the outer drift ring the applied voltage is equal to $2V_{dep}$ to ensure enough drift potential for the electrons towards the anode. Leakage current is a very important parameter in the SDDs which defines noise level. Bulk leakage current can be reduced by selecting a high quality wafer and lowering the process temperature. Surface generation leakage current can originate from processing defects and interface states generated in the bandgap region near the surface by abrupt discontinuity in the silicon interface. A sink anode is a structure to reduce the surface leakage current by providing a path to drain away the surface electrons through the p^+ field electrodes. In order to improve the energy resolution as much as possible, total capacitances including anode capacitance and stray capacitance (connection path to the external circuit), should be equal to the input capacitance of the external amplifier. A guard ring structure maintains low leakage current for the SDD without any breakdown at high voltage biases for depletion and drift mechanisms. The entrance window can be made from a PureB layer which has only a 2nm-thick dead layer for the p^+ layer. Therefore measuring lower energies (as low as 100eV) should be possible. Furthermore, PureB made resistors can be used as voltage dividers in the drift region of the detectors. A continuous layer of boron can act as a distributed resistor to drift the electrons toward the anode.

However, calculations and simulations showed one layer of boron cannot generate enough electric field to drift the electrons. The inner part has a higher resistance than outer part; therefore the electric field is concentrated only in the center of the detector and there is no force on the electrons to drift them to the anode. For the designed detector with an inner radius of 135µm and outer ring radius of 3135µm using the boron layer with a sheet resistance value of $10^5\Omega/\square$, the total resistance between the contact pads is equal to 50k**Ω**. Yet 95% of this value is concentrated only in a 135µm to 500µm region of the detector. The electric field is around three orders of magnitude less in the outer ring thus it is only effective at the inner side of the detector; there is not enough electric field to move the electrons toward the anode in the outer sides of the detector. Potential distribution shows at a 40V applied voltage, electrons will be accumulated in the gutter, the minimum of the potential energy, and will be moved slowly to the anode. At 160V, the drift voltage slope along the detector surface is lightly sharper than the 40V case but still too small to drift the electrons toward the anode. Therefore around 80% of the drift area has an almost zero electric field. However, a dual boron layer with two different sheet resistances and a special design can create a constant electric field in the drift region while the leakage current is still low. In this design the whole surface covered with two layers of boron to have minimum leakage current where the low sheet resistance layer is denser near the anode, and the high sheet resistance layer is denser in the outer rings to produce a constant resistance and electric field over the drift area.

Chapter 4 describes designing a guard ring structure and integrating an on-chip amplifier for SDDs where there is no multiplication mechanism. Consequently an on-chip or off-chip amplifier is necessary. With on-chip amplification, undesirable interference effects related to wire bonding, such as stray capacitance and microphonic noise, can be avoided. To select the type of transistor for the SDD, a JFET is preferred because of noise considerations. Bipolar transistors have higher shot noise and CMOS transistors have a higher 1/f noise component. In designing the JFET there is a trade-off between obtaining minimum noise and minimum capacitance while keeping the transconductance (g_m) as high as possible. Gate capacitance plays an important role in this trade-off. Since mobility

of an nFET is higher, it offers a higher cut-off frequency than a pFET. For optimum SDD resolution, input capacitance of the JFET is equal to detector's capacitance. In a SDD typically the JFET is placed inside the anode, which is isolated by a p-type region. The anode is connected to the gate, in the common source configuration the drain is connected to the power supply, and the source is connected to the external circuit. Accumulated charges on the anode can be discharged by reset devices such as a diode, JFET or MOSFET. Availability of technology and layout compatibility, minimum added noise and maximum linearity determine the choice of the reset transistor. In this thesis two types of on-chip JFET structures with a 4.5µm gate length together with different reset devices were designed for SDDs. The reset devices were embedded either in the JFET or in the small anode region. The parasitic capacitor between the detector anode and the transistor guard ring can act as a feedback capacitor. In the fabrication process flow, in order to find the optimum implantation parameters (energy and dose) for the gate (p^+), S/D (n^+) and deep n- and deep p-regions, two different routes were investigated. For gate doping, a combination of boron implantation and boron layer deposition was used.
Moreover in this chapter designing multi-guard ring structures was discussed. According to electrical measurements at different temperatures, a positive temperature coefficient for the breakdown voltage was found, which means the breakdown mechanism is an avalanche type. To prevent breakdown, several multi-guard ring structures were studied. Multi-guard ring structures consist of a conventional large p-type guard (240µm width), a series of intermediate concentric circular p-type guard rings (with different pitches, widths and metal overlap of the field plate), and a large n^+-type guard (150µm width) near the scribing line. The function of the n+ guard ring is to shield any existing positive charges in the oxide and prevent extension of depletion region toward the dicing line. As a result, the leakage current drops significantly. In this structure, parameters such as gap size, oxide charge, bulk doping concentration and field plate (metal extension) design have influence on the potential distribution of the guard rings. One of the designed structures works up to the limit of the measurement systems (1100V) with very low leakage current in the range of 1.5-3nA/cm^2. In this structure the width of the guard rings was 25µm, the first gap

(between the large guard and first intermediate guard ring) was 35μm, and the pitch was 80μm for the rest of the rings, with an inward field plate extending 5-30μm. Other structures show a roughly 400V breakdown voltage. According to the measurements of different designed guard ring structures, a gap of around 40μm is an optimal value for the distance between the large guard ring and first ring of the multi-guard structure. Moreover, it was found that a field plate in the inward direction offers a higher breakdown voltage because of charge shielding.

In **Chapter 5** the fabrication process and characterization results of SDDs were discussed. Since processing is performed on both sides of the wafers, special care should be considered during the processing steps such as wafer handling, implantation and wet etching in order to prevent any damage to the other side of the wafer. Furthermore, since the carrier lifetime is very important in SDD performance, high temperature processing steps should be avoided as much as possible. Therefore activation of dopants, particularly in case of JFET integration, at lower temperatures can be a challenge. In general a typical fabrication process flow starts with dry oxidation followed by guard ring and anode implantations by boron and phosphorous dopants. The next step is TEOS oxide deposition and annealing. Then the oxide layer is etched to open the regions for boron deposition to create p^+ regions. Boron deposition is selective which means it deposits only on silicon. Al metallization on both sides is the next step. In order to etch Al and expose the boron layer a combination of dry (keeping the dimensions same as the design) and wet etching in diluted HF (to land on the boron layer without damaging it) is performed. Alloying in forming gas is the last step to create Ohmic contact of doped silicon with Al. For the double boron layer process flow, two reticles (litho steps) are used before boron deposition. Using the first litho step, oxide was etched in the drift region to leave a 30nm-thick oxide. With the second litho step, a 30nm-thick oxide was etched from low sheet resistance areas. A low sheet resistance boron layer was deposited and followed by a 10sec BHF step to etch a 30nm-thick oxide from the rest of drift region. The previously deposited boron layer is not attacked by this short BHF step. At the end, high sheet resistance boron layer was deposited. In the process flow for JFET integration there are several implantation steps for deep p, deep n, S/D and gate regions.

Fabricated wafers were subjected to electrical measurement to characterize the wafer quality and fabricated SDDs. Measurement and calculation of the doping profile from CV curves result in 144.5μm and 217.5μm depletion depths on the entrance window side and device side of the silicon wafer, respectively. This measurement reveals that the entrance window (front side) of the wafer has a lower resistivity than the device side (backside). Knowledge of the bulk generation lifetime (τ_g) and surface generation velocity (s_g) of the wafer is essential for process control and radiation-damage monitoring in radiation detectors. Using the designed gated diode structures, τ_g and s_g can be extracted. The gate area (A_g) is 0.3 mm^2-1.5 mm^2 with a gate length (L_g) of 95-470μm. During the measurement, the diode is kept at a constant reverse voltage (V_d) while the changes of the diode current are monitored when the gate is swept from accumulation toward the inversion. I-V measurement was done on 12 samples for each gate length, then using the bulk and surface generation currents and depletion region formulas, τ_g and s_g were extracted. The average value of the bulk generation lifetime was 40ms and surface generation velocity was 2.1cm/s for the fabricated wafers. Furthermore, the boron layer is used as a voltage divider between the inner and outer rings. The resistors made with 500°C and 700°C PureB layers are stable in different locations in the wafer with a maximum tolerance of 1.7% over the wafer for high temperature samples compared to 4.9% for low temperature samples. The resistors made with implantation in general have more fluctuation over the wafer. The calculated value of the tolerance for resistors made with implantation is 30% (only working devices were considered) while for resistors made with 500°C PureB it is only 4.9% (all devices were working). A thicker passivation layer leads to a lower leakage current. For boron layer SDDs there is no difference in the leakage current between oven and Epsilon annealing suggesting a lower thermal budget process using an Epsilon reactor with a very short time. Having field plate (metal overlap on the oxide) which covers the oxide in the drift rings of the SDD reduces the leakage current by factor of two. Using the double boron layer process, the leakage current was lower than the single boron layer process. The explanation can be that second boron layer introduces a layer of holes which suppresses the minority carrier's currents resulting in a very low leakage current. Finally leakage current of the continuous

design (one boron layer) and constant field design (double boron layer) are around 6 and 20 times lower than a conventional SDD, respectively. Since measuring the JFET in SDD structure is not possible (gate is connected to the anode) at the wafer level, individual JFET structures were placed in the layout with similar dimensions as SDD JFETs. The length of transistor is L=4.5µm and the width is W=48.5µm with the saturation current equal to 412.5µA, transconductance (g_m) equal to 198.65µA/V at a drain voltage of 4V, a gate voltage of zero volts, pinch-off voltage of -4V and gate capacitance of 71.48fF. At the end of the chapter a novel interposer is introduced to measure the devices with contact pads on both sides. In this interposer, the device is mounted on the center hole and there are TSV-type connections in the periphery of the center hole. With wire bonding, contact pads are connected to the TSV connections to transfer all pads to one side. In order to protect the wire bonds, a Teflon cavity was developed. Therefore all contact pads are available for measurement from the top side of the complete package. Using this developed package we could do all DC and CV measurements on the probe station successfully.

Samenvatting

Ontwikkeling van Silicium Driftdetectoren met behulp van Boorlaag-technologie

Stralingsdetectoren worden gebruikt in een grote verscheidenheid van vakgebieden, zoals medische, veiligheid, defensie, geofysische, industriële en natuurkunde. Ze zijn ontwikkeld om de energie of de positie van straling of geladen deeltjes te detecteren.
In **hoofdstuk een** wordt een aantal röntgenstralingsdetectoren kort geïntroduceerd. In een gasgevulde röntgendetector, ioniseren inkomende fotonen inert gas tot elektronen en ionen. Deze worden verzameld bij een dunne anodedraad aan de binnenkant van het apparaat. Het voordeel van deze type detectoren is de mogelijkheid om het signaal of lading te versterken, wat leidt tot een hoge signaal-ruisverhouding. Aan de andere kant hebben ze last van lage röntgendetectie-efficiëntie vanwege de lage dichtheid van het gebruikte gas. In een scintillatiedetector, botsen röntgenfotonen met een scintillator en creëren UV of zichtbaar licht dat omgezet kan worden tot een elektrisch signaal door een fotodiode. Het grootste nadeel van scintillatiedetectoren is de slechte energieresolutie, vanwege grote verliezen, en de relatief hoge ionisatie-energie zoals 20-500 eV. In halfgeleiderdetectoren kunnen elektron-gatparen (EHPs) bij veel lagere energieën worden gegenereerd dan met gasgevulde detectoren. De mogelijkheid om zowel de positie als de energie van inkomende straling te nauwkeurig te meten, zijn unieke eigenschappen voor halfgeleiderdetectoren. Ze hebben echter geen intrinsieke signaalversterking zoals bij gasgevulde detectoren. Daarom is een geïntegreerde of externe versterker vereist voor deze type detectoren. In de keuze van halfgeleidende materialen moet: een hogere dichtheid en een hoger atoomnummer voor een betere absorptie-efficiëntie, een lagere bandgap voor een betere resolutie, en een hogere mobiliteit voor snelle detectie naast lagere lekstroom en een dikker substraat worden beschouwd. Onder de verschillende halfgeleidermaterialen is silicium een interessante keuze voor röntgendetectors vanwege de beschikbaarheid in de fabricageprocestechnologie, lagere kosten, en de mogelijkheid voor geavanceerde elektronische circuits en verdere signaalbewerking. PIN fotodiodes gemaakt in hoge-weerstand

siliciumsubstraten zijn het eenvoudigst, commercieel verkrijgbaar en goedkoopste type röntgendetectors waarin de volledige dikte van het silicium wordt uitgeput in sperrichting om de gegenereerde EHPS te extraheren bij bestraling. PIN detectoren bezetten echter een groot gebied voor de anode waardoor de uitgangscapaciteit groot is. Dit leidt tot een hogere ruisniveau op de uitgang. In Si (Li) en Ge (Li) detector worden kristallen van silicium of germanium met een dikte van ongeveer enkele mm tot cm gebruikt. Om intrinsieke materiaal te verkrijgen (concentratie zo laag als 10^9 cm^{-3}) voor de volledige dikte, wordt een Li driftproces gebruikt, waarbij de Li als donor werkt, te compenseren voor acceptorionen. De typische instelspanning is 500V tot 4000V. Om herverdeling van Li atomen te voorkomen, moet de detector bij lage temperatuur worden gehouden met behulp van vloeibare stikstof; dit is het grootste nadeel van dit type detector. Silicium stripdetectoren maken 2D positiegevoelige detectie mogelijk. Ze lijken op PIN diodes maar het p^+ gebied wordt verdeeld in veel strips aan de voorkant om de gaten te verzamelen en het n^+ gebied wordt verdeeld in veel n^+ strips aan de achterkant om de elektronen te verzamelen. In een silicium pixeldetector (SPD) wordt slechts aan één zijde van de p^+n is gepatroneerd en elke pixel heeft zijn eigen uitleeselektronica die via soldeerstoten aan elkaar is gehecht. In p-n CCD's wordt de driftfunctie uitgevoerd door externe pulsen uit te oefenen op achteruit en vooruit ingestelde p-n overgangen in periodieke cycli, om te fungeren als reeks van shiftregisters en de elektronen te leiden naar de anode. Silicium driftdetectoren (SDD) zijn detectoren met een extreem kleine anode en een lage uitgangscapaciteit dus dit leidt tot minder ruis en een hoge energie-resolutie. In cirkelconfiguratie maken de p^+ drift ringen een elektrisch veld evenwijdig aan het oppervlak om de elektronen in het kleine anodegebied te verzamelen. Onafhankelijke van het actieve gebied van de detector, is een typische uitgangscapaciteit van de SDD ongeveer 60fF. On-chip-elektronische apparaten worden op de voorkant geplaatst om het signaal te versterken. In de Silicon Drift Detector Droplet (SD^3) is de anode en de geïntegreerde transistor verplaatst naar het gebied waar ze kunnen worden afgeschermd van de directe straling met de juiste collimator. Dit heeft een sterk effect op de lage-energie achtergrond in SDD vergeleken met de SD^3, de verhouding tussen piek en achtergrond wordt hiermee verhoogd van 3000 naar 5000. Multichannel SDD's zijn samengesteld uit vele SDDs met individuele uitlezing maar met een gezamenlijke ingangsraam, schutring en netspanning waarbij het gevoelige gebied zeer groot is, tot enkele cm^2, zonder verlies van de energie-resolutie en telkracht van een enkele SDD. Ten slotte, in 3D detectoren worden geïmplanteerde elektroden van conventionele SDDs vervangen door een 3D-

reeks van p^+ en n^+ elektroden in het silicium. In een 3D detector zijn de verzamelafstanden en tijden ongeveer een orde van grootte lager dan vlakke strip en pixeldetectoren en de uitputspanning is ongeveer twee orde van grootten lager. Het fabricageproces is echter complex en duur.

In **hoofdstuk twee** worden de eigenschappen van het boorlaag grondig beschreven. De boorlaag wordt gedeponeerd in een ASM Epsilon reactor met diboraan (B2H6) en waterstof als doteringsgas en dragergas bij temperaturen van 500°C tot 700°C. Een typische dikte van de boorlaag gedeponeerd op 700 °C gedurende 7 minuten is 2-3nm. Deponeren bij lagere temperaturen leidt tot een onregelmatig boorlaag. Dit is bevestigd via een TEM-analyse. Gefabriceerde PureB diodes gedragen zich als conventionele diepe p^+-n overgang met bijna ideale idealiteitfactoren lager dan ≈ 1.02, en een lage verzadigingsstroom. Weerstanden zijn sleutelelementen in geïntegreerde circuits en kunnen gemaakt worden met een p-n overgang of door poly depositie. Echter, instellingsafhankelijkheid en een hoge parasitaire capaciteit voor hoog-ohmse weerstanden in overganggemaakte weerstanden en grote variatie en proces afhankelijkheid voor poly gemaakt weerstanden zijn nadelen voor deze twee technologieën. Typische vierkantsweerstandwaarden van gedeponeerde boorlagen is ongeveer 100kΩ/□ welke aangepast kunnen worden afhankelijk van de depositietijd en gloeitemperatuur. In dit proefschrift worden de fotodiodes gefabriceerd op hoge-weerstand Si (HRS) <100> wafers n-type fosfor-gedoteerd tot 2-10kΩ-cm. De weerstanden zijn ook rechtstreeks in het HRS geplaatst zodat aangesloten depletiegebieden tientallen microns breed zijn, zelfs bij 0 V instelling. Daarom is de spanningsafhankelijkheid van de weerstandswaarde verwaarloosbaar. Het fabricageproces bestaat uit oxidatie, gevolgd door een etsstap, boorlaag depositie en tenslotte metallisatie. Om het Al bovenop de boorlaag te verwijderen wordt een combinatie van droog- en een korte nat-etsstap in verdunde HF werd gebruikt. De vierkantsweerstandwaarden verkregen uit de ringstructuurmetingen zijn $2,5 \times 10^4$ Ω/□ voor een 7-min 700°C depositie en $3,8 \times 10^5$ Ω/□ voor een 20-min 500°C depositie. Gefabriceerd weerstanden tonen hoge lineariteit in spanningsbereiken van 10V tot 100V en zijn temperatuurstabiel tussen 15 °C en 95 °C. De 500°C weerstanden hebben een TCR (temperatuur coëfficiënt van de weerstand) van minder dan 200 ppm/°C tot een meettemperatuur van 70°C daarna groeit het tot ongeveer 1000 ppm/°C bij 95°C. De TCR van de 700°C monster heeft een nagenoeg constante waarde van minder dan 400 ppm/°C gedurende de meting over het gehele temperatuurbereik. De gemeten lekstroom is lager dan 1nA/cm^2 bij 10V achteruit instelling over alle microchips

van een 100mm wafer. De gemeten weerstandtolerantie lag tussen 1% en 5% voor zowel kΩ- en MΩ-weerstanden.
Omdat Puur-Al de ondiepe overgangen met de bulk kan kortsluiten, met name wanneer de boorlaag is gedeponeerd bij lagere temperaturen (ongelijkmatige boorlaag) of wanneer er een defect op het substraat bestaat, wordt een legering van AlSi (1% Si) gebruikt. Hoewel het verwijderen van de AlSi door een nat proces niet geschikt is voor het boorlaagproces. Daarom is het beter om een diffusiebarrièrelaag tussen Al en de boorlaag te creëren. Verschillende diffusiebarrièrelagen waren bestudeerd waaronder Ti, TiN, AlN en ZrN. Alleen ZrN toonde betere procescompatibiliteit en had geen invloed op de elektrische werking van de detectoren. Optische- en SEM-inspecties toonden defectvrije oppervlakten van de detectoren bij het gebruik van een 10nm ZrN tussen Al en de boorlaag voor zowel de op 700 als de 500°C gedeponeerde lagen. Als alternatief is het lift-off proces ontwikkeld om Al residuen op de boorlaag te voorkomen. Na PureB depositie op 700°C of 500°C is een negatief fotolak (AZ®nLOF) toegepast en gepatroneerd, gevolgd door het opdampen van een 400nm dikke Al laag. Vervolgens is de lak verwijderd in aceton of een NMP oplossing in een ultrasonisch bad. Voor beide PureB lagen gedeponeerd op 700°C of 500°C was het lift-off-proces geslaagd. De beperking van de Al dikte en depositiemethode (opdampen) vormt echter een een uitdaging voor sommige toepassingen.

In **hoofdstuk drie** wordt het werkingsprincipe van de SDD bestudeerd. Ze hebben een hoge telsnelheid en betere energieresolutie vergeleken met andere röntgendetectoren. Om werkende detectoren te verkrijgen moeten verschillende aspecten van de SDDs worden gekozen, ontworpen en zorgvuldig worden gesimuleerd. Het beginmateriaal voor de SDD is een hoog-ohmse silicium wafer vanwege de betere levensduur van de ladingsdragers (in de orde van milliseconden) en de lagere vereiste spanning voor volledige uitputting. Om een betere uniformiteit van de wafers te verkrijgen, worden deze gemaakt met een neutron transmutatie gedoteerde (NDO) methode waarbij uniformiteit van de fosfor dotering wordt bereikt door het blootstellen van een staaf van zeer zuiver silicium aan een gelijkmatige stroom van thermische neutronen. Voor detectie van hogere energieën moeten dikkere wafers worden gebruikt. Daarnaast heeft een <100> silicium substraat een hogere lading-verzamelefficiëntie (CCE) van zachte röntgenstralen (onder 200 nm golflengte) en hebben een lagere oppervlakte lekstroom ten opzichte van de <111> oriëntatie. Het ingangsvenster van de detector bepaalt de laagste detecteerbare energie. In een SDD wordt het ingangsvenster in vacuüm

gehouden door beryllium of polymeervensters te gebruiken. Deze vensters kunnen het lagere bereik van detecteerbare röntgenstraling beperken. In TEM systemen wordt een hoge vacuümtoestand gebruikt. Hierdoor zijn deze vensters niet meer vereist. Op deze manier kan het lager detecteerbaar bereik worden verminderd. Om nog lagere energieën van röntgenstralen (enkele honderden eVs) te detecteren, moet het dode laag van het p^+ gebied in het ingangsvenster zo dun mogelijk zijn, dus een ondiepe overgang is vereist. Een typische dode laag is 40nm door implantatie. Om een volledige uitputting in het midden van de detector te houden, wordt het ingangsvenster ingesteld op V_{dep} welke overeenkomt met de spanning voor de uitputting van de volledige waferdikte. Op de buitenste driftring staat een spanning van $2V_{dep}$ om voldoende driftpotentiaal voor de elektronen naar de anode te garanderen. Lekstroom is een belangrijke parameter in de SDD welke het ruisniveau bepaalt. Bulk lekstroom kan worden beperkt door de keuze van een hoge kwaliteit wafer en het verlagen van de procestemperatuur. Oppervlaktegeneratielekstroom kan ontstaan vanuit de verwerking van defecten en raakvlaktoestanden gegenereerd in het bandgatgebied dichtbij het oppervlakte door abrupte discontinuïteit in het silicium-raakvlak. Zink-anode is een structuur bedoeld om de oppervlaktelekstroom te verminderen door een pad te creëren waar oppervlakte-elektronen kunnen worden weggespoeld via de p^+ veld elektroden. Om de energieresolutie zoveel mogelijk te verbeteren, moeten de totale capaciteiten waaronder de anodecapaciteit en de parasitaire capaciteit (verbinding met het externe circuit) gelijk zijn aan de ingangscapaciteit van de externe versterker. Beschermringstructuren behouden een lage lekstroom voor de SDD zonder doorslag op hoogspanningsinstellingen voor uitputting- en driftmechanismen. Het ingangsvenster kan met een PureB laag gemaakt worden die slechts een 2 nm dode laag heeft voor de p^+ laag. Daarom moet het meten van lagere energieën (zoals 100eV) mogelijk zijn. Daarnaast kunnen PureB weerstanden gemaakt worden als spanningsdeler in het driftgebied van de detectoren. Een continue laag van boor kan fungeren als verdeelde weerstand om de elektronen naar de anode te driften, maar uit berekeningen en simulaties blijkt dat een enkele boorlaag, een onvoldoende elektrisch veld genereert om de elektronen te kunnen driften. Het binnenste deel heeft een hogere weerstand dan het buitenste deel, dus is het elektrisch veld alleen geconcentreerd in het midden van de detector en wordt er geen kracht uitgeoefend op de elektronen om naar de anode te driften. Voor de ontworpen detector is de straal van de binnenring 135μm en de buitenring 3135μm, gemaakt met een boorlaag met een vierkantsweerstand van $10^5\Omega/\square$. De totale weerstand tussen de contacten is

gelijk aan 50kΩ. 95% van deze waarde komt van 135µm tot 500 urn van het detectorgebied. Het elektrisch veld is ongeveer drie ordes van grootte lager in de buitenste ring dus is het alleen effectief aan de binnenzijde van de detector, en is er een onvoldoende elektrisch veld om de elektronen naar de anode aan de buitenzijden van de detector te verplaatsen. Potentiaalverdeling geeft een 40V aangelegde spanning aan, elektronen worden geaccumuleerd in de goot, het minimum van de potentiële energie, en langzaam worden verplaatst naar de anode. Bij 160V is de driftspanningshelling langs het oppervlakte van de detector iets hoger dan bij 40V, maar nog steeds te klein om de elektronen naar de anode te laten driften. Daarom heeft ongeveer 80% van het driftgebied bijna een elektrisch veld van bijna nul. Een dubbele boorlaag met twee verschillende vierkantsweerstanden en een speciaal ontwerp kan echter een constant elektrisch veld in het driftgebied creëren, terwijl de lekstroom laag blijft. In dit ontwerp i het gehele oppervlakte bedekt met twee lagen van boor om een minimale lekstroom te verkrijgen, waarbij een lage vierkantsweerstand is dichter, in de buurt van de anode, en een hoge vierkantsweerstand van de laag dichter is, in de buitenste ringen om een constante weerstand en elektrisch veld te produceren over het driftgebied.

Hoofdstuk vier beschrijft de integratie van de versterker-op-chip en het ontwerpen van de beschermringstructuur voor de SDD waar geen vermenigvuldiging mechanisme is, dus een on-chip of off-chip versterker is vereist. Met on-chip versterking kan ongewenste interferentiebijwerkingen die bij draadhechting bijkomt, zoals parasitaire capaciteiten en microfonische ruis, worden vermeden. Om het type transistor voor de SDD te selecteren, wordt de voorkeur gegeven aan een JFET tegen de ruis. Bipolaire transistoren hebben een hogere hagelruis en CMOS transistoren hebben een hogere 1/f ruis. Bij het ontwerpen van de JFET is er een trade-off tussen het verkrijgen van een minimum aan ruis en minimale aan capaciteit terwijl steilheid (gm) zo hoog mogelijk moet worden gehouden. Gate-capaciteit speelt een belangrijke rol in deze trade-off. Aangezien mobiliteit van de nFET hoger is, biedt deze een hogere kantelfrequentie dan de pFET. Voor een optimale SDD-resolutie moet de ingangscapaciteit van de JFET gelijk zijn aan de detectorcapaciteit. In een SDD wordt vaak de JFET transistor in de anode geplaatst, welke geïsoleerd is door een p-type gebied van de anode. De anode is verbonden aan de gate en in gemeenschappelijke-bronconfiguratie wordt de drain aangesloten op de voedingsspanning en de source is aangesloten op het externe circuit. Opgestapelde lading op de anode kan worden afgevoerd door reset-apparaten zoals de diode, JFET en MOSFET. De lineariteit van de transistor,

ruisoverwegingen, beschikbaarheid van technologie en opmaakcompatibiliteit, bepalen de keuze van de reset-transistor. In dit proefschrift zijn twee typen JFET-op-chip met 4.5μm gate-lengte, samen met verschillende reset apparaten ontworpen voor de SDD. De resetapparaten worden ingebed in de JFET of in het kleine anodegebied. De parasitaire condensator tussen de detector anode en de transistor-beschermring kunnen als terugkoppelcondensator dienen . In het fabricageproces om de optimale implantatieparameters (energie en dosis) te vinden voor de gate (p^+), S/D (n^+) en diepe n en diepe p gebieden, worden twee verschillende manieren uitgevoerd. Voor de gate-dotering, is een combinatie van boor implantatie en boorlaagdepositie gebruikt.
Bovendien wordt in dit hoofdstuk het ontwerpen van multi-beschermringstructuren besproken. Volgens elektrische metingen bij verschillende temperaturen, is een positieve temperatuurcoëfficiënt voor doorslagspanning gevonden. Dit betekent dat de doorslagspanning een lawine-type is. Om doorslag te voorkomen, zijn verschillende multi-beschermringstructuren bestudeerd. Multi-beschermringstructuren bestaan voornamelijk uit een grote p-type bescherming (240 μm breedte), een reeks tussenliggende concentrische cirkelvormige p-type beschermringen (met verschillende standplaatsen en breedtes en metaaloverlap van de veldplaat) en een groot n^+-type bescherming (150 μm breedte) dichtbij de scribe-lijn. De functie van n^+ beschermring is om alle bestaande positieve ladingen in het oxide te schermen en voorkomt uitbreiding van het uitputtingsgebied in de richting van de chipsnijlijn, waardoor de lekstroom aanzienlijk daalt. In deze structuur, ontwerpparameters zoals de grootte van de opening, oxidelading, bulk doteringsconcentratie en veldplaat (metalen uitbreiding) hebben invloed op de potentiaalverdeling van de beschermringen. Eén van de ontworpen structuren werkt tot de limiet van het meetsysteem (1100V) met zeer lage lekstroom tussen 1.5-3nA/cm^2. In deze structuur was de breedte van de beschermringen 25 μm. De eerste kloof (tussen de grote beschermring en eerstvolgende beschermringring) was 35 μm en de plaatsing was 80 μm voor de rest van de ringen, met binnenwaartse veldplaat van 5-30μm uitbreiding. Andere structuren gaven rond 400V doorslag. Volgens de metingen van verschillende ontworpen beschermringstructuren, zit rond de 40 μm kloof een optimale waarde voor de afstand tussen de grote beschermring en de eerstvolgende ring in multi-beschermringstructuur. Bovendien werd gevonden dat een veldplaat in binnenwaartse richting leidde tot een hogere doorslagspanning vanwege afscherming van de ladingen.

In **hoofdstuk 5** wordt het fabricageproces en de karakterisering resultaten van de SDDs besproken. Omdat waferbewerkingen is uitgevoerd op beide zijden van de wafers, is speciale zorg vereist tijdens verwerkingsstappen zoals wafertransportsystemen, implantatie en nat etsen worden om schade aan beiden kanten van de wafer te voorkomen. Verder omdat het levensduur van de lading erg belangrijk is voor de werking van de SDD, worden hoge temperatuurprocesstappen zoveel mogelijk vermeden. Daarom kan activering van doteringsmiddelen bij lagere temperaturen, met name in het geval van de JFET-integratie, een uitdaging zijn. In het algemeen begint een typisch fabricageproces met droge oxidatie, gevolgd door beschermring en anode implantaties door boor en fosfor doteerstoffen. De volgende stap is TEOS oxide depositie en uitgloeiing. Dan wordt de oxidelaag geëtst om de gebieden te openen voor boordepositie om p^+ gebieden te creëren. Boron depositie is selectief, dat betekent dat alleen op silicium gedeponeerd wordt. Al metallisatie aan beide zijden is de volgende stap. Om Al te etsen en de boorlaag bloot te stellen, is een combinatie van droog (om de afmetingen van het ontwerpen te behouden) en nat etsen in verdunde HF nodig, om te landen op de boorlaag zonder beschadiging van deze laag. Legeren in de vormeergas is de laatste stap om een ohmisch contact van gedopeerd silicium met Al te creëren. Voor het dubbele boorlaagproces, worden twee maskers (litho stappen) gebruikt voorafgaand de boordepositie. Met behulp van de eerste lithografische stap, wordt oxide geëtst in het driftgebied waarna 30nm oxide over is gelaten . Door de tweede lithografische stap, werd 30nm oxide geëtst uit lage vierkantsweerstandgebieden. Lage-vierkantsweerstandboorlaag is gedeponeerd en gevolgd door een 10 seconden BHF stap om 30nm oxide te etsen in de rest van het driftgebied. De vooraf gedeponeerde boorlaag wordt niet aangevallen door deze korte BHF stap. Aan het einde is een hoge-vierkantsweerstandboorlaag gedeponeerd. In het fabricageproces voor de JFET integratie zijn er verschillende implantatiestappen voor diepe p, diepe n, S/D en gate regio's.

Gefabriceerd wafers werden onderworpen aan elektrische metingen om de waferkwaliteit en de SDDs te karakteriseren. Meting en berekening van het dopingprofiel van de CV krommen resulteerden in 144.5µm en 217.5µm uitputtingsdiepten aan de kant van het ingangsvenster van het apparaat-kant van het silicium wafer, respectievelijk. Uit deze meting blijkt dat de ingangsvenster (voorkant) van de wafer een lager soortelijke weerstand heeft dan het apparaat-kant (achterkant). Kennis van bulk generatielevensduur (τ_g) en oppervlakte generatiesnelheid (s_g) van de wafer is essentieel voor procesbeheersing en stralingsschadecontrole in stralingsdetectoren. Met behulp

van ontworpen gated-diodestructuren kunnen τ_g en s_g worden gevonden. Het gate-gebied (Ag) is 0,3 mm^2-1.5 mm^2 met een gate-lengte (LG) van 95-470µm. Tijdens de meting wordt de diode gehouden in een constante sperspanning (V_d), terwijl de veranderingen van de diodestroom wordt geanalyseerd wanneer de gate wordt geveegd van accumulatie naar de inversie. IV metingen zijn uitgevoerd op 12 monsters van elke gate-lengte, en vervolgens met behulp van bulk en oppervlaktegeneratiestromen en uitputtingsgebieden-formules worden τ_g en s_g gevonden. De gemiddelde waarde van bulk generatielevensduur is 40ms en oppervlakte generatiesnelheid is 2.1cm/s voor de gefabriceerde wafers. Verder wordt de boorlaag als spanningsdeler gebruikt tussen de binnenste en buitenste ringen. De weerstanden van 500°C en 700°C PureB lagen zijn stabiel op verschillende locaties in de wafer met maximaal 1,7% tolerantie over de wafer voor hoge-temperatuurmonsters vergeleken met 4.9% voor lage-temperatuurmonsters. De weerstanden die met implantatie zijn gemaakt hebben over het algemeen meer waarde-schommelingen over de wafer. De berekende waarde van de tolerantie voor weerstanden gemaakt door implantatie is 30% (alleen werkende apparaten werden beschouwd), terwijl voor de weerstanden gemaakt met 500°C PureB slechts 4,9% tolerantie bezaten (alle apparaten werkten). Een dikkere passiveerlaag leidt tot een vermindering van de lekstroom. Voor de boorlaag-SDD is er geen verschil in lekstroom tussen oven en Epsilon gegloeide proces, wat voor processen met een lagere thermische budget de Epsilon reactor met zeer korte gloei tijden, gebruikt kan worden. Een veldplaat (metaaloverlapping op oxide) die de oxide in de drift ringen van de SDD bedekt, vermindert de lekstroom door een factor twee. Een dubbele boorlaagproces leidde tot een lagere lekstroom dan een enkele boorlaagproces. De verklaring hiervoor kan zijn dat de tweede boorlaag een laag van gaten introduceert die stromen van minderheidsladingsdragers onderdrukt, wat tot een zeer lage lekstroom leidt. Tenslotte, de lekstroom van een continu-ontwerp (één boorlaag) en constante-veldontwerp (dubbele boorlaag) zijn ongeveer 6 en 20 keer lager dan bij conventionele SDDs, respectievelijk. Omdat het meten van JFETs in een SDD structuur niet mogelijk is op waferniveau (gate is verbonden met de anode), zijn individuele JFET structuren geplaatst in het ontwerp met gelijke afmetingen als de SDD JFETs. De lengte van de transistor is L = 4.5µm en de breedte is W = 48.5µm met verzadigingsstroom gelijk aan 412.5µA, de steilheid (g_m) gelijk aan 198.65µA/V bij drainspanning van 4V, gatespanning van nul volt, pinch-off spanning van -4V, en gate capaciteit van 71.48fF. Aan het einde van het hoofdstuk wordt een nieuwe tussenlaag ingevoerd om de apparaten met contactvlakken aan beide zijden te meten. In deze tussenlaag zijn apparaten

gemonteerd op het centrale gat en zijn er TSV-soort verbindingen in de omtrek van het centrale gat. Door draadhechting, zijn contact pads verbonden met de TSV verbindingen om alle pads naar één kant te kunnen verplaatsen. Om de bedrading bij draadhechting te beschermen is een Teflon holte ontwikkeld. Daarom zijn alle contactvlakken toegankelijk aan de bovenzijde van het complete pakket om te kunnen meten. Met behulp van deze ontwikkelde pakket kunnen we alle DC en CV-metingen doen op de meetsystemen.

List of publications

Journal papers

1. **Negin Golshani**, J. Derakhshandeh, C.I.M. Beenakker, R. Ishihara, “PureB multi-guard ring structures for detector applications”, submitted to Microelectronic Engineering journal 2015.

2. **Negin Golshani**, C.I.M. Beenakker, R. Ishihara, “Manufacturing of uniform field silicon drift detector using double boron layer”, Nuclear Instruments and Methods in Physics Research Section A (NIMA), In press, available online 28 May 2015.
   DOI: 10.1016/j.nima.2015.05.011

3. **Negin Golshani**, J. Derakhshandeh, C.I.M. Beenakker, R. Ishihara, “High-Ohmic Resistors Fabricated by PureB layer for Silicon Drift Detectors Applications”, Solid-State Electronics, vol. 105, pp. 6–11, March 2015. available online, Dec. 2014.
   DOI: 10.1016/j.sse.2014.11.022

4. **Negin Golshani**, V. Mohammadi, H. Schellevis, C.I.M. Beenakker, R. Ishihara, “Reactively sputtered nanometer-thin ZrN film as a diffusion barrier between Al and Boron layers for radiation detector applications”, APL Materials, vol. 2, no. 10, October 2014.
   DOI: 10.1063/1.4897959.

5. V. Mohammadi, **N. Golshani**, K.R.C. Mok, W.B. de Boer, J. Derakhshandeh, L.K. Nanver, “Temperature Dependency of the Kinetics of PureB CVD Deposition over Patterned Si/SiO2 Surfaces”, Microelectronic Engineering, vol. 125, pp. 45-50, Aug. 2014.

6. Ryoichi Ishihara, Jin Zhang, Miki Trifunovic, Jaber Derakhshandeh, **Negin Golshani**, Daniel M. R. Tajari mofrad, Tao Chen, Kees Beenakker and Tatsuya Shimoda, “Single-Grain Si Thin-Film Transistors for Monolithic 3D-ICs and Flexible Electronics”, IEICE Transactions on Electronics, vol. E97-C, no.4, pp. 227-237, 2014.
   http://dx.doi.org/10.1587/transele.E97.C.227

7. L.K. Nanver, L. Qi, V. Mohammadi, K.R.M. Mok, W.B. de Boer, **N. Golshani**, A. Sammak, T.L.M. Scholtes, A. Gottwald, U. Kroth, F. Scholze, “Robust UV/VUV/EUV PureB Photodiode Detector Technology with High CMOS Compatibility”, invited paper, J. Selected Topics in Quantum Electronics, vol. 20, no. 6, pp. 1-11, 2014.

8. V. Mohammadi, L. Qi, **N. Golshani**, K. R. C. Mok, W. B. de Boer, A. Sammak, J. Derakhshandeh, van der Cingel, L. K. Nanver, “VUV/Low-Energy-Electron Si Photodiodes with Post-Metal 400°C PureB Deposition”, IEEE Electron Device Letters, vol. 34, no. 12, pp. 1545–1547, Dec. 2013.
   DOI: 10.1109/LED.2013.2287221.

9. R. Ishihara, J. Derakhshandeh, M.R. Tajari Mofrad, T. Chen, **N. Golshani**, C.I.M. Beenakker, “Monolithic 3D-ICs with single grain Si thin film transistors”, Solid-State Electronics, vol. 71, pp. 80-87, May 2012.
   DOI 10.1016/j.sse.2011.10.025.

10. A. Sakic, T.L.M. Scholtes, W. de Boer, **N. Golshani**, J. Derakhshandeh, L.K. Nanver, “Arsenic-doped high-resistivity-silicon epitaxial layers for integrating low-capacitance diodes”, Materials, vol. 4, no. 12, pp. 2092-2107, Dec. 2011.
DOI 10.3390/ma4122092.

11. Jaber Derakhshandeh, **Negin Golshani**, Ryoichi Ishihara, Mohammad Reza Tajari Mofrad, Michael Robertson, Thomas Morrison and C.I.M Beenakker, “Monolithic 3D Integration of SRAM and Image Sensor Using Two Layers of Single Grain Silicon”, IEEE Transactions on Electron Devices (TED), vol. 58, no. 11, pp. 3954 – 3961, Sep.2011.
DOI: 10.1109/TED.2011.2163720.

12. **Negin Golshani**, Jaber Derakhshandeh, R. Ishihara, C.I.M Beenakker, “High speed 6T SRAM cells using single grain TFTs fabricated by μ-Czochralski-Czochralski process at low temperature”, Japanese Journal of Applied Physics (JJAP), vol. 49, no. 3S, March 2010.
DOI: 10.1143/JJAP.49.03CA09.

13. J. Derakhshandeh, **N. Golshani**, S. Mohajerzadeh, E. Asl Soleimani, “Current assisted germanium-Induced crystallization of amorphous silicon”, Thin Solid Films, vol. 427, pp. 324-329, March 2003.
DOI: 10.1016/S0040-6090(02)01167-7

Conferences

1. **N. Golshani**, V. Mohammadi, S. Ramesh and L.K. Nanver, “High-Ohmic Resistors using Nanometer-Thin Pure-Boron Chemical-Vapour-Deposited Layers”,
43rd European Solid-State Device Research Conference (ESSDERC), Bucharest, Romania, pp. 210-213, Sep. 2013.
DOI: 10.1109/ESSDERC.2013.6818856.

2. V. Mohammadi, **N.Golshani**, K.R.C. Mok, W.B. de Boer, J. Derakhshandeh, L.K. Nanver, “Temperature Dependency of the Kinetics of PureB CVD Deposition over Patterned Si/SiO2 Surfaces”, European Materials Research Society (E-MRS), Warsaw Poland, Fall Meeting Sep. 2013.

3. J. Derakhshandeh, **N. Golshani**, L.A. Steenweg, W. van der Vlist, L.K. Nanver, “A novel silicon interposer for measuring devices requiring complex two-sided contacting”, IEEE International Conference on Microelectronic Test Structures (ICMTS), Osaka, Japan, pp. 43-46, March 2013.
DOI: 10.1109/ICMTS.2013.6528143.

4. R. Ishihara, M.R. Tajari Mofrad, J. Derakhshandeh, **N. Golshani** and C.I.M. Beenakker, “Monolithic 3D-ICs with single grain Si thin film transistors”, IEEE 11th International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Xi'an, China, Oct. 2012.

5. L.K. Nanver, A. Sammak, A. Šakic, V. Mohammadi, J. Derakhshandeh, K.R.C. Mok, L. Qi, **N. Golshani**, T.M.L. Scholtes, W.B. de Boer, “Applications of PureB and PureGaB ultrashallow junction technologies”, IEEE 11th International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Xi'an, China, pp. 303-306, Oct. 2012.
DOI: 10.1109/ICSICT.2012.6467697.

6 L.K. Nanver, A. Sammak, V. Mohammadi, K.R.C. Mok, L. Qi, A. Sakic, **N. Golshani**, J. Derakhshandeh, T.M.L. Scholtes, W.D. de Boer, “Pure dopant deposition of B and Ga for ultrashallow junctions in Si-based devices”, ECS Trans. 2012, vol. 49, No. 1, 27th Symposium on Microelectronics Technology and Devices (SBMicro), Brazil, Brasilia, pp. 25-33, 2012.

7 R. Ishihara, M. R. T. Mofrad, J. Derakhshandeh, **N. Golshani** and C. I. M. Beenakker, “Monolithic 3D- ICs with Single Grain Si Thin Film Transistors”, IEEE 11th International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Xi'an, pp. 1-4, Oct.2012.
DOI:10.1109/ICSICT.2012.6467714

8. R. Ishihara, **N. Golshani**, J. Derakhshandeh, M.R. Tajari Mofrad and C.I.M. Beenakker, “Monolithic 3D-ICs with single grain Si thin film transistors”, 12th International Conference on Ultimate Integration on Silicon (ULIS), Cork, Ireland, pp. 1-4, Mar. 2011.
DOI: 10.1109/ULIS.2011.5758004.

9. **Negin Golshani**, Jaber Derakhshandeh, Shu Yi Liu, Ryoichi Ishihara, J. Van der Cingel and C.I.M Beenakker, “Low Subthreshold Slope and High Mobility Single Grain Silicon TFTs Using Grown Oxide”, European Materials Research Society (EMRS) Symposium I, PP. 8-48, 2010.

10. **Negin Golshani**, Jaber Derakhshandeh, Ryoichi Ishihara, C.I.M Beenakker, Michael Robertson and Thomas Morrison, “Monolithic 3D Integration of SRAM and Image Sensor Using Two Layers of Single Grain Silicon”, IEEE International Conference on 3D System Integration (3D IC), Munich, Germany, Nov. 2010.
DOI: 10.1109/3DIC.2010.5751441.

11. **Negin Golshani**, R. Ishihara, J. Derakhshandeh, C.I.M Beenakker, “Fabrication of 6T SRAM cell using single grain TFTs obtained by μ-Czochralski process”, In Proceedings of Active-Matrix and Flat Panel Displays (AMFPD), Nara, Japan, 2009.

12. J. Derakhshandeh, S. Mohajerzadeh, **N. Golshani**, E. Asl Soleimani, M.D. Robertson, “Field-Assisted Germanium Induced Crystallization of Amorphous Silicon”, MRS Spring Meeting,
In MRS Proceedings, vol. 762, 2003.
DOI:10.1557/PROC-762-A16.3

13. J. Derakhshandeh, **N. Golshani**, S. Mohajerzadeh and E. Asl Soleimani, “Current-assisted germanium-induced crystallization of amorphous silicon on glass”, European Materials Research Society (EMRS), SymposiumK,Thin Film Materials for Large Area Electronics, Strasbourg, France, June 18-21, 2002.

Workshops

1. **Negin Golshani**, Jaber Derakhshandeh, Agata Sakic, Lis Nanver, “Silicon Drift Detectors for the detection of x-rays down to energies as low as 100 eV”, Micro Nano conference, Ede, The Netherlands, Dec.2013.

2. V. Mohammadi, **N. Golshani**, K.R.C. Mok, W.B. de Boer, J. Derakhshandeh and L.K. Nanver, “Investigation of the Issues Arising by Lowering the Deposition Temperature of the PureB-layer on Si/SiO2 Surfaces”, Proc. ICT.OPEN, Eindhoven, The Netherlands, Nov. 2013.

3. **N. Golshani**, W.B. de Boer, T.L.M. Scholtes, A. Sakic, L.K. Nanver, "The influence of stacking faults on the leakage current of B-layer p+n diodes", Proc. STW-SAFE, Veldhoven, Nederland, pp. 81-84, 2010.

4. **Negin Golshani**, Jaber Derakhshandeh, R. Ishihara, C.I.M Beenakker, "High speed 6T SRAM cells using single grain TFTs fabricated by μ-Czochralski process at low temperature", Proc. SAFE, Veldhoven, Netherlands, Nov. 26-27, 2009.

Presentations / report in NanoNextNL Programme 09A:

1. **Negin Golshani**, "Progress on new detector technology for SEM imaging using PureB layer – Continuous and Uniform electric field PureB-SDDs (Dual Boron layer SDD)", Eindhoven, The Netherlands, 13 April 2012.

2. **Negin Golshani**, "New detector technology for SEM imaging – A navel Silicon interposer and PureB-Multiguard rings for SDD applications", Utrecht, The Netherlands, 23 Nov. 2012.

3. **Negin Golshani**, "Progress on new detector technology for SEM imaging", Eindhoven, The Netherlands, 15 April 2013.

4. **Negin Golshani**, "Progress on new detector technology for SEM imaging", 31 August 2013.

5. **Negin Golshani**, "Project highlights", 2 October 2014.

Presentations given in the regular meetings with Companies (FEI and /or PANalytical):

1. **Negin Golshani**, "Multi-anode linear SDDs for high-resolution X-ray spectroscopy charge confinement and integration of read-out electronics (review of PhD thesis of Jan ˇSONSK´Y)", TU Delft, March 2011.

2. **Negin Golshani**, " Review of Silicon Drift Detectors – literature study", TU Delft, 11 April 2011.

3. **Negin Golshani**, "Test structures for qualifying HRS wafers and SDD process", TU Delft, 16 may 2011.

4. **Negin Golshani**, "SDD preliminary measurement results", FEI Company, Eindhoven, 22August 2011.

5. **Negin Golshani**, "PATENT – Review and summary of 20 SDD patents", FEI company, Eindhoven, 3 Nov. 2011.

6. **Negin Golshani**, "Designing the drift rings to have continuous SDD with the uniform electric field", TU Delft, 13 Jan 2012.

7. **Negin Golshani**, " Electric field compensation in ring structure", PANalytical, Almelo, 26 March 2012.

8. **Negin Golshani**, "Study on Leakage current and Sheet resistance of the two times deposited Boron Layer", 13 June 2012.

9. **Negin Golshani**, "Breakdown in the Detector – Effect of gap distance and field plate on the breakdown voltage", FEI company, Eindhoven, 10 September 2012.

10. **Negin Golshani**, "Preliminary results (11 different PureB-SDDs and compering them with a fabricated conventional implanted SDD)", TU Delft, 12 April 2013.

11. **Negin Golshani**, "High-Ohmic Resistors using Nanometer-Thin Pure-Boron Chemical-Vapour-Deposited Layers", TU Delft, 7 June 2013.

12. **Negin Golshani**, "3-D Silicon Detectors", TU Delft, 7 June 2013.

13. **Negin Golshani**, "Progress on Silicon Drift Detector using Boron layer", TU Delft, June 2014.

Acknowledgments

This research work was supported by NanoNextNL, a micro and nanotechnology program of the Dutch Government, and 130 partners (Programme 09A.03). Their support is gratefully acknowledged.
I would like to give my great thanks to my promotor Prof. Dr. Kees Beenakker and Co-promotor Dr. Ryoichi Ishihara, who helped and supported me with wrapping up my thesis and publications. Furthermore, I would like to thank Rector Magnificus of the Delft University of Technology Prof. Ir. Karel Ch.A.M. Luyben, Dean of the Faculty of Electrical Engineering, Mathematics and computer Science Prof. Dr. Ir. Rob Fastenau, Head of the Electronic Components, Technology and Materials Laboratory and Microelectronic Department Chair Prof. Dr. Lina Sarro, Dr. N.W. Stolp, Elly Pauw and Lotte Ophey for their continuous support and helping me in turbulent times. I also would like to thank Prof. Dr. Lis Nanver for initiating this project and many scientific discussions.

Many people helped me during the last four years. Without their support, help and companionship, this work would not have been possible. The complete story of how they all helped me will be another chapter of my thesis. Therefore, I am summarizing my acknowledgments in the following table.

I would like to give my thanks to:	
Discussions in scientific research	Prof. Dr. Kees Beenakker, Dr. Ryoichi Ishihara and Dr. Jaber Derakhshandeh FEI Company: Dr. Seyno Sluyterman, Kees Kooijman, Patrick Vogelsang and Dr. Gerard van Veen Panalytical Company: Dr. Petra Hegeman, Dr. Vladimir Jovanovic and Yannick Coquereau And Prof. Dr. Lis Nanver
Assistance during fabrication and measurement	Dr. Wiebe de Boer, Tom Scholtes and Dr. Amir Sammak for Boron layer deposition, Hugo Schellevis for metallization and support for the process flowcharts Jan Cornelis Wolff, Jan Groeneweg for mask preparation Silvana Milosavljevic, Tom Scholtes and Koos van Hartingsveldt for implantation Loek Steenweg and Wim van der Vlist for dicing and packaging Charles (Chuck) de Boer for the safety course and Silvana Milosavljevic for the cleanroom diploma training And all other members of the DIMES IC Processing Group: Alex van den Bogaard, Bert Goudena, Cassan Visser, Dr. Gregory Pandraud, Dr. Henk van Zeijl, Jan Warmerdam, Johan van der Cingel, Dr. Johannes van

	Wingerden, Joost Berendse, Mario Laros, Michiel van der Zwan, Robert Verhoeven, Ron van Viersen, Ruud Klerks, Wim Tiwon and Wim Wien. And Peter Swart for assistance in the measurement room
Support staff of ECTM and DIMES	Marian Roozenburg, Bianca Knot, Marysia Lagendijk and Xandra Tober
Staff members of ECTM	Prof. Dr. Kees Beenakker, Prof. Dr. Lina Sarro, Prof. Dr. Kouchi Zhang, Prof. Dr. ir. Ronald Dekker, Dr. Ryoichi Ishihara and Dr. Fredrik Creemer
Colleagues and friends	Dr. Agata Sakic, Dr. An Tran, Dr. Aslihan Arslan, Dr. Benjamin Mimoun, Bruno Morana, Dr. Caroline Mok, Cinzia Silvestri, Dr. Chenggang Shen, Dr. Daniel Tajari Mofrad, Dr. Elina Iervolino, Dr. Fabio Santagata, Dr. Francesco Vitale, Dr. Gianpaolo Lorito, Giuseppe Fiorentino, Dr. Hoa Pham, Dr. Huaiyu Ye, Dr. Jia Wei, Dr. Jiaqi Tang, Dr. Jin Zhang, Dr. Jing Zhang, Dr. Lei Shi, Lin Qi, Dr. Luigi Mele. Dr. Marko Mihailovic, Maryam Yazdan Mehr, Miki Trifunovic, Pan Liu, Parastoo Maleki, Pengfei Sun, Dr. Ramses van der Toorn, Rene Poelma, Robert Sokolovskij, Ronald Stoute, Dr. Saeed Khoshfetrat Pakazad, Dr. Sebastian Sosin, Dr. Serge Evseev, Dr. Sima Tarashioon, Siva Ramesh, Dr. Sten Vollebregt, Dr. Tao Chen, Dr. Thomas Moh, Dr. Vahid Mohammadi, Dr. Vijay Rajaraman , Dr. Vincent Henneken, Dr. Vladimir Jovanovic, Dr. Vladimir Milovanovic, Zahra Kolahdouz Esfahani and Dr. Theodoros Zoumpoulidis
English editing of my thesis	Sarah von Galambos
Dutch translation of the summary of my thesis	Miki Trifunovic
Family friends in the Netherlands	Family of Dr. Ali Mohammadi-Gheidari Family of Dr. Reza Lotfi
Love and encouragement	My family: Jaber, Ouldouz and Mohammad My brothers and their families: Kambiz, Azita and Kiana; Vahid, Nazanin, Mahyar and Arnica; Mobina, Aylin and in the memory of my brother Reza; My parents: Hedayat and Ferangiz

About the author

Negin Golshani was born in Oroumieh, Iran, in 1974. She received her Bachelor's degree in Electrical Engineering (Electronics) from the University of Tabriz in 1997. Then she worked at a company and at the University of Tehran (TFT laboratory of the Electrical Engineering Faculty) on crystallization of amorphous silicon layers. In 2005 she joined the K.N.Toosi University of Technology, Faculty of Electrical Engineering for her M.Sc. in bioelectric engineering. In 2006 she moved to the Netherlands. In September 2007 she started her Master of Science at the Microelectronics department of Delft University of Technology (TU Delft) Faculty of Electrical Engineering, Mathematics, and Computer Science (EEMCS). In 2008 she joined the Laboratory of Electronic Components, Technology and Materials (ECTM) and the Delft Institute of Microsystems and Nanoelectronics (DIMES), both part of the TU Delft, Faculty of EEMCS for her M.Sc thesis on SRAM in three Dimensional Integrated Circuits. She graduated in July 2009 then joined the Iszgro Diodes BV Company and worked on the documentation, fabrication and measurement of Electron Detectors. In January 2011 she started her Ph.D. on the development of Silicon Drift Detectors using Boron layer technology. She also co-lectured the M.Sc. IC technology course for two years.