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A Signal-Dependent Simultaneous Multi-Channel Quantization SAR-RAMP ADC Architecture for Implantable Neurorecording Microelectrode Arrays.

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September 21, 2025

Abstract

This thesis explores the design and evaluation of a novel multi-channel hybrid SAR–RAMP analog-to-digital converter (ADC) for high-density neural-recording probes by leveraging the spatial signal correlation between neighbouring channels. Increasing electrode counts in micro-electrode arrays (MEAs) demand compact, low-power signal acquisition. MEArec-generated neural signals were analysed at probe pitches of 10–50 µm, revealing that neighbouring channels in denser arrays often carry overlapping information. Exploiting this property, a hybrid ADC architecture was modelled in Simulink, combining the low-power binary-search algorithm of a successive-approximation register (SAR) with a ramp (RAMP) converter. System-level simulations show that, for 8-bit resolution, the proposed design achieves a 63% reduction in switching activity compared with a conventional RAMP ADC.

The 8-bit, 4-channel, 25 kHz sampling-rate (fs) hybrid ADC was implemented and analysed at system level in MATLAB/Simulink, examining the relationship between input signal characteristics and ADC performance. Finally, key circuit blocks were implemented in 1.1 V, 40 nm CMOS, including a sample-and-hold stage, a single-ended-to-differential dynamic switching scheme, a strongARM comparator, a binary-weighted CDAC, and the associated digital logic, demonstrating the practical feasibility of the proposed architecture.

Contents

1 Introduction

The ever evolving study of the brain circuits to understand various neural interactions such as thoughts, cognition, perception, and actions and the processes underlying neurological disorders and brain diseases, brain-computer-interfaces (BCI) and theurapeutic electroceuticals requires more, smaller and more power efficient recording probes. For this, implantable microelectrode array neural probes that can record with sub-millisecond temporal resolution from multiple neuronal cells are of utmost necessity. Implantable probes provide a much greater spatial and temporal resolution to access fine grained neural activity when compared to non-invasive electroencephalography (EEG) devices [1] and to less invasive electrocorticography (ECoG) devices [2].

The placement of EEG, ECoG and microelecrode arrays and other probes in the brain can be seen in figure 1 below. EEG and ECoG arrays are much larger and are placed on the surface of the brain either externally or internally however they do not record any signals that occur at a deeper in the brain. The probes will be discussed more in detail in chapter 1.1.

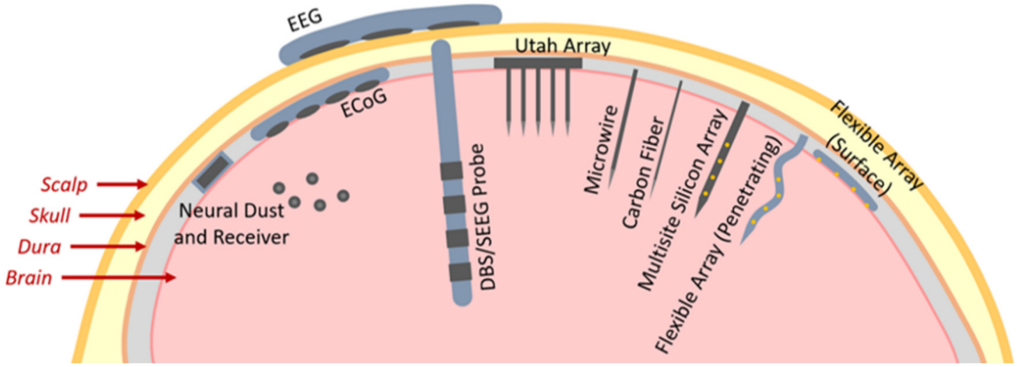


Figure 1: Neural electrode interfaces in the brain [3].

Large scale recordings of neuronal signals have proven to restore motor control through brain computer interfaces (BCI) [4][5], communication disabilities through speech-to-text [5] [6], hand control-to-text [7] and voice to speech synthesizers [8], hearing [5]. These approaches address impairments caused by conditions such as amyotrophic lateral sclerosis, spinal cord injury, stroke, and cerebral palsy [9].

From the new products released annually by neural probe companies and the ongoing advances in research, it is evident that neural array probes with an ever-increasing number of electrodes/channels [10] and smaller pitch sizes that allow for higher spatial resolution are still in demand. An overview of channel count trends through the years can be seen in Figure 2 below. One of the leading high-density CMOS probes, Neuropixels was updated 1.0 (2017) to the 2.0 version (2021) where the probe features a further pitch reduction from $20\mu m$ down to $15\mu m$.

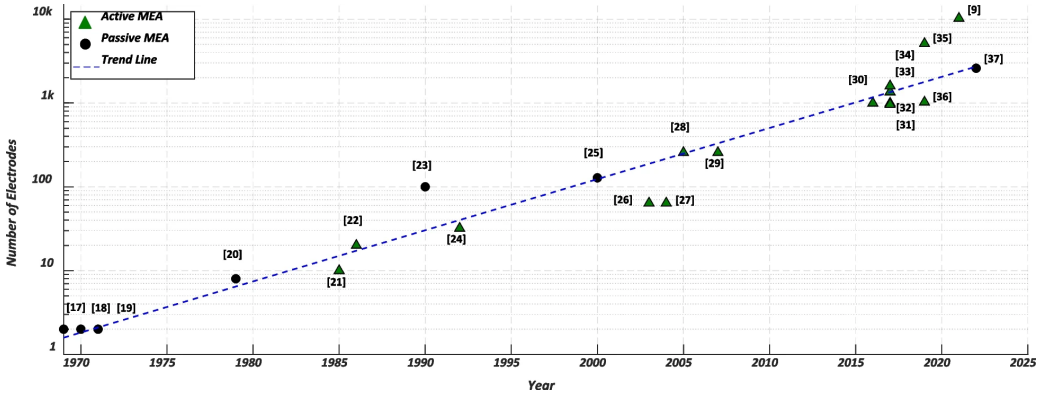


Figure 2: Exponential growth of channel number through the years [10].

The ever-growing number of recording channels enables denser and more area-specific signals, allowing clearer distinction between neuronal populations thus improving circuit-level mapping of local microcircuits and understanding fine-scale connectivity. This increased density also facilitates better spike sorting, as the closer proximity of electrodes improves single-neuron discrimination, while brain–computer interface (BCI) applications for prosthetics or neural decoding could benefit from more precise control and more precise feedback. However, higher channel counts come with the challenge of increased area requirements for routing, increased data to work with, and greater overall power consumption which directly translates to a higher temperature dissipation.

With the ever-increasing volume of neural data to be processed, a central research focus in on-implant signal processing is data reduction, encompassing spike detection, spike extraction and spike sorting (SS) [10]. These methods mainly focus on recording action potential (AP) (300 to 2000 Hz) spikes snippets and sorting them while disregarding local field potentials (LFP) band (0.1 to 300 Hz). Spike detection method allows a high temporal and spatial spike resolution with a huge power saving over recording all the brain signal spectrum of both LFPs and APs but there is a wide frequency spectrum of information that has proven to be useful that is ignored. It can be seen from Table 1, each frequency band carries its own specific information. Lower frequencies such as ISA, LFPs, and ripples are mainly investigated as research biomarkers for understanding network dynamics, seizures, and memory processes [11][12]. On the other hand, APs are used as primary signal source for practical applications such as BCIs. Nonetheless, LFPs and high-frequency oscillations are increasingly explored for clinical translation. For example, ISA waves have proven to detect epilepsy pre-seizure biomarkers minutes before a seizure occurs [12][13].

LFPs are usually ignored as they carry the same information as APs with a lower temporal precision and are usually seen to only offer insights into population-level activity. However, some studies have suggested that purely AP-based BMI/BCIs are not as robust for chronic recordings as LFP-less based solutions are more susceptible to tissue reactions degrading the recorded signal [14][15][16] and drift which may require frequent calibration and continuous assistance of technicians to maintain performance [14][17][18].

Table 1: Frequency bands recorded with implantable neuro-shank probes

Signal class	**Band**	**Applications**
Infra-slow activity (ISA)	0.01–0.1 Hz	Seizure onset detection
Local Field Potentials (LFP)	0.1–300 Hz	Network oscillation analysis, synchrony studies
Ripples (physiological HFO)	80–250 Hz	Memory consolidation research
Fast ripples / pathological HFO	250–500 Hz	Epileptogenic-zone localisation, anti-seizure stimulation
Spike / multi-unit activity	300–3000 Hz	Single-neuron coding, spike sorting, BMI/BCI
Very-fast ripples / axonal spikes	600–2000 Hz	Axonal conduction studies, ultra-fast oscillations

1.1 Neural signals and probes overview

Having looked at the possible application achievements of high density recording arrays, channel count trends with generated information amount challenges that come with them and the importance of specific neural frequency bands, it is important to understand the possible microelectrode probes that exist and what challenges do they bring with them at this level. The following chapter will delve into a short overview of micro electrode array families, exploring their constraints and limitations.

1.1.1 Micro electrode array families

Figure 3 groups implantable neural probes into four families: passive silicon probes (Red), active dense CMOS probes (Blue), microwire probes (Yellow), and flexible probes (Green). Since the Michigan probe (1970) [19] demonstrated lithography-based array fabrication possibilities, and the Utah array (1997) [20] introduced a high-density 3D silicon array, probe architectures have diversified in pursuit for a greater channel count, higher spatial density, improved power efficiency and enhanced chronic performance.

The first neural recordings used glass micropipettes[21] (1940s-1950s), which enabled intracellular measurements but were fragile and limited to single sites. In the 1950s-1960s, metal microelectrodes such as tungsten and platinum-iridium wires became widely used, allowing extracellular single-unit recordings. These probes were simple and provided limited spatial resolution. In the 1970s, the Michigan probe [19] was introduced as the first high-density, silicon-based planar probe for intracortical recordings. This showed the potential of new lithography-based manufacturing techniques for neural probe arrays. In 1997, the Utah array followed suit introducing the first high-density silicon-based 3D array. These were the first passive array probes to be introduced. Passive probe arrays are referred as such because they route all the signals from the individual electrode sites to the base where all of the signal processing is performed. With advances in miniaturization brought by CMOS manufacturing technology brought other improvements, probes shifted to integrating the analog front end (AFE) and analog to digital converter (ADC) directly beneath each electrode site [22][23]. Moving the whole signal conditioning circuit (amplification, filtering and digit) allowed to significantly reduce the area taken up by the interconnection wires which grows with each added channel and the amplification and filtering circuit closer to the electrode site reduces noise and interference on the already small signal. Less interconnect wiring means that even more electrodes can be placed on the probe. However, these high-density monolithic probes have the disadvantage of being a rigid body, which may, during the insertion or through micro-motion when in place, cause tissue damage and inflammation, igniting a foreign body reaction that prematurely scars the tissue

around the probe which reduces the recorded signal. Microwire neural probes offer a solution for this problem with the small individual electrode strands. The individual insulated metal electrode strands are placed into the brain in various locations and create minimal electrode local glial response. This allows for longer chronic recording as the recorded signal does not degrade as quickly, however this is traded for the high resolution of the array. Recently, a new solution has emerged that combines the high spacial density of monolithic arrays and the flexibility of microwire probes. These are referred to as flexible probes. These devices can be easily implanted with temporary rigid shuttles/stiffeners [24], or fabricated from mechanically adaptive materials that are initially stiff during insertion and then soften in vivo within minutes [25]. All of the above described probes location in the brain is illustrated in Figure 1.

1.1.2 Thermal constraints

Moving circuits like the AFE from the base to the shank relocates heat generation into brain tissue, tightening the allowed thermal limits. It has been globally recognised that implants should not raise local temperature by more than 1 °C [26]. Studies using finite element modelling (FEM) have reported maximum allowed power budgets for high-density probes to not exceed the 1°C limit: The NeuroSeeker probe has reported the maximum power dissipation allowed to be 5 mW for the implanted shank and 45 mW for the base [27]. Some other probes like the NeuroPixel have published more stringent power dissipation ceilings allowing only 1.8 mW in the shank and 20 mW at the base [28]. This requirement may be a challenge for on shank integrated architectures like the Sigma-delta ADCs which already tend to dissipate more power than SAR equivalents, further emphasizing careful power allocation requirements.

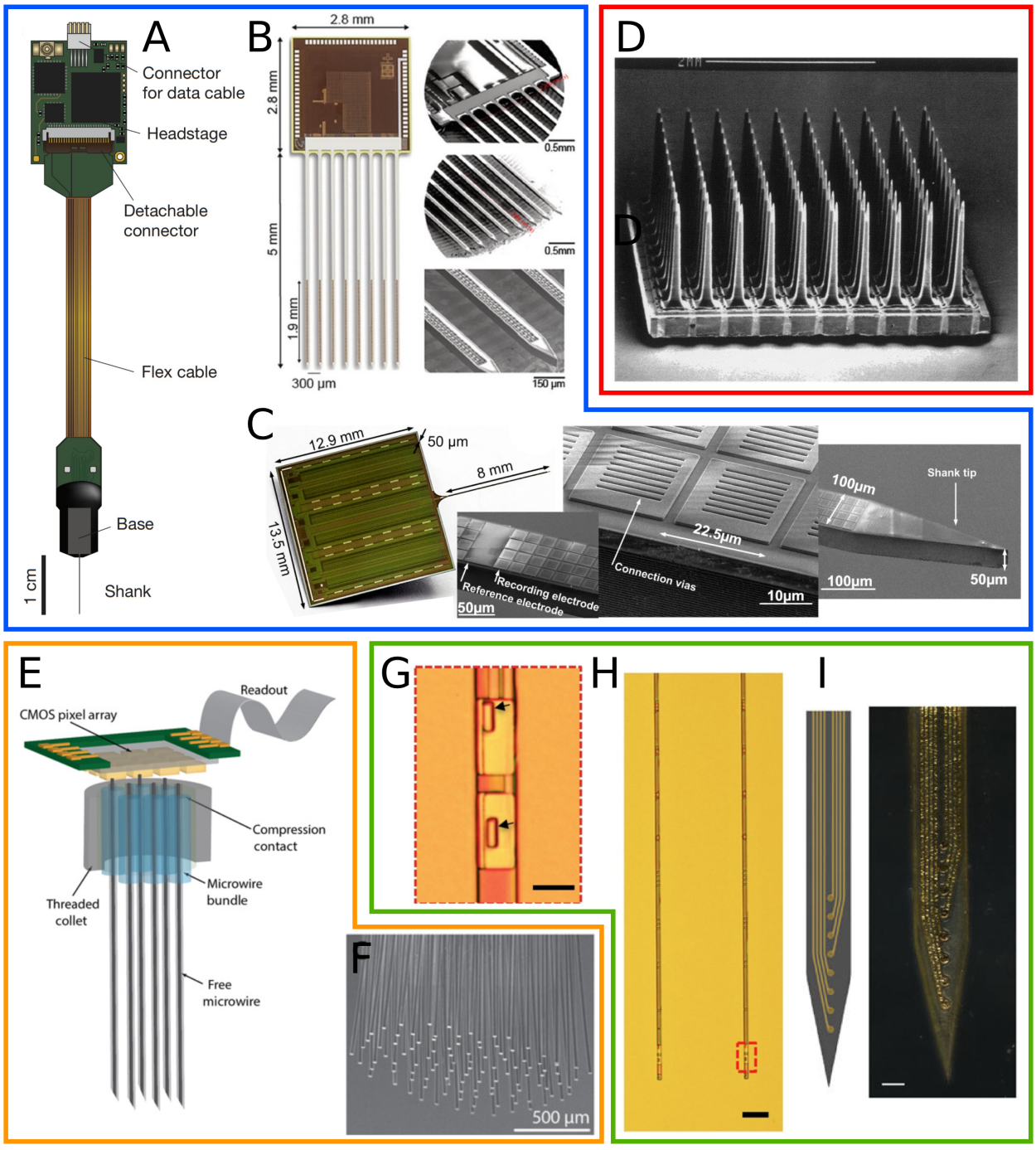


Figure 3: (Blue section): Active CMOS dense neural probes**(A)** Neuropixel 1.0 probe [29]. **(B)** 8-shank SiNAPS probe at different magnification levels [30]. **(C)** NeuroSeeker probe [31]. (Red section): Passive silicone probe. **(D)** Utah array [32]. (Orange section) Microwire neural probes: **(E-F)** bundle of microwires mated to a large-scale microelectrode array for signal acquisition [33]. (Green section): Flexible probes.**(G-H)** Nanoelectronic thread probes (scale bar 10 μm)[34], **(I)** Neuronexus Mechanically-adaptive, resveratrol-eluting (MARE) neural probe [25].

1.2 Neural application ADC overview

Conventional implantable neuro recording Nyquist rate ADC systems consist of an analog front end that amplifies and filters, followed by a mixed signal part consisting of a sample and hold circuit, comparator, and finally a digital back end used to process the decoded information i.e. compression, signal sorting, a memory bank. Finally this is transmitted outside of the body by means of a wired connection terminal or a wireless link. Such a system is illustrated below in 4.

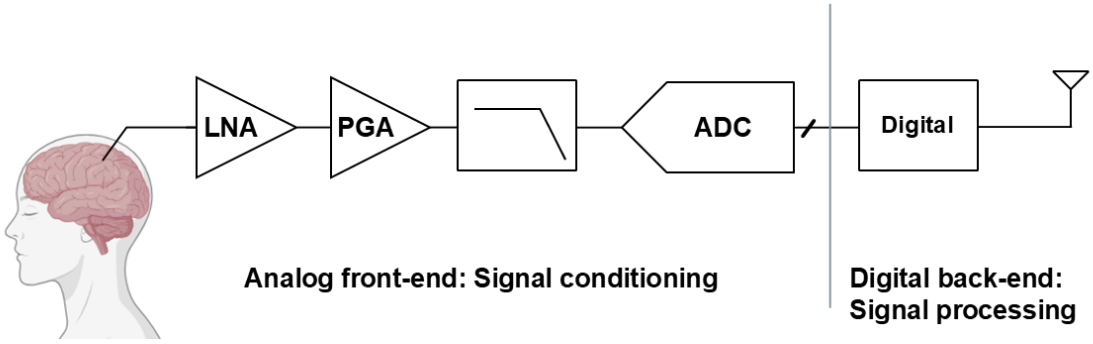


Figure 4: Classical analog-to-digital implantable neurorecording signal path.

Focusing specifically on implantable MEA neural recording application ADCs it is difficult to draw a definitive conclusion from existing literature for the area and power consumption of the ADC, AFE or the full system. Published designs offer widely different system implementations. The first major distinction is the physical location of the circuitry: (i) fully integrated AFE+ADC on shank, (ii) AFE on shank with all the ADC and signal processing at the base, (iii) fully passive arrays that do all of the processing at the base. These three system implementations strongly influence how area and power are optimized, with base-mounted solutions typically incurring higher power dissipation and a larger area compared to on-shank integration because of relaxed temperature and area constraints. Secondly, designs differ in terms of recordable bandwidth: some have programmable filters for tunable bandwidths focusing on recording either APs or LFPs or both, others may have only a static one. Thirdly, a large number of systems focus on APs with event driven system on chip (SoC) that record specific time snippets or perform spike sorting which tends to reduce overall power consumption. Additionally systems range typically from 8 to 12 bits with some $\Sigma - \Delta$ designs offering up to 14 bits resolution. Metrics that tend to match across all designs is the input referred noise: this tends to be around 5 to 10 μV_{RMS}. The noise is chosen in this region such to be able to resolve the smallest possible signal input. An analysis was performed for MEA ADC system implementations, the full Table 7 can be found in the appendix, here in Table 2 a shortened version of for all of the above mentioned parameters is presented. In Table 2 an additional row "architecture" is added which describes the implementation being either AFE on shank and the digital part on the base (AFES+ADCB), or non separated full shank (FS) implementation.

Table 2: Architecture performance comparison of MEA recording SoCs.

	[28]	[31]	[35]	[36]	[37]
Architecture	AFES+ADCB	AFES+ADCB	FS	FS	FS
Topology	SAR mux	SAR mux	SAR mux	RAMP	$\Delta\Delta\Sigma$
multiplex ratio	12	8	8	NA	NA
Bits/ENOB [bit]	10/8.16	10/-	10/-	8/-	-/10.9
Technology [nm]	130	130	180	28	180
Supply [V]	1.2/1.8	1.2/1.8	-	1	0.5/1
Input Noise [μVrms]	6.36 (AP)	12.4/50.2 (AP/LFP)	10.4 (AP)	7.4 (AP)	3.32 (AP+LFP)
Area/ch. [mm^2/ch.]	0.12	0.12	0.219	0.00129	0.058
Power/ch [μW/ch.]	49.06	45	5.9	0.496	3.05
fs [kS/s]	30	40	24.4	20	25
BW [Hz]	0.5-10k	0.5-8k	300-5k	300-5k	0.5-7.5k

The main metrics that are important in neuro-recording AFEs and ADCs are: Area, power dissipation, channels crosstalk noise, input reffered noise and data throughput. The analysis will primarily focus on power and area.

Currently the most common ADC topologies in neural MEAs recording of a full frequency spectrum spanning both LFPs and APs that are used are:

1. SAR: Successive approximation ADCs are very power efficient for moderate resolutions (8-10bits), but tend to be rather large in size because of the area taken up by the CDAC. Most neuro recording systems have on average between 4 to 16 channels multiplexed onto a single ADC.

2. Σ–Δ: Sigma delta ADCs are extremely popular as they are rather small and offer a low noise due to its noise shaping properties which is beneficial for low frequencies such as LPFs where 1/f noise is dominant. The main disadvantage that they pose is a comparably high power consumption compared to the SAR due to the high frequency required and the power consumed by the decimation circuit at the digital side.

3. VCO: Voltage controlled oscillator ADC are growing in popularity these last years. They have an ultra-compact area footprint, a low power consumption due to the mostly digital based circuitry and offer good scalability with newer technologies.

4. Ramp/Single slope (SS): Ramp ADCs are quite attractive because of their area efficiency. They use a single global ramp signal which allows an easy expandability for extra channels. They have seen some popularity in ECOG applications, however they do not seem to be as popular in the domain of MEA ADCs because of high channel crosstalk.

It is observed that most systems designed for recording full-bandwidth spectra rely on generic ADC topologies that have been adapted to the specific application. This raises the question of why designers have not explored application specific architectures that leverage inherent signal characteristics to enhance the area and power efficiency of ADCs. Although ADCs based on level crossing detection demonstrate the viability of signal-dependent conversion, such approaches remain confined to action potential (AP) recording [38][39].

An ADC architecture which has not been seen in neuro recording but has seen uses in other applications that demand higher bit resolutions e.g., instrumentation, imaging is the hybrid ADC which combines a SAR and a ramp ADC for a coarse + fine search. Such a system is referred to as a hybrid ADC or SAR-RAMP hybrid. It offers the best of both worlds between a SAR algorithms power efficiency due to its search algorithm and a ramp ADCs area efficiency. This specific architecture has yet to be explored in the application of MEA recording.

1.3 Problem statement

Intracranial neural probes are increasingly incorporating larger numbers of channels with higher spatial densities, which places new demands on signal acquisition, processing and routing. However, power and area remain strictly constrained by physiological safety constraints, such as thermal dissipation limits within the brain tissue and risk of tissue damage from large implants that compromise long-term implant biocompatibility. Despite the unique bandwidth characteristics and statistical properties of neural signals, all current systems continue to rely on generic ADC architectures, such as large time-multiplexed SARs converters, power-hungry $\Sigma - \Delta$ modulators and slow single-slope designs. This raises a fundamental question: is it possible to design an ADC architecture specifically optimized for neural signals while operating within stringent power and area budgets?

1.4 Proposed solution

This work proposes a multichannel hybrid SAR-ramp ADC that exploits the neighbouring channel signal similarities that occur in higher density probes. The ADC architecture aims to reduce the area per channel consumed by sharing a single DAC between channels compared to a single channel-single SAR solution, while the logic aims to take advantage of a binary search method across channels simultaneously to minimize comparison count and save power compared to a global ramp solution.

2 Neural signal and probe analysis

Understanding the effects of electrode distance and the signals is crucial for the proper design of the proposed ADC. This chapter delves into an analysis of signal correlation between the different channels through the means of simulated neural signals for different probe electrode pitch sizes. The open source python based simulator MEArec is used to generate the extracellular signals. It offers a wide variety of library and user custom defined probe designs.

2.1 Probe dimensions and electrode layout

Common array layouts reported in the literature and available commercially include single-column electrodes, planar 2D grids, staggered (hexagonal) 2D grids, and 3D arrays (e.g., the Utah array). The planar and staggered/hexagonal layouts are the most prevalent. Table 3 lists probes with the smallest commercially available electrode pitches; these values define realistic reference ranges for the simulations in the subsequent analysis.

Table 3: Commercially available probe electrode pitches.

Probe	**Pitch**	**Array Layout**	**Channels**
NeuroNexus - A4x16-Poly2-6mm-20s-stag-190-160 [40]	20μm	staggered	64
Cambridge NeuroTech [41]	25-50μm	staggered	16-128
Maxwell Biosystems - MaxTwo [42]	17.5μm	staggered	26400
3Brain - MCorePlate 1W 27/42 [43]	42μm	planar	4096
Blackrock Neurotech - 96 NeuroPort Electrode [44]	400μm	planar	16-1024
Neuropixels 1.0 [45]	16/20μm (row/col)	staggered	384
Neuropixels 2.0 [46]	15/32μm (row/col)	planar	384

2.2 Generated neural data spatial analysis

In the following analysis, the Neuronexus-32 probe was chosen. The probe is available in the standard library of probes of MEArec. It consists of a three staggered column array of 32 channels. The probes electrode pitch was then later modified to demonstrate the correlation and neighbouring channel signal differences which will become more relevant in the following chapter.

Simulations were performed in MEArec with physiological rotation disabled to fix neuron orientation, isolating electrode-pitch effects on neighbouring-channel cross-correlation and on the maximum difference within four-channel clusters. Results are therefore interpreted as orientation-invariant trends. In vivo, orientation variability due to physiological rotation would be expected to reduce neighbouring-channel cross-correlation and slightly increase maximum inter-channel differences; these effects are often small at very tight pitches. The rest of the simulation settings were kept as default with a slightly increased number for neuron to surface density such to reflect brain tissues.

The baseline probe simulation is performed with the original Neuronexus32 probe that can be seen in Figure 6. The simulated channel positions can be seen in Figure 5. Each channel is separated with a distance of $25\mu m$ vertically, $18\mu m$ horizontally and the middle column is offset vertically compared to the left and right column by 12.5μm.

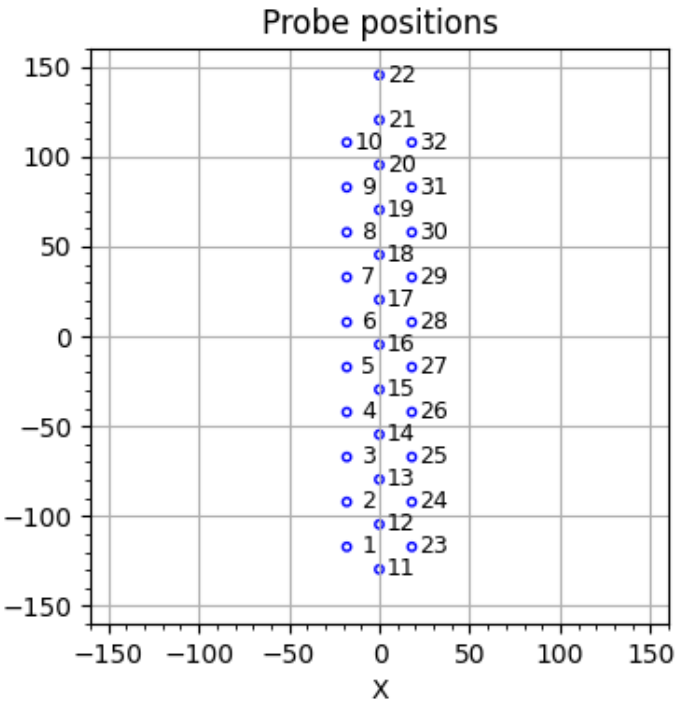


Figure 5: Simulated neuronexus 32 probe.

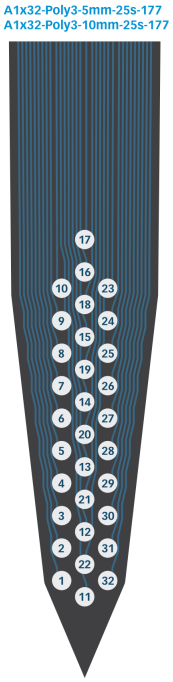


Figure 6: Neuronexus32 probe [www.neuronexus.com].

Performing a correlation between all channels of the probe reveals that the signal between the channels is correlated with their position on the probe. In Figure 7 it can be seen that the most correlated parts occur in a diagonal fashion in 9 locations of a similar diagonal pattern. Because the plot is symmetric along the main diagonal, the top right three quadrants are just repetitions of the bottom left three thus the numbering for them is ignored. These quadrants are split up and numbered in Figure 8. Regions 1, 2 and 3 correspond to the signal correlation for channels that are nearby within the same column and correspond to the left, centre and right column respectively. Regions 4 and 5 correspond to the horizontal spacial signal correlation between the left to centre and right to centre channel columns. Finally region 6 is the horizontal correlation between the left and right channel columns. As expected, the diagonal correlation values in region 6 are smaller than in the other regions as the two columns are spatially further apart.

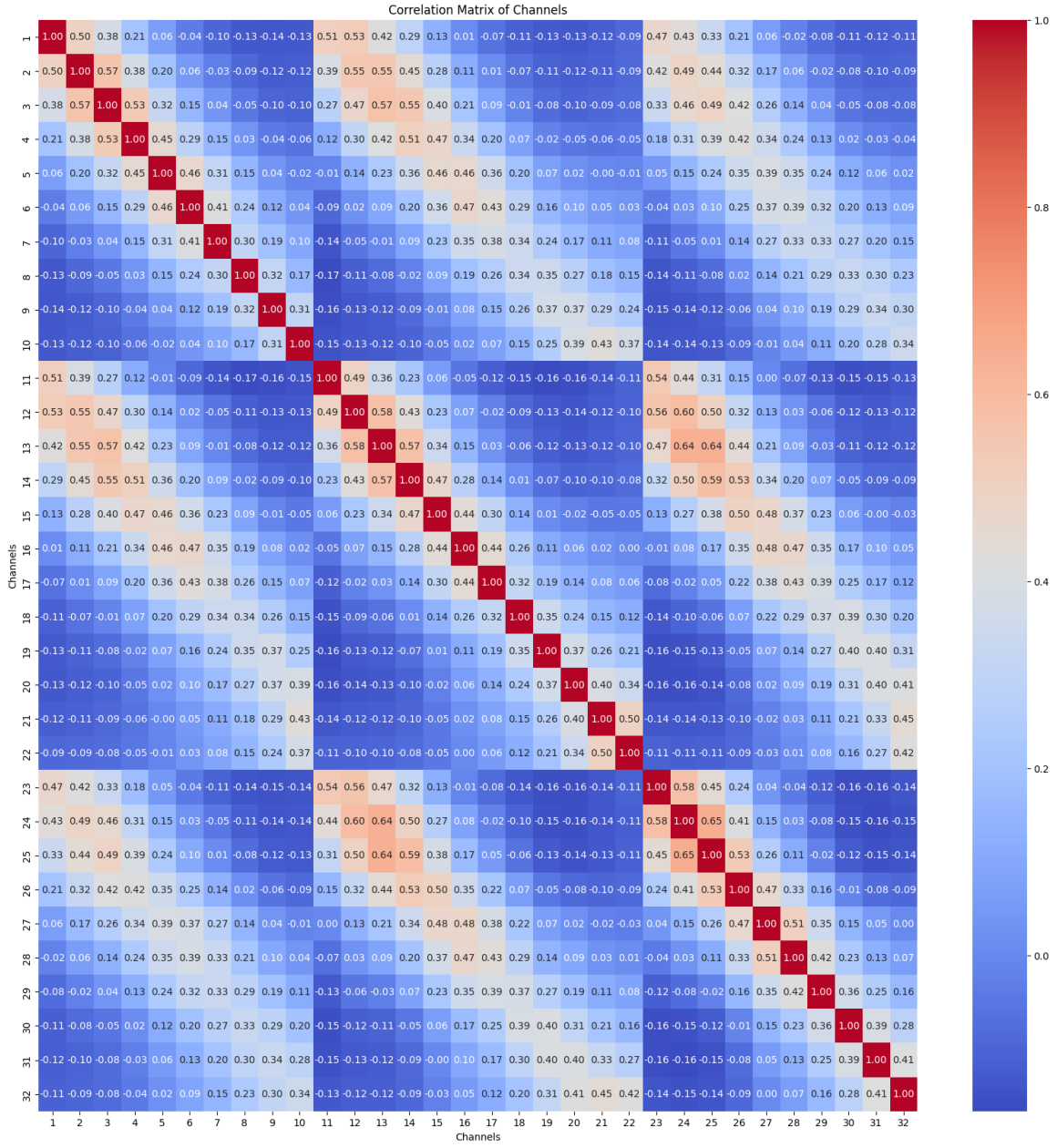


Figure 7: Neuronexus-32 (25um pitch) probe channel correlation.

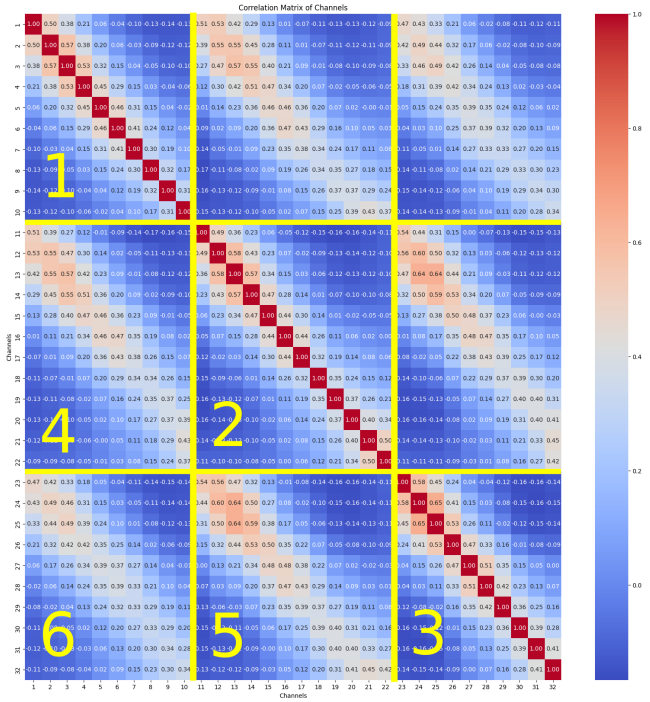


Figure 8: Neuronexus-32 probe channel correlation regions.

Three different pitches of the same probe layout were simulated in MEArec using the same seed. The pitch sizes were chosen to be $50\mu m$, $25\mu m$ and $10\mu m$ as these sizes align with what exists as seen in Table 3. As expected, it can be seen from the three Figures 9, 10 and 11, that the cross-correlation between channels increases significantly as the distance between electrodes reduces.

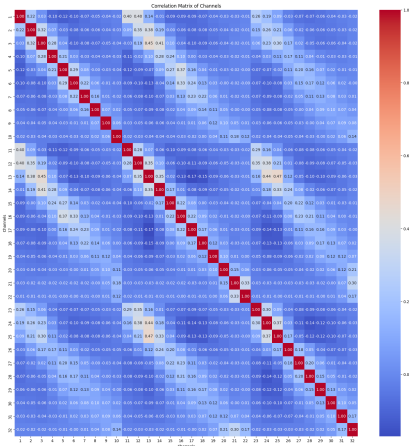


Figure 9: $50\mu m$.

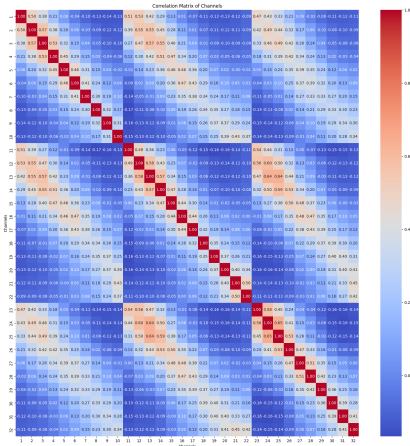


Figure 10: $25\mu m$.

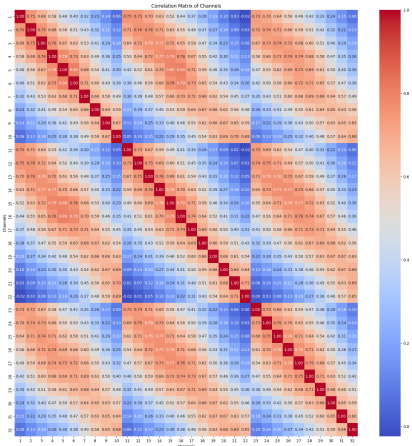


Figure 11: $10\mu m$.

Figure 12: Probe signal cross-correlation for varying probe channel pitches.

2.3 Bit redundancy

Higher inter-channel correlation indicates a higher signal redundancy being recorded as neighbouring channels could be seen carrying part of the same information. Consequently, the per-channel information content is reduced, allowing a lower per-channel quantization depth (bits/sample) without a meaningful loss in overall signal quality.

In the case that the signal is Gaussian distributed then the mutual information between two variables with correlation ρ is given as:

$$I(X;Y) = -\frac{1}{2} log_2(1-\rho^2). \tag{1}$$

By taking a cross correlation between two between two physically adjacent channels, e.g., 15 and 26 of the probe and comparing the effect of bit saving from the change of probe pitch from $25\mu m$ to $10\mu m$ this results in a gain of:

$$\begin{aligned} \Delta I &= -\frac{1}{2} log_2(1-0.76^2) + \frac{1}{2} log_2(1-0.5^2) \\ &= 0.621 - (0.208) \\ &= 0.413 \text{ bits} \end{aligned} \tag{2}$$

The heatmap seen in Figure 13 below shows the overall bit saving across the whole probe for a change of channel pitch from 25 to $10\mu m$.

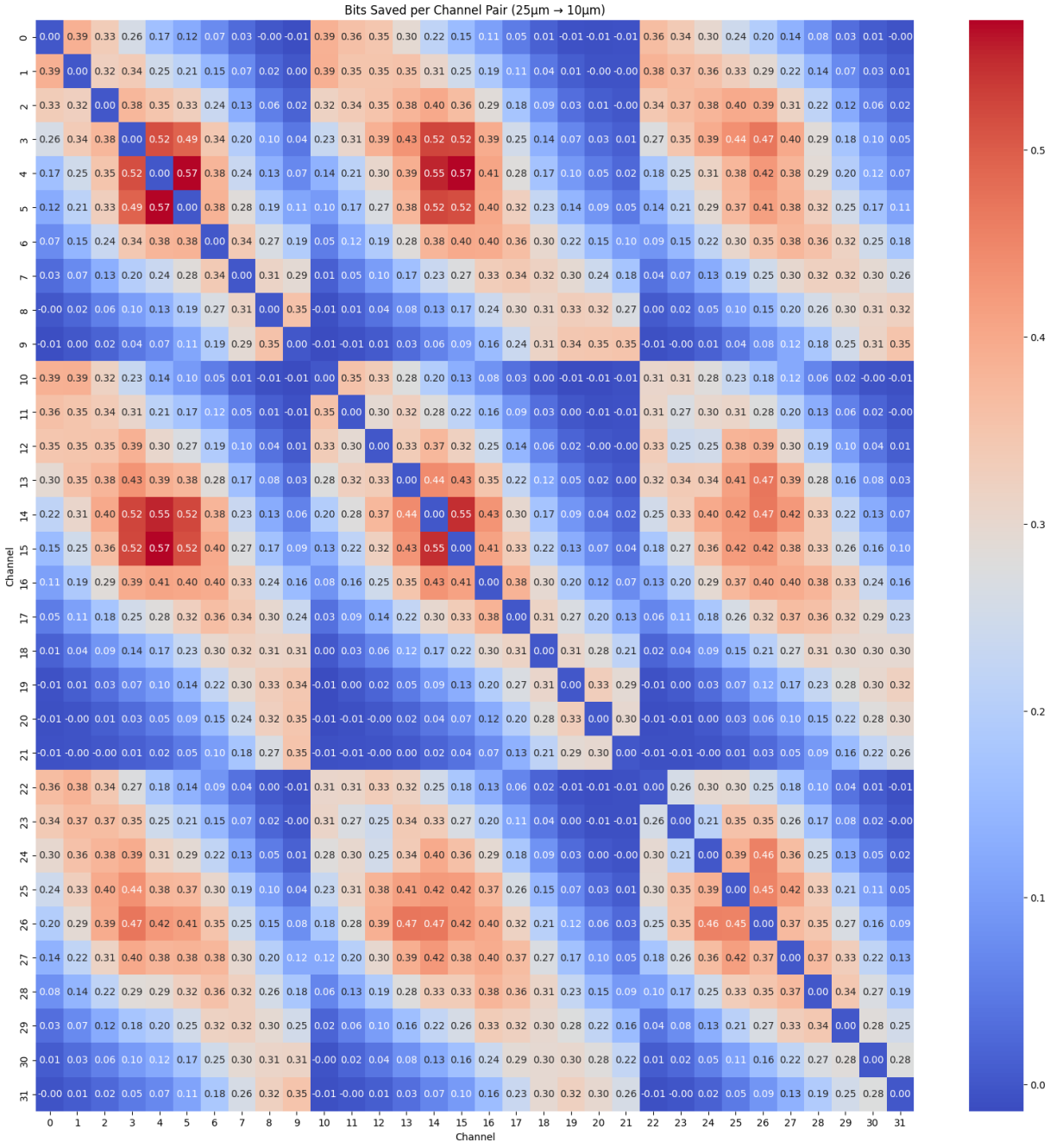


Figure 13: Neuronexus-32 probe bit save from 25um to 10um.

An additional analysis was performed for seeing the effect of bit redundancy for different neural signal bands. LFPs have a much higher bit redundancy from channel to channel compared to AP. Similar trends have been reported in other neuro-recording applications. However, this analysis does demonstrate the trend of the possibility to reduce the required bit resolution from current ADC resolutions but as of yet the bit gain is not significant.

2.4 Differential analysis of neighbouring neural data signals

The generated neuro signals of the 25μm pitch probe are scaled to fit the input range of the ADC. This thesis does not examine circuit-level implementations. In practice, MEA front ends typically use one of three schemes: (i) single LNA per channel with fixed or coarse gain, (ii) a

single LNA per channel followed by a often shared programmable-gain amplifier (PGA) before the ADC in the case of a multiplexed ADC, or (iii) a per channel LNA whose gain is itself programmable. A cluster of four neighbouring channels was taken and the differences between each channel was computed. The absolute maximal and minimal differences amongst the cluster were taken and plotted against time and are seen in Figures 14 and 15. The first one (fig. 14) is for the whole input spectrum, and the second one (fig. 15) is for LFPs only. The input difference is an important extra metric in addition to the correlation matrix seen above: the correlation matrix only shows the trend of the change of one channel to another. Here, the input difference metric is explored that shows the minimum and maximum differences between all four channels. As it will be seen later in Section 4.1, the maximum ΔV_{in} will be a limiting factor in overall system performance.

On the right-hand side of Figures 14 and 15, the probability density function (PDF) can be seen. This shows the probability of having a specific ΔV_{in} input. As it can be seen from the PDF plots, the PDF of the max ΔV_{in} of the LFPs has a smaller LSB variance whose mean also falls at a much smaller LSB value. The peak of the PDF drops from around 18LSBs for APs (fig. 14) down to 2.6 LSBs for the LFPs(fig. 15). This shows that if the system would be to function for only LFP recording, it would be an advantage to the system in the case the signal value proximity was to be explored. The following Chapter will propose a system solution based on this signal proximity between neighbouring channels and will explore the effects of this signal difference on the overall performance of the proposed ADC.

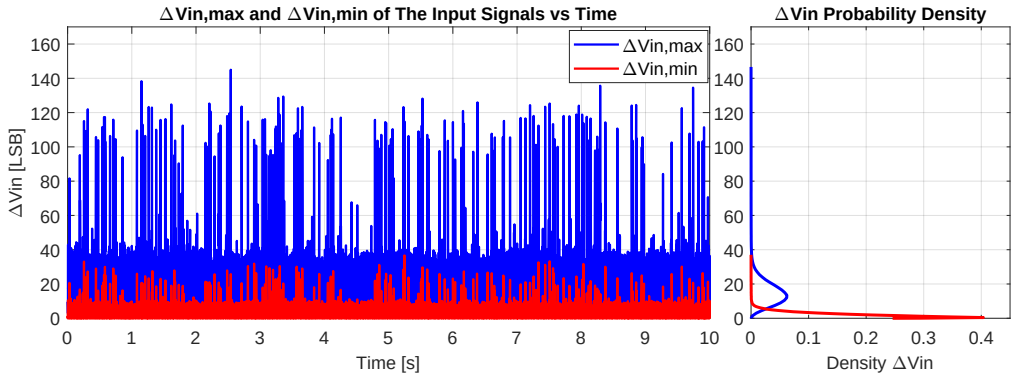


Figure 14: ΔV_{in} extrema of 4 channels time plot and its signal density probability.

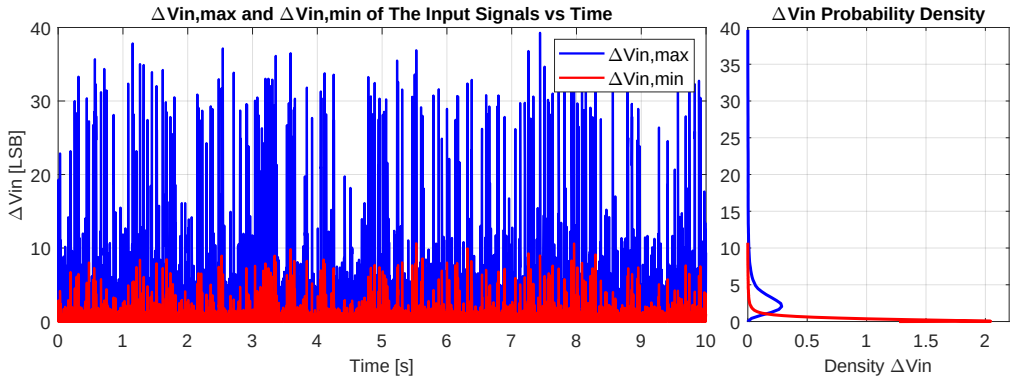


Figure 15: ΔV_{in} extrema of 4 channels filtered LFP time plot and its signal density probability.

3 System level design and implementation in Simulink

This chapter explores the implementation of the conceptualized ADC system within the Simulink environment. It begins with a concise overview of the system architecture, its operational principles, and its distinctions from other hybrid ADC designs. Subsequently, a detailed quantitative analysis of system performance is presented, based on Simulink simulations, which investigates the impact of input channel signal differences on the overall comparison count. The chapter concludes with a simulation employing the neural recording signals introduced in Section 2.2, comparing the proposed system's performance against a SAR and a simulated ramp ADC.

3.1 System description

The proposed system is a combined idea of both SAR and ramp ADC architecture, but not in a pipelined or subranging (coarse + fine) fashion. The proposed system idea consists of having several channels share one DAC for their conversion steps on multiple channels for both SAR and RAMP operation. It could be simplified in technical terms to a limited channel count RAMP ADC with an accelerated search algorithm. The comparators and registers used throughout the decoding also stay the same for each channel. The proposed system level architecture implemented in Simulink is presented in Figure 16.

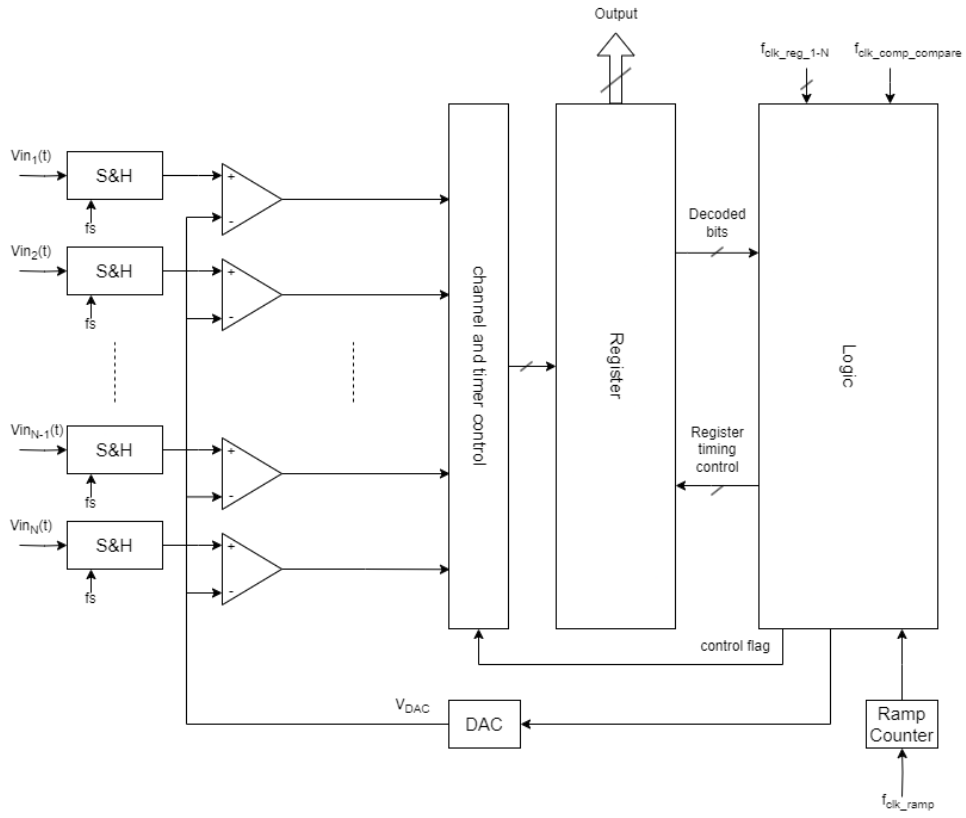
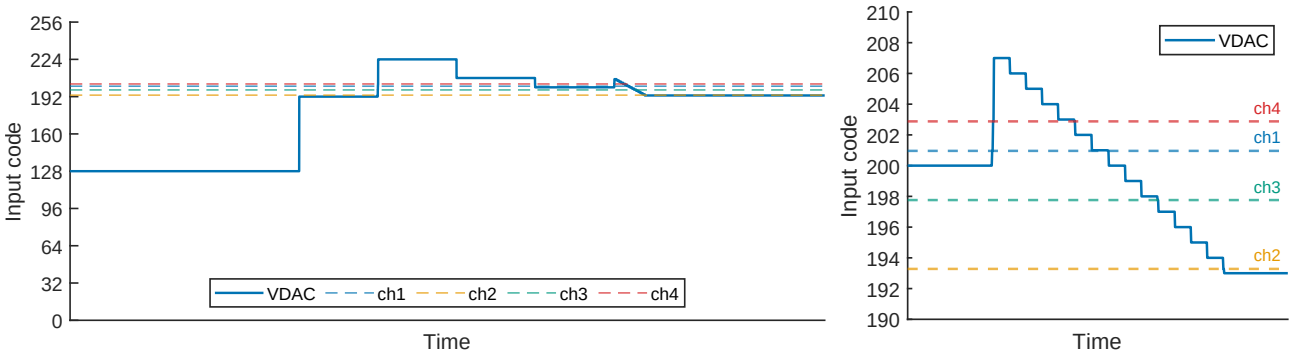


Figure 16: Proposed system architecture.

3.2 Functioning principle

The basic functioning logic can be described as follows: Firstly, each channel is sampled and held on their own respective sampling circuits. Secondly, the system starts its comparison

commencing in the SAR logic comparing all sampled values to the DAC generated voltage reference simultaneously. If all outputs are the same at the end of the comparison, then the next DAC voltage level is chosen as if it was a SAR. This continues until the channels comparator output differs. The difference means that one or more channel values fall into different binary coded areas. After this, the system switches to ramp mode. The DAC voltage goes back to the previous voltage and starts ramping up. When a channels comparator output is detected the corresponding voltage DAC code is stored in the register of that specific channel. When all channels are resolved all outputs will be the same again and some logic signals the DAC to stop ramping up. The described functioning steps are illustrated by means of the four channel inputs and the DAC voltage in Figure 17 below.



(a) DAC voltage with 4 inputs plot for a single sample T_S.

(b) Zoomed in ramp section.

Figure 17: Proposed system DAC voltage search algorithm steps.

The system level analysis was used to conceptualize and implement the system starting from the logic, to data paths, and required clocking schemes. It was not used to perform power or area estimates, however it did allow for the analysis of the comparison count in terms of the effect of the input signal. The comparison count is relevant to an extent as it can be extrapolated to power consumption used by the comparator and the DAC. The subsections below will go further into depth into the performance analysis which was defined in terms of comparisons performed. It will explore the effects of input signal difference and input signal mean positioning in the input range.

3.3 System step count

The number of comparisons performed by the proposed ADC is very dependant on the input signals as it will determine how many steps will be performed by the SAR and the RAMP parts of the ADC. The general worst case comparison count only regarding SAR-RAMP partitioning can be described by:

$$N_{comp} = \begin{cases} N_{ch} \cdot n_{SAR} & , n_{RAMP} = 0 \\ N_{ch} \cdot \left(2^{n_{RAMP}} + n_{SAR} + 1\right) & , n_{RAMP} \neq 0. \end{cases} \tag{3}$$

Here N_{comp} corresponds to the total comparison count, N_{ch} to the number of channels used in the system, and n_{SAR} and n_{RAMP} correspond to the amount of bits resolved by the SAR and the RAMP section respectively. For the case $n_{RAMP} = 0$, the system performs fully in SAR ADC mode.

This can be simplified into the worst and best case scenario comparison count and is shown in comparison with a normal SAR and ramp ADC in Table 4 below.

Table 4: Comparison count per architecture.

	SAR	RAMP	SAR-RAMP hybrid	This system
Worst case	$N_{ch} \cdot n$	$N_{ch} \cdot 2^n$	$N_{ch} \cdot ((n-a) + 2^a)$	$(N_{ch} - 1) \cdot 2^n + 2^{n-1}$
Best case	$N_{ch} \cdot n$	N_{ch}	$N_{ch} \cdot ((n-a) + 2^a)$	$N_{ch} \cdot n$

4 System level analysis and results

4.1 System comparison count vs signal.

The system comparison count can be quantified and estimated by performing a system analysis by sweeping the mean of the channels signals across the full range while having different max channel signal input differences. In all of the following comparison count plots, the x-axis represents the DC mean of all channel signals, while the y-axis shows the number of comparisons required to fully resolve all four channels. The plots were generated by having two channels at $V_{ch1,ch2} = V_{DC} + \frac{\Delta V_{in}}{2}$ and the other two channels at $V_{ch3,ch4} = V_{DC} - \frac{\Delta V_{in}}{2}$.

4.1.1 4 bit system

A 4 bit system simulation is used to clearly demonstrate the functioning of the proposed system. As seen in Figure 18, the 'proposed ADC' curve has a baseline and a couple of peaks that sit at different heights. The baseline is the minimum number of comparisons that can be performed. This is when the system functions fully in SAR mode thus only:

$$N_{comp} = n_{ch} \cdot n = 4 \cdot 4 = 16 \text{ comparisons.} \tag{4}$$

It can be noticed that the peaks occur on the SAR decision levels. The highest peak is in the middle at 8lsb which corresponds to the MSB, the second largest peaks occur at 4 and 12lsb and finally the last peak at the 3rd MSB at 2, 6, 10 and 14 lsb codes. The downwards stairway section of each peak is the region where the RAMP takes over the functioning.

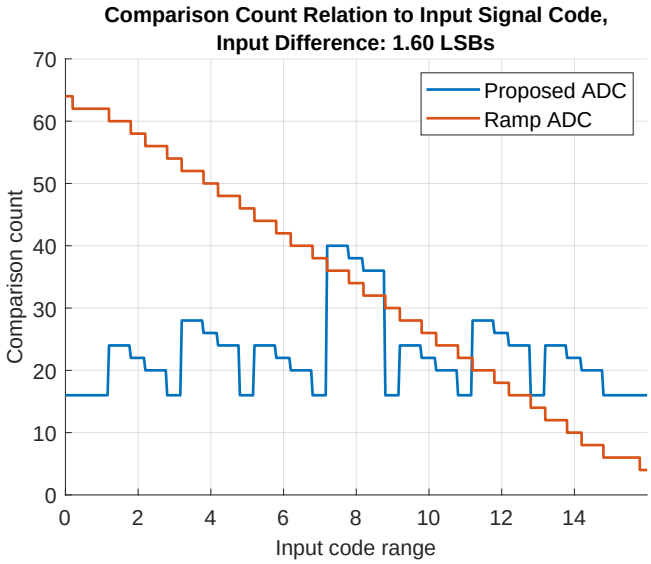


Figure 18: Comparison count vs signal for 4 bit system with input difference: 1.6 LSB.

As the signal difference ΔV_{in} increases, the peaks grow and start to take the ramps shape as it can be seen in Figures 19 and 20 below. Additionally it can be noticed that the proposed ADCs comparison count increases above the ramp ADC equivalent in two cases. The first case is inherent to the system design as it consumes one extra cycle to detect different SAR comparison outputs and then switch to a ramp functioning. This is the offset by 1 comparison upwards and is best seen on the largest peak. The second case is at the largest input. This occurs because the ramp comparison has to take less steps to decode the output but the proposed system needs to first search through the first couple of SAR bits before engaging the ramp. As the number of bits of the system increase the relative difference becomes negligible.

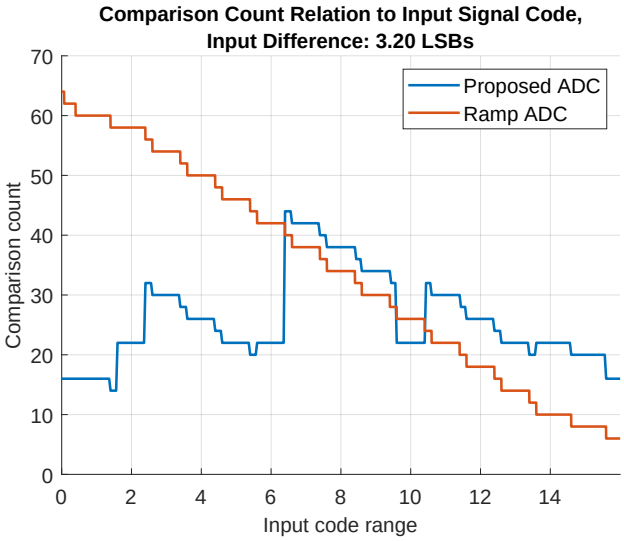


Figure 19: Comparison count vs signal for 4 bit system with input difference: 3.2 LSB.

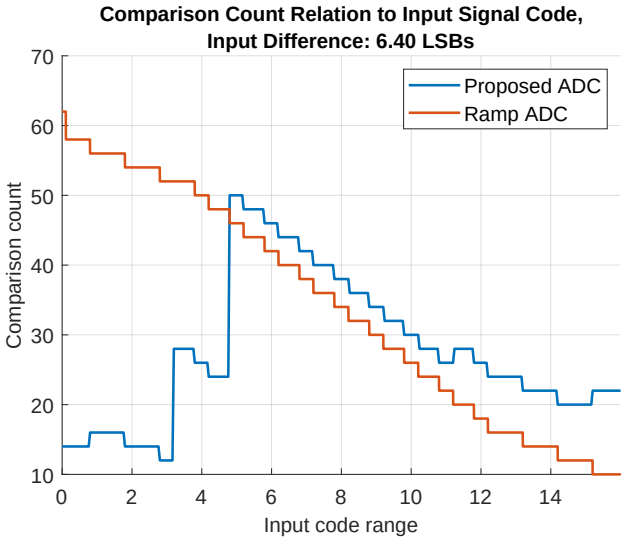
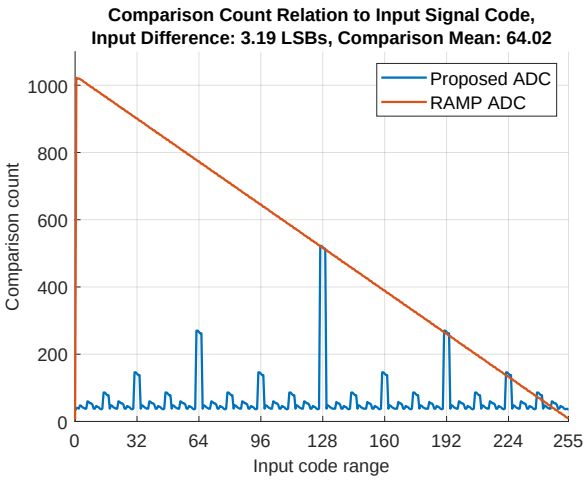


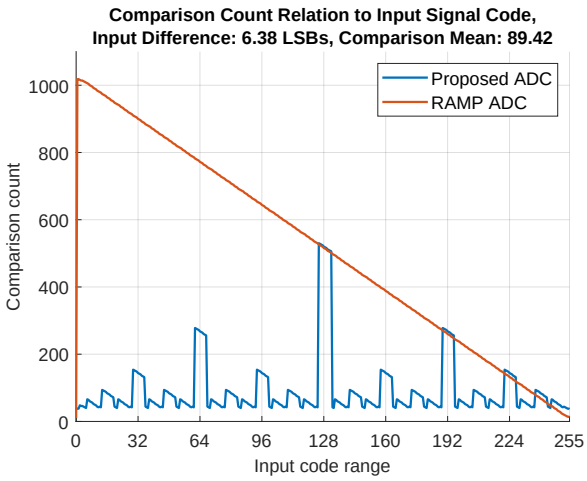
Figure 20: Comparison count vs signal for 4 bit system with input difference: 6.4 LSB.

4.1.2 8 bit system

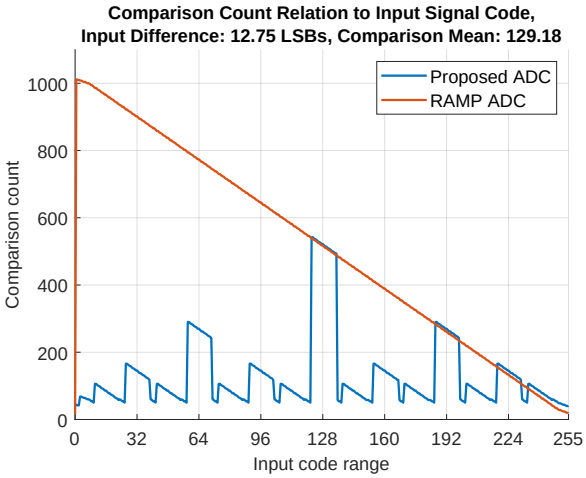
The 8-bit system simulations were also performed and the corresponding plots for different ΔV_{in} can be seen in figure 21 below.



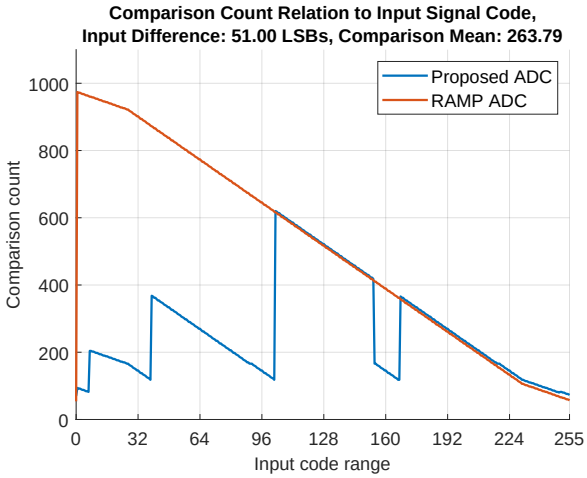
(a) Input Difference: 3.19 LSB.



(b) Input Difference: 6.38 LSB.



(c) Input Difference: 12.75 LSB.



(d) Input Difference: 51.00 LSB.

Figure 21: Comparison count needed to decode the output vs different input signal differences for 8 bit system.

4.2 Analysis: system performance vs input signal

4.2.1 Signal difference analysis

It can be seen that as expected, the average number count of comparisons rises as the difference between the input signals grows. From Figures 21a, 21b, 21c, 21d, the peaks in the comparison count plot grow wider with each increase in the input difference and their indicated comparison means also increase. Simulations were performed for multiple different inputs and the relation between average comparison count vs the input difference can be see in Figure 22 below.

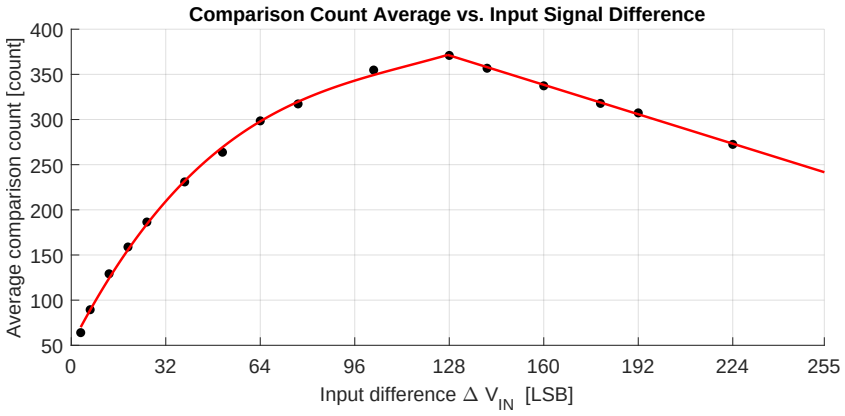


Figure 22: Comparison count average vs. Input signal difference for 8 bit system.

From Figure 22 it can be seen that there are two trends happening. The left half (0 to 128 LSB ΔV_{IN}) follows a logarithmic shape, and the right half (128 to 255 LSB ΔV_{IN}) a linear one.

The linear trend on the right half is explained by the count being distorted due to the factor that one end of the input extremes makes the ADC switch to the RAMP mode on the first MSB comparison. This should keep the average comparison count flat, however there is a downwards slope. This slope is due to the the fact that for most of the mean input range half of the inputs are clipped into one of the rails thus effectively reducing the total comparison count. As the signal difference ΔV_{IN} grows, the likelihood of clipping increases thus the downwards linear trend. This can be seen from the change of the trend at the middle code (128 LSB). This effect of signal clipping can also be clearly seen as a change of comparison count in the individual plots where the proposed ADCs count starts to look closer to the RAMP ADC count. This trend can be seen in Figure 21d where the middle and the input extremes start to have a wide slope.

The half that is of interest here is on the left side which follows a logarithmic curve. This trend properly shows the effect of the growing input signal difference between channel and the expected comparison count. In this half, as ΔV_{in} increases, the likelihood of the ramp engaging at bits closer to the MSB increases. At smaller input difference ΔV_{in}, a rough estimate can be done: when ΔV_{in} doubles, the comparison count increases by a factor ≈ 1.4.

4.2.2 Signal mean performance analysis

As it was shown in the previous subsection, the comparison count depends heavily on the input signal difference. However there is another important factor that contributes to a lower count: it is where should the input signal mean be in the input range. From the four plots in Figure 21 one can deduct that the input signal mean should be aimed for the gaps between the pillars. This can be simplified as to avoid being close to MSB, MSB-1, MSB-2, etc. in that order as to avoid serving a big penalty in comparison count. Of course the input signal differences do not stay constant throughout the whole recording and fluctuate a bit.

To analyse the effect of mean on comparison count, all of the afore mentioned Figures and more and additional simulations were used to compute the average overall comparison count. The result is presented in Figure 23. It shows the average of all the data points for ΔV_{in}

between 3.2 to 64 LSB. From the plot it can be deduced that the best placement of the DC mean would be in one of the valleys. As it is seen here, for neuro signals it should be placed around the 166th LSB code. This point is most optimal because it is one of the local minimas and also has quite a large acceptable variation of the mean. The walley around 80 LSBs input is also a good option but it it more sensitive to variations of the mean as the valley is more narrow.

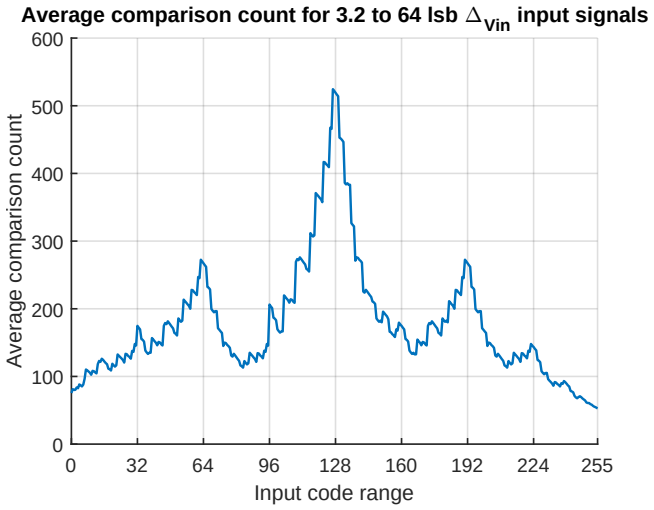


Figure 23: Comparison count average vs. Input signal mean for ΔV_{in} 0.05 to 1V inputs for 8 bit system.

4.2.3 System level considerations and recommendations

The system initially was aimed to be designed to be a 12 bit system. This was done such to overdesign of the effective number of bits as there would have been some ENOB degradation due to noise and other sources of errors and effectively would have dropped the ENOB down to 10 to 11 bits which is a typical ADC ENOB value for neuro recording systems. However, due to simulator limitations the final presented system consists of 8 bits as it does not require an as demanding simulation time and still provides a good bit resolution to properly demonstrate the advantages and limitations of the system. The system should be easily implementable as a 10 or 12 bit system.

4.3 Comparison count benchmark simulation

The comparison count of the proposed system and a ramp ADC were simulated using generated MEArec signals. The signals selected for the four channels were those of four neighbouring channels, being channels 5, 15, 16 and 27 that can be seen in Figure 7. These four were chosen because of their rather high cross correlation. The simulated data represents 1 second of the neuro-recording that was sampled at a frequency of 32kHz thus meaning 32000 samples.

For the ramp ADC comparison count a four channel 8 bit RAMP ADC was implemented in Simulink. The ramp ADC re-uses the already existing architecture but never goes through a binary search sequence. It consists of a ramp that starts from the highest value of the input range and ramps down. This was done as to keep a relatively advantageous playing field for the RAMP ADC compared to the proposed system because the neurosignals occur mostly in the top third of the input range. The number of comparisons for each channel was counted until

the correct code level is reached. After the level has been reached for a channel, the remaining levels for that specific channel are not added to the total any more even if the ramp counter continues on working.

What concerns the SAR ADC, the simulation was not performed as the number of comparison performed are not related to the signal that the ADC is trying to decode and always follow the same number of comparisons for any input. The number of comparisons per channel signal follows directly from the number of how many bits the ADC has at its output.

The total number of comparisons to be performed for m channels, c cycles and n bit SAR is described in equation 5 below. For a system of 4 channels of a 8 bit SAR and 32000 samples the total number of comparisons performed is:

$$\begin{aligned} \text{Total SAR comp} &= \mathrm{N_{bits}} \cdot \mathrm{n_{ch}} \cdot \mathrm{N_{samples}} \\ &= 8 \cdot 4 \cdot 32000 \\ &= 1.024.000 \text{ [cycles]}. \end{aligned} \tag{5}$$

4.4 Comparison count benchmark simulation: results

The results of the comparisons amount simulation is shown in Table 5 below.

Table 5: Comparison count per architecture.

Probe pitch	SAR	RAMP	Proposed system	vs SAR (%)	vs RAMP (%)
50u	1.024.000	10.166.535	6.377.150	+522.77%	-37.27%
25u	1.024.000	11.005.864	4.055.119	+296.01%	-63.15%
10u	1.024.000	11.243.329	4.188.668	+309.05%	-62.75%

The proposed system performs as expected in terms of comparison count at the system level implementation. It shows increased performance in terms of comparisons with a reduction of around 63% compared to the conventional RAMP. The first entry in the table has only 37.27% improvement but that may be ignored as the signals for that case were recorded on a much wider pitch electrode array. The final system implementation aims on having a pitch below 25μm. Compared to the SAR ADC, the comparison count increases by around 300%.

4.5 Area and power consumption comparison

There exists a breaking point between the proposed ADC and a time division multiplexed (TDM) SAR implementation in terms of power and area consumption.

Looking in terms of settling speed between the proposed and a multiplexed SAR implementation which corresponds to power consumption. The proposed ADC 8 bit system would require to accommodate 257 comparisons to be performed during a single sample regardless of the amount of channels. On the other hand the SAR ADC for a 8 bit system with the similar settling speed, it would be possible to multiplex 256/8=32 channels. This means that for the proposed system to start being beneficial in terms of power one should connect a cluster of 32 neighbouring channels onto the single ADC. This is achievable however, this comes with a large penalty in the number of comparisons and DAC switching because the comparison count

increases. Beyond 32 channel multiplexing the SAR settling speed would be higher than that of the proposed system, however it is to be noted that the proposed system comparison count could still be 300% higher.

The main advantage of the proposed system over a TDM SAR ADC implementation is that that for an increased number of channels to be decoded the ADCs speed does not need to be changed as it only depends on factors such as: (i) the sampling frequency and (ii) bit depth. Whereas a multiplexed SAR ADC scales with: (i) sampling frequency, (ii) bit depth, and (iii) number of channels being multiplexed. Increasing the number of channels multiplexed results and an increase of speed requirement which corresponds to an increase in power consumption.

From the area perspective, the single SAR that is being multiplexed has a similar area to that of the proposed system. For the same specifications both ADCs would have a comparable DAC area. The main difference would be in the extra circuitry needed for the analog multiplexing for the TDM SAR, and for the proposed system the digital overhead for the search logic and the increased number of comparators required.

However, compared to the generic RAMP ADC, the proposed system does take a penalty in area as it needs one dac per cluster of channels but it does make up for it in a reduction of comparison and DAC switching power with the possibility to save up to 60% of power.

5 Circuit implementation

In this chapter, the system is implemented in Cadence. It begins with a discussion of noise allocation, followed by the timing scheme, and concludes with the design of key building blocks, including the CDAC, sampling network, single-ended-to-differential switching scheme, and the comparator.

5.1 Noise allocation

From circuit design as a general rule of thumb the input referred noise is kept $\frac{1}{10}$ of the the smallest recordable signal. In higher density recording neural interfaces the recorded signals typically range between a few μV to mV: LFP fall into 1$\sim$3 mV and APs 100$\sim$300 μV [37]. Some sources do report however smaller amplitudes for LFP and AP signals ranging between 10μV$\sim$1mV. However generally in denser recording arrays the smaller AP signals that can be detected are from further away neuronal APs and are generally not of interest. From the ADC analysis in chapter 1.2, it can be seen that the input referred noise usually falls in the range of 3 to 10 $\mu V_{n,in,RMS}$ which aligns closer to the first range discussed. For this design the input reffered noise is chosen to be $\mu V_{n,in,RMS} = 4\mu V$.

The total input referred noise can be described as:

$$V^2_{n,in,rms} = V^2_{n,AFE,rms} \cdot BW + \frac{V^2_{n,rms,ADC}}{A^2_{AFE}} \quad [V^2], \tag{6}$$

where $V^2_{n,AFE,rms}$ is the noise generated by the analog front end which consist of the amplifier and other possible circuitry, BW is the systems bandwidth, $V^2_{n,rms,ADC}$ the noise generated by the ADC components such as the sampling circuit, DAC, and comparator, and finally the amplifier stage gain A^2_{AFE}

In neural ADC systems usually the total input referred noise is dominated by the analog front end that is not explored in this thesis. Because of this, generally the noise is allocated 70% to the AFE and 30% for the ADC. This leaves $V^2_{n,AFE,rms} = 2.8\mu V$ and for the ADC part $1.2\mu V$. Here the input range of the ADC was designed to be 0 to 1.1V. Taking into account the recorded signal and input amplitudes it can be found that for the worst case scenario gain occurs for the largest input of 3mV thus giving: $A^2_{AFE} = \frac{1.1}{3mV} = 366.7[V/V]$. $A^2_{AFE} = 355[V/V] = 51dB$ was chosen for the amplifier as to tighten the noise constraint used by the ADC section. This thus determines the total noise allowed at the input of the ADC to be: $V^2_{n,rms,ADC} = 426\mu V$.

5.2 Timing scheme

Because the ADC operates at both SAR and RAMP mode, the worst case condition being $T_{sample} + T_{SAR} + T_{RAMP} + t_{idle}$ must fit within a single samples time period. The sampling frequency is fs=25kHz thus a single sample takes in total $Total_{time} = 40\mu s$. The worst case of comparisons is $2^N + 1$ which for the 8 bit system equates to being 256+1=257 comparison steps performed during a single conversion cycle. Usually in RAMP ADCs the total time allocated for the sampling and conversion time is 1% and 99% respectively. This relaxes the time constraints needed for comparator and DAC to settle and still allows enough time for the sampling circuit to settle at the required precision.

Each step of the total 257 conversion steps is composed of two phases. The first half is used for logic propagation and DAC switching with settling. The second phase is used for the comparison to settle to resolve the input. These halves use their own separate clocks that are derived from a single master clock. The clock used for the sampling phase is also to be derived from one of these clocks. This allows for a simpler clocking scheme and clock partitioning. For the following explanation time value x is used to express the time taken by a single comparison or CDAC to settle that was previously mentioned. This value is used to determine the best possible clock frequency to be used such to From this the total time relation can be expressed as:

$$\begin{aligned} \mathrm{Total_{time}} &= \mathrm{T_{sample}} + \mathrm{T_{conversion}} + \mathrm{T_{idle}} \\ &= \mathrm{N_{sample\ cycles}} \cdot \mathrm{X} + 257 \cdot 2 \cdot \mathrm{X} + \mathrm{T_{idle}} \end{aligned} \tag{7}$$

The equation can be rewritten in terms of idle time and plotted to see the the variation of idle time vs X. The result is seen in figure 24. Here the y-axis shows the time allowed for both the idle and sampling period.

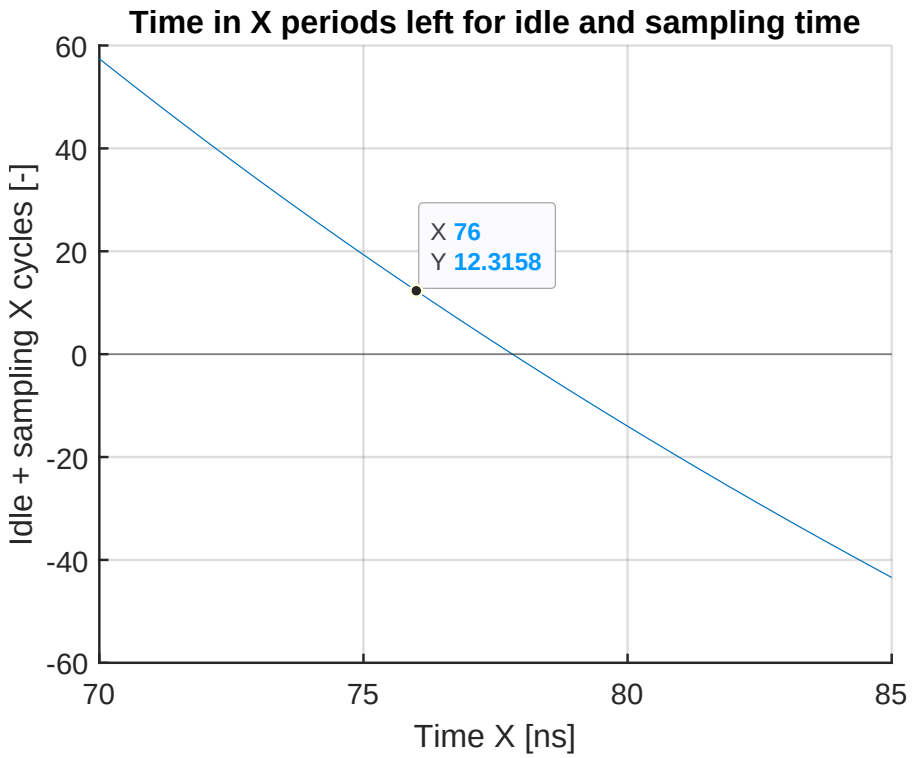


Figure 24: Time in X periods left for idle and sampling time.

The allocated percentage time can be used to find the required number of X cycles needed for the sampling period.

$$\mathrm{Sampling_{percentage}} = \frac{\mathrm{Cycles_{sample}} \cdot \mathrm{X}}{257 \cdot 2 \cdot \mathrm{X} + \mathrm{Cycles_{sample}} \cdot \mathrm{X}} \cdot 100 = 1\% \tag{8}$$

which can be rewritten to:

$$\mathrm{Cycles_{sample}} = \frac{257 \cdot 2}{99} = 5.192\ [\mathrm{X\ periods}]. \tag{9}$$

6 X time periods equating to 456ns were chosen for the sampling period. From Figure 24 X=76ns was chosen as this allows for a short idle time of 6.3158 X periods equating to approximately 480 ns before the next conversion cycle starts.

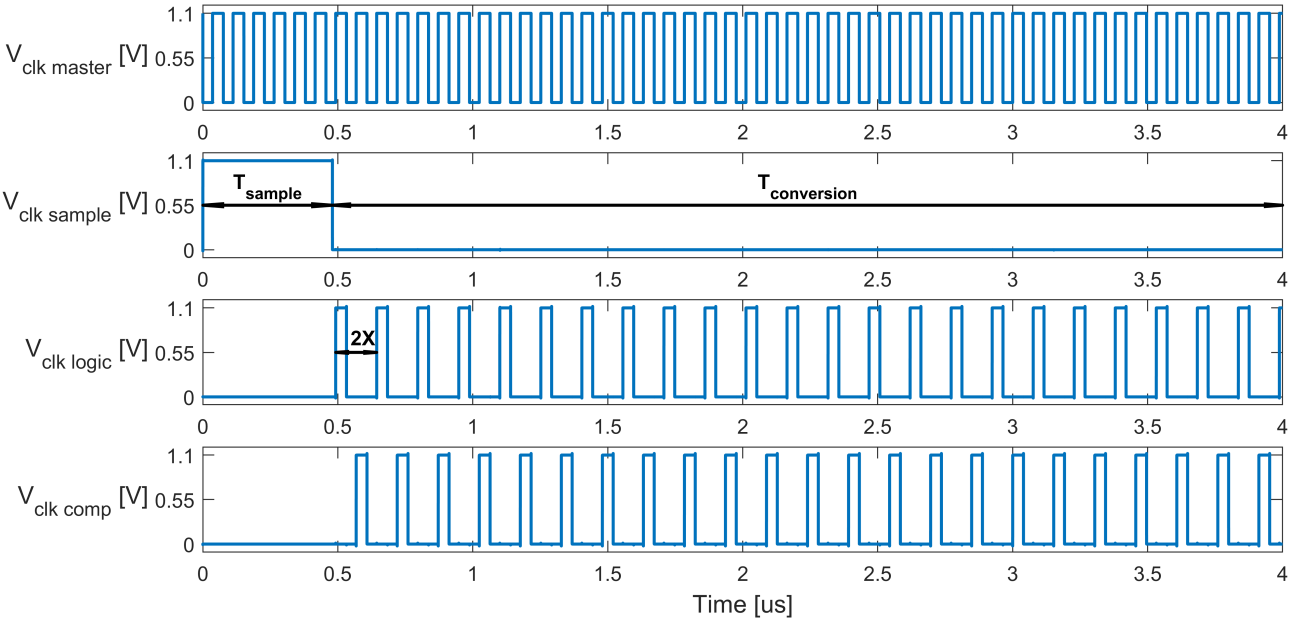


Figure 25: Master clock, sampling clock and generated clocks used for timing logic and comparisons.

In Figure 25, the first 4μs of a single sample conversion is shown. The total $T_{conversion}$ extends to 40μs. There are two clocks that are generated from the master clock: clk_{logic} and clk_{comp}. It can be noticed that there is a idle time between the two clocks of X/2=38ns. This is not an issue for the logic clock which is used to read the previous states logic output and update the next DAC output voltage as the time X is fully used. However, the comparison clock $clk_{compare}$ is actually not optimized as only time X/2 is used by the comparator to resolve the input. Nonetheless this is not an issue for this implementation as the settling time of the comparator as it will be seen in the comparator section 5.4 this is enough to settle.

5.3 DAC

A CDAC was chosen because of its simplicity and power efficiency. A differential CDAC was made that only makes use of VSS and VDD as switching nodes. This was chosen such to not require an extra biasing voltage source and having in mind that the previous stage has a near rail to rail output. The CDACs achievable output voltage range spans from -1.1V to 1.0914V. One could notice from this range that the middle code voltage is not exactly Vdd/2 but this is of no concern as it does not affect the functioning of the system. Of course it is possible that one would implement the previous stage with an output swing smaller than what the DAC can accommodate, this would reduce the ADCs performance by:

$$\text{bits}_{\text{lost}} = \log_2\left(\frac{V_{\text{pp,full}}}{V_{\text{pp,used}}}\right) \quad [\text{bit}], \qquad V_{\text{pp,full}} = |\text{V}_{\text{max}}| + |\text{V}_{\text{min}}|, \tag{10}$$

where $|V_{\text{max}}|$ and $|V_{\text{min}}|$ are the input maxima and minima, and $V_{\text{pp,full}}$ with $V_{\text{pp,used}}$ are the full-scale range input available and the input range used respectively. For example a -0.9V to 0.9V input range would reduce the ADCs performance by:

$$\text{bits}_{\text{lost}} = \log_2\left(\frac{1.1 + 1.09140625}{1.8}\right) = 0.2839 \quad [\text{bit}]. \tag{11}$$

The output voltage of the DAC determines the systems lsb to be:

$$\text{LSB} = \frac{V_{\text{pp,full}}}{2^8 - 1} = \frac{1.1 + 1.09140625}{255}\ [\text{V}] = 8.5938\ [\text{mV}]. \tag{12}$$

A binary weighted CDAC was implemented with 5.75fF unit cap. The total capacitance of the DAC equates to 1.5392pF.

5.4 Comparator

A strong-arm latch comparator was chosen due to its simplicity, good speed and relatively good offset performance. The used comparator consist of a single transistor input pair. This is done as to reduce the offset of the comparator more easily. Most common implementations that have a differential input use two input pairs, one used for the input signal and the other for the differential DAC voltage.

The proposed system consists of four comparators running in parallel. The matching of these comparators is crucial for a proper functioning of the overall ADC performance. This is due to the factor that the search algorithm is dependant on the difference of the input signals as discussed in Chapter 3.

5.4.1 Offset

Offset is a circuit non ideality that occurs due to mismatch of devices making the circuit not perfectly symmetric. It is usually treated as a small input voltage difference seen at the input of the comparator input pair. Typically it can range anywhere between 1 to 20mV depending on the sizing of the circuit input pair. This error can give an incorrect output for a small input difference. The offset is mostly dominated by the input pairs mismatch [47]. It is described as the variance of the threshold voltage V_T among adjacent transistors. The variance reduces inversely with the gate area (W and L) and seen in the equation below:

$$\sigma^2_{V_T} = \frac{A^2_{V_T}}{2 \cdot W \cdot L}, \tag{13}$$

where A_{V_T} is the process dependant constant.

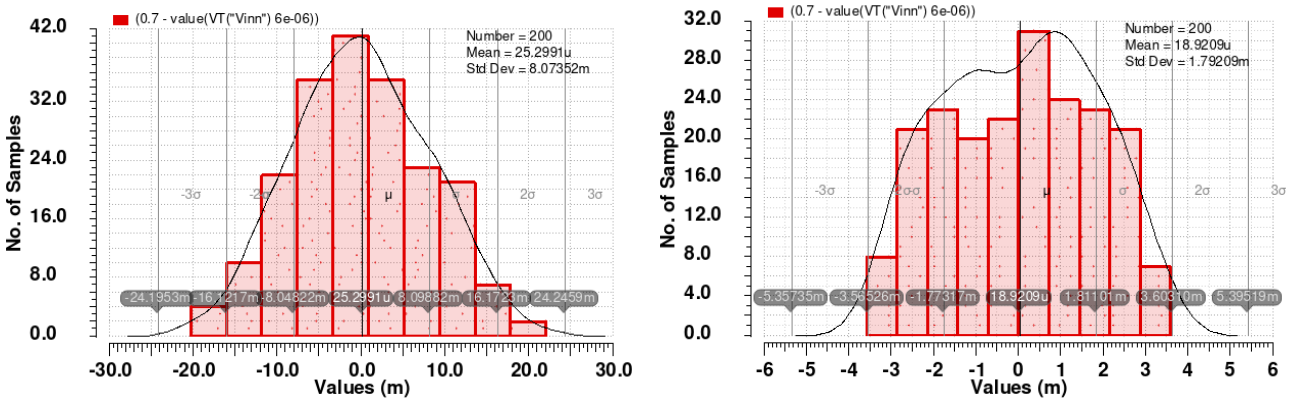
The designed lsb is 8.6mV and for already large input pairs the comparator does not satisfy the maximum offset requirement allowed of 0.25 lsb = 2.15mV. It would be possible to increase the input pairs sizing but because offset reduces with the square root of the area it would make the input pair enormous. Additionally a large input pair would increase comparator kickback. The 0.25 lsb requirement comes from the fact to allow enough matching between the comparators that are running in parallel.

Various offset correction/calibration techniques exist. The main ones include:

- Capacitive bank array

- Bulk voltage control
- Transconductance controller array
- Second input differential pair control
- Auto-zeroing
- Chopping
- Digital back end correction

A bulk controlled voltage offset correction was implemented with VerilogA that searches during the ADCs idle time for the offset, and differentially applies a DC voltage in steps of 10mV around the common mode voltage V_{CM} (Vdd/2) to the bulk of the input pair transistor. It was found that a DAC 3 bit DAC of 10mV step size is enough to satisfy the $\sigma_{\text{Voffset}} \leq 2.15\text{mV}$ condition. A 200 point Monte Carlo simulation was performed resulting in the probability distribution change seen in Figure 26.



(a) Offset variation Monte Carlo simulation without calibration.

(b) Offset variation Monte Carlo simulation with calibration.

Figure 26: Offset variation Monte Carlo calibration results.

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The differential bulk voltage change of ±10mV corresponds to roughly 7mV offset change. This is seen by the fact that the $|V_{\text{Max}}| + |\text{VMin}|$ of the offset folds back down to the 7mV range centred around the offset mean. The results of the offset calibration can be seen in Table 6.

Table 6: Monte Carlo offset result for before and after calibration.

	V_{min}	V_{max}	σ_{offset}
Without calibration	-20.3 mV	22.13 mV	8.074 mV
With calibration	-3.58 mV	3.604 mV	1.792 mV

The input pair sizing was chosen not to be too small as to hit the required offset spec and not require an increased bit for the calibration DAC. The sizing used of the input pair is W=120.0nM, L=40nM with a number of N=40 fingers. The regeneration latch also was increased to slightly reduce the mismatch and reduce offset with a finger number of $W_{\text{latch}} = 20$.

5.5 Sample & hold circuit

Because the system cannot employ the CDAC capacitor bank as a sampling circuit capacitance separate sampling capacitors are used for each channels. The proposed sampling circuit is combined with a switching scheme that allows to perform some power saving and increase the input signal by a factor 2x by making it differential.

5.6 Single ended to differential stage

The proposed system was implemented in TSMC 40nm which operates with a rail supply of 1.1V. This voltage level is a limiting factor in terms of available headroom available as this greatly reduces the lsb of the system and tightens the constraints on comparator offset and allowed noise during sampling. Therefore, a differential ADC is beneficial as it would effectively double the signal swing by a factor 2x relaxing the afore mentioned constraints. For this a single ended to differential stage must be used. The proposed system explores a switched capacitor scheme to achieve single ended to differential output. This comprises of sampling the input signal into two sampling capacitors and inverting one of the capacitors connection terminal and connecting each one to the differential DAC output such to get a differential output signal.

5.6.1 Switching network

The circuit network is illustrated in Figure 27. The circuit consists of two sides of the differential circuit. One side consists of three transistor switches. Firstly $M_{1a,b}$ consist of bootstrapped gate switch as to increase the maximal allowable sampling input at the higher end of the rail and reduce any possible distortion due to input signal dependency. The second switch $M_{2a,b}$ consists of providing a sampling reference for the input signal V_{in}. Thirdly the $M_{3a,b}$ switch which connects the DAC output voltage to either the positive or negative terminal of the capacitor such to create a differential output across nodes V_{DAC+} and V_{DAC-}.

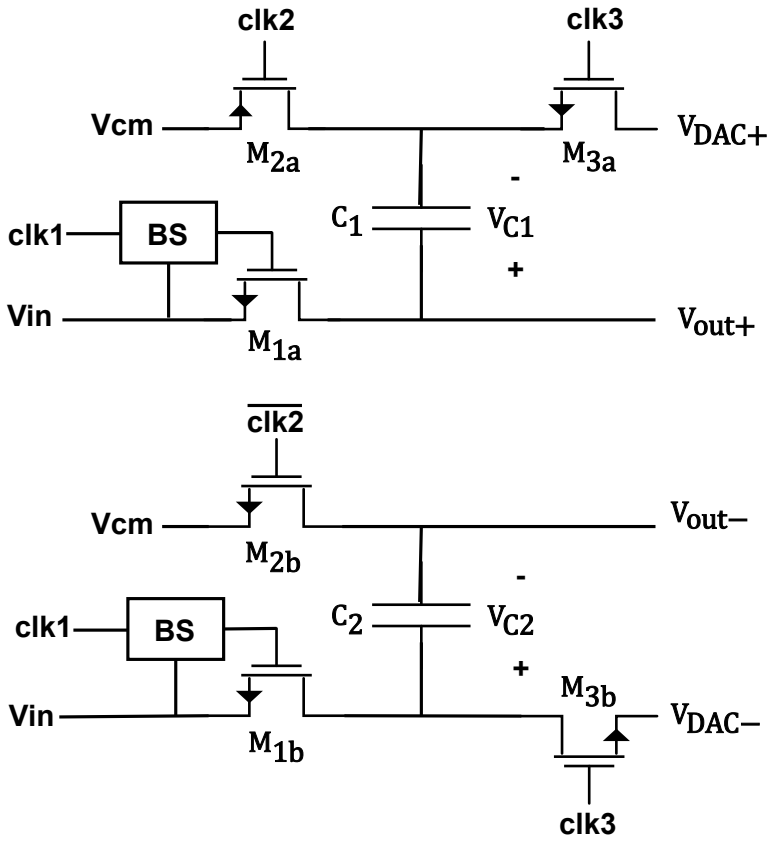

Figure 27: Sampling and single ended to differential switching network.

5.6.2 Switching network timing

The switching network is controlled by three clocks. These timing sequence of these clocks is shown in Figure 28 below. During the first phase when clk1 is high and clk2 is low consists of the tracking phase. The capacitors C_1 and C_2 are connected to V_{in} and V_{cm} the

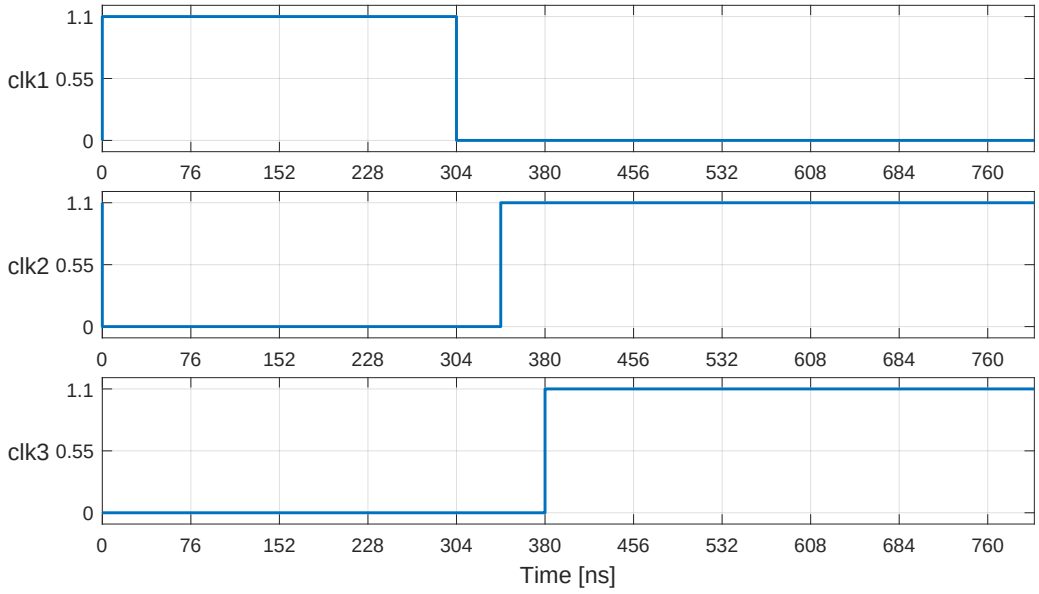

Figure 28: Sampling and single ended to differential clock switching scheme.

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5.6.3 Sampling noise

The effective differential noise of the circuit follows the same noise as any sampling capacitor and is described as:

$$V^2_{n,sample,rms} = \frac{2kT}{C_{sample}} \quad [V^2] \tag{14}$$

Where k is Boltzmann's constant, T the temperature in Kelvin and C_{sample} the sampling capacitance which in this case is: $C_{sample} = C_1 = C_2$. To allow a negligible SNR degradation penalty $V^2_{n,sample,rms}$ is designed to be less or equals the quantization noise $V_{q,rms}$ of the ADC which simplifies to:

$$\begin{aligned} V_{n,sample,rms} &\leq \frac{1}{2} V_{q,rms} \\ \sqrt{\frac{2kT}{C_{sample}}} &\leq \frac{LSB}{2\sqrt{12}} = \frac{V_{FS}}{2 \cdot 2^N \sqrt{12}} \\ C_{sample} &\geq \frac{96\,kT\,2^{2N}}{V^2_{FS}} \quad [F]. \end{aligned} \tag{15}$$

For the brain temperature of 38°C, 8 bits and $V_{FS} = 1.0914V$ gives $C_{sample} = 22.7fF$ which is overshot due to needed much larger capacitor values as to reduce unwanted change injection during the switching phase.

5.6.4 Charge injection

There is charge injection that occurs predominantly because of transistor M_1. The parasitic gate capacitance injects unwanted charge when turning off thus resulting in a changed V_{in} voltage. For this reason a bootstrapped transistor was placed at the input node of the capacitor such to make the charge injected a constant. To reduce the error the sampling capacitor was increased until the effective sampling error was reduced to be within ±0.25lsb error. The resulting plot can be seen in Figure 29. The resulting error is kept within the ±0.25lsb range for a sampling capacitance of $C_{sample} = 240.26fF$.

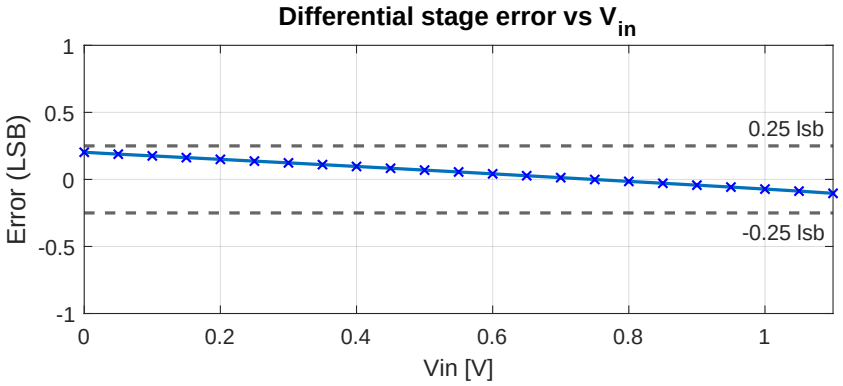

Figure 29: Error added due to charge injection vs V_{in}.

The sampling capacitor proposed is much smaller than the total capacitor array value in a typical SAR which tends to have something closer to 1.5pF or more. The proposed scheme results in needing a less power hungry drive stage to drive it which translates to power saving.

6 Conclusion and discussion

6.1 Conclusion

This work investigated the feasibility and performance of a novel simultaneous multi channel input hybrid SAR–RAMP analog to digital converter (ADC) intended for high density neural recording probes. The study combined neural signal analysis, system-level modelling in Simulink, and critical block-level circuit design.

Firstly, MEArec generated neural signals were used to quantify correlations across varying probe pitches from 10μm to 50μm. As electrode pitch decreased, cross-correlation and information redundancy increased, indicating that neighbouring channels often carry partially overlapping signal content but it is not enough to reduce the required bit resolution of the system as a change of electrode pitch from 25 to 10μm showed a reduction of only 0.413 bits. The generated data was used to perform an analysis on the max signal differences in a cluster of four neighbouring channels which lead to show that AP and LFP band signal differences ranged around 18 to 2.6 LSBs difference. The signal correlation and max channel signal difference observation motivated an ADC architecture that can exploit spatial signal proximity to reduce conversion overhead compared to a RAMP ADC.

A novel multi channel hybrid SAR–RAMP ADC was implemented and simulated in Simulink. Its operation begins with a coarse binary search. Once channel outputs diverge, the search algorithm transitions to a RAMP search. System level analysis revealed that the comparison count which relates to dynamic power depends strongly on the clusters channel signal difference ΔV_{in}, and on the clusters mean input voltage. For small ΔV_{in} values the average comparison count followed a logarithmic growth with an increase of 2x of ΔV_{in} translated into a 1.4x increase in comparison count. Properly positioning the multiple channels signal DC mean away from MSB SAR decision boundaries reduced the comparison count. The most optimal DC mean point for a 8 bit system was found to be the 166th LSB input as it offers the lowest comparison count without serving a comparator count penalty for small varying DC mean.

Benchmark simulations of a 8-bit ADC using the generated neural data showed that the proposed ADC offered up to 63% savings in dynamic power (Comparator+DAC) over a RAMP based ADC. Compared to a TDM SAR ADC, the proposed system was greatly outperformed in terms of power consumption, with an increase of 300% for smaller pitches electrode arrays such as 25μm and 10μm.

The proposed system can only break even with a TDM SAR ADC at a settling speed level at around the 32 channel count which is an unfeasible solution for the proposed ADC. The maximal input signal difference ΔV_{in} in a larger cluster of channels would increase as the recorded area would be larger. This in turn would increase the probability of RAMP mode operation to be switched on at a larger bit value thus degrading performance.

One main advantage of the proposed system over a TDM SAR ADC implementation exists that is: for an increased number of channels to be decoded the ADC's speed does not need to be changed as it only depends on factors such as: (i) the sampling frequency and (ii) bit depth. Whereas a multiplexed SAR ADC scales with: (i) sampling frequency, (ii) bit depth, and (iii) number of channels being multiplexed. Increasing the number of channels multiplexed results and an increase of speed requirement which corresponds to an increase in power consumption.

At circuit level the importance of the offset matching was discussed as a bad matching between different channel comparators directly affects the comparison count and thus the system performance. Offset reduction comes with the cost of an increase in power, area and complexity. The system was implemented with a bulk driven calibration scheme reducing the offset σ_{offset} from 8.074mV down to 1.792mV.

A single ended to differential scheme was proposed that samples the input signal and connects it on top of the DACs differential output. This reduced sampling capacitor which in turn offers some minor power saving as the sampling load is not as big as the total capacitor bank of the CDAC as is the case in SAR ADCs.

6.2 Future work & recommendations

- The behavioural application of the system was verified the but lacked the full exploration of the area analysis. A layout of the complete system would be required to demonstrate the actual area benefits of the proposed architecture.
- Because the RAMP ADC comparison speed is a limiting factor in terms of comparison count, look into the possibility of having a multi channel search with a SAR as is currently implemented but instead of switching to a RAMP, continue with a binary search for each channel individually. This could in effect outperform a multiplexed SAR with a increase in digital overhead.
- Explore the idea of having a multi technology and voltage node implementation. A smaller node and voltage would be beneficial for the digital implementation and a larger node and voltage such as 65nm or 180nm for the analog circuits part would relax noise and matching constraints.
- Adapt the ADC system implementation for other applications that are based on array like recordings such as image sensor applications.
- To reduce the total area of the DAC look into using a split DAC topology.
- The digital electronics was mostly implemented with standard cell digital blocks. The use of Electronic Design Automation (EDA) tools could be beneficial to refine the design.

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7 Appendix

Overview of common MEA ADC architecture

Source	Author	Year	ADC	channels	pitch	bits	ENOB	Tech node	Voltage	ADC Power	Area
https://doi.org/10.1016/j.bios.2018.10.032	SINAPS/Gian Nicola Angotzi	2019	NA	512	28µm	12	-	180nm	-	-	-
https://ieeexplore.ieee.org/document/8100720	Sung-Yun Park et al.	2017	Delta-Sigma	128	-	-	10.9	180nm	0.5/1.0V	3.05µW/ch	0.058mm2/ch
https://ieeexplore.ieee.org/document/9531935	Xiaohua Huang et al.	2022	Delta-Sigma incremental	1	-	11	-	22nm	0.8V	-	0.0001mm2
https://ieeexplore.ieee.org/document/8497041	De Dirugo et al.	2018	Delta-Sigma incremental	64/144	70µm	11	8.2	180nm	1.8V	-	0.00049mm2/ch
https://ieeexplore.ieee.org/document/9834314	Wendler et al.	2023	Delta-Sigma incremental	8	55µm	11	-	180nm	1.8V	-	0.00462/ch mm2
https://ieeexplore.ieee.org/document/6055371	R. Shulyzki	2011	RAMP	256	200µm	8	-	350nm	3V	-	-
https://ieeexplore.ieee.org/document/10376186	MoonHyung Jang et al.	2023	RAMP	1024	36µm	8	-	28nm	1V	0.268µW/ch	0.001296mm2/ch
https://ieeexplore.ieee.org/document/6923484	M. Ballini et al.	2014	RAMP	1024	17.5µm	10	-	-	3.3V	13.68µW/ch	0.04mm2/ch
http://dx.doi.org/10.14257/ijbsbt.2015.7.1.08	Jimin Cheon	-	RAMP	16	-	8	7.7	350nm	3V	-	-
https://doi.org/10.3389/fnins.2019.00234	Jun ogi et al	2019	RAMP	432	24µm	12	-	140nm	-	-	-
https://doi.org/10.1116/1.4997358	Jun ogi et al	2017	RAMP	6912	24µm	12	-	140nm	-	-	-
https://arxiv.org/html/2505.04128v1	W.Lemaire et al	2025	RAMP event driven	49	-	8	-	25nm	1.2V	2.5µW/ch AFE	50x60um2/ch or 4300 total AFE and digital/ch
https://ieeexplore.ieee.org/document/9094199	J.P.Uehlin et al	2020	RAMP event driven	64	-	-	14	65nm	1.2/2.5V	3.21µW/ch	4mm2
https://ieeexplore.ieee.org/document/6718118	Dong Han et al.	2013	SAR mux	100	-	10	-	180nm	0.45V	1.35µW @200kS/s/10ch, or 1µW @140k/s	-
https://www.mdpi.com/1424-8220/17/10/2388	B.C.Raducanu	2017	SAR mux	678	22.5µm	10	-	130nm	1.2V	-	0.12mm2/ch
https://ieeexplore.ieee.org/document/6642150	C. M. Lopez et al.	2014	SAR mux	52	35µm	10	9.2	180nm	1.8V	-	0.19/ch mm2
https://ieeexplore.ieee.org/document/7900417	C. M. Lopez et al.	2017	SAR mux	384	20µm	10	-	130nm	1.2-1.8V	-	0.12mm2/ch
https://doi.org/10.1016/j.bios.2018.10.032	Neuropixels	-	SAR mux	-	-	10	-	130nm	-	-	-
https://doi.org/10.1016/j.bios.2018.10.032	Neuroseeker	-	SAR mux	-	-	10	-	130nm	-	-	-
https://ieeexplore.ieee.org/document/9385387	Xinyue Yuan et al. (MaxWell bio)	2017	SAR mux	19584	18µm	10	-	180nm	-	-	0..219mm2/ch (total 6×9mm2)
https://ieeexplore.ieee.org/document/8094930	Yan Liu et al.	2017	SAR mux	64	-	10	9.1	350nm	3.3	0.45µW/ch analog, 1.1µW digital	0.3 mm2/ch (total 19.3 mm2)
https://www.mdpi.com/2079-9292/10/21/2726	Xinagwei Zhang et al.	2021	SAR mux	64	-	10	-	180nm	1.8V	-	0.25mm2/ch
https://ieeexplore.ieee.org/document/6964818	R.Muller	2015	VCO	64	500µm	13	-	65nm	0.5V	2.3µW/ch	1.6mm2

Power	power/ch	FoM	noise	freq band	fs	Other features
-	< 6 µW/pixel	-	7.5uV (0.3–7.5 kHz)	-	25kHz	-
-	3.05µW/ch	ADC 35.2fJ/C-s, 108.83/ch	3.32µVrms	10.9kHz	25kHz	delta-delta-sigma shapes noise out
-	0.3µW/ch	-	11.3µVrms, 10µVrms(LFP, AP)	~0-10kHz	-	event driven input biasing
39.14, 43.32, and 46.29 µW	39.14, 43.32 and 46.29 µW/ch	17.58 fJ/C-s	6.02 µVrms (LFP), 39.14 µW(AP)	1Hz-10kHz	20MHz	modular, ADC under each electrode, 3 modes of amplification
8.57 µW (AFE), 6.05 µW (transmit)	14.62µW/ch	-	4.88, 4.46, 2.51 µVrms (FS/AP/LPF)	0-10kHz	2.72 MHz	-
13.5mW	52µW/ch	-	7.99µVrms	0.5Hz-10kHz	-	-
508.7µW	0.268µW/ch	-	7.4µVrms	300Hz-5kHz	20kHz	Box-car sampling, pulse-position modulation (PPM)-based 146x data reduction
75mW	45µW/ch	-	2.4µVrms AP, 5.4µVrms LFP	1Hz-6kHz	20kHz	32 stimulus units less than 2degrees C
-	12µW/ch	-	-	0.1Hz-10kHz	40kHz	-
-	-	-	4.75µVrms	-	48ksps	sampling freq is 8x higher than 6kHz required thus reducing folding noise
-	-	6.21[kch/(s\m2 \Vrms)]	23.2µVrms (full) 15.3µVrms(AP)	-	12kHz	interleaved 4 electrodes onto 1 channel
534µW (measured)	10.49µW/ch	-	10µV (0.5-6kHz)	0.5-9.2kHz	20kHz	compression done on spikes
0.62mW	3.21µW/ch	-	-	Tunable <32kHz	16kS/S	-
-	0.73µW/ch	22fJ/conv-step	3.2Vrms	10kHz	-	Has 2 modes for recording: low noise & low power
-	45µW/ch	-	50.2µVrms (LFP), 12.4µVrms (AP)	0.5/300/500/1000Hz to 300/500/1000/8000Hz	400kS/s (20ch)	Various recording bands
949.8µW & 1.45mW (core & total)	27.84µW/ch	219.7fJ/conv-step	5.8, 3.2uV (LFP,AP)	0.5Hz-6kHz	fADC = 120kHz fs= 30/15kHz	-
-	49.06µW/ch	108.4fJ/conv-step	6.36µV (0.3-10kHz)	0.5Hz-10kHz	fADC = 390kHz, fs= 30kHz	2 parallel PGA signal branches + mux+10bit SAR
-	-	-	5µV (0.3–10 kHz)	-	30kHz	-
-	63 µW/pixel & 45 µW/out ch.	-	31uV (0.3–7.5 kHz)	-	40kHz	-
5.9µW APS, 39.1µW SM	39.1µW/ch	-	10.9µV APS, 3.1uV SM	300 Hz-5 kHz	24.4kHz SM	APS (active pixel sensor) & SM (switch matrix) readout
7.36mW (stream), 6.60mW (snippet)	23µW/ch	-	2.12µVrms (AP), 1.16µVrms (LFP)	0.05H-10kHz	16kHz	configurabl 4 stage AFE with 4 modes of readout bands
-	130µW/ch	-	5.5 µVrms (1 Hz–10 kHz)	0.1-20Hz to 6-8kHz	20kHz	Programmable low and high pass corners
147.2µW	2.3µW/ch	-	1.2µVrms	1-500Hz	1kHz	ECoG and EEG based recordings, chopped differential amplification stage

Table 7: Electrophysiological neural-recording probes

Category	Example probes	Placement	Main signal class
Non-invasive surface	Scalp EEG caps	On scalp	Global field potentials (0.1–100 Hz)
Semi-invasive surface	Subdural ECoG grids/strips	On cortical surface (pia/dura)	Cortical field potentials (0.1–300 Hz)
Depth macro-electrodes	Stereo-EEG shafts, DBS leads	Deep nuclei /white matter	Depth LFPs, high-frequency oscillations (1–500 Hz)
Penetrating shank/array	Utah array, Neuropixels, NeuroNexus silicon shanks	Intracortical (pierce pia)	Unit spikes (300 Hz–5 kHz) and local LFPs (0.1–300 Hz)
Microwire bundles	Tetrodes, floating microwires	Intracortical	Unit spikes, multi-unit activity
Flexible polymer probes	Neuralink threads, NeuroNexus EdgeFlex	Intracortical (flexible)	Unit spikes, local LFPs

Time saving SAR based approach of comparator offset verilog code:

```
// VerilogA for Thesis_system, comparator_offset_search_differential, veriloga

`include "constants.vams"
`include "disciplines.vams"

module comparator_offset_search_differential(compOut, clk, Vout_p, Vout_n, ON, Vmin, Vmax);
    inout compOut, clk, ON, Vmin, Vmax;
    output Vout_p, Vout_n;

    electrical compOut, clk, Vout_p, Vout_n, ON, Vmin, Vmax;

    // Static bounds
    real Vinmin;
    real Vinmax;

    // Search stop threshold
    parameter real Vsearch = 1e-14;

    // Internal search variables
    real Vcommonmode, delta_v, step;

    analog begin
        // Initialize search range
        @(initial_step) begin
      Vinmin = V(Vmin);
      Vinmax = V(Vmax);
            Vcommonmode = (Vinmin + Vinmax) / 2;
            delta_v = 0;
            step = (Vinmax - Vinmin) / 4;
        end

        // Reset search on ON falling below threshold
        @(cross(V(ON) - 0.55, -1)) begin
      Vinmin = V(Vmin);
      Vinmax = V(Vmax);
```

```
            Vcommonmode = (Vinmin + Vinmax) / 2;
            delta_v = 0;
            step = (Vinmax - Vinmin) / 4;
        end

        // Update search based on comparator output
        @(cross(V(clk) - 0.55, -1)) begin
            if (V(ON) > 0.55) begin
                if (step > Vsearch) begin
                    if (V(compOut) > 0.55) begin
                        delta_v = delta_v - step;
                    end else begin
                        delta_v = delta_v + step;
                    end
                    step = step / 2;
                end
            end
        end

        // Drive symmetric differential output
        V(Vout_p) <+ transition(Vcommonmode + delta_v, 0, 1n);
        V(Vout_n) <+ transition(Vcommonmode - delta_v, 0, 1n);
    end
endmodule
```

VerilogA - Single ended to differentiala output ideal block

```
`include "constants.vams"
`include "disciplines.vams"

module sample_hold_verilogA_differential_out_inverted(comp_p, comp_n, Vdac_1
    , Vdac_2, in_p, in_n, clk, VSS, VDD);
    output comp_p;
    output comp_n;
    input Vdac_1;
    input Vdac_2;
    input in_p, in_n;
    input clk;
    input VSS, VDD;

      electrical comp_p, comp_n;
  electrical Vdac_1, Vdac_2;
      electrical in_p, in_n;//sampling input variables positive and negative
      electrical clk;
      electrical VSS, VDD;

    real sample;
  real Vcm;

    analog begin
        @(initial_step) begin
      sample = 0;
      Vcm = (V(VDD)-V(VSS))/2;
            $discontinuity(0);
        end

        // Sample on rising edge of clk (threshold 0.55V)
        @(cross(V(clk) - Vcm, +1)) begin
            sample = V(in_p, in_n);// in_p = positive sampling, in_n =
```

```
    negative sampling
32              $discontinuity(0);  // Ensures solver knows there's a jump
33          end
34
35          // Output the held value
36          V(comp_p) <+ V(Vdac_1) + sample;
37          V(comp_n) <+ V(Vdac_2) - sample;
38      end
39  endmodule
```

8 Schematic circuits

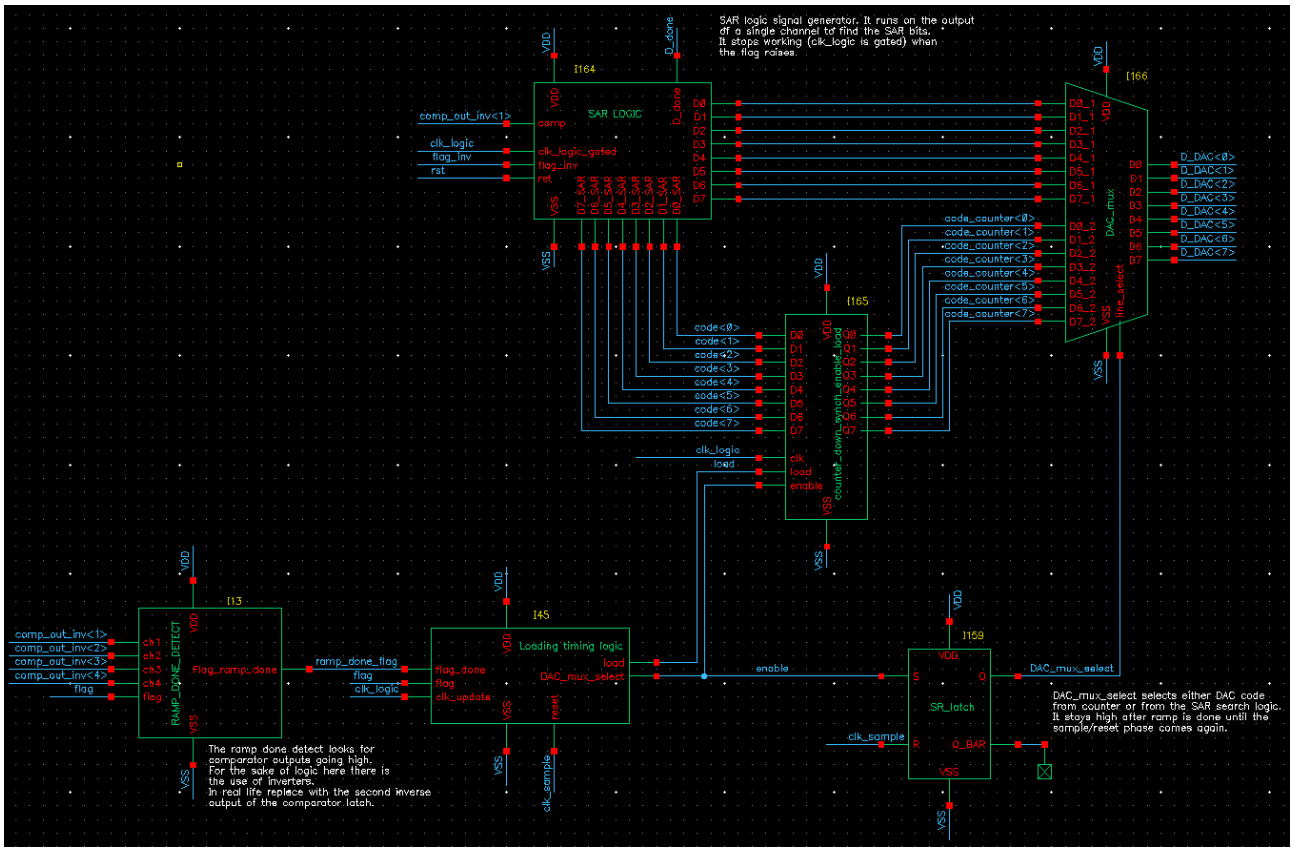

Figure 30: ADC Logic - SAR logic, counter, logic SAR/RAMP switch and bit output.

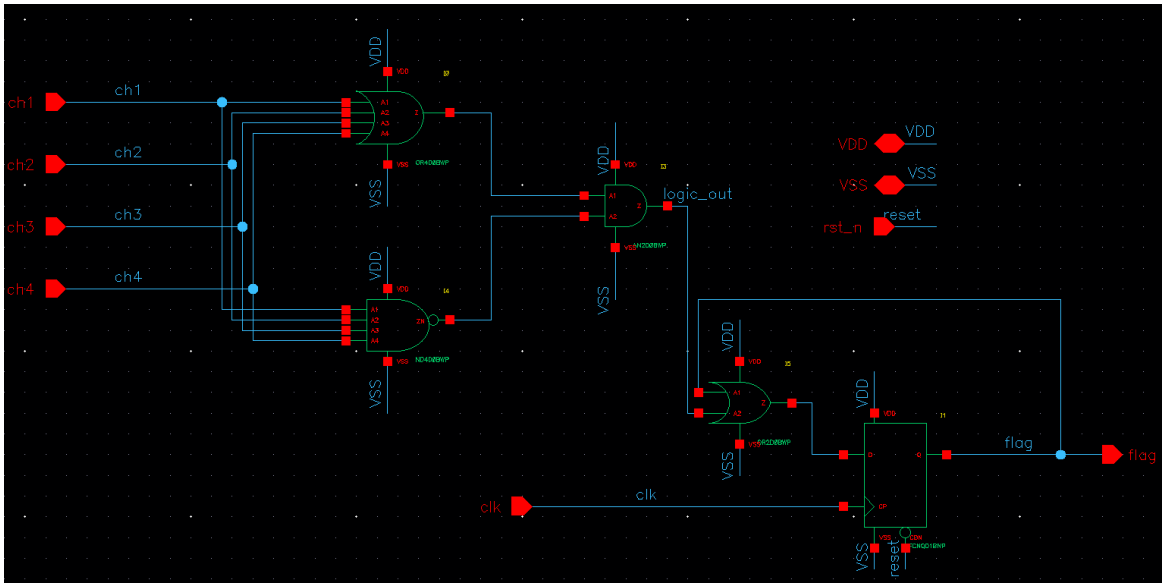

Figure 32: SAR to RAMP detect logic.

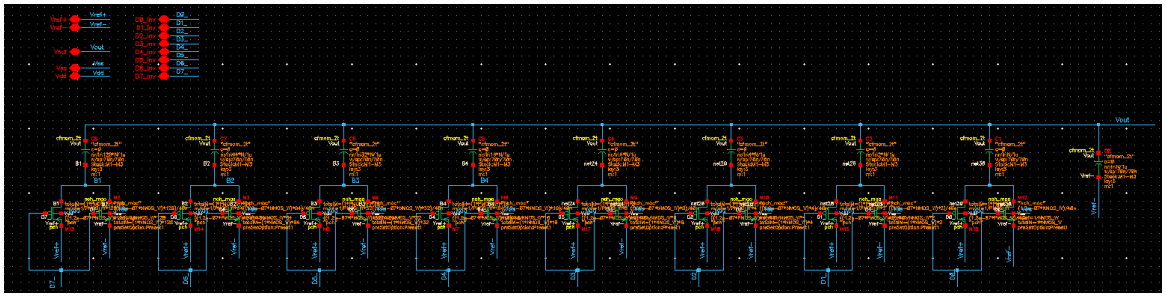

Figure 33: CDAC.

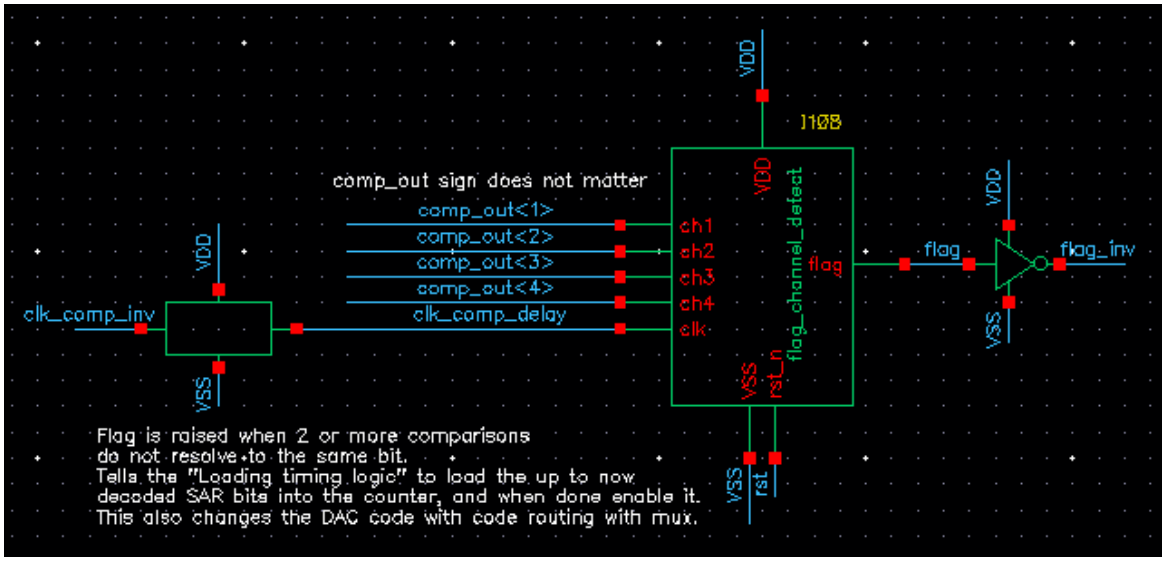

Figure 31: Logic detect for SAR to RAMP switch.

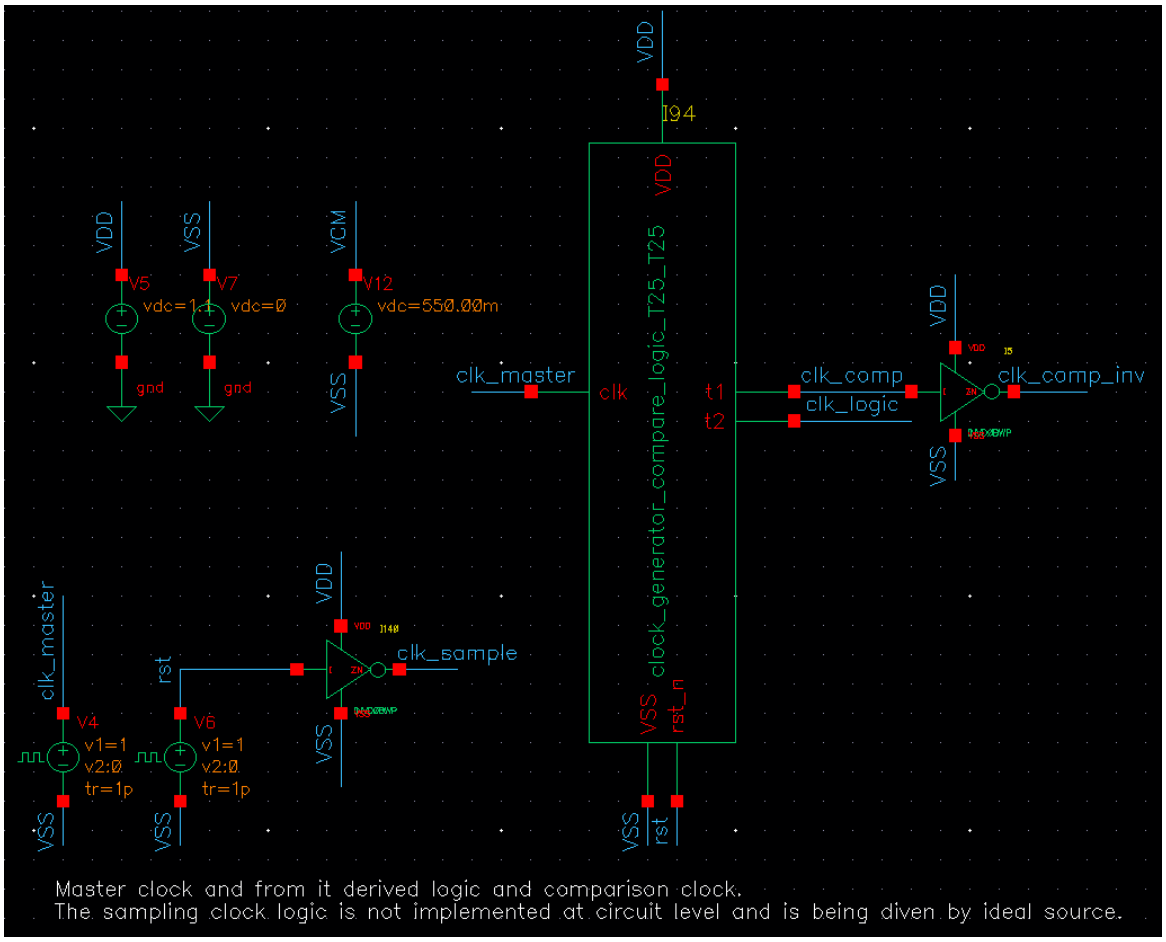

Figure 34: Used clock network.

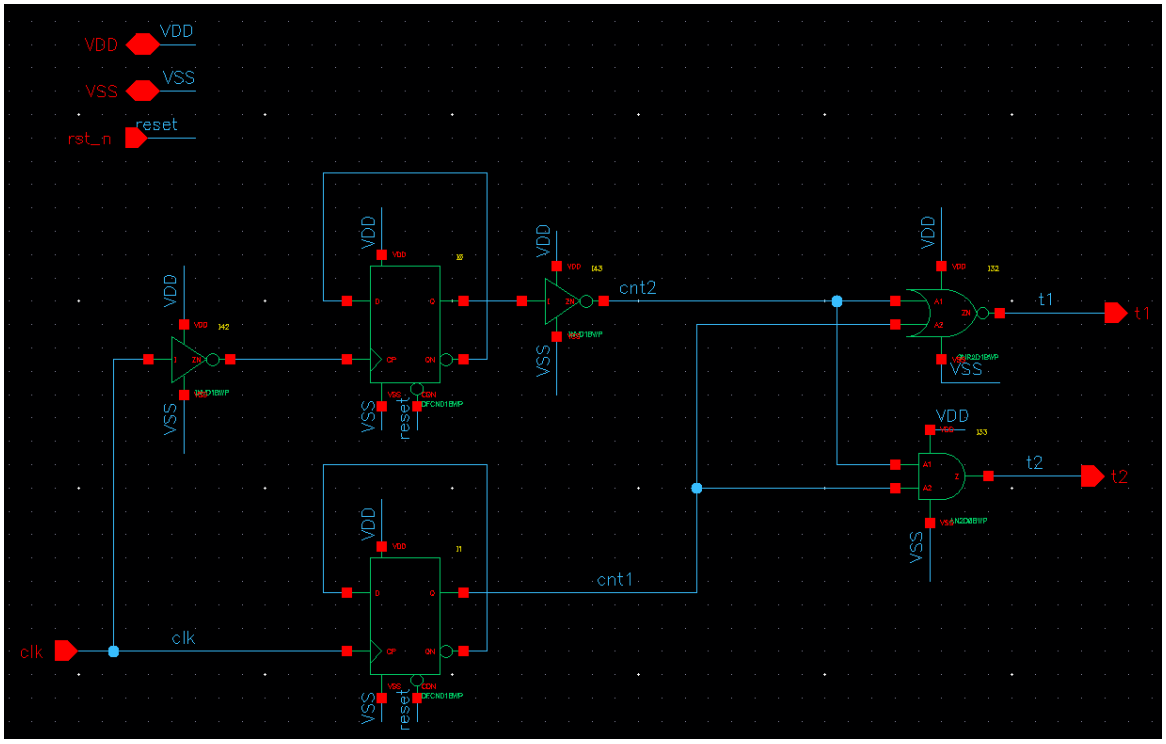

Figure 35: Clock generator.

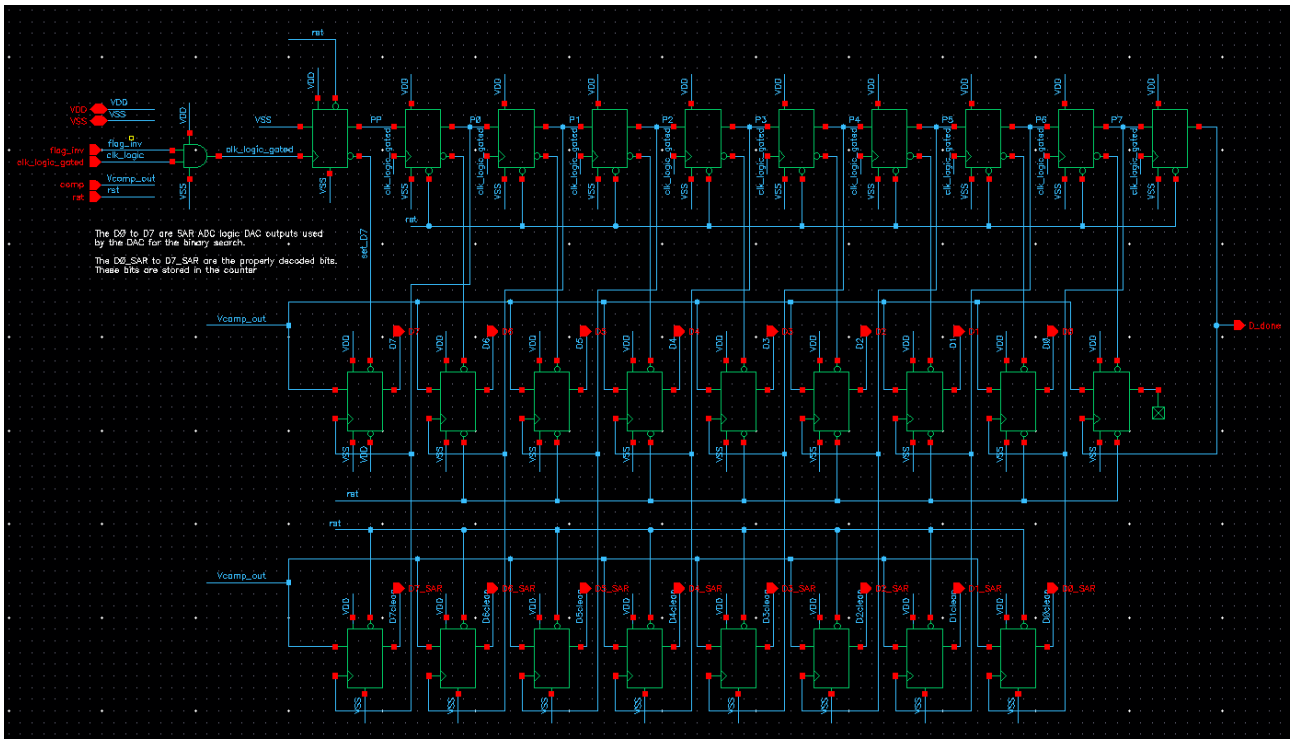

Figure 36: Synchronous SAR logic.