A wide range input and output driver for a Hydraulic Simulation System

Design report

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TU Delft

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by

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TU Delft

Summary

This thesis is written as part of the Bachelor Graduation Project of the Bachelor Electrical Engineering at the Delft University of Technology. Six students have the opportunity to design a hydraulics simulation system for HedoN Electronics Development B.V.
HedoN is a high-tech electronic development and production company and is a long-term partner of Huisman, HedoN creates a Hydraulic Motor Controller for Huisman their secondary hydraulic plants. The group of six students got the opportunity to create for this application a simulation system. This simulation system should be able to mimic these hydraulic plants such that the Hydraulic Motor Controller is able to work as in a normal setup with an actual crane.
This thesis focuses on the hardware design of the pin driver, the hardware unit that connects to the in- and outputs of the HMC. The main design principle for the pin driver is modularity. Every in- and output of the HMC should be able to be driven through the pin driver.

The Pin driver should be able to be act like a voltage amplifier, transconductance amplifier or route an external signal. The design is split up in three separate parts. At first an general system design is proposed and in- and outputs signals are defined to be able to control the different modes (Chapter 3). The first mode is the Pin Driver as a Voltage Amplifier (Chapter 4), where a control system and a hardware design is proposed to create an amplifier which is capable of delivering a voltage up to plus or minus 40 V with an precision of at least 10 mV. The stability under certain loads is tested and the amount of noise in the system is calculated to verify the desired precision.
This is followed by a design of the transconductance amplifier (Chapter 5), which needs to be able to create currents up to 4 A. As the HMC has a lot of current controlled inputs with different current levels and different precisions, a higher level of precision is desired over certain ranges. To suffice this need of precision, within the transconductance amplifier, different output current levels are defined with a different precision per level. A method for switching between these levels is proposed aswell as a method to overcome the common-mode voltage while measuring, which can be up to 40 V.
In Chapter 6 solutions are proposed to incorporate these systems, further reduce noise and a protocol which is able to make switching between the systems possible.
Simulations have been done on the system, to verify the working in each different mode and whether the requirements have been met. These are the results of the Pin Driver design and are located in Chapter 7. Also a test plan is created for the situation when an actual pin driver has been created.
The thesis ends with conclusions and recommendations upon the working of the Pin Driver. The Pin Driver functions properly and is able to drive a variety of loads. However, by implementing some of the recommendations the precision could be brought within margin. The transconductance amplifier does not meet the nice-to-have requirement, however does meet the must-have requirement. For the transconductance amplifier recommendations are given to possibly be able to meet the nice-to-have precision level.

T.J. de Smalen & R.V. Prins
Delft, June 2017

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1 Introduction

1.1. Background Information

HedoN is a high-tech electronic development and production company based in Delft. The company was founded in 1979 as a spin-off from Delft University of Technology. HedoN has been Huisman's technology partner since 1979 for hydraulic motor controls. Huisman constructs large hydraulic plants that are controlled by a Hydraulic Motor Controller (HMC), which is designed by HedoN. This HMC handles input and output signals to and from the plant such that it can be operated in a safe manner.

Hydraulic plants need to be commissioned by very specialised commissioning engineers. Huisman has a small team of those engineers, but is interested in expanding that team. The problem with training commissioning engineers however, is that training can only happen at sea, where the hydraulic plants are. A solution to this problem would be to simulate the behaviour of these hydraulic plants. With a simulation system, commissioning engineers could be trained on land which greatly reduces training costs and in turn enables Huisman to afford more specialised commissioning engineers. Furthermore, a simulation provides a safer environment for commissioning engineers in training to make mistakes.

Another application of the simulation system could be for the engineers designing the HMC at HedoN. Right now HMC05 has been developed, but software fine-tuning based on results from a simulation could still be very helpful to improve the HMC. For example, the latest HMC supports up to four motors, where four HMC's could be connected parallel and will be able to control up to 16 motors. There's not yet a real hydraulic plant with this many motors, therefore a simulation would be helpful to test such a system.

An important design consideration concerning the simulation system is that it has been designed with modularity in mind. This will enable HedoN to perfect its simulation system with Huisman and then potentially branch out to other industries. Automotive and aerospace industries for example could also benefit from such simulation systems.

1.2. Simulation System

In figure 1.1 a schematic overview of the simulation system is shown. On the right hand side of the figure the HMC05, developed by HedoN, is displayed. This hydraulic motor controller would normally be connected to a hydraulic plant in order to control it. That plant has now been replaced by the simulation system.

In order to mimic the behaviour of a hydraulic plant, various electrical components are required to generate an analog signal for the HMC, namely pin drivers, LVDT's, servo's and encoders. These components then communicate through Ethernet with a Hydraulic Simulation Unit (HSU). The HSU runs hydraulic simulation code that resembles the dynamic behaviour of the hydraulic plant. Also, there is another Ethernet connection to an external computer/web-server to give relevant information to the operators of this simulation system.

As per assignment for the bachelor graduation project, the group of six students had to be split up in three sub groups. Group 2 will design the communication between the HSU and the pin drivers [1], group 3 will

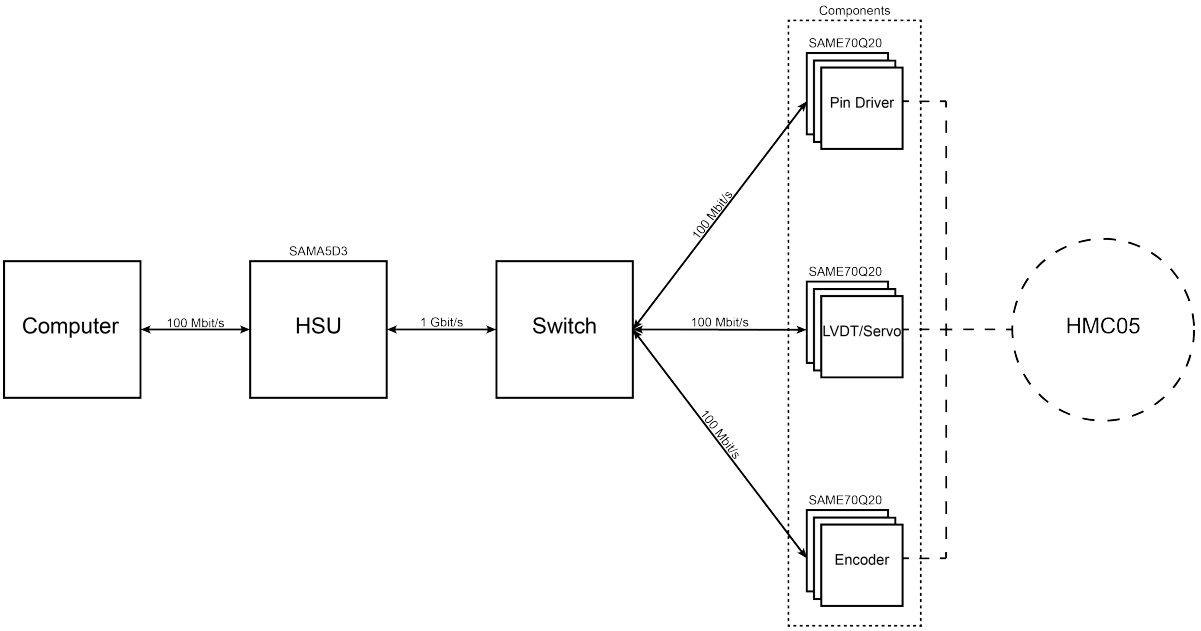


Figure 1.1: System Overview

design the simulation on the HSU and a link to the computer/web-server [2]. Group 1 will design the pin driver, as will be described in this particular thesis.

1.3. The Pin Driver

Thus the overall goal of the project is to create a system that is able to mimic a hydraulic plant. As stated in the previous section, the pin driver is a device that handles the in- and output relation between the Hydraulic Motor Controller, abbreviated as HMC, and the Hydraulic Simulation Unit, abbreviated as HSU.
The HMC has over 70 in- and outputs, these pins are pre-defined in the HMC set-up. Thus it would be possible to make a specific driver for every in- or output. However, this would be a time consuming job, which would be very costly. When a driver would break down, work would be halted until a new one is made or for all different drivers there would be a spare version needed. One of the solutions one would think of is to group in- or outputs that behave very likewise, but now still multiple groups would be present and a wrong driver at the wrong place would destroy that driver completely. Good management for such a system is needed.
HedoN wants to take this a step further by creating just one generic pin driver that is up to all of the different tasks, the pin driver would be configured to do a certain task and will receive an update on this task every millisecond. Since the HMC has over 70 in- and outputs with signals of very different order of magnitudes, these range from as small as 10s of milli amps to a couple of amps. Since all these pins have such different orders, they also have different precision levels associated with them. This has led to the pin driver having 3 current operating ranges, from 35 mA up to 3.5A, which is further elaborated on in the program of requirements.
The task of the Bachelor Graduation Project Group is to solve this problem and this thesis describes the design of the hardware for the generic pin driver associated with the HMC. The Pin Driver will have a Micro Controller Unit, MCU, which will be programmed and controlled by the Communication group. Further information on the MCU and its workings can be found in their thesis [1].

1.4. Outline of Report

In this Report the design of the pin driver is discussed. In Chapter 2 a system overview is provided and the Programme of Requirements is discussed. Chapter 3 describes the Overall Design Choices which consider the in- and output signals, the amplification stage, the feedback method and the control system. Chapter 4 describes the Design of the Voltage Amplifier. It describes the control system, system overview, the noise calculation and the stability of the the voltage amplifier. Chapter 5 describes the Design of the Transconductance Amplifier. This description is done in a similar way as the Voltage Amplifier, but the focus of this chapter is on precise measurement done in the circuit and how these are accomplished. Chapter 6 describes

the merging of the subsystems and solving the problems that are encountered. This includes measurement positions, the design for the handling protocol and pre-filter design. In Chapter 7 the Testing Methods for both the simulation and an actual system are discussed. This is followed by carrying out these tests. Unfortunately no actual systems have been carried out. The thesis is then wrapped up with the conclusion and evaluation in chapter 8.

2

Programme of Requirements

In this chapter a short system overview is presented where both the in- and outputs and the internal signals of the pin driver are discussed. Followed by the Requirements for the Pin Driver Unit.

2.1. System Overview

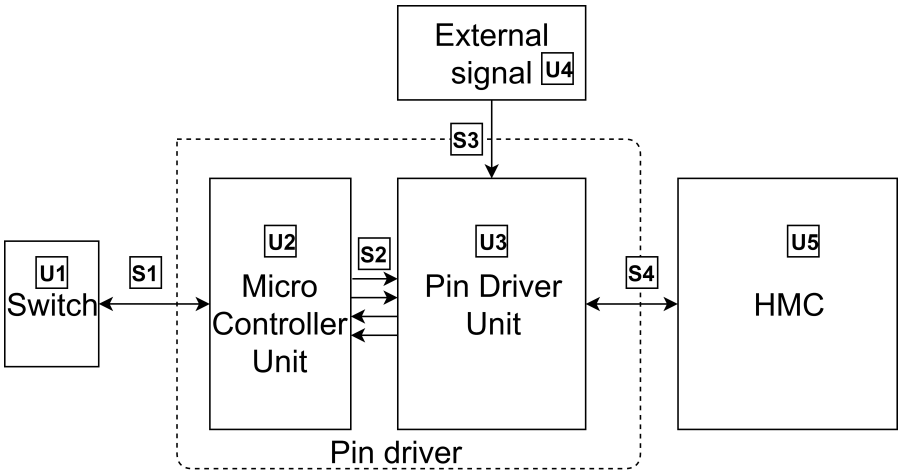


Figure 2.1: System overview of a Pin Driver with the neighbouring devices.

As briefly discussed in Chapter 1, the pin driver is the device driving the pins of the HMC connected in a simulation setting. Meaning, the pin driver needs to be able to drive a voltage or current output to the HMC and measure. In Figure 2.1 the system set-up is shown.

On the left side the Switch named Unit 1, abbreviated as U1, is located. The switch is connected to the pin driver module with an Ethernet connection, S1. This switch distributes the Ethernet packages received from the Hydraulic Simulation Unit, the corresponding setup can be seen in Figure 1.1. In these packages the mode of the pin driver and signal to drive on the output is sent.

U2 is the Micro Controller Unit (MCU), the MCU processes the data received from both the Switch and the Pin Driver Unit (PDU), U3. Signals 2 abbreviated to S2 describe the different connections between the MCU and the PDU, the desired output is sent to the PDU using a SPI connection to Digital to Analog Converter, just as the measured voltage and current are sent back over a SPI connection using a Analog to Digital Converter. Also several control signals are sent to the PDU, further elaboration on these signals can be found in Section 3.1.
The parts U1, S1, U2 are not in scope of this thesis and are done by sub-group 2 [1]. S2 is on the border between the two different groups and their assignments.

The Pin Driver Unit, U3, is responsible for the creation and measuring of the desired output (S4). This is either a voltage or a current. Some signals have such precise performance requirements, such that they are not made by the pin driver. However, the pin driver should be in charge, whether this signal should be used or not. To do this, an external signal from a different module (U4) such as a LVDT-Servo can be provided (S3) and fed to the output (S4).

The output of the system is connected to the HMC, U5. Which can be either "receiving" the voltage or current or, when the Pin Driver Unit is in voltage mode, the HMC can be driving a current onto the output S4. Such that the HMC is controlling the current the Pin Driver is receiving.

2.2. Requirements

In this section the requirements are discussed, first the requirements for the total system are discussed. Followed by the functions of the Pin Driver, the input signals of the Pin Driver Unit, the output signals of the Pin Driver Unit and lastly the additional requirements.

2.2.1. Total System Requirements

The requirements described in this section are the basis criteria for the complete system, from Hydraulic Simulation Unit to the Pin Driver.

Req. T-1. The key requirement for the overall system is the speed. The total system should be able "to update" every millisecond. This means for the pin driver module that the output should be changeable every millisecond and it needs to be able to send back its measured current and voltage.

Req. T-2. The system should be modular, which translates to the pin driver being versatile and should be able to be replaced for each other. All pin drivers should be able to do all functions.

2.2.2. Functions of Pin Driver

In this section the functions and the corresponding requirements for the Pin Driver Unit (U3) are discussed. First the requirements of the Functions are described, followed by the different output modes and lastly the different measurements the system needs to do.

Req. F-1. Switching times between different output modes may take up several tenths of milliseconds.

Output Modes

Req. FO-1. The PDU needs to be able behave like a voltage amplifier.

Req. FO-2. The PDU needs to be able behave like a transconductance amplifier.

Req. FO-3. The PDU needs to be able to route an external signal to the output of the Pin Driver (S4).

Measurements

Req. FM-1. The PDU needs to measure the voltage driven on the output.

Req. FM-2. The PDU needs to measure the current driven on the output.

Req. FM-3. The temperature of the amplification stage in the circuit needs to be measured.

Req. FM-4. The external signal does not need to be measured.

2.2.3. Input Signals

Req. I-1. The input voltage for a certain output level, is received using a SPI connection to a DAC.

Req. I-2. Control signals to determine the mode are sent from the MCU.

Req. I-3. The output voltage and output current need to be measured and is read by the MCU using a SPI connection to an ADC.

2.2.4. Output Signal

This section describes requirements of the output signal to the HMC, S4.

Req. O-1. The settling time must be less than 100 µs, while 10 µs would be nice to have.

Req. O-2. The pin driver should be able to drive purely resistive loads. Desired would be when the pin driver is able to drive inductive loads with an inductance in the order of millihenry's.

Voltage

Req. OV-1. The output voltage may range from -35V to +35V.

Req. OV-2. The output voltage needs to be controlled and measured with a precision of 10 mV referred to output.

Current

Req. OC-1. The output Current may range -3.5A to +3.5A.

Req. OC-2. The output current needs to be controlled and measured with a precision as in Table 2.1 for the corresponding levels of output current.

Req. OC-3. The highest output current mode is only used for a short period of time, in the order of tens of milliseconds.

Table 2.1: The different current ranges and the precision associated with these ranges.

Number:	Current Range (min.):	Current Range (max.):	Nice to Have-Precision	Must Have - Precision	HMC output Precision
1	-35 mA	35 mA	10 μA	50 μA	20 μA
2	-350 mA	350 mA	100 μA	500 μA	200 μA
3	-3500 mA	3500 mA	1000 μA	5000 μA	2000 μA

The External Signal

Req. OE-1. The voltage may range from -35 to +35 V.

Req. OE-2. The voltage may range from -3.5 to +3.5 A.

2.2.5. Additional Requirements

The following additional requirements to the pin driver are present.

Req. A-1. The system needs to work with a power supply which supplies both -40 and +40 V direct current.

Req. A-2. The Micro Controller Unit is a SAM E70.

Req. A-3. At least two pin drivers, and more pin drivers would be preferred, should fit on a Euro Card format PCB which is 100 millimeters by 160 millimeters. This is due to the need to make the overall system as small as possible, the amount of needed pin drivers for a simulation system and the amount of switch inputs.

Req. A-4. For functional purposes, the power dissipation in the current sense resistor should not exceed one watt.

3

Overall Design Choices

Chapter 1 and 2 explain what the pin driver needs to do, which connections it has and the requirements it has. This chapter describes the basic setup which has been introduced in Chapter 2 in more detail, the signals will be further elaborated on. Section 3.1 the input and output signals of the PDU are described. The amplification stage is explained in Section 3.2. The design choice of the type of feedback method is discussed in Section 3.3. In Section 3.4 the design choices regarding the control system are explained.

3.1. Input and Output signals

In Section 2.1 an introduction has been made on the input- and output signals of the pin driver. The overview of these signals can be found in Figure 3.1. As mentioned before Signal S1 is not in the scope of this thesis. The signals S2, S3 and S4 are further explained. Of these signals several aspects (e.g. function and type of signal) will be explained. The signals and hardware which connect the digital and analogue side of the system and their consequences are elaborated on.

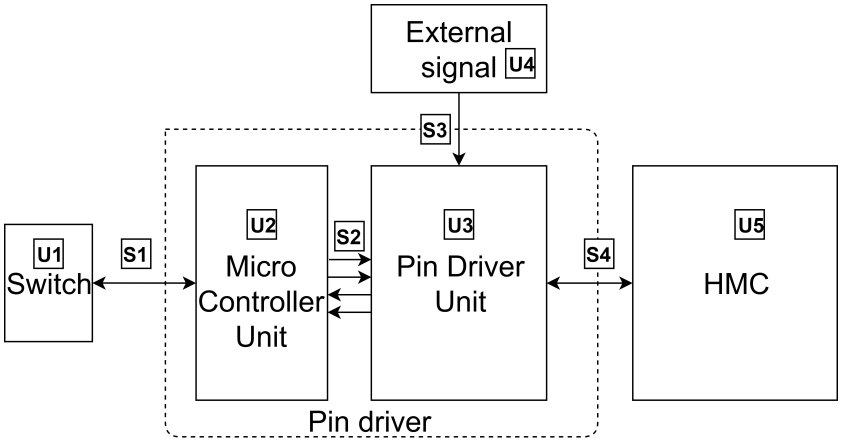


Figure 3.1: Pin driver overview.

3.1.1. Input signals

This section will discuss the signals going into the PDU. There are a total of 4 different signals which enter the PDU.

1. Digital-to-Analogue Controller - SPI signal (S2)
    - Source: MCU
    - Function: Control the DAC voltage level

The DAC-SPI-signal originates from the MCU and communicates the desired voltage level to the DAC and in this way controls the input voltage of the PDU. The established input voltage multiplied by the gain factor of the system will result a certain voltage. The choice of a SPI communication interface over other interfaces has been made due to the preference from the communication team.

DAC selection The DAC translates the digital input to analogue input for the PDU to work with. To decrease input errors high accuracy is demanded. Even with 1 ms tick the speed of the PDU is compared to the capabilities of modern day DACs not demanding. A high precision DAC is therefore favoured over a high speed Digital-to-Analog Converter.
The focus points of this high precision DAC are: bipolarity, resolution, settling time and integral non linearity (INL). The system is bipolar, to be able to meet the voltage range in Requirement OV-1 the DAC must be bipolar. In the group of high precision bipolar DACs the preferable DACs are ± 5V. These DACs combine high resolution (16-bits) and low INL (maximal 2 bits).

An overview of a selection of ± 5V DACs is presented in Table 3.1. A Buffered output is preferred over a unbuffered output because it has the advantage of having a lower output impedance and no need of an external amplifier.[3] [4] The decision has been made to choose a combination of low settling time and low INL. The DAC8734 is used as it preforms best in the combination of these factors.

Table 3.1: Overview of (± 5 V) DAC - Datasheets are in Appendix C

Model	Resolution (bits)	Settling Time (µs)	INL (bits)	Output
DAC714	16	10	1	Buffered
DAC8734	16	6	1	Buffered
DAC8871	16	1	1	Unbuffered
DAC8831	16	1	1	Unbuffered
DAC8832	16	1	1	Unbuffered
DAC7734	16	10	2	Buffered
DAC7731	16	5	3	Buffered
AD5760	16	2.5	0.5	Unbuffered
AD5781	18	1	0.5	Unbuffered
LT2642	16	1	1	Unbuffered

The output of the pin driver can reach -35 to 35 V (Req. OV-1). To be sure the DAC doesn't throttle at high outputs the maximum level of the output is raised to ± 40 V. This will result that when the signals are kept within the requirement (OV-1) the maximum level of the DAC will not exceed ± 4.375 V. The chosen DAC has the range of ±5V, it therefore requires a amplification of eight to reach the ± 40V.
At a resolution of 16 bits the stepping size of the signal can vary at a maximum of 80V (± 40V) the following precision can be obtained:

$$stepping\ size = \frac{voltage\quad range}{resolution} = \frac{80}{2^{16}-1} = 1.2mV$$

2. Control mode switching signal (S2)

   - Source: MCU
   - Function: Controls which feedback loop is used in the PDU.

   As will be discussed in Section 3.4.2 the PDU can switch between the voltage or transconductance feedback loops. To be able to change between these loops switches need to be opened or closed. An in depth look on how this process takes place is provided in Chapter 6.

3. Control measurement range (S2)

   - Source: MCU
   - Function: Controls the measurement range of the sense resistors

To provide better accuracy the measurement ranges can be changed by selecting different sense resistors using switches. The influence of these measurement ranges are explained in Section 5.2.1. The control signals provide a way to open or close these switches.

4. External signal (S3 & S2)
    - Source: External and MCU
    - Function: Controls output mode

    As stated in specification FO-3 it must be possible to route an external signal through the PDU. Therefore it is required to use a control signal (S2) to control the relay between the external output (S3) and the output of the PDU(S4). The All the signals which will run through the external path through the PDU will be the same voltage, current and time specifications as the PDU.
    The main purpose of the external signal is to be able to simulate broken cables, possible errors in the crane and signals from specialized systems i.e. LVDT/Servo. This signal does not get measured or altered in any way.

3.1.2. Output signals

This paragraph will discuss the signals which the PDU delivers. There are a total of three signals.

1. SPI-ADC signal (S2)
    - Destination: MCU (E70)
    - Function: Measuring results from the ADC

    The Analogue-to-Digital (ADC) measures the voltage levels at certain parts of the PDU. These values corresponds to voltage and current levels in the PDU. These values are send back to the MCU using the SPI communication.

    ADC selection For the ADC the same criteria as the DAC selection have been used. An extra criteria for the ADC is the input type of the ADC. A pseudo-differential true bipolar ADC is preferred as it does not need an additional op amp for input control [5]. A selection of ADCs is shown in Table 3.2.
    A combination of high resolution and low INL the LTC2328 can achieve the best measurement results.

Table 3.2: Overview of ADC's - Datasheets are in Appendix C

Model	Resolution (bits)	offset (bits)	INL (bits)
LTC1419	14	5	0.8
LTC1855	14	0.5	1
LTC1859	16	0.5	3
LTC2328	18	0.5	1
AD7606	16	0.5	2

2. Temperature (S2)
    - Destination: MCU
    - Function: Prevention of overheating

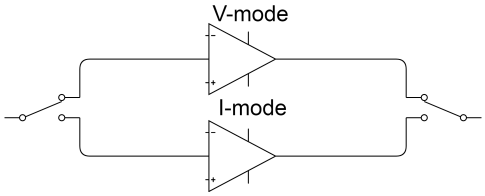
    To prevent overheating or increasing noise and errors it is necessary to monitor the temperature. This signal is used to shut down the system when the temperature becomes critical and may cause damage to the pin driver.

3. Signal to the HMC (S4)
    - Destination: HMC
    - Function: Output signal

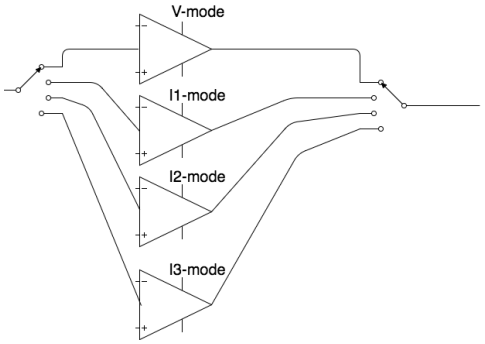
    This signal is used as information carrying signal to the HMC. The (changing of) values of voltage and current represents data from the simulation. The signal has several requirements stated in Section 2.2.4.

3.2. Amplification stage

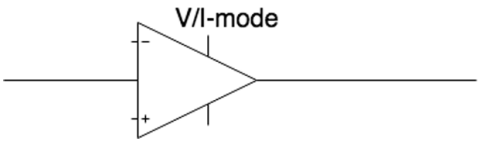
As discussed in Requirement FO-1 and FO-2 the pin driver can be set to a voltage amplifier and a transconductance amplifier. Both of these modes require a amplification stage to be able to meet the maximum voltage level ±35V (Req OV-1) and maximum current level ±3.5A (Req OC-1). To be able to get from a ± 5V DAC to these ratings an amplification stage is needed.
There are several methods to choose the implementation of the amplification stage. One of the options would be to design two completely different circuits for the different modes, which the output would switch to. Figure 3.2a is a schematic drawing of this.
The second option would be to also create different stages according to the three current levels, which can be found in Figure 3.2b.
The last option is to, in some way, incorporate these two possible output modes in a circuit which uses only one amplifier stage as in Figure 3.2c.
From a spacial point of view also the last choice would be preferable. Since, requiring just one amplifier stage takes less space in a design. This provides a possibility of fitting more PDU on the pin driver (A-3). From a financial point of view the last choice, only one amplifier stage, would be preferable since power amplifiers are relative expensive and thus requiring more than one would be undesirable.
Thus, the choice has been made to only use one amplification stage for both current and voltage.



(a) A different amplifier stage for voltage and current systems. All current modes are embedded in one system.



(b) A different amplifier stage for the different voltage and current levels. Every mode is split up.



(c) One amplifier stage for both current and voltage controlled systems.

Figure 3.2: Schematic view on different amplification options.

3.3. Feedback

Feedback is the backbone of design and control processes of electrical signals. Feedback is used to create a linear relation between the in- and output and is one of the most important aspect in designing circuits. Since poorly designed feedback networks could easily lead to instability or unwanted effects. In this section, multiple considered feedback topologies are discussed. On the base of the specifications in Chapter 2 considerations have been made on, i.e. controllability, feasibility and ease of implementation.

3.3.1. Digital adjustment

The first option is to control the system using digital feedback method, meaning the system will be controlled by either the Micro Controller Unit (MCU) or using dedicated Digital to Analog- and Analog to Digital Converters. As schematically depicted in Figure 3.3 The benefit of this system is that the values already need to be send back to the MCU since this is a requirement (Req. FM-1 & FM-2). One of the problems with this solution is that the feedback will only change at discrete time steps. Set by the speed of either the MCU or the dedicated DAC & ADC. Which could lead to high overshoot or oscillations around the desired solution. This could be solvable, since the values are already digitized and could easily be altered to for example make the oscillation as small as possible. A reason why this solution could be desirable is that this solution will probably needs less components. Since all controlling happens with components that are already needed for the system. A problem with the system is however with the implementation, for this implementation there needs to be very close collaboration between the communication group, subgroup 2, since they do all the working on the MCU. Which leads to a very high dependency between the two groups. which is seen as too risky.

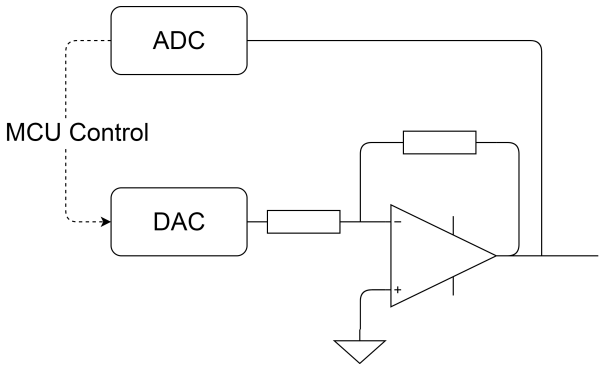


Figure 3.3: Feedback using both DAC and ADC. The MCU controls the feedback loop digitally using the values from the ADC.

3.3.2. Analog feedback

A different method that has been considered is an analog feedback implementation. One of the advantages of an analog implementation is that there is no intensive collaboration with sub-group 2 is needed. Also there is no conversion from analog to digital domain and vice versa in the feedback loop. Previous described problems will not be present. Another advantage of an analog system is the predictability, the performance might change due to heating but the system will behave in the same way every time. While, when looking at digitally controlled system the timing might impact the results extensively. Also an analog system can be quite easily tested in a simulation system, for example LTSpice. The last advantage of an analog feedback is after the designing process. A stable analog feedback network can benefit from additional digital control systems by using the ADC to build databases of in regularities and errors which can be compensated to decrease errors.

3.3.3. Decision

Because of the risk being to dependent on subgroup 2 and the possibility of simulation, the analog feedback system has been chosen over the digital feedback network.

3.4. Control System

As the choice of an analog feedback method has been made, the next step is the implementation of the control system. The control system of both subsystem will be designed in order to control the input voltage, give the preferred output and prevent the system from becoming in stable.

3.4.1. Implementation

The implemented option uses an integrator within the system. A system as in Figure 3.4 would be implemented. The negative feedback in the control loop is used to control the output and prevent is from instability. The full control systems and its abilities of the voltage amplifier and transconductance amplifier will be

explained in Section 4.3 and 5.4

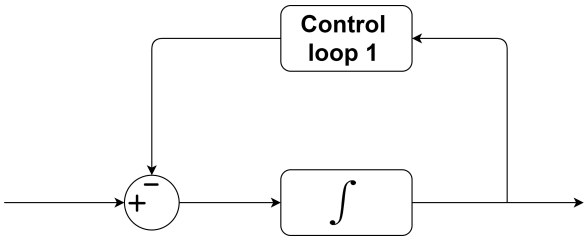


Figure 3.4: Implementation of the control loop using feedback.

3.4.2. Combination

Both the voltage amplifier and the transconductance amplifier have a different control system. In Figure 3.5 an overview is provided of the implementation of switches in the control system. Using control signals from the MCU a change between the control loops can be executed.

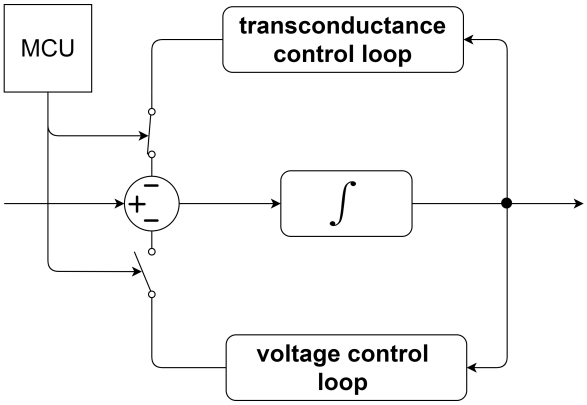


Figure 3.5: Control system using multiple feedback loops with switching capability.

4

Design of Voltage Amplifier

This chapter describes the design of the Voltage Amplifier. First the control system is described. Then the value selection to determine settling times are discussed. Continued by a discussion of the chosen system elements. The combination of selection these three are then used for the noise calculations. After the noise calculations the system is checked for stability. At last an overview of the system is provided.

4.1. Control System Design

As discussed in Section 3.4, the feedback will use an integrator. An integrator design is showed in Figure 4.2. The transfer function corresponding to such a system can be found in Equation 4.1 [6].

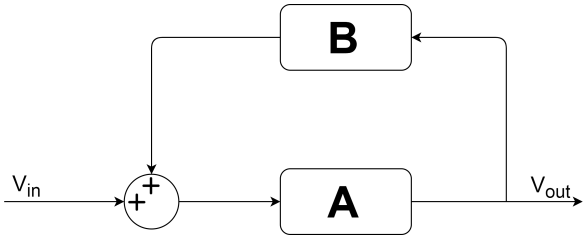


Figure 4.1: Feedback circuit using an arbitrary A and B in the system. Where A is implemented as an integrator.

$$H_{sys} = \frac{A}{1 + AB} \tag{4.1}$$

Parameter A in Figure 4.1 represents the integrator as in Figure 3.4. An integrator as an electric circuit can be defined as in Figure 4.2. It's corresponding transfer function is defined as in Equation 4.2.

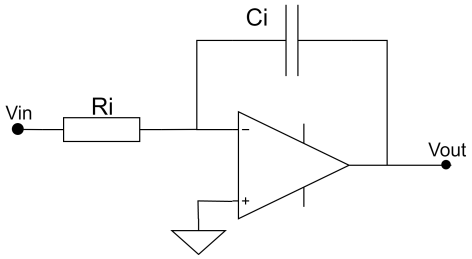


Figure 4.2: Integrator implemented in an electronic circuit.

$$H_{int}(s) = \frac{-1}{sR_iC_i} \tag{4.2}$$

Combining Equation 4.1 and 4.2 together the following transfer function for the control system is determined:

$$H_{sys}(s) = \frac{A}{1+AB} = \frac{H_{int}(s)}{1+H_{int}(s)B} = \frac{-1/sR_iC_i}{1-B/sR_iC_i} = \frac{-1/R_iC_i}{s-B/R_iC_i} \tag{4.3}$$

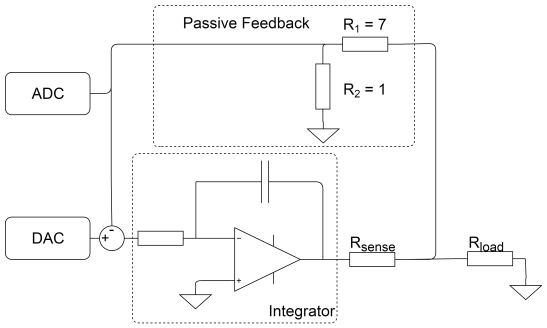
In which the pole of this system would be at:

$$pole: s - \frac{B}{R_iC_i} = 0 \rightarrow s = B/(R_iC_i) \tag{4.4}$$

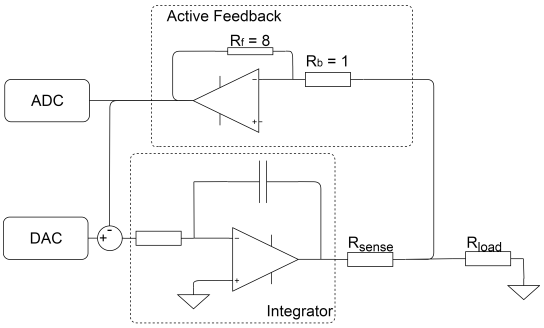
Both R_i and C_i are real and positive values. The pole of the system is in the right half plane (RHP) when B is a negative value, which means the system is unstable [7]. As long as B is a positive value the system is stable and controllable. As stated in Section 3.1.1 the voltage amplifier should have an amplification factor of 8, thus be needs to be:

$$|H_{sys}(0)| = |\frac{-1/R_iC_i}{-B/R_iC_i}| = |\frac{-1}{-B}| = 8 \rightarrow |B| = 1/8 \tag{4.5}$$

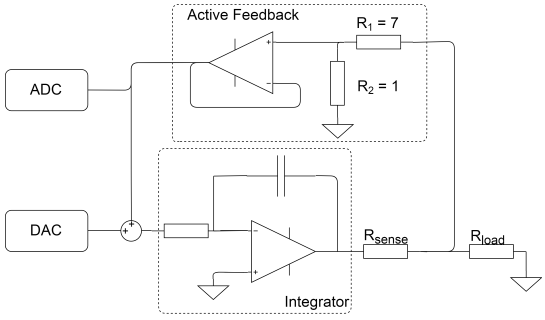
The value of $1/8$ can be obtained in several ways. It can be done in either active or passive feedback. The passive version will use a set of resistors as a voltage divider as seen in Figure 4.3a. The first active solution is to use an op amp to lower the voltage as seen in in Figure 4.3b. The second active option is to use the way implemented in the passive version but with a buffer attached to it. The reason for adding a buffer is the ADC being part of the feedback loop and a buffer guarantees enough current can be supplied for both the ADC and the feedback.
To be able to deliver these currents an active circuit is chosen over a passive. The reason a buffer is favoured over a system as Figure 4.3b is a higher input impedance. This results in only a very small current need. [8]



(a) Feedback circuit using an integrator and a passive feedback circuit.



(b) Feedback circuit using an integrator and an active op amp in the feedback circuit



(c) Feedback circuit using an integrator and an active buffer amplifier in the feedback circuit

Figure 4.3: Schematic view on different feedback methods

The transfer function of the feedback circuit with the buffer implementation as seen in Figure 4.3a provides the negative voltage to control the voltage amplifier. The transfer function is:

$$B(s) = \frac{V_{out}}{V_{in}} = \frac{R_2}{R_1+R_2} \tag{4.6}$$

Using this function for B in the transfer function in Equation 4.2results in the transfer function of the voltage amplifier

$$H(s) = \frac{A(s)}{1 + A(s)B(s)} = \frac{\frac{-1}{sC_iR_i}}{1 + \frac{-1}{sC_iR_i}\frac{-R_2}{R_1+R_2}} = \frac{\frac{-1}{R_iC_i}}{S + \frac{1}{R_iC_i}\frac{R_2}{R_1+R_2}} \tag{4.7}$$

This results in the location of the pole at:

$$pole :\rightarrow S = -\frac{1}{R_iC_i}\frac{R_2}{R_1 + R_2} \tag{4.8}$$

Knowing the ration between R_1 and R_2 results the pole position in

$$pole :\rightarrow S = -\frac{1}{8R_iC_i} \tag{4.9}$$

The system as shown in Equation 4.7 is a first order system. These systems are attached to the following parameters:

$$H(s) = \frac{D}{s + C} \tag{4.10}$$

$$\text{Impulse response } = De^{-Ct} \tag{4.11}$$

$$\text{Step response } = \frac{D}{C}(1 - e^{-Ct}) \tag{4.12}$$

The parameters these results in:

$$\text{Impulse response } = \frac{-1}{R_iC_i}e^{\frac{-1}{R_iC_i}\frac{R_2}{R_1+R_2}} = \frac{-1}{R_iC_i}e^{\frac{-1}{8R_iC_i}} \tag{4.13}$$

$$\text{Step response } = \frac{\frac{-1}{R_iC_i}}{\frac{1}{8R_iC_i}}(1 - e^{-\frac{1}{8R_iC_i}t}) = -8(1 - e^{\frac{1}{8R_iC_i}t}) \tag{4.14}$$

total function becomes

4.2. Value selection using control system

In accordance with Figure 4.3c, the system parameters are determined. These are the resistors and capacitors that determine the system its characteristic. In section 4.1 the preliminary work has already been done.

4.2.1. Calculations for the system

Using the formula 4.15 and 4.16 the settling time and rise time of the system can be calculated. The settling time and rise time are calculated as follows:

$$\text{settling time } T_s = \frac{4}{C} = \frac{4}{\frac{1}{8R_iC_i}} = 32R_iC_i \tag{4.15}$$

$$\text{rise time } R_s = \frac{2.2}{C} = \frac{2.2}{\frac{1}{8R_iC_i}} = 17.6R_iC_i \tag{4.16}$$

To get the settling time and rise time within the 1% margin of the 1ms the parameters are set to.

$$t_s \approx 10^{-5}, \text{ where } t_s = 32R_iC_i \rightarrow 32R_iC_i \approx 10^{-5} \tag{4.17}$$

$$t_r \approx 10^{-5}, \text{ where } t_r = 17.6R_iC_i \rightarrow 17.6R_iC_i \approx 10^{-5} \tag{4.18}$$

The resistance R_i of the integrator gets supplied by the DAC. As the DAC needs to deliver the current to create the desired voltage over this resistor, it is not desirable to make the resistor to small. The maximum

Table 4.1: Table containing all determined values for the voltage transfer function

Parameter	Value (in kΩ)	Parameter	Value (in pF)
R_i	10	C_i	100
R_1	700		
R_2	100		

voltage swing that could theoretically happen is 10V (from -40 V to 40V instantaneously). With a 10kΩ resistance the opamp then needs to deliver 1 mA, which most opamps are well capable to do.
The capacitor value C_i is picked according to the settling time formula. In order to keep the settling time within marges of the Requirement O-1 the capacitor needs to be around the 1 nF range.

The following parameters are determined giving the following system characteristics:

When these parameters filled in Equation 4.16 and 4.15 will result in the settling and rise time.

$$\text{Settling time } t_s = 32R_iC_i = 32 * 10000 * 100 * 10^{-12} = 3.2 * 10^{-5}[s] \tag{4.19}$$

$$\text{Rise time } t_r = 17.6R_iC_i = 1.76 * 10^{-5}[s] \tag{4.20}$$

R_1 and R_2 are relatively high valued resistors as will be discussed in Section 6.1 it is undesirable to have high current leaks, through the sense resistors. The downside of these high valued resistor is the amount of gain-error, as the input of the operational amplifier can be seen as parallel to R_2. Their equivalent resistor value is given by:

$$R_{eq} = \frac{R_2 R_{opamp}}{R_2 + R_{opamp}} \tag{4.21}$$

Where R_{opamp} is the input resistance of the operational amplifier. The gain will be given by:

$$G = \frac{R_{eq}}{R_{eq} + R_1} = \frac{\frac{R_2 R_{opamp}}{R_2 + R_{opamp}}}{\frac{R_2 R_{opamp}}{R_2 + R_{opamp}} + R_1} = \frac{R_2}{R_1 + R_2 + R_1 R_2 / R_{opamp}} \tag{4.22}$$

As the equations show, the bigger R_{opamp} is in comparison to R_1 and R_2 the smaller the effect on the gain is. When increasing the resistor values, the effect of the operational amplifier input resistance gets bigger. The choice for the values as stated here, is based on the elaboration in Section 6.1.

Using the values from Table 4.1 the transfer function becomes:

$$H(s) = \frac{\frac{-1}{R_iC_i}}{S + \frac{1}{R_iC_i}\frac{R_2}{R_1+R_2}} = \frac{\frac{-1}{1000*1*10^{-9}}}{s + \frac{1}{1000*1*10^{-9}}\frac{1}{8}} = \frac{-1 * 10^6}{s + 1.25 * 10^5} \tag{4.23}$$

The cut off frequency can be calculated and is:

$$|H(j\omega)|^2 = \frac{1}{2} \rightarrow f = 1.989 * 10^4 Hz \tag{4.24}$$

4.3. System overview

In this section the ideal system according to the control system is depicted. According to this ideal system the needed operational amplifiers are selected.

4.3.1. Ideal System

The ideal system can be found in Figure 4.4, this system is based on the control system described in Section 4.2. The added summator resistors sums the feedbackloop voltage from that of the DAC input voltage.
The amplified output signal goes through the sense resistor to the load connected. The sense resistor is needed for current measurements as is depicted in Chapter 5.

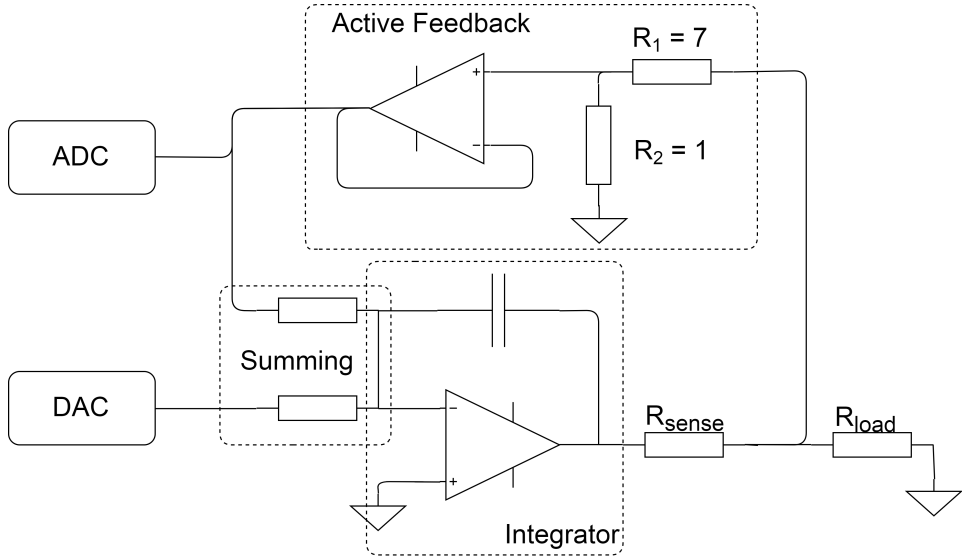


Figure 4.4: Overview ideal system based on setup of Section 4.2

4.3.2. Addition of System Elements

Integrator

For the integrator part a high current amplifier is required. An overview of the options is depicted in Table 4.2. The op amp must be bidirectional (± 35V). Therefore a double supply (± V) is needed, which can at least deliver these voltages. The OPA 2541, APEX PA61 and OPA541 still hold up to this spec. The OPA 2541 and APEX PA61 are high in price (over 100 euros per amplifier). Due to this price difference the OPA541 is picked as it still has similar specs at a lower price.

components didn't get our preference is due to the price of the component, which is over 100 euros per amplifier. The OPA541 is chosen as the high current amplifier.

Table 4.2: Different opamps for the integrator stage - Datasheets are in Appendix C

Name	Output current (A)	Slew rate ($V/\mu s$)	supply voltage(+/-V)
OPA 541	10	10	40
OPA549	8	9	30
OPA 2541	7	8	40
LM675	4	8	60(single)
OPA544	4	8	35
OPA2544	4	8	35
Apex PA61	10	2.8	45

Buffer

For the buffer amplifier the most important features are the low noise, low offset and to be able control at least +/- 5V. The AD8597, LMH6624,LT1028 and OPA211 all have high undesired bias currents. The OPA192 lacks the $\frac{1}{f}$ noise decreasing and therefore produces much noise (going to 500 $\frac{nV}{\sqrt{Hz}}$ at low frequencies). Because of these reasons the TLC2654 op amp has been chosen. It combines low voltage (e_n) and current noise density (i_n) at low and high frequencies and has low offset values.

4.4. Noise

Using the implementation discussed in Section 4.3, noise calculations are done on voltage amplifier. The noise calculations are Return-to-Output, since the specs are also given in Return-to-Output relationship. The noise bandwidth is taken from 0.1 Hz to 100 kHz, the pin driver only drives an update once every millisecond. However, the ADC chosen has a much shorter sampling time. Which could pick up this higher frequency

Table 4.3: Different opamps for the feedback stage - Datasheets are in Appendix C

Name	offset voltage(μV)	bias current (pA)	$e_n(\frac{nV}{\sqrt{Hz}})$	$i_n(\frac{pA}{\sqrt{Hz}})$	supply voltage(+/-V)
TLC2654	5	50	47(10Hz) 13 (1kHz)	0.004	8
OPA192	5	5	100 (10Hz) 12 (1kHz)	0.00015	18
AD8597	10	25000	1.07(10Hz) 1.5(1kHZ)	4.3	15
LMH6624	-25000	13000	0.92 (1MHz)	2.3 (1MHz)	6
OPA211	30	60000	2(10Hz) 1.1(1kHz)	3.2	18
ICL7652	0.6	4	94 (10Hz) 23 (1kHz)	0.004	8
LT1028	15	30000	1 (10Hz) 0.85 (1kHz)	1 (1kHz)	22

noise. In Figure 4.5 the noise sources and their position of introduction to the system are shown. All these noise sources are discussed in the upcoming sections.

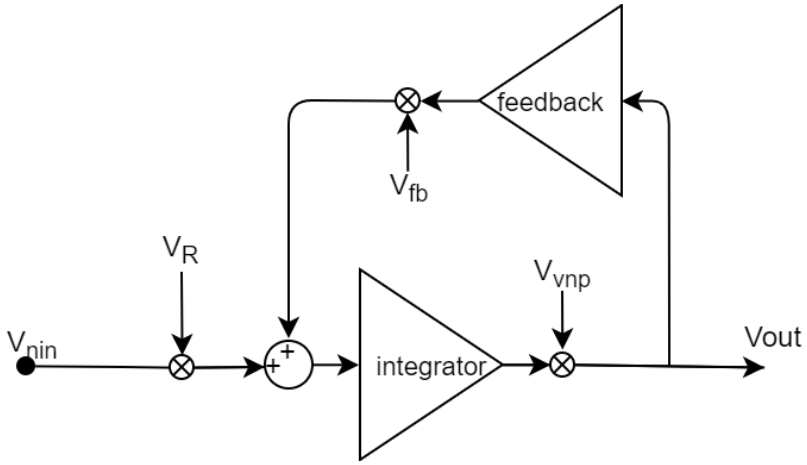


Figure 4.5: Noise sources and their positions in the voltage amplifier.

4.4.1. Input Noise

The Digital-to-Analog Converter is not an ideal voltage supply, it has a certain noise figure as depicted in the datasheet. The datasheet states the following figures; 1 µV for 0.1 Hz to 10 Hz, 40 µV for 0.1 Hz to 100×10^3 Hz and 60 $\text{nVHz}^{-1/2}$ for 0.1 Hz to 10×10^3 Hz.

With these figures the following input noise spectral density for the system is determined:

$$v_n = \begin{cases} 300\text{nVHz}^{-1/2}, & \text{for } 0.1 < \text{f} < 10 \text{ Hz.} \\ 60\text{nVHz}^{-1/2}, & \text{for } 10 < \text{f} < 10000 \text{ Hz.} \\ 110\text{nVHz}^{-1/2}, & \text{for } 10000 < \text{f} < 100000 \text{ Hz.} \end{cases} \tag{4.25}$$

Using Equation 4.25, the output reffered noise coming from the input can be determined.

$$H(f) = \frac{-1 * 10^6}{j2\pi f + 1.25 * 10^5} \tag{4.26}$$

$$\begin{aligned} \overline{V_n^2} &= \int_{0.1}^{100000} v_n^2 |H(f)|^2 df \\ &= \int_{0.1}^{10} 9 * 10^{-14} |H(f)|^2 df + \int_{10}^{10000} 3.6 * 10^{-15} |H(f)|^2 df + \int_{10000}^{100000} 1.21 * 10^{-14} |H(f)|^2 df \\ &= 5.70 * 10^{-11} + 2.14 * 10^{-9} + 1.40 * 10^{-8} \\ &= 1.62 * 10^{-8} \text{V}^2. \end{aligned} \tag{4.27}$$

$$\overline{V_n} = \sqrt{\overline{V_n^2}} = \sqrt{1.62 * 10^{-8}} = 0.13\text{mV} \tag{4.28}$$

4.4.2. Summing Resistors

Resistor noise, also known as Thermal noise, is a noise source which is always present for any resistor. The amount of noise is calculated as in Equation 4.29. [9]

$$\overline{v_R^2} = 4kTR(\frac{V^2}{Hz}) \tag{4.29}$$

Where $\overline{v_R^2}$ is the voltage noise density for a resistor, k is the Boltzmann constant, T is the temperature in kelvin and R is the value of the resistor in ohm. Since their values are the same and in an equivalent model they can be set before the resistor, they can be seen as inputs for the feedback loop. Such that, the same relation to the output applies as in Equation 4.27.

$$\overline{V_R^2} = \int_{0.1}^{100000} \overline{v_R^2} |H(f)|^2 df \tag{4.30}$$

The voltage noise density per resistors is as follows:

$$\overline{v_R^2} = 4kTR = 4 * k * 293.15 * 1000 = 4.05 * 10^{-18}(\frac{V^2}{Hz}) \tag{4.31}$$

Which has an output referred noise as follows:

$$\overline{V_R^2} = \int_{0.1}^{100000} \overline{v_R^2} |H(f)|^2 df = \int_{0.1}^{100000} 4.05 * 10^{-18} |H(f)|^2 df = 7.08 * 10^{-12} \text{V}^2 \tag{4.32}$$

$$\overline{V_R} = \sqrt{\overline{V_R^2}} = 2.66 \mu\text{V} \tag{4.33}$$

4.4.3. Integrator noise

The integrator noise consists of the noise sources from the operational amplifier. For the power amplifier used for the integrator there is one noise source specified, the voltage noise spectral density at the input of the opamp terminals. First the noise from this sources to the output of the integrator is determined, than by calculating a transfer function which has its input after the integrator. A new transfer function is determined. The precise elaboration can be found in Appendix A.1. An elaboration on the calculations can be found in [9].

The voltage noise of the opamp referred to the output of the pin driver is as follows.

$$\overline{V_{vn_p}^2} = \int_{0.1}^{100000} \overline{v_{vn_p}^2} (1 + \frac{1}{4\pi^2 f^2 R_i^2 C_i^2}) |H_{int_{out}}(f)|^2 df \tag{4.34}$$

Where, $\overline{v_{vn_p}^2}$ is the voltage noise spectral density of the opamp, R_i is the resistance of the integrator, C_i is the capacitance of the integrator and $|H_{intout}(f)|^2$ is the transfer function corresponding inserting a noise source after the integrator as stated in Appendix A.1. However the voltage noise spectral density is not constant over frequency as can be seen in Figure 4.6.

For the calculations the following approximation has been made.

$$v_{vn_p} = \begin{cases} 300\text{nVHz}^{-1/2}, & \text{for 0.1 < f < 10 Hz.} \\ 100\text{nVHz}^{-1/2}, & \text{for 10 < f < 100 Hz.} \\ 70\text{nVHz}^{-1/2}, & \text{for 100 < f < 1000 Hz.} \\ 30\text{nVHz}^{-1/2}, & \text{for 1000 < f < 100000 Hz.} \end{cases} \tag{4.35}$$

$$\begin{aligned} \overline{V_{vn_p}^2} &= \int_{0.1}^{100000} \overline{v_{vn_p}^2} (1 + \frac{1}{4\pi^2 f^2 R_i^2 C_i^2}) |H_{int_{out}}(f)|^2 df \\ &= \int_{0.1}^{10} \overline{v_{vn_p}^2} (1 + \frac{1}{4\pi^2 f^2 R_i^2 C_i^2}) |H_{intout}(f)|^2 df + \int_{10}^{100} \overline{v_{vn_p}^2} (1 + \frac{1}{4\pi^2 f^2 R_i^2 C_i^2}) |H_{intout}(f)|^2 df \\ &+ \int_{100}^{1000} \overline{v_{vn_p}^2} (1 + \frac{1}{4\pi^2 f^2 R_i^2 C_i^2}) |H_{intout}(f)|^2 df + \int_{1000}^{100000} \overline{v_{vn_p}^2} (1 + \frac{1}{4\pi^2 f^2 R_i^2 C_i^2}) |H_{intout}(f)|^2 df \\ &= 5.70 * 10^{-11} + 5.76 * 10^{-11} + 2.60 * 10^{-10} + 2.11 * 10^{-10} = 5.86 * 10^{-10} \end{aligned} \tag{4.36}$$

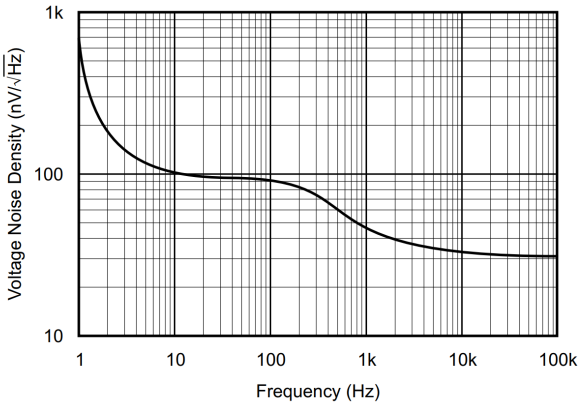


Figure 4.6: Voltage noise spectral density of the OPA541 power amplifier. [10]

$$\overline{V_{vn_p}} = \sqrt{5.86 * 10^{-10}} = 24.2\mu V \tag{4.37}$$

4.4.4. Noise from the feedback loop

Again some resistor noise is present in this part of the system. The found amount of noise is given in Equation 4.38. To buffer the voltage, an opamp is used. This opamp again introduces noise. For this opamp the noise is specified in voltage noise density and current noise density. The found value is given in Equation 4.39, the elaboration on the method used is found in Appendix A.2.

$$\overline{V^2_{fb_R}} = 3.54 * 10^{-11} \rightarrow \overline{V_{fb_R}} = 6\mu V \tag{4.38}$$

$$\overline{V^2_{fb_{op}}} = 3.54 * 10^{-11} + 3.73 * 10^{-11} = 7.27 * 10^{-11} \rightarrow \overline{V_{fb_{op}}} = 8.53\mu V \tag{4.39}$$

4.4.5. Output Noise

These noise figures can be summed as follows [9]:

$$\begin{aligned} \overline{V^2_{out}} &= \overline{V^2_n} + \overline{V^2_R} + \overline{v^2_{vn_p}} + \overline{V^2_{fb_R}} + \overline{V^2_{fb_{op}}} \\ &= 1.62 * 10^{-8} + 7.08 * 10^{-12} + 5.86 * 10^{-10} + 3.54 * 10^{-11} + 7.27 * 10^{-11} \\ &= 1.69 * 10^{-8} \end{aligned} \tag{4.40}$$

$$\overline{V_{out}} = \sqrt{\overline{V^2_{out}}} = \sqrt{1.69 * 10^{-8}} = 0.13mV \tag{4.41}$$

This results in a Peak-Peak output Voltage, V_{pp}, which covers 99.94% of the peaks[9].

$$V_{pp} = 6.8\overline{V_{out}} = 0.884mV \tag{4.42}$$

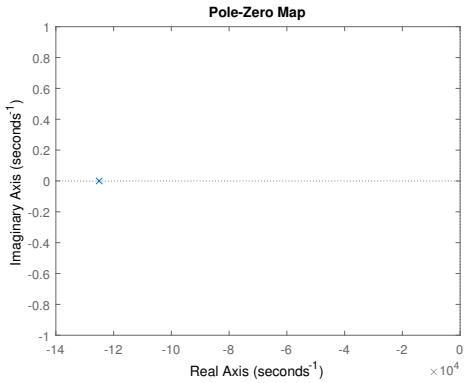
The major source of the output noise is the noise from the input of the Digital-to-Analog Converter. The output noise figure is well within the margin of 10 mV of Requirement OV-2.

4.5. Stability

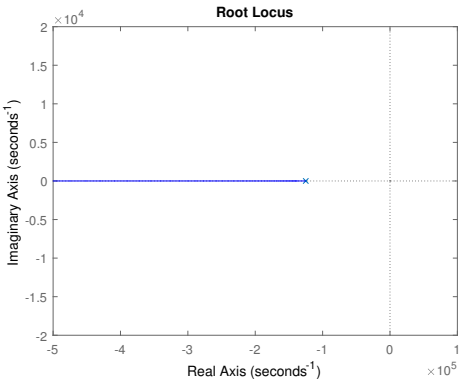
This section focuses on the stability of the voltage amplifier. Using various loads an estimation of the stability can be given. For this estimation the transfer function is needed from Section 4.2. The pole zero placement with corresponding root locus of the transfer function is plotted in Figure 4.7. Three types of load will be tested. At first the resistive load, then the capacitive load and at last the inductive load.

4.5.1. Resistive load

Using a resistive load the transfer functions does not change. This means the pole placement and root locus are the same as in Figure 4.7a and 4.7b. As the root locus goes to minus infinity the system can be considered stable. Therefore Using a resistive load the voltage amplifier is stable.



(a) Pole zero placement of the voltage amplifier.



(b) Root locus of the voltage amplifier.

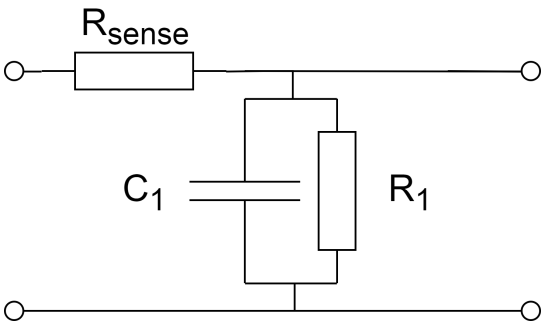
Figure 4.7: Stability of the voltage amplifier.

4.5.2. Complex load

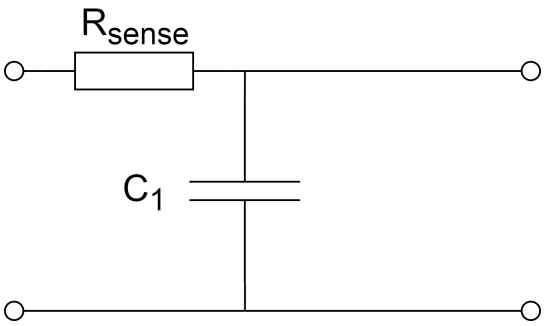
By introducing capacitive and inductive loads shown in Figure 4.8 and 4.11 the transfer function does change. It is therefore necessary to check if under these loads the system remains stable.

Capacitive load

The loads shown in Figure 4.8 shows to tested capacative loads.



(a) Resistor in parallel with a capacitor.



(b) First order capacitive LPF.

Figure 4.8: Schematic view of the Capacitive load types.

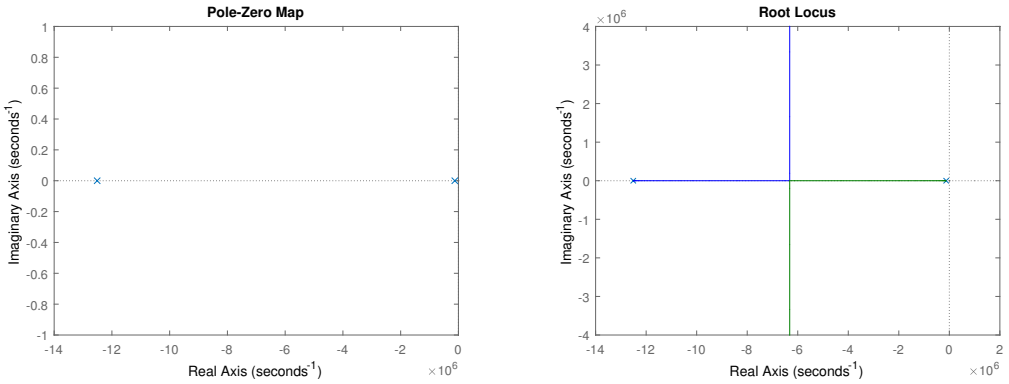
The following transfer functions are related to the voltage amplifier with the loads. The transfer function of the system with load of Figure 4.8a is

$$H(s) = H_{sys}(s)H_{load}(s) = \frac{-1*10^6}{s+1.25*10^5} * \frac{\frac{R_1}{1+R_1sC_1}}{R_{sense}+\frac{R_1}{1+R_1sC_1}} = \frac{-1*10^6}{s+1.25*10^5} * \frac{\frac{1}{R_{sense}C_1}}{s+\frac{R_1+R_{sense}}{R_1R_{sense}C_1}} \tag{4.43}$$

From Figure 4.8b the load will set the load to the transfer function of:

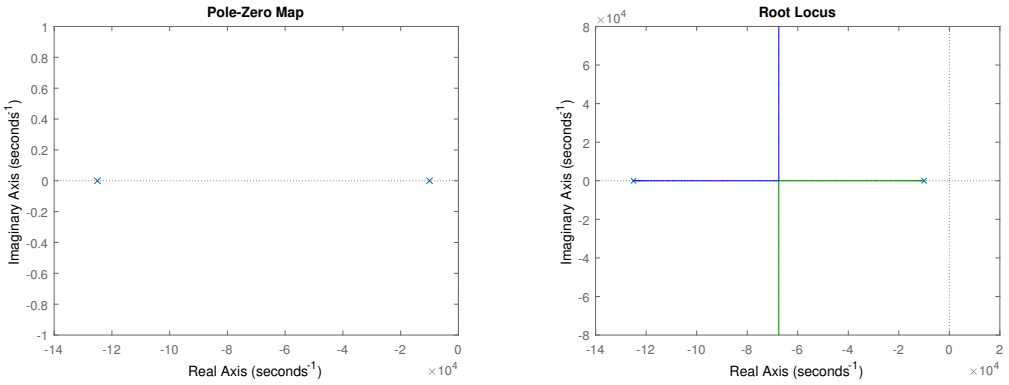
$$H(s) = H_{sys}(s)H_{load}(s) = \frac{-1*10^6}{s+1.25*10^5} * \frac{1}{SC_1R_{sense}+1} = \frac{-1*10^6}{s+1.25*10^5} * \frac{\frac{1}{R_{sense}C_1}}{s+\frac{1}{R_{sense}C_1}} \tag{4.44}$$

These transfer function will results in a change in the pole zero placement depicted in Figure 4.9a and 4.10a with the corresponding root locus in Figure 4.9b and 4.10b. Adding a resistor parallel to the capacitor shifts the pole more to the left. This means adding a resistor parallel to the load will keep the system more stable. As seen at the location of the poles in in the root locus they are positioned far in the left plane. The attachment of this load can be considered stable.
Even if the system is stable it can still be harmed by peak voltages or currents. Because the capacitor will charge up and can release this voltage very fast it is adviced to not use capacitors above 1,6 μF as these can cause spikes above 40 V.



(a) Pole zero placement. (b) Corresponding root locus.

Figure 4.9: Stability of the voltage amplifier using a capacitive load displayed in Figure 4.8a(values R_{sense} = 80 $m\Omega$, R=100 Ω and C = 1 μF)

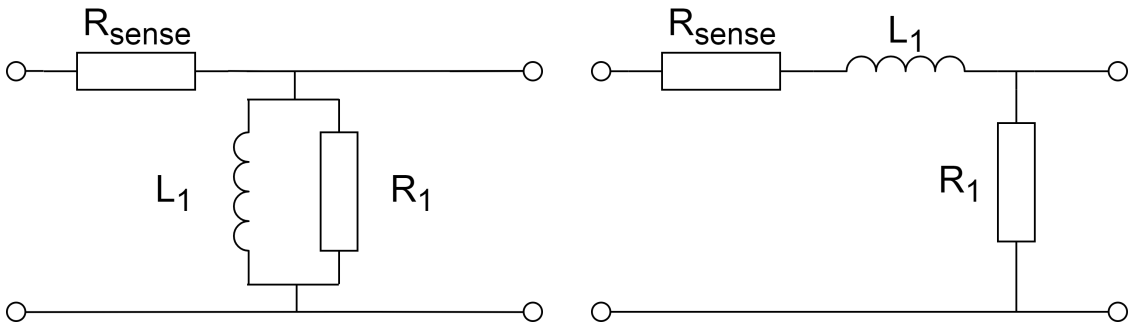


(a) Pole zero placement. (b) Corresponding root locus.

Figure 4.10: Stability of the voltage amplifier using a capacitive load displayed in Figure 4.8b (values R_{sense} = 80 $m\Omega$, R=100 Ω and C = 1 μF)

Inductive Load

The loads shown in Figure 4.11 are the tested inductive loads.



(a) Resistor in parallel with a inductor (b) First order inductive LPF.

Figure 4.11: Schematic view on Inductive load types

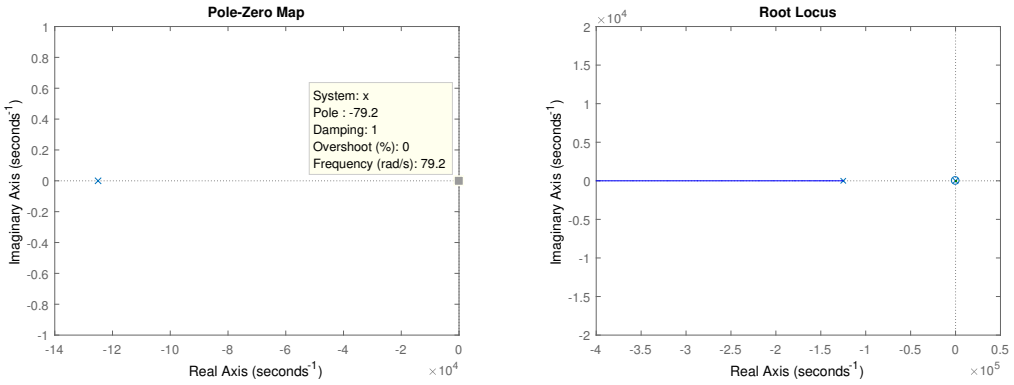
The same as for the capacitive loads, the transfer function changes due the type of load attached. The transfer function of the voltage amplifier with the load of Figure 4.11a

$$H(s) = H_{sys}(s)H_{load}(s) = \frac{-1*10^6}{s+1.25*10^5} * \frac{\frac{sL_1R_1}{R_1+sL_1}}{R_{sense}+\frac{sL_1R_1}{R_1+sL_1}} = \frac{-1*10^6}{s+1.25*10^5} * \frac{s\frac{L_1R_1}{L_1R_{sense}+L_1R_1}}{s+\frac{R_{sense}R_1}{L_1R_{sense}+L_1R_1}} \tag{4.45}$$

The transfer function of the voltage amplifier with the load of Figure 4.11b

$$H(s) = H_{sys}(s)H_{load}(s) = \frac{-1*10^6}{s+1.25*10^5} * \frac{R_1}{R_1+(sL+R_{sense})} = \frac{-1*10^6}{s+1.25*10^5} * \frac{\frac{R_1}{L_1}}{s+\frac{R_1+R_{sense}}{L_1}} \tag{4.46}$$

These transfer function will results in a change in the pole zero placement depicted in Figure 4.12a and 4.13a with the corresponding root locus in Figure 4.12b and 4.13b. Adding a resistor parallel to the inductor results in an extra zero. This has no influence on the stability and both systems can be considered stable.
To be able to control the system with the op amps it is adviced to not lower the value of the inductor below of 3 mH. This to decreases possible voltage spikes. This value guarantees a safe operating range.

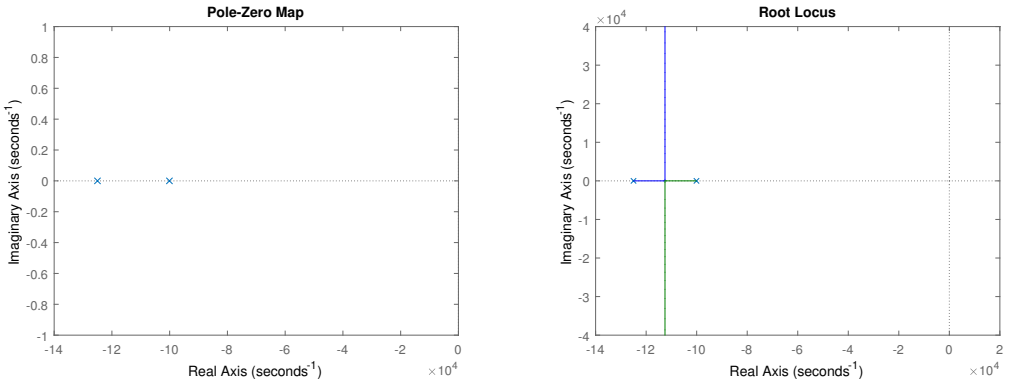


(a) Pole zero placement. (b) Corresponding root locus.

Figure 4.12: Stability of the voltage amplifier using an inductive load from Figure 4.11a (values R_{sense} = 80 $m\Omega$, R=100 Ω and L = 1 mH)

4.6. Final implementation

The overview of the voltage amplifier subsystem can be found in Appendix B.1. The Figure also incorporates the transconductance amplifier (Chapter 5) and the pre-filter (Chapter 6). The testing of the simulation and the results of the implementation are located in chapter 7.



(a) Pole zero placement.

(b) Corresponding root locus.

Figure 4.13: Stability of the voltage amplifier using an inductive load from Figure 4.11b (values R_{sense} = 80 $m\Omega$, R=100 Ω and L = 1 mH)

5

Design of Transconductance Amplifier

In this chapter the design of the transconductance amplifier is discussed. First the measurement method of the current is discussed. Followed by the elaboration of the difference in control system in comparison with the voltage amplifier. This is than followed by a system overview and the noise figures for the transconductance amplifier. Lastly the final implementation is shown.

5.1. Design

The design of the transconductance amplifier is similar to that of the voltage amplifier. The main difference between both systems is the way of measuring. Where by the VA the ouput voltage is measured, for the TA the voltage drop over a sense resistor is measured to determine the current flow.
In comparison to the Voltage amplifier, the transconductance amplifier must be way more precise. The following section will describe the proposed solution to the desired precision.

5.2. Current measurement

As stated in Requirement OC-2, the Pin Driver has 3 different current ranges with different levels of precision associated with them. These current ranges are repeated in Table 5.1.

Table 5.1: The different current ranges and the precision associated with these ranges.

Number:	Current Range (min.):	Current Range (max.):	Nice to Have- Precision	Must Have - Precision
1	-35 mA	35 mA	10 μA	50 μA
2	-350 mA	350 mA	100 μA	500 μA
3	-3500 mA	3500 mA	1000 μA	5000 μA

5.2.1. Current Sensing

The current sense resistor needs to work with a wide range of currents, the specifications say the maximum power dissipation in the current sense resistor is around one watt. Which means the maximum resistor value is determined by this power dissipation limit:

$$P_d = U * I = I^2 * R \rightarrow R = \frac{P_d}{I^2} = \frac{1}{3.5^2} \approx 80m\Omega \tag{5.1}$$

Which results in maximal burden voltage [11] of:

$$U = R * I = 80 * 10^{-3} * 4 = 320mV$$

Now by looking at the smallest current range, the voltage drop over the resistor can be determined and the smallest precision step for the lowest crrent mode can be determined.

$$R = \frac{U}{I} \rightarrow U = I * R = 35 * 10^{-3} * 80 * 10^{-3} = 0.0028V = 2.8mV \tag{5.2}$$

$$R = \frac{U}{I} \rightarrow U_{step} = I * R = 10 * 10^{-6} * 80 * 10^{-3} = 0.0008V = 0.8\mu V \tag{5.3}$$

The best of these opamps have voltage offsets in the order of 20 μV and offset drift of 0.1 µVK^{-1}. The smallest precision step, of 0.8 µV, is so small that instrumentation amplifiers would not be a solution that could work.

A solution is to switch the current sense resistor, as in Figure 5.1, however having switching mechanisms in the path of the current sense resistor is undesired, since this contributes to losses and switching mechanisms are not necessarily very precise resistors especially when the mechanism must also be able to handle up to 3.5 amperes. Another option is described by [12], this option removes the switch from the path by creating a resistor bank where the path is "taken" according to the mode selected, as can be seen in Figure 5.2a. When operating there is always only one path conducting, while the other two paths are not.

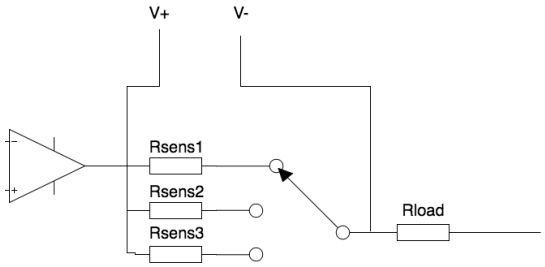
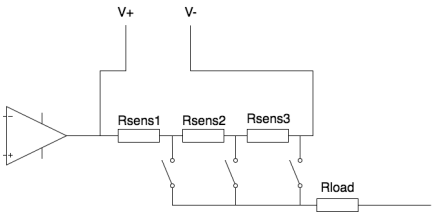
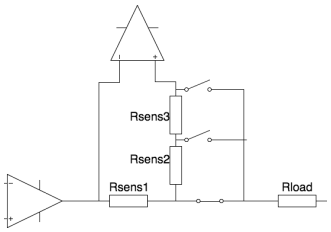


Figure 5.1: Switching between three resistor modes. The switch is in the measuring path.

The first resistor would be the smallest resistor, maximum of 80 mΩ, for the highest current mode as calculated in equation 5.1. The resistor values go up with a factor of 9 for the other modes to be able to use the same feedback loop for high current modes with a factor 10 increase. The first two resistors combined are the resistive value for the middle current mode, and all three resistors together are for the smallest mode. An example of such a mode is shown in Figure 5.2b. Giving the values of R_{sens1} of 80 mΩ, R_{sens2} of 720 mΩ and R_{sens3} of 7200 mΩ. Giving for each of the modes the following resistance values of; R_{mode1} of 80 mΩ, R_{mode2} of 800 mΩ and R_{mode3} of 8000 mΩ.



(a) Switching method using three resistors where the switch is not in the path of the second measure terminal (V-).



(b) Example of conducting path using the switching method.

Figure 5.2: The 3 switches method where the switch is not in the path

This is an implementation that removes the switching mechanism from the conducting path, while having the same voltage sense range in all different modes. However, the input resistance of the second terminal, V-, does change due to the other Sense resistors being part of the path. For R_{mode1} these are R_{sens2} and R_{sens3}, and for R_{mode2} this is R_{sens3}. An example of a mode can be seen in Figure 5.2b. However, an typical op amp has a input impedance in the order of GΩ. The two resistors combined total to a maximum of 8800 mΩ. Hence there is a difference in order of magnitude of 10^8, this difference is big enough to neglect their effects.

5.2.2. Voltage Range of input voltage

Since both the HMC and the system are able to drive a current, as described in Chapter 2, it is not possible to measure the current on the low side which means between the source and the ground. As seen in Figure

5.3a. So, high side current sensing is necessary as in Figure 5.3b. This implies there is a high common-mode voltage over the terminals of the op amp.

(a) Low side current sensing

(b) High side current sensing

Figure 5.3: Current Sensing methods

Divider

A problem that arises is with the common-mode voltage present. From research into the opamps there have been no instrumentation amplifiers found that support a common mode voltage that can range from -35 to +35 volt, most high range instrumentation amplifiers have a range of 15 volt bi-directional. To counter the Common-Mode Voltage multiple solutions are possible, one of these solutions is to "divide" the signal. As can be seen in figure 5.4.

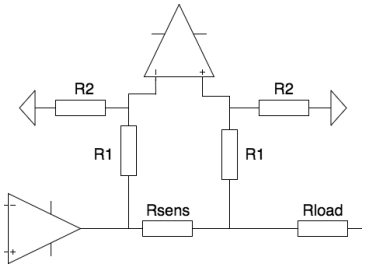


Figure 5.4: Instrumentation amplifier with divider. The Common-Mode Voltage is lowered by a factor R2/(R1+R2).

This division weakens the signal to such a level such that it fits the instrumentation amplifier's maximum Common-Mode Voltage. A division of 4 would be sufficient to fit the maximum common-mode voltage of the Op amp without further reducing the accuracy. For illustrative purposes, the smallest signal mode is used, with an resistor value of 8 Ω and a current in the -35 mA to 35 mA range with a desired precision of 10 μA. Over such a current sense resistor a step size of 10μA will lead to a voltage drop of:

$$U_{sens} = I * R = 10 * 10^{-6} * 8 = 80\mu V$$

This signal is then weakened by the factor of 4, which gives a measured voltage of 20 μV. Most instrumentation amplifiers have at least 25 μ V voltage offset, which is already higher than the input precision. Taking into account voltage offset on the output, which is Returned-To-Input:

$$V_{os_{RTI}} = V_{os_{in}} + V_{os_{out}}/G$$

Where G is the Gain factor of the instrumentation amplifier, the output offset will result into a bigger difference, which is obviously undesired. Another factor of influence is the Common-Mode Rejection Ratio, shortened to CMRR,which gives the influence on the output of the Common-Mode Voltage on the input of the amplifier. This is calculated as follows, as stated in [13] [14]. For illustrative calculations the AD8421BR [15] has been used with a 144 dB Common-Mode Rejection Ratio.

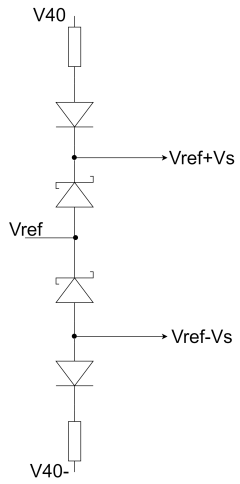
$$CMRR(dB) = 20log_{10}(\frac{\Delta V_{cm}}{\Delta V_{os}}) \rightarrow \Delta V_{os} = \Delta V_{cm} * 10^{\frac{-CMRR(dB)}{20}} \tag{5.4}$$

$$\Delta V_{os_{CMRR}} = 35 * 10^{\frac{-114}{20}} \approx 70 * 10^{-6} = 70\mu V \tag{5.5}$$

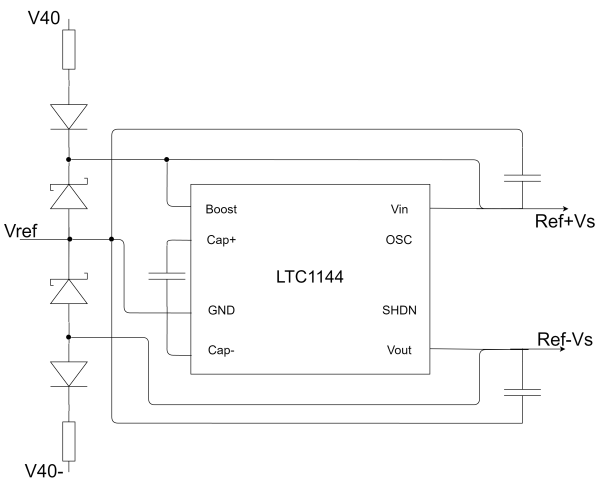
This also adds up to the measurement error, this influences the system to such an extend such that this option becomes unusable with the required precision.

Sense with a floating amplifier

Another option is provided by [12] and [16]. This solution tries to overcome the common mode voltage, by instead of weakening the signal to fit the maximum common-mode voltage. To let the amplifier float around the same level as in the input Commond-Mode Voltage, this is done by using a floating source and floating reference. Which can be seen in Figures 5.5a & 5.5b, where V_{ref} is the output voltage of the Pin Driver and used as reference voltage.



(a) Principle of floating supply



(b) floating supply with an active element

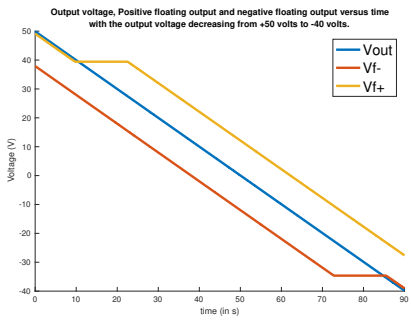
Figure 5.5: Floating supplies

The two Zener diodes around V_{out} are 16 volt zeners, while the two near the supply rails are regular diodes. Using these zener diodes, according to Vout the voltages Vf+ and Vf- are created. The voltage of V_{f+} and V_{f-} are:

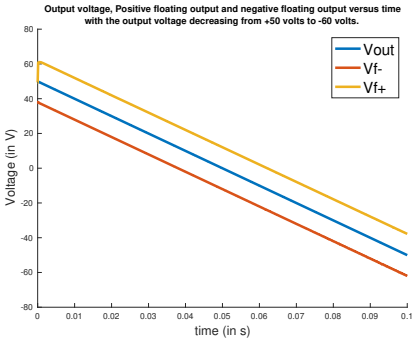
$$V_{f+} = V_{ref} + V_{zener} \text{ for } V_{f+} < V_{supply+}$$

$$V_{f-} = V_{ref} - V_{zener} \text{ for } |V_{f-}| < |V_{supply-}|$$

Where V_{zener} is the voltage drop over the zener diode in path. This basic system is in principle enough, however it has a "dead space" in which the voltage is no longer increasing. Because the source is no longer able to supply the desired voltage. This can be seen in Figure 5.6a. This is problematic since the system needs to work to at least 35 volts on the output, meaning a voltage of 51 volts must be created.



(a) Plot of Voltages of floating supply by using the circuit of Figure 5.5a. Where V+ is 40 volts, V- is -40 volts.



(b) Plot of Voltages of floating supply by using the circuit of Figure 5.5b. Where V+ is 40 volts, V- is -40 volts.

Figure 5.6: Plot of Voltages of floating supply without and with using the LTC1144.

To counter this dead zone the LTC1144 [17] is used, this is a voltage converter with a reference input. The voltage conversion works both ways, input referred or output referred. In combination with the capacitors to

gain energy from the reference the system is able to overcome the dead space as can be seen in Figure 5.6b.

This solution has the advantage of a small Common-Mode Voltage, which means the signal does not need to be weakened to fit the specifications of the amplifier such that the voltage drop precision of 80 µV can be completely used to full extend. As stated before the voltage offset is 25 μV, which is well within margin. With the divider circuit, the source has been taken as ideal. Such that it does not impose any problems. With the floating source, as implemented above there are fluctuations on the source output. This has to do with the switched-capacitor working of the floating source, as these peaks can be filtered out to some extend. However, these peaks are a trade off with settling time of the output of the floating source. The settling time will give a higher Common-Mode voltage in this period of time, while the fluctuations in the source will give difference due to the Power Supply Rejection Ratio (PSRR). The PSRR can be determined as follows [11], [18]:

$$PSRR(dB) = 20log_{10}(\frac{\Delta V_{supply}}{\Delta V_{out}}G) \rightarrow \Delta V_{out} = 10^{(\frac{-PSRR(dB)}{20})} * \Delta V_{supply} * G \tag{5.6}$$

Most instrumentation amplifiers have different PSRR values per input [19]. In the worst case scenario, these two differences will add up, giving the following formula. The used deviations are taken from simulations, using the LTC1144 [17]. The PSRR are from the AD8421BR [15].

$$\Delta V_{out} = \Delta V_{out_p} + \Delta V_{out_n}$$

$$\Delta V_{out} = 10^{(\frac{-PSRR(dB)}{20})} * \Delta V_{supply_p} * G + 10^{(\frac{-PSRR(dB)}{20})} * \Delta V_{supply_n} * G$$

$$\Delta V_{out} = 10^{-(55/20)} * 0.02 * 10 + 10^{(-90/20)} * 0.02 * 10 = 360\mu V$$

However, there are also some losses in the power supply which add up as well. These are in the order 0.01V for the negative supply and 0.1 for the positive supply. Which leads to a loss of x μV, totalling the ΔV_{out} to x μV. Which is rather high, however this is Referred to the Output. With the gain of 10 and an input precision of 80 μV, the output precision is at 800 μV. Which would fit the constraints.
This output is however still on a floating reference, using a second instrumentation amplifier this can be removed. The same implementation as in Figure 5.4 can be used. By dividing the signal by a factor of 4. The signal has a output precision of 200 μV, with the voltage offset in the order of 25 μV. This implementation would suffice the needed precision. The last option that has been discussed is also using a floating source and floating reference. The main difference between the implementations was the other implementation used galvanic separation. Which could help overcome possible ground loops [20]. However, due to time constraints this option has not been researched further on.

5.2.3. Implementation of Sensing Technique

Using the above described method, the set-up as in Figure 5.7 is created. The first stage, the amplifier stage, amplifies the signal with a factor 50. The factor 50 is near the maximum voltage that can be created with the amplifier since the supply voltage is ±16V over a burden voltage to amplify of 320 µV at 4 A. The second stage removes the common-mode voltage, and lowers the voltage down to the level of the input voltage of ± 5V. This is done with a ratio of 1 over 3.2 to create the combined gain factor of 15.625.

5.3. Control system

For the transconductance amplifier, the control system is just slightly different compared to the voltage amplifier as depicted in Figure 5.8. Since most of the calculations are the same as for the Voltage amplifier, the most important aspects are highlighted in this section. The precise calculation methods are done as in sections 4.1 & 4.2.

The control system depends of the sense resistor, R_s, which is different per mode and the resistance of the load for a resistive load. If the load is a complex load, this will influence the system. As stated in Section 3.1 the input is -5 to +5V. With a maximum Burden Voltage of 320 mV, to bring this burden voltage to the same level as the input an amplification of 15.625 is needed.

Using the formulas of Section 4.1, with B as gain factor of 15.625. The following transfer function for the system can be determined.

$$H(s) = \frac{-1/((R_i C_i)(R_s + R_l))}{s - B/((R_i C_i)(R_s + R_l))}, \text{ with } B = 15.625R_s \tag{5.7}$$

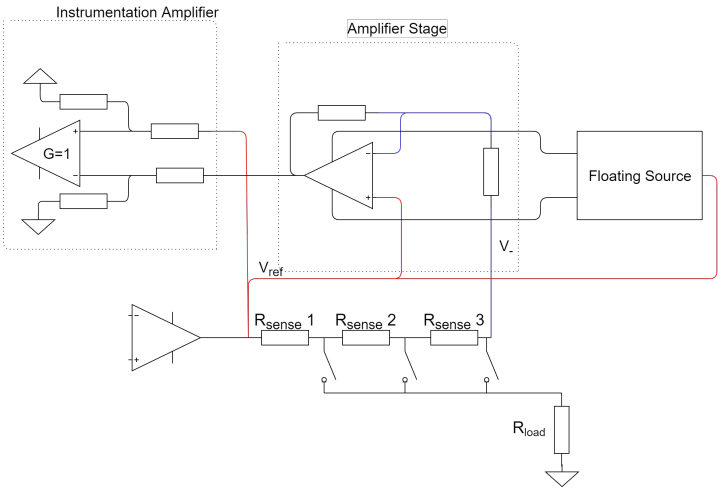


Figure 5.7: Circuit setup for the feedback loop of the transconductance amplifier

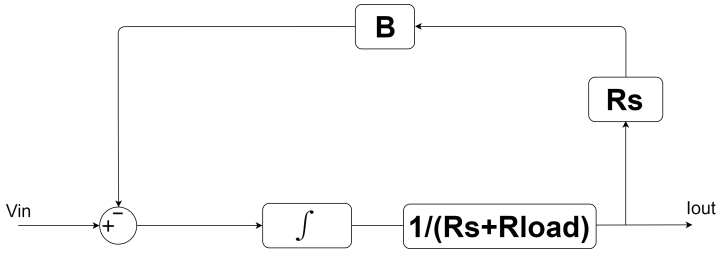


Figure 5.8: Feedback loop for Current Controlled Circuit. Where Rs represents the sense resistor in each different mode and Rload represent the the Load resistance.

Formulas 4.15 & 4.16 can be used to determine the rise - and settling time of the system. As both R_i and C_i are the same as for the voltage amplifier, these are 10 kΩ and 100 pF respectively.

$$t_r = \frac{2.2}{B/(R_i C_i)} = \frac{2.2 R_i C_i (R_s + R_l)}{15.625 R_s} = 140.8(1 + \frac{R_l}{R_s}) * 10^{-9} \tag{5.8}$$

$$t_s = \frac{4}{B/(R_i C_i)} = \frac{4 R_i C_i (R_s + R_l)}{15.625 R_s} = 256(1 + \frac{R_l}{R_s}) * 10^{-9} \tag{5.9}$$

Both the rise- and settling time depend on the value of the load, as the load size becomes greater the settling time increases. The cut-off frequency can be calculated using the following formula.

$$|H(j\omega)|^2 = 1/2 \tag{5.10}$$

As for the rise- and settling time the cut-off frequency also depends on the load of the system. When the rise- and settling time increase, the cut-off frequency and vice versa. The consequence of this is that the amount of noise at the output is dependent on the load size and type.

The minimum load is approximated at 0 ohms, the following characteristics are determined.

$$t_r = 140.8\text{ns}$$

$$t_s = 220\text{ns}$$

$$f_c = 1.55\text{MHz}$$

The maximum load is determined by the maximum settling time that is allowed, which is 100 µs, giving the following calculation.

$$\frac{R_l}{R_s} = \frac{3117}{8}$$

$$R_l = \frac{3117 R_s}{8}, \text{ with } R_s = 80, 800 \text{ or } 8000\text{m}\Omega \tag{5.11}$$

For every current mode, the maximum resistor value is different than for the other modes as in formula. At the maximum value, both the timings and cut-off frequency are the same for the different modes.

$$t_r = 55\mu\text{s}$$

$$t_s = 100\mu\text{s}$$

$$f_c = 6\text{kHz}$$

The most important observation is of course the big difference in settling time and the high variety of cut-off frequencies possible.

5.4. System Overview

5.4.1. Ideal system

The ideal system of the transconductance amplifier is depicted in Figure 5.9. This system is based on the components from Section 5.2 combined with the control system from Section 5.3. The output signal from the integrator will be a current which will flow to the switching network to the load.

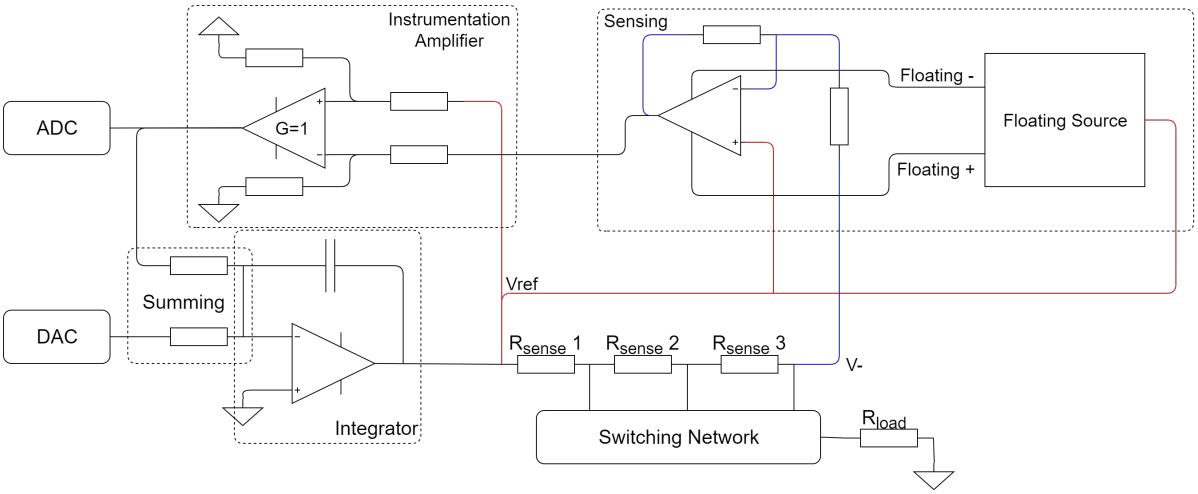


Figure 5.9: Overview of the ideal current system

5.4.2. Addition of System Elements

In this circuit some new elements are introduced, for the amplifier stage it is not possible to use the amplifier as for the Voltage amplifier, since the amplifier in this circuit needs to be able to deliver voltages up to 16 V.

Operational Amplifier

For the operational amplifier, the most important aspects that have been considered are the voltage offset and the noise density. As these parameters to a great extend influence the precision of the circuit. In Table 5.2 some of the choices are stated. There are only slight differences between the different opamps, the OPA189 looks to be the best pick with a much lower voltage offset and only a little higher voltage noise density. However, the OPA189 is still in the preview phase and the Spice was not yet working with the circuit design. Thus the LT1007 is used as this is the runner-up in the specifications.

Instrumentation amplifier

In Table 5.3 multiple optional instrumentation amplifiers are stated. The noise figure for the INA114 is the best of all the instrumentation amplifiers, however it has a large bias current and the highest voltage offset. The AD8421 has the best specifications in comparison to the others, as it has the lowest voltage offset, lowest bias current. Thus the AD8421 is used.

Table 5.2: List of operational amplifiers for amplifier stage - Datasheets are located in Appendix C

Name	offset voltage(μV)	$e_n(\frac{nV}{\sqrt{Hz}})$	$i_n(\frac{pA}{\sqrt{Hz}})$	Offset Drift µV°C^{-1}	supply voltage(+/-V)
LTC1151	5	23	-	0.1	18
LT1007	25	4	0.6	0.6	18
LT1012	25	13	0.01	0.6	18
OPA189	4.5	5.8	0.165	0.0035	18

Table 5.3: Different instrumentation amplifiers for the instrumentation amplifier stage - Datasheets are located in Appendix C

Name	input offset voltage(μV)	bias current (pA)	$e_{n-in}(\frac{nV}{\sqrt{Hz}})$	$i_n(\frac{pA}{\sqrt{Hz}})$	CMMR (dB)	Max. Output Voltage (in V)	supply voltage(+/-V)
AD8421	25	100	3.2	0.2	110	Vs-1.6	18
LT1167	40	350	12	0.124	90	Vs-1.3	18
INA114	50	2000	1.3	0.8	90	Vs-1.3	18
INA101	25	10000	13	0.35	115	Vs-2.5	18

5.5. Noise

Using the implementation discussed in Section 5.4, noise calculations are done on this system. The noise calculations are Return-to-Output, since the specs are also given in Return-to-Output relationship. The noise bandwidth is taken from 0.1 Hz to 100 kHz, the pin driver only drives an update once every millisecond. However, the ADC chosen has a much shorter sampling time. Which could pick up this higher frequency noise. The noise is calculated for the worst case scenario where the cut-off frequency is furthest away, as depicted in the previous section. Which gives an R_l of zero Ω. The noise sources described in the coming Sections are depicted in Figure 5.10. Also the smallest current mode is used, since the most noise influence is expected

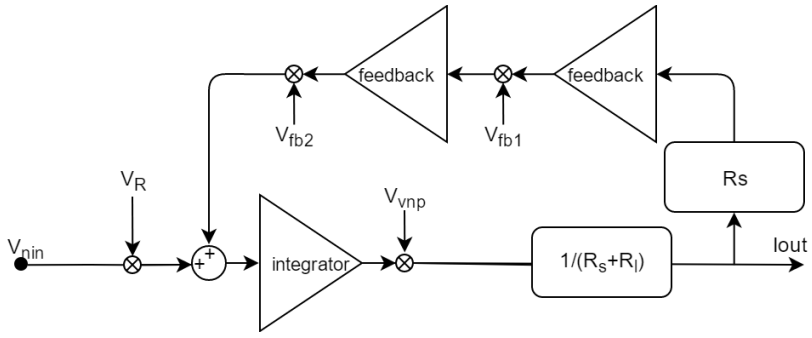


Figure 5.10: Noise sources and their positions in the transconductance amplifier.

5.5.1. Input Noise

As discussed in Section 4.4.1 the input noise from the Digital to Analog Converter to the output is determined. The difference between the voltage amplifier implementation and the transconductance implementation is the transfer function used. The transfer function for the transconductance amplifier is given in Equation 5.12.

$$H(s) = \frac{-1/((R_i C_i)(R_s + R_l))}{s - B/((R_i C_i)(R_s + R_l))}, \text{with } B = 15.625 R_s \tag{5.12}$$

Which gives:

$$|H(f)|^2 = \frac{1}{4\pi^2 f^2 R_i^2 C_i^2 (R_s + R_l)^2 + 15.625^2 R_s^2} \tag{5.13}$$

With R_l being zero and R_s being 8 Ω for the lowest current mode. The transfer function is simplified to:

$$|H(f)|^2 = \frac{1}{4\pi^2 f^2 R_i^2 C_i^2 8^2 + 15.625^2 8^2} = \frac{1}{256\pi^2 f^2 * 10^{-12} + 15625} \tag{5.14}$$

The rest of the calculations happen in the same way as in Equation 4.27, giving the value depicted in Equation 5.15.

$$\overline{I_n^2} = 5.21 * 10^{-12} \rightarrow \overline{I_n} = 2.28\mu A \tag{5.15}$$

5.5.2. Summing Resistors

Just as for the input noise, for the summing resistors only the transfer function changes. Giving the following noise figure:

$$\overline{I_R^2} = 5.76 * 10^{-17} \rightarrow \overline{I_R} = 7.59nA \tag{5.16}$$

5.5.3. Integrator noise

As for the integrator noise, the same calculations can be used as for the voltage amplifier. Only the transfer function from the integrator point is different, which can be found in Appendix A.3.

$$\overline{I_{vnp}^2} = 4.8 * 10^{-14} \rightarrow \overline{I_{vnp}} = 220nA \tag{5.17}$$

5.5.4. Noise from the feedback loop

The feedback consists of more elements than the feedback loop of the Voltage amplifier. It consists of a operational amplifier to amplify the signal with a factor of 50. Which is than followed by a instrumentation amplifier, where the signal is down-scaled with a factor of 3.2. As stated in Section 5.2.3.

First Stage

The noise of the first amplifier is given in Equation 5.18, the further calculations can be found in Appendix A.4.1.

$$\overline{I_{fb_1}^2} = 1.31 * 10^{-12} \tag{5.18}$$

Second Stage

The calculations for the second stage in the feedback loop are found in Appendix A.4.2. The calculated values are:

$$\overline{I_{fb_2}^2} = 2.32 * 10^{-18} \tag{5.19}$$

5.5.5. Output Noise

Combining all Return to Output noise sources as in Section 4.4.5 giving the following noise figure. By multiplying the noise figure by 6.8 the peak to peak output noise current can be determined which covers 99.94% of the peaks.

$$\begin{aligned}\overline{I_{out}^2} &= 5.21 * 10^{-12} + 5.76 * 10^{-17} + 4.8 * 10^{-14} + 1.31 * 10^{-12} + 2.32 * 10^{-18} \\ &= 6.56 * 10^{-12}\end{aligned} \tag{5.20}$$

$$\overline{I_{out}} = 2.56\mu A \rightarrow I_{pp} = 6.8 * \overline{I_{out}} = 17.41\mu A \tag{5.21}$$

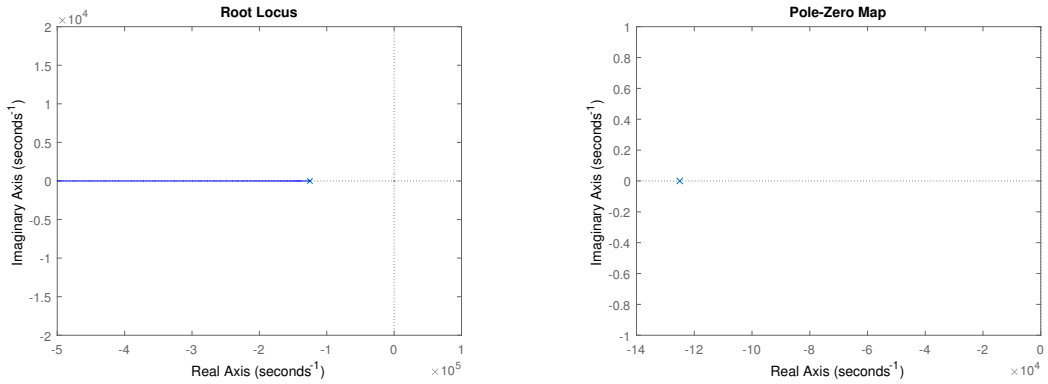
The output noise is more than desired, however is within margin of the criteria of 50 µA precision.

5.6. Stability

This section is focused on the stability of the transconductance amplifier using various loads. Using the same method as in Section 4.5 a estimation of the stability can be given. Using the transfer function from Equation 5.7 the pole zero placement is depicted in Figure 4.7a and the root locus in 4.7b.

5.6.1. Resistive load

Using a resistive load the transfer function pole shifts to the right if R_l increases and shift left if it decreases. Because R_l can not become negative the pole will stay in the left half plane. The system can therefore be considered stable in this situation.



(a) Root locus of the voltage amplifier

(b) Pole zero placement of the voltage amplifier

Figure 5.11: Stability of the voltage amplifier

5.6.2. Complex load

The capacitive load is at the transconducatance amplifier different from the voltage amplifier as it is based on the current flowing through the output. Instead of using the voltage over the load now the current through the load will be used in the equivalent of the load R_l.

Capacitive load

The loads shown in Figure 5.12 shows to tested capacative loads.

(a) Resistor in parallel with a capacitor.

(b) Resistor with a capacitor.

Figure 5.12: Schematic view of the Capacitive load types.

The equivalent R_l for Figure 5.12a is

$$R_l = R_{sense} + \frac{R_1 \frac{1}{sC_1}}{R_1 + \frac{1}{sC_1}} = R_{sense} + \frac{\frac{1}{C_1}}{s + \frac{1}{R_1 C_1}} \tag{5.22}$$

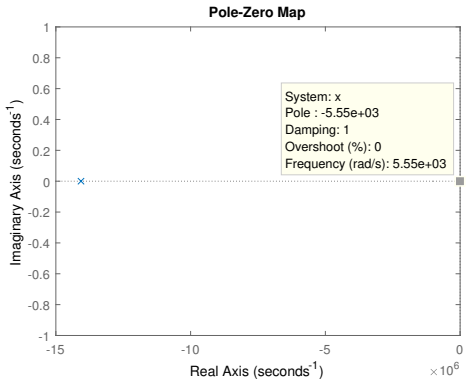
For Figure 5.12a this results in

$$H(s) = \frac{-1/((R_i C_i)(R_s + R_{sense} + \frac{\frac{1}{C_1}}{s + \frac{1}{R_1 C_1}}))}{s + 15.625 R_s/((R_i C_i)(R_s + R_{sense} + \frac{\frac{1}{C_1}}{s + \frac{1}{R_1 C_1}}))} \tag{5.23}$$

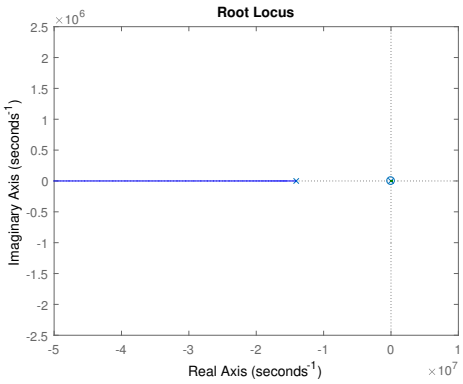
Using Matlab the pole zero map has been plotted in Figure 5.13a with the root locus in Figure 5.13b. The system shows two poles and a zero. Both of these poles are far in the left plane. Therefore the transconductance amplifier stays stable under this kind of load.

For Figure 5.12b

$$R_l = R_{sense} + \frac{1}{sC_1} \tag{5.24}$$



(a) Root locus of the transconductance amplifier.



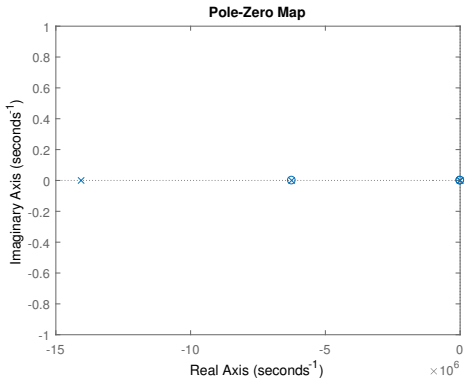
(b) Pole zero placement of the transconductance amplifier.

Figure 5.13: Stability of the transconductance amplifier using a capacitive load from Figure 5.12a (values R_{sense} = 80 $m\Omega$, R=100 Ω and C = 1 μF).

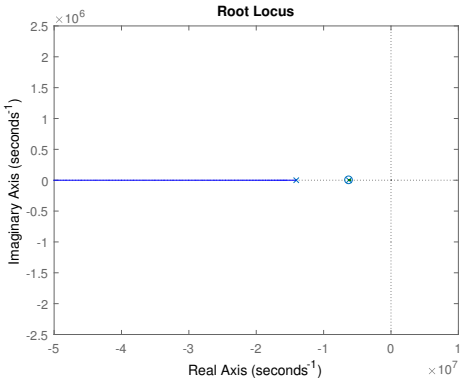
For Figure 5.12b this results in

$$H(s) = \frac{-1/((R_i C_i)(R_s + R_{sense} + \frac{1}{sC_1}))}{s + 15.625 R_s/((R_i C_i)(R_s + R_{sense} + \frac{1}{sC_1}))} \tag{5.25}$$

Using Matlab the pole zero map has been plotted in Figure 5.14a with the root locus in Figure 5.14b. Using only a capacitor the system quickly disrupts. This having the reason no current can flow through the capacitor. It is not advised to use this load with the transconductanse amplifier.



(a) Root locus of the transconductance amplifier.

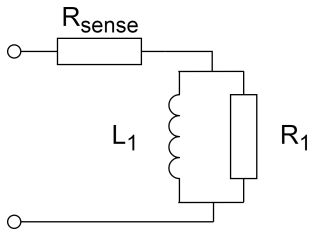


(b) Pole zero placement of the transconductance amplifier.

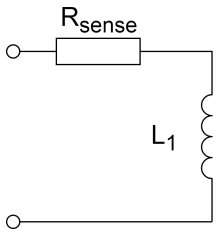
Figure 5.14: Stability of the transconductance amplifier using a capacitive load from Figure 5.12b. (values R_{sense} = 80 $m\Omega$, R=100 Ω and C = 1 μF)

Inductive Load

The loads shown in Figure 5.15 shows to tested inductive loads.



(a) Resistor in parallel with a inductor.



(b) Resistor with a Inductor.

Figure 5.15: Schematic view of the Inductive load types.

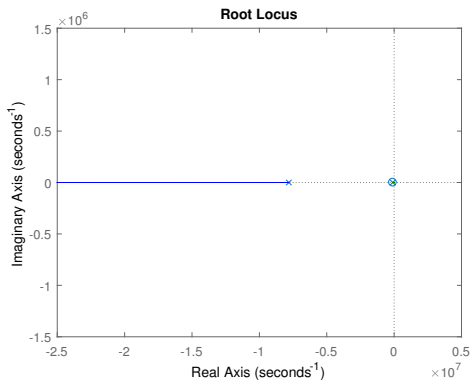
The same as with the capacitive loads the equivalent R_l changes due the type of load attached. For Figure 5.15a

$$R_l = R_{sense} + \frac{R_1}{s + \frac{R_1}{L_1}} \tag{5.26}$$

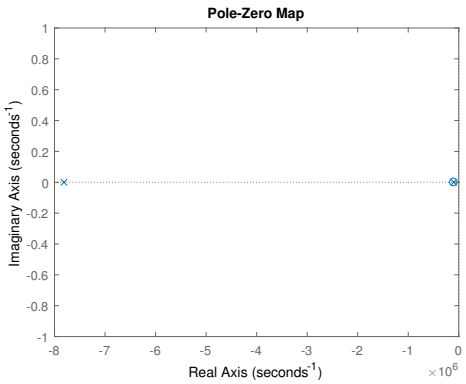
This results in

$$H(s) = \frac{-1/((R_i C_i)(R_s + R_{sense} + \frac{R_1}{s+\frac{R_1}{L_1}}))}{s + 15.625R_s/((R_i C_i)(R_s + R_{sense} + \frac{R_1}{s+\frac{R_1}{L_1}}))} \tag{5.27}$$

Using Matlab the pole zero map has been plotted in Figure 5.16a with the root locus in Figure 5.16b. As seen in the Figure poles are both far in the left plane. Therefore the system is considered stable. It is advised to use a resistor value of R = 10 $k\Omega$ and a inductor values around L = 10 mH.



(a) Root locus of the transconductance amplifier.



(b) Pole zero placement of the transconductance amplifier.

Figure 5.16: Stability of the transconductance amplifier using a Inductive load from Figure 5.15a (values R_{sense} = 80 $m\Omega$, R=100 Ω and L = 1 mH).

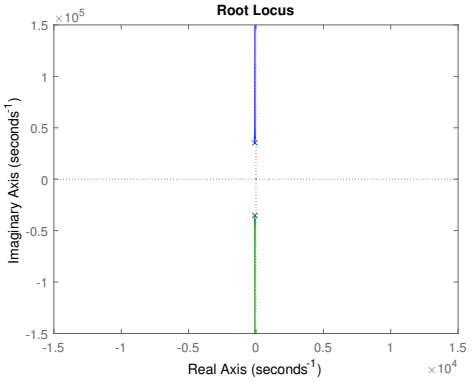
And for Figure 5.15b

$$R_l = R_{sense} + sL_1 \tag{5.28}$$

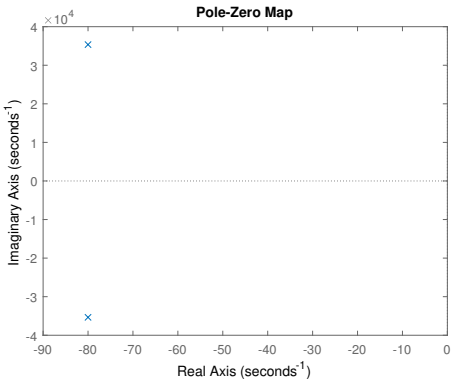
This results for Figure 5.15b in

$$H(s) = \frac{-1/((R_i C_i)(R_s + R_{sense} + sL_1))}{s + 15.625R_s/((R_i C_i)(R_s + R_{sense} + sL_1))} \tag{5.29}$$

Using Matlab the pole zero map has been plotted in Figure 5.17a with the root locus in Figure 5.17b. These figures show that the system is unstable. The system starts to oscillate and is therefore advised not to add a inductor directly to the transconductance amplifier.



(a) Root locus of the transconductance amplifier.



(b) Pole zero placement of the transconductance amplifier.

Figure 5.17: Stability of the transconductance amplifier using a Inductive load from Figure 5.15b (values R_{sense} = 80 $m\Omega$, R=100 Ω and L = 1 mH).

5.7. Final Implementation

The LTspice model of the transconductance amplifier can be found in appendix B.2. The Figure also incorporates the voltage amplifier (Chapter 4) and the pre-filter (Chapter 6). The test results can be found in Chapter 7.

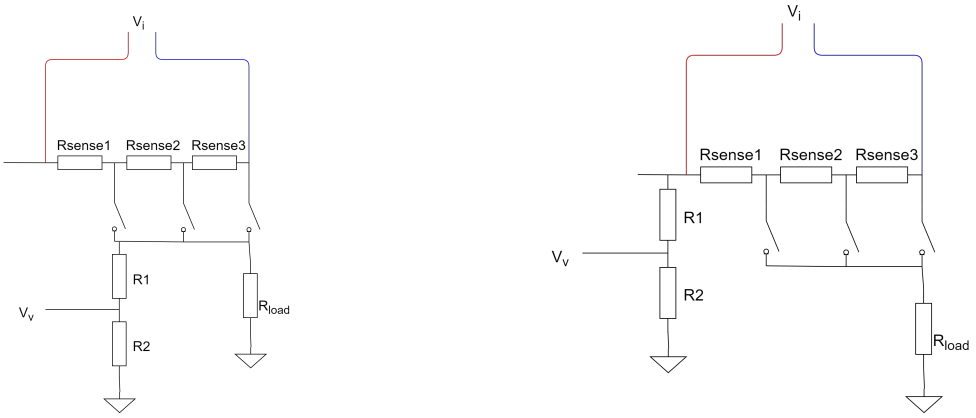
6

Merging of subsystems

In this chapter the two subsystems, the voltage amplifier and transconductance amplifier, are merged to create the Pin Driver. To merge the subsystems a consideration on precision needs to be made. Followed by a method to increase precision, by decreasing noise. Also a safe manner of switching needs to be defined, thus all signals controlling the Pin Driver are discussed and a protocol is defined to be able to switch between the different output modes.

6.1. Measure Positions

In an ideal situation the two different modes and measuring paths would not influence each other and can be seen as two completely different systems as in Figure 3.5. However, in an actual setup they cannot be seen as separate. For the measurement of a current, a sense resistor is needed. While for measuring a voltage, a measerument point must be made where a small current is flowing. Since both of the measuring paths influence each other, there is a choice to which one needs to be measured first. Two setups are possible, measuring the current and then the voltage, or vice versa. The options are depicted in Figure 6.1a and Figure 6.1b.



(a) Possible measuring setup, where the current is measured before the voltage is measured.

(b) Possible measuring setup, where the voltage is measured before the current is measured.

Figure 6.1: Possible measuring setups

In the first situation, Figure 6.1a, the current is measured before the voltage is measured. The error that arises from this measurement system is in the current. This error is due to the current needed to measure the voltage. As discussed in Section 4.2.1 the resistors R1 and R2 are 700 kΩ and 100 kΩ respectively. As the maximum voltage is 40V, the maximum current loss is 50 µA. This could be problematic for the lowest current mode, where a precision of 10 µA is desired. However, since the voltage is measured as well, compensation for this error is possible.

The second option, Figure 6.1b, the voltage is measured before the current. The error in this method is in the voltage measurement. The burden voltage and the switches are in the path to the output. The burden voltage is up to 320 mV over the sense resistor. This does not include the voltage drop over the switch, as switches may differ in resistive value and are not necessarily constant a more intensive voltage drop may be present. Just as for the current deviation as in the first situation, the burden voltage can be compensated for since the current is measured. However, the voltage drop over the switch cannot be compensated for.
As discussed the voltage drop over the switches cannot be compensated for and the voltage drop over the current resistor is much bigger than the current loss in the voltage measurement path. Therefore the first option, as Figure 6.1a, is used.

6.2. Pre-Filter

As discussed in Section 4.4 & 5.5 in both implementations the noise of the Digital-to-Analog Converter is a major noise source, since this is amplified throughout the whole circuit. For the transconductance amplifier, the noise bandwidth even depends on the size of the load. The noise can be reduced by using a filter between the output of the DAC and the input of the pin driver unit. The transfer function of the pre-filter would be as in Equation 6.1 and can be cascaded in front of the sytem as in Figure 6.2 and Equation 6.2.

$$C(s) = \frac{\frac{-R_{f_{pre}}}{R_{b_{pre}}}}{sR_{f_{pre}}C_{f_{pre}} + 1} \tag{6.1}$$

$$H(s) = H_1 H_2 = C\frac{A}{1 + AB} \tag{6.2}$$

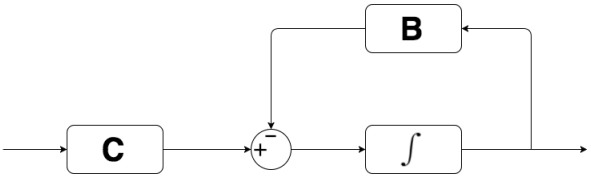


Figure 6.2: Control system with cascaded filter in front of system.

The calculations to determine the noise figure can be found in Appendix A.5.

For the current mode, while using a pre-filter the output noise is decreased up to 1.6 µA. However, the question is whether the system is still stable. The same tests as in Section 4.5 and Section 5.6 have been performed and the system is still stable. There is a small change in settling time, however the change is so small such that it is negligible.

6.3. Mode switching

On several positions in the PDU, switches and relays are applied to be able to control the output state. These choice of location and method are discussed in Section 6.3.1. The mode switching protocol is discussed in Section 6.3.2.

6.3.1. Lay-out

The overview of the switching positions is depicted in Figure 6.3. The placement of the switches are as follows.

1. Control feedback mode signal

   - Function: Controls whether the PDU is a voltage or transconductance amplifier
   - Type: A reed relay

   A reed relay is used to switch between the feedback loop. The choice of a reed relay is due to lower power consumption and noise, therefore having a smaller influence on the signal. [21] [11] A reed relay can in this circuit function properly, since the currents flowing through the feedback loop are small. The reason a single pole double throw (spdt) is picked over two single pole single throw (spst) is this implementation will guarantee one of the feedback networks is always connected.

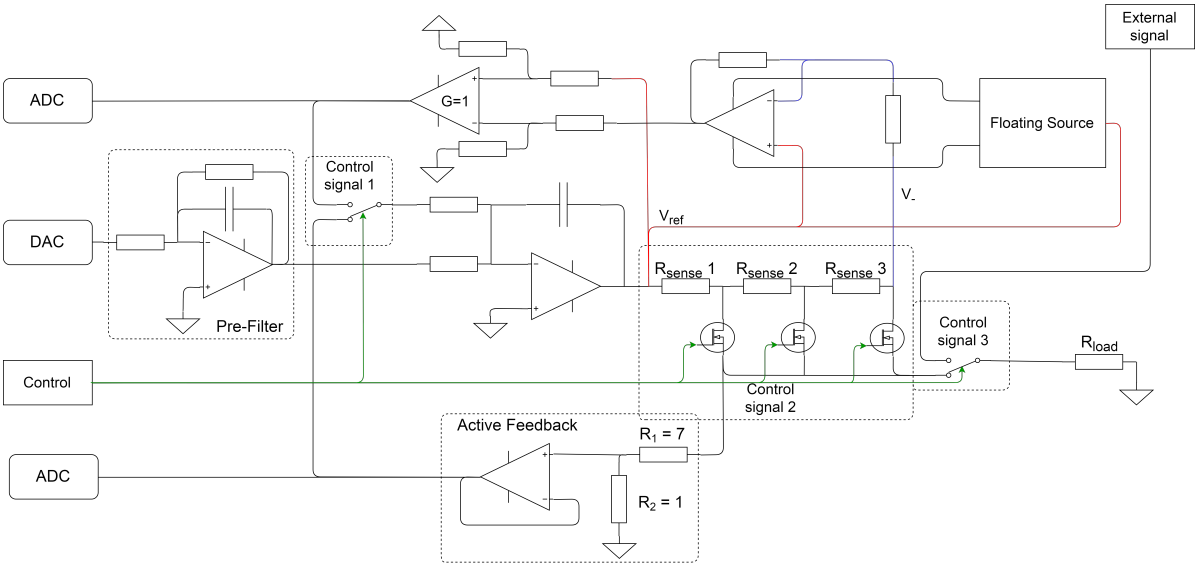


Figure 6.3: Complete layout of the PDU with switching locations, a pre-filter and measuring position.

2. Control measurement signal

   - Function: Controls the measurement range of the sense resistors
   - Type: Power MOSFET

   These power MOSFETs are positioned after the sense resistors to set the measurement range. At all times only one of these switches is closed. The reason why Power MOSFETs are used is due to their low input resistance, size, price and being able to handle the ± 3.5 A output. An overview of some possible power MOSFETs is shown in Table 6.1. The CSD18536KTT power MOSFET is picked for it's low resistance. The reason the other MOSFETs are not chosen even if they have lower resistance is because they failed to stay within the Safe Operating Area

Table 6.1: Overview MOSFET selection.

Name	Type	$R_{DS}(m\Omega)$	V_{DS}
CSD18510Q5B	Power MOSFET	0.96	40
CSD18536KTT	Power MOSFET	1.6	60
IRL7472L1	Power MOSFET	0.59	40
IPT007N06N	Power MOSFET	0.75	60

3. External signal control

   - Function: Controls which source is used as output (external or PDU)
   - Type: Solid State Relay (SSR)

   The external signal should not be influenced by the PDU output signal and vice versa, to prevent this isolation is required. At position 3 a Solid State Relay (SSR) is positioned to keep the signals galvanic isolated. A SSR is preferred over reed relay, because a SSR can handle the high current.

6.3.2. Protocol

This switching of the relays and switches can not be realised instantaneous. A protocol can prevent possible damage from occurring. The steps of the protocol of the PDU can be seen in Figure 6.4. Since the switching behaviour is allowed to be much slower than 1 ms (Requirement F-1) it is possible to first set the output to zero and then switch system loops.

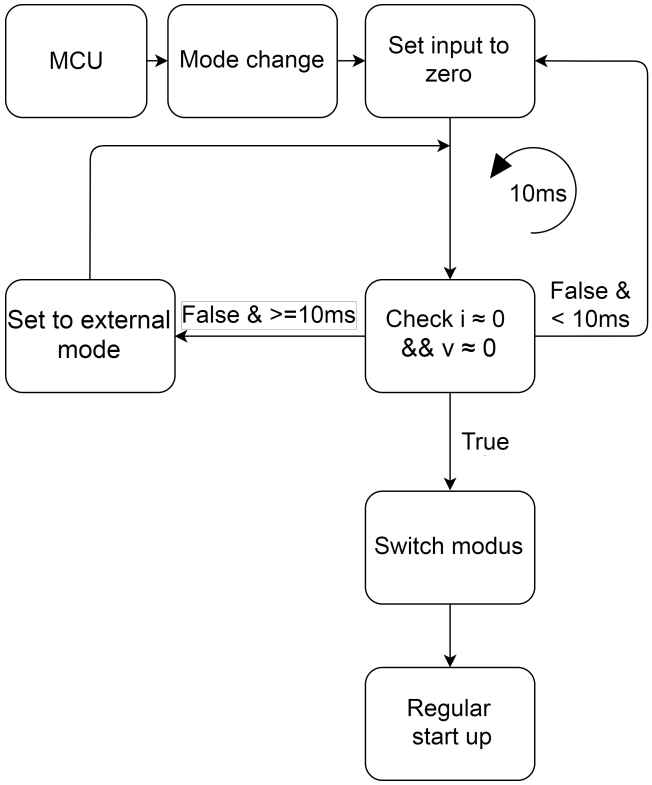


Figure 6.4: System Overview

As seen in Figure 6.4 the loop starts when the MCU wants to change a mode. At every mode change the input will be set to zero. Through the ADC the MCU knows when the output voltage and current are approximately zero. When both current and voltage approximate zero the switching of modes can start. If this is not true the system checks, for a period of 10ms, continuously if the current or voltage drops to zero. If after 10ms the current or voltage is still not approximately zero one of the switches will be set to external mode. The reason why this is implemented because the HMC can also provide a current. This loop continues until the voltage and current are zero. When they are both at zero the MCU will set the switches to the desired position.

7

Testing Methods and Results

This chapter describes how the requirements of the pin driver are tested and the tests that are performed in the form of simulations in LTSpice to check whether the requirements are met.

7.1. Output Modes

Requirements FO-1 and FO-2 state that the system must be able to behave like a voltage amplifier or as a transconductance amplifier. This is tested during the tests for the other requirements. Section 7.2.2 proofs the working of both output modes. The switching time between modes, Requirement F-1, is not proven by these simulations since the testing requires an actual pin driver with an Micro Controller Unit assembled where the protocol described in Section 6.3.2 is running.

7.2. Settling Time

7.2.1. Method

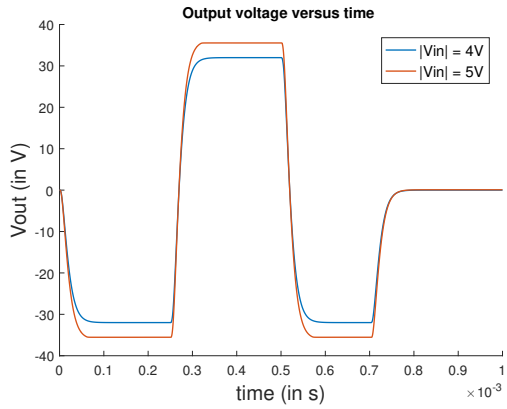
As described in Requirement O-1 the settling time of the Pin Driver Unit, has a nice to have settling time of 10 µs and a must have settling time of 100 µs. This requirement needs to be sufficed for both the Voltage Amplifier and the transconductance amplifier. A test is done with a purely resistive load on both subsystems where the input goes from the negative maximum to the positive maximum value. As the settling time of the transconductance amplifier mode depends on the size of the load this is also checked with the biggest load possible as defined in Equation 5.11.

7.2.2. Results

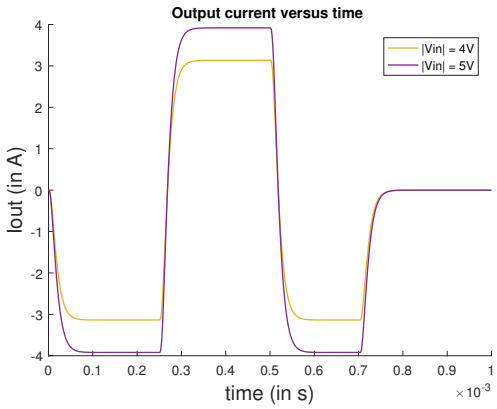
Figure 7.1a shows the voltage swing of the output in voltage mode, when the input is negative, than switched to positive and after that turned off. The input voltages plotted in this figure are 4 and 5 V. The load connected is 10Ω, which has the same settling time as the voltage amplifier for both the calculation and simulation.
The settling time for the voltage amplifier from the negative maximum to the positive maximum is 70 µs, where from calculations 64 µs was expected. This difference is due to the slew rate of the input step and slew rates of the operational amplifiers.
Figure 7.1b shows the current swing of the output in transconductance amplifier. From calculations 65 µs was expected, whilbe from simulations 72 µs is shown. which seems to due to the same effects as for the voltage amplifier.

7.3. Maximum ratings

The maximum ratings for both the voltage Requirement OV-1 and OC-1 are proven when the settling times are checked. Since the system is than driven to the maximum voltage and current possible. Thus these requirements do not need further testing.
For the voltage amplifier the maximum output voltage is 35.6 V, which is more than the 35 V. Thus the requirement is met.
For the transconductance amplifier the maximum output current is 3.93 A. Input values that try to create an output current bigger than 3.93 A, the system becomes uncontrollable and saturates to maximum output



(a) Maximum rating test for the voltage amplifier, showing the input from most negative to most positive value and vice versa. The settling time does not depend on the voltage to drive.



(b) Maximum rating test for the transconductance amplifier, showing the input from most negative stable value to most positive value stable value and vice versa. The settling time does not depend on the current to drive.

Figure 7.1: Maximum rating output test for both the voltage amplifier and the transconductance amplifier.

current. In an actual setup, this could be overcome by using the overcurrent pin of the OPA541. Using this method a maximum current can be set on the operational amplifier itself.

7.4. Precision

7.4.1. Method

The precision for the voltage amplifier and the transconductance amplifier are stated in Requirements OV-2 and OC-2 respectively. Multiple aspects affect the voltage or current precision on the output. These consist of noise, non-linearity, offset and the step size of the Digital-to-Analog Converter. Since these results are base on simulations it is possible to run a noise simulation within LtSpice. For the linearity and offset, all possible input values are tested. Where the offset can be found from. The DAC step size is already determined in Section 3.1.1.

7.4.2. Results

Noise

Since some of the opamp models are not a good representation of their actual noise figures or do not have a noise figure at all. The noise figures calculated are used for the results. For the Voltage amplifier the peak-peak noise voltage found is:

$$V_{pp} = 0.884\text{mV}$$

For the transconductance amplifier the noise is given by:

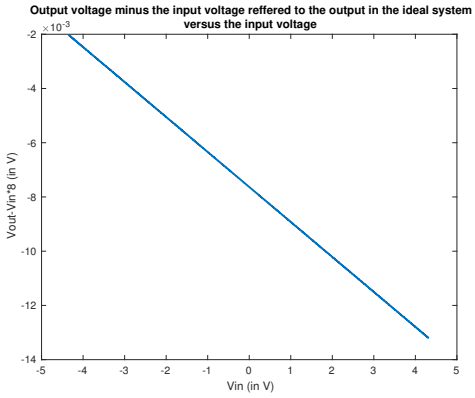
$$I_{pp} = 13.6\mu\text{A}$$

Offset and Non-linearity

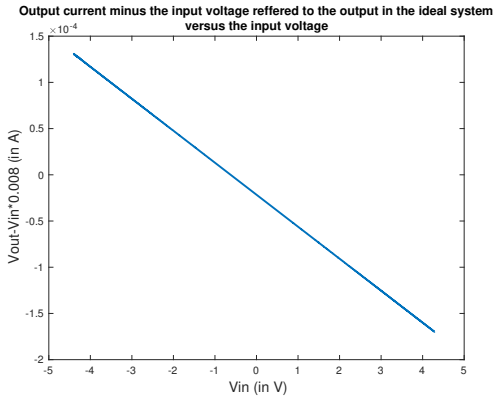
To check the non-linearity of the Pin Driver, a slowly increasing input from -5 to +5V has been created. By scaling the voltage or current on the output down to the input range. The difference between the input and the output can be determined. The results can be found in Figure 7.2a-d.
Multiple parameters influence the outcome of this experiment, the precision loss due to the gain resistor and operational amplifier input. This is not compensated for and is seen as part of the non-linearity of the pin driver.
For the transconductance amplifier, leakage currents are also not accounted for and are not taken into consideration and are seen as part of the non-linearity.
One of the most important influences on the output is the delay, it takes a moment for the pin driver to get to a certain value. No compensation has been done to correct this.

The following list describes the offset and non-linearity per mode to the maximum value with respect to the voltage offset.

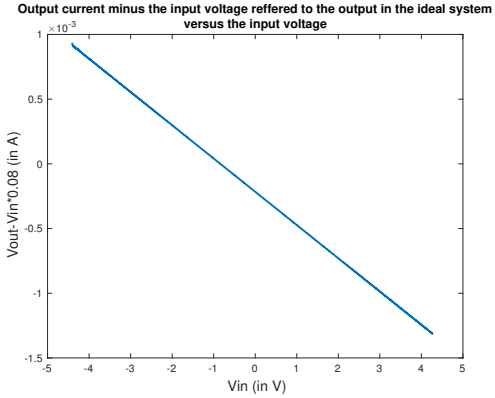
- Voltage Amplifier:
  - Offset: 7 mV
  - Non-Linearity: ± 6 mV
- Transconductance Amplifier (40 mA):
  - Offset: -20 µA
  - Non-Linearity: ± 150 µA
- Transconductance Amplifier (400 mA):
  - Offset: -215 µA
  - Non-Linearity: ± 1.1 mA
- Transconductance Amplifier (4000 mA):
  - Offset: -2.1 mA
  - Non-Linearity: ± 9 mA



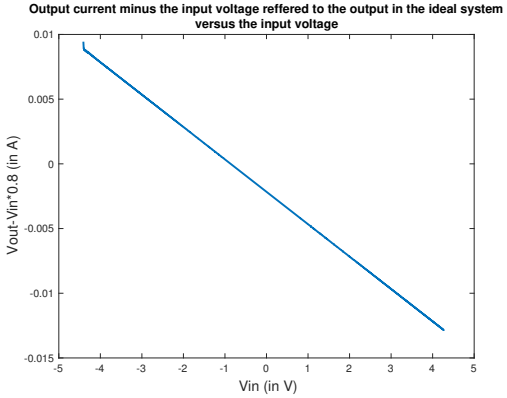
(a) Voltage output minus the input voltage referred to the output versus the input voltage which is indepedent of the current mode chosen.



(b) Current output minus the input voltage referred to the output versus the input voltage for the 40mA mode.



(c) Current output minus the input voltage referred to the output versus the input voltage for the 400mA mode.



(d) Current output minus the input voltage referred to the output versus the input voltage for the 4000mA mode.

Figure 7.2: Non-linearity for all different modes.

Combination of the precision influencers

To conclude on the level of precision, the different imperfections are summed to determine what the maximum possible error is. This incorporates the maximum voltage, maximum current and noise based on a load with creates the most noise within the pin driver (R_l of 0 Ω). For the voltage amplifier the maximum would be:

$$V_{out_{err}} = V_{noise} + V_{os} + V_{n-lin} = 0.844 + 7 + 6 = 13.884\text{mV}$$

The maximum error is 1.3 times the desired output precision and thus does not suffice the wanted precision of 10 mV (Requirement OV-2). However, as the voltage offset is constant. This could be compensated for. Which would bring, in the best case, the error down to 6.844 mV.

For the current modes the maximum output error is given as follows. The noise current for the 400 and 4000 mA mode is approximated at 10 and 100 times the noise for the 40 mA mode. Maximum output error of 40 mA mode:

$$I_{out_{err}} = I_{noise} + I_{os} + I_{n-lin} = 13.6 + 20 + 150 = 183.6\mu\text{A}$$

Maximum output error of 400 mA mode:

$$I_{out_{err}} = I_{noise} + I_{os} + I_{n-lin} = 136 + 215 + 1100 = 1451\mu\text{A}$$

Maximum output error of 4000 mA mode:

$$I_{out_{err}} = I_{noise} + I_{os} + I_{n-lin} = 1360 + 2100 + 9000 = 12.46\text{mA}$$

The precision requirement, Requirement OC-2, is not met. As can be seen, the remaining error current is spaced around the voltage offset linearly. This non-linearity in the system introduces the most error to the output.
The lowest current mode receives the most impact from this error. One of the explanations for is the influence of the current loss due to the voltage amplifier.
A second observation that has been made is that this non-linearity to a great extend depends on the output voltage. The error current increases as the output voltage increases.
The noise for the 400 and 4000 mA mode is now calculate as 10 and 100 times the noise of the 40 mA. This is higher than expected in a actual setup, since not all noise sources are dependent on the mode the system is in.
Because the non-linearity is so evenly spaced, compensating for it is a possibility. Which could reduce the error significantly.

7.5. Load

7.5.1. Method

Requirement O-2 states that at least resistive loads need to be driven. In the following situation it would also be nice to be able to drive inductive and capacitive loads. By connecting several types of loads and by setting pulses through the input. The working with these types of loads are tested.

7.5.2. Results

Resistive Load

The working with a resistive load is checked during the test for the settling time the results of these tests can be found in Section 7.2.2. To conclude, the system is able to drive a resistive load.

Capacitive Load

For a capacitive load, a simular simulation as in Section 7.2.2 has been run and also the Phase Margin is determined. For the Voltage Amplifier, the system is stable for a capacity smaller than 10 µF, using a capacitor of 10 µF will have a Phase Margin of 44 degrees.
Using the transconductance amplifier, for all loads the pin driver is stable. However, to maintain a certain current the voltage level needs to increase. This load will work until the voltage saturates, after which the system will get unstable.
With an resistor in parallel for the transconductance amplifier, the system is stable for capacitive values less than 1 µF in combination with a resistor of at least 2 Ω.

Inductive Load

For an inductive load, also a simular simulation as the simulation in Section 7.2.2 has been done. Also the Phase margin is determined.

With the voltage amplifier a purely inductive load is connected, all possible inductor values are stable. However, as the current has to increase to maintain a certain voltage. This solution is bounded by the time it takes to get to the maximum output current.
For the transconductance amplifier, the inductive load needs to be at least 10 μF in parallel with a resistance of 5 Ω.

7.6. Input Signals

The Requirements concerning the input signals, the signals coming from and going to the MCU. Requirements I-1, I-2 and I-3 have been taken into account. The DAC and ADC use SPI as a communication method and the control signals are in place to control the Pin Driver Unit. So by design these requirements are met.

7.7. External Signal

The Requirements concerning the external signal, namely Requirements FO-3, OE-1, FM-4 and OE-2, are solved and do not require testing in a simulation system. In an actual setup it is possible to test the working for these requirements.

7.8. Summary

To summarise the last Requirements are used, Requirement T-1 and T-2. Within the set conditions the pin driver is able to set its output every millisecond. The values can be measured and send back to the MCU with a precision as required. With these building blocks it is possible to create a system which is modular where every Pin Driver can be switched out for one another.

7.9. Actual Setup

7.9.1. Testing plan

In this section the testing method for an actual setup is discussed. The requirements are incorporated in the test plan. **Step one:** Check for all different modes if the system is capable to work on a non-edge case value with a resistive load.

Step two: Drive the system for (all different possible) values in the different modes using a signal generator with an resistive load, measure the output at the ADC and at the load to determine what kind of offsets or errors there are present in the system.
The settling time of the system can also be determined if both the input signal and output signal are presented on an oscilloscope (or another way to compare the data). Use these measurements at the output also to determine the noise figure on the output (using an oscilloscope).

Step three: Drive the system for (all different possible) values in the different modes using the DAC with an resistive load, measure the output at the ADC and at the load to determine what kind of offsets or errors there are present in the system.
Use these measurements at the output also to determine the noise figure on the output (using an oscilloscope). If there is much difference between Step two and Step three. The additional test could be run.

Step four: Drive the system (all different possible) values in the different modes using the DAC with an inductive load, measure the output at the ADC and at the load to determine what kind of offsets or errors there are present in the system and if they increase/decrease if the inductive load is changed.

Step five: Use an output of the HMC or likewise which is current controlled and drive the voltage on the pin driver side to check whether the system will still function properly and deliver desired values.

Additional possible tests: Test the quality of the Digital-to-Analog Converter. The following criteria could be tested; amount of noise introduced, stability of output, settling time. Upon this the choice could be made to use another DAC (as long as no final PCB has been made).

7.9.2. Results

Unfortunately no test setup has been made upon the writing of this thesis. This has led to no actual setup test results. However as previously discussed there is a functional test plan made for the pin driver module. Also some recommendations are made upon expected results (in accordance with the simulation test results), these recommendations are located in Section 8.2.

8

Evaluation

In this chapter the conclusions according to the results will be discussed. Which is followed by the Recommendations for the pin driver and its implementation.

8.1. Conclusion

The overall goal of the project, as stated in chapter 1, is to design a simulation system that is able to mimic a hydraulic plant. A great amount of the total system is not part of the scope of this thesis and can be found in [1], [2]. The scope of this thesis is limited by the hardware side of the pin driver. According to the requirements made for the overall system and specifically for this hardware component conclusions will be drawn.
Most conclusions are not hard because no actual pin driver has been build and the tests that have been done are simulations.
The overall pin driver requirement is to create a modular pin driver which is versatile and should be able to be replaced for one another. While some of the requirements have not been met to the maximum the baseline has been met and the design and architecture do work and are a good setup for further development.

8.1.1. Requirements

Some of the requirements are met by design, others apply only to an actual setup pin driver. In this Section, the most important requirements which in simulations can be verified are highlighted.

Requirements OV: The Pin Driver needed to be able to drive a voltage range of -35V to +35V with a precision of 10 mV. This requirement is not met, the total output precision is 13 mV. However, using some of the recommendations it is expected that the voltage will be in range.

Requirements OC: The Pin Driver needed to be able to drive a current range of -4 to +4A with a different precision per range as given in Table 2.1. This requirement is not met due to the large non-linearity present in the system. This non-linearity is not is linear over the input voltage, thus is is expected that effect could be mitigated.

Requirement O-1: The settling time of the system, is as long as the load does not slow the system too much, within the must-have of 100 µs.

Requirement O-2: The pin driver is able to drive resistive loads, while for capacitive the capacitive value should be lower than 10 µF and for inductive loads above 10 µH

8.2. Recommendations

In accordance with the conclusions drawn in the previous section the following recommendations are presented.

8.2.1. Non-linearity

As the non-linearity of the system has the biggest influence on the output current, but also has a regularity in growth. It could be implemented in the Micro Controller Unit to compensate for the error possible. Such a correction formula would be as:

$$v_{cor} = i_{os}/G + i_{nlin} * V_{out}$$

Where i_{os} is the offset current (in µA), G is the Gain of the transconductance amplifier (in VA^{-1}), i_{nlin} is the non-linearity compensation in (in AV^{-1}) and V_{out} is the output voltage (in V).

8.2.2. Leakage current correction

As discussed in Section 6.1 a leakage current of up to 50 µA at 40 volt could be present. This current is a problem especially for the smallest current mode. This leakage current is dependent on the output voltage. Since the output voltage is measured, compensation for this current is possible.
A solution would be to do start-up tests, where the current is measured in the voltage amplifier mode with no load connected. All current measured is than only used by the divider resistors of the voltage amplifier. A list of current values could be made which than could be linearized over the full range. This would minimise the influence of the leakage current.
However, if the voltage fluctuates to a great extend. It is hard to have a compensation that is fast enough.
A second option would be to increase the resistor value, however this would influence the gain of the voltage amplifier to a great extend such that this solution is undesired.

8.2.3. Gain correction

As briefly discussed in Section 4.2.1 and 6.1, the higher the value of the divider resistors. The smaller the leakage current is and the bigger the gain error is. As stated, the gain is given by the following formula.

$$G = \frac{R_2}{R_1 + R_2 + R_1 R_2 / R_{opamp}}$$

The gain error depends on the value of the resistors and on the input resistance of the buffer. One of the solutions to mimimize the gain error is to use a very high input impedance operational amplifier.
A second solution would be to use smaller resistors at the compromise of leakage current, this could be done when the solution provided in the previous section is implemented in such a good quality that the increase of leakage current does not influenced.

8.2.4. Lowering bandwidth

Within the simulation there is margin to further reduce the bandwidth of the pin driver, to lower the noise even further. Such that noise figure on the output becomes smaller, however this is only a effective measure for the transconductance amplifier. Such that it might meet the nice to have precision of 10 µA. On the other hand this sacrifices bandwidth and could also sacrifice the band of possible capacitive or inductive loads.

8.2.5. Unbuffered DAC

Most unbuffered digital-to-analog converters have lower noise figures than the buffered versions, this is due to the extra buffering stage present. Simulations could be run, where it could be tested if a Unbuffered DAC with a external buffer would have a lower noise figure. This could also decrease output noise.

A

Noise Calculations

A.1. Integrator in Voltage Amplfier

As briefly discussed in Chapter 4, only one noise source is specified for the OPA541, the voltage noise spectral density. According to [9]. The amplification factor within the integrator is determined. This is:

$$|H_{int}(f)|^2 = 1 + \frac{1}{4 * \pi^2 f^2 R_i^2 C_i^2} \tag{A.1}$$

This noise source is return-to-output. As this has a different "entry point" in the system than the regular input, another transfer function applies. This transfer function is described below:

$$H_{intout}(s) = \frac{1}{1 - 1/(8sR_iC_i)} \rightarrow |H_{intout}(f)|^2 = \frac{1}{1 + 1/(256 * \pi^2 * f^2 R_i^2 C_i^2)} \tag{A.2}$$

By multiplying these transfer functions and integrate over the voltage spectral density. The output voltage of this noise source is determined as in Equation4.37.

A.2. Feedback Loop in Voltage Amplifier

In the feedback loop, two noise sources are present. The noise from the operational amplifier and the noise from the resistors. The resistor noise is determined according to their resistive value. The first resistor, Resistor R_1 of 700 kΩ is amplified by the gain factor. While the second resistor, R_2 is used as an imput voltage of the operational amplifier. These together form the output noise of the resistors.

$$\overline{V_R^2} = \overline{V_{R1}^2} + \overline{V_{R2}^2} \tag{A.3}$$

The noise from the operational amplifier itself is calculated using [9]. Both input terminals have an equivalent noise current density, as stated in [22] , while the equivalent noise voltage density is only calculated over the positive input of the operational amplifier. For both the current densities, the Return to Output path is determined as in the [9] page 13-14.

Again a different transfer function from this point in the system is determined, this transfer function is as in the following Equation.

$$H_{fbout}(s) = \frac{1}{(sR_iC_i) - 8} \rightarrow |H_{fbout}(f)|^2 = \frac{1}{4 * \pi^2 * f^2 R_i^2 C_i^2 - 64} \tag{A.4}$$

The calculated values are as in Equation 4.38 and 4.39.

A.3. Integrator in Transconductance Amplifier

The same calculations apply as in Appendix A.1, the only difference again is the transfer function. Which is depicted below.

$$|H_{int}(f)|^2 = \frac{1}{1 + \frac{15.625^2}{4\pi^2 f^2 R_i^2 C_i^2}} \tag{A.5}$$

A.4. Feedback loop in the Transconductance Amplifier

A.4.1. First Stage

As discussed in Section 5.5.4. The first stage amplifies the signal by a factor of 50, this is done using the LT1007. Just as with the feedback for the Voltage Amplifier, the noise consists of noise from the resistors and noise from the operational amplifier itself. This is again done using [9], with these noise sources calculated another transfer function needs to be determined from this point in the system. Giving the following transfer function:

$$H_{fb1}(s) = \frac{1/(3.2sR_iC_iR_s)}{1+\frac{50}{3.2sR_iC_i}} \tag{A.6}$$

The rest of the calculation is the same as described in Section 4.4.

A.4.2. Second stage

For the second stage, the same principles apply. Again both Resistor noise and opamp noise are present and are determined using [9]. The gain of the second stage is 1 over 3.2. The noise from the opamp itself is stated in the datasheet according to the corresponding gain factor. The transfer function associated with these noise sources is as follows.

$$H_{fb2}(s) = \frac{1/(sR_iC_iR_s)}{1+\frac{15.625}{sR_iC_i}} \tag{A.7}$$

A.5. Pre-filter

As in Section 4.4.1, the noise density of the Digital-to-Analog Converter is given.

$$v_n = \begin{cases} 300\text{nVHz}^{-1/2}, & \text{for } 0.1 < \text{f} < 10 \text{ Hz.} \\ 60\text{nVHz}^{-1/2}, & \text{for } 10 < \text{f} < 10000 \text{ Hz.} \\ 110\text{nVHz}^{-1/2}, & \text{for } 10000 < \text{f} < 100000 \text{ Hz.} \end{cases} \tag{A.8}$$

The low pass filter is designed as in Figure A.1. Which the transfer function as in Equation 6.1. The resistors R_f and R_b have the same value, to not further change the output. C_f is chosen the same as C_i to not extensively impact the settling time of the system.

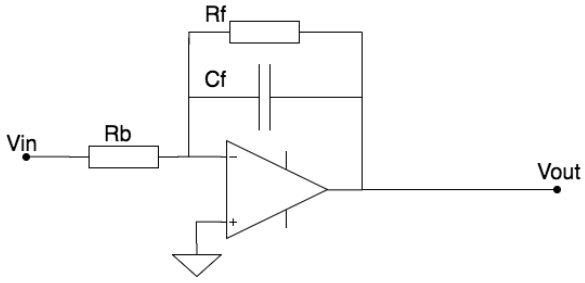


Figure A.1: Low pass filter used for filtering the DAC-output

The first step is to check whether a filter would even help. In the circumstances without an input filter the noise contributed by the input is 0.13 mV for the voltage amplifier and 2.15 µA for the Transconductance Amplifier.

In the situation with a pre filter, the calculation would be as in the following Equation where H(f) has the pre-filter integrated.

$$\overline{V_n^2} = \int_{0.1}^{100000} v_n^2 |H(f)|^2 df \tag{A.9}$$

For the voltage mode the output voltage noise would be:

$$\overline{V_n^2} = 8.47\mu\text{V} \tag{A.10}$$

For the current mode the output current noise would be:

$$\overline{I_n^2} = 67.80\text{nA} \tag{A.11}$$

At first glance it seems like a good option to use a pre-filter to further damp the noise of the DAC. However, this does not take the noise of the operational amplifier in to account. These noise sources are calculated separately and summed to form an output noise source. As the noise is most important for the transconductance amplifier, only for this amplifier the noise is calculated. The steps are calculated as in [9], the same operational amplifier as for the voltage amplifier, TLC2654, is used.

$$\overline{I_n^2} = 1.66 * 10^{-14} + 2.53 * 10^{-14} + 1.36 * 10^{-13} = 1.78 * 10^{-13} \tag{A.12}$$

$$\overline{I_n} = 0.42\mu\text{A} \tag{A.13}$$

The noise in the situation without a pre-filter was 2.15 µA, after the pre-filter the noise totals to 0.43 µA referred to the output. This is a decrease of 1.6 µA

B

Scheme

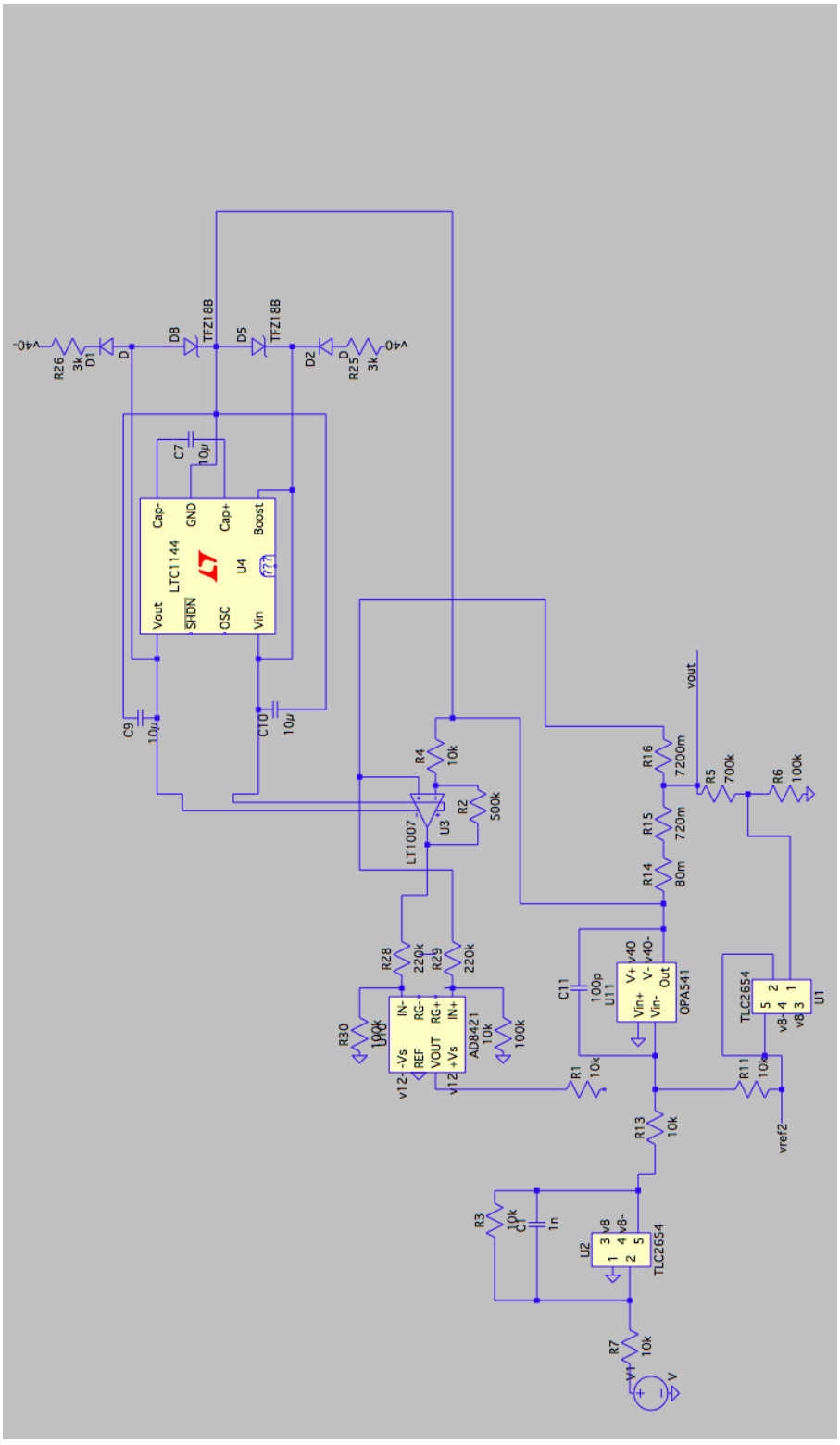


Figure B.1: LTspice model of the Pin driver in voltage amplifier mode.

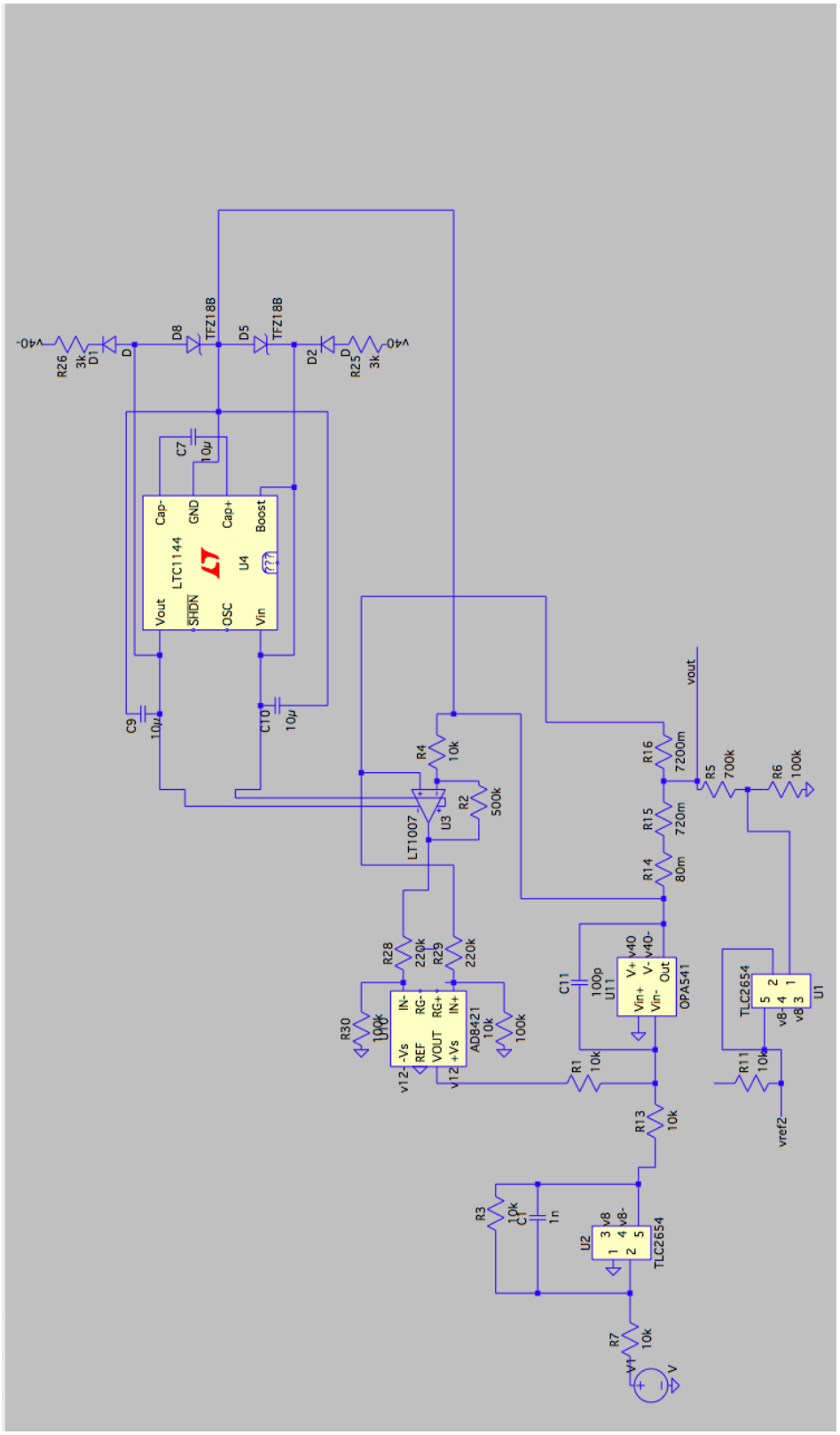


Figure B.2: LTspice model of the Pin driver in transconductance amplifier mode.

C

Datasheets

In this appendix all datasheets are located which are referenced in the tables:

DAC:

DAC714: http://www.ti.com/lit/ds/symlink/dac714.pdf
DAC8734: http://www.ti.com/lit/ds/symlink/dac8734.pdf
DAC8871:http://www.ti.com/lit/ds/symlink/dac8871.pdf
DAC8831: http://www.ti.com/lit/ds/symlink/dac8831.pdf DAC8832: http://www.ti.com/lit/ds/symlink/dac8832.pdf
DAC7734: http://www.ti.com/lit/ds/symlink/dac7734.pdf
DAC7731: http://www.ti.com/lit/ds/symlink/dac7731.pdf
AD5760: http://www.analog.com/media/en/technical-documentation/data-sheets/AD5760.pdf
AD5781: http://www.analog.com/media/en/technical-documentation/data-sheets/AD5781.pdf
LT2642: http://cds.linear.com/docs/en/datasheet/26412fd.pdf

ADC:

LTC1419: http://cds.linear.com/docs/en/datasheet/1419fb.pdf
LTC1855: http://cds.linear.com/docs/en/datasheet/185456fa.pdf
LTC1859: http://cds.linear.com/docs/en/datasheet/185789fb.pdf
LTC2328: http://cds.linear.com/docs/en/datasheet/232818fb.pdf
AD7606: http://www.analog.com/media/en/technical-documentation/data-sheets/AD7606_7606-6_7606-4.pdf

Power Opamp:

OPA541: http://www.ti.com/lit/ds/symlink/opa541.pdf
OPA549: http://www.ti.com/lit/ds/symlink/opa549.pdf
OPA2541: http://www.ti.com/lit/ds/symlink/opa2541.pdf
LM675: http://www.ti.com/lit/ds/symlink/lm675.pdf
OPA544: http://www.ti.com/lit/ds/symlink/opa544.pdf
OPA2544: http://www.ti.com/lit/ds/symlink/opa2544.pdf
APEX PA61: https://www.apexanalog.com/resources/products/pa61u.pdf

Opamp buffer and filter:

TLC2654: http://www.ti.com/lit/ds/symlink/tlc2654a.pdf
OPA192: http://www.ti.com/lit/ds/symlink/opa192.pdf
AD8597: http://www.analog.com/media/en/technical-documentation/data-sheets/AD8597_8599.pdf
LMH6624: http://www.ti.com/lit/ds/symlink/lmh6626.pdf
OPA211: http://www.ti.com/lit/ds/symlink/opa211.pdf
ICL7652: http://www.ti.com/lit/ds/slos046/slos046.pdf
LT1028: http://cds.linear.com/docs/en/datasheet/1028fd.pdf

Instrumentation amplifiers:
AD8421: http://www.analog.com/media/en/technical-documentation/data-sheets/AD8421.pdf
LTC1167: http://cds.linear.com/docs/en/datasheet/1167fc.pdf
INA114: http://www.ti.com/lit/ds/symlink/ina114.pdf
INA101: http://www.ti.com/lit/ds/sbos133/sbos133.pdf

Power MOSFET:
CSD18510Q5B: http://www.ti.com/lit/ds/symlink/csd18510q5b.pdf
CSD18536KTT: http://www.ti.com/lit/ds/symlink/csd18536ktt.pdf
IRL7472L1:https://www.infineon.com/dgdl/Infineon-IRL7472L1-DS-v02_00-EN.pdf?fileId=5546d46254e133b
IPT007N06N: https://www.infineon.com/dgdl/Infineon-IPT007N06N-DS-v02_01-en.pdf?fileId=
db3a30433e9d5d11013e9e4618320118

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