Combined Virtual Prototyping and Reliability Testing Based Design Rules for Stacked Die System in Packages

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Abstract

Since the last 2-4 years, the focus in microelectronics is gradually changing from front-end to packaging. More added values are put into packages, where System in Packages (SiP) is an answer for the ongoing function integration trend. In SiP several dies are placed into one package, either side-by-side or on top of each other. The miniaturization trend more or less forbids placing dies side-by-side, since it will make the package larger. Several stacking die concepts exist, in this paper we have investigated two different ones: silicon spacer versus ball spacer. In the silicon-spacer concept, a thin piece of silicon is used to separate the actives dies in the stack. In the glue-spacer concept this is accomplished with a filler-filled die-attach. Virtual prototyping techniques are used to explore the stress/strain hotspots for different package types, being QFN, BGA, QFP, and LQFP using both stacking concepts. It is found that the QFN package type has the highest stress levels compared to BGA and QFP. Optimization techniques are used to explore the design space of the worst-case package type. For example, it is found that the spacer thickness should be equal or thinner than the die stacked on top of it to prevent the occurrence of die crack. Standard qualification experiments on specific worst-case design will be conducted in future to verify the calculated responses. By combining virtual prototyping techniques with smartly chosen reliability tests allows that possible failure mechanisms within stacked die SiP packages to be better understood and thus prevented.

1. Introduction

Packaging has evolved during the last 3 decades, starting with 2 pins transistors (TO) in the late 1960s, wire bonding technologies in the mid 1970s, surface mount technologies (SMT) in the 1980s, and Flip Chip (FC) technologies in the 1990s. To replace the wire bonding technology, per today, the major technology trend for microelectronic packages is focused on function integration. Function integration into one package is covered by the development of the System in Package (SiP) in which several dies are placed into one package. Figure 1 indicates the packaging development trend over the years. As years have progressed, the number of package styles exploded rather than evolved. In an evolving mode, package styles are replaced but this is not the case: old package styles like SDIP are still manufactured and sold at rather high volumes. Instead, new package styles are continuously added to the market and SiP is one of the latest.

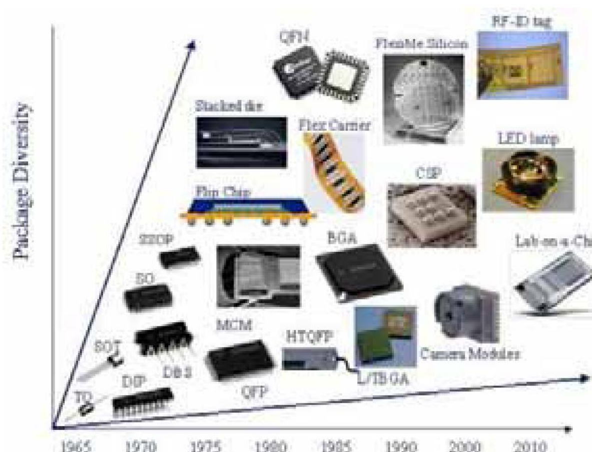

Figure 1: Packaging development trend.

The technical feasibility and unique potential of SiP offer better performance due to reduced interconnect length and power consumption, smaller form factor, higher device density, integration of devices from heterogeneous substrates, and the capability to process different functional entities on different wafers, in different fabs and by different manufacturers; opening new possibilities for future devices. The focus now lies on innovative manufacturing and integration schemes, which meet both economic and technical demands. Vertical chip stacking can be performed as chip-to-chip, chip-to-wafer, or wafer-to-wafer processes. Even though the fundamental principles of SiPs and single die packages are similar, the range of applications requires a variety of different manufacturing processes. Besides this, SiP introduction leads to increased chances and consequences of failures, increased design complexity, dramatically decreased design margins and increased difficulty to meet quality, robustness, and reliability requirements. This paper highlights our major research and development results for state-of-the-art virtual prototyping and virtual reliability qualification of SiP with stacked die technology. Thermo-mechanical reliability issues have been identified as major bottlenecks in the development of future microelectronic components [1]. In this paper, we focus on the virtual thermo-mechanical prototyping and qualification ranking for different packaging families, including QFN, BGA, QFP, and LQFP. Combined with a specific experimental matrix, the results of our research project are used to predict, qualify, and optimize the

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thermo-mechanical behavior of the SiP package reliability, against the actual requirements prior to major physical prototyping, manufacturing investments and reliability qualification tests.

2. Stacking Dies

Two stacked die concepts are evaluated, being silicon-spacer and glue-spacer. In the silicon-spacer concept, a thin piece of silicon is used to separate the active dies in the stack. In the glue-spacer concept this is accomplished with a filler-filled die-attach. Figure 2 shows schematically both stacking concepts for two dies. Of course, both concepts can be used for stacking more dies as well. Introducing stacks of such a stiff material, Silicon, into the package increases the bending resistance. Associated with that is the increased risk and/or vulnerability for cracks during assembly and/or reliability testing, either in the package body (moulding compound) or in the die itself. Figure 3 gives examples of such failures. Important design issues to prevent these failures in stacked SiP are:

- What properties are optimal for the ball spacer material?
- What thickness is optimal for the silicon spacer?
- What is the maximum overhang of the daughter die?
- What are the limits of both concepts, in terms of number of dies to be stacked?
- Which package family is more suited, which one less [2]?

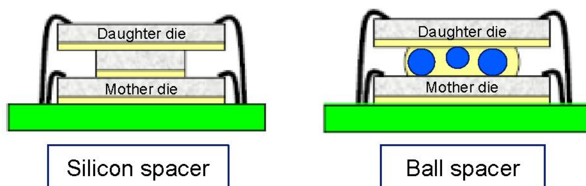

Figure 2: Investigated stacking concepts.

Figure 3: Fractures within package body (left) and silicon (right).

3. Finite Element Modeling

Parametric models are developed to obtain 'package stress/strain hotspots' using the state-of-the-art virtual prototyping / qualification techniques. FE models are constructed for both stacking concepts in QFN, BGA, QFP, and LQFP packages, see Figure 4 for examples. The nonlinear FE models include isotropy for silicon, visco-elasticity for moulding compound and die-attach, elasto-plasticity for copper, and orthotropic visco-elasticitity for FR4 [3]. Calculated response are moisture intake, package warpage, die stress values, and interface stress levels as a concequence of the thermal and hygro-swelling changes during manufacturing and testing. We have used the 'wetness' approach [4, 5, 6], which assumes continuity of the weighted moisture concentration across interfaces of different materials. The wetness is defined as $W = C/C_{sat}$. Using the wetness approach, the moisture diffusion implementation in commercial available FE software codes becomes straightforward with the help of appropriate user subroutines. All the appropriate materials (moulding compound, substrate, die-attach) have been characterized with regard to their moisture behavior under MSL conditions. It is assumed that the moisture uptake in the polymer materials can be described with Fick's Law of diffusion. Note that for different package families there are different material types.

The prediction models for the different package types are combined with advanced simulation-based optimization methods, such as sequence DOE and stochastic RSM techniques, to evaluate the design space of the different concepts [7, 8].

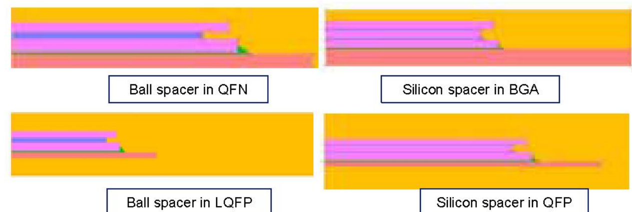

Figure 4: Example parametric models of different package types.

4. Results

Looking at the calculated stress/strain responses, the FE results identify the hotspots for the different stacking concepts. These hotspots are:

1. Package warpage
2. Die-crack for mother, daughter, and spacer die
3. Die-to-spacer delamination
4. Die-to-compound delamination
5. Compound-to-frame delamination
6. Body crack

Figure 5 shows the moisture concentration after MSL1 conditions for a QFN package and compares the silicon and ball spacer concept. Clearly, the package is not fully saturated after MSL1. This in contrast to a single die QFN, which will be fully saturated after MSL1. The moisture gradients are input for the further hygro-thermo-mechanical stress calculations.

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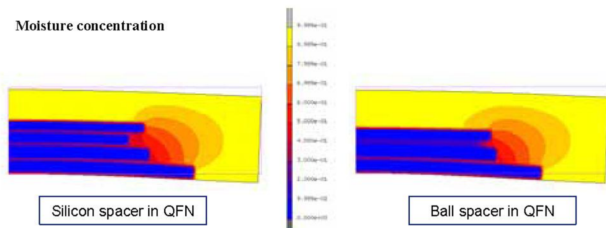

Figure 5: Moisture concentration comparing both stacking concepts in QFN.

Figure 6 shows a typical result of stress responses. The figure shows the maximum stresses in the dies for the silicon spacer concept in QFN. Hotspots in terms of stresses can be found at the center of the daughter and spacer die as well as the point where the daughter dies hang over the spacer. These points are used in the optimisation part.

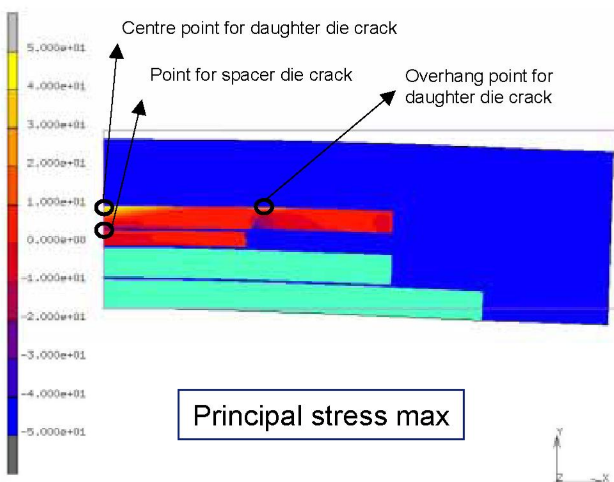

Figure 6: Stress response for the silicon spacer concept in QFN.

Comparing the different package styles the stress response can be totally different. Figure 7 shows the deformed structure for the silicon spacer concept for QFN and BGA. In a BGA, the stiffness of the substrate is about 15GPa, which is a bit lower than the one for the compound, approximately 20GPa at 25degC. In the QFN package, the frame is made of copper, with a typical stiffness of 123GPa, which is close to values for Silicon. As a consequence of another stiffness distribution in the package, the resulting deformations are totally different, as Figure 7 shows. In QFN, the frame is able to pull the stack above, but in BGA, it is the compound that opens the stack. This has significant implications for the reliability, in terms of outer design boundaries, for the stacking concepts.

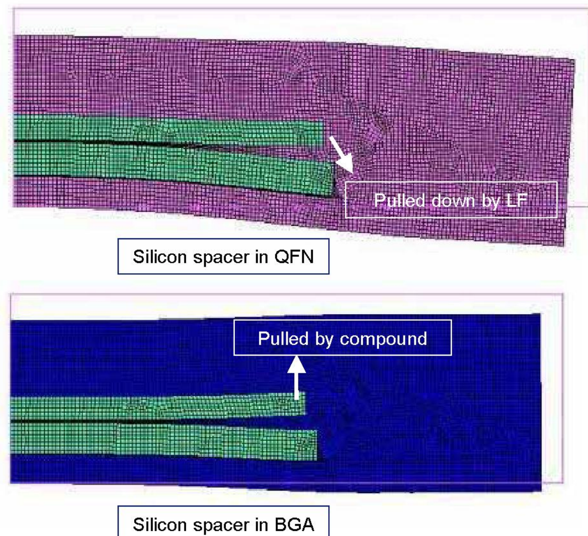

Figure 7: Deformed structure for silicon spacer concept in QFN versus BGA.

Given the six hotspots mentioned above, a ranking is made for each concept in the selected package types. Table 1 lists the worst-case package type for each of the six hotspots. Of course, these hotspots are related with possible failure modes. Looking at Table 1, the stress response of the QFN package family is found to be most critical. Therefore, this package is chosen to perform the optimization step.

Table 1: Hotspot ranking for the different package styles.

	Worst-case Package	
Hotspot	Silicon spacer	Ball spacer
Package warpage	QFN	QFN
Die-crack	QFN	BGA
Die-to-spacer delamination	QFN	QFN
Die-to-compound delamination	QFP	QFP
Compound-to-frame delamination	QFP	QFP
Body crack	QFN	QFN

A space-filling Latin-Hypercube DOE consisting of 9 input parameters and over 100 calculations is constructed. Using the parametric non-linear 3D FEM models, FEM simulations are carried out for all the 100 numerical experiments, and the earlier mentioned output variables (hotspots) are used as the response parameter.

For all response parameters quadratic models with interactions are used for RSM generation. Using OPTIMUS [9] automatic running procedure based on

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cross-validation, the unimportant model terms were deleted. The regression statistics are indicated that for all quadratic models the accuracy requirements are satisfied (in all cases: $R^2 > 0.9$).

Figure 8 shows a typical result of the optimization process. The figure shows the stress in the daughter die as function of its thickness and the thickness of the spacer die for a 12x12 mm^2 body size; a 75% pad-body-ratio; a 90% die-pad-ratio, and a 200μm leadframe thickness. Assuming an allowable stress level of 150MPa for Silicon [10], a clear risk area can be identified: a thick daughter die with a thick spacer in between. This will need an experimental verification. A design rule that can be deducted from Figure 8, is the fact that the silicon spacer should always be thinner than the thickness of the die on top of it. This is independent on the amount of stacks created. Other significant parameters that play a role for this stress reponse are:

- Body size: larger is worse
- Die-to-pad ratio: larger is worse
- Leadframe thickness: thinner is better

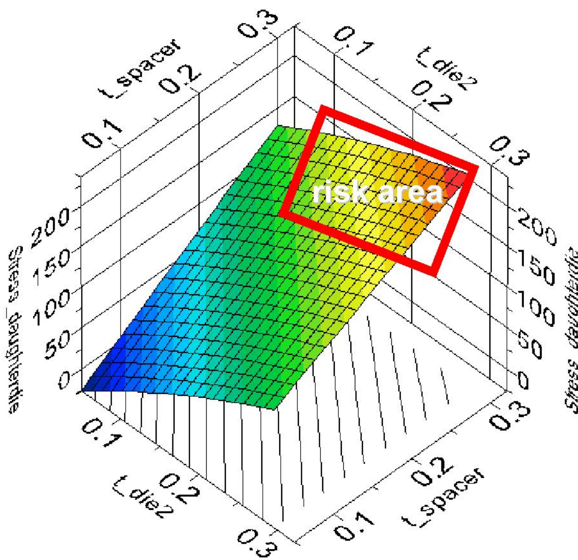

Figure 8: Response surface for daughter die crack in QFN: daughter die versus spacer die thickness.

Figure 9 shows the response surface for the stress in the compound as a function of pad-to-body and die-to-pad ratio. Other parameters are fixed to: 12x12 mm^2 body size; 150μm stacked die thickness, 150μm spacer die thickness, and 200μm leadframe thickness. For compounds, typical strength is in the order of 80-100MPa [1], in Figure 9 this value is not reached. But the figure indicates that increasing the number of stacks in the package, this risk will be a realistic one. The figure also indicates the effect of the die-to-pad ratio on the stress response in the compound. While increasing the ratio, the risk for body crack is higher. This needs an experimental verification. A design rule that can be deducted should relate the number of stacks with the maximum allowable. Other significant parameters that play a role for this stress reponse are:

- Body size: larger is worse
- Leadframe thickness: thinner is better

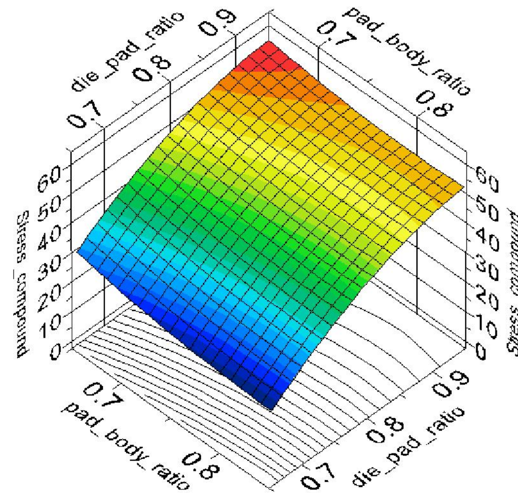

Figure 9: Response surface for compound crack in QFN: pad-to-body versus die-to-pad ratio.

5. Experimental Verifications

Standard qualification experiments will be conducted to verify the above mentioned calculated responses. Based on the optimization results, a smartly selected number of samples are created for which reliability qualification tests are performed. These samples are at the boundaries of possible failure modes as die-crack, die-to-die and die-to-compound delamination. For example, to investigate possible fracture in the daughter die a sample will be built with a 7x7mm2 body size, fixed mother and daughter die thickness and several spacer thicknesses, e.g. 150μm versus 300μm. The simulation results predict that the version with the 150μm thickness will survive (stress level is 85MPa) and the 300μm version not (170MPa). The samples will be subjected to TMCL testing, test until failure, and monitor failures at given cycles. The reliability tests are performed until failures to obtain acceleration factors for the specific failure mode.

For those legs that fail for the worst-case package style, see Table 1, identical samples will be built for the other package types. In this way, the ranking over the different package styles can be verified. At present, the sample building is in progress.

6. Conclusions

In this paper we have investigated two different concepts of die stacking in SiP packages: silicon spacer versus ball spacer. Virtual prototyping techniques are used to explore the stress/strain hotspots for different

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package types, being QFN, BGA, QFP, and LQFP. In general, QFN has the highest stress levels compared to laminate based (less stiff carrier) and QFP (has a bottom plastic balancer).

Optimization techniques are used to explore the design space of the worst-case package type. For example, it is found that the spacer thickness should be equal or thinner than the die stacked on top of it to prevent the occurrence of die crack. Standard qualification experiments on specific worst-case design will be conducted in future to verify the calculated responses.

By combining virtual prototyping techniques with smartly chosen reliability tests allows that possible failure mechanisms within stacked die SiP packages to be better understood and thus prevented.

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