Finite Element Optimization of Thermal-Mechanical Coupling in Smart P^2 Packagingaging Frontal Interconnects

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***Abstract*—With the rapid advancement of power semiconductor packaging technologies, Smart P^2 Packagingaging has emerged as a pivotal innovation for enhancing system performance and miniaturization. This study systematically investigates the thermal conduction characteristics and stress distributions of copper-filled vias (CFVs) in Smart P²Pack frontal interconnects through coupled thermal-mechanical finite element analysis. Results indicate that increasing CFV diameter enhances vertical heat conduction but causes localized heat accumulation and stress concentration due to the low thermal conductivity of encapsulation materials, elevating interfacial failure risks. Conversely, expanding CFV pitch promotes dispersed heat flow and reduces chip temperature but concurrently lowers local structural stiffness and exacerbates stress concentration. Optimal CFV design thus requires balancing thermal diffusion performance and mechanical constraints to ensure structural reliability and thermal stability.**

Keywords—Smart* P^2 *Packagingaging, Thermal-mechanical coupling, Copper-filled vias

I. INTRODUCTION

With the rapid advancement of modern power semiconductor packaging technologies, Smart P^2 Packagingaging has emerged as a pivotal innovation, offering multidimensional integration advantages that significantly enhance the performance and miniaturization of power electronic systems [1]. Smart P^2 Packagingaging technology enables the direct embedding of power devices such as MOSFETs and IGBTs into multilayer printed circuit boards (PCBs), resulting in a compact, low-inductance, and high-density packaging structure [2,3]. This integrated approach not only minimizes parasitic inductance and resistance but also supports higher switching frequencies and greater system efficiency. The incorporation of local DC-link capacitors within the PCB further optimizes electrical performance, suppresses high-frequency losses, and enhances transient response [4].

Thermal management is a critical design consideration for the Smart P^2 Packagingaging. By utilizing thermally conductive and electrically insulating materials together with a highly integrated stacked structure, the technology significantly reduces thermal resistance. This ensures rapid and efficient heat dissipation, thereby maintaining device stability and reliability under elevated current densities and harsh operating conditions. Manufacturing efficiency is achieved through the adoption of standardized modular S-Cell units, which streamline the assembly process and reduce system costs. This modular design paradigm not only simplifies production but also enables scalability, facilitating widespread adoption across a broad spectrum of applications [5].

Smart P^2 Packagingaging technology is increasingly deployed in electric vehicles, industrial automation, renewable energy systems, and other high-growth sectors [6]. Its superior electrical, thermal, and integration performance makes it a preferred solution for achieving high power density, compactness, and operational reliability. As the technology matures and the supporting supply chain strengthens, Smart P^2 Packagingaging is positioned to become a cornerstone in the evolution of next-generation power electronic systems.

Despite these advancements, the packaging process still encounters significant challenges in ensuring the thermal and mechanical reliability of copper-filled vias (CFVs), which are crucial for robust frontal interconnections. Addressing these challenges, this study employs coupled thermo-mechanical finite element analysis (FEA) to systematically investigate the heat transfer characteristics and stress distribution within CFVs under realistic operating conditions. This comprehensive simulation provides valuable insights for further optimization of the Smart P^2 Packagingaging module's frontal interconnect performance and long-term reliability.

II. Simulation model setup

To investigate the thermo-mechanical behavior of copper-filled vias (CFVs) in the Smart P²Pack power module, a three-dimensional finite element model was established using COMSOL Multiphysics. The simulation model consists of multiple layers, including a copper frame, a SiC MOSFET chip (1200 V/16 mΩ), a high thermal conductivity insulation layer, copper interconnects, and copper traces. For a balanced approach between accuracy and computational efficiency, the CFVs were simplified as cylindrical elements arranged in a 6×6 array. Leveraging the geometric and loading symmetry of the package, only one-quarter of the entire structure was constructed. Symmetrical thermal and mechanical boundary conditions were applied to the relevant planes, further reducing computational complexity. The diameter and pitch of the vias were defined as key variables to systematically analyze their influence on thermal conductivity and mechanical stress distribution. The SiC chip, serving as the primary heat source, was represented by a volumetric heat load. For the thermal boundary setup, forced convection was assigned to the top and bottom surfaces to emulate active cooling. In contrast, natural convection was set at the side boundaries to better approximate real operating conditions.

III. Results and Discussion

A. *Effect of CFV Diameter on Interconnect*

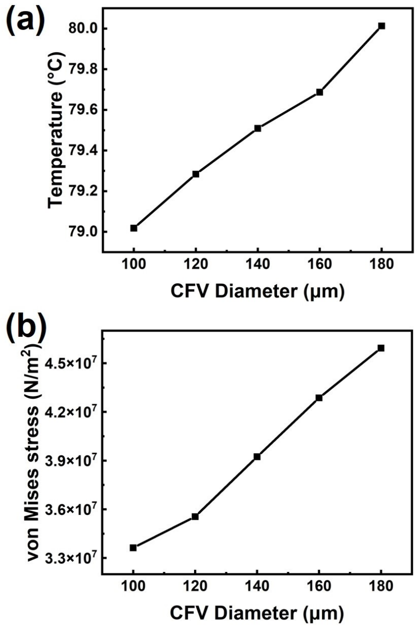

Fig. 1. (a) Effect of copper-filled via (CFV) diameter on average temperature within the CFV region. (b) Effect of CFV diameter on average von Mises stress under steady-state thermal loading

To systematically evaluate the effect of copper-filled via (CFV) diameter on the thermo-mechanical performance of Smart P^2 Packagingaging modules, this study designed a series of simulation cases with via diameters ranging from 100 μm to 180 μm, while keeping all other parameters constant. The average temperature and average von Mises stress within the copper pillar were extracted and analyzed, as presented in Fig. 1. As shown in Fig. 1(a), the average temperature in the CFV region exhibits an approximately linear increase with the enlargement of CFV diameter. When the via diameter increases from 100 μm to 180 μm, the average temperature rises from 79.02 °C to 80.01 °C. This phenomenon can be attributed to the enhanced thermal conductivity of the upward heat dissipation path as the cross-sectional area of the CFV increases, allowing more heat flow to be conducted towards the upper structure. However, the low thermal conductivity of the encapsulation medium above the copper pillar hinders effective heat release, causing heat accumulation within the pillar, especially near the chip region, and resulting in an average temperature rise. Meanwhile, the diversion of heat flow to the upper channel reduces the downward heat conduction, leading to a decrease in heat flux at the bottom surface. Fig. 1(b) illustrates the trend of average von Mises stress as the CFV diameter changes. The results show that the stress level increases significantly with larger via diameters, rising from 3.36×10^7 N/m^2 at 100 μm to 4.60×10^7 N/m^2 at 180 μm.

This effect is mainly due to the increased local stiffness caused by the larger via diameter, which reduces the overall structural flexibility and limits the release of thermal strain. The enhanced mechanical constraint during thermal expansion leads to higher stress concentration around the vias, particularly at the interface between the chip and copper traces, thereby increasing the risk of interfacial delamination or crack propagation.

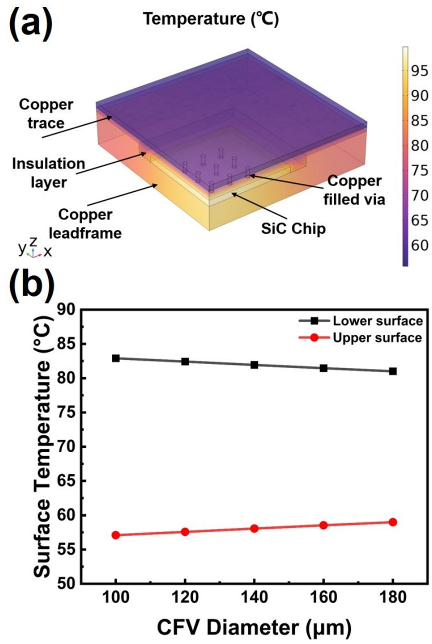

Fig. 2. (a) 3D temperature distribution of the smart P2 Packagingaging structure under steady-state thermal load. (b) Surface temperature trends on the top and bottom surfaces of the package with increasing CFV diameter

Further, the top surface of the SiC chip is directly connected to the copper-filled via (CFV), while the bottom surface dissipates heat through a highly thermally conductive substrate. The chip acts as the main heat source, and heat is primarily transferred vertically to both the upper and lower structures. As illustrated in Fig. 2(a), the three-dimensional temperature distribution clearly shows that the lower copper substrate region provides more effective heat spreading, making it the primary pathway for heat dissipation. In contrast, the upper encapsulation medium (such as molding compounds) has a relatively low thermal conductivity, which limits its ability to release heat effectively. Fig. 2(b) shows the temperature trends at the upper and lower surfaces for different CFV diameters. As the CFV diameter increases, the temperature at the upper surface rises slightly, while that of the lower surface decreases marginally. This phenomenon indicates that enlarging the CFV cross-sectional area enhances its thermal conductance, thus channeling more heat toward the upper structure. However, due to the limited thermal conductivity of the upper encapsulation medium, heat tends to accumulate near the CFV and at the chip's top surface, resulting in a localized temperature rise in this region. Conversely, the diversion of heat flow reduces the amount of heat transmitted downward. Still, the high thermal conductivity of the lower copper substrate continues to maintain a relatively low temperature level.

Overall, achieving optimal thermal management and structural reliability in CFV design requires a comprehensive approach that takes into account vertical heat dissipation paths, package material properties, and overall heat flow distribution.

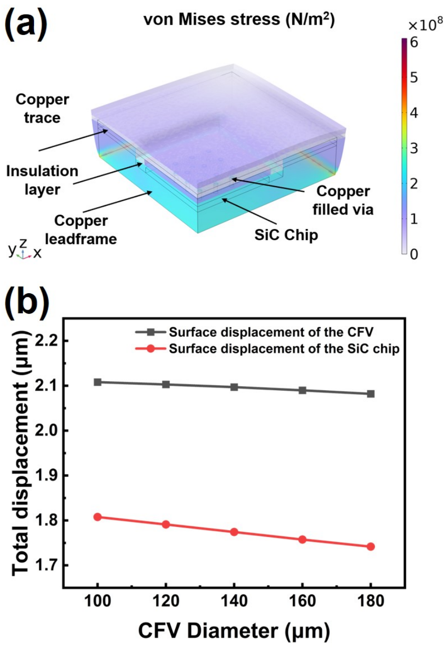

Fig. 3. (a) 3D von Mises stress distribution of the smart P2 Packagingaging structure under steady-state thermal load. (b) Surface displacement variation trends on the CFV and SiC chip of the package with increasing CFV diameter

Fig. 3(a) illustrates the average von Mises stress distribution of the package structure under thermal loading. It can be observed that the stress is mainly concentrated at the interfaces between the copper-filled via (CFV), the SiC chip, and the copper trace, indicating that these regions are susceptible to stress concentrations during thermal loading, thus becoming potential failure sites for structural failure. Fig. 3(b) shows the total thermal expansion displacement trends at the upper surfaces of the CFV and the chip for different CFV diameters. The results reveal that, as the CFV diameter increases, the thermal deformation displacement on both surfaces decreases, with a more pronounced reduction observed at the CFV surface. This is primarily attributed to the higher structural stiffness brought by larger diameter copper pillars, which provide stronger constraints against thermal expansion under load, thereby limiting the local displacement response.

It is noteworthy that, although increasing the CFV diameter leads to a rise in von Mises stress, the surface displacement differences are reduced accordingly. This reduction in displacement mismatch helps lower the risk of damage at the chip–CFV interface under thermal fatigue conditions.

B. Effect of CFV Pitch on Interconnect

To systematically investigate the influence of copper-filled via (CFV) pitch on the thermo-mechanical performance of Smart P^2 Packagingaging packaging structures, this study performed parametric finite element simulations with varying CFV pitches (ranging from 450 μm to 650 μm), while keeping all other structural parameters constant. The average temperature of the chip region and the average von Mises stress within the structure were extracted for each condition, as illustrated in Fig. 4. As shown in Fig. 4(a), the average temperature of the chip region decreases progressively with increasing CFV pitch. This result indicates that appropriately increasing the via pitch promotes a more dispersed heat flow path, mitigates local heat accumulation, and thereby enhances the overall thermal diffusion capability of the package.

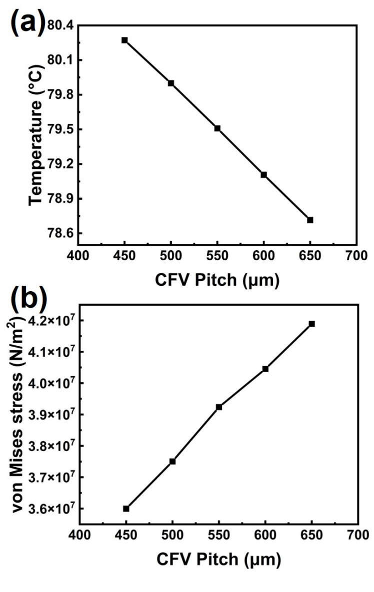

Fig. 4. (a) Effect of copper-filled via (CFV) pitch on average temperature within the CFV region. (b) Effect of CFV pitch on average von Mises stress under steady-state thermal loading

However, Fig. 4(b) demonstrates that the average von Mises stress increases significantly as the CFV pitch widens. With a sparser via arrangement, the effective mechanical support region within the structure is reduced, resulting in lower local stiffness. Under thermal expansion loading, this leads to greater deformation in the vicinity of the via, exacerbating stress concentration and ultimately increasing the equivalent stress level within the copper pillars.

In summary, the optimization of CFV pitch requires a careful balance between thermal diffusion performance and mechanical constraint. While increasing the pitch can help reduce chip temperature, it may also elevate local stress risks. Therefore, the via arrangement should be tailored to the specific application requirements, ensuring both effective thermal management and structural reliability.

Fig. 5 illustrates the three-dimensional vector distribution of heat flux within the package structure. It can be observed that the heat generated by the chip is primarily conducted vertically through the copper leadframe and then, together with the copper-filled vias (CFVs), diffuses toward both the upper and lower parts of the structure. Notably, the heat flux toward the lower copper leadframe is more concentrated and intense, indicating that it serves as the main heat dissipation pathway within the package. In contrast, although some heat is conducted upward through the CFVs, the heat flow in the upper channel gradually diminishes due to the low thermal conductivity of the molding compound, resulting in restricted heat transfer.

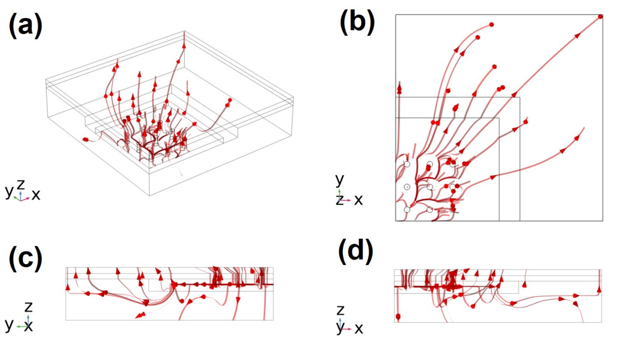

Fig. 5. (a) 3D heat flux distribution under thermal loading in the package structure (CFV Diameter = 140 μm, CFV Pitch = 550 μm). (b), (c) and (d) are top, side, and front views of the corresponding heat flux distribution

It is also noteworthy that the heat flux exhibits clear branching in the CFV region, and a pronounced heat accumulation zone is formed at the interface between the chip and the CFVs, suggesting this area is prone to thermal buildup and may become a potential hotspot. This distribution pattern highlights the competitive nature of heat flow between the upper and lower pathways. Therefore, rational optimization of CFV layout density and path distribution is crucial in package design to enhance overall thermal diffusion efficiency and thermal reliability.

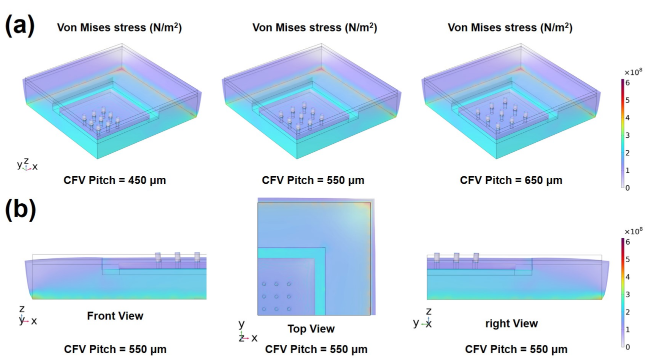

Fig. 6. (a) von Mises stress distribution of the package structure for different copper-filled vias (CFV) spacing conditions (450 μm, 550 μm, and 650 μm). (b) Multiple views of von Mises stresses at a CFV Pitch of 550 μm (The deformation scale factor is 100)

With the spacing between CFVs increasing, the cooperative mechanical constraint among adjacent CFVs diminishes significantly, as shown in Fig. 6(a). Each via becomes increasingly isolated in its response to thermomechanical loads, thereby bearing expansion-induced stresses individually rather than in a collectively constrained system. This structural decoupling leads to a notable increase in the average von Mises stress within each CFV. The inability of neighboring vias to share deformation reduces the redistribution efficiency of thermal strain, imposing greater localized stress on individual CFVs and consequently elevating the risk of interfacial or structural failure.

Meanwhile, the expansion of the overall CFV array area grants the packaging structure greater degrees of freedom for thermal deformation. Under thermal loading, this increase in spatial flexibility allows the global deformation to be more uniformly distributed, resulting in a reduction in the maximum displacement observed at individual CFVs. This inverse relationship is attributable to the fact that thermal expansion-induced strain can be absorbed over a wider structural domain, thereby alleviating extreme localized deformations.

As illustrated in Fig. 6(b), CFVs located at the periphery and corners of the package experience significantly greater thermally induced displacements compared to those situated near the geometric center. This variation arises from the reduced mechanical constraints and longer expansion paths encountered by edge vias, which facilitate larger deformation accumulation. In contrast, centrally located CFVs are restrained by symmetric surrounding structures, limiting their freedom to deform. These insights emphasize the critical need to reinforce thermal-mechanical reliability in peripheral and corner regions of CFV arrays to prevent interfacial mismatch, delamination, or crack propagation.

IV. Conclusion

This paper employed coupled thermal-mechanical finite element analysis to explore the impact of CFV dimensions and spacing on the thermal and mechanical performance of Smart P²Pack structures. Findings highlight that increasing CFV diameter improves vertical thermal conductivity but introduces challenges of heat accumulation and heightened mechanical stress. Enlarging the CFV pitch can effectively reduce chip temperatures but may weaken structural rigidity, enhancing local stress concentration. Consequently, CFV optimization necessitates a balanced approach between thermal management and structural integrity, with particular attention to reinforcing edge areas to mitigate failure risks.

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