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Modeling and Analysis of SRAM PUF Bias Patterns in 14nm and 7nm FinFET Technology Nodes

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***Abstract*—SRAM Physical Unclonable Functions (PUFs) are one of the popular forms of PUFs that can be used to generate unique identifiers and randomness for security purposes. Hence, their resilience to attacks is crucial. The probability of attacks increases when the SRAM PUF start-up values follow a predictable pattern which we refer to as bias. In this paper, we investigate the parameters impacting the SRAM PUF bias of advanced FinFET SRAM designs. In particular, we analyze the bias with respect to temperature, mismatches in the power supply network, and ramp-up time. We also consider process variation, circuit noise, and SRAM layout in our analysis. Our simulations results match with the silicon measurements. From the experiments we conclude that (i) the SRAM layout and in particular the power supply network can lead to a bias, (ii) this bias increases with temperature, and (iii) this bias increases when the supply ramp-up time decreases.**

***Index Terms*—Bias, FinFET, Power Supply Network, SRAM PUF, Temperature**

I. Introduction

Physical unclonable functions (PUFs) are security primitives implemented in hardware that are utilized as a source of device-unique fingerprints. They commonly exist on electronic commercial boards or can be easily implemented [1]. PUFs have an intrinsic variation as a consequence of the manufacturing process and can be used as a randomness source, i.e., it makes the same design behave differently for each produced chip. SRAM circuits are one of the popular candidates for PUFs due to their availability on most of chips. The SRAM start-up values of the cells after power-up create a unique fingerprint that can be used as PUF. To evaluate the PUFs' reliability (e.g., impact of environmental parameters (e.g., temperature, noise, and power supply) [2, 3]) and security (e.g., resilience against machine learning attacks) [4], different metrics are used. For example, fingerprints should consist of a random pattern to satisfy the required entropy. Particularly for security reasons, it is critical that they do not have strong location-dependent bias patterns; otherwise, cell responses can be predicted based on neighbouring cells. For examples, in our measurements we observed for some advanced FinFET designs a new bias pattern that acerbates with higher temperature. Therefore, it is important for such advanced nodes to evaluate the reliability and security metrics. In the literature, no articles exist that reported clear temperature-dependent bias patterns for SRAM. Instead, typical publications on PUFs focus on PUF designs evaluated with their *reliability* and *security*. Regarding the *reliability*, existing literature on SRAM PUF is mainly focused on planar technology, where Hamming distance to a reference measurement (e.g., enrollment measurement) is mainly used as the reliability measure [2, 5, 6]. These studies also demonstrate that the Hamming distance to an enrollment measurement of SRAM PUF in the planar technology can be corrected by selecting error correcting codes (ECCs) with a sufficient error correction capability. In [3, 5], only the SRAM PUF's reliability in FinFET technology is investigated, and it is demonstrated that the SRAM PUF remains reliable as the technology scales down. Regarding the *security*, existing literature on SRAM PUF mainly focuses on SRAM PUF attacks. In particular, the authors investigate attacks based on low-temperature data remanence in [7] and similarity in SRAM devices' specifications and manufacturing facility in [8]. Furthermore, the authors proposed two schemes for debiasing, i.e., selection and balancing for SRAM PUFs in [9] to secure SRAM PUF.

To the best of our knowledge, this work is the first work that analyzes the SRAM PUF temperature dependent bias patterns, found in 14nm and 7nm FinFET SRAM designs. As an evaluation metric, we use the Hamming weight of SRAM PUF values. The contributions of this paper are:

- Identification of this new bias pattern from silicon measurements and a theoretical explanation why it exists.
- Simulation model based on the theory to assess the bias of SRAM PUF for FinFET technology nodes 14nm and 7nm considering different temperatures (from 0°C to 85°C), different ramp-up times (from 1μs to 50μs), process variation, circuit noise, and SRAM layout design in terms of the interconnects model.
- Validation of simulation model and the underlying theory with the corresponding silicon measurement.

The remainder of the paper is organized as follows. Section II provides background on SRAM PUF security and the parameters affecting the security. Section III provides the silicon results and shows the new bias pattern. Section IV presents the theory, simulation framework and validates the results with silicon. Finally, Section V discusses the results and concludes this paper.

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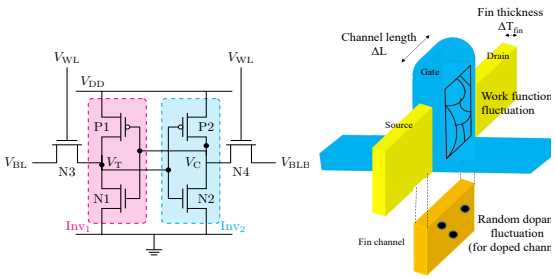

Fig. 1. (a) SRAM Cell (b) FinFET Structure and Sources of Variation [13]

II. Background

In this section, we briefly explain the major parameters that impact the SRAM PUF bias, such as process variation, environmental parameters, and cell layout. Thereafter, we present the relevant SRAM PUF metrics for this work.

A. SRAM PUF

An SRAM PUF consist of the start-up values (SUV) of typical 6-transistor (6T) SRAM cells. Each SRAM cell contains two cross-coupled inverters, as shown in Fig. 1. An SRAM cell is ideally designed as a fully symmetric cell, as the pFETs and nFETs (P1, P2, and N1, N2 in Fig. 1) of the cross-coupled inverters are symmetrically designed. As a result, both corresponding transistors in inverters have identical electrical parameters by design, e.g., threshold voltage (V_{TH}). The cell power-up value is at the middle point of the power supply (VDD) for an ideal SRAM cell because of the symmetry in the cell. However, as transistors are affected by process variation, their parameters follow a normal distribution. This leads to different electrical parameters than the intended design parameters. When the SRAM cell powers on, based on the random transistor mismatch, one inverter is stronger and turns on sooner and decides the start-up value of the SRAM cell. The SRAM cells are placed in a two dimensional array, as shown in Fig. 2. As it can be seen, the power supply lines are connected to each SRAM cell, either horizontally or vertically.

B. Process Variation

The FinFET manufacturing process leads to different types of variation in transistors' parameters. Fig. 1 shows the FinFET structure and the main sources of process variation, i.e., channel length, fin thickness, oxide thickness, and gate work function. The process variations can be categorized into global variation and local variation. Global process variation is typically a result of variations in the lithography process and wafer etching [10]. These variations are typically constant over larger areas, and lead to different process corners [11]. Local process variation cause variations in transistors locally [12], i.e., two neighbouring transistors are affected by it differently. Hence, the SRAM startup values are mostly affected by local process variation.

C. Environmental Parameters

Environment parameters also affect the SRAM PUF values. The main environmental parameters are temperature and various noise sources. Each is briefly described next.

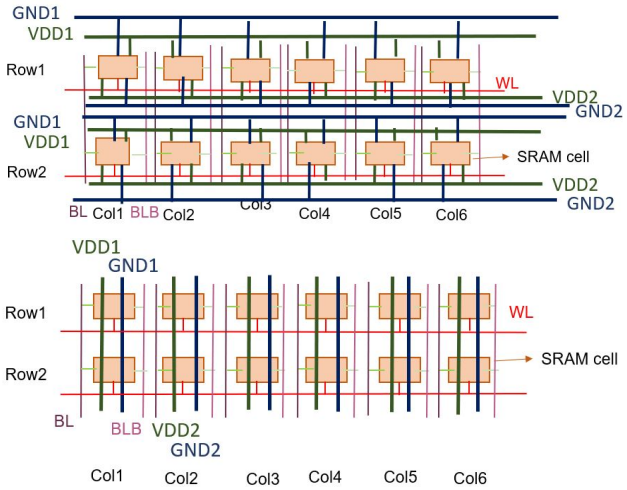

Fig. 2. SRAM With a) Horizontal Power Lines b) Vertical Power Lines

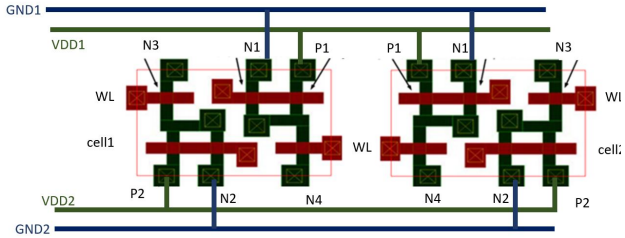

Fig. 3. SRAM Layout for Two Neighbor SRAM Cell (Modified From [14])

Temperature: Temperature variation has an impact on the electrical parameters of transistors and hence, affect the SRAM start-up values. An start-up value, which is specified by V_T and V_C in Fig. 1.(a), depends on the transistor currents through both inverters (i.e., the current through P1 and N1, and the current through P2 and N2) during voltage ramp-up, which further depends on the threshold voltage V_{th} and transistor mobility [2]. Therefore, to investigate the impact of temperature on SRAM PUF, it is required to understand how V_{th} and mobility are impacted by the temperature. The temperature dependency of V_{th} is shown in Eq. (1).

$$\frac{\partial V_{th}}{\partial T} = \frac{\partial \Phi_{ms}}{\partial T} + t_{ox} \times \frac{\sqrt{4\varepsilon q N_a}}{\varepsilon_{ox}} \times \frac{\partial \sqrt{\Phi_F}}{\partial T} + 2 \times \frac{\partial \Phi_F}{\partial T}, \quad (1)$$

where T represents the temperature, Φ_{ms} the work function difference between the gate and substrate, t_{ox} the oxide thickness, ε the permittivity, q the charge, N_a the dopant concentration, ε_{ox} the oxide permittivity, and Φ_F the Fermi potential [15].

Note that by increasing temperature, Φ_{ms} and Φ_F decrease. Therefore, one can conclude that V_{th} decreases with increasing the temperature [15].

Circuit Noise: The SRAM start-up value can also be affected by all noise sources in a chip. The most relevant noise types in FinFETs are thermal noise and flicker noise. Thermal noise originates from the resistance that a current flow faces inside the channel and is mainly affected by the temperature. Flicker noise originates from current variations in a conductor [16] due to the different paths that electrons take when traveling through the conductor. These variations depend mainly on the

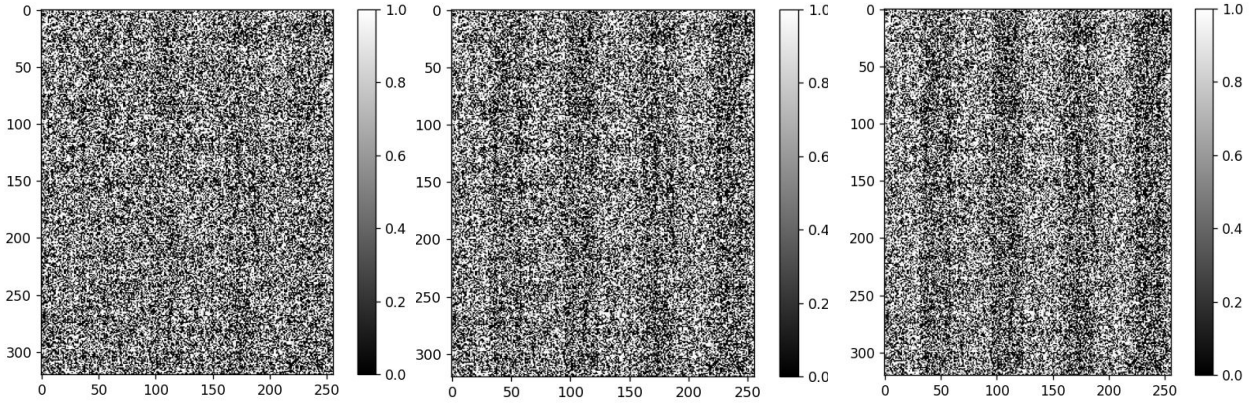

Fig. 4. The Probability of a 0 or 1 SUV for Each Bit for the 7nm PUF at 0°C, 25°C, and 35°C, Respectively

operating frequency, transistor size and capacitance. Therefore, the temperature has no or little impact on the flicker noise. We ignore the power supply noise in a chip as its impact is negligible [17].

D. SRAM Cell Layout and Power Network

One of the typical layout designs for the SRAM cell (see Fig. 1) is shown in the left side of Fig. 3. Its two inverters are placed in two rows: on the top row the left inverter (consisting of N1 and P1) and on the bottom row the right inverter (N2 and P2). Each row also contains a pass transistor, denoted by N3 and N4. Similarly, the right side of Fig. 3 contains a mirrored 6T cell.

In the layout design of the SRAM devices, the VDD and GND lines can be connected in two different ways (see also Fig. 2: horizontally or vertically. In case they are horizontally connected as shown in Fig. 3, the transistors on the same row are connected to same VDD line, i.e., VDD1 or VDD2.

E. Bias Metric for SRAM PUFs

To evaluate the bias (and hence randomness) of an SRAM PUF, Hamming Weight (HW) can be used. The HW is defined as:

$$HW = \frac{\text{number of cells with SUV='1'}}{\text{number of cells}},$$

When a PUF is biased towards '1' (or '0'), the HW comes closer towards 1 (0) and the min-entropy, which is a measure of unpredictability for a random variable like a PUF response [18], decreases from its ideal value of 1. An ideal completely unbiased SRAM PUF has a HW value of 0.5. SRAM PUFs with lower min-entropy, which correspond to HW value closer to 1 or 0, are more vulnerable to attacks. This means that the probability of guessing a PUF response is higher [4]. We evaluate the results in this paper based on the Hamming weight metric.

III. Silicon Measurements

In this section, we present the silicon results for 14nm and 7nm SRAM PUF measurements. The measurements focus on measuring the Hamming weight at different temperatures for a PUF based on Xilinx 7nm and NXP 14nm SRAM.

Fig. 4 shows the bitmaps (i.e., probability of raw PUF responses being 0 or 1) for the 7nm SRAM PUF at three temperatures, i.e., 0°C, 25°C, 35°C. As can be seen from the figure, the start-up values are not completely random and a visible bias pattern in the form of striped columns starts to appear based on the location and temperature. To analyze this bias, we calculate the Hamming weight of the vertical stripes. Although we do not know the internal structure and size of the SRAMs, we have plotted the start-up values based on a 256-bit width memory. Note that this does not affect the presence of the bias pattern. From the bitmap and its fast Fourier transform (FFT), we calculated the period of repeating bits, which are grouped and biased towards a specific value, i.e., '0' and '1'. We observed that after every 32 bits a bias towards either 0 or 1 takes place. Thereafter, we group all cells into 32-bit groups and calculate the Hamming weight for the two groups by referring to them as even and odd columns. The Hamming weight values for these groups for the 7nm SRAM PUF are shown in Fig. 5 a and b. As it can be seen, when the temperature increases, the Hamming weight almost monotonically increases from the value of 0.5 for even columns and monotonically decreases from the value of 0.5 for odd columns. Note that this impacts both the reliability and security of the PUF.

Similarly, we have calculated the Hamming weight for the PUF based on NXP 14nm SRAM. There we observed a bias pattern every 64 bits. The results are shown in Fig. 5 (c)-(d). Comparing Fig. 5 (a)-(b) with Fig. 5 (c)-(d), we conclude that the bias increases with technology scaling. Furthermore, for the 14nm it seems that the temperature impact stabilizes after a certain point (i.e., after 15°C).

IV. Theory and Simulation Results

This section presents a theory for the observed pattern, the experiment setup and results.

A. Theory

The observed bias pattern in the previous section is hard to explain with process variations only in the cross-coupled inverters. We have verified with simulations that the cross-coupled inverters are not responsible for this. Hence, another explanation has to be found.

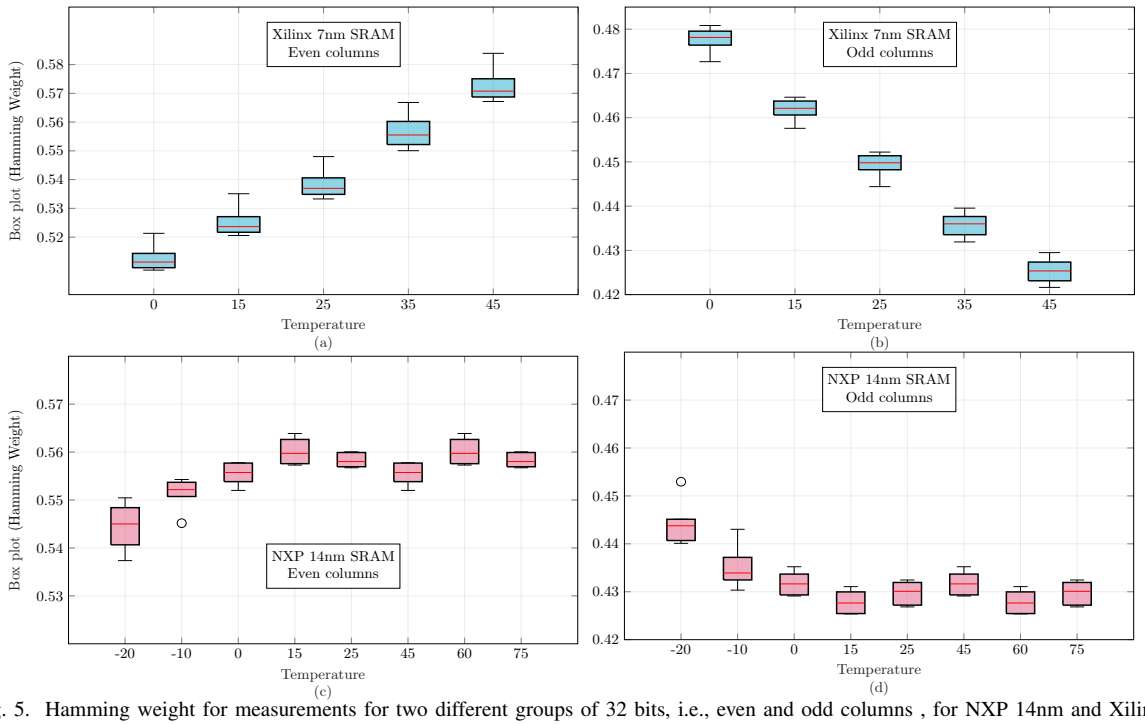

Fig. 5. Hamming weight for measurements for two different groups of 32 bits, i.e., even and odd columns , for NXP 14nm and Xilinx 7nm

As it is discussed in Section II, the power lines can be connected horizontally and vertically, where Fig. 3 showed the horizontal configuration. As it can be seen, the two inverters from the same SRAM cell have a different path to the power supply and ground, i.e., VDD1, VDD2, GND1, and GND2. Due to different lengths of the wires and process variation, each path to power supply and ground has different resistance and capacitance values. Although this affect is negligible once the power is stable, it nevertheless can affect the start-up value of a cell during ramp-up. We believe that the fundamental cause of the newly observed bias pattern is due to the asymmetrical power delivery to the cell. We model this asymmetry with a resistance and capacitance. We insert these components between the pull-up transistor and VDD and between the pull-down transistor and GND of one of the inverters only. Even if we assume that the resistance and capacitance are temperature independent, they affect the start-up current of the inverters (i.e., current through N1 and P1 and the current through N2 and P2 in Fig. 1). At higher temperature, these currents increase with the same ramp-up time and hence the inverter with the resistance and capacitance will slow down, which biases the cell value at higher temperature. In reality, the resistance increases as well at higher temperature which further strengthens the affect; it can be modeled by: $R(T) = R(T_0)(1+\alpha(T-T_0))$, where T, T_0, and α are operational temperature, initial temperature and the temperature coefficient of copper, respectively [19].

The start-up values at different temperatures are also affected by the temperature dependency of process variation and thermal noise. When the temperature increases, the impact of process variation and thermal noise increase as well. However, when the added resistance and capacitance to model a mismatch in the network are large enough, it can overcome the effects caused by process variation and thermal noise. As a result, the systematic asymmetry in the SRAM PUF cells increases and the bias pattern becomes more visible.

The even and odd stripes repeating every 32 in Fig. 4 can be explained with cell mirroring [20]. In cell mirroring, the two inverters of the cell are mirrored. For example, in Fig. 3 the right cell is the mirror of the left cell.

B. Simulation setup

In this work, we consider the traditional 6T SRAM cell with minimum transistor sizes. Each cell consists of two pull-up pFETs, two pull-down nFETs, and two nFETs access transistors. The ratio between their number of fins i.e., pull-up:pull-down:access transistors, equals 1:2:2. This sizing ratio is required for reliable read and write operations [21].

We model the process variation using local variations on the four main parameters of transistors: channel length (L), fin thickness ($tfin$), oxide thickness (tox), and work-function (ϕ). We model the sources of variation using normal distributions in which their mean corresponds to their nominal value. Furthermore, the standard deviations of L, $tfin$, tox, and ϕ are 4%, 4%, 4%, and 1.3%, respectively [22]. We simulate 100 different cells that are affected by local variation, 50 normal ones and 50 mirrored ones. We measure their start-up values for 100 different noise samples; we use the HSPICE noise model for transistors in the time domain to realize this. When we use more samples (e.g., 500 samples), we observe a negligible difference in our results. Hence, 100 samples are selected to maintain a feasible simulation time.

We vary the temperature and ramp-up time to investigate their corresponding impact on the start-up values of the SRAM PUFs. We model the resistance and capacitance of

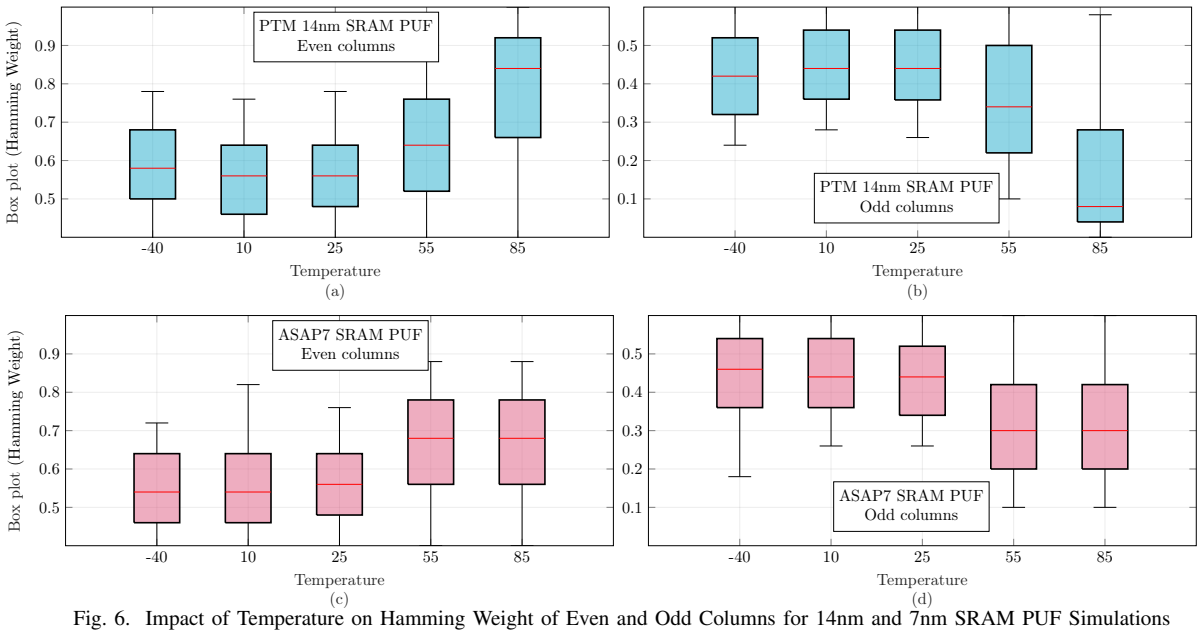

Fig. 6. Impact of Temperature on Hamming Weight of Even and Odd Columns for 14nm and 7nm SRAM PUF Simulations

the mismatch in the power network using typical ranges for interconnects and calibrate their values based on the measurements [23]. We vary the resistance between 50Ω to 200Ω and capacitance between 100fF to 10pF and we selected the values that match the trends from silicon measurements the best. We evaluate the Hamming weight for the different column strips, i.e. even (with normal cells) and odd columns (with mirrored cells) in the SRAM structure.

C. Simulation Results

In this section, we present the simulation results. In particular, we evaluate the impact of temperature, mismatches in the power network, and ramp-up time on the bias.

1) Impact of Temperature: The impact of temperature on 14nm SRAM PUF is shown in Fig. 6. From the figure, it can be concluded that the Hamming weight monotonically increases with temperature. This can be seen by comparing the mean values of the different boxplots in the figure. The trends observed from simulation generally match with those of the measurement results and hence, the model and explanations provided in Section IV-A are correct. However, due to the mismatches in libraries and noise models, the exact numbers differ. Looking at the absolute values, especially the older PTM model is inaccurate in terms of absolute values. Nevertheless, its HW trends matches the silicon results of 7nm (see Fig. 5 (a)-(b)) The trends with the ASAP7 library follow actually the silicon trends observed in Fig. 5 (c)-(d). In particular, we expect to have smaller boxes (higher precision) if we consider more accurate noise models as they are responsible for the heights of the boxplots. Note that the noise models do not impact the average trend but just the height of the boxplots.

2) Impact of Mismatches in Power Network: The impact of power lines on the SRAM PUF Hamming weight is shown in Fig. 7. We vary the resistance from 25Ω (blue bars) to 500Ω (red bars). As can be derived from the figure, by increasing the resistance that represents mismatch in the power supply lines, the Hamming weight for the even columns is larger than 0.5 and it increases monotonically. For odd columns, the Hamming weight is smaller than 0.5 and it decreases monotonically. We excluded the figure for odd columns from the paper due to space limitation. If the mismatch between both VDD lines is small (i.e., a small R value) the noise and process variation still dominate as the blue bars in Fig. 7 vary only slightly from the nominal value of 0.5.

3) Impact of Ramp-Up Time: The impact of the ramp-up time on the HW is shown in Fig. 8. Due to space limitations, we only show the simulation results for the 14nm design and randomly picked 10 out of 100 noise samples. From the figure, we conclude that a slower ramp-up time (i.e., 50 μs) leads to a Hamming weight 0.5 for all the cells. This means that the noise and process variation are dominant here. When the ramp-up time decreases, the Hamming weight reduces. Note that with a fast ramp-up time, more current flows through the cross-coupled inverters. In that case the resistance and capacitance that model the mismatch in power supply become more dominant, which leads to more biased cells. This behaviour is similar to the case where the temperature was increased. Unfortunately, we had no means to very the ramp-up time with silicon measurements.

V. Discussion and Conclusion

In this work, we analyzed the SRAM PUF bias in FinFET technology. From the results, we conclude the following:

SRAM PUF Bias: An SRAM PUF ideally requires fully random values, i.e., the Hamming weight of 0.5 for all even and odd columns. We showed that there is a bias based on the location of bits with respect to their start-up values. Therefore, the Hamming weight of such cells differs from the ideal 0.5 value. Furthermore, we showed that the reason for such

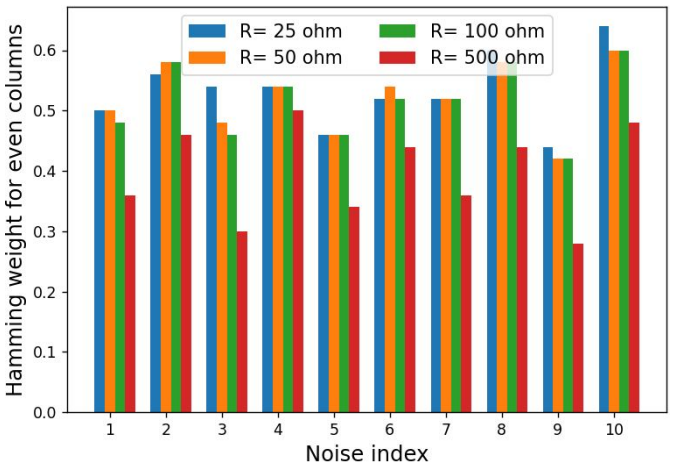

Fig. 7. Impact of Different Resistance Values on Hamming Weight

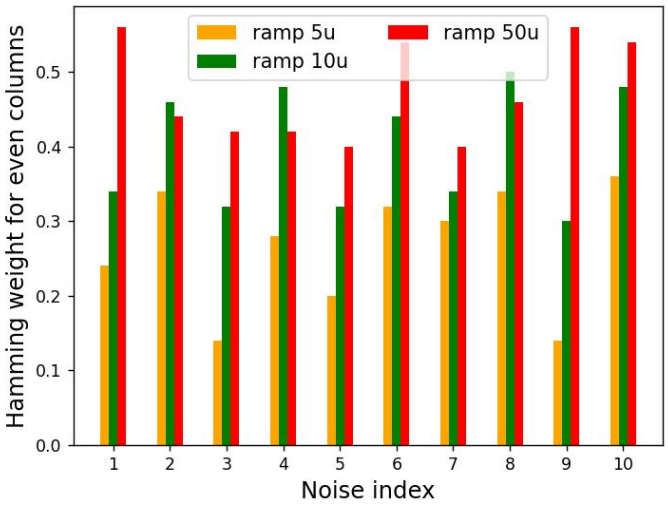

Fig. 8. Impact of Ramp-Up Time on Hamming Weight

behavior can be explained by a mismatch in the power supply network, which could be modeled with an RC model. Based on the potential layout of SRAM devices we used this RC model in the supply and ground lines. The RC model integrated in the simulation model matches well with the measurement results performed at 14nm and 7nm SRAM PUF designs. We observed that the actual bias depends not only on temperature, but also the transistor technology, noise, ramp-up time etc. Hence, it is critical to analyze the impact of these parameters on advanced SRAM PUFs before they are deployed.

Impact of temperature on bias in SRAM PUF: Using the simulation model and measurements, we showed that by increasing the temperature, the bias in SRAM PUF increases for the targeted designs. This means that the PUF is vulnerable at higher temperatures, and hence, it is easier to attack the PUF. However, it also means that the ECC must be increased in order to get correct responses [3]. Although we showed results for 2 designs (7nm and 14nm) we also had other designs that did not exhibit this bias pattern at higher temperatures. We believe that it depends on the power supply network as shown in this paper and it is further discussed in the last point.

Impact of ramp-up time on bias in SRAM PUF: To reduce the impact of the temperature-induced bias, one could slower the VDD ramp-up time. Using a slower ramp-up time results in Hamming weights closer to 0.5 and thereby canceling the impact of the mismatch in the power supply network. However, it might be better to use different ramp-up times for low and high temperatures, in order to minimize the noise impact [2].

Cells with less bias: A second way to get rid of this temperature-dependent bias is to redesign the SRAM cells. Instead of connecting both inverters to two different VDD lines, they have to be connected to the same VDD line. For example in Fig. 3, this would mean that the left cell would be connected to the top VDD1 and the right cell to the bottom VDD2.

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