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In this work, we present the fabrication technology of a monolithically integrated photonic platform combining key components for optical coherence tomography (OCT) imaging, thereby including a photonic interferometer, a collimating lens, and a 45° reflecting mirror that directs the light from the interferometer to the collimator. The proposed integration process simplifies the fabrication of an interferometric system and inherently overcomes the complexity of costly alignment procedures while complying with the necessarily stringent optical constraints. Fabricated waveguide characterization shows total optical losses as low as 3 dB, and less than 1 dB of additional loss due to the Si 45° mirror facet. The alignment standard deviation of all components is within 15 nm. The integrated lens profile achieves a divergence angle smaller than 0.7°, which is close to that of a collimator. The proposed photonic platform provides the premise for low-cost and small-footprint single-chip OCT systems.

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1. INTRODUCTION

Early-stage disease detection plays a major role in any successful medical treatment. Due to early detection, treatments are more effective and recovery is faster, which significantly contribute to lower medical costs. In particular, dermatological problems, especially skin cancer, are unfortunately constantly rising and putting future generations at higher risk [1–3]. Biopsy, a frequently used medical examination procedure, implies surgical removal and histopathological examination of the tissue by trained medical specialists. Biopsy, however, evidences only a temporary disease condition, and consequently it is not suitable for periodical monitoring of lesion changes; furthermore, the procedure is employed only once the illness is recognized.

As an alternative, optical coherence tomography (OCT) is a non-invasive imaging technique that, by using low coherence light interferometry, achieves a good lateral and axial resolution (around 10 μm) and a penetration depth into the skin of several millimeters [4,5]. This allows real-time visualization of the morphology of the epidermis, the junction, and the dermis layer at the same time. The main working principle of OCT is based on the reflection of light waves from a translucent scanning object [6]: low coherence interferometry is used to measure a time delay, i.e., the optical path length of the light signal. Figure 1 illustrates the interferometer configuration for the three most common types of OCT systems: time-domain (TD) OCT, spectral-domain (SD) OCT, and swept-source (SS) OCT, respectively. Each of the three configurations consists of several discrete components, making OCT systems sensitive to their misalignment. Hence, OCT systems are typically assembled using delicate and time-consuming assembly procedures, which makes them expensive.

Both size and costs of an OCT system can in principle be significantly reduced, while preserving the required image quality, by replacing discrete components with integrated optics. Indeed, many components of the TD-, SD-, and SS-OCT systems have a functional equivalent in photonic integrated technology. Moreover, integrated optics technology provides significant fabrication scalability, especially in silicon-based systems; and monolithic integration can directly solve the components alignment problem.

In integrated optics, optical fibers are replaced with waveguides, while beam splitters and signal combiners are replaced by multimodal interferometers (MMIs) [7]. For TD-OCT systems, a movable reference mirror is a delay line that can be made in Si using the thermo-optic effect [8], while a SD-OCT spectrometer can be made using an array waveguide grating

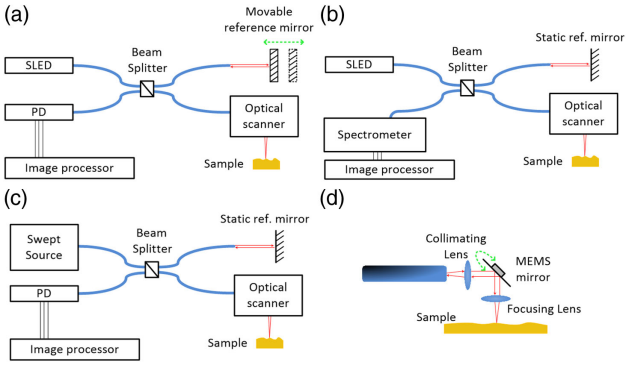

Fig. 1. Interferometer configuration for (a) TD-OCT, (b) SD-OCT, and (c) SS-OCT systems. SLED, super-luminescent light emitting diode; PD, photodetector. (d) Standard configuration for a lateral scanner.

(AWG) [9]. Therefore, a solution for assembly and packaging simplification is monolithic integration of all OCT components together into a single chip.

Such solutions have already been implemented. A complete Mirau interferometer including a microelectromechanical systems (MEMS) scanner for SS OCT was demonstrated in Ref. [10]. However, this solution requires stacking chips one on top of another; thus, it cannot be considered as a photonic integrated circuit (PIC). Fully functional small-footprint interferometers for SS OCT were presented in [11,12]. CMOS compatible SD interferometers with AWG have already been demonstrated [9,13] and as such can be integrated with photodetectors. A step further was given in Ref. [14] where a PIC interferometer for SS OCT was integrated with two photodetectors for balanced detection.

Nevertheless, none of the presented solutions integrates a collimating lens. Although in all these systems assembly complexity is significantly reduced, still they all require an external collimating lens. Therefore, they do not completely solve the issue of OCT components optical alignment. Moreover, full integration of these systems with MEMS actuators would make optical alignment with the external lens more challenging during its operation.

Since OCT for dermatology uses 1.3 μm wavelength for which Si is transparent, all components can be made using standard MEMS and integrated circuit (IC) microfabrication technology. This allows self-alignment of all optical components, and alignment quality to be defined simply by the IC fabrication mask overlay capability of the exposure tool used in lithography. Further, to provide light movement, a collimating lens and a waveguide finished with a 45° mirror facet should be monolithically integrated into a movable block. Such a concept was presented in Ref. [15] and is illustrated in Fig. 2.

The first step towards a fully integrated MEMS-based OCT system is combining all optical components into a single Si block. Thus, a Si photonics OCT interferometer [16] with a 45° ending facet [17] and Si microlens [18] must be fabricated as a single device. In this paper, we present the integration of all optical components into a single photonic platform for potential use in a single-chip micro-opto-electro-mechanical system (MOEMS)-OCT device. The photonic platform has a

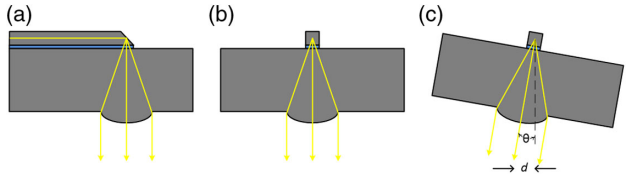

Fig. 2. Monolithically integrated micro-opto-electromechanical scanner with waveguide, mirror, and lens integrated in a single Si block. (a) Device cross section alongside the waveguide: Si-based photonic circuit with a 45° ending waveguide facet scatters the light towards a microlens at the bottom of the chip. (b) Si block in initial state. (c) Upon rotation, the Si block moves the light beam and translates angular displacement θ into surface scanning range d [device cross section perpendicular to the waveguide in (b) and (c)].

footprint of $5 \times 10\ \text{mm}^2$, out of which 20% is used for the PIC, the mirror, and the lens, while the rest is left for potential fabrication of MEMS actuators. The alignment standard deviation is within 15 nm, which is limited only by lithography exposure tool specification. The paper provides design guidelines and focuses on fabrication process development of the integrated photonic platform. As a proof of concept, the final device is optically characterized, and the results are discussed.

2. SYSTEM DESIGN

The whole interferometer is designed in a thick silicon-on-insulator (SOI) PIC technology [16,19,20]. The interferometer, schematically depicted in Fig. 3, consists of a single light input, a reference loop, and a measurement path with two outputs. The interferometer consists of rib and ridge waveguides, rib-to-ridge waveguide converters, and 2×2 MMIs for beam splitting and recombination. To characterize the optical performance, a set of test waveguides with MMIs, rib-to-ridge converters, mirrors, and Euler and S-bends is added to the design as well.

The concept proposed in Ref. [15] suggests a device featuring a collimating lens at the output. A configuration with a

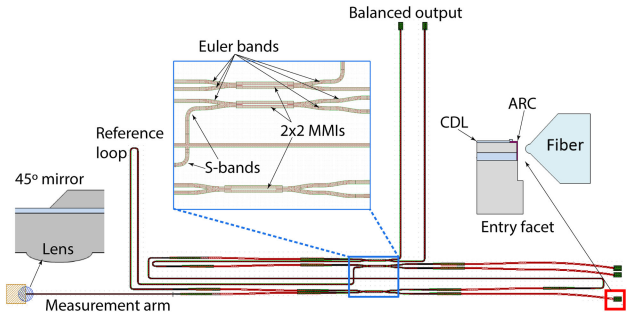

Fig. 3. Interferometer design for the single-chip OCT system. The input light is split into two signals: measurement and reference. The measurement signal goes through the measurement arm, reflects from the mirror towards the lens, and illuminates the sample. The reflected light from the sample travels the same path backwards. The reflected measurement beam is then recombined with the reference signal. The reference signal is maintained in a simple waveguide delay line. The recombined measurement–reference signal is finally split into two identical signals to improve signal-to-noise ratio through balanced detection. CDL, cladding layer; ARC, anti-reflective coating.

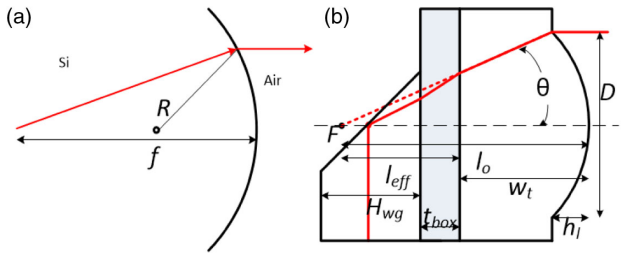

Fig. 4. Collimating Si lens. (a) Refraction of a light beam from Si to air, resulting in a beam parallel to the optical axes. (b) Light propagation and effective focal point to have a collimated beam at the lens output. Light beams indicated in red.

collimated lens requires an additional focusing lens, for which assembly is needed. However, due to the properties of a collimated beam, this configuration is less sensitive to alignment, and light will not lose focusing during lens actuation.

The collimated microlens can be of spherical, aspheric, Fresnel, or planar binary optic type. Fresnel and binary optic lenses are diffractive optical components, whose design strongly depends on the wavelength used. Moreover, they are sensitive to chromatic aberrations when broadband light is used. For the bandwidth of a superluminescent light-emitting diode (SLED) source with 1.3 μm wavelength, as used in this work, silicon has low chromatic dispersion [21], making Si spherical and aspheric lenses the best choice to collimate the light at the output of the interferometer optical path. Further, aspheric and Fresnel lenses are fabricated using a grayscale lithography process, which is more challenging for development compared to the photoresist reflow technique [18]. Therefore, for the purpose of feasibility of this platform, a spherical lens is used.

The goal is to collect at the chip backside the light beam diverged from the 45° facet into the chip [Fig. 2(a)]. The integrated lens ensures intrinsic alignment with the other components. Low surface root mean square roughness for all the optical components, i.e., less than 1/10 of the working wavelength in the medium, is required to have good quality images. For the operation wavelength at 1.3 μm in Si, the roughness of the microlens must be below 37 nm.

To have a collimated light beam, the source should be placed in the focal point of the lens [Fig. 4(a)]. Using Snell's law, lens equation, effective object distance [Fig. 4(b)], and the fact that the image projection must be infinity to have a collimated beam, the radius of lens curvature R can be expressed as [22]

$$R = \frac{n_{\mathrm{Si}} - 1}{n_{\mathrm{Si}}} w_t + \frac{n_{\mathrm{Si}} - 1}{2 \cdot n_{\mathrm{Si}}} H_{\mathrm{wg}} + \frac{n_{\mathrm{Si}} - 1}{n_{\mathrm{SiO_2}}} t_{\mathrm{box}}, \tag{1}$$

where w_t is wafer thickness, while the rest of the parameters in Eq. (1) are explained in Table 1.

All parameters in Table 1 are set by the waveguide design and as such give a constant contribution to the lens radius of curvature. Thus, the choice of w_t directly determines the lens radius of curvature, i.e., the focal length. To minimize optical losses in the system, the lens numerical aperture $\mathrm{NA} = \tan\theta$ must be larger than or equal to the numerical aperture of the Si waveguide, namely, $\mathrm{NA_{Si}}$. The lens diameter can be defined as [22]

Table 1. "Thick" SOI Waveguide Parameters for Single-Chip OCT System

Parameter	Value (nm)
Thickness H_{wg}	3000
Step-height h_{rib}	1800
BOX thickness t_{box}	400
Width w_{wg}	3000
MMI width w_{mmi}	5000
SiO_x cladding layer thickness t_{cdl}	240
SiN_x anti-reflective coating thickness t_{arc}	165

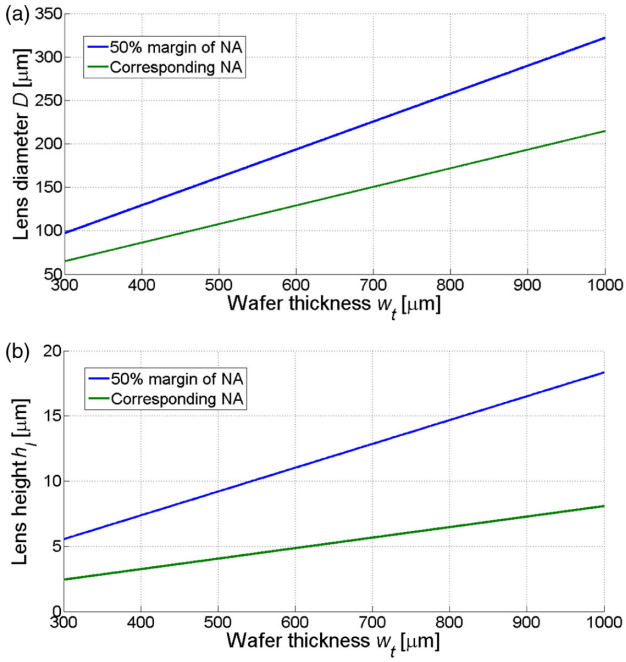

Fig. 5. Collimating Si lens parameters versus wafer thickness: (a) lens dimeter D and (b) lens height h_l.

$$D \geq 2 \cdot \tan\theta \cdot f = 2NA_{\mathrm{Si}} \cdot f = 2 \cdot \frac{\mathrm{NA_{air}}}{n_{\mathrm{Si}}} \cdot \left(w_t + \frac{1}{2} H_{\mathrm{wg}} + \frac{n_{\mathrm{Si}}}{n_{\mathrm{SiO_2}}} t_{\mathrm{box}}\right), \tag{2}$$

where $\mathrm{NA_{air}}$ is the waveguide numerical aperture in air. Commercially available SOI ridge waveguides have $\mathrm{NA_{air}}$ of 0.38. The diameter together with the radius of curvature define lens height [Fig. 4(b)]:

$$h_l = R - \sqrt{R^2 - \frac{D^2}{4}}. \tag{3}$$

To ensure all light is collected by the lens, a design rule for lens diameter is to add 50% to its minimal requirement. Figure 5 represents lens diameter and lens height versus substrate thickness with and without 50 % margin.

The wafers should be thick enough to minimize deformation caused by the intrinsic stress in the deposited layers, yet thin enough to make actuator fabrication easier [23].Therefore, a standard thickness for photonic application is 700 μm. The chosen wafer thickness of 700 μm for the collimated lens translates into a radius of curvature of $R = 500$ μm. Considering 50% increase in the numerical aperture, the lens diameter is 225 μm, which gives a 12.82 μm lens height. However, such a high lens would severely increase the backside topography, making further processing of the integrated device problematic. The lens diameter D is therefore fixed to 150 μm, based on the corresponding waveguide numerical aperture and on the lens height h_l of 5.67 μm.

3. SYSTEM INTEGRATION

The photonic platform must integrate three different technologies into a single device on both wafer sides. Therefore, each fabrication step must be well positioned within the fabrication process to minimize the total number of steps and to not lose device functionality. To allow mirror facet fabrication, the whole design, i.e., all lithography mask exposures, must be oriented at 45° with respect to the primarily flat wafer. The whole process is fully scalable, since it was developed with fully automated cassette-to-cassette tools for microfabrication. Device definition was done using UV lithography with the ASML PAS 5500/80 wafer stepper, which ensures alignment performance reproducibility of 15 nm.

The starting material is defined based on system design and number of thermal oxidation steps in the fabrication process. Thus, the starting material for the integrated photonic platform is a double-side-polished (DSP) 700 μm thick SOI wafer with 400 nm thick buried oxide (BOX) layers. Initial device layer thickness must include extra Si for smoothening oxidation of the lens (2.5 μm 18]) and of the waveguides (0.5 μm [19,20]). Hence, for a target waveguide height of 3 μm, the initial device layer thickness must be 4.35 μm.

The last consideration to be taken into account is the order of component fabrication. Component order is dictated mainly by the amount of thermal oxidation and combining functional layers deposition to minimize complexity. All optical components require SiN antireflective coating (ARC), thus ARC implementation should be left for the very end of fabrication process. The lens requires thick thermal oxidation and must be done at the beginning of the process. Mirror and waveguide formation do not have such strict orders for fabrication, as long as the smoothening oxidation step is done after both etchings. In order to have a better overview of the alignment performance, first the mirror is etched and then the 45° facet is formed.

A. Lens Fabrication

The microlens is formed on the backside of the wafer. However, optical circuitry is sensitive to any mechanical scratches. Thus, the wafer frontside must be protected with 1 μm thick plasma-enhanced chemical-vapor-deposited (PECVD) SiO_x during lens formation. The lens formation is based on photoresist thermal reflow and on dry SF_6/O_2 plasma etch to transfer the geometry into Si. Using the selectivity value of 3.10 ± 0.05 for the Si etching process at 50 mTorr [18], the initial photoresist ball cap height was estimated at 17.58 ± 0.28 μm to fabricate the 5.67 μm high lens. Assuming 20% of photoresist volume shrinkage during the thermal reflow process [18], the initial photoresist thickness should be 10.91 ± 0.15 μm.

Table 2. Optimal Spinning Speed for Final Lens Height

Spinning speed (rpm)	1050	1100	1150	1200
Lens height (μm)	5.74	5.66	5.5	5.4

To obtain this, the optimal spinning speed for resist coating was experimentally determined (see Table 2). After coating, the wafers were soft baked in an automated coating/development track for 90 s at 100°C followed by additional 120 s at 115°C. Photoresist exposure under ultraviolet light through the designed mask defined cylinders with a diameter of 150 μm. After development, the wafers were baked for 4 h at 160°C to allow the cylinders to reflow. Finally, the wafers were dry etched for 50 min. The Si microlens height was measured by mechanical profilometry and is summarized in Table 2. The best result is obtained using 1100 rpm photoresist coating, and this parameter was used to process wafers.

After the etching, microlens surface roughness must be reduced through an oxidation procedure. Since there was already an oxide layer on the frontside of the wafer, to have controlled Si consumption on the frontside, the protective layer had to be removed using a wet etching process in buffered hydrogen fluoride (HF) (BHF) solution. Next, 2.5 μm thick wet thermal oxide at 1100°C was grown to reduce lens surface roughness, and subsequent BHF wet etch was used to strip the oxide away. The frontside oxide is used as a protective layer, and during the wet etch strip, it is covered with a photoresist layer. All fabrication steps for the Si microlens are illustrated in Figs. 6(a)–6(e).

The microlenses fabricated this way were characterized using white-light interferometry (WLI) [Fig. 7(a)]. The spherical approximation of the lens geometry gives a radius of curvature $R = 520 \pm 10$ μm, which corresponds to a 730 ± 15 μm focal length. The calculated divergent angle amounts to $0.25 \pm 0.13°$ compared to the reference, and it is acceptable to be used as a collimated beam. However, due to wafer non-uniform etching, only 60% of devices had the desired lens curvature. The lens surface roughness of 30 nm was measured using a Keyence VK-X250 3D laser confocal microscope, which agrees with previously achieved results [18] and complies with the design requirements. Figure 7(b) represents an optical image of the fabricated lens.

The Si microlens must be protected during waveguide end-mirror fabrication. Also, the frontside must be cleared down to the silicon. Therefore, the photoresist layer was stripped, and on the wafer backside, i.e., lens surface, a 1 μm thick PECVD SiN layer was deposited as scratch protection. Hence, wafers could be emerged in BHF solution to strip the frontside oxide layer while preserving the backside protection [Fig. 6(f)].

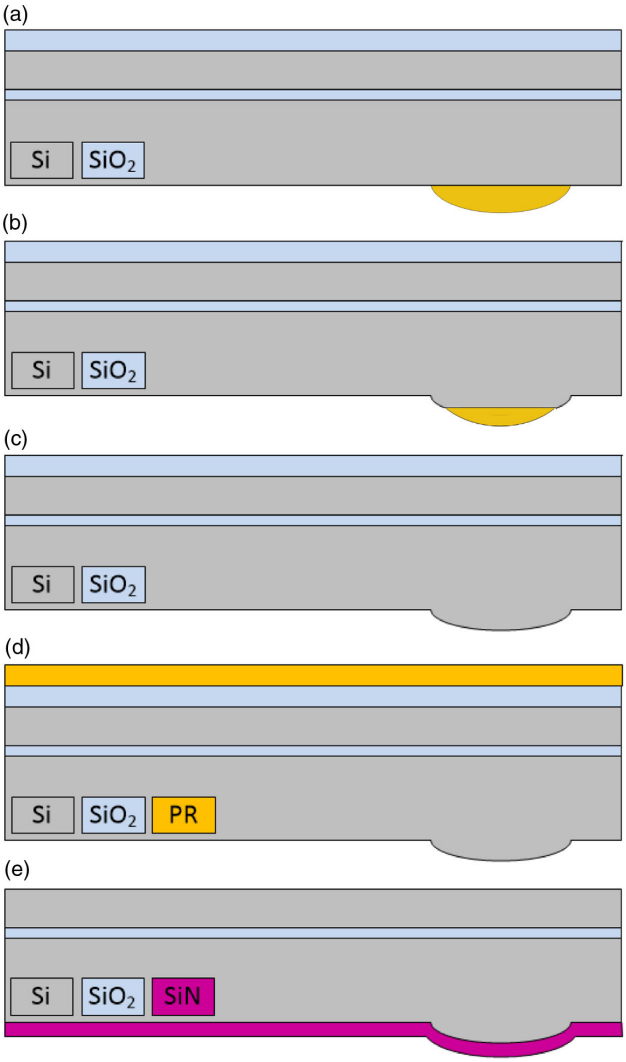

Fig. 6. Integrated SI microlens fabrication: (a) 1 μm thick SiO_x frontside protection and thermal reflow of the photoresist cylinder into a ball cap. (b) Dry etching transfer of Si photoresist ball cap into Si. (c) Completely etched Si lens. (d) Lens roughness reduction process and backside oxide strip. (e) Wafer with Si microlenses ready for waveguide fabrication.

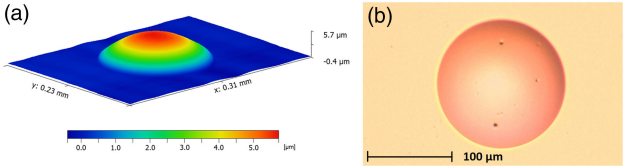

Fig. 7. Si microlens: (a) 3D WLI image of lens surface and (b) optical image of Si microlens.

B. Waveguide Etching

The waveguide fabrication was based on commercial waveguide technology developed by VTT Technical Research Centre of Finland Ltd [16,19,20]. The main step of the two-step waveguide Si etching consists of a Bosch deep reactive ion etching (DRIE) process with short cycles [24]. The rationale is to minimize scattering losses induced by sidewall roughness, as created by, e.g., inductively coupled plasma (ICP) etching or RIE. Standard ICP or RIE dry etching processes create sidewall roughness perpendicular to the light propagation, which is responsible for scattering losses in waveguides. Conversely, the Bosch process creates scallops that are parallel to the light propagation and do not create any obstacle along the light path. The waveguide etching process parameters are given in Table 3. The platen temperature during the process was kept at 20°C and duty cycle of the pulsed platen power was 20%.

Table 3. Waveguide Etching Process Parameters

Parameter	Passivation	Etch
Time (s)	1.2	1.8
Pressure (mTorr)	45	25
Power (W)	2200	2200
Bias (W)	0	80
C_4F_8 gass flow (sccm)	280	0
SF_6 gas flow (sccm)	0	350

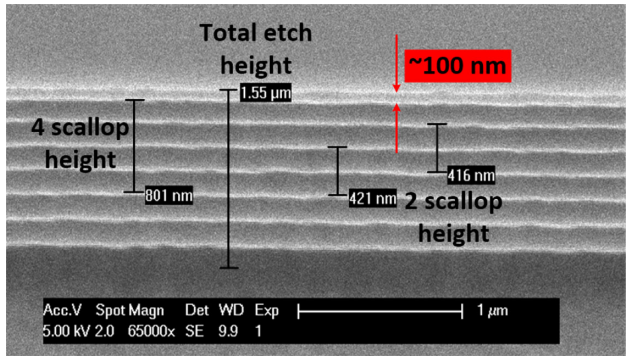

Fig. 8. SEM image of the waveguide sidewall after etching without prior native oxide removal.

The result obtained with nine cycles of this etching process is shown in Fig. 8. Measurements show a scallop height of 200–210 nm and a total of eight scallops, where the first scallop height is only 100 nm. The first and a part of the second etch step were used to break through the native SiO_2 formed on the wafer surface [25]. This results in a lower step height with respect to the subsequent cycles. Better etching control was achieved by introducing a 4 min wet etch in 0.55% HF solution to remove the native oxide and passivate the Si surface just before any DRIE process for waveguides fabrication took place.

Waveguide fabrication starts with a thin layer of PECVD silicon oxide (200 nm) deposition as a hard mask layer. The hard mask pattern is defined with lithography and dry etching of silicon oxide. Then, the second lithography is defined. First, waveguide etching is done with 4 min long 0.55% HF dip and nine-cycle-long dry etching using the recipe defined in Table 3 to form a 1.8 μm deep trench [Fig. 9]. After photoresist removal, the second etching is performed with 4 min long 0.55% HF dip and six-cycle-long dry etching (Table 3). In the final step of etching, the silicon oxide hard mask must be stripped off using the wet etch process.

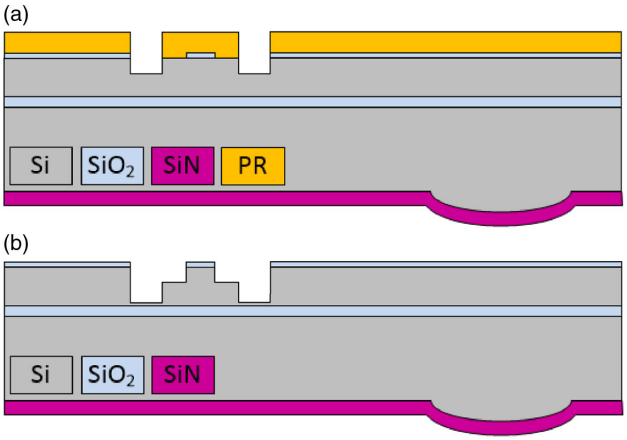

Fig. 9. Two step waveguide etching: (a) first waveguide etching with photoresist mask. (b) Second waveguide etching with silicon oxide hard mask.

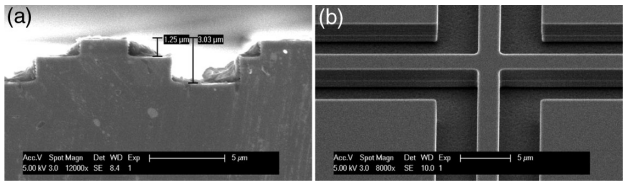

Fig. 10. Waveguide etching results. (a) Vertical cross section of the rib-to-ridge waveguide converter. Etching is done on a normal (non-SOI) wafer to confirm step height control in bulk Si. (b) Waveguide crossover after etching.

The vertical cross section of the rib-to-ridge converter was etched in two steps of nine and six cycles, respectively, with native oxide removal prior to etching [Fig. 10(a)]. The targeted depth of 3 ± 0.1 μm was achieved with a total of 15 cycles, each 200 nm in depth. A crossover of two waveguides is depicted in Fig. 10(b). Good scallop size control is achieved and thus, the BOX oxide layer is untacked during the hard mask stripping, since silicon over-etch is prevented during the waveguide etch process.

C. Mirror Formation

The next optical component of the device is the 45° mirror facet. It is based on wet tetramethylammonium hydroxide (TMAOH) etching and landing on the ⟨110⟩ Si crystal plane, which has a 45° slope towards the ⟨100⟩ wafer surface [17,26,27]. Additional surfactants must be introduced to reduce surface roughness of the ⟨110⟩ and ⟨100⟩ planes. A 25% TMAOH etching solution with 50 ppm of Triton-X-100 at 85°C was used here following the results presented in Ref. [27].

A test etch of 30 min was performed after adding 50 ppm of Triton-X-100. 300 nm of LPCVD silicon oxide was patterned as a hard mask for mirror fabrication. To expose the ⟨110⟩ plane, the mask opening was rotated 45° with respect to the primarily flat wafer. A passivation of the Si surface was done using 4 min 0.55% HF etching and Marangoni drying to avoid native oxide formation.

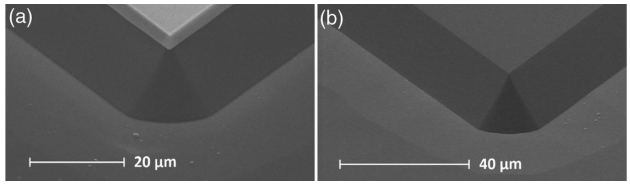

Fig. 11. Si mirror: (a) 45° facet after etching and (b) 45° facet after hard mask removal.

Figure 11 shows SEM images of 45° facets. The total measured height is 14.7 ± 0.2 μm and the undercut is 3.3 ± 0.1 μm. The facets look very smooth. The presented results agree with those in Ref. [26] and can be used to determine process and design parameters for the mirror formation. The total etch time for 3 μm high waveguides is fixed to 6 min and 10 s, and the mask design includes an offset of 675 nm to compensate for the etching undercut and to maintain mirror–lens alignment.

Once the mirror etching process was established, the process wafers were coated with 300 nm LPCVD silicon oxide and patterned to form a hard mask for the mirror fabrication [Fig. 12(a)]. After photoresist removal, a 45° facet was formed using the previously described process, and the hard mask was removed using wet etching in BHF solution [Fig. 12(b)]. To prepare wafers for finalization of waveguide processing, the protective SiN layer on the lens surface was removed using H_3PO_4 solution at 157°C. Then, a waveguide and mirror smoothening step was performed by 500 nm thick thermal oxidation and subsequent oxide wet etch removal using BHF solution. In this step, Si microlens surface was also oxidized, and no further surface quality improvement was observed. These steps are summarized

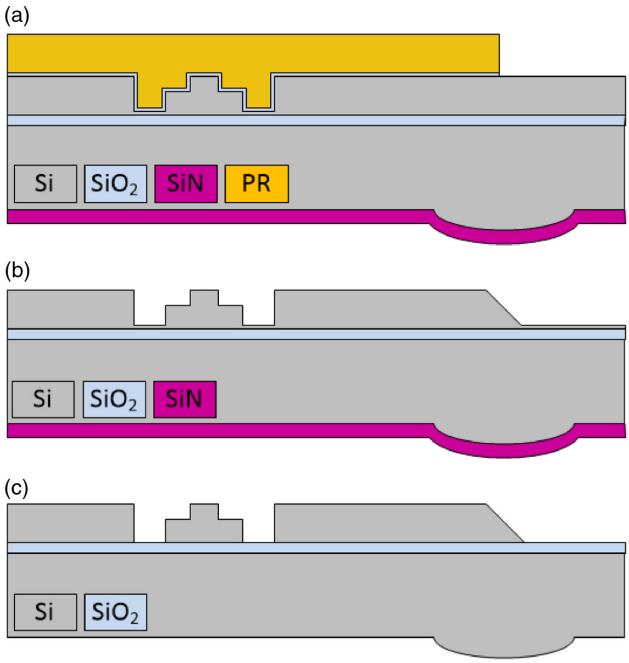

Fig. 12. Mirror formation: (a) hard mask definition for mirror etching, (b) mirror etching and hard mask removal, and (c) SiN scratch protection removal and thermal oxidation for surface quality improvement.

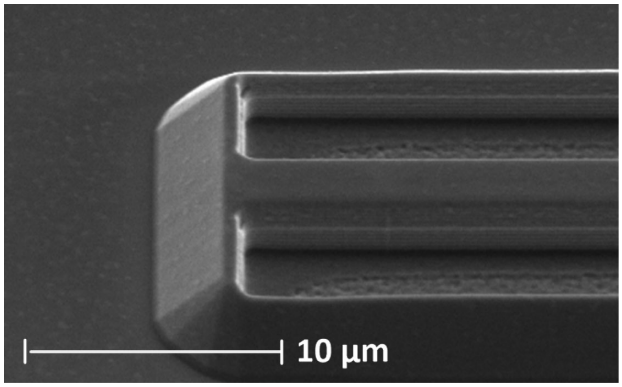

Fig. 13. 45° mirror facet at the end of the measurement arm waveguide.

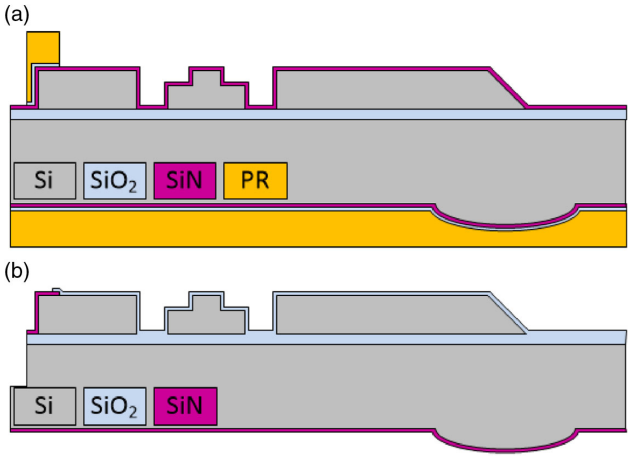

Fig. 14. Finalization of the photonic platform: (a) ARC layer definition of waveguide entry facet and the lens and (b) final view of the chip cross section with all optical components.

in Fig. 12(c). The final mirror etching result is presented in Fig. 13.

D. Finalization of the Photonic Platform

Final steps in the integration process of all optical components are the application of ARC and a cladding layer for better light confinement inside the waveguides. A 165 nm thick LPCVD silicon nitride ARC was applied on every air–photonic circuit interface, i.e., on each waveguide facet and on the lens. Patterning of ARC was done using a 100 nm thick LPCVD silicon oxide as the hard mask. Since the SiN layer must remain on the lens surface as well, the hard mask on the wafer backside had to be protected. Therefore, after frontside lithography for ARC definition, the wafer backside was coated as well [Fig. 14(a)].

The hard mask was patterned using wet BHF etching, and the silicon nitride layer was removed with H_3PO_4 solution at 157°C. Then, a 240 nm thick layer LPCVD silicon oxide was deposited as the cladding layer. To expose waveguide inlets and the lens, the cladding layer and remaining 100 nm-thick hard mask layer are patterned using frontside lithography and subsequent wet etch process in BHF solution. Finally, to

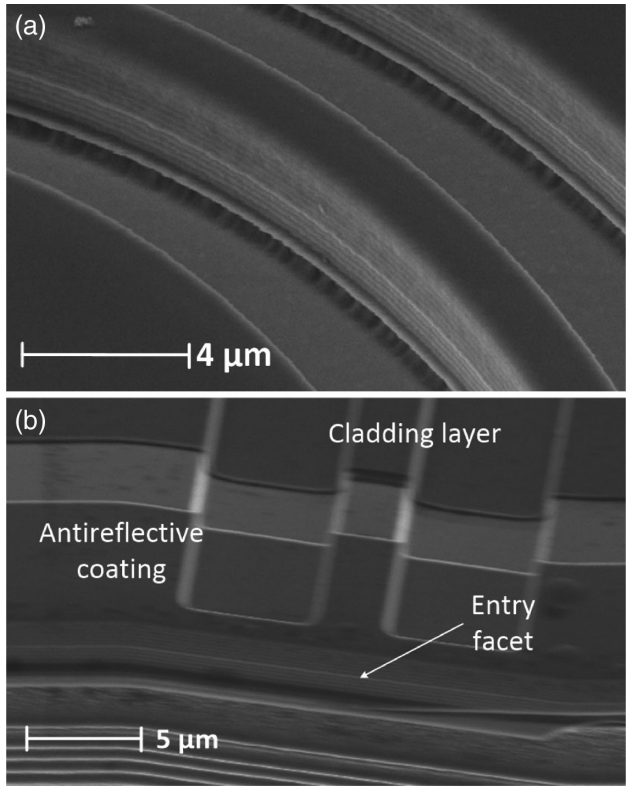

Fig. 15. Snapshots from fabrication results: (a) SEM image of waveguide S-bend and (b) SEM image of waveguide entry facet.

enable fiber coupling into the photonic platform, a 100 µm deep trench was etched using the Bosch process in front of the waveguide entry facet [Fig. 14(b)].

Fabrication results of the photonic platform are presented in Fig. 15. SEM images of waveguide S-bend [Fig. 15(a)] and entry facet [Fig. 15(a)] confirm an overall good waveguide definition. However, in spite of the surface improvement step that was introduced, a slight scalloping can still be noticed. This should not disturb waveguide propagation losses, but it might cause higher light coupling losses on the entry facet. Also, the BOX layer is partially etched next to the waveguide, probably during the waveguide smoothening process. Most importantly, there is no undercut, and waveguide integrity was preserved.

4. OPTICAL CHARACTERIZATION

A. Optical Loss Measurements

Figure 16 depicts the setup used to characterize propagation losses of the test waveguides. Light coming out of the 1.3 µm SLED is coupled to the waveguide using a lensed fiber. At the waveguide end, light is decoupled from the fiber again and reaches the photodetector [Fig. 16(a)]. To characterize optical losses at the mirror facet, the photodetector was placed below the mirror [Fig. 16(b)].

A straight waveguide with 2 rib-to-ridge converters (at input and at output) was characterized as a reference giving 3 ± 0.5 dB total loss. Waveguides with 1 to 20 Euler bends were then measured, and the optical losses less than 0.1 dB per single Euler

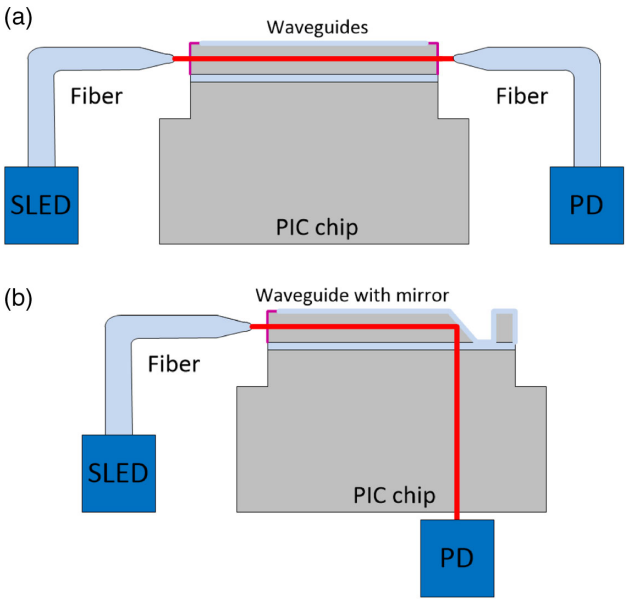

Fig. 16. Schematic view of the measurement setup used for waveguide characterization: (a) different waveguide geometry and (b) 45° mirror facet and lenses. Light path is sketched in red.

bend were calculated based on a difference between these waveguides. The same approach was applied for waveguides with two, four, and six S-bends, giving the optical loss of less than 0.25 dB per S-bend.

MMIs with one input and two outputs were used as beam splitters. Hence, at least 3 dB of additional optical losses were expected at each output. Measurements showed a total loss of 8 ± 1 dB, which means an additional loss of 4 ± 1 dB per output. A straight waveguide with a 45° mirror facet was used to characterize mirrors and showed to have less than 1 dB losses per mirror. The addition of the Si microlens did not influence loss measurement. Having all components characterized, total optical loss of the interferometer was calculated to be 14 dB in the measurement arm and 23 dB in the reference arm.

The optical performance of the presented photonic components is slightly worse compared to that of commercially available passive optical circuitry, since the losses are slightly higher (1–2 dB on average). The waveguide etching process could be further optimized to reduce the scallop size. Even though, as mentioned, the scalloping does not significantly influence the propagation losses, it can introduce scattering losses at the waveguide entering facet [Fig. 15(b)], which can explain the major difference from commercially available circuits.

The mirror shows good optical performance. However, the aggressive TMAOH etch imposes rather short etching times, which makes such etching of Si hard to control. Furthermore, TMAOH etching depends strongly on etching temperature. Hence, it is advised to pre-heat the wafer for better process control.

B. Light Spot Characterization

The light spot characterization setup is depicted in Fig. 17. The light coming out of the Si microlens drops on a 64 × 512-pixel

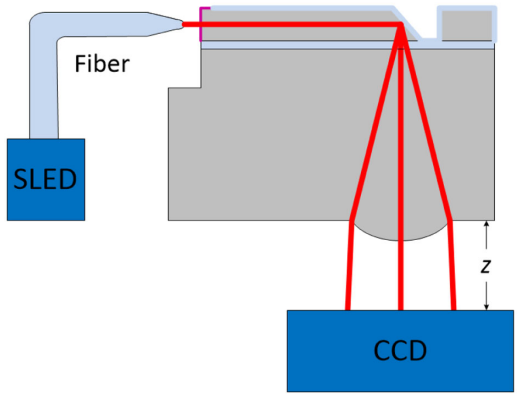

Fig. 17. Schematic view of the measurement setup used for light spot characterization. Light paths indicated in red.

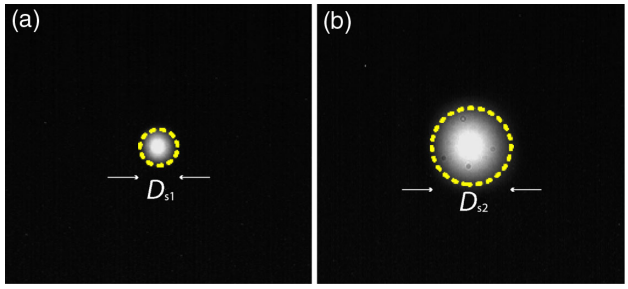

Fig. 18. CCD image of the light spot measured at (a) $z_1 = 33 \pm 5$ mm and (b) $z_2 = 81 \pm 12$ mm.

resolution CCD camera for infrared light. The light spot was measured at two working distances, $z_1 = 33 \pm 5$ mm and $z_2 = 81 \pm 12$ mm, while the acquisition time for the CCD camera was set to 10 μs.

Figures 18(a) and 18(b) illustrate measured light spots at $z_1 = 33 \pm 5$ mm and $z_2 = 81 \pm 12$ mm, respectively. As expected, the light beam is observed to diverge, and the spot size at a longer working distance appears bigger. The maximum intensity of the CCD camera is reached in the center of the beam. This is the result of both light beam power and acquisition time. Upon measuring the light spot diameter D_s, the divergence angle α was calculated based on [22]

$$\tan \alpha = \frac{D_{s2} - D_{s1}}{2 \cdot \Delta z} = \frac{D_{s2} - D_{s1}}{2 \cdot (z_2 - z_1)}. \tag{4}$$

The diameter D_{s1} is measured to be 0.86 ± 0.05 mm, while D_{s2} is 1.91 ± 0.05 mm. The calculated divergence angle of 0.63° agrees with the expected values given in Section 3.A.

To extract the light beam intensity profile, the CCD image acquisition time was lowered to 5 μs to avoid saturation of the image intensity. The pixel size of the camera was 20 μm, and since the beam was already diverging, the profile shape is better illustrated for longer working distance. The relative light spot intensity at 81 mm and its Gaussian fit are presented in Fig. 19, where a good match of the profile with the fitting function is observed.

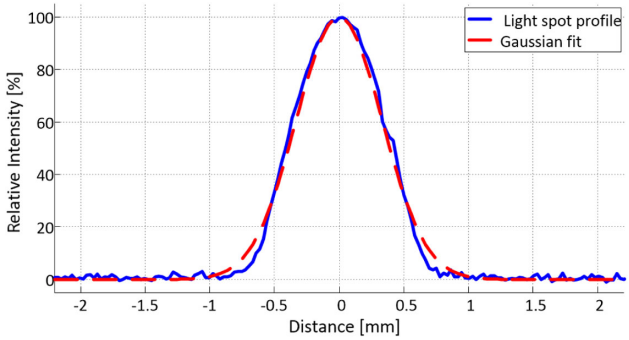

Fig. 19. Relative intensity of the light spot measured at 81 ± 12 mm with acquisition time of 5 µs. Measured light spot diameter is 1.67 ± 0.05 mm.

The light spot characterization shows that the measured divergence angle α matches the values obtained using surface profilometry. The value of α lies on the higher side of the range. However, the measurement uncertainty is high due to the impossibility to directly measure distance z. The lens was designed excluding the 50% margin to reduce the wafer topography.

With the numerical aperture of the waveguide higher than 0.38, during the CCD image acquisition with a longer time, the portion of light not collected by the lens could be amplified, and bigger spot diameters could be measured. Comparison of the lens diameter from Fig. 18(b) (50 µs acquisition time) and Fig. 19 (5 µs acquisition time) shows the measured light spot diameter can be up to 13% lower. However, the lower spot diameter can also be a result of low camera sensitivity.

5. CONCLUSION

This work presented a description of a fully integrated photonics platform that potentially enables a single-chip OCT system and reduces complexity of standard optical alignment. It consists of a monolithically integrated Si microlens, waveguides, and 45° mirror facet. The system was designed to accommodate the needs for MEMS actuator fabrication and to exclude any possible topographical for photolithographical processing. The fabrication process was optimized to reduce the number of film depositions. Yet, additional protective layers had to be applied to preserve the surface from accidental wafer scratches during wafer handling. The fully integrated photonic platform was successfully fabricated and characterized.

The achieved lens geometry yields a divergence angle of 0.63°, which is considered as low. Moreover, the lens does not influence the power distribution of the light, i.e., it preserves the Gaussian profile from the waveguide. The optical characterization shows in total 1–2 dB higher optical losses compared to commercially available straight waveguides. The mirror facets show maximal losses below 1 dB, while the lens does not introduce any optical losses. The whole interferometer has losses of around 14 dB in the measurement arm and 23 dB in the reference arm. Alignment accuracy of all components is within 15 nm.

The presented photonic platform demonstrates the feasibility of a single-chip OCT system. Moreover, the photonic platform is suitable for other imaging and metrology applications such as lidar, optical profilometry, confocal microscopy, etc. The presented work provides the premise for low-cost and small-footprint fabrication of such a technological solution.

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REFERENCES

1. T. Diepgen and V. Mahler, "The epidemiology of skin cancer," Br. J. Dermatol. **146**, 1–6 (2002).
2. F. Erdmann, J. Lortet-Tieulent, J. Schüz, H. Zeeb, R. Greinert, E. W. Breitbart, and F. Bray, "International trends in the incidence of malignant melanoma 1953-2008—are recent generations at higher or lower risk?" Int. J. Cancer **132**, 385–400 (2013).
3. V. Madan, J. T. Lear, and R.-M. Szeimies, "Non-melanoma skin cancer," Lancet **375**, 673–685 (2010).
4. T. Gambichler, V. Jaedicke, and S. Terras, "Optical coherence tomography in dermatology: technical and clinical aspects," Arch. Dermatol. Res. **303**, 457–473 (2011).
5. J. M. Schmitt, M. J. Yadlowsky, and R. F. Bonner, "Subsurface imaging of living skin with optical coherence microscopy," Dermatology **191**, 93–98 (1995).
6. A. F. Fercher, W. Drexler, C. K. Hitzenberger, and T. Lasser, "Optical coherence tomography—principles and applications," Rep. Prog. Phys. **66**, 239–303 (2003).
7. G. Yurtsever, P. Dumon, W. Bogaerts, and R. Baets, "Integrated photonic circuit in silicon on insulator for Fourier domain optical coherence tomography," Proc. SPIE **7554**, 75541B (2010).
8. E. Margallo-Balbás, M. Geljon, G. Pandraud, and P. J. French, "Miniature 10 KHz thermo-optic delay line in silicon," Opt. Lett. **35**, 4027–4029 (2010).
9. B. I. Akca, B. Považay, A. Alex, K. Wörhoff, R. M. de Ridder, W. Drexler, and M. Pollnau, "Miniature spectrometer and beam splitter for an optical coherence tomography on a silicon chip," Opt. Express **21**, 16648–16656 (2013).
10. P. Struk, S. Bargiel, Q. A. A. Tanguy, F. E. G. Ramirez, N. Passilly, P. Lutz, O. Gaiffe, H. Xie, and C. Gorecki, "Swept-source optical coherence tomography microsystem with an integrated Mirau interferometer and electrothermal micro-scanner," Opt. Lett. **43**, 4847–4850 (2018).
11. V. D. Nguyen, N. Weiss, W. Beeker, M. Hoekman, A. Leinse, R. G. Heideman, T. G. van Leeuwen, and J. Kalkman, "Integrated-optics-based swept-source optical coherence tomography," Opt. Lett. **37**, 4820–4822 (2012).

12. G. Yurtsever, N. Weiss, J. Kalkman, T. G. van Leeuwen, and R. Baets, "Ultra-compact silicon photonic integrated interferometer for swept-source optical coherence tomography," Opt. Lett. **39**, 5228–5231 (2014).
13. M. Sagmeister, G. Koppitsch, P. Muellner, S. Nevlacsil, A. MaeseNovo, R. Hainberger, D. Seyringer, and J. Kraft, "Monolithically integrated, CMOS-compatible SiN photonics for sensing applications," in *Multidisciplinary Digital Publishing Institute Proceedings* (2018), Vol. **2**, p. 1023.
14. S. Schneider, M. Lauermann, P.-I. Dietrich, C. Weimann, W. Freude, and C. Koos, "Optical coherence tomography system mass-producible on a silicon photonic chip," Opt. Express **24**, 1573–1586 (2016).
15. MEDLUMICS, "Optical beam scanner," U.S. patent 9690093B2 (27 June 2017).
16. K. Solehmainen, T. Aalto, J. Dekker, M. Kapulainen, M. Harjanne, K. Kukli, P. Heimala, K. Kolari, and M. Leskela, "Dry-etched silicon-on-insulator waveguides with low propagation and fiber-coupling losses," J. Lightwave Technol. **23**, 3875–3880 (2005).
17. C. Strandman, L. Rosengren, H. G. A. Elderstig, and Y. Backlund, "Fabrication of 45/spl deg/mirrors together with well-defined v-grooves using wet anisotropic etching of silicon," J. Microelectromech. Syst. **4**, 213–219 (1995).
18. A. Jovic, G. Pandraud, K. Zinoviev, J. L. Rubio, E. Margallo, and P. M. Sarro, "Fabrication process of Si microlenses for OCT systems," Proc. SPIE **9888**, 98880C (2016).
19. T. T. Aalto, M. Harjanne, M. Kapulainen, P. Heimala, and M. J. Leppihalme, "Development of silicon-on-insulator waveguide technology," Proc. SPIE **5355**, 81–95 (2004).
20. K. Solehmainen, T. Aalto, J. Dekker, M. Kapulainen, M. Harjanne, and P. Heimala, "Development of multi-step processing in silicon-on-insulator for optical waveguide applications," J. Opt. A **8**, S455–S460 (2006).
21. M. A. Green, "Self-consistent optical parameters of intrinsic silicon at 300k including temperature coefficients," Solar Energy Mater. Sol. Cells **92**, 1305–1310 (2008).
22. E. Hecht, *Optics* (Pearson/Addison-Wesley, 2002).
23. A. Jovic, G. Pandraud, N. S. Losilla, J. Sancho, K. Zinoviev, J. L. Rubio, E. Margallo-Ballbas, and P. M. Sarro, "A mems actuator system for an integrated 3-D optical coherent tomography scanner," J. Microelectromech. Syst. **27**, 259–268 (2018).
24. F. Gao, S. Ylinen, M. Kainlauri, and M. Kapulainen, "Smooth silicon sidewall etching for waveguide structures using a modified Bosch process," J. Micro/Nanolithogr. MEMS MOEMS **13**, 013010 (2014).
25. M. Morita, T. Ohmi, E. Hasegawa, M. Kawakami, and M. Ohwada, "Growth of native oxide on a silicon surface," J. Appl. Phys. **68**, 1272–1281 (1990).
26. D. Resnik, D. Vrtacnik, U. Aljancic, and S. Amon, "Micromachined crystal plane on (100) and (110) silicon for optical mirror applications," Proc SPIE **5276**, 489–497 (2004).
27. D. Resnik, D. Vrtacnik, U. Aljancic, M. Mozek, and S. Amon, "The role of triton surfactant in anisotropic etching of {110} reflective planes on (100) silicon," J. Micromech. Microeng. **15**, 1174–1183 (2005).