Improving the Detection of Undefined State Faults in FinFET SRAMs

Cardoso Medeiros, G.; Fieback, M.; Copetti, Thiago; Gebregiorgis, A.B.; Taouil, M.; Bolzani Poehls, L. M.; Hamdioui, S.

DOI
10.1109/DTIS53253.2021.9505130

Publication date
2021

Document Version
Accepted author manuscript

Published in
International Conference on Design & Technology of Integrated System in Nanoscale Era (DTIS)

Improving the Detection of Undefined State Faults in FinFET SRAMs

G. C. Medeiros[1], M. Fieback[1], T. S. Copetti[2], A. Gebregiorgis[1], M. Taouil[1], L. B. Poehls[2,3], S. Hamdioui[1]
[1]Computer Engineering Laboratory, Delft University of Technology, The Netherlands
[2]IDS, RWTH Aachen University, Germany, [3]EASE, PUCRS, Brazil
Email: {G.CardosoMedeiros, S.Hamdioui}@tudelft.nl

***Abstract*—Manufacturing defects in FinFET SRAMs can cause hard-to-detect faults such as Undefined State Faults (USFs). Detection of USFs is not trivial, as they may not lead to incorrect functionality. Nevertheless, undetected USFs may have a severe impact on the memory's quality: they can cause random read outputs, which might lead to test escapes and no-trouble-found devices later when the device is already in the field, as well as compromise the circuit's quality by reducing the memory cell's Static Noise Margin (SNM). Therefore, the detection of USF is critical. This paper proposes a test solution to improve the detection of USFs in FinFET SRAMs. To achieve this, we first analyze the impact of USFs on the cell's SNM and bitline swing during read operations. Then, we perform an experimental study of stress conditions' (SCs) impact on sensitizing and detecting USFs. Finally, we propose a dedicated Design-For-Testability (DFT) scheme for FinFET SRAMs to detect such faults. This scheme introduces a small area overhead while significantly improving USF detection. Hence, using the proposed DFT leads to fewer test escapes and higher-quality FinFET SRAMs.**

***Index Terms*—Memory Testing, Undefined State, SRAM, FinFET, DFT**

I. Introduction

During the manufacturing of FinFET devices, they can be affected by manufacturing defects such as opens in fins [1] and oxide pinholes [2]. In FinFET SRAMs, these defects cause Hard-to-Detect faults [3] such as *Undefined State Faults* (USFs), i.e., the cell's storing nodes are not in V_{DD} or GND [4]. This imbalance prevents the cell from correctly discharge the bitlines (BLs) during a read operation, leading to random read outputs and test escapes [5]. Furthermore, it also reduces the cell's Static Noise Margin (SNM) (i.e., the maximum noise the cell can endure before destroying its content), affecting its reliability [6]. USFs can only be detected if the random read output does not match the cell's expected value or if the cell's content flips somehow. Nevertheless, both methods are inefficient as only part of the random read outputs will lead to incorrect outputs [7], and the cell's content will only be destroyed if the cell suffers from a retention fault alongside the USF [8]. Otherwise, the USF is not detected, compromising the device's functionality. Therefore, dedicated methodologies are required to reduce USF test escapes and improve the quality and reliability of FinFET memories [9].

USF detection is not trivial. March algorithms such as SS and FFDD [10, 11] can only detect USFs that will either lead to an incorrect read output caused by a Random Read Fault [7] or if the cell's content was destroyed due to a retention fault [8]. Therefore, complex solutions (e.g., stress tests and *Design-for-Testability* (DFT) circuits) must be used to detect USFs. A common approach is to change the write operation stress conditions, e.g., write operations with reduced write time or supply voltage [12]. A weaker write driver [13] can also be used to detect cells in undefined states. However, both approaches have limitations, such as the need for extended write operations, which requires modifying the memory's timing scheme. Furthermore, they were implemented in older CMOS technologies [13], and emerging memories with unique mechanisms [12]. Hence, a dedicated DFT to detect USFs in FinFET SRAMs is still missing.

This paper addresses these problems by proposing a test solution to reduce USF test escapes. First, we analyze the influence of USF on the cell's SNM and BL swing and show that USF-induced disturbances on storing nodes will negatively impact these parameters, leading to cells with reduced SNM and consequently impaired reliability and cells that are more likely to cause Random Read Faults. We then perform simulation experiments under various *stressing conditions* (SCs) to identify which lead to the highest USF sensitization and detection. Finally, we evaluate existing test solutions that focus on USFs and, based on their limitations, propose a new DFT scheme to maximize USF detection in FinFET SRAMs. Compared to the state of the art, this DFT significantly improves USF detection rate with no yield loss, leading to higher-quality FinFET SRAMs.

The main contributions of this paper are as follows:

- The modeling of USF's impact on SNM and BL swing.
- An experimental analysis on USF detection.
- The evaluation of existing USF-focused test solutions and their applicability to FinFET SRAMs.
- The implementation, validation, and evaluation of a new DFT scheme for USFs in FinFET SRAMs.

This paper is organized as follows. Section II models the impact of USF on memory's parameters. Section III explores the USF's detection dependency on SCs. Section IV analysis existing test solutions for USFs and, based on their limitations, proposes a new DFT to improve the detection of USFs. Section V presents a brief discussion on the DFT and its limitations. Finally, Section VI concludes the paper.

This work is supported by European Union's Horizon 2020 Research and Innovation through RESCUE project under grant 722325.

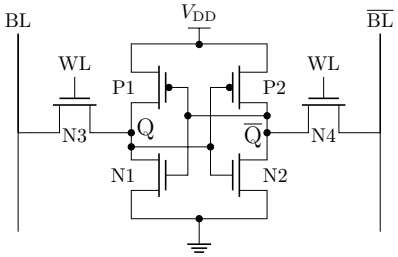


Figure 1. A 6T SRAM cell.

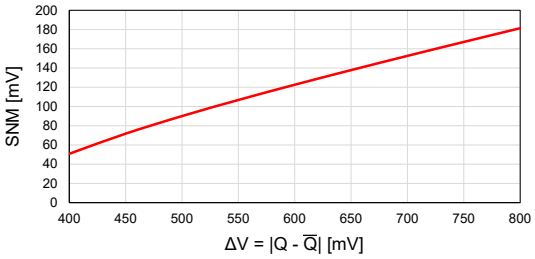


Figure 2. Impact of ΔV on the cell's SNM.

II. USFs and their Impact

A. Causes & Definition

SRAMs are volatile memories formed by a cell array and peripheral circuitry. The cell array consists of rows and columns of 6T memory cells; each cell (Fig. 1) is composed of two cross-coupled transistors (P1 & N1 and P2 & N2) and two access transistors (N3 and N4) connected to a *word line* (WL) and a pair of *bitlines* (BL and $\overline{BL}$). The cell's content is stored in Q while $\overline{\text{Q}}$ stores the opposite voltage. The peripheral components (decoders, *write drivers* (WDs), sense amplifiers) provide write and read capabilities to the SRAM. SRAMs can be designed using FinFET devices. During their manufacturing process, small particles and lithography inconsistencies can result in defective structures [14], e.g., partial opens, damaged fin structure [1, 15]. These defects may impact the cell's storage nodes, leading to voltage deviations on Q and $\overline{\text{Q}}$. An *Undefined State Fault* (USF) [4] occurs when these voltages deviations severely impact the voltage difference between the storage nodes $\Delta V = |Q - \overline{Q}|$, which should be V_{DD}. This undefined state may impact other memory's parameters, such as the *static noise margin* (SNM) or BL swing.

The Fault Primitive notation [16] describes USFs as faults in which the fault element (F) is expressed as **U**. For example, $\langle 1w0/U/-\rangle$ denotes a write '0' operation in a cell that is currently storing '1'. However, instead of undergoing a transition, the cell's state ends up undefined, i.e., Q and $\overline{\text{Q}}$ are deviated from GND and V_{DD} respectively. Because USF detection is not guaranteed by performing a sequence of write and read operations, they are classified as Hard-to-Detect faults [17]. If not detected, USFs become test escapes, a known cause for no-trouble-found components [5]. Furthermore, they may also compromise the memory's reliability once used in the field due to the reduced SNM. [6]. Therefore, detection of USFs is critical to assure high-quality FinFET SRAMs.

B. USF's Impact on SNM

An SRAM cell can withstand a certain level of exterior interference, such as white, flicker, and temperature noise, α particles, and cross-talk. This noise level, i.e., the SNM, is determined based on the cell's technology and its sizing ratios between pull-ups, pull-downs, and access transistors. More specifically, the SNM can be defined as [18]:

$$\text{SNM} = V_{TH} - \left(\frac{1}{k+1}\right)\left(\frac{V_{DD} - \frac{2r+1}{r+1}V_{TH}}{1+\frac{r}{k(r+1)}} - \frac{V_{DD} - 2V_{TH}}{1 + k\frac{r}{q} + \sqrt{\frac{r}{q}\left(1 + 2k + \frac{r}{q}k^2\right)}}\right) \quad (1)$$

where r is the ratio between pull-down and access transistors, q is the ratio between pull-down and pull-up transistors, V_{TH} is the threshold voltage, and

$$k = \left(\frac{r}{r+1}\right)\left(\sqrt{\frac{r+1}{r+1-V_s^2/V_r^2}} - 1\right),$$
$$V_s = V_{DD} - V_{TH},$$
$$V_r = V_s - \left(\frac{r}{r+1}\right).$$

USF's impact on the cell's SNM can be estimated by replacing V_{DD} in Eq. 1 for ΔV, as shown in Fig. 2. For this analysis, it was assumed a cell ratio of 2:2:1 for pull-down, access, and pull-up transistors, respectively, V_{DD} = 0.8 V, and V_{TH} = 0.11 V [19]. It is clear that the smaller the ΔV, the smaller the cell's SNM. Accordingly, a cell with smaller SNM is more likely to suffer upsets from exterior noises such as noise and radiation, i.e., memory cells with reduced reliability. Thus, it is essential to identify and flag these compromised cells, as they could severely impact high-demanding applications such as automotive and aerospace.

C. USF's Impact on Bitline Swing

During a read operation, the BL discharge rate depends on many factors, such as the BL capacitance, the access and pull-down transistors' sizing, and the voltage on the storing nodes. Hence, deviations on Q and $\overline{\text{Q}}$ may affect a cell's ability to discharge its BLs and impact the cell's BL swing, which is the voltage difference between a BL pair when the SA is enabled, i.e., BL swing = $|BL - \overline{BL}|$. A reduced BL swing may result in a random output, i.e., either '0' or '1', a faulty behavior known as *Random Read Faults* (RRFs) [4]. It is statistically expected that some RRFs will lead to a failure, i.e., the SA will not output the expected logic value, thereby enabling RRF detection. The remaining will lead to correct outputs and consequently test escapes.

The impact of BL swing on RRF detection has recently been discussed [7]. Nevertheless, the impact of USFs on BLs'

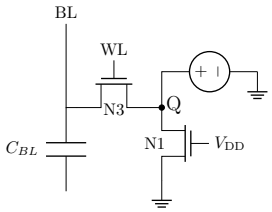


Figure 3. BL discharging circuit.

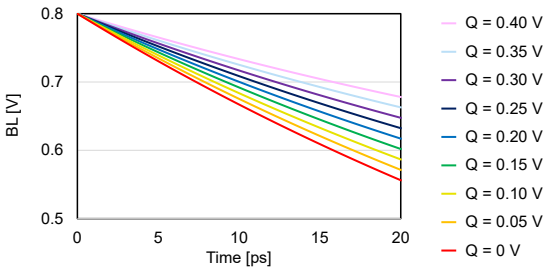


Figure 4. BL Discharge based on the voltage on Q.

discharge has not been explored yet. Thus, we investigate how voltage deviations on the discharge node disrupt the cell's discharge capabilities by calculating the voltage on the BL capacitor during a read operation. The simplified version of the cell's discharging circuit is shown in 3. A voltage source is directly connected to the storing node Q to represent the USF's effect on the storage node; furthermore, we assume that BL is pre-charged to V_{DD} and $\overline{\text{Q}}$ is not affected (i.e., $\overline{\text{Q}}$ = V_{DD}). The voltage on BL is calculated by estimating the charge in the capacitor over time [20]:

$$V_{BL}(t) = \frac{C_{BL}V_Q - Ke^{-t/C_{BL}R}}{C_{BL}},$$

where R is the resistance of N3, and

$$K = C_{BL}V_Q - Q_0,$$

$$Q_0 = V_{BL(t=0)}C_{BL}.$$

Fig. 4 shows the BL discharge for a period of 20ps considering R = 3K Ω. Clearly, the introduced voltage on the storing node has a significant impact on the final BL swing. This analysis assumed that only the discharging node is impacted; voltage deviations on $\overline{\text{Q}}$ could also have impacted $\overline{BL}$ i.e., $\overline{BL} < V_{\text{DD}}$, which would affect the BL swing even further.

Based on the analysis of USF's impact on both the SNM and BL swing, we conclude the following:

- USFs impact the cell's parameters rather than its functionality. Nonetheless, this parametric impact may lead to functional faults.
- USFs can lead to both test and reliability issues: the first by hindering the cell's ability to develop a BL swing, thus leading to random read outputs, and the second by reducing the cell's SNM, making the cell vulnerable to outside noise and more likely to suffer upsets.
- Without dedicated design-for-testability (DFT) circuits, USFs can only be detected if they (1) lead to an incorrect output generated due to an RRF, or (2) suffer an upset caused by noise.

III. USF Detection Dependency on SCs

This section estimates the impact of *stress conditions* (SCs) on the detection of USF. We first introduce a classification of SCs, followed by a description of the simulation setup, and finally, the detection results.

A. Classification of Stress Conditions

SCs categorized into two classes: algorithm-related and environment-related [21]. Algorithm-related stresses specify the sequence of operations and addresses. Examples of algorithm-related SCs are as follows:

- **Base Test (BT)**: A BT is a sequence of operations (reads and writes) applied to a memory cell.
- **Address Order (AO)**: The AO is the address sequence generated by an addressing method (e.g., increasing (⇑), decreasing (⇓), binary, hamming distance, H2/H3/HN1 [22]) that defines how the algorithm accesses addresses.
- **Address Direction (AD)**: The AD indicates how the AO is applied considering rows and columns. The most common ADs are fast-row and fast-column [21].
- **Data Background (DB)**: DB is the pattern of ones and zeros as seen in the memory array. The most known DBs are Solid, Checkerboard, and Row/Column Stripe [21].

Environment-related SCs use additional stress sources to change the operating conditions of the memory. These include [21], but are not limited to:

- **Voltage Stress** in the entire circuit (e.g., changing the supply voltage) or a peripheral (e.g., write driver, SA).
- **Timing Stress** in the entire circuit (e.g., changing frequency) or specific components (e.g., write driver, SA) to change memory operations' timing.
- **Temperature Stress** by either increasing or reducing the temperature from its nominal value.

B. Simulation Setup

Memory model: the netlist is described using the predictive technology model (PTM) 14 nm FinFET SPICE library [23]. The array comprises 128 rows and 64 columns; each column has a write driver, SA, and prechargers. Capacitive loads are applied to BLs and word lines to emulate a 1 kB memory. The memory operates on a nominal clock frequency of 2 GHz and contains a timing circuit to generate control signals.

Injected defects: Twenty-eight single-cell resistive defects have been injected in the cell, as shown in Fig. 5. They are either *Resistive-Open* (RO), *Resistive-Short* (RS), or *Resistive-Bridge* (RB) defects [24].

Experiments: Each defect was swept with increasing resistances to identify USFs. Each simulation scenario (i.e., using stress conditions X and injecting defect Y of size Z) was simulated 100 times using MC simulations. PV effects are modeled using Pelgrom's model [25] and simulated using a voltage source on the transistor's gate. Measure commands are used to check the voltage on the cell's storage nodes and read outputs.

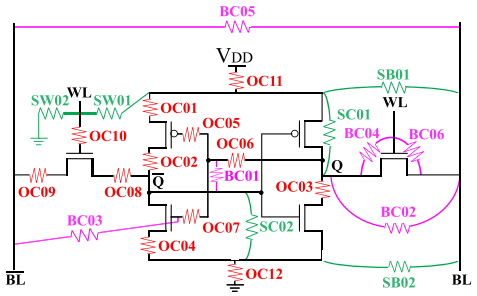


Figure 5. A 6T cell and the injected resistive defects: opens, shorts, bridges.

C. Detecting USFs with Algorithm-Related SCs

We focus on USF detection only; the SCs discussed below may impact other types of faults differently. Detection of USF relies on two steps: (1) sensitizing the USF and (2) reading the cell in an undefined state. Step 1 involves manipulating the cell's content to trigger an undefined state. Experiments have shown that USFs can be sensitized by either applying transition write operations or read operations. After the sensitizing operation, the voltage deviation on the faulty storing node may slowly decay, stay in the same value, or, in the case of read operations, increase and eventually lead to a dynamic read destructive fault. Step 2 involves reading the faulty cell's content; since the cell is in an undefined state, the read operation may lead to a random output, i.e., an RRF. Therefore, any SCs that improve RRF detection should be used as well. Based on the experiments, we conclude the following:

- The most efficient sensitizing BTs are 0w1, 1w0, 0r0, and 1r1. A read operation should follow to try to detect the undefined state, even though RRFs may occur.
- AO and AD did not lead to an increase in USF sensitization nor detection.
- DB did not lead to an increase in USF sensitization. Nevertheless, Checkerboard DB significantly improves RRF detection [7], and thus should be used when targeting USFs as well.
- Defects that led to USFs but no RRFs cannot be detected using only algorithm-related SCs.
- Defects that led to USFs and RRFs can be detected using algorithm-related SCs, but the detection rate will be very small.

Four defects have sensitized USFs: OC01, OC02, OC11, and BC01. In all cases, it was observed that after the USF was sensitized, the SNM and the BL swing have been significantly reduced. We exemplify this behavior by analyzing the impact of OC01, which sensitize a USF after a transition write. Nevertheless, this defect will also lead to a significantly reduced SNM and BL swing. The impact on cell's SNM is illustrated in Fig. 6, which shows the ΔV and the cell's SNM right after the write transition. We can see a clear relation between the cell's ΔV and SNM, and that the cell's SNM is significantly reduced from its original value, meaning that this cell is more likely to suffer upsets from exterior noise. Thus, this faulty cell must be flagged during test.

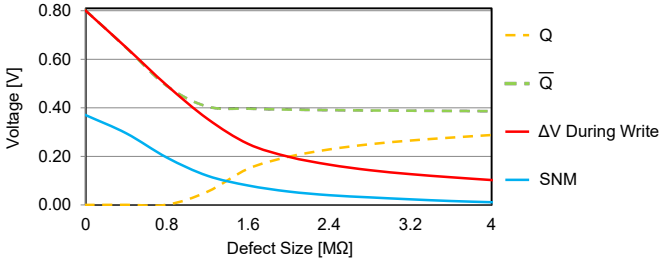


Figure 6. Impact on SNM due to defect OC01 after a transition write.

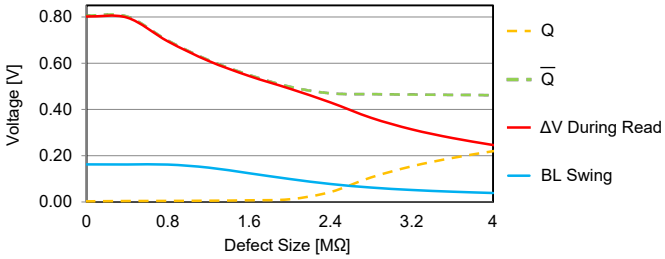


Figure 7. Impact on BL swing due to defect OC01.

The only way to detect this cell is by reading the cell. Nevertheless, as the cell is in an undefined state, it fails to properly discharge the cell, as illustrated by Fig. 7. The figure shows the cell's ΔV and BL swing during a read operation that followed the transition write operation that triggered the USF. Again, we can see a clear relation between ΔV and BL swing. Furthermore, by the point of OC01 = $4\text{M}\Omega$, the read operation did not detect any fault. Thus, more complex SCs must be used to increase the detection of USFs.

D. Detecting USFs with Environment-Related SCs

Environment-related SCs set the memory's operating conditions. Changing these conditions will shift the defect size range in which faults are sensitized. Regarding USF detection, supply voltage has the most significant impact as it directly changes the maximum ΔV, e.g., a reduced supply voltage leads to a reduced voltage difference between Q and $\overline{\text{Q}}$. Frequency and temperature will also impact the cell's SNM and BL swing; reducing the frequency shortens the WL enable time, leading to a reduced BL swing due to less time to discharge BLs, and to write transition faults due to less time to flip the cell's content. Nevertheless, frequency and temperature will not directly impact the cell's ΔV and thus will not impact the sensitization of USFs, only its detection through other means, e.g., RRFs and transition faults. Based on the experiments using different types of SCs, we conclude the following:

- Reducing supply voltage increases the sensitization of USFs as it diminishes the cell's ΔV and hinders both the SNM and BL swing, thus increasing the detection of USFs through RRFs.
- Changing temperature or frequency does not change the sensitization of USFs, but instead changes the detection of other types of faults (e.g., RRFs and failed transitions), which may lead to the detection of USFs.

IV. Test Solutions to Detect USFs

A. Existing Solutions

Different test solutions have been proposed to detect USFs or faulty behaviors present in USFs. Some works have focused on Data Retention faults [26], i.e., the cell's content flip after some time. Nevertheless, focusing on Data Retention faults will not fully cover USFs as not all USFs lead to a bit-flip. Other solutions focused on using DFT circuits to apply additional environment-related SCs such as frequency and voltage. These techniques, e.g., Short Write Time-Based, and Low Write Voltage-Based DFT circuits [12, 27], have been applied to emerging memories. However, such techniques are unrealistic for FinFET SRAMs as the write time and the supply voltage in these memories are already aggressively scaled-down. Therefore, reducing it even further could lead to yield loss, i.e., fault-free cells being flagged as faulty. Furthermore, changing the memory's timing and supply voltage scheme may significantly increase the DFT's hardware complexity.

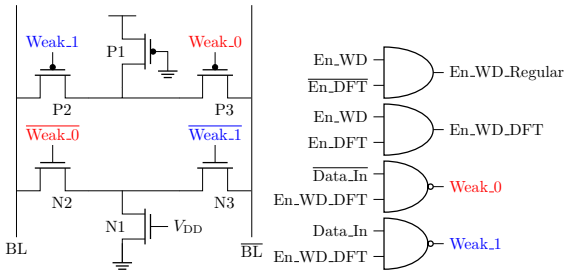
A well-known strategy to detect USFs is to use weak-write mode [13], i.e., a weaker write driver is activated during test mode instead of the standard write driver. This weak write driver can force a new value in these cells but fails to force new values in fault-free cells. USFs are then detected by checking which cells have flipped after a weak write operation. While efficient, this test solution still presents limitations, such as prolonged write operations and the additional write driver. To evaluate if this test solution is still applicable to FinFET SRAMs, we have adapted the circuit in [13] to our 14nm FinFET SRAM. We were unsuccessful in using this weak driver to write cells in undefined states, even when over-designing it (i.e., using a high amount of fins in the FinFET transistors). Therefore, a dedicated test solution for USFs in FinFET SRAMs is still missing.

B. Proposed DFT

The DFT technique proposed in this work uses the previously-discussed concept of weak-write test mode to target USFs; it uses a similar organization as the circuit in [13] to weakly force a new value into the cell. The DFT's organization and control signals are illustrated in Fig. 8. Our proposed DFT differentiates from the one in [13] in the following aspects:

- The proposed DFT does not require additional write time, thus avoiding the overhead related to changing the memory's time scheme.
- All pull-up transistors are PMOS devices instead of NMOS devices.
- N1's gate is V_{DD}, rather than its source.

Only one additional signal is necessary to activate the DFT. Furthermore, four additional logic gates are included to generate the appropriate control signals. The detection principles of the proposed DFT scheme are the same as the weak write test mode, i.e., flip the content of weak cells and not flip the content of defect-free cells. Thus, detection is enabled by performing a weak write on the cell and then reading it to check its content. Furthermore, the stress applied during the additional read operation is adjusted to improve the detection of RRFs, i.e., use a checkerboard DB stress to manipulate the output latch to influence the sense amplifier's amplification phase [7].



(a) Weak Write Driver. (b) DFT Control.

Figure 8. DFT Organization.

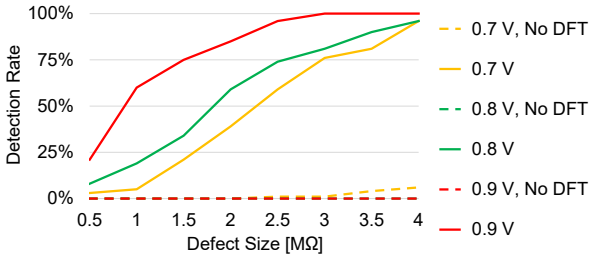


Figure 9. DFT Detection rate for detect OC01.

C. Detection Results

Simulations have been performed in the same manner as described in Section III-B; each scenario (i.e., injecting defect Y of size Z) was simulated 100 times using MC simulations. Measure commands are used to check read outputs and define whether the USF was detected or not. Then, an average detection rate for each scenario is estimated.

Fig. 9 shows the DFT's OC01 detection; algorithm-related SCs have been appropriately adjusted to maximize the detection of USFs and RRFs. Without the DFT, detecting USFs is only possible if it also triggers an incorrect read output due to an RRF. We can see that detection is minimal, with only 6% at OC01 = 4MΩ and V_{DD} = 0.7V; coming back to Figs. 7 and 6, both the SNM and BL swing are already very much impacted at this point. A considerable increase in detection rate is observed when using our DFT, with the highest detection obtained with V_{DD} = 0.9 V.

Finally, Fig. 10 illustrates the DFT's BC01 detection rate. Again, SCs have been set to maximize the detection of USFs and RRFs. While detecting BC01 is easier than OC01, we can see that the DFT still provided significant detection gain by detecting weak cells that lead to BL swing and SNM deviations. Overall, the DFT proved to be efficient in detecting defects that lead to USF and its related faulty effects, such as a reduced SNM and BL swing. Furthermore, no yield loss was observed during the experiments, i.e., the DFT did not flag a fault-free cell as faulty, thus confirming that the proposed test solution is indeed an appropriate approach to detect USFs in FinFET SRAMs.

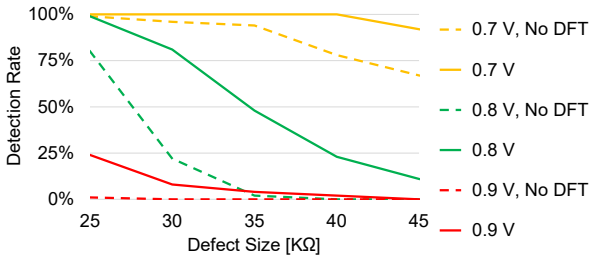


Figure 10. DFT Detection rate for defect BC01.

V. Discussion

Applicability: the costs of increasing USF detection may not always be justified. Nevertheless, for critical applications such as automotive and aerospace, the requirement of 0 defective parts per million justifies additional DFT circuits. Additionally, DFT solutions that improve RRF detection [7] can be used alongside to boost fault detection ever further. Furthermore, the DFT can also be used during the memory's characterization to identify the occurrence of USFs and improve memory yield before mass production.

Applicability to scaled FinFET memories: to the best of our knowledge, no public works have investigated USFs in deep-scaled memories, e.g., nano-sheets in 7 and 5 nm. However, USFs will likely be as relevant in scaled memories as in 14 nm memories; with the scaling down of supply voltage and increased parasitics, even slight environmental noise may lead to upsets. Thus, our DFT could be used in smaller-node technologies if USFs are ever reported in such circuits.

Calibration Capabilities: even though no yield loss was observed during our experiments, it is still possible to calibrate the DFT. Run-time calibration can be achieved using different SCs to minimize detection. Post-silicon calibration is possible by changing the DFT timing to adjust when the DFT is enabled; this can be implemented with a dynamic delay selector on the control gates, like the calibration in [17].

Overhead: the overhead introduced by the proposed DFT scheme is very small. The DFT's control comprises only four 2-input gates, thus negligible compared to other peripheral circuitry. Furthermore, the additional write driver (six transistors) introduced into each column is also negligible as it roughly represents the same size as one 6T. The DFT does require an additional sequence of operations to achieve USF detection; however, this additional sequence consists of only four operations maximum, i.e., sensitize USF from '1', read cell, sensitize USF from '0', read cell. Nevertheless, the gains obtained from using the DFT justify the additional test time.

Drawbacks & Limitations: the main drawback is the extra WD, which requires adapting the memory's layout. Moreover, the DFT's main limitation is its lack of parametric testing. As it is a functional test solution, it still requires an incorrect functional behavior to detect USFs. To fully detect all parametric deviations on the cell's storage nodes and ΔV, more complex parametric test solutions, such as monitoring the cell's current flow, might be required. Nevertheless, further analysis on this type of test solution is still required.

VI. Conclusion

We have presented an analysis of *Undefined State Faults* (USF) in FinFET SRAMs. We have shown that these faults impact the voltage on the cell's storage nodes, leading to a reduced *static noise margin* (SNM) and *bitline* (BL) swing. USF detection is very complex as it relies on detecting other faulty behaviors such as random read faults. Furthermore, we have proposed a dedicated DFT scheme to detect USFs by flipping weak cells' contents. The DFT significantly improves USF coverage, thus leading to reduced test escapes and higher quality FinFET SRAMs.

References

[1] Y. Liu *et al.*, "On modeling faults in FinFET logic circuits," in *Int. Test Conf.* IEEE, nov 2012.

[2] R. Dibaj *et al.*, "Comprehensive Investigation of Gate Oxide Short in FinFETs," in *VLSI Test Symp.* IEEE, apr 2017.

[3] M. Fieback *et al.*, "Device-aware test: A new test approach towards DPPB," in *Int. Test Conf.*, 2019.

[4] S. Hamdioui *et al.*, "An experimental analysis of spot defects in SRAMs: realistic fault models and tests," in *Asian Test Symp.* IEEE, 2000.

[5] S. Davidson, "Towards an understanding of no trouble found devices," in *IEEE VTS 2005*, may 2005.

[6] H. Villacorta *et al.*, "FinFET SRAM hardening through des. and technol. param. considering process var." in *RADECS 2013*. IEEE, sep 2013.

[7] G. C. Medeiros *et al.*, "Detecting random read faults to reduce test escapes in FinFET SRAMs," in *2021 IEEE Eur. Test Symp. (ETS)*, May 2021.

[8] G. C. Medeiros *et al.*, "Hard-to-Detect Fault Analysis in FinFET SRAMs," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2021.

[9] M. Shah *et al.*, "A Qual. and Rel. Driven DFT and DFR Strategy for Automot. and Ind. Markets," in *VLSI Test Symp.* IEEE, apr 2019.

[10] S. Hamdioui *et al.*, "March SS: a test for all static simple RAM faults," in *Int. Workshop on Memory Technol., Des. and Test*. IEEE, jul 2002.

[11] G. Harutyunyan *et al.*, "Memory Physical Aware Multi-Level Fault Diagnosis Flow," *IEEE Tran. on Emerging Topics in Computing*, 2018.

[12] S. Hamdioui *et al.*, "Testing open defects in memristor-based memories," *IEEE Transactions on Computers*, 2015.

[13] A. Meixner *et al.*, "Weak write test mode: an SRAM cell stability design for test technique," in *Int. Test Conf.*, nov 1997.

[14] T. Matsukawa *et al.*, "Comprehensive analysis of variability sources of FinFET characteristics," *Symp. on VLSI Technol.*, jun 2009.

[15] F. Forero *et al.*, "Modeling and Detectability of Full Open Gate Defects in FinFET Technology," *IEEE Tran. on VLSI Systems*, 2019.

[16] A. J. van de Goor *et al.*, "Functional memory faults: a formal notation and a taxonomy," in *Asian Test Symp.* IEEE, apr 2000.

[17] G. C. Medeiros *et al.*, "A DFT scheme to improve coverage of hard-to-detect faults in FinFET SRAMs," in *Des., Test, and Automation in Eur.* IEEE, mar 2020.

[18] E. Seevinck *et al.*, "Static-noise margin analysis of mos sram cells," *IEEE Journal of Solid-State Circuits*, 1987.

[19] L. Darsen Duane *et al.*, "Compact Models for Future Generation CMOS," Ph.D. dissertation, Univerity of Califionia, Berkeley, 2011.

[20] R. L. Boylestad *et al.*, *Electronic devices and circuit theory*. Pearson, 2013.

[21] A. J. van de Goor *et al.*, "Detecting faults in the peripheral circuits and an evaluation of SRAM tests," in *Int. Conf. on Test*. IEEE, oct 2004.

[22] S. Hamdioui *et al.*, "An investigation on capacitive coupling in RAM address decoders," in *Int. Design and Test Workshop*. IEEE, dec 2007.

[23] Nanoscale Integration and Modeling (NIMO), "Predictive Technology Model (PTM)," 2012. [Online]. Available: http://ptm.asu.edu/

[24] S. Hamdioui *et al.*, "Memory fault modeling trends: A case study," *Journal of Electronic Testing: Theory and Applications*, jun 2004.

[25] M. J. M. Pelgrom *et al.*, "Matching properties of mos transistors," *IEEE Journal of Solid-State Circuits*, 1989.

[26] L. Dilillo *et al.*, "Data retention fault in sram memories: analysis and detection procedures," in *23rd IEEE VLSI Test Symp. (VTS'05)*, 2005.

[27] N. Z. Haron *et al.*, "Dft schemes for resistive open defects in rrams," in *2012 Design, Automation & Test in Europe (DATE)*, 2012.