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## A Self Bias-flip Piezoelectric Energy Harvester Array without External Energy Reservoirs achieving 488% Improvement with 4-Ratio Switched-PEH DC-DC Converter

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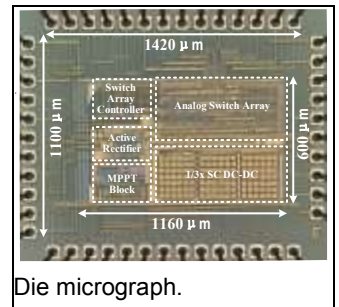
With the advent of the Internet-of-Things (IoT) era, sensor nodes are required in almost all fields to achieve a better interaction between humans and the environment. Piezoelectric energy harvester (PEH), which exhibits an equivalent electrical model of an AC current source  $I_P$  in parallel with the inherent capacitor  $C_P$ , is a promising technology to resolve the energy problem of such sensor nodes. Recently, inductor-based rectifiers, capacitor-based rectifiers and hybrid rectifiers have been proposed to improve the energy extraction efficiency of PEH devices [1-5]. However, these structures all require the aid of additional capacitors or inductors to achieve bias-flip operation, as illustrated in Fig. 1. These extra passive devices are typically large, which can be a major bottleneck in system-volume-constrained applications such as MEMS [4]. In response to the above problem, this work proposes a novel 8-phase self bias-flip PEH interface with charge recycling and reusing (SBFRR). By using the  $C_P$  of 4 PEHs as flipping capacitors, this scheme achieves a high voltage flipping efficiency without using extra energy reservoirs. The 4  $C_P$  can also serve as flying capacitors to achieve switched-PEH DC-DC (SPDC) conversion for MPPT, while maintaining a MOPIR of  $>3.5\times$  with a PEH input voltage ( $V_P$ ) from 0.78V to 4.9V.

Fig. 1 shows the proposed system using 4 PEHs, with three operating states including energy harvesting (EH), zero-crossing (ZC), and MPPT. During the EH state, the 4 PEHs work as normal harvesters and flipping capacitors alternately to extract vibration power. The ZC state consists of the recycle phase (PH<sub>RYC</sub>), bias-flip phase (PH<sub>BF1-5</sub>), reuse phase (PH<sub>RUS</sub>) and rebalance phase (PH<sub>RB</sub>). For illustration purpose, we assign PEH<sub><1,2></sub> serve as conventional PEHs, and configure PEH<sub><3,4></sub> as flipping capacitors. Starting from PH<sub>RYC</sub>, PEH<sub><3,4></sub> transfer half of the charge to  $C_{RECT}$ , followed by PH<sub>BF1</sub> where the residual charge is completely discharged. The charge on PEH<sub><1,2></sub> is gradually flipped in 3 steps from PH<sub>BF2</sub> to PH<sub>BF4</sub>, and then finally cleared in PH<sub>BF5</sub>. To improve the energy extraction efficiency, the previously recovered charge at  $C_{RECT}$  is re-injected to PEH<sub><1,2></sub> in PH<sub>RUS</sub>, and the PEH voltage is then equalized in PH<sub>RB</sub>. As the duration of the ZC state is about 80 $\mu$ s which accounts for only 1.6% of half the excitation cycle, PEH<sub><3,4></sub> can be regarded as flipping capacitors during this period without sacrificing the energy harvesting efficiency. The involvement of the charge recycle and reuse phases (i.e., PH<sub>RYC</sub> and PH<sub>RUS</sub>) can also theoretically improve the MOPIR from 3.88 $\times$  to 5.13 $\times$ .

Fig. 2 presents the operation of the proposed SPDC at EH state, where the 4 PEHs serve as flying capacitors for DC-DC conversion to extend the input power range. It is composed of 3 phases (PHE<sub>H0</sub>~PHE<sub>H2</sub>). During PHE<sub>H0</sub>, the 4 PEHs transfer charges to  $C_{RECT}$  through the active rectifier (AR), which is also responsible for zero-crossing detection and  $I_P$  polarity determination. At PHE<sub>H1</sub>, the PEH array and  $C_{RECT}$  together form a SPDC to deliver charge to the load, with a total 4 possible voltage conversion ratios (VCRs) through SPDC reconfiguration. To prevent error during zero-crossing detection at PHE<sub>H2</sub>, the voltages on PEH<sub><1,4></sub> and  $C_{RECT}$  are rebalanced in PHE<sub>H2</sub>. This can also prevent the PEH from deviating from the MPP. In this work, the time duration ratio of PHE<sub>H0</sub>~PHE<sub>H2</sub> is 3:1:2. The proposed system typically transits between the ZC and EH states. Upon the triggering of the external signal  $V_{MODE}$ , the system will temporarily switch to the MPPT state. As observed in the system diagram, the AR outputs  $V_{CP<1,2>}$  serve to generate the corresponding ZC/EH pulse sequences to control the analog switch array. Dual supply domains are employed in order to reduce power consumption. The chip occupies an active area of  $\sim 0.7\text{mm}^2$  as illustrated in the die micrograph.

Fig. 3 depicts the schematics of the key circuit modules. The analog switches are sized according to the path current to increase the power density. In order to prevent oscillation of  $V_{CP<1,2>}$  as induced by the comparator offsets, the proposed anti-oscillation technique

ensures that only one transition of  $V_{CP<1,2>}$  can occur per half excitation cycle.  $V_{CP<1,2>}$  will be sampled at 2/3 the duration of PHE<sub>H0</sub> to obtain  $V_{ZC<1,2>}$ , which is then processed by the ZC and EH sequencer to generate the required control sequence. The digital sequence generation blocks operate at 1.6V, and level shifters (LS) are employed to convert the 4.8-V supply for driving the switch array. Each LS only consumes 0.53pJ per cycle.



Die micrograph.

We explore the fractional open-circuit voltage (FVOC) method for MPPT, and employ a ratioed peak detector to prevent detection error or overshoot. Here,  $D_1$  is responsible for rectifying the PEH output, and  $R_1$  for reducing the impedance across the PEH terminals. The detected peak voltage  $V_{RPV}$  is scaled to about 0.5 $V_P$ . The 3-bit comparator outputs pulses according to  $V_{RPV}$  for triggering DFF<sub>1</sub> and DFF<sub>2</sub>, with the results further processed by the encoder to configure the VCR and  $f_{OSC\_SLOW}$ .

Fig. 4 shows the measured waveform across the PEH terminals with VCR=2 at an excitation frequency of 100Hz. During the ZC state, after 8 phases of SBFRR operation, the PEH voltage is flipped from [2.5V] to [1.5V], corresponding to a voltage flipping efficiency of 80%. At EH state,  $V_{PEH<1,4>}$  is charged from the rebuilt voltage ( $V_{RBT}$ ), with the clock signal ( $f_{ZCD\_SAMPLE}$ ) triggering the sampling of  $V_{CP<1,2>}$ . When  $V_{PEH<1,4>}$  exceeds  $V_{RECT}$ , AR is turned on, and the system starts to operate among the EH phases (PHE<sub>H0</sub>~PHE<sub>H2</sub>). If  $V_{PEH<1,4>}$  is lower than  $V_{RECT}$ , the system will reenter the ZC state, leading to a droop at  $V_{RECT}$  as observed in Fig. 4 as induced by the charge injection in the PH<sub>RYC</sub> phase. This droop will be recovered in the PH<sub>RUS</sub> phase due to the connection to  $C_{RECT}$ .

Fig. 5 presents the MPPT results, where the system automatically switches from VCR=2 to VCR=1, with the driving clock  $f_{OSC\_SLOW}$  also adaptively updated. Fig. 5 also depicts the relationship between  $P_{RECT}$  versus  $V_{RECT}$  under different  $V_P$ , as well as  $P_{OUT}$  versus  $V_P$  under different VCR. The test results show that the energy loss caused by the vibration mismatches of four PEHs can be ignored. The measured MOPIR<sub>RECT</sub> can be up to 4.98 $\times$  when  $V_P \sim 2.3V$ . The MOPIR is obtained by comparing the measured maximum output power with the calculated output power for an ideal full-bridge rectifier (with diode drop  $V_D=0$ ). When VCR=1, the MOPIR of the system can reach 4.88 $\times$ . As VCR increases, the MOPIR reduces due to the reduction of the zero-crossing accuracy. However, when VCR=4, the MOPIR can still reach 2.78 $\times$ , which is a 39% improvement compared to the ideal switch-only rectifier. The entire system can maintain a MOPIR of  $>3.5\times$  when  $V_P$  is from 0.78V to 4.9V. Fig. 6 shows the comparison of the proposed design with the state of the art. Compared to [4], this work achieves MPPT by using switched PEH converter while requesting a much smaller chip area. Compared to [1-3, 5], this work achieves the highest FoM without using external energy reservoirs, which is imperative to applications requiring an ultra-compact system volume.

### Acknowledgments:

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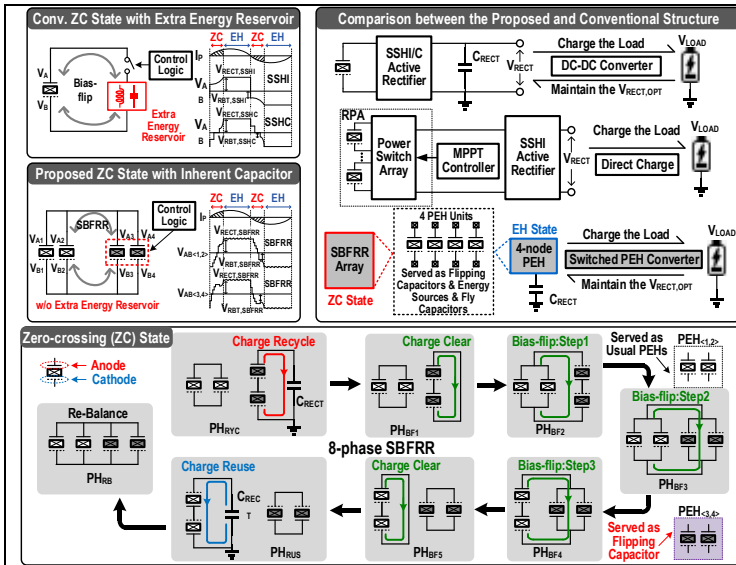


Fig. 1. Comparison of the conventional technique with the proposed scheme (top); and operation of the zero-crossing state (bottom).

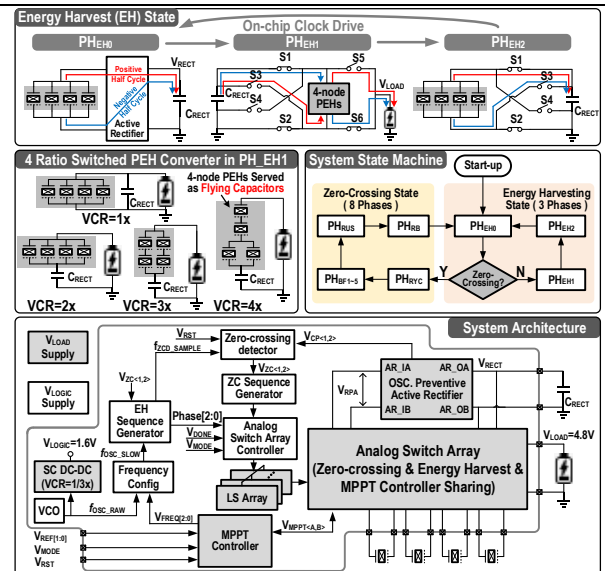


Fig. 2. Operation of the energy harvesting state (top); SPDC and system state machine; and the system architecture (bottom).

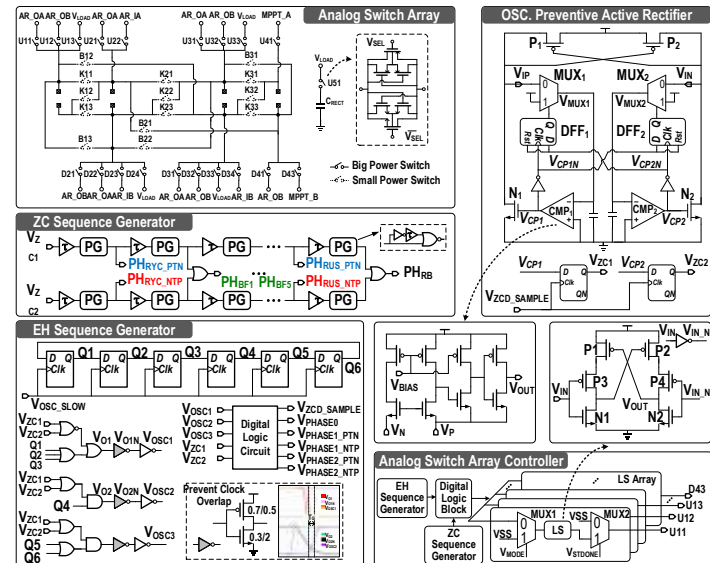


Fig. 3. Circuit implementation of switch array, oscillation preventive active rectifier and sequence generators.

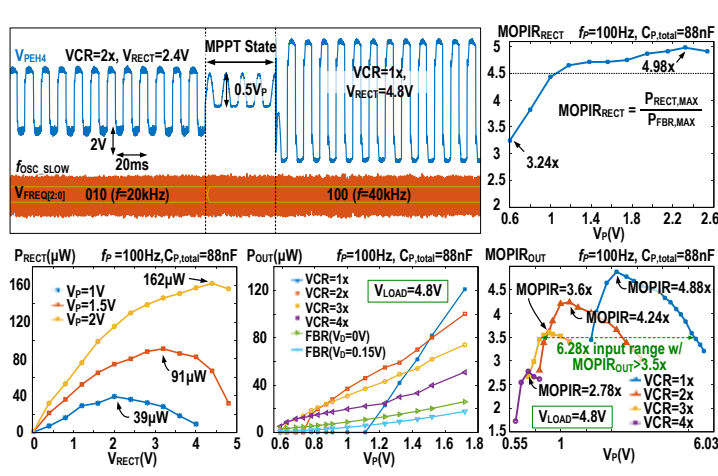


Fig. 5. Measured MPPT operation (top left);  $P_{RECT}$  vs.  $V_{RECT}$  at 1/1.5/2V  $V_P$  (bottom left); measured  $P_{OUT}$  vs.  $V_P$  under different VCR (bottom middle); measured  $MOPIR_{RECT}$  and  $MOPIR_{OUT}$  vs.  $V_P$  with 4 VCR (right).

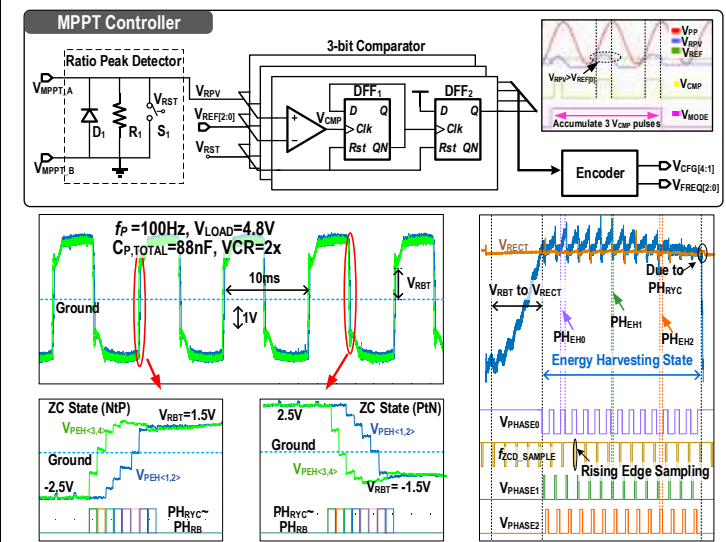


Fig. 4. MPPT controller (top); measured waveform of the  $V_{PEH}$  and zoomed-in zero-crossing state and energy harvesting state (bottom).

	JSSC'19 [1]	JSSC'20 [2]	ISSCC'19 [3]	JSSC'19 [4]	ISSCC'22 [5]	This Work
Technology	0.13 $\mu$ m	0.18 $\mu$ m	0.18 $\mu$ m	0.18 $\mu$ m	65nm	0.18 $\mu$ m
Technique	SSHIC	SPFCR	SaS	SE-SSHIC	MSVR SECE	Self Bias-Flip
Passive Energy Reservoir for Bias-Flip	L=33 $\mu$ H	$C_{TOTAL}=272nF$	L=1mH $C_{TOTAL}=10nF$	$C_{TOTAL}=4nF$	L=22 $\mu$ H	None
Passive Energy Reservoir for DC-DC	N/A	$C_{TOTAL}=272nF$	L=1mH $C_{TOTAL}=10nF$	N/A	L=22 $\mu$ H	None
Normalized Volume VNOR*	1.3	1.3	11.15	1	1.29	1
Chip Size	0.53mm <sup>2</sup>	0.2mm <sup>2</sup>	0.47mm <sup>2</sup>	3.9mm <sup>2</sup>	3.11mm <sup>2</sup>	0.7mm <sup>2</sup>
Pin Adaptation	N/A	SC DC-DC	Sense and Set Rectifier	N/A	SECE	Switched PEH Converter
No. of Inputs	1	1	1	4	3	4
Piezoelectric Capacitor	22nF	22nF	8nF	1.94nF	N/A	88nF (22nF each)
Flipping Efficiency	0.88	0.84	N/A	0.85	N/A	0.8
MOPIR*	3.66x	3.7x ~ 6.26x	3.96x	2.57x ~ 5.89x	3.2x	2.78x ~ 4.88x
FoM*	2.82	2.84 ~ 4.77	0.36	2.57 ~ 5.89	2.48	2.78 ~ 4.88
Conversion Ratio	N/A	1/3x, 2.3x, 1x, 2x	Continuous	N/A	Continuous	1x, 2x, 3x, 4x
Operating Freq.	432Hz	200Hz	85Hz	219Hz	N/A	100Hz

Fig. 6. Performance summary and benchmark with prior art.