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DOI
10.1109/TMTT.2025.3586815

Publication date
2025

Document Version
Final published version

Published in
IEEE Transactions on Microwave Theory and Techniques

Citation (APA)
Martino, C. D., Esposito, C., Malotaux, E. S., Lehmann, S., Zhao, Z., Mothes, S., Kretzschmar, C., Shokrolahzade, E., Schröter, M., & Spirito, M. (2025). Test-Fixture Design Flow for Broadband Validation of CMOS Device Models up to (sub)mm-Waves. *IEEE Transactions on Microwave Theory and Techniques*, *73*(11), 8956-8965. https://doi.org/10.1109/TMTT.2025.3586815

Test-Fixture Design Flow for Broadband Validation of CMOS Device Models up to (sub)mm-Waves

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***Abstract*—This work presents a structured, CAD-assisted design flow to realize broadband on-wafer calibration structures, validated in the prefabrication phase, and extract the intrinsic device response up to (sub)mm-waves. The strict requirements imposed by the design rule checks (DRCs) of 22 nm CMOS technology are incorporated during the design phase of the fixture by using a scripted connectable tile elements approach. The minimum dimension of a critical feature of the fixture is then identified using a newly defined metric based on the correspondence between the EM field distribution in the fixture versus a nonperturbed case of the same standard (STD) artifact. A simulation test bench environment, augmented with experimental data, is then used to add the uncertainties arising from three main error contributors: vector network analyzer (VNA) receiver noise, probe placement error, and calibration residual errors. Including these errors allows for the generation of pre-silicon numerical uncertainty bounds, which are benchmarked with experimental data using calibration quality metrics and device-level parameters. Measurement results ranging from 1 to 325 GHz are presented to demonstrate the validity of the proposed approach to establish the quality of on-wafer calibration approaches integrated in the back-end of line of Si-based technologies and to validate the compact model of CMOS devices up to (sub)mm-waves.**

Received 12 March 2025; revised 3 May 2025 and 11 June 2025; accepted 29 June 2025. Date of publication 18 July 2025; date of current version 26 November 2025. This work was supported in part by the Dutch Technology Foundation STW through Project Terahertz Silicon-Integrated CAMera, TiCAM, part of The Netherlands Organization for Scientific Research (NWO), funded by the Ministry of Economic Affairs under Grant 13325 and in part by the European Union within "NextGeneration EU", by the Federal Ministry for Economic Affairs and Climate Action (BMWK) on the basis of a decision by the German Bundestag and by the State of Saxony with tax revenues based on the budget approved by the members of the Saxon State Parliament in the framework of "Important Project of Common European Interest - Microelectronics and Communication Technologies", under the Project "EUROFOUNDRY". The work of Ciro Esposito and Michael Schröter was supported by the Deutsche Forschungsgemeinschaft under Grant SCHR695/14 and Grant SCHR695/30. *(Carmine De Martino and Ciro Esposito contributed equally to this work.) (Corresponding author: Marco Spirito.)*

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Digital Object Identifier 10.1109/TMTT.2025.3586815

***Index Terms*—Broadband characterization, CMOS, device model, mm-wave, on-wafer calibration, sub-THz.**

I. Introduction

An increasing number of commercial applications, from beyond 5G communication to the next generation of automotive radar systems [1], [2], are targeting mm- and sub-mm-wave frequencies to go beyond current system performances. This frequency upscaling has generated a strong need from technology foundries to validate the accuracy of their active device models [i.e., active components included in the process design kit (PDK)] at the frequencies targeted by these applications. This need is reinforced by the fact that the experimental data used to extract the model parameters are often limited to frequencies below 100 GHz. Similar frequency ranges for parameter extraction are also employed when considering technologies with $f_T/f_{\max}$ above 300 GHz, relying on the fact that the (advanced) compact model structure will account for the device behavior across the entire frequency range. Accurate transistor-level measurements need to be carried out to validate those claims. Here, the challenge lies in the need to employ data referred to the intrinsic device plane (or at the first metal layer plane in some cases), i.e., the device model plane. This requirement implies that the systematic errors provided by the measurement test bench (i.e., network analyzer up to the wafer probes) as well as the parasitic loading introduced by the fixture, interfacing the device under test (DUT) with the probing environment, need to be removed. The first step, i.e., removing the systematic errors the test bench provides, is achieved through a first-tier calibration. Traditionally, off-wafer impedance standard (STD) substrates (ISSs) provided by various commercial vendors have been employed to perform probe tip-level first-tier calibration. More recently, multiple papers reported the limitations of the ISS-based approach in achieving single-mode propagation, due to the electrically thick substrates, and the increased error in calibration transfer to the on-wafer environment in the higher mm-wave frequency range [3], [4], [5], [6].

These limitations are most prominent when attempting device characterization above 67 GHz, as was reported in [7], where a worst case difference larger than 0.5 in measurements corrected by SOLT on ISS was reported.

Afterward, several papers [7], [8], [9] have reported how to achieve accurate vector network analyzer (VNA) calibrations up to sub-mm-wave frequencies employing partially known calibration algorithms such as thru-reflect-line (TRL) or multiline TRL [10], [11] in the same DUT environment.

Despite this, the de facto standard approach in model extraction for foundries' PDKs [12] is to use commercial, ISS-based substrates. This approach provides a fixed distance (probe-to-probe) measurement environment and enables broadband capabilities when calibration algorithms, such as

TABLE I
COMPARISON WITH THE STATE-OF-THE-ART

		This work	[7]	[21]	[22]
Calibration method		SOLR/TRL	mTRL	TRL	TRL
Frequency range [GHz]		1-67/67-325	1-110	220-325	13-500
Relative BW in octaves		8.34	6.78	0.56	5.26
De-embedding to the intrinsic DUT		Measurement-based open-short	Measurement-based open-short	EM based	Measurement-based open
Technology		CMOS 22nm	CMOS 45nm	BiCMOS 130nm	BiCMOS 130nm
Longest line employed		150 μm	2000 μm	150 μm	560 μm
Confidence bound		3σ error bound	95% confidence	NA	NA
WCEB / *Uncertainty*	110 [GHz]	0.039 ±*0.026*	±0.023		0.05
	220 [GHz]	0.056 ±*0.059*		0.049	0.082
	325 [GHz]	0.048 ±*0.073*		0.038	0.103

short-open-load-thru/reciprocal (SOLT/SOLR) or line-reflect-match (LRM/LRRM), are used [13], [14]. Among the reasons for this choice is also the complexity of designing and validating the accuracy of a custom-built first-tier calibration kit that can be embedded in the same DUT environment, and finding solutions that can enable high accuracy at (sub)mm-wave while also providing low-frequency capabilities.

After the (first-tier) VNA-based test bench calibration, a second step is required to reach the intrinsic device plane. This is obtained by the removal of the device fixture parasitic elements, and is often termed de-embedding. This step is realized by measuring a set of dummies of the test fixture or part of it, excluding the DUT, and often assuming idealized terminations such as open and short. This step is done to realize a lumped equivalent of the fixture, which can then be used to remove the fixture loading from the DUT measurements [15], [16]. Over the years, the complexity of the test fixture models has gradually increased, mainly to provide an increased model-to-hardware correlation in the higher frequency bands. This has been achieved at the expense of a larger number of required dummy elements [17], [18], [19]. It is important to mention that the minimum dimension of the fixture is constrained by mechanical requirements such as: the landing pad area (fixed by the probe tip dimensions, which do not generally scale with frequency) and the input to output probe distance (limited by the probe-to-probe crosstalk effect [20]). For the above reasons, current fixture dimensions have reached the practical lower limit; the increased fixture model complexity is a direct result of the lumped approximation starting to fail when the propagation delay over the considered structure becomes comparable to the rise time of the signal.

To enable a simple open-short de-embedding, without trading off model accuracy, and at the same time benefitting from a consistent calibration/measurement environment employing low-dispersion transmission line components, Galatro et al. [21] and Fregonese et al. [22] proposed the concept of shifting the primary calibration plane in close proximity to the intrinsic device. The residual fixture parasitic can then be removed by employing a simple open-short de-embedding, providing high model-to-hardware correlation up to frequencies above 200 GHz, as was shown in [23]. Nevertheless, the mentioned works using TRL and/or multiline line TRL fail to cover the low-frequency part of the band, often required to enable accurate comparison in the frequency ranges where current model parameters are being extracted. A comparison with the state of the art is provided in Table I, where the 95% confidence in [7] and the worst case error bound (WCEB) in [22] have been extracted from data reported in the manuscripts.

In this work, we introduce and discuss in detail.

1) A design/simulation and validation flow to realize metal 1 (M1) direct calibration/de-embedding approaches for broadband device model validation starting from 1 GHz up to sub-mm-wave frequencies, compliant with the stringent CMOS design rule checks (DRCs).
2) A procedure, based on a quantifiable metric, to design minimum-size device fixtures to minimize fabrication costs.
3) An advanced test bench to provide numerical uncertainty bounds of calibration quality metrics and key device parameters, during the prefabrication phase.

The work concludes by presenting measured data up to 325 GHz for small signal operation of key device-level parameters, to validate the quality of the proposed broadband M1 test fixture. The extracted data are compared with the results of the PDK device model, including the numerical uncertainty bounds.

II. CMOS BROADBAND M1 TEST-FIXTURE

For decades, chemical-mechanical polishing (CMP) of interlevel dielectrics [24] has been employed in CMOS technologies to improve global planarization and overall yield. Nevertheless, since CMP processes are sensitive to the metal densities, procedures to comply with metal-fill design rules have become an integral part of the layout process. The electrical impact of the metal-fill dummies has been recognized from the early years [25], at first accounting mostly for the increased capacitance of those layers, and more recently recognizing and modeling the complete electromagnetic behavior of layers containing the metal fills, by employing equivalent anisotropic dielectric layers [26]. Aside from the modeling challenges, the current inclusion of dummy fills in the design flow (i.e., via automatic fill algorithms) is prone to inconsistencies. To provide a qualitative example of this statement, in Fig. 1(a) the outline of a generic fixture is shown. In the center element of the fixture, the DUT and the dummies (open and short) are placed. When the various fixtures are placed in a design (i.e., often forming a matrix pattern), the number and position of the floating inclusions [depicted as small squares in

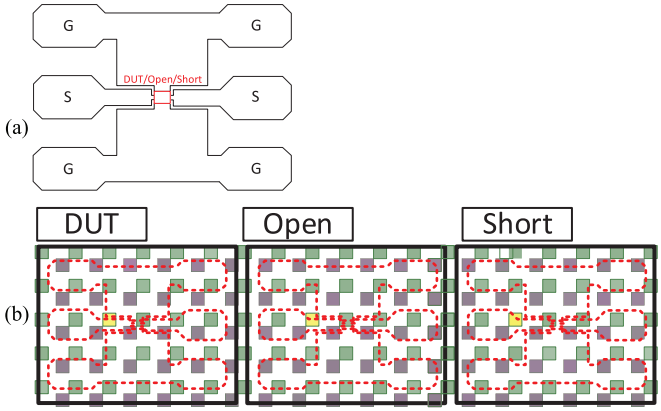


Fig. 1. Simplified example showing. (a) Outline of a generic fixture to implement open/short de-embedding. (b) Difference in relative position and number of the fill tiles' inclusion under the (dashed) frame of the fixture, leading to inconsistencies in the de-embedding approach. Yellow highlight for a single tile to better identify the relative change with respect to the same fixture position.

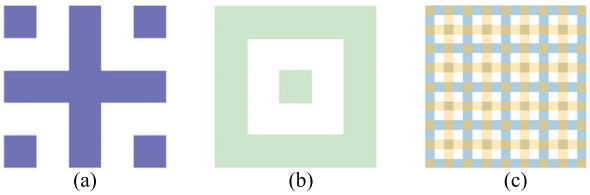


Fig. 2. 3-D drawing of the basic element which guarantees DRC compliant for a metal layer (i.e., M1) (a) subsequent layer (i.e., M2), (b) which can be easily interconnected through vias at the corners and in the center, and (c) basic unit resulting from the combination of basic elements to generate larger drawn areas.

Fig. 1(b)] may vary under the fixture location [sketched in red dashed line in Fig. 1(b)]. These relative changes provide small variations in the equivalent inductance and capacitance across the fixture, thus creating an error in the final de-embedded results. This effect is mostly relevant when sub-mm-wave frequencies are considered, given the reduced dimensions and parasitic loading of the fixture.

To overcome this error, we employ a scripted hierarchical construction of the basic unit shapes, which are then parametrized by their (metal density) fill factor. These unit cells can then be made compliant with fabrication requirements, thus completely avoiding the problem shown in Fig. 1.

A. Basic Element/Units and Blocks

Basic elements realize the lowest level in the hierarchy, see Fig. 2(a) and (b), which can be drawn in a parametrized fashion using a scripting language, i.e., Skill [27].

Subsequently, the basic elements can be combined into larger sections, thus realizing a basic unit. Various basic units employing different sets of metal layers can then be realized to provide the designer with a large library that can be used to draw any shape or structure. It is important to note that, thanks to the parametric nature of the scripts, all the derived structures can be made DRC compliant to both local and global densities.

The basic units are then combined into building blocks, see Fig. 3.

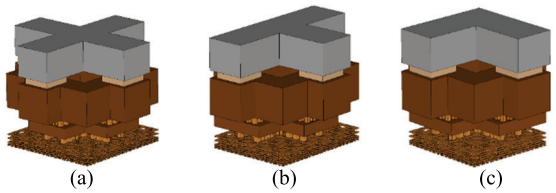


Fig. 3. Building blocks, composed of the basic units of Fig. 2(a) and (b) to realize connectable tile elements units (a) with four cardinal points, (b) three cardinal points, i.e., to be used at an edge, and (c) two cardinal points, i.e., to be used at a corner of the structure.

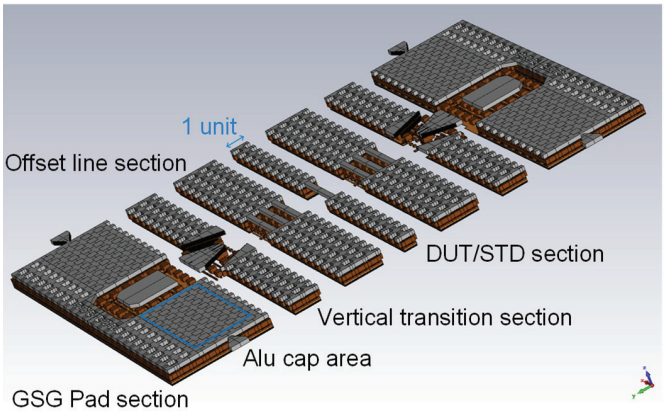


Fig. 4. Description of the various sections of the test fixture realized from different basic blocks; highlight of the dimension of the 1 unit quantization value used to simplify the cascading (i.e., connectable tile elements) approach.

B. Fixture Subsections

The various building blocks described in Fig. 3 are then combined to create the various subsections of the device fixture, see Fig. 4. In this work, the fixture approach to realize direct calibration/de-embedding presented in [21] is employed. The fixture topology employs capacitively loaded inverted CPWs (CL-ICPWs) to realize a metal 1 (M1) calibration reference plane, i.e., placing the (first-tier) calibration reference plane in close proximity to the device to be modeled. In this work, the fixture is created with the scripting approach previously introduced, and each section is realized by an integer number of sections. The DUT/STD section is realized with a single unit to minimize the parasitic addition from the calibration reference planes (1 unit, see Fig. 4).

The usage of unit cells is done to simplify the entire die floor plan when aiming at a large number of devices to be modeled/characterized.

The requirements and optimization steps of each of the test fixture sections are summarized below.

1) *GSG Pad Section:* The probe landing section of the fixture is designed to accommodate different probe pitches, given the broadband requirements of the modeling/validation measurements. The fixture implemented for this work supports probe pitches from 100 μm down to 50 μm. The pad area is made of a continuous aluminum layer to allow low-resistance contact with the probe tips, often termed Alu cap.
2) *Vertical Transition Section:* This section interfaces the (top metal) pads with the CL-ICPW placed at M1. The inverse pyramidal shape from [21] is also employed here to minimize (impedance) discontinuities and interface the larger top metal lines with the narrow M1 section. The electrostatic discharge (ESD)/antenna protection

TABLE II
CST MICROWAVE STUDIO SIMULATION SETTINGS

Parameter	*Value*
Background	Normal (vacuum)
Boundaries	Open and Electric (PEC) on the bottom
Solver	Frequency Domain (FEM)
Solver order	2nd order
Solver Accuracy	1e-5
Mesh Type	Tetrahedral
Excitation	Waveguide ports

diodes are also included in this section. It is important to mention that in ultrascaled CMOS nodes, those protection diodes are strictly required even when dealing only with R&D test structures. Given the fact that these protection diodes are now embedded in the calibration path, they need to provide full "transparency" (i.e., no measurable variation) in the entire bias characterization window of the DUT. When full "transparency" is not achieved (i.e., due to the limited stacking capability of the protection diodes) within the characterization window, an error split box procedure, as demonstrated in [28], should be applied. The antenna (triple) diode stack employed for the fixture reported in this work provided "transparent" behavior up to 1 V.

3) *Offset Line Section:* The offset line allows the setting of the reference plane of the (first-tier) calibration "far enough" from the vertical transition, to reach an area where the line only exhibits a mono-modal quasi-TEM propagation mode, as required by the TRL algorithm. A detailed analysis of the complex tradeoffs that occur in the offset line design is given in Section III.
4) *DUT/STD Section:* This single-unit section allows for embedding the different STDs to enable the various calibration algorithms (i.e., SOLR and TRL) as well as the various DUTs to be measured for testing and modeling. Within the scripting approach, this allows for the layout of the various fixtures by employing a simple case statement.

III. OFFSET LINE ANALYSIS

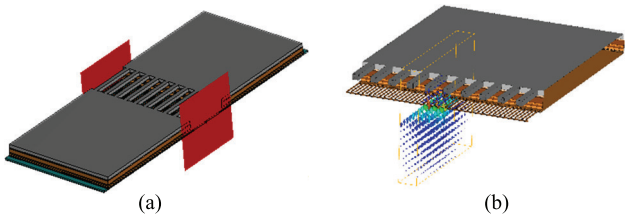
Given the high cost of wafer area in advanced CMOS nodes, an accurate and quantifiable procedure is needed to define the minimum distance from the vertical transition required to reach mono-modal quasi-TEM propagation.

The minimum distance is numerically analyzed in this section employing a 3-D FEM solver.

The simulations described in this section have been carried out with CST Microwave Studio from Dassault Systèmes; the solver parameter settings are summarized in Table II.

The first step is to compute the field inside a uniform CL-ICPW line where no discontinuities are present. To extract this field, the line is excited by waveguide ports, see Fig. 5(a), and the field is selected on a 2-D cross section inside the structure, i.e., at the center of the line, see Fig. 5(b).

This field is then assumed as the single-mode quasi-TEM field supported by the CL-ICPW line. Afterward, the entire



(a) (b)

Fig. 5. (a) Standalone section of the M1 line excited using waveguide ports to analyze the nonperturbed field. (b) Non-perturbed field extracted at the center of the standalone section of the M1 line.

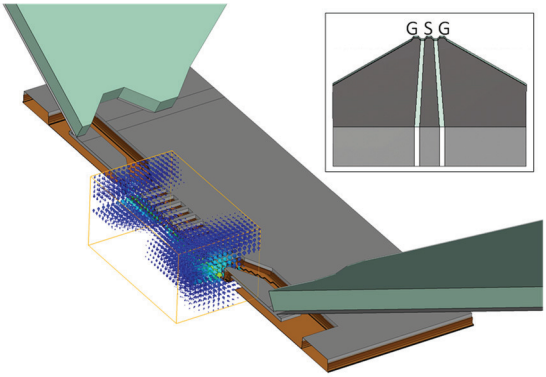
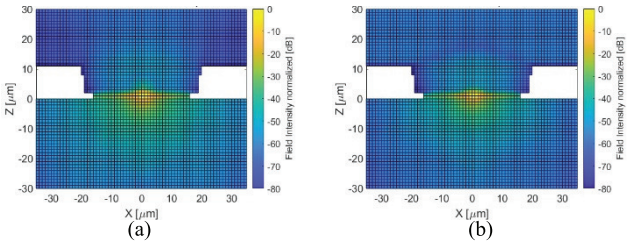


Fig. 6. Highlight of the 3-D volume of the field inside the structure extracted from the CST simulation. The inset provides details on the CPW configuration of the probe side contacting the pads.



(a) (b)

Fig. 7. Field distribution on the cross-sectional area along the M1 transmission line, for (a) uniform line, i.e., waveguide port fed, and (b) inside the fixture, i.e., where the vertical transition discontinuity is included.

fixture is excited by a realistic model of the wafer probe tip to mimic, with good accuracy, the field disturbances at the probe-pad transition. The 3-D volume inside the CL-ICPW section of the fixture is then considered and exported for further analysis, as shown in Fig. 6. The inset of Fig. 6 details the CPW configuration of the probe side contacting the pads. It is worth noting that given the presence only of the probe tip (no accurate probe body is mapped in the proposed simulation), this work, differently from [29], does not provide specific information on crosstalk reduction strategies.

The 2-D field of the uniform line [see Fig. 7(a)] can then be compared to the field inside the fixture [Fig. 7(b)] at different offset distances from the vertical transition, using the metrics introduced in (1), where the superscript TF identifies the Test Fixture, while REF identifies the uniform line. The metric represents the mean absolute error between the field distribution of the propagation mode over the sample grid within the test fixture (at a given y location, see Fig. 8 axis) and the mono-modal case

$$\text{Field Error} = \frac{1}{n}\sum_{i=1}^{n}\left(E_i^{\text{TF}} - E_i^{\text{REF}}\right)^2. \tag{1}$$

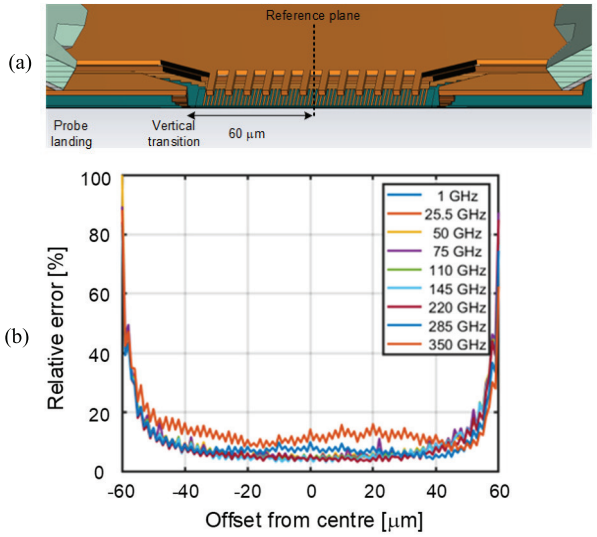


Fig. 8. (a) Cross section of the line used for the analysis, with reference dimensions, (b) error computed using (1) along the M1 line for various frequencies.

The result of this analysis is then presented in Fig. 8. Here, we can observe that moving 20 μm from the vertical transition, the error becomes independent of the distance to the transition. This region can then be identified as the single-mode quasi-TEM zone. The quick decay of the error and the (almost) independence from the frequency can be explained by the fact that nonpropagating reactive fields (also known as evanescent) present a decay length which is only weakly dependent on the frequency.

To minimize the chip area, an offset line length of 30 μm was chosen for the fixtures realized in this work.

IV. Simulation of Broadband STDs

To allow for accurate characterization in the frequency range below 67 GHz, where the parameters of compact device models are usually extracted, the proposed test fixture needs to include broadband STDs, i.e., open, short, and load. The measurement of these STDs in conjunction with the TRL enables the usage of broadband calibration algorithms such as SOLR [13], which can be used to extract the device's lower frequency response, i.e., below 67 GHz. This allows a reduction of the maximum line length required to 150 μm (WR10 band), as mentioned in Table I.

The nominal responses of the STDs are then extracted via 3D-EM simulations of the (1 unit, see Fig. 4) STD section.

For consistency, the reference plane of the SOLR is located in the same plane set by the TRL, i.e., the center of zero length through.

Following the analysis presented in III, setting the location of the SOL STDs at the center of the thru line suggests that the field computed by the waveguide port, see Fig. 9, will be an accurate representation of the response of the STD termination, which will then be used in the calibration process.

Reducing the 3-D simulation to the volume of the 1-unit section (see Fig. 4) allows for the inclusion of most of the artifacts that will be embedded in the DRC clean layout.

The inclusion of several of the structure features together with a localized increased mesh density, see Fig. 10, allows for an accurate extraction of the STD response.

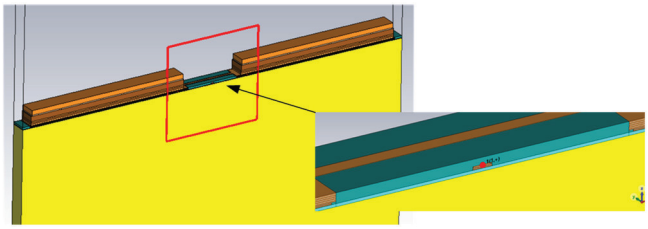


Fig. 9. 3-D view in CST of the open structure for the STD definition, (inset) zoomed-in view of the center of the port where the short line section is created to provide continuity with the M1 line environment at the port section.

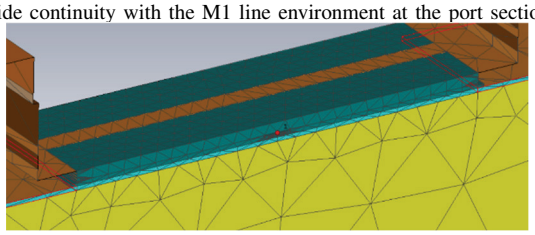


Fig. 10. Mesh details highlighting the local, i.e., layer-dependent, increased mesh density.

The reflect STDs, i.e., open and short employing only metals of the back end of line, will be subject to very limited changes in their response due to process variation. The reason for this is easily explained by the fact that lateral and vertical dimensions in advanced CMOS nodes are very strictly controlled to reach the target process yield.

The load STD, on the other hand, often employs doped layers, as the polylayer in CMOS technology. These layers can present a higher spread to nominal values, which would result in a deviation in the load EM computed response. To minimize this error, a technique based on a dc load extraction and a parametrized EM model, as the one presented in [30], can be used.

V. Presilicon Simulation Test Bench

To incorporate the simulated data, based on the PDK (i.e., synthetic data), the expected measurement errors, to provide realistic uncertainty bounds on device-level metrics, we consider, in this article, an extension of the work described in [31]. Three main sources of errors are included:

1) The VNA impedance-dependent trace noise,
2) The M1 on-wafer calibration residual errors, and
3) The probe placement errors.

The Keysight ADS simulation environment is used to include and propagate these error sources through the calibration and data manipulation equations. As presented in [31], the VNA receiver noise is included using a MonteCarlo simulation to generate a stochastic variable, which introduces a noise voltage on the waves sampled by the VNA, as sketched in Fig. 11.

The VNA error term block is used to map the error term of the test bench, which will be physically used in the characterization step. This inclusion allows for accurate scaling of the analyzer's noise through the calibration process. The EM simulation of the entire fixture, including the various STDs, allows for estimating the calibration residual errors. This is done by comparing the corrected synthetic data of the fixture to a known device, i.e., a 150 μm line. The calibration residuals are then expressed using the WCEB metric from [33], described in (2), as shown in Fig. 12

$$\mathrm{WCEB}(f) = \max \left| S'_{ij}(f) - S_{ij}(f) \right| \quad \forall i, j \in [1, 2] \qquad (2)$$

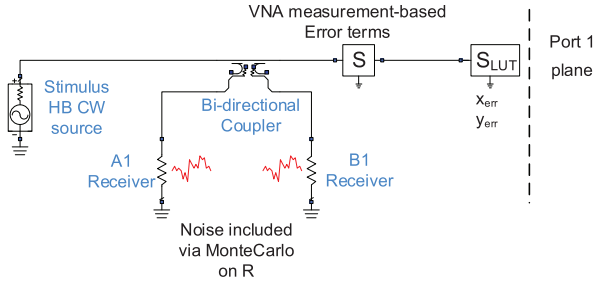


Fig. 11. Circuit schematic representing the input/output section of the source and receiver circuit, including the receiver noise sources, the VNA error-terms (S-parameter block), and the parametrized EM model of the on-wafer test-fixture (S_{LUT}).

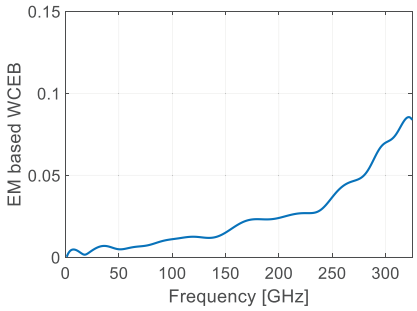


Fig. 12. WCEB computed from 3-D EM data of the test fixture employing the TRL calibration algorithm and a nonperturbed CPWG line of 150 μm length as a reference device.

where S' is the reference scattering matrix of the verification line (i.e., 3-D simulated S-parameters), $S(f)$ is the frequency-dependent scattering matrix resulting from the entire fixture calibration.

Different from [31], the probe placement error included in this work is obtained by employing a full 3-D parametric simulation of the displacement of the probe tip on the pad structure, as shown in Fig. 13(a). The generated look-up table (LUT) from CST Microwave Studio is then included in the test bench via a parametrized S-parameter LUT, based on the x and y placement errors. Note that the proposed approach enables proper accounting of the probe shadow and the tip coupling to the BEOL, which is an important aspect in the simulation accuracy, as was discussed in [32].

The proposed approach allows a considerable reduction in simulation time since only the probe tip, the pad section, the vertical transition, and the offset line section [see Fig. 13(b)] are included in the two-port parametric simulation. The probe landing point is varied over x and y (i.e., longitudinal and transversal) to generate an S-parameter database, which can be subsequently interpolated [gray grid in Fig. 13(b)] during the MonteCarlo analysis carried out in ADS. The 3-D simulation is carried out in CST Microwave Studio [red points on the grid shown in Fig. 13(b)].

The value to be applied to the x and y perturbation was extracted from visual inspection of the landmarks on the pad structure using the TU Delft piezo station (see Section VI). A σ of ± 3.5 μm on the longitudinal and of 2.5 μm on the transversal dimension was used, in the MonteCarlo simulation.

The ADS test bench can then be used to propagate the numerical uncertainty to the WCEB across the various

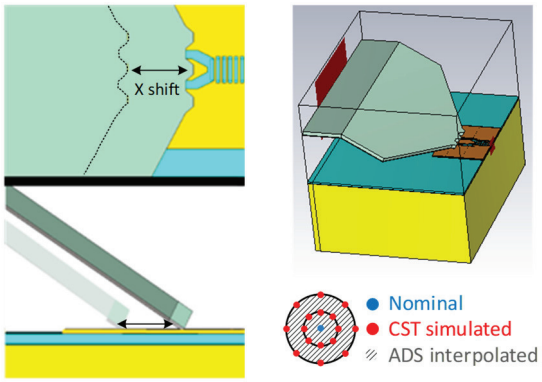


Fig. 13. (a) lateral and vertical view of the probe pad structure, highlighting the x shift movement. (b) 3-D view of the probe and the half fixture section, with the inset representing the simulation grid and the ADS interpolated data.

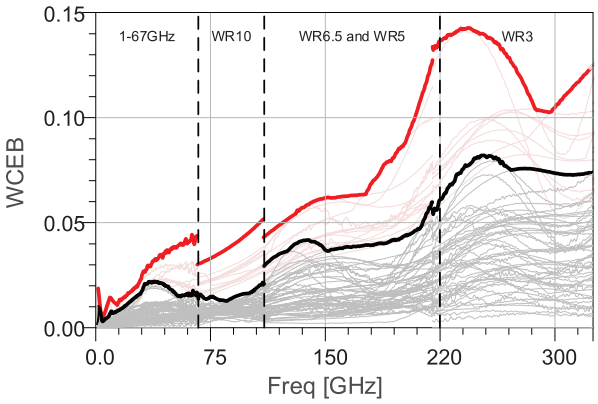


Fig. 14. Different WCEB, computed with the ADS test bench via the MonteCarlo simulation, including the VNA receiver noise and the probe placement error from Fig. 13, gray lines assuming placement errors (x = ± 3.5 μm and y = ± 2.5 μm), black line presenting the max bound from this set, light red lines assuming placement errors (x, y = ± 5 μm), red line presenting the max bound from this set.

characterization bands, as can be seen in Fig. 14. It is worth noting that the jumps occurring at the band edges at WR10 in the synthetic data shown in Fig. 14 are to be attributed to the limited number of MonteCarlo iterations (i.e., 51). The large swing around 220 GHz is attributed to a large probe misplacement value in the MonteCarlo iteration, still compatible with the given distribution (σ_x of ± 3.5 μm σ_y 2.5 μm).

VI. Experimental Setup

The measurement setup used in this work covers the frequency range from 1 to 325 GHz, employing one four-port VNA, namely the N5227A 67 GHz PNA, and four different mm-wave extender units.

1) TU Delft custom WR10 VNA extender modules (i.e., operating from 67 to 110 GHz) based on VDI AMC multipliers.
2) VDI WR6.5 VNA extender modules (i.e., operating from 110 to 170 GHz).
3) VDI WR5 VNA extender modules (i.e., operating from 140 to 220 GHz).
4) OML Inc. WR3 VNA extender modules (i.e., operating from 220 to 325 GHz).

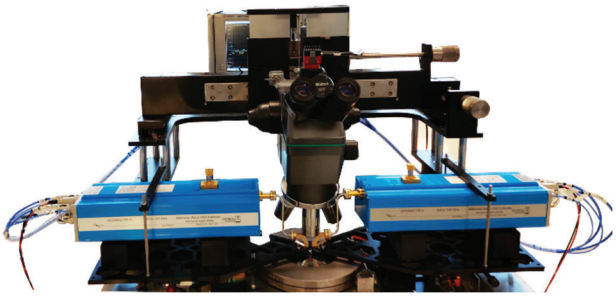


Fig. 15. TU Delft/VSL custom-developed probe station with high-resolution Newport piezo actuators.

A TU Delft VSL jointly developed probe station, see Fig. 15, based on a Cascade Microtech Summit 9000 and employing four piezo actuators (for x, y, z, and tilt control) from Newport, for each manipulator, enabling a step resolution of ~20 nm [34], [35]. The station allows for remotely controlled alignment and landing procedures, thus minimizing the vibration arising from operator contact with the probe station.

The RF probes used are form factor infinity probe 100 μm pitch for the coaxial band, WR10, WR6, and WR5 band, and GGB 75 μm pitch for the WR3 band. The measurements have been carried out using the Vertigo MMW-STUDIO software, allowing a probe tip power control of −25 dBm, which guarantees small signal operation of the characterized nMOS device.

VII. Experimental Model Validation

The test fixture discussed in Section II was implemented in the CMOS 22 nm FD-SOI process from GF to realize the SOLR and TRL M1 calibrations for covering the frequency range from 1 to 325 GHz.

By employing the ADS test bench presented in Section V, we can incorporate the uncertainties introduced by the probe placement error and the VNA noise on the WCEB metric. This is obtained by propagating the perturbations realized by the MonteCarlo simulation (see Fig. 12) onto the calibration residual errors evaluated from the EM approach (see Fig. 14). This expanded error metric can then be compared with the experimental results over the various characterization bands, as shown in Fig. 16.

Two numerical WCEB are included, one with gray color considering the probe placement errors, the values obtained employing the probe station with piezo actuators available at TU Delft, the second with light red color assuming a placement error of 5 μm in both x- and y-directions. The continuous increase in the WECB reinforces the importance of striving to minimize the probe placement error when targeting accurate sub-THz calibrated measurements.

Moreover, from the figure, it can be seen that the proposed presilicon numerical uncertainty bound provides a very realistic indication of the measurement quality that will be achieved in the measurement phase. The experimental WCEB (see Fig. 16, black line) is computed using the nonperturbed (i.e., waveguide-fed response) 150 μm M1 line as a reference.

The proposed method was then applied to the device metrics to validate the PDK model provided by the foundry. A 16-finger 18 nm gate length and 500 nm gate width nMOS was embedded in the M1 test fixture shown in Fig. 17. To increase the correlation between the measurement data and

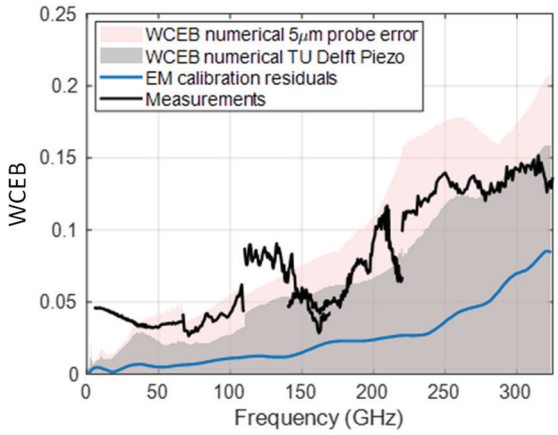


Fig. 16. Nominal calibration residual WCEB (blue trace), region defined by including the results from the MonteCarlo simulation shown in Fig. 14 on the nominal WCEB (red area/gray area), WCEB computed from measurement (black line) on M1 on-wafer calibration kit integrated in GF 22 nm FD-SOI technology.

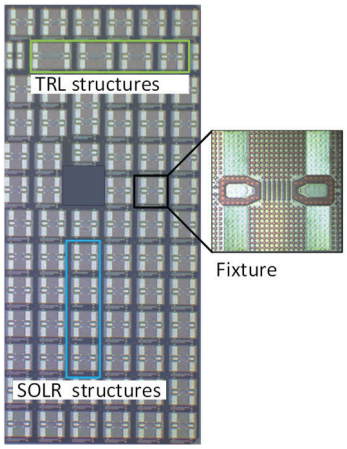


Fig. 17. Microphotograph of the realized chip in the GF 22 nm FD-SOI technology, with highlights on the set of structures to realize the SOLR and TRL calibration. Zoom-in of one of the structures where the characterized DUT discussed in Section VII is embedded.

the PDK model, an extra open short de-embedding step after the M1 calibration plane was added, as discussed in [23].

Different key device metrics were measured over the frequency range discussed in Section VI and compared with the foundry PDK model in Fig. 18(a)–(e).

It is important to note that different frequency-banded probes, different calibration kit artifacts (i.e., using structures from different dies), and thus different transistors have been used in the measurement campaign.

As was mentioned in [35], this can lead to discontinuities at measurement bands' edges. It is then important to note that these discontinuities can be attributed to both calibration uncertainties and process variations. The proposed approach can then be used to incorporate process spread.

VIII. Discussion

The proposed presilicon numerical uncertainty bound provides a very realistic perturbation on the synthetic data, giving an accurate prediction of the accuracy with which the metrics can be ultimately measured. When examining the

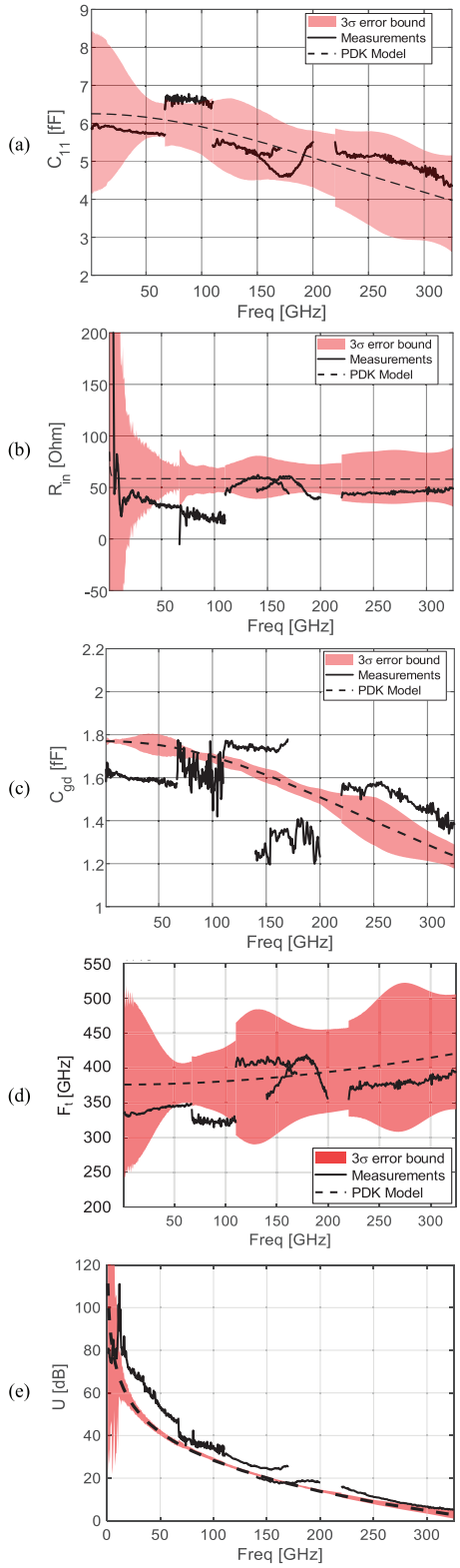


Fig. 18. (dashed line) PDK model response, (black line) measured data after M1 calibration and open-short de-embedding, (red area) 3 sigma numerical error bound extracted following the procedure described in Section V for different device model parameters (a) input capacitance (C_{11}), (b) input resistance (R_{in}), (c) gate–drain capacitance (C_{gd}), (d) maximum transit frequency (F_t), and (e) unilateral power gain.

correlation between the measurement and the PDK model-based simulation, we can appreciate the consistency of the de-embedding approach used in this work with the one used for model parameters extraction, thus resulting in a similar intrinsic device-level plane. In the higher frequency bands, i.e., above 110 GHz, the residual positive reactance leading to a small decrease of the input and gate–drain capacitance is tracked by both the model and measurements. The nonfrequency dependent input resistance is accurately extracted by the measurements and follows closely the model response. It is worth noting the large expansion of the uncertainty bounds in the lower bands, which is mostly due to the extremely high reflection coefficient of the unmatched transistor at these frequencies. Both the trend of the computed cutoff frequency (F_t) and the frequency at which the unilateral gain goes to 1 are properly tracked in the measurement model comparison. The capability of measuring device metrics at their limit frequency provides an important tool for model verification regarding distributed and special high-frequency effects. Finally, it is worth to note that a larger deviation of the gate–drain capacitance from the predicted bound is attributed to both the extremely low value of the parameter as well as to the impact of probe crosstalk effects which need to be accounted for these type of metrics (i.e., based on port 1 to port 2 transfer) as discussed in [36].

IX. Conclusion

In this article, we presented a structured design flow, based on commercially available CAD tools, to design and validate on-wafer broadband calibration kits to be integrated in the back-end of line of advanced CMOS technologies.

Special emphasis was placed on how to incorporate the stringent design rules constraints into a parametrized connectable tile element set of basic blocks to allow quick optimization of the layout during the different phases of the flow. A structured analysis with a novel introduced metric was presented to define the minimum offset line length to achieve a monomodal TEM propagation at the calibration reference plane. Furthermore, a measurement-based augmented simulation test bench was introduced to identify during the prefabrication phase the expected uncertainties that are expected during the experimental phase. Finally, the approach as well as the prediction of the numerical uncertainty bounds was validated for the calibration quality as well as key device model parameters up to 325 GHz.

The final results show the accurate prediction capability of the approach and the capability of the designed fixture to provide device-level metrics over the intended broadband frequency range.

Acknowledgment

The authors would like to acknowledge Juan Bueno from the Delft University of Technology for the fruitful discussion and help in managing the experimental test benches.

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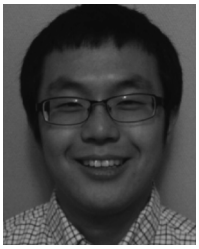

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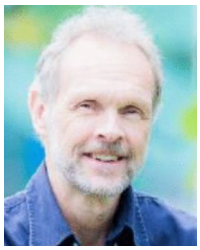

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