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Gate Driver Design for Solid-State Circuit Breaker with Integrated Latch Current Limiter in Shipboard DC Systems

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Abstract—This paper proposes an integrated gate driver featuring soft turn-off and current limiting for a solid-state circuit breaker in primary shipboard DC systems. The added functionalities allow solid-state circuit breakers to mitigate part of the voltage resonances caused by a hard turn-off, and to reduce unnecessary tripping during overloading events. The proposed design is based on well-known DC protection strategies, which are enhanced by the custom gate driver, simulated in SPICE software. The paper shows that the proposed strategy effectively attenuates the adverse effects of the hard turn-off present in popular off-the-shelf devices, while effectively breaking the fault current. The low propagation delay of the selected components facilitates the rapid break of the current, reaching approximately 69 A peak. In addition, the latch current limiter prevents the feeder from overloading, creating a voltage drop of 51% for tens of nanoseconds. The results are promising in motivating future prototyping of the design in an attempt to accelerate the acceptance of shipboard DC systems.

Index Terms—DC protections, gate driver, latch current limiter, shipboard DC systems, solid-state circuit breaker

I. INTRODUCTION

The efforts to enable energy transition include decarbonization of the maritime industry, which is responsible for about 3.1% of CO₂ emissions worldwide, which could expectedly grow close to 18% by 2050 if no corrective action is taken [1], [2]. Studies for the reduction of CO₂ involve alternative power sources and fuels, optimization of operation, and extensive electrification [3], [4]. This electrification could implicate a paradigm shift from well-known shipboard AC systems to modern DC grids, which enable variable speed operation of

generator sets and simplified integration of batteries and fuel cells. [5], [6].

Power electronics converters govern the normal operation of DC power systems. This implies that their development is essential for multiple applications. However, some characteristics of shipboard grids produce application-specific challenges that must be addressed [7], [8]. For instance, high-power filtering capacitors are necessary for the high power density drives utilized in low voltage systems [9]. In the event of a pole-to-pole short circuit, the energy stored in the capacitors flows uncontrollably to the fault point through a low-impedance path [10]. The generated high-speed impulse current can degrade and damage several components in the circuit, potentially compromising the safety of the vessel, hence the relevance of protection systems on board. Unfortunately, protections for multi-megawatt DC systems are not sufficiently developed, and a cost-effective and efficient solution is missing [9].

Existing AC protection devices rely on the natural zero-crossing current to break the fault [11], [12]. Since DC systems lack that characteristic, well-known AC protections are not suitable, thus imposing the development of dedicated solutions. State-of-the-art shipboard DC systems utilize breaker-based and fuse-based protections to galvanically isolate the defective part from the rest of the grid [13]–[16]. However, short circuits are among the most threatening hazards on a ship, and most DC circuit breakers cannot contain them effectively.

For example, mechanical circuit breakers are inexpensive and efficient, but ineffective against pole-to-pole short circuits due to their limited response time (*several milliseconds*) [17]. Fuses also have relatively long response times and an extensive replacement time [18]. In contrast, solid-state circuit breakers (SSCB) feature an adequate response time (*several*

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microseconds), but relatively high conduction losses and are usually expensive [19]. Furthermore, the hard turn-off of some commercial SSCBs can generate sympathetic tripping, worsening the consequences of a potential fault, and can trip unnecessarily during relatively simple overloads.

Solutions are needed to overcome the limitations of SSCBs to make them efficient, effective, and safe. Part of the solution might be found in the design of an integrated gate driver to improve the controllability of the semiconductor, enhancing the breaker effectiveness. The custom solution enables the soft turn-off transition and facilitates the use of SSCBs as current limiters [20], [21]. A successful solution can unlock the potential of DC ships, building confidence about their effectiveness and safety.

This work focuses on protecting a simplified shipboard DC system against severe short circuits by means of a SSCB. The objective of this paper is to propose an integrated gate driver that enables the soft turn-off and the latch current limiter in a SSCB for ship DC systems. By doing so, it could be possible to prevent part of the voltage oscillations created during the hard turn-off of a SSCB, present in popular off-the-shelf devices. In addition, the latch current limiter can prevent unnecessary tripping of the SSCB during temporary overloading events, avoiding disconnection of important loads. This research is based on well-known solid-state DC protection strategies that are enhanced by the custom gate driver, simulated in SPICE. The article contributes to the development of SSCB by showing that the proposed strategy effectively breaks the fault current without aggressive voltage oscillations. In addition, the SSCB successfully operates as a latch current limiter, preventing the feeder from overloading and tripping unnecessarily. The latching produces a 51% voltage drop for tens of nanoseconds, which could be acceptable compared to breaking. The validation of results by means of a SSCB prototype tested under different scenarios is part of the future work of this research.

The remainder of the paper is organized as follows. Section II describes the reference use case and the feeder and SSCB models. Section III explains the functional block of the custom gate driver and the way control signals are enhanced. Section IV summarizes the system and the SSCB parameters, and the simulations showing the current limiting and breaking actions. Finally, Section V contains the outlook of the research conducted and the future work expected.

II. MODEL

The simulation model in this study is based on a real superyacht, which features a state-of-the-art primary shipboard DC system. The power grid configuration was modified to analyze the performance of the SSCB in a distributed architecture. This architecture implies that the power converters are close to the loads and sources, distant from the main switchboard, as explained in [22]. The system under study is a simplification of the reference case and it has three levels of detail to be considered.

- A) Primary DC system: main generators, loads, and protection devices.
- B) Simplified feeder: single source with output filter, transmission lines, SSCB, and loads.
- C) SSCB: unipolar bidirectional solid-state protection with bipolar no-load switch (NLsw).

A. Shipboard DC system

The primary system is intended to integrate the main sources and consumers. The distributed switchboard in Fig. 1 connects the following components:

- Main generators: ≈ 1.5 MW
- Secondary generators: ≈ 1 MW
- Battery packs: ≈ 500 kW
- Main thrusters: ≈ 2 MW
- Bow thruster: ≈ 300 kW
- Hotel loads: ≈ 500 kW

The components in the green shade are physically located inside the switchboard. The groups of engine, generator/battery and voltage source converter (VSC)/DC-DC converter are located close to each other, outside of the switchboard, and connected to the bus bars via fuses and DC transmission lines.

The power grid in Fig. 1 has two unipolar bus bars (A and B), a floating ground and are coupled by using a solid-state bus-tie switch (BTS). Depending on the application it is possible to find three solutions for the BTS. 1) Mechanical circuit breaker, 2) NLsw with a high-speed fuse, and 3) SSCB. The latter is in the scope of this research, and to better analyze its behavior, a simplified circuit is necessary.

B. Simplified feeder

The use of a generator-load feeder facilitates the development of the SSCB in a rather simple setup while including parameters that emulate (part of) the primary system. Fig. 2 represents use case feeder including sources, output filter, loads with RL transmission lines, SSCB, overload, and fault branches.

- **Generator:** The VSC is modeled with a zero-volts-grounded power supply with a Thevenin resistor R_{th} , and a flywheel diode.
- **Output filter:** Includes the equivalent series resistance (R_{ESR}) and the parasitic inductance (L_p) together with the equivalent capacitor.
- **Loads:** Simplified as RL branches, divided load zones A and B (R_{LA} and R_{LB})
- **Overload and fault:** The overload resistance (R_{OL}) is designed to be connected and disconnected multiple times, whereas the short circuit resistance (R_{SC}) can be connected a single time in the test.

C. Solid-state circuit breaker

The SSCB architecture utilized in the design, shown in Fig. 3, is well-known in the literature [23], [24]. Conceptually, it is designed to offer high-speed bidirectional protection with

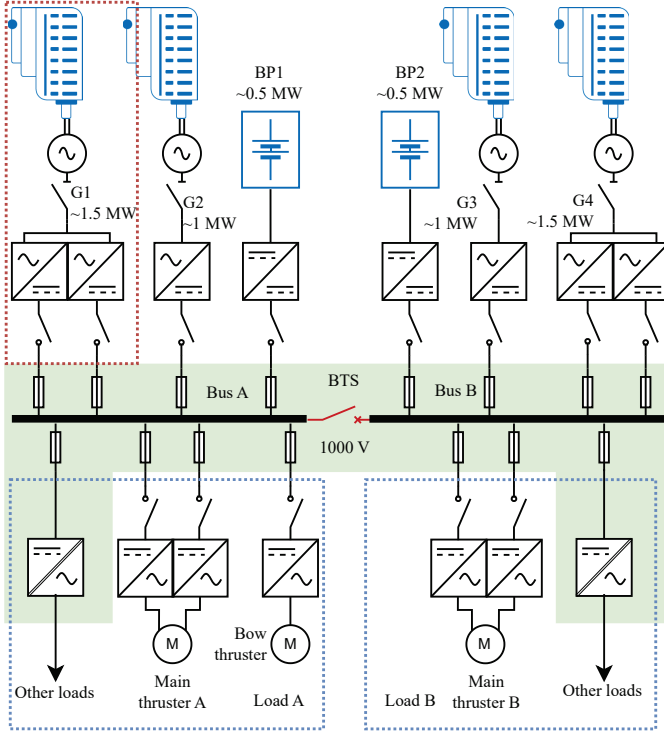


Fig. 1. Referential case study for shipboard DC systems. Primary shipboard DC system, suitable for the superyacht. Red dots: Components placed close together, blue dots: load zones, green shade: switchboard components placed close together.

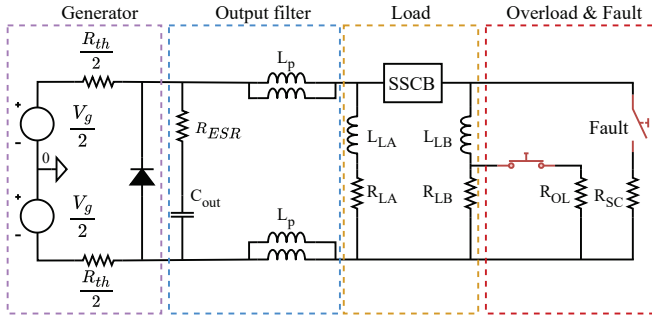


Fig. 2. Schematic of the simplified DC system under test. Simple generator with output filter, RL loads A and B, SSCB, overload and short circuit branches.

power switches and galvanic isolation with the NLsw as in [9].

The SSCB schematic has three main parts: 1) power MOSFETs and a NLsw to break the current and isolate the circuit, respectively, 2) hall effect sensor and voltage meter across the detection inductance (L_d) to measure average current and di/dt for fault detection, and 3) metal-oxide varistor (MOV) as overvoltage clamping circuit and power dissipation branch. The selectivity scheme intended for the SSCB is the three-level time-discriminating scheme in [25].

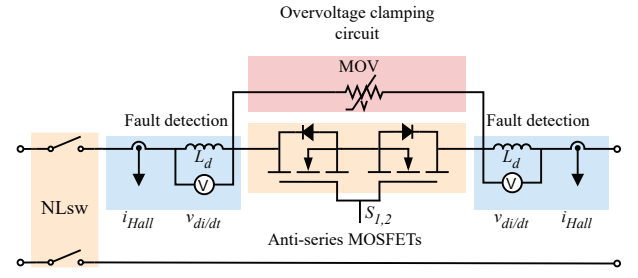


Fig. 3. Schematic of the solid-state circuit breaker topology utilized for the primary shipboard DC system. Yellow shade: current interruption components, blue shade: fault detection sensors, red shade: energy dissipation branch.

III. INTEGRATED GATE DRIVER

This section explains the functional blocks and characteristics of the custom gate driver, the gate signal modulation for latching and breaking actions. When considering solid-state protection against pole-to-pole short circuits and excessive overloads a customized design is necessary. The strategy taken in semiconductor driving has a significant effect on the outcome of the protective action. The work in [21] shows a custom gate driver for a latch current limiter in space applications. The investigation in [20] explains the potential effects of a soft turn-off in a SiC switch by designing a gate driver that integrates high-speed desaturation protection. Researchers in [26], [27] demonstrate how high-speed detection and action is essential for effective protection. Therefore, time-critical control signals and gate driving actions require an integrated solution that is not currently available in the market, and a tailored design is imperative.

A. Functional blocks

Developing an integrated gate driver can be simplified using an existing product as a baseline and adding complementary functional blocks. The diagram in Fig. 4 summarizes the integrated gate driver constitution to provide current latching and breaking. The SSCB controller monitors the voltage, current and di/dt signals, and compare with the set-points. The controller also commands the on-off signal to the isolated gate driver stage, based on the reference UCC21222, to obtain a low propagation delay (max. 40 ns).

The gate resistors R_{ON} and R_{OFF} are chosen in such a way that the desired gate modulation is achieved and the driver source-sink parameters are preserved. For the gate driver UCC21222, the peak source and sink currents are 4 A and 6 A respectively. The effective peak source and sink current of the gate driver includes the gate drive loop resistance, which is determined by the output stage, the diodes, and the power MOSFET, as described in Eqs. (1) and (2).

$$I_{ON} = \frac{V_{DD} - V_{GDF}}{R_{NMOS} \parallel R_{OH} + R_{ON} + R_{GFET}} \quad (1)$$

$$I_{OFF} = \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} + R_{GFET}} \quad (2)$$

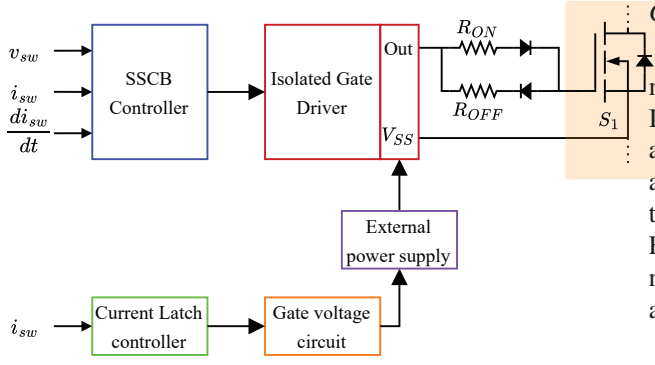


Fig. 4. Simplified functional blocks of the gate driver employed in the SSCB for primary DC protection onboard. Yellow shade: current interruption component.

Where V_{GDF} is the forward voltage in the gate diode, R_{NMOS} and R_{OH} are pull-up resistances part of the driver output stage, R_{GFET} is the gate resistance of the power switch and R_{OL} is the pull-down resistance of the output stage.

The floating side of the gate driver is powered by an external isolated power supply, which requires two output voltage levels for latching and normal operation. The current latch controller commands the gate voltage circuit to modify the output voltage of the external power supply.

B. Current limiter

The latching functionality exploits the linear region operation of FETs to work as a controlled resistor that varies with the gate-source voltage [21]. During latching, the on-resistance and power losses in the semiconductor increase significantly, which generates voltage and current drops. The gate-source modulation necessary to achieve this functionality is shown in Fig. 5.

Initially the voltage $V_{g_{on}}$ indicates normal operation, after T_{on} the overload is detected and the active gate voltage drops to $V_{g_{latch}}$. The latching decreases the drain current until it is within the normal operation boundaries, triggering the latch reset (after T_{latch}). The functionality is also active during a fault. In such cases, the drain current will exceed the breaking threshold, triggering the soft switch turn-off (starting from $V_{g_{latch}}$). Notice that the values of T_{on} and T_{latch} in Fig. 5 are illustrative only and do not represent periodic patterns. The latching is time-limited by the thermal characteristics of the switch.

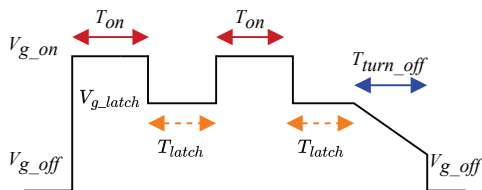


Fig. 5. Gate signal modulation waveforms for the SSCB operating as a latch current limiter using a three-level with ramp turn-off transition.

C. Controlled turn-off

A soft turn-off operation is desirable to attenuate electromagnetic compatibility issues related to fast current breaking. In principle, the gate of a power MOSFET can be modeled as a gate-source parasitic capacitor [28]. The soft turn-off aims to limit the discharge current of such a capacitor into the gate driver. Normally, the capacity can be estimated using Eq. (3). Unfortunately, the test parameters in datasheets are not necessarily compatible with the SSCB design, and further adjustments from simulation models are frequently necessary.

$$C_{gs} = \frac{Q_{gs}}{V_{gs}} \quad (3)$$

The soft turn-off control signal is shown in Fig. 6. At first, the voltage $V_{g_{on}}$ indicates normal operation, after T_{on} overload is detected and the active gate voltage drops to $V_{g_{latch}}$.

Since the drain current continues to increase, it will exceed the threshold, triggering the soft turn-off. The voltage drops from $V_{g_{latch}}$, increasing the switch losses until the fault is completely interrupted.

IV. SIMULATION

The model of the simplified DC system from Fig. 2 utilizing the SSCB in Fig. 3 with the integrated gate driver described in Fig. 4 was implemented in LTspice. The purpose was to achieve relatively high fidelity results and analyze potential components, necessary for a future prototype. The parameters in Table I summarize the system under simulation. The SPICE models of the following components are used in the model.

- Power MOSFET: IPWS65R050CFD7A
- Schottky diode: MBR0520L
- Electrolytic capacitor: 520C562T500DG2B
- High-speed rail-to-rail comparator: TLV3601
- D-flip flop: CD54AC273

To validate the functionalities proposed in Section III, two scenarios were simulated highlighting the effect of each functionality. A) Overload test: to demonstrate the effect of the latch current limiter in a power MOSFET, and B) Short circuit test: to show the soft turn-off of the SSCB.

A. Overload test

To implement the overload, R_{OL} (see Fig. 2) increases the drain current above the overload factor of 20% (Table I). The excess current is detected by the high-speed comparator. Then,

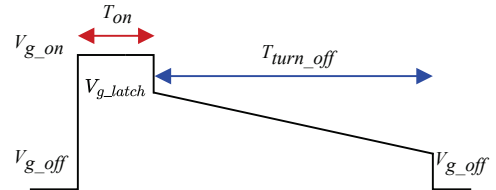


Fig. 6. Gate signal modulation waveforms for SSCB turn-off control using a three-level with ramp turn-off transition.

TABLE I
SYSTEM AND CIRCUIT BREAKER PARAMETERS.

Parameter	Value	Subsystem
Nominal voltage	350 V	Generator
Filter capacitance	17.88 mF	Output filter
Capacitor ESR	1.53 mΩ	Output filter
Parasitic inductance	4 nH	Output filter
Nominal current	10 A	Generator, SSCB
Overload factor	1.2	SSCB
On-resistance (FET)	≈55.9 mΩ	SSCB
On-resistance (Diode)	≈54.9 mΩ	SSCB
Detection inductance	0.75 μH	SSCB
Current latch threshold	>12 A	Gate driver
Current break threshold	40 A	Gate driver
Peak source current	6 A	Gate driver
Peak sink current	4 A	Gate driver
Line inductance	1.32 μH	Load
Load resistance	35 Ω	Load
Overload resistance	118.12 Ω	Overload & fault
Short circuit resistance	10 mΩ	Overload & fault

the signal propagates through the current latch controller and triggers the gate voltage circuit. The gate-source voltage is clamped to a lower value, as shown in Fig. 7, forcing the power MOSFET into the linear region.

Therefore, the conduction resistance increases (see Fig. 7) and the drain current decreases. When the current falls close to its nominal value, the latch resets, allowing the current to rise, attenuating MOSFET losses. The latching will be triggered should the overload condition remain until a temperature alarm activates the breaking. A voltage drop with similar waveform to the drain-source resistance, with peak value at around 180 V is a consequence of the latching. Nevertheless, the effect of such a drop could be limited by its duration (around 69 ns).

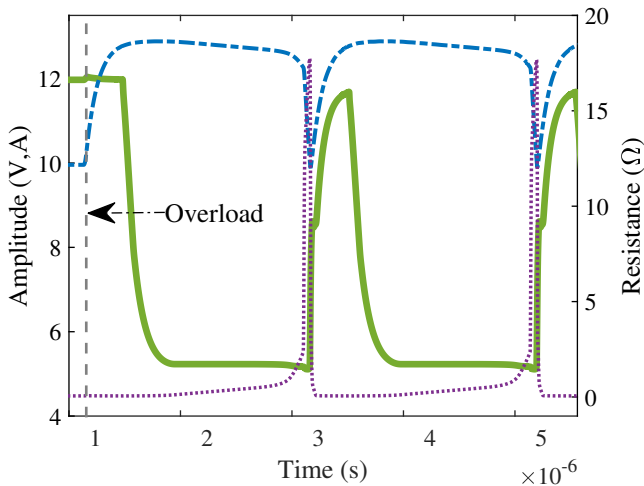


Fig. 7. Simulation of the overloaded DC system using a SSCB with integrated gate driver operating as a latch current limiter. Solid green: gate-source voltage, dashed blue: drain current, dotted purple: drain resistance.

B. Short circuit test

In the short circuit test, the resistance R_{SC} (see Fig. 2) triggers the current latch for a brief interval. Since latching is not sufficient to contain a short circuit fault, the drain current keeps rising until, surpassing the threshold (Table I). The respective high-speed comparator activates a D-latch that interlocks the gate driver. The output stage of the isolated gate driver sinks the energy in the parasitic gate-source capacitor that executes a soft turn-off, as shown in Fig. 8.

The low propagation delay in the considered components allow an expedite current breaking. The fault duration from the occurrence up to the zero current is about 300 ns. The latch delay is about 71 ns, whereas the short circuit detection delay (from the threshold value) is approximately 80 ns. The breaking current process takes about 85 ns from the detection time, and close to 165 ns from threshold surpass. The model accounts for most of the foreseeable propagation delays, resulting in a peak current of 69 A. This value exceeds the nominal of the semiconductor (55 A), but is within the pulsed current maximum of 211 A. The temperature rise in such events is therefore low for the power semiconductor, keeping the operation of the device in a safe range.

V. OUTLOOK AND FUTURE WORK

The widespread deployment of shipboard DC systems can be accelerated with the development of further primary SSCBs. Increasing the perceived value of SSCBs could motivate their implementation in new ship designs. Using SSCBs as latch current limiters with soft turn-off functionality has the potential to boost their value. These capabilities are enabled by the proposed integrated gate driver. The simulation results suggest that the proposed design not only fulfills the requirements, but exceeds the protection capabilities of commercial products.

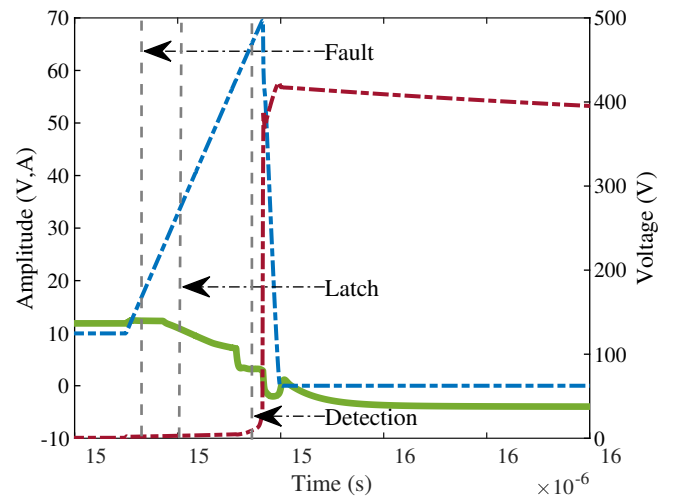


Fig. 8. Simulation of the DC system under a short circuit when using a SSCB with integrated gate driver for current latching and soft turn-off. Solid green: gate-source voltage, dashed blue: drain current, dotted purple (with right-side voltage axis): drain-source voltage.

Future experimental results should demonstrate that it is possible to effectively protect scaled-down DC systems without compromising the system availability. The experimental validation should also confirm the feasibility of short propagation delays, which are critical performance indicators. A combination of different fidelity simulation models, prototyping, and extensive testing are necessary to raise the technology readiness level of the proposed solution.

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