Static and Dynamic Translinear Circuits

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PROEFSCHRIFT

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Introduction

Due to the ongoing trends towards lower supply voltages and low-power operation, the area of *analogue integrated filters* is facing serious challenges. The supply voltage severely restricts the maximum dynamic range achievable using conventional filter implementation techniques, such as opamp-MOSFET-C, transconductance-C and switched-capacitor. In ultra-low-power environments, linear resistors become too large for on-chip integration. The situation is even further complicated by high-frequency demands and the fact that the filter transfer function often has to be tunable.

In the area of *continuous-time* filters, a promising approach to meet these challenges is provided by the class of 'Translinear Filters'. Due to the encouraging expectations, research efforts have increased rapidly and TransLinear (TL) filter design has become a trend. This is illustrated by Fig. 1.1.

Translinear filters were originally introduced by Adams in 1979 [1]. Since Adams at the time did not recognise the TL nature of these circuits, he coined the term 'log-Domain Filters', based on the logarithmic relation between the voltages and currents. For many years, the idea of log-domain filtering was to gather dust. In 1990, Seevinck independently reinvented the TL filter concept, which he called 'Current-mode Companding' [2].

The filters presented by Adams and Seevinck were first-order. Interest in TL filters really took off in 1993, when Frey published a synthesis method enabling the design of higher-order log-domain filters [3]. In addition, Frey proposed a more general class of TL filters, which he termed 'Exponential State-Space Filters' [4].

From that time, many other researchers began to investigate these circuits. Toumazou *et al.* published an implementation in weak inversion MOS, showing the potential for low-power operation [5]. The first experimental results were published by Perry and Roberts [6]. In addition, they proposed an alternative

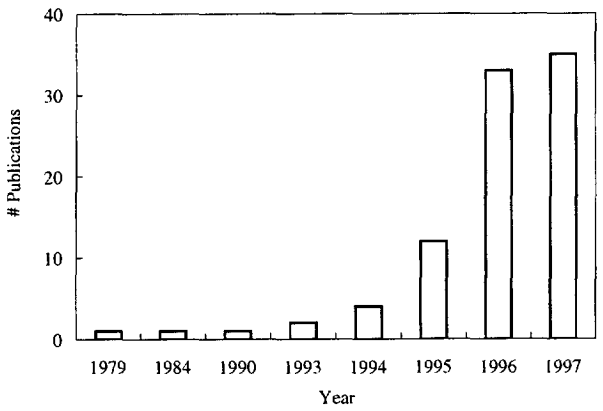

Figure 1.1: Publications on dynamic translinear circuits.

synthesis method based on the simulation of LC ladder filters. The first experimental results in subthreshold MOS were presented by Ngarmnil *et al.* [7]. Punzenberger *et al.* demonstrated the suitability for low-voltage applications [8] and the favourable dynamic range specification resulting from class-AB operation: 65 dB at a 1.2 V supply voltage [9]. Different *synthesis* methods were proposed by various researchers [10–15]. A general *analysis* method was published by Mulder *et al.* [16], who also coined the term 'Translinear Filter'. Alternative analysis methods were described in [14, 17, 18]. Application of the underlying design principle to non-linear dynamic functions was proposed by various researchers. These applications include oscillators [19–21], RMS-DC converters [22, 23], mixer-filter combinations [24, 25] and phase-locked loops [26–28]. A generalisation to strong inversion MOS was proposed independently by Mulder *et al.* [29] and Payne *et al.* [30]. At present, there are many research efforts in the area of noise analysis [31–39] and other second-order effects [40, 41].

Translinear filters are based on the 'Dynamic Translinear Principle' [42], which is a generalisation of the conventional 'Static Translinear Principle' formulated by Gilbert in 1975 [43]. Both Static TransLinear (STL) and Dynamic TransLinear (DTL) circuits exploit specific properties of the exponential function. In STL circuits, the equivalence relation:

$$e^a \cdot e^b = e^{a+b}, \tag{1.1}$$

is used to realise a multiplication in the current domain by an addition in the voltage domain. In DTL circuits, the feature:

$$\frac{de^{x(t)}}{dt} = e^{x(t)} \cdot \frac{dx(t)}{dt}, \tag{1.2}$$

is used to implement the time derivative of a current by means of a product of currents, which in turn is realised by means of eqn (1.1).

Static translinear circuits

The multiplication properties of the exponential function are fundamental to conventional TL circuits. The first TL circuits, a current amplifier and a multiplier, were proposed by Gilbert in 1968 [44, 45]. Gilbert also formulated the (static) 'Translinear Principle' in 1975 [43]. In 1979, Hart formulated a slightly more general form of the TL principle by including PTAT[1] voltage sources in the TL loops [46].

It was soon realised that STL circuits can be used to implement a wide variety of both linear and non-linear *static* transfer functions. Successively, many new circuits were published including: amplifiers [44], multiplier/dividers [45, 47–49], square function [50], square-root function [50], cross quads [51], digital signal processing [52–54], absolute value function [50], sine approximation [43], geometric and harmonic mean functions [50, 55], RMS-DC conversion [56, 57], vector magnitude circuits [43, 58] and frequency-doubling circuits [59, 60].

The design of most of these circuits was based on a heuristic approach. A systematic approach to the analysis and synthesis of STL circuits was developed by Seevinck [50]. Next to [50], overviews on STL circuit design can be found in [61–65].

Most theory and circuit designs were developed during the seventies. In more recent years, STL circuits have experienced a revival due to the trend towards low-voltage and low-power operation. Especially in the area of analogue VLSI (neural) networks, where a high functional density is of primary importance, STL circuits implemented by MOS transistors operated in the weak inversion region have found wide employment, see, e.g., [65, 66].

Voltage-translinear circuits

Translinear circuits are based on the exponential characteristics of the bipolar or subthreshold MOS transistor. In the strong inversion region, the MOS transistor is (approximately) described by a square law. More or less analogous to the class of TL circuits, the square law is the basis of the class of 'Voltage-TransLinear[2]' (VTL) circuits.

Static voltage-translinear circuits Translinear networks consist of closed loops of base-emitter junctions. Likewise, VTL circuits are characterised by

[1] Proportional-To-Absolute-Temperature

[2] The term 'Voltage-Translinear' proposed in [63, 64] is used throughout this thesis as it clearly distinguishes between TL principles based on the exponential law and VTL principles based on the square law, as opposed to the term 'MOS Translinear' proposed in [67].

closed loops of gate-source voltages, and can be used to realise a variety of transfer functions based on the large-signal quadratic behaviour of the MOS transistor, see, e.g., [67–70]. Time-multiplexing techniques can be used to simulate VTL loops owing to the favourable properties of the MOS transistor to implement switches [71, 72]. A formal description of the underlying fundamental design principle was described by Seevinck and Wiegerink in 1991 [67]. The structured analysis and synthesis of VTL circuits was treated in [70].

Dynamic voltage-translinear circuits The class of 'Dynamic Voltage-TransLinear Circuits' offers continuous-time *dynamic* transfer functions. These dynamic VTL circuits are based on a generalisation of the DTL principle to strong inversion MOS. This class of circuits was proposed independently by Mulder *et al.* [29] and Payne *et al.* [30] in 1996. Experimental results were published in [73].

Background of the thesis

Since 1986, the Electronics Research Laboratory of the Delft University of Technology, Faculty of Information Technology and Systems, Department of Electrical Engineering, has had a project group for 'low-voltage low-power electronics'. As TL circuits and subthreshold MOS transistors are especially useful in this area of analogue electronics, a project was initiated to explore the use of subthreshold MOS transistors in TL circuits. In particular, the application of the back-gate was to lead to additional possibilities for low-voltage operation and to result in TL circuits with a higher functional density.

During the course of this project, DTL circuits became an active field of research, see Fig. 1.1, and investigations were extended in this direction. As a result, this thesis now deals with structured methodologies for the analysis and synthesis of both STL and DTL circuits.

Some of the work described in this thesis has been published in various papers, which are listed on page 283.

Outline of the thesis

The TL and VTL principles are explained in Chapter 2 using a current-mode approach. Dynamic translinear and dynamic voltage-translinear filters are members of a more general class of 'externally-linear internally-non-linear' circuits, which is therefore discussed first.

Chapter 3 discusses the analysis of TL circuits. First, the analysis of STL circuits is reviewed. Based on this theory, two methods, called 'global analysis' and 'state-space analysis', are developed for the analysis of DTL circuits. Alternative analysis methods for DTL circuits proposed in the literature are

described as well. In addition, the characteristics of the three different classes of DTL circuits published to date are analysed.

The reverse process of analysis is synthesis, which is treated in Chapter 4. Based on the synthesis theory of STL networks, a generalised design methodology is presented covering the synthesis of both STL and DTL circuits. A comparison is made with a number of alternative synthesis methods for TL filters described in the literature. Further, the concept of class-AB operation, which is closely related to synthesis, is treated.

The synthesis method described in Chapter 4 is based on ideal transistor behaviour. In Chapter 5, the deviations introduced by second-order effects are discussed. Methods to reduce or even eliminate the influences of these non-idealities are reviewed.

Noise is the topic of Chapter 6. The signal-to-noise-ratio and dynamic range properties of TL circuits are discussed and methods for the analysis of noise in both STL and DTL circuits are proposed. These methods incorporate the non-linear and non-stationary aspects of noise in TL circuits.

Chapter 7 is devoted to VTL circuits. Arguments are given to show that VTL circuits do not have much practical value.

Several realisations of TL and VTL circuits are presented in Chapter 8.

Finally, Chapter 9 concludes the thesis.

2

Design principles

The continuing trend towards lower supply voltages has increased interest in the application of companding[1] techniques [2,8,29,31,74–78]. This chapter discusses the design principles that are fundamental to the realisation of companding signal processors. In Section 2.1, an abstract approach is pursued to describe the general principle of distortionless companding. At a less abstract level, Sections 2.2 and 2.3 are geared toward the inherent companding characteristics of TransLinear (TL) and Voltage-TransLinear (VTL) circuits, respectively.

2.1 A general approach to companding

In a system employing companding, the Dynamic Range[2] (DR) of the signal being processed is different at various points along the signal path. The DR is altered by compression and expansion stages. The traditional set-up of a companding system is shown in Fig. 2.1(a). The input signal is first compressed, in block $\mathcal{C}$, before it is applied to $\mathcal{H}$, where the actual signal processing is performed. At the output of $\mathcal{H}$, the DR of the original input signal is restored through an expansion in block $\mathcal{E}$.

The benefit of companding is that a signal with a certain DR can be processed in a system block with a smaller DR than the signal [74]. This is illustrated in Fig. 2.1(b). The DR of a signal processing block $\mathcal{H}$ is limited on two sides. At the upper level, the maximum amplitude of the input signal is limited by the generation of distortion for too large signals. At the lower level, the noise floor of the block determines the smallest signals that can be processed. Since the DR is limited on two sides, the influence of companding on the signal being

[1] *Companding* is a combination of *com*pressing and ex*panding*.

[2] The exact definitions of the dynamic range and the signal-to-noise ratio used throughout this thesis are formulated in Section 6.1.

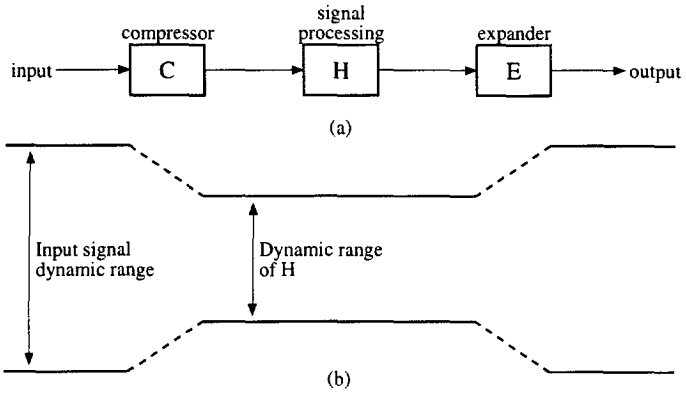

Figure 2.1: (**a**) Traditional set-up of a companding system. (**b**) The dynamic range of the signal along the signal path.

processed can be explained from two points of view. At the upper level, large input signals are attenuated by the compressor $\mathcal{C}$ down to a level where they can be processed by $\mathcal{H}$ without causing excessive distortion. At the lower level, small input signals are amplified by $\mathcal{C}$ to a level well above the noise floor of $\mathcal{H}$, making the signal less susceptible to noise and interference.

Syllabic and instantaneous companding

Companding systems can be divided into two major classes: syllabic and instantaneous. These two classes differ with respect to the nature of the compression and expansion functions.

In a syllabic companding system, the transfer function of $\mathcal{C}$ is determined by a compression *signal*, which is a function of some measure of the average strength of the signal being processed. The compression signal can be derived from the processed signal at any stage of the signal path, e.g., from the input or output, or even from a companion system with scaled signals [75]. A simple example of a compression signal is the envelope of the input signal, which can be generated through rectification followed by low-pass filtering.

In an instantaneous companding system, the output of $\mathcal{C}$ is a function of the instantaneous value of the input signal. In other words, the transfer function of the compressor is static and non-linear. An example is the logarithmic I-V conversion performed at the input of a TL filter.

Distortion

Companding methods cannot be applied without due caution. In the compressor, the DR of the input signal is decreased. This is a non-linear function and as a result harmonics of the input signal are generated. Nevertheless, the linearity of the overall transfer function of the complete signal path, shown in Fig. 2.1, can still be retained. A linear overall transfer function is obtained if the transfer function of $\mathcal{H}$ is linear and frequency-independent, and the compression and expansion functions are inverse functions, i.e., $\mathcal{C} \circ \mathcal{E} = 1$.

In practice, not only the DR, but also the bandwidth of $\mathcal{H}$ will be limited, resulting in a frequency-dependent transfer function. This limited bandwidth can be unwanted when it is caused by parasitic reactive elements. It can also be intentional, e.g. when the function of the complete system is to filter the input signal in the frequency domain. The frequency-dependent transfer function of $\mathcal{H}$ does not comply with the redistribution of the input signal information across the frequency spectrum by $\mathcal{C}$. As a result, distortion arises, even when $\mathcal{C} \circ \mathcal{E} = 1$.

The generation of distortion can also be explained with respect to the memory elements present in $\mathcal{H}$ [76, 79]. In the memory elements, the history of the signal is stored. The state of $\mathcal{H}$ not only depends on the course of the processed signal, but also on the value of the (small-signal) gain of the compressor. If the compression gain changes in time, which is the case in a companding system, the coherence between the state of $\mathcal{H}$ and the history of the processed signal is lost.

Updating the state variables

To prevent the generation of distortion, the one-to-one relation between the state of $\mathcal{H}$ and the processed signal has to be re-established. This is realised by updating the state variables in $\mathcal{H}$ as a function of the time-variant compression gain [76, 79]. This applies both to syllabic and instantaneous companding systems.

The theory on distortionless syllabic companding is closely related to early work in control system theory (see [31] for an overview). The application of this theory at circuit level was first proposed by Blumenkrantz in 1994 in [76, 79], where the idea of updating the state variables, the 'Analog Floating Point Technique', is described. Implicitly, distortionless instantaneous companding at circuit level was described earlier, by Adams in 1979 in [1], where log-domain filters are introduced.

In [75], a general model for distortionless companding systems is described by Tsividis. The model incorporates both syllabic and instantaneous companding, showing that both types of distortionless companding are in fact based on the same mechanism of updating the state variables.

In the following, a general model of distortionless companding systems is described. The approach will be somewhat different from the one presented in [75].

A first-order model

For a signal processor having a frequency-dependent transfer function, two basic functions are required to describe the process of distortionless companding. First, a dynamic transfer function is required because the distortion is caused by the frequency-dependent transfer function of $\mathcal{H}$. To gain insight, it is convenient to consider a first-order dynamic system. Further on, the results are generalised to higher-order dynamic systems. A first-order dynamic transfer function can be modelled by a single linear integrator.[3] The input and output signals of this internal integrator are denoted by $\dot{x}$ and x, respectively, where the dot represents differentiation with respect to time.

Secondly, compression and expansion functions are required. It is sufficient to model only the expansion function E, since the accompanying compression function can be derived from E. The input signal of E is the output signal x of the integrator. The output signal of E is denoted by y. The basic model thus obtained is shown in Fig. 2.2.

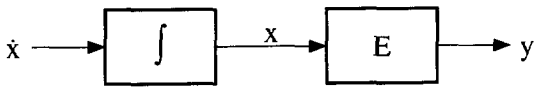

Figure 2.2: The two basic functions of a companding integrator.

The expansion function E is directly related to the type of companding. Therefore, in order to obtain a general model, both instantaneous and syllabic expansion functions have to be accommodated.

In an instantaneous companding system, the output signal y is a function of the instantaneous value of the integrator output x. Since all signals are implicitly a function of time t, the output y can be described as: $y(t) = E(x(t))$. For example, in a log-domain filter, the expansion function is given by $y(t) = \exp x(t)$.

In a syllabic companding system, the expansion function is controlled by one or more time-variant signals $g_i(x(t), t)$, where $i \in [1, \ldots, N]$, which can be represented by the column vector $\vec{g}$. Thus, $\vec{g}(x(t), t)$ is a vector function. For example, in a traditional set-up, the expansion block is a variable gain amplifier, controlled by a single time-variant expansion factor $g(x(t), t)$, i.e., $y(t) = g(x(t), t) \cdot x(t)$.

[3] In principle, other first-order dynamic transfer functions, such as a differentiator, can be used here just as well. The choice of an integrator complies with the general application of the integrator as the basic building block for filters [80,81].

The general model for the transfer function E of the expander $\mathcal{E}$, including both instantaneous and syllabic companding, is given by:

$$y(t) = E\left(x(t), \vec{g}(x(t), t)\right). \tag{2.1}$$

In principle, $E = E(x(t), t)$ is an equally valid representation. However, eqn (2.1) clearly distinguishes between the two different types of companding.

The possible choices of E are restricted by the fact that, at all times, i.e., for all possible values of the signals g_i, E has to be a strictly monotonous function with respect to x. Otherwise, when different values of x are projected onto the same value of y, information is lost, resulting in irrecoverable distortion. As a consequence, at all times the function E has an inverse function E^{-1} given by:

$$x(t) = E^{-1}\left(y(t), \vec{g}(x(t), t)\right). \tag{2.2}$$

The correct input signal

At the input of the internal integrator, shown in Fig. 2.2, the signal $\dot{x}$ has to be supplied. The question is what this signal should look like in order to obtain a system with a linear transfer function from $\dot{y}$ to y, the input and output signal, respectively, of the complete companding integrator. The correct signal $\dot{x}$ can be calculated from the expansion function.

An expression for $\dot{y}$ can be derived from eqn (2.1) by calculating the first derivative with respect to time. Since E is only implicitly a function of time, the chain rule has to be applied. This yields:

$$\dot{y} = \frac{\partial E}{\partial x}\dot{x} + \nabla_g E \cdot \left(\frac{\partial \vec{g}}{\partial x}\dot{x} + \dot{\vec{g}}\right), \tag{2.3}$$

where

$$\nabla_g E = \left(\frac{\partial E}{\partial g_1}, \ldots, \frac{\partial E}{\partial g_N}\right).$$

From eqn (2.3), the signal $\dot{x}$, to be applied to the internal linear integrator, can be found:

$$\dot{x} = \frac{\dot{y} - \nabla_g E \cdot \dot{\vec{g}}}{\frac{\partial E}{\partial x} + \nabla_g E \cdot \frac{\partial \vec{g}}{\partial x}}. \tag{2.4}$$

Figure 2.3 shows the system level implementation of this equation, resulting in a theoretically distortionless companding integrator.

Alternatively, applying the inverse function theorem, $\dot{x}$ can be calculated from eqn (2.2). The first-order time derivative yields:

$$\dot{x} = \frac{\frac{\partial E^{-1}}{\partial y}\dot{y} + \nabla_g E^{-1} \cdot \dot{\vec{g}}}{1 - \nabla_g E^{-1} \cdot \frac{\partial \vec{g}}{\partial x}}. \tag{2.5}$$

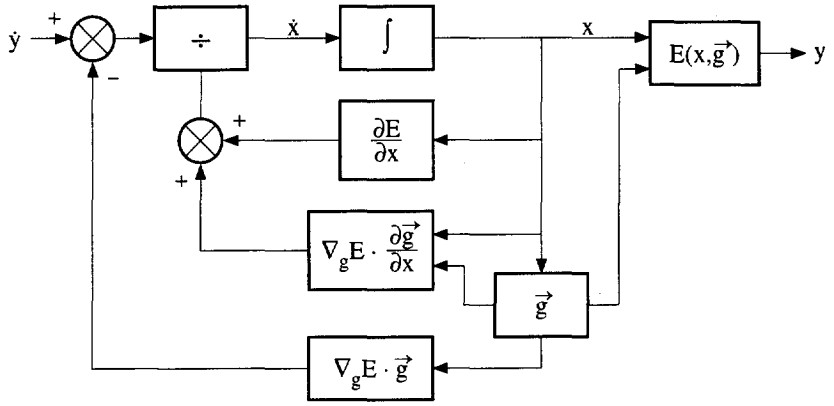

Figure 2.3: Realisation of a theoretically distortionless companding integrator.

This equation results in a different system level implementation.

An n^{th}-order model

In general, the dynamic transfer function to which companding is applied is of order n. The dynamic behaviour of the internal signal processing block can now be represented by n integrators. The inputs and outputs of these internal integrators are described by the column vectors $\dot{\vec{x}}$ and $\vec{x}$, the elements of which are $\dot{x}_j$ and x_j, respectively, where $j \in [1, \ldots, n]$. In principle, expansion can be applied to each of these integrators, resulting in n output signals y_j, represented by the vector $\vec{y}$. The expansion function does not have to be identical for each of the outputs x_j. In general, n different expansion functions E_j, represented by the vector function $\vec{E}$, can be defined. Each expansion function can depend on the complete state of the system, i.e., on all n state variables x_j. In general, the expansion vector $\vec{E}$ can be described by:

$$\vec{y}(t) = \vec{E}\left(\vec{x}(t), \vec{g}(\vec{x}(t), t)\right). \tag{2.6}$$

The correct input vector

The input vector $\vec{x}$, to be supplied to the n internal integrators, in order to realise a system of n linear companding integrators, can be derived from eqn (2.6) by calculation of the first-order time derivative. This yields:

$$\dot{\vec{y}} = \mathrm{E}_x \dot{\vec{x}} + \mathrm{E}_g \left(\mathrm{G}_x \dot{\vec{x}} + \dot{\vec{g}}\right), \tag{2.7}$$

where E_x, E_g, and G_x are Jacobian matrices given by:

$$\mathrm{E}_x = \begin{bmatrix} \frac{\partial E_1}{\partial x_1} & \cdots & \frac{\partial E_1}{\partial x_n} \\ \vdots & & \vdots \\ \frac{\partial E_n}{\partial x_1} & \cdots & \frac{\partial E_n}{\partial x_n} \end{bmatrix}, \quad \mathrm{E}_g = \begin{bmatrix} \frac{\partial E_1}{\partial g_1} & \cdots & \frac{\partial E_1}{\partial g_N} \\ \vdots & & \vdots \\ \frac{\partial E_n}{\partial g_1} & \cdots & \frac{\partial E_n}{\partial g_N} \end{bmatrix},$$

$$\mathrm{G}_x = \begin{bmatrix} \frac{\partial g_1}{\partial x_1} & \cdots & \frac{\partial g_1}{\partial x_n} \\ \vdots & & \vdots \\ \frac{\partial g_N}{\partial x_1} & \cdots & \frac{\partial g_N}{\partial x_n} \end{bmatrix}.$$

Expression (2.7) is a linear system in the n derivatives $\dot{x}_j$. The system can be solved for the vector $\dot{\vec{x}}$:

$$\dot{\vec{x}} = (\mathrm{E}_x + \mathrm{E}_g \mathrm{G}_x)^{-1} \left(\dot{\vec{y}} - \mathrm{E}_g \dot{\vec{g}} \right), \tag{2.8}$$

where '$^{-1}$' denotes the inverse matrix operation.

Examples

The practical applicability of the distortionless companding principle cannot be derived from the general and abstract approach used above. The specific choice of the expansion function(s) and of the dimensions of the signals being processed will strongly influence to what extent a companding system is suitable for on-chip implementation. To conclude this section, some practical examples of distortionless companding systems are mentioned.

Dynamic translinear circuits Translinear filters, or Dynamic TransLinear (DTL) circuits in general, form a good example of instantaneous companding. In DTL circuits, the internal integrator, shown in Fig. 2.2, is a linear capacitor. The output of this integrator is expanded by exploiting the large-signal exponential transfer function of the bipolar transistor or the MOS transistor in the weak inversion region. The expansion function is different for the various classes of DTL circuits. For example, it is given by $y(t) = \exp x(t)$ [1], $y(t) = \tanh x(t)$ and $y(t) = \sinh x(t)$ [10] for log-domain, tanh and sinh filters, respectively. The principle behind DTL circuits is treated in more detail in Section 2.2.2.

Dynamic voltage-translinear circuits Another example is given by the class of Dynamic Voltage-TransLinear (DVTL) circuits, which are also instantaneous companding. In DVTL circuits, again, the internal integrator is a linear capacitor. The output of this integrator is expanded by exploiting the large-signal quadratic behaviour of the MOS transistor in the strong inversion region. For a common-source output stage, the expansion function is given by

$y(t) = [x(t) - a]^2$ [29], where a is a constant. The principle behind DVTL circuits is treated in more detail in Section 2.3.2.

Syllabic companding Examples of syllabic companding systems are described in [75, 76, 79, 82], where the expansion function is given by $y(t) = g(t)x(t)$. The systems differ mainly in the way the signal $g(t)$ is generated. In [76, 79], where syllabic companding is applied to a $\Sigma\Delta$ analogue-to-digital converter and an operational-transconductance-amplifier-based filter, $g(t)$ is switched between different ranges. Within each range, $g(t)$ is constant. At the switching instants, the state variables are updated by a compensation term, which has the shape of an impulse function. This impulse function can be implemented by a switched capacitor. A syllabic companding filter with a continuously varying compression factor $g(t)$ is described in [75, 82].

Instantaneous and syllabic companding Combinations of instantaneous and syllabic companding within one circuit are also possible [78, 83, 84]. An example is the syllabic companding TL filter described in Section A.1. Since TL filters are inherently instantaneous companding, the two types of companding are co-existent in a syllabic companding TL filter. Hence, the expansion function is given by $y(t) = g(t) \exp x(t)$.

Non-linear capacitor The last case described here considers a non-linear capacitor. Virtually, in a non-linear capacitor, the two functions of integration and expansion, shown in Fig. 2.2, are performed in one device. The relation between the input current I_{cap} and the charge Q on the capacitor is linear and is given by $I_{\text{cap}} = \dot{Q}$. This equation describes a linear integration. The non-linear behaviour of a non-linear capacitor only applies to the relation between Q and the voltage V_{cap} across the capacitor. Consequently, the transfer function of a non-linear capacitor can be split into two functions: a linear integrator followed by a non-linear static transfer function, the differential capacitance $C(V_{\text{cap}}) = \partial Q / \partial V_{\text{cap}}$. This static function can be regarded as the expansion function shown in Fig. 2.2.

An interesting example of a non-linear capacitor is the base-emitter capacitance C_π of a bipolar transistor in the region where the base-charging capacitance is dominant [85]. In this region, the logarithmic non-linearity of the diffusion capacitance is cancelled by the exponential V-I transfer function of the bipolar transistor, resulting in a theoretically linear integrator.

2.2 Translinear principles based on the exponential law

Both Static TransLinear (STL) and DTL circuits exploit the exponential large-signal transfer function of the bipolar transistor or the MOS transistor in the weak inversion region. The term 'translinear' is derived from the equation for the small-signal transconductance g_m of a bipolar transistor, given by:

$$g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{I_C}{U_T}, \tag{2.9}$$

where I_C is the collector current, V_{BE} is the base-emitter voltage and U_T is the thermal voltage kT/q. Equation (2.9) shows that the *trans*conductance is *linear* in the collector current.

The conventional, i.e., static, TL principle [43] can be used to implement a wide variety of linear and non-linear static transfer functions [50]. The STL principle is reviewed in Section 2.2.1.

The DTL principle [22] can be used to implement both linear and non-linear, frequency-dependent functions, i.e., linear and non-linear Differential Equations (DEs). The DTL principle can be regarded as a generalisation of the STL principle. In a broader context, DTL circuits are based on the theory of distortionless companding described in Section 2.1. The dynamic element is the capacitance. The exponential function, or a composite exponential function, is employed as the expansion function, which expands a capacitance voltage into a transistor current. In Section 2.2.2, the DTL principle is described using a current-mode point of view.

2.2.1 Static translinear principle

Although invented as early as 1968 [44,45], the (static) TL principle was first formulated by Gilbert in 1975 [43]. Translinear circuits are based on the exponential relation between voltage and current, characteristic for several semiconductor devices, such as the bipolar transistor, the diode and the MOS transistor in the weak inversion region.

In this section, the STL principle is explained using the expression for the collector current I_C of the bipolar transistor. The important difference between bipolar transistors and MOS transistors in the weak inversion region is the slope of the exponential characteristic. The slope of the MOS transistor is characterised by the process-dependent parameter n [86], whereas the slope of the bipolar transistor is almost process-independent. With some minor modifications, the following theory is equally applicable to subthreshold MOS transistors.

The collector current of a bipolar transistor in the active region is given by:

$$I_C = \lambda I_S e^{\frac{V_{BE}}{U_T}}, \tag{2.10}$$

where λ is the emitter area scale factor and I_s is the saturation current of the unity transistor.

The STL principle applies to loops of semiconductor junctions with an exponential V-I relation. The slope of the exponential function has to be the same for all devices. A TL loop is characterised by an even number of junctions. The number of devices with a clockwise orientation equals the number of counter-clockwise oriented devices. Further, all devices have to operate at the same temperature.

An example of a four-transistor TL loop is shown in Fig. 2.4. It is assumed that the transistors are somehow biased at the collector currents I_1 through I_4. As the four transistors are connected in a loop, Kirchhoff's Voltage Law (KVL) can be used to describe the loop:

$$V_{\mathrm{BE}_1} + V_{\mathrm{BE}_3} = V_{\mathrm{BE}_2} + V_{\mathrm{BE}_4}. \tag{2.11}$$

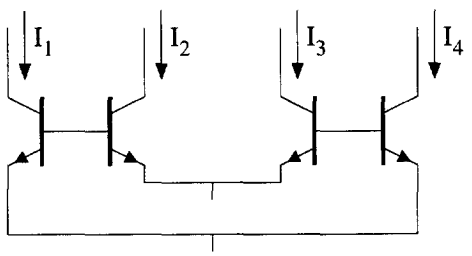

Figure 2.4: A four-transistor translinear loop.

Current-mode

Translinear circuits are typical examples of current-mode circuits [87]. That is, the behaviour of a TL circuit can be described best in terms of currents. The voltages are only of secondary interest. The voltage-mode description (2.11) can be transformed into a current-mode description using the exponential law (2.10) describing the bipolar transistor. This yields:

$$U_T \ln \frac{I_1}{\lambda_1 I_s} + U_T \ln \frac{I_3}{\lambda_3 I_s} = U_T \ln \frac{I_2}{\lambda_2 I_s} + U_T \ln \frac{I_4}{\lambda_4 I_s}, \tag{2.12}$$

where λ_i are the emitter area scale factors of the four transistors.

Since all transistors are supposed to operate at the same temperature, the slope of the exponential function, represented by U_T, is the same for all transistors. Therefore, the factor U_T can be eliminated from eqn (2.12). Further, the sum of two logarithmic functions equals the logarithm of the product of the

two arguments of these functions. Eqn (2.12) can thus be simplified to:

$$\ln \frac{I_1 I_3}{\lambda_1 \lambda_3 I_s^2} = \ln \frac{I_2 I_4}{\lambda_2 \lambda_4 I_s^2}. \tag{2.13}$$

The logarithm is easily eliminated from eqn (2.13).

The saturation current I_s is equal for all transistors, owing to the identical operating temperature.[4] The powers to which I_s is raised in the denominator at both sides of eqn (2.13) are equal to the numbers of devices in the TL loop connected clockwise and counter-clockwise, respectively. As these numbers are equal, I_s can be eliminated. This finally yields the familiar representation of TL loops in terms of products of collector currents:

$$I_1 I_3 = \lambda_{eq} I_2 I_4, \tag{2.14}$$

where $\lambda_{eq} = \lambda_2 \lambda_4 / (\lambda_1 \lambda_3)$ is the equivalent area ratio of the TL loop.

Application

Equation (2.14) shows that the STL principle can be used to implement the arithmetic operations of multiplication and division. The operations of addition and subtraction are easily implemented in the current-domain. Using the addition and subtraction operations, linear combinations of the input and output currents can be forced through the transistors comprising a TL loop. In combination with the multiplication and division operations supplied by the TL loop, a wide variety of polynomials $\mathcal{P}_m$, rational functions $\mathcal{P}_m/\mathcal{P}_n$ and n^{th}-order root functions can be realised.

Some of the major advantages of TL circuits follow directly from eqn (2.14). During the derivation of the STL principle, all temperature-dependent and process-dependent constants, i.e., U_T and I_s, are eliminated. As a consequence, the transfer function implemented by a STL circuit is theoretically temperature and process-independent. Further, a multiplication is implemented using a very simple circuit, the TL loop shown in Fig. 2.4. Thus, TL circuits are characterised by a very high functional density.

To conclude, the STL principle can be summarised in the following definition due to Gilbert [43]:

"A translinear circuit is one having inputs and outputs in the form of currents and whose primary functions arises from the exploitation of the proportionality of transconductance to current in certain electronic devices so as to result in fundamentally exact, temperature-insensitive algebraic transformations."

[4] In principle, paired matching of the saturation currents is a sufficient condition.

2.2.2 Dynamic translinear principle

Though very versatile, the STL principle, derived in Section 2.2.1, is limited to frequency-independent transfer functions. By admitting capacitors in the TL loops, the TL principle can be generalised to include frequency-dependent transfer functions. To name the principle on which this new class of circuits is based, the term 'Dynamic Translinear Principle' was coined by Mulder *et al.* in [22]. This term was chosen to emphasise the TL nature of these circuits.

As a consequence of the exponential behaviour of the transistor, TL circuits are inherently instantaneous companding. The voltages in a TL circuit are logarithmically related to the currents. Due to this non-linear behaviour, adding a capacitor to a TL loop will in most cases result in severe distortion.

Current mirror

As an example, the generation of harmonic distortion is illustrated for the most simple TL circuit: the current mirror. Figure 2.5 shows a current mirror in which a capacitor C is connected in parallel with the diode-connected input transistor. The capacitor can be regarded as the internal integrator and the output transistor as the expander of a companding system, as shown in Fig. 2.2. The current mirror is biased in class A by a dc bias current I_{dc}; the ac input current I_{in} is superposed on I_{dc}.

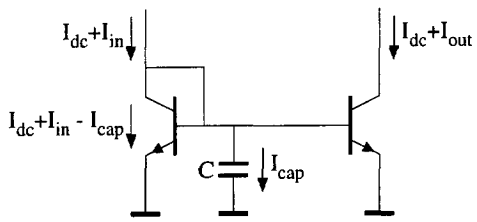

Figure 2.5: A capacitor added to a current mirror.

For very small values of I_{in}, the transconductance g_m of each of the two transistors comprising the current mirror is approximately constant. In that case, the transfer function from the capacitance voltage swing to the ac output current I_{out} is linear. Consequently, the transfer function of the current mirror is described by a linear DE:

$$\frac{CU_T}{I_{\mathrm{dc}}}\dot{I}_{\mathrm{out}} + I_{\mathrm{out}} = I_{\mathrm{in}}. \tag{2.15}$$

The transfer function described by eqn (2.15) is that of a first-order low-pass filter.

For large input signal swings, the exponential expansion realised by the output transistor cannot be approximated by a linear transconductance. As a result, to accurately describe the transfer function of the current mirror, a non-linear DE is required. A general analysis method is presented in Chapter 3. For the circuit shown in Fig. 2.5 this results in:

$$CU_T\dot{I}_{\text{out}} + (I_{\text{dc}} + I_{\text{out}})\, I_{\text{out}} = (I_{\text{dc}} + I_{\text{out}})\, I_{\text{in}}. \tag{2.16}$$

Figure 2.6 shows a large-signal ac simulation of the transfer function of the current mirror, and HD_2 and HD_3, the second and third-order harmonic distortion components, respectively. The simulation is based on a harmonic balance method. In the simulation, the amplitude of I_{in} is 90% of I_{dc}, I_{dc} is 50 μA and C is 300 pF. Significant distortion is evident from the results shown.

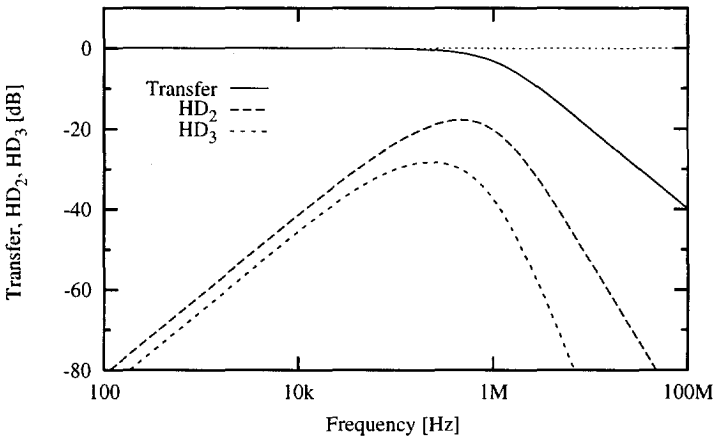

Figure 2.6: Large-signal simulation of the transfer function, HD_2 and HD_3 of the current mirror shown in Fig. 2.5.

Distortionless companding

To prevent distortion in DTL circuits, the general principle described in Section 2.1 has to be obeyed. The DTL principle is a special case of this general principle, which applies to TL circuits. Instead of the abstract approach used in Section 2.1, a more practical approach is used here to derive the DTL principle. More specifically, a current-mode approach is used.

The exponential function has two very favourable characteristics. First, multiplication of two exponential functions e^a and e^b is equivalent to addition of the two arguments a and b, see eqn (1.1). This characteristic is exploited in

the STL principle. Second, the derivative of an exponential function equals the exponential function itself, see eqn (1.2). This characteristic is the basis of the DTL principle.

To calculate the derivative of eqn (2.10) for I_C with respect to time, the chain rule has to be applied, as V_{BE} is a function of time. This results in:

$$\dot{I}_C = I_C \frac{\dot{V}_{BE}}{U_T}. \tag{2.17}$$

The derivative $\dot{V}_{BE}$ of the base-emitter voltage is very similar to the constitutive law describing a capacitance C. The relation between the capacitance current I_{cap} and capacitance voltage V_{cap} is given by:

$$I_{cap} = C\dot{V}_{cap}. \tag{2.18}$$

When $\dot{V}_{BE}$ in eqn (2.17) is multiplied by C, the product $C\dot{V}_{BE}$ can be regarded as the current through a capacitance C with a voltage V_{BE} applied across it. This is illustrated in Fig. 2.7. Note that the dc voltage source V_{const} does not influence the capacitance current. Thus, eqn (2.17) can be written as:

$$CU_T\dot{I}_C = I_C \cdot C\dot{V}_{BE}, \tag{2.19}$$

$$= I_C \cdot I_{cap}. \tag{2.20}$$

Note that the dimension of both sides of eqn (2.20) equals [A^2].

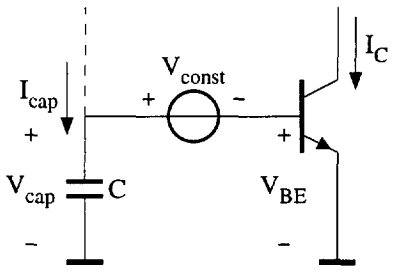

Figure 2.7: Principle of dynamic translinear circuits.

Equation (2.20) directly states the DTL principle [22]: "A time derivative of a current is equivalent to a product of currents." At this point, the conventional STL principle comes into play. The product of currents on the Right-Hand Side (RHS) of eqn (2.20) can be realised very elegantly by means of this principle.

Equation (2.20) was derived for the structure shown in Fig. 2.7, which is typical for the class of log-domain filters. For these filters, the derivative is equivalent to the product of a capacitance current and one collector current. The principle is equally valid for other classes of TL filters, such as tanh and sinh filters. As shown in Section 3.3, these cases differ with respect to the currents comprising the product at the RHS of eqn (2.20).

Application

The DTL principle can be used to implement DEs. A wide variety of signal processing functions is described by DEs. For example, filters are described by linear DEs. Examples of non-linear DEs for signal processing are harmonic and chaotic oscillators, PLLs and RMS-DC converters.

Addition, multiplication and linear derivatives are basic functions in DEs. The additions are easily implemented in the current domain. The multiplication operation can be implemented using the STL principle. To implement the derivatives, the DTL principle can be applied. A derivative is replaced by a product of currents, which is implemented by means of the STL principle.

Equation (2.20) reveals yet another characteristic of DTL circuits. In general, TL loops can be described by current-mode polynomials [50]. As shown in detail in Chapter 3, the relation between these current-mode polynomials and the DEs describing the transfer functions of DTL circuits is given by equations like (2.20). If the RHS of eqn (2.20) is implemented by (part of) a TL loop then the Left-Hand Side (LHS) is (part of) the DE describing the dynamic transfer function realised, which implies that the term CU_T is part of the DE. As a consequence, the transfer function becomes temperature-dependent through U_T. Fortunately, this temperature-dependence can be cancelled by making (some of) the currents in the DTL circuit PTAT[5] [1,2].

Inductance

For theoretical completeness, it is interesting to investigate the possible application of an inductance instead of a capacitance as the dynamic element in a TL circuit. When an inductance L is used, eqn (2.17) has to be compared to the constitutive law of inductance given by:

$$U_L = L\,\dot{I}_L, \tag{2.21}$$

where U_L and I_L are the inductance voltage and current, respectively.

In this case, the derivative $\dot{I}_C$ of the collector current can be identified with the derivative $\dot{I}_L$ of the current through the inductance. Applying this identification to eqn (2.17) yields:

$$\frac{L}{U_T}\dot{V}_{BE} = \frac{U_L}{I_C}. \tag{2.22}$$

This equation states that the derivative of a voltage is equivalent to the division of a voltage by a collector current. As the RHS of this equation is not current-mode, it cannot be implemented by TL circuitry. The only solution is to convert U_L into a current using a transconductance. However, in that case,

[5] Proportional-To-Absolute-Temperature

the inductance and the transconductance operate in the 'linear domain', not in the 'translinear domain'.

2.3 Voltage-translinear principles based on the square law

In the strong inversion region, the MOS transistor can be modelled by a square law. The validity of the square law model is not as good as the exponential law for the bipolar transistor. Especially not in modern sub-micron IC processes, where velocity saturation dominates almost the entire strong inversion region. This issue is treated in more detail in Section 7.1.

In IC processes where the square law is still valid, the MOS transistor can be used to implement a second type of TL circuits. In [64], the term 'Voltage-Translinear' was proposed. This term is derived from the equation for the small-signal transconductance g_m of the MOS transistor in the strong inversion region, given by:

$$g_m = \frac{\partial I_{\mathrm{DS}}}{\partial V_{\mathrm{GS}}} = \beta \left(V_{\mathrm{GS}} - V_{\mathrm{th}} \right), \tag{2.23}$$

where I_{DS} is the drain-source current, V_{GS} is the gate-source voltage, β is the transconductance factor and V_{th} is the threshold voltage. Equation (2.23) shows that the *trans*conductance is *linear* with the gate-source excess *voltage*.

Voltage-translinear circuits can be regarded as another special case of the general theory on distortionless companding treated in Section 2.1. In DVTL circuits, the dynamic element is the capacitor. The square law of the MOS transistor is applied as the expansion function. The DVTL principle can also be regarded as a generalisation of the conventional Static Voltage-TransLinear (SVTL) principle. Therefore, the SVTL principle is first reviewed in Section 2.3.1. The DVTL principle is derived in Section 2.3.2.

2.3.1 Static voltage-translinear principle

The VTL principle was first formulated by Seevinck and Wiegerink in 1991 [67]. Circuits based on this principle were however reported earlier. A linear transconductance is reported by Nedungadi in [68], published in 1984, which is based on a loop of four MOS transistors operating in the strong inversion region. The input of this transconductance circuit is a voltage and not a current. However, whereas current-mode input and output signals are fundamental in TL circuits based on the exponential function, voltage-mode input and output signals are allowed in VTL circuits. This is due to a fundamental difference between the exponential function and the quadratic function. The exponential

function is transcendental, whereas the quadratic function is a polynomial. As a consequence, it is impossible to obtain a linear relation between voltage and current using only exponential devices. For quadratic devices such a linear relation can be realised.

In general, the SVTL principle applies to loops of MOS transistors operated in the strong inversion region. A VTL loop is characterised by an even number of devices. The numbers of transistors connected clockwise and counter-clockwise are equal. Further, the transistors have to operate at the same temperature. Figure 2.8 shows an example of a four-transistor VTL loop. The transistors are assumed to be biased by currents I_1 through I_4.

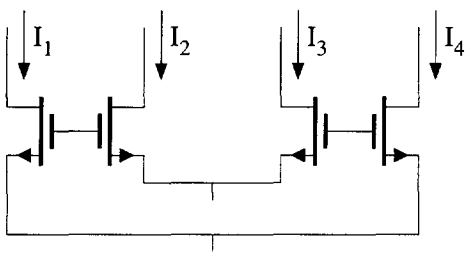

Figure 2.8: A four-transistor voltage-translinear loop.

The circuit shown in Fig. 2.8 can be described by the KVL as the four gate-source voltages V_{GS_1} through V_{GS_4} are connected in a loop:

$$V_{GS_1} + V_{GS_3} = V_{GS_2} + V_{GS_4}. \tag{2.24}$$

The MOS transistors comprising the loop are characterised by a quadratic relation between the gate-source voltage V_{GS} and the drain current I_{DS}. The square law model is given by:

$$I_{DS} = \frac{\beta}{2}(V_{GS} - V_{th})^2. \tag{2.25}$$

The transconductance factor β is given by:

$$\beta = \beta_{\square}\frac{W}{L},$$

where $\beta_{\square}$ is the unity transconductance factor and W/L is the aspect ratio.

Current-mode

A current mode description of the loop shown in Fig. 2.8 can be obtained by substitution of eqn (2.25) in (2.24). This yields:

$$V_{\text{th}} + \sqrt{\frac{2I_1}{\beta_1}} + V_{\text{th}} + \sqrt{\frac{2I_3}{\beta_3}} = V_{\text{th}} + \sqrt{\frac{2I_2}{\beta_2}} + V_{\text{th}} + \sqrt{\frac{2I_4}{\beta_4}}. \tag{2.26}$$

Since the numbers of devices connected clockwise and counter-clockwise are equal, the threshold voltage can be dropped from eqn (2.26). Further, the common term $\beta_\square$ in the transconductance factors β_1 through β_4 can be eliminated. This leaves a current-mode expression describing the loop:

$$\sqrt{\frac{I_1}{W_1/L_1}} + \sqrt{\frac{I_3}{W_3/L_3}} = \sqrt{\frac{I_2}{W_2/L_2}} + \sqrt{\frac{I_4}{W_4/L_4}}. \tag{2.27}$$

Hence, VTL loops can be described by the sums of square-roots of the drain currents. The drain currents are weighted by the aspect ratios of the transistors.

Equation (2.27) demonstrates an interesting characteristic of SVTL circuits: the transfer function of an SVTL circuit is both temperature and process-independent.

Application

In the current domain, additions and subtractions are easily realised. Using these operations, linear combinations of the input and output currents can be forced through the MOS transistors comprising the VTL loop. In combination with the non-linear operation described by the general VTL loop equation (2.27), various linear and non-linear static transfer functions can be implemented.

2.3.2 Dynamic voltage-translinear principle

The conventional SVTL principle, described in Section 2.3.1, can only be used to implement static transfer functions. By admitting capacitors in the VTL loops, dynamic transfer functions can be realised. The term 'Dynamic Voltage-Translinear' is proposed to describe this new class of circuits.

Due to the quadratic behaviour of the MOS transistor in the strong inversion region, the voltages in a VTL circuit are related to the drain currents through square-root functions. This implies that instantaneous companding is an inherent characteristic. As a consequence, in general, a capacitor cannot be added to a VTL circuit without causing distortion.

Current mirror

The generation of distortion is illustrated with respect to the most simple VTL circuit. Figure 2.9 shows a current mirror where a capacitor C is added in parallel with the input transistor. The capacitor can be regarded as the internal integrator and the output transistor as the expander of a companding system, as shown in Fig. 2.2. The current mirror is biased in class A by a dc bias current $I_{\rm dc}$. The ac input current $I_{\rm in}$ is superposed on $I_{\rm dc}$.

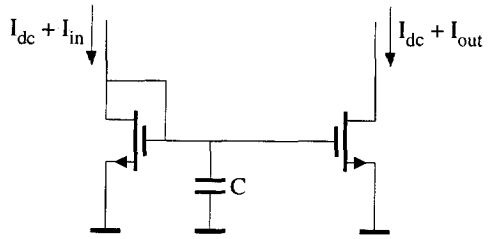

Figure 2.9: A capacitor added to a strong inversion MOS current mirror.

When the amplitude of $I_{\rm in}$ is small with respect to $I_{\rm dc}$, the transconductance g_m of the output transistor is approximately constant. Therefore, the relation between the capacitor voltage and the output current $I_{\rm out}$ is almost linear. The transfer function of the current mirror can be described by a linear DE:

$$\frac{C}{\sqrt{2\beta I_{\rm dc}}}\dot{I}_{\rm out} + I_{\rm out} = I_{\rm in}. \tag{2.28}$$

Equation (2.28) describes a first-order low-pass filter.

When the amplitude of $I_{\rm in}$ is close to the value of the bias current $I_{\rm dc}$, g_m cannot be approximated by a constant. Consequently, the transfer function of the current mirror has to be described by a non-linear DE:

$$\frac{C}{\sqrt{2\beta}}\dot{I}_{\rm out} + \sqrt{I_{\rm dc} + I_{\rm out}}I_{\rm out} = \sqrt{I_{\rm dc} + I_{\rm out}}I_{\rm in}. \tag{2.29}$$

Figure 2.10 shows the result of a large-signal harmonic balance simulation of the current mirror using a realistic transistor model from a 2 μm process. In the simulation, the amplitude of $I_{\rm in}$ is 90% of $I_{\rm dc}$, $I_{\rm dc}$ is 50 μA, $V_{\rm th}$ = 0.8 V and β = 50 μA/V^2. The plots of HD_2 and HD_3 show that the distortion is significant. In comparison with Fig. 2.6, the distortion generated in the bipolar transistor current mirror is much higher than for the MOS transistor current mirror. This is explained by the fact that the square function is far less non-linear than the exponential function.

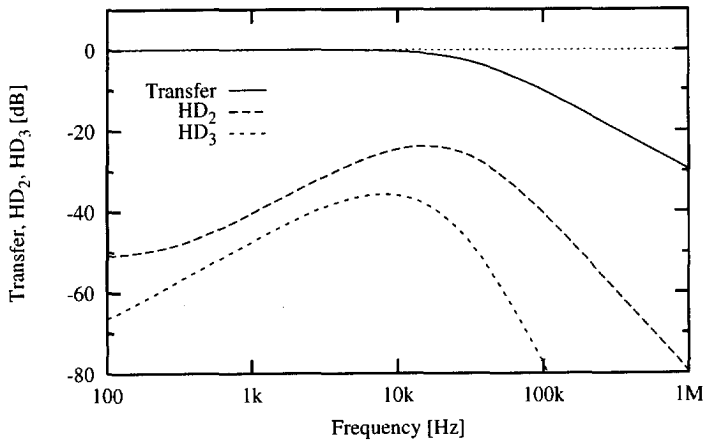

Figure 2.10: Large-signal simulation of the transfer function, HD_2 and HD_3 of the current mirror shown in Fig. 2.9.

Distortionless companding

The generation of distortion can be prevented by applying the general principle described in Section 2.1. For strong inversion MOS transistors, this results in the DVTL principle, which is described here with reference to the circuit structure shown in Fig. 2.11. The MOS transistor shown in this figure is described by the square law, eqn (2.25). The derivative with respect to time of the drain current is given by:

$$\dot{I}_{DS} = \beta \left(V_{GS} - V_{th}\right) \dot{V}_{GS}. \tag{2.30}$$

The excess gate-source voltage $(V_{GS} - V_{th})$ in this expression is quite inconvenient. It does not comply with the current-mode nature of VTL circuits. This factor can be replaced by a current-mode expression. Application of eqn (2.25) yields:

$$\dot{I}_{DS} = \sqrt{2\beta I_{DS}}\dot{V}_{GS}. \tag{2.31}$$

In Fig. 2.11, the voltage V_{GS} is applied across the capacitor C. Therefore, the constitutive law of the capacitance, eqn (2.18), describes the relation between the capacitance current I_{cap} and the derivative $\dot{V}_{GS}$. As a result, $\dot{V}_{GS}$ can be replaced by I_{cap} and a completely current-mode expression for $\dot{I}_{DS}$ is obtained:

$$\frac{C}{\sqrt{2\beta}}\dot{I}_{DS} = \sqrt{I_{DS}}I_{cap}. \tag{2.32}$$

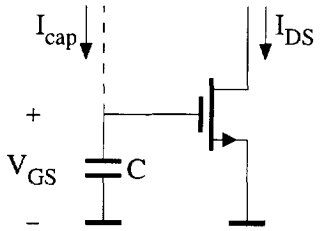

Figure 2.11: Principle of dynamic voltage-translinear circuits.

Equation (2.32) directly states the DVTL principle: "A time derivative of a current is equivalent to a multiplication of a current and the square root of a current." The current-mode algebraic expression on the RHS of eqn (2.32) can be realised by applying the SVTL principle.

A linear derivative is a basic function of any DE. Consequently, the DVTL principle can be used to implement both linear and non-linear DEs.

Equation (2.32) reveals yet another important characteristic of DVTL circuits. Since the RHS of eqn (2.32) is implemented by (part of) a VTL loop, the LHS is (part of) the DE describing the dynamic transfer function of the loop. This implies that the factor $C/\sqrt{2\beta}$ is part of the DE. Hence, the transfer function is process and temperature-dependent through $\beta_{\square}$.

In the above, the VTL principle was derived for the one-transistor structure shown in Fig. 2.11. It is shown in Section 7.4 that the principle can easily be generalised to structures of two or more transistors, in analogy with the generic output structures of tanh and sinh TL filters.

3

Analysis of translinear circuits

Although synthesis is more powerful than analysis, it must go together with a generally applicable analysis method in the same domain. This is a prerequisite for structured electronic design. This chapter therefore explores the possible analysis procedures that can be applied to investigate the behaviour of Static TransLinear (STL) and Dynamic TransLinear (DTL) circuits, before synthesis methodologies are surveyed in Chapter 4.

The analysis of STL circuits is reviewed in Section 3.1. The various methods for the analysis of DTL networks are treated next, in Section 3.2. Finally, Section 3.3 is devoted to the characteristics of the three different classes of TransLinear (TL) filters proposed in the literature, i.e., log-domain, tanh and sinh filters.

This chapter is concerned with the 'ideal' behaviour of TL circuits; ideal transistor models are assumed in all calculations. The analysis of second-order effects is deferred until Chapter 5. Throughout this chapter, the application of bipolar transistors is assumed. With some minor modifications, all theory presented is similarly applicable to TL circuits comprising alternative exponential devices.

3.1 Analysis of static translinear circuits

Two types of equations are involved in the analysis of the ideal behaviour of STL circuits. First, the TL loop equations describe the multiplicative relation between the collector currents of the transistors comprising the loops. Secondly, the KCLs (Kirchhoff's Current Law) express the relation between the transistor

currents and the independent current sources applied to the circuit. Owing to the current-mode nature of both the TL loop equations and the KCLs, a relatively simple analysis method results.

In the analysis of STL circuits, three successive steps have to be performed:

- Determine the fundamental translinear loops;
- Calculate the collector currents;
- Solve the system of loop equations.

Determine the fundamental translinear loops

The STL principle, explained in Section 2.2.1, uniquely defines the characteristics of a TL loop. Based on this definition, the transistors comprising the TL loops can be separated from the transistors serving other purposes, such as buffering of base currents.

A TL circuit may consist of more than one TL loop. In general, TL circuits are characterised by a set of L fundamental loops [50]. These loops can be translated directly into a set of L TL loop equations, applying the well-known expression [43, 50]:

$$\prod_i I_{C,Q_{2i}} = \lambda \prod_i I_{C,Q_{2i-1}}, \tag{3.1}$$

where λ is the emitter area scale factor of the loop, I_{C,Q_i} represents the collector currents of the transistors comprising the loop, and the products on the Left-Hand Side (LHS) and Right-Hand Side (RHS) are over the clockwise and counter-clockwise connected transistors, respectively.

In this context, simple current mirrors are not accounted for in the set of L fundamental loops. This is due to the fact that the TL loop formed by a current mirror is trivial as it contains no multiplications of collector currents. In other words, a current mirror can only realise a linear transfer function.

Different loops in a TL circuit can either be disjunct or coupled. Coupled loops can be coupled directly or indirectly. These three situations are illustrated in Fig. 3.1. Two TL loops are said to be *coupled directly* if they have one or more base-emitter junctions in common. Thus, the base-emitter junctions span a non-separable graph. Two loops are said to be *coupled indirectly* if they are part of the same non-separable graph, but have no base-emitter junctions in common. Two loops are called *disjunct* if they are part of two unconnected graphs.

If coupled loops exist in a circuit, more than L different TL loops can be identified. However, only L loops are fundamental. Note that the set of fundamental TL loops is not uniquely determined.

For the analysis of the circuit to succeed, it is important to find a complete set of fundamental TL loops, while excluding all loops that are not fundamental.

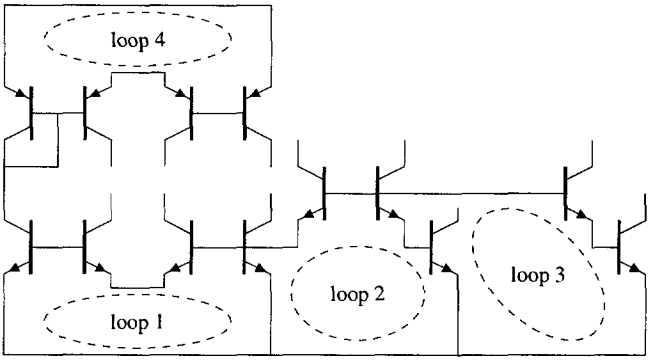

Figure 3.1: A circuit comprising four translinear loops. Loop 1 and 2 are coupled directly. Loop 1 and 3 are coupled indirectly. Loop 1 and 4 are disjunct.

For TL circuits where the base-emitter junctions span a non-separable planar graph, the number of fundamental loops is related to the number of base-emitter junctions B and the number of circuit nodes N by [50]:

$$L = B - N + 1. \tag{3.2}$$

In large circuits containing many coupled TL loops, eqn (3.2) can be used to confirm whether the complete set of fundamental loops has been found.

Calculate the collector currents

The TL loop equations (3.1), resulting from the first analysis step, describe the TL loops in terms of products of collector currents. The second analysis step comprises the calculation of the collector currents in terms of the input and output currents,[1] denoted both by I_j, where $j \in \mathbb{N}$. These calculations are based on the KCLs derived for each node of the circuit. Since the resulting system of KCL equations is linear, it is easy to solve, i.e., to obtain the collector currents in terms of the input and output currents. Often, the collector current expressions can even be obtained directly by inspection of the circuit schematic. In general, the collector currents are thus described by:

$$I_{\mathrm{C},Q_i} = \sum_j c_j I_j, \tag{3.3}$$

where c_j are constant coefficients.

An important distinction has to be made between single-loop and multiple-loop TL circuits. In a circuit comprising only one TL loop, all collector currents

[1] For simplicity, dc bias sources are considered as being input currents.

can be expressed as linear combinations of the input and output currents. In general, this is not true for multiple-loop circuits. If a multiple-loop circuit has Z linearly independent output currents, where $Z \leq L$, then a maximum of $L-Z$ currents are possibly non-linearly related both to the input currents and to the Z output currents. Consequently, if $Z < L$, it is not possible, based on the KCLs only, to express all collector currents as linear combinations of the input and output currents.

For example, consider a two-loop circuit with one input current I_{in} and one output current I_{out}, as shown in Fig. 3.2. The first loop generates a current I_{p}, which is applied to the second loop. Consequently, I_{p} acts as an intermediate 'input' and 'output' current. Without solving the TL loop equations, it is not possible to determine whether I_{p} is linearly or non-linearly related to I_{in} or I_{out}. Thus, I_{p} cannot be eliminated from the set of KCL equations.

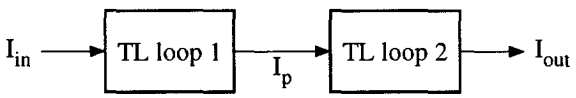

Figure 3.2: Generation of an intermediate current I_{p} in a two-loop translinear circuit.

As a result, in analysing TL circuits, it is convenient to appoint some of the collector currents, which cannot be expressed (*a priori*) as linear combinations in the input and output currents, as intermediate currents. All intermediate currents, denoted by I_{p_j}, where $j \in \mathbb{N}^+$, are chosen to be mutually independent. This way, all collector currents can be expressed as linear combinations of the input, output and the intermediate currents. The number of intermediate currents to be defined equals $L - Z$.

Note that, at this point, it is possible to check whether all fundamental TL loops have been obtained during the first analysis step. If more than $L - Z$ intermediate currents have to be defined to express all collector currents as linear combinations of the input, output and intermediate currents, it is likely that the set of fundamental TL loops is not yet complete.

Solve the system of loop equations

Substitution of the collector current expressions, obtained from the KCLs, in the TL loop equations, results in a system of polynomials in the input, output and intermediate currents. In general, the TL loop equations are thus described by:

$$\prod_i \sum_j c_{2i,j} I_j = \lambda \prod_i \sum_j c_{2i-1,j} I_j. \tag{3.4}$$

This set of equations can be solved for each of the unknowns. To solve the system for one of the output or intermediate currents, the other unknowns have to be eliminated. Finally, this will result in a single polynomial in the unknown current, denoted here by I_{out}. The various 'coefficients' of the polynomial in I_{out} are formed by the (known) input currents. In general, the polynomial can be of higher-order in I_{out}. Consequently, it might be necessary to resort to numerical methods to find the roots of the equation for I_{out}.

For an n^{th}-order polynomial in I_{out}, there are n roots. Not all of these roots represent physically meaningful solutions, resulting in negative or even complex collector currents [50]. Furthermore, not all of the physical solutions result in stable operation of the circuit. The stability of a solution for I_{out} can be investigated using small-signal or numerical analysis methods. Alternatively, the stability analysis method described in [50] can be applied. A similar method can be used to calculate the sensitivity of the roots to variations of the circuit parameters [50].

Example: Analysis of a squaring circuit

To illustrate the analysis procedure for TL circuits, consider the circuit shown in Fig. 3.3 [50], where I_{in} and I_{out} denote the input and output current of the circuit, respectively, and I_{o} is a dc bias current. The collector currents of Q_1–Q_5 are denoted by I_1 through I_5.

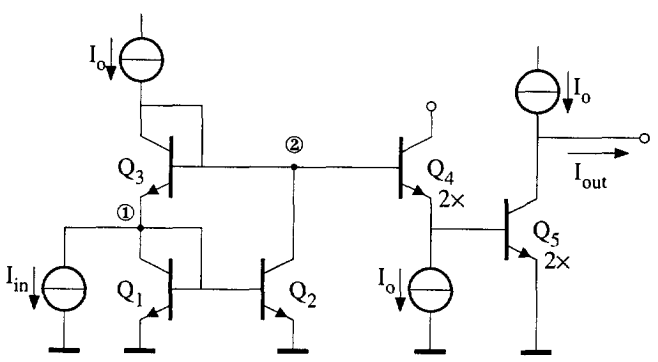

Figure 3.3: A squaring circuit [50].

The first step is to identify the set of fundamental TL loops. Excluding the current mirror Q_1-Q_2, a trivial TL loop, the circuit includes only one TL loop, Q_1-Q_3-Q_4-Q_5. The corresponding TL loop equation is given by:

$$I_1 \cdot I_3 = \tfrac{1}{2} I_4 \cdot \tfrac{1}{2} I_5. \tag{3.5}$$

The two factors $\frac{1}{2}$ in eqn (3.5) are due to the emitter area scaling of Q_4 and Q_5.

The second step is to derive the collector currents in terms of the input and output currents. Since the circuit embraces only one TL loop, no intermediate currents have to be defined. The expressions for the collector currents of Q_4 and Q_5 are evident from the circuit:

$$I_4 = I_o, \tag{3.6}$$

$$I_5 = I_o - I_{out}. \tag{3.7}$$

The collector currents of Q_1 and Q_3 can be calculated from the KCLs for nodes ① and ②, which are given by:

$$I_2 + I_3 = I_o, \tag{3.8}$$

$$I_3 - I_1 = I_{in}. \tag{3.9}$$

Since $I_1 = I_2$, this yields:

$$I_{2,3} = \tfrac{1}{2}\left(I_o \mp I_{in}\right). \tag{3.10}$$

Note that eqn (3.10) directly yields a condition for correct operation of the circuit. Only when $|I_{in}| < I_o$, are all the collector currents strictly positive, and the TL circuit operates correctly.

Substitution of eqns (3.6), (3.7) and (3.10) in (3.5) yields the TL loop equation in terms of I_{in}, I_o and I_{out}:

$$\tfrac{1}{2}\left(I_o - I_{in}\right) \cdot \tfrac{1}{2}\left(I_o + I_{in}\right) = \tfrac{1}{2} I_o \cdot \tfrac{1}{2}\left(I_o - I_{out}\right). \tag{3.11}$$

Equation (3.11) is a first-order polynomial in I_{out}. Solving it for I_{out} yields:

$$I_{out} = \frac{I_{in}^2}{I_o}. \tag{3.12}$$

As a final result, eqn (3.12) reveals that the circuit shown in Fig. 3.3 implements the squaring function, for $|I_{in}| < I_o$.

Example: Analysis of a frequency-doubling circuit

As a more complicated example, consider the circuit depicted in Fig. 3.4 [60], comprising two coupled TL loops: Q_1-Q_2-Q_3-Q_4 and Q_4-Q_5-Q_6-Q_7. The two loops have one base-emitter junction, of transistor Q_4, in common. Transistors Q_8 and Q_9 are not part of the TL core of the circuit; they merely serve as buffers for the base currents of Q_2-Q_3 and Q_5-Q_6, respectively. The TL core of the circuit comprises seven junctions and six nodes. The collector currents of Q_1–Q_7 are denoted by I_1 through I_7. According to eqn (3.2), the circuit contains two fundamental TL loops. Consequently, the third loop, formed by Q_1-Q_2-Q_3-Q_5-Q_6-Q_7, is not a fundamental one.

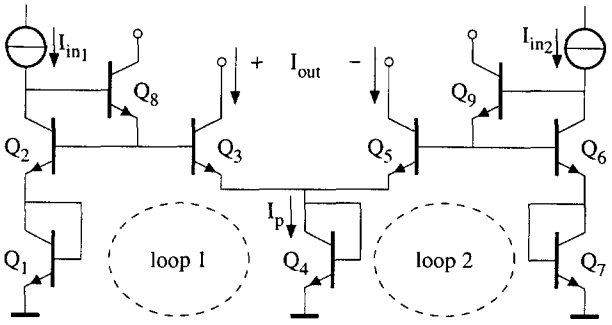

Figure 3.4: A frequency-doubling circuit [60].

The circuit has two input currents, I_{in_1} and I_{in_2}, and one output current I_{out}, which equals the difference of the collector currents I_3 and I_5. The collector currents of Q_1, Q_2, Q_6 and Q_7 are readily expressed in terms of the input currents:

$$I_1 = I_2 = I_{\text{in}_1}, \qquad I_6 = I_7 = I_{\text{in}_2}. \tag{3.13}$$

However, I_3, I_4 and I_5 cannot be expressed as linear combinations of I_{in_1}, I_{in_2} and I_{out}. Therefore, one intermediate current I_{p} is introduced. If, by definition, I_4 equals I_{p}, I_3 and I_5 can now be written as linear combinations of I_{out} and I_{p}:

$$I_{3,5} = \tfrac{1}{2}\left(I_{\text{p}} \pm I_{\text{out}}\right). \tag{3.14}$$

Using eqns (3.13), (3.14), and $I_4 = I_{\text{p}}$, the two loop equations can be described by:

$$I_{\text{in}_1}^2 = \tfrac{1}{2}\left(I_{\text{p}} + I_{\text{out}}\right) I_{\text{p}}, \tag{3.15a}$$
$$I_{\text{in}_2}^2 = \tfrac{1}{2}\left(I_{\text{p}} - I_{\text{out}}\right) I_{\text{p}}. \tag{3.15b}$$

Both polynomials are first-order in I_{out} and second-order in I_{p}.

To solve eqns (3.15a) and (3.15b) for I_{out}, I_{p} has to be eliminated. Expressions for I_{p}^2 and I_{p} are obtained, respectively, by addition and subtraction of eqns (3.15a) and (3.15b). This yields:

$$I_{\text{p}}^2 = I_{\text{in}_1}^2 + I_{\text{in}_2}^2, \tag{3.16a}$$
$$I_{\text{p}} I_{\text{out}} = I_{\text{in}_1}^2 - I_{\text{in}_2}^2. \tag{3.16b}$$

Now, I_{p} can be eliminated by subtraction of eqn (3.16a) multiplied by I_{out}^2 from the square of (3.16b). The resulting polynomial has a degree of four:

$$I_{\text{out}}^2\left(I_{\text{in}_1}^2 + I_{\text{in}_2}^2\right) = \left(I_{\text{in}_1}^2 - I_{\text{in}_2}^2\right)^2. \tag{3.17}$$

Equation (3.17) is second-order with respect to I_{out}. Hence, the two roots are readily found. Only one of these two roots is physically meaningful; the other results in negative collector currents. The correct solution is given by:

$$I_{\text{out}} = \frac{I_{\text{in}_1}^2 - I_{\text{in}_2}^2}{\sqrt{I_{\text{in}_1}^2 + I_{\text{in}_2}^2}}. \tag{3.18}$$

If $I_{\text{in}_1} = I_{\text{m}}|\cos\omega t|$ and $I_{\text{in}_2} = I_{\text{m}}|\sin\omega t|$, the output current equals $I_{\text{out}} = I_{\text{m}}\cos 2\omega t$. Thus, the circuit shown in Fig. 3.4 implements an amplitude-conserving frequency doubling [60].

This circuit is probably the best example to demonstrate the high functional density that can be obtained using TL techniques. With only seven transistors, a complicated function (3.18) involving squaring, addition, subtraction, square rooting and division is realised.

3.2 Analysis of dynamic translinear circuits

Most publications on DTL circuits have emphasised the synthesis rather than the analysis of these circuits. Nonetheless, a number of different analysis methods have been proposed. Static translinear circuits have always been analysed in terms of currents, as described in Section 3.1. In Section 3.2.1, this method is generalised to facilitate the investigation of DTL circuits [13, 16, 88]. The resulting current-mode analysis method yields the global transfer function, i.e., the Differential Equation (DE) describing the circuit being examined.

A variant of the global analysis method is described in Section 3.2.2 [17,18]. It is shown that a state-space approach can significantly simplify the analysis of higher-order TL filter circuits.

The operation of electronic circuits is always an interplay of voltages and currents. Consequently, instead of a description in terms of currents, a voltage-mode approach to the analysis of DTL circuits can be followed [1]. The global and state-space variants of this method are reviewed in Section 3.2.3, along with two other analysis procedures: small-signal analysis and analysis based on Bernoulli's DE [14].

3.2.1 Global current-mode analysis

In developing a general analysis method for DTL networks, it is necessary to get a clear picture of the difference between STL and DTL circuits. In other words: why is it not possible to apply the analysis method developed for STL networks to the analysis of DTL networks? The answer to this question lies in the system of equations describing the circuit in question.

Together, the TL loop equations and the KCLs, obtained from the first two analysis steps, comprise a complete set of equations necessary to unravel the circuit behaviour. Now, the difference between STL and DTL circuits emerges when writing down the KCL equations. In dynamic networks, the KCLs are linear equations not only in the collector currents, input currents and output currents, but also in the *capacitance currents*. In this context, a capacitance current can be viewed as a special kind of 'bias current', which is derived from the input, intermediate and/or output currents. This capacitive 'current source' can be single-ended or floating.

During analysis, the capacitance currents are unknown, and therefore the system of equations cannot be solved unless additional expressions can be found for these capacitance currents. This is exactly the problem to be solved in order to obtain a general analysis method for DTL networks. In order to eliminate an unknown variable from a system of equations it is, in general, necessary to have at least two independent expressions in the unknown variable. A first expression for the capacitance currents is found from the KCLs. An independent second expression has to be found from a third type of equations, next to the TL loop equations and KCLs. Accordingly, the analysis method for STL networks has to be supplemented with one extra step to facilitate the analysis of DTL circuits. The analysis method for DTL circuits thus becomes:

- Determine the fundamental translinear loops;
- Calculate the collector currents;
- Obtain expressions for the capacitance currents;
- Solve the system of equations.

The first two and the last step are treated in Section 3.1. Consequently, this section only deals with the procedure to obtain expressions for the capacitance currents.

Analysis of a first-order log-domain filter

For the first-order log-domain filter shown in Fig. 3.5 [1], the first TL filter ever published, an expression for the capacitance current I_{cap} is readily obtained. The situation of the capacitor C is very similar to the sub-circuit shown in Fig. 2.7. Diode D_3 is biased by a dc current I_0 and therefore complies with a constant voltage source. The output current flows through diode D_4, which is an exponential device, exactly like the bipolar transistor shown in Fig. 2.7. Accordingly, I_{cap} satisfies eqn (2.20). This yields:

$$I_{\text{cap}} = CU_T \frac{\dot{I}_{\text{out}}}{I_{\text{dc}} + I_{\text{out}}}, \tag{3.19}$$

where the dot denotes differentiation with respect to time.

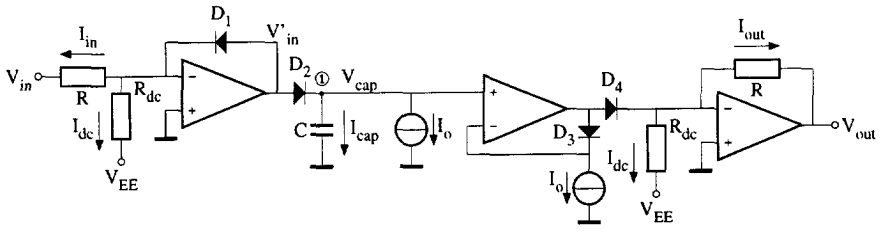

Figure 3.5: A log-domain first-order low-pass filter [1].

Together, the four diodes, D_1–D_4, constitute a TL loop. The op amps are merely used for V-I and I-V conversion at the input and output, by means of the resistor R, and to force the appropriate currents through each of the diodes. The resistors R_{dc} are simple current source implementations adding a dc current I_{dc} to the input current I_{in} and the output current I_{out}.

For the circuit shown in Fig. 3.5, the capacitance current appears in the KCL applied to node ①. The current through D_2 equals $(I_{\mathrm{o}} + I_{\mathrm{cap}})$. The other diode currents are obvious. Hence, the TL loop equation is given by:

$$(I_{\mathrm{dc}} + I_{\mathrm{in}})\, I_{\mathrm{o}} = (I_{\mathrm{o}} + I_{\mathrm{cap}})\, (I_{\mathrm{dc}} + I_{\mathrm{out}})\,. \tag{3.20}$$

In order to solve eqn (3.20) for the output current, I_{cap} has to be eliminated using (3.19). In addition, the additive term $I_{\mathrm{o}} I_{\mathrm{dc}}$, common to both sides of eqn (3.20), can be deleted. Finally, this yields the linear DE describing the linear dynamic transfer function of the circuit:

$$C U_T \dot{I}_{\mathrm{out}} + I_{\mathrm{o}} I_{\mathrm{out}} = I_{\mathrm{o}} I_{\mathrm{in}}. \tag{3.21}$$

A general expression for the capacitance current

The foregoing example of the analysis of Adams' filter has demonstrated that TL filters, or at least log-domain filters, can be analysed in a TL fashion. The current-mode expression (3.19) for the capacitance current proves to be the key to TL analysis of DTL networks. To generalise this method of analysis to arbitrary n^{th}-order DTL circuits, a general method is required to provide expressions for the currents flowing through all the capacitors in a DTL circuit. Another way of putting this is that eqn (3.19) has to be generalised.

In a TL filter, each capacitor C_k, where $k \in [1, \ldots, n]$, is always connected in series with a certain number of base-emitter junctions. This is illustrated in Fig. 3.6. Most often, these junctions are part of a TL loop, in which case the capacitance is connected between two circuit nodes of that loop. Though any TL loop comprises an even number of junctions, the number of junctions in series with the capacitor may be odd or even. Moreover, the junctions in

this loop may be connected in the same direction, in opposite directions or in a combination of the two. Thus, the loop shown in Fig. 3.6 does not have any of the characteristics of a TL loop.

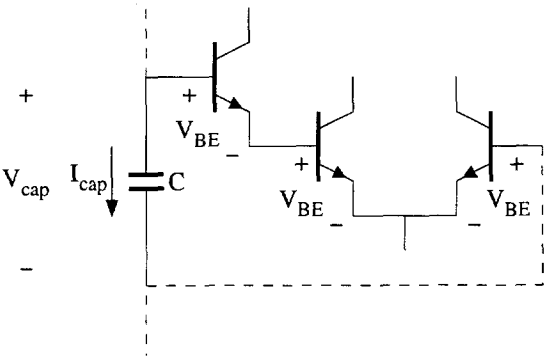

Figure 3.6: A capacitance in (a part of) a translinear loop.

As the capacitance and the junctions together comprise a loop, the capacitance voltage V_{C_k} can be expressed in terms of the junction voltages, using the KVL:

$$V_{C_k} = \sum_i \pm V_{\mathrm{BE},Q_i}, \tag{3.22}$$

$$= U_T \sum_i \pm \ln\left(\frac{I_{\mathrm{C},Q_i}}{\lambda_i I_\mathrm{s}}\right), \tag{3.23}$$

where I_{C,Q_i} are the collector currents corresponding to the base-emitter voltages V_{BE,Q_i} and λ_i are the relative emitter area ratios. The sign of each voltage V_{BE,Q_i} in eqn (3.23) is dependent on the orientation of the base-emitter junction in the loop.

The current I_{C_k} through the capacitance is equal to the derivative $\dot{V}_{C_k}$ multiplied by the value C_k of the capacitance. Differentiating eqn (3.23) and multiplying it by C_k thus yields the capacitance current:

$$I_{C_k} = C_k U_T \sum_i \pm \frac{\dot{I}_{\mathrm{C},Q_i}}{I_{\mathrm{C},Q_i}}. \tag{3.24}$$

Equation (3.24) is the basis of the general analysis method for DTL circuits! Note that λ_i and I_s have no influence whatsoever on the capacitance currents.

Equation (3.24) gives an expression for each of the capacitance currents that is independent from the TL loop equations and KCLs comprising the rest of the system of equations. With the aid of these additional equations, the system can be solved, i.e., the transfer function of the circuit can be obtained.

Like the TL loop equations and the KCLs, the expressions resulting from eqn (3.24) are *current-mode.* Hence, a DTL circuit can be described by a system of equations completely in terms of currents.

Each capacitor comprises at least two loops with the junctions in a TL circuit. Therefore, more than one expression for a capacitance current can always be derived. With respect to the other equations necessary to describe the circuit, these capacitance current expressions are dependent. Consequently, eqn (3.24) has to be applied to each capacitance just once. The other possible capacitance current expressions are superfluous. The most intelligent choice is to apply eqn (3.24) to the loop in which none of the collector currents contains the capacitance current under consideration. This prevents the capacitance current, and its derivative, from appearing at the RHS of eqn (3.24), which would complicate the elaboration of the system of TL loop equations.

It is interesting to note that dc collector currents flowing through some of the transistors in a capacitance–junction(s) loop are automatically eliminated from eqn (3.24), since the derivative of a constant equals zero.

To demonstrate the application of the proposed analysis method, two TL filters are analysed. The first example describes the analysis of a second-order log-domain filter. Then, a first-order filter is used to explain the impact of different choices for the capacitance-junction(s) loops, which have to be made in order to apply eqn (3.24). Later on, the analyses of a tanh and a sinh filter are described in Sections 3.3.2 and 3.3.3, respectively.

Example: Analysis of a second-order low-pass filter

As an illustration of the proposed analysis method, a second-order low-pass filter, see Fig. 3.7 [3], is analysed. All transistors comprising the TL loops are compound transistors, but for analysis purposes they can simply be treated as single transistors, as explained in Section 4.5.2, changing U_T in eqn (2.10) into $2U_T$.

The filter consists of two coupled TL loops. The first loop comprises transistors Q_1-Q_2-Q_3-Q_4-Q_7-Q_8. The second loop comprises Q_3–Q_6. A TL loop equation can be derived for both loops.

Solving the system of KCLs for the collector currents, it follows that I_2 and I_5, the collector currents of Q_2 and Q_5, cannot be expressed as linear functions of the input current I_{in}, the output current I_{out}, the dc bias current I_{o}, and the capacitance currents I_{C_1} and I_{C_2}. Therefore, an intermediate current I_{p} is introduced, which is chosen equal to I_2. Now, direct substitution of the KCLs in the TL loop equations yields:

$$I_{\text{o}}^2 I_{\text{in}} = I_{\text{p}} \left(I_{C_1} + I_{\text{o}}\right) I_{\text{out}}, \tag{3.25a}$$

$$2I_{\text{o}}^2 = \left(I_{C_1} + I_{\text{o}}\right) \left(I_{\text{p}} + I_{\text{o}} - I_{C_2}\right), \tag{3.25b}$$

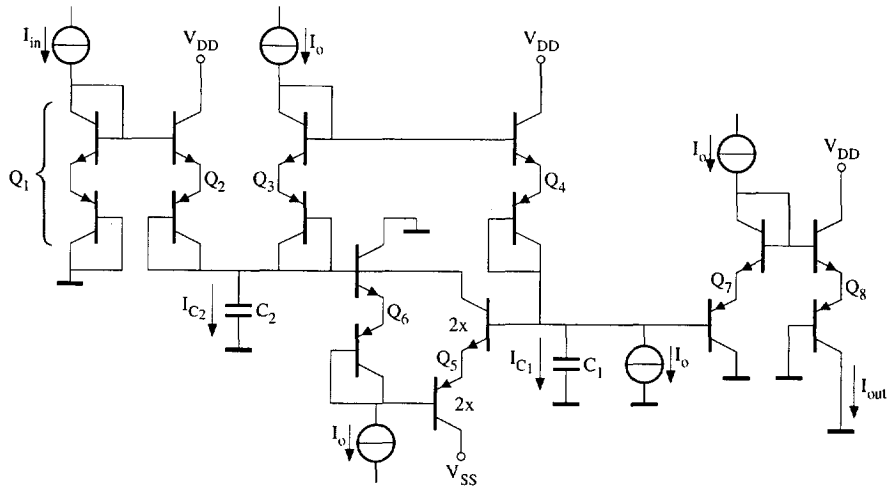

Figure 3.7: A second-order low-pass filter [3].

where the factor 2 in eqn (3.25b) is a consequence of the emitter area scaling of Q_5.

Next, two expressions for I_{C_1} and I_{C_2} are derived. In order to apply eqn (3.24), two loops have to be chosen. For I_{C_1} the loop C_1-Q_7-Q_8 is used, as the collector currents of Q_7 and Q_8 do not contain I_{C_1}. Likewise, for I_{C_2} the loop C_2-Q_3-Q_4-Q_7-Q_8 is used, since the corresponding collector currents do not contain I_{C_2}. This particular choice for the two capacitance-junctions loops leads to relatively simple expressions for I_{C_1} and I_{C_2}. Other choices result in the appearance of the derivatives $\dot{I}_{C_1}$ and/or $\dot{I}_{C_2}$ in the equations for I_{C_1} and I_{C_2}. The capacitance currents are therefore expressed by:

$$I_{C_1} = 2C_1 U_T \frac{\dot{I}_{\text{out}}}{I_{\text{out}}}, \tag{3.26a}$$

$$I_{C_2} = 2C_2 U_T \left(\frac{\dot{I}_{C_1}}{I_o + I_{C_1}} + \frac{\dot{I}_{\text{out}}}{I_{\text{out}}} \right), \tag{3.26b}$$

where the factor two in both equations is a consequence of the use of compound transistors.

The collector currents I_3 and I_7, of Q_3 and Q_7, are equal to the constant bias current I_o. Since the derivative of a constant is zero, I_3 and I_7 do not appear in the equations for I_{C_1} and I_{C_2}. The base-emitter junctions of Q_3 and Q_7 can in this context be regarded as dc voltage sources.

Now, the system of eqns (3.25)–(3.26) has to be solved to obtain the transfer function of the filter. To begin with, the intermediate current I_p is eliminated

from eqns (3.25a) and (3.25b), which are both linear in I_p. This yields:

$$I_{out}\left[I_{C_1}\left(I_{C_2}-I_o\right)+I_o\left(I_{C_2}+I_o\right)\right]=I_o^2 I_{in}. \tag{3.27}$$

Next, eqn (3.26a) and its derivative can be used to eliminate I_{C_1} and $\dot{I}_{C_1}$ from eqn (3.26b). The capacitance current I_{C_2} is now described in terms of the first-order and second-order derivatives of the output current:

$$I_{C_2}=2C_2U_T\frac{2C_1U_T\ddot{I}_{out}+I_o\dot{I}_{out}}{2C_1U_T\dot{I}_{out}+I_oI_{out}}. \tag{3.28}$$

Finally, substitution of eqns (3.26a) for I_{C_1} and (3.28) for I_{C_2} in (3.27) results in a linear DE, expressing the linear transfer function from the input to the output:

$$4C_1C_2U_T^2\ddot{I}_{out}+2\left(C_2-C_1\right)U_TI_o\dot{I}_{out}+I_o^2I_{out}=I_o^2I_{in}. \tag{3.29}$$

Equivalently, the Laplace-domain transfer function $H(s)$ is given by:

$$H(s)=\frac{I_o^2}{4s^2C_1C_2U_T^2+2s\left(C_2-C_1\right)U_TI_o+I_o^2}. \tag{3.30}$$

Clearly, the terms C_1U_T and C_2U_T are part of the transfer function, as explained in Section 2.2.2.

The cut-off frequency ω_c of this low-pass filter function equals:

$$\omega_c=\frac{I_o}{\sqrt{C_1C_2}U_T}. \tag{3.31}$$

Equation (3.31) shows that ω_c can be controlled linearly through I_o. This is a general characteristic of TL filters. The quality factor Q of the filter is determined by the factor (C_2-C_1) appearing in eqn (3.30). In [5], a modification of this filter is described in which the Q-factor is electronically tunable as well.

Example: Analysis of a translinear integrator

A capacitor C connected to the circuit nodes of a TL loop will always form at least two different loops with the base-emitter junctions comprising the TL loop. For example, in the TL integrator shown in Fig. 3.8 [2], two capacitance-junction(s) loops can be identified. These are C-Q_1-Q_2-Q_3 and C-Q_4. Hence, two different expressions can be derived for the capacitance current I_{cap}. A choice has to be made between the two of them, since only one expression is necessary to analyse the transfer function of the integrator. The most convenient choice is to use the loop C-Q_4, since the collector current I_{out} of Q_4 does not

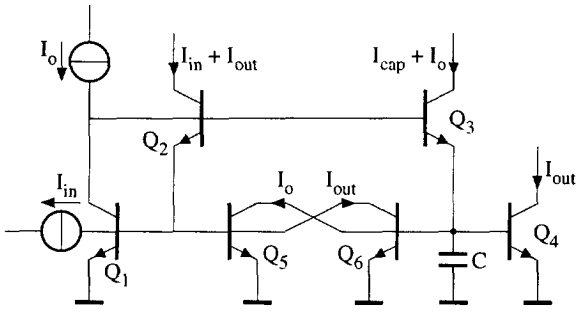

Figure 3.8: A translinear integrator [2].

contain I_{cap}. However, for illustrative purposes, the expression for I_{cap} resulting from the loop C-Q_1-Q_2-Q_3 is used here to analyse the circuit.

Application of eqn (3.24) to the loop C-Q_1-Q_2-Q_3 yields:

$$I_{\text{cap}} = CU_T \left(\frac{\dot{I}_{\text{in}} + \dot{I}_{\text{out}}}{I_{\text{in}} + I_{\text{out}}} - \frac{\dot{I}_{\text{cap}}}{I_{\text{o}} + I_{\text{cap}}} \right). \tag{3.32}$$

Due to the presence of I_{cap} in the collector current of Q_3, I_{cap} is now expressed as a function of I_{cap} itself and its derivative $\dot{I}_{\text{cap}}$.

Instead of using the expression for I_{cap} in the TL loop equation, the approach now must be to substitute the TL loop equation in eqn (3.32). The TL loop equation is given by:

$$I_{\text{o}} \left(I_{\text{in}} + I_{\text{out}} \right) = \left(I_{\text{o}} + I_{\text{cap}} \right) I_{\text{out}}. \tag{3.33}$$

Equation (3.33) yields an expression for I_{cap} and, after differentiation with respect to time, also for $\dot{I}_{\text{cap}}$:

$$I_{\text{cap}} = \frac{I_{\text{o}} I_{\text{in}}}{I_{\text{out}}}, \tag{3.34}$$

$$\dot{I}_{\text{cap}} = I_{\text{o}} \frac{\dot{I}_{\text{in}} I_{\text{out}} - I_{\text{in}} \dot{I}_{\text{out}}}{I_{\text{out}}^2}. \tag{3.35}$$

Substitution of eqns (3.34) and (3.35) in (3.33) finally results in the transfer function of the integrator:

$$CU_T \dot{I}_{\text{out}} = I_{\text{o}} I_{\text{in}}. \tag{3.36}$$

From the foregoing example it can be concluded that, in principle, a different choice for the capacitance-junction(s) loop does not hamper the correct analysis of a DTL circuit. However, the total number of calculations to be

made increases, as derivatives are generated during the analysis in intermediate expressions that are eliminated later on; $\dot{I}_{\text{in}}$ and $\dot{I}_{\text{cap}}$ in this example. It goes without saying that for large DTL circuits the intermediate expression swell, a well-known mathematical phenomenon, due to 'wrong' choices of the capacitance-junction(s) loops can be impressive and will certainly diminish the insight into the behaviour of the circuit.

3.2.2 State-space current-mode analysis

The global analysis method for DTL circuits, presented in Section 3.2.1, is believed to be generally applicable, which makes it a powerful tool for analysis and design purposes. Notwithstanding this major advantage, for large and high-order DTL circuits, the procedure suffers from intermediate expression swell, which can make the global analysis of TL filters a cumbersome occupation. The complexity of the intermediate expressions encountered during the global analysis of TL filters vanishes only in the final stage of the calculations when the ultimate solution, a linear n^{th}-order DE, is obtained.

The intermediate expression swell is mainly associated with the equations for the capacitance currents. In an n^{th}-order TL filter, n successive differentiations have to be performed to express each of the n capacitance currents in terms of the (derivatives of the) input and output current. The resulting expressions tend to become very complex, due to the non-linear dynamic relation between the capacitance currents and the input and output currents. For example, eqn (3.28) is already more complex than (3.26a). Note that this difficulty does not arise in conventional filters, since only linear components are employed.

State-space techniques have proven very effective in the area of conventional filters, as they break down a higher-order DE into a system of first-order DEs. With respect to TL filters, state-space, or equivalently, signal flow graph methods, can be applied beneficially as well. In fact, most synthesis methods for TL filters published to date depend fully on these techniques [8, 10, 14, 89].

This section serves to demonstrate that the state-space approach forms an adequate means to the analysis of large TL filters. More precisely, since the analysis result is a state-space description in which only first-order derivatives are involved, the expressions for the n capacitance currents remain very simple, thus preventing excessive intermediate expression swell.

Filter structure

In theory, every DE can be described by an infinite number of different state-space descriptions. However, in order to transfer the (low) parameter-sensitivity of a particular state-space description to the circuit realisation, most synthesis methods for (both TL and conventional) filters constitute a one-to-one relation

between the state-space description and the corresponding circuit implementation. Applying a state-space approach thus leads to the additional benefit that the analysis also reveals information about the state-space description, or linear filter structure, used to synthesise the filter.

Choice of the states

In order to find a state-space description of a filter, it is necessary to choose some state variables. For conventional filters containing capacitors and inductors, it is customary to choose the capacitance voltages and inductance currents to represent the memory of the circuit.

For TL filters, the choice of the state variables is of crucial importance. Capacitances are used exclusively as the memory elements in these networks. Nevertheless, using the capacitance voltages to obtain a state-space description is not the most suitable choice. Voltages do not comply with the current-mode nature of TL circuits. Due to the instantaneous companding inherent to TL circuits, the voltages are logarithmically related to the currents. Current being the principal carrier of information, an analysis in terms of voltages will inevitably result in complicated transcendental equations, impeding a thorough understanding of the circuit's operation.

Not surprisingly, the application of an exponential-like transformation to each of the capacitance voltages restores the linear relation between the states and the information being processed. This is illustrated in Fig. 3.9. It goes without saying that the 'exponential transconductance' should not influence the capacitance voltage. Hence, it must have a negligible input current.

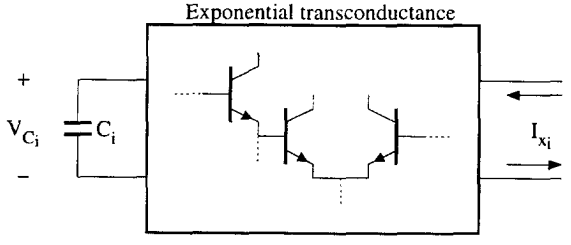

Figure 3.9: An exponential transformation of the capacitance voltages restores the linear state-space.

Now, the key is to use additional (fictitious) transistors to implement the transformations. The resulting transistor *currents*, denoted by I_{x_l}, where $l \in [1, \ldots, n]$, form the basis of subsequent state-space analysis. Except for a multiplicative constant, the state currents are uniquely related to the capacitance voltages. The supplementary circuitry can be applied in such a way as to satisfy

the STL principle, i.e., all extra loops thus introduced are TL loops. Under this condition, the TL analysis techniques described in Sections 3.1 and 3.2.1 can be applied to obtain a state-space description of a TL filter.

Implementation of the exponential transformations

The nature of the non-linear relation between the capacitance voltages and the transistor currents depends on the type of TL filter begin analysed. To date, three different classes of TL filters have been proposed in the literature [10]: log-domain, tanh and sinh filters. Different transformations (exp, tanh and sinh, respectively) have to be applied for each of these filter types to obtain a set of linear state variables I_{x_l}. Consequently, the additional circuitry required to facilitate TL analysis has to be tailored to the specific filter class.

Information about the exponential transconductance to be applied can be deduced from the output section of a TL filter. As the output current can be considered as being one of the state variables, the sub-circuit used to generate the output current from a corresponding capacitance voltage reveals the nature of the output expansion function. On condition that all first-order DEs comprising the total state-space description have been implemented by the same class of DTL circuitry, similar transconductance networks can be used to expand each capacitance voltage. The output expansion circuits of log-domain, tanh and sinh filters are shown in Figs 3.14, 3.19 and 3.23, respectively. Whereas the output stage of a log-domain filter comprises a single transistor in common-emitter configuration, tanh filters are characterised by a differential-pair output stage, and sinh filters by a second-order TL loop implementing the geometric mean function. Note that each of these output stages has an ideally infinite input impedance and therefore does not disturb the capacitance voltage being sensed.

If a DTL filter comprises a mixture of log-domain, tanh and sinh techniques, the foregoing procedure will fail. The remaining alternative is to apply the global analysis method described in Section 3.2.1.

By applying additional (fictitious) circuitry to the filter under inspection, new TL loops are created as the capacitances are connected between the nodes of existing TL loops. In order for the STL and DTL analysis methods to be applicable, these extra loops have to be TL loops. That is, the numbers of clockwise and counter-clockwise oriented devices have to be equal. Hence, level shifts, implemented by dc biased diodes are often required in addition to the output stages shown in Figs 3.14, 3.19 and 3.23. The dc bias currents and relative emitter areas of the level shifts are unimportant. They are simply translated into multiplicative constants.

Further, the STL principle dictates the devices to be used in the additional circuitry, as the exponential slope factors of all devices in a TL loop have to be identical. For example, for a TL filter comprising compound transistors, the exponential transconductances have to be implemented by compound transistors

as well. Again, for a TL loop containing different devices, i.e., NPN and PNP transistors, the numbers of clockwise and counter-clockwise oriented devices have to be equal for both types of devices individually.

Translinear analysis of the state-space filter circuit

Having augmented the TL filter by additional output expansion stages, a state-space analysis can now be performed. Basically, the method described in Section 3.2.1 has to be applied.

Due to the additional circuitry, the set of fundamental TL loops has increased with respect to the original filter circuit. The number of extra fundamental TL loop equations equals the number of additional expansion stages applied.

The expansion of the set of fundamental loop equations is counterbalanced by a commensurate increase of intermediate currents, being the state variable currents I_{x_l}. Applying the KCL equations, the collector currents can be expressed as linear combinations of the input currents, the output current, the capacitance currents I_{C_k} and the intermediate currents, I_{p_j} plus I_{x_l}. These expressions are substituted into the TL loop equations to obtain a set of current-mode polynomials.

Now, the procedure to be followed is to solve the system of loop equations for each of the capacitance currents I_{C_k}. Elimination of the intermediate currents I_{p_j} and all the capacitance currents but one, yields expressions for I_{C_k} in terms of the input currents and the state variables I_{x_l}.

The main improvement of the state-space analysis method is the simplicity of the expressions for the capacitance currents. Equation (3.24) is applied to the loop formed by C_k and the transistors Q_i comprising the transconductance expansion stage. In most TL filter circuits, the currents I_{C,Q_i} are all related to only one state variable, I_{x_k}, and possibly some dc bias currents. This results in an elegantly simple equation for $I_{C_k} = I_{C_k}(I_{x_k}, \dot{I}_{x_k})$, containing only the first-order derivative of I_{x_k}.

Substitution of $I_{C_k}(I_{x_k}, \dot{I}_{x_k})$ into the polynomial expressions for I_{C_k} obtained from the set of TL loop equations ultimately results in a linear state-space description of the filter.

To illustrate the state-space analysis method, a fifth-order low-pass filter is analysed next.

Example: State-space analysis of a fifth-order low-pass filter

Figure 3.10 shows a log-domain fifth-order Chebyshev low-pass filter designed by Perry and Roberts [89]. This circuit is used here to demonstrate both the intermediate expression swell of the global analysis method, described in Section 3.2.1, and the application of the state-space analysis method.

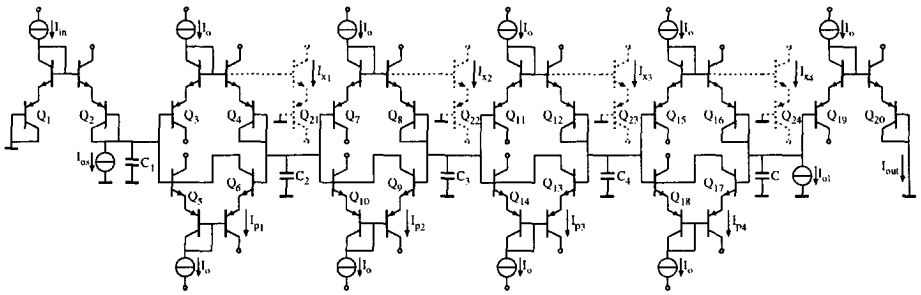

Figure 3.10: State-space analysis of a fifth-order low-pass filter [89], with the aid of some additional transistors (the dotted components).

Global analysis — Intermediate expression swell The TL filter comprises five fundamental TL loops of compound transistors, Q_1 through Q_{20}. For the moment we disregard the dotted transistors Q_{21}–Q_{24}. A possible set of fundamental TL loop equations is given by the four second-order loops Q_3–Q_6, Q_7–Q_{10}, Q_{11}–Q_{14}, and Q_{15}–Q_{18}, which are coupled by a sixth-order loop Q_1-Q_2-Q_6-Q_5-Q_{10}-Q_9-Q_{14}-Q_{13}-Q_{18}-Q_{17}-Q_{19}-Q_{20}.

To express the resulting TL loop equations in terms of the input, output and intermediate currents, by direct substitution of the KCLs, four intermediate currents I_{p_j}, $j \in [1, \ldots, 4]$, have to be introduced, as indicated in Fig. 3.10. The five fundamental TL loop equations are thus given by:

$$I_{\mathrm{o}}^2 = I_{\mathrm{p}_j}\left(I_{\mathrm{p}_{j+1}} + I_{C_{j+1}}\right), \qquad j \in [1, \ldots, 3], \tag{3.37a}$$

$$I_{\mathrm{o}}^2 = I_{\mathrm{p}_4}\left(I_{\mathrm{ol}} + I_{C_5}\right), \tag{3.37b}$$

$$I_{\mathrm{in}} I_{\mathrm{p}_1} I_{\mathrm{p}_2} I_{\mathrm{p}_3} I_{\mathrm{p}_4} I_{\mathrm{o}} = \left(I_{\mathrm{os}} + I_{\mathrm{p}_1} + I_{C_1}\right) I_{\mathrm{o}}^4 I_{\mathrm{out}}, \tag{3.37c}$$

where I_{in} is the input current, I_{out} the output current, I_{o}, I_{os} and I_{ol} are dc bias currents, and I_{C_k}, $k \in [1, \ldots, 5]$, denotes the current flowing through each of the five grounded capacitances C_k.

The third step of the global analysis method, described in Section 3.2.1, is to obtain current-mode expressions for the capacitance currents. Application of eqn (3.24) yields:

$$I_{C_5} = 2C_5 U_T \frac{\dot{I}_{\mathrm{out}}}{I_{\mathrm{out}}}, \tag{3.38a}$$

$$I_{C_4} = 2C_4 U_T \left(\frac{\dot{I}_{\mathrm{out}}}{I_{\mathrm{out}}} - \frac{\dot{I}_{\mathrm{p}_4}}{I_{\mathrm{p}_4}}\right), \tag{3.38b}$$

$$I_{C_3} = 2C_3U_T\left(\frac{\dot{I}_{\text{out}}}{I_{\text{out}}} - \frac{\dot{I}_{\text{p}_4}}{I_{\text{p}_4}} - \frac{\dot{I}_{\text{p}_3}}{I_{\text{p}_3}}\right), \tag{3.38c}$$

$$I_{C_2} = 2C_2U_T\left(\frac{\dot{I}_{\text{out}}}{I_{\text{out}}} - \frac{\dot{I}_{\text{p}_4}}{I_{\text{p}_4}} - \frac{\dot{I}_{\text{p}_3}}{I_{\text{p}_3}} - \frac{\dot{I}_{\text{p}_2}}{I_{\text{p}_2}}\right), \tag{3.38d}$$

$$I_{C_1} = 2C_1U_T\left(\frac{\dot{I}_{\text{out}}}{I_{\text{out}}} - \frac{\dot{I}_{\text{p}_4}}{I_{\text{p}_4}} - \frac{\dot{I}_{\text{p}_3}}{I_{\text{p}_3}} - \frac{\dot{I}_{\text{p}_2}}{I_{\text{p}_2}} - \frac{\dot{I}_{\text{p}_1}}{I_{\text{p}_1}}\right). \tag{3.38e}$$

Equations (3.38a) through (3.38e) already hint at the increasing complexity of the expressions for the capacitance currents. To obtain the transfer function of the filter, the currents I_{C_k} have to be rewritten in terms of the output current and its time derivatives.[2] The currents I_{C_4} down to I_{C_1} are treated successively, I_{C_5} being already in the right format. To obtain I_{C_4} in terms of the output current, first, eqn (3.38a) is substituted in (3.37b). This equation is then solved for I_{p_4}. Next, $\dot{I}_{\text{p}_4}$ is calculated, which involves the calculation of the time derivative $\dot{I}_{C_5}$ of I_{C_5}. Finally, substitution of the expressions for I_{p_4} and $\dot{I}_{\text{p}_4}$ result in an equation $I_{C_4} = I_{C_4}(I_{\text{out}}, \dot{I}_{\text{out}}, \ddot{I}_{\text{out}})$.

The currents I_{C_3} down to I_{C_1} are rewritten in a similar fashion. However, the derivative operations that have to be performed on the intermediate currents become more and more cumbersome. The intermediate expression swell is reflected in the capacitance currents, which become increasingly complicated. Equation (3.38a) gives an elegant expression for I_{C_5}, but I_{C_3} is already as complex as:

$$I_{C_3} = 2C_3U_T\frac{2C_4U_T\left(2C_5U_T\dddot{I}_{\text{out}} + I_{\text{o}}\ddot{I}_{\text{out}}\right) + I_{\text{o}}^2\dot{I}_{\text{out}}}{2C_4U_T\left(2C_5U_T\ddot{I}_{\text{out}} + I_{\text{o}}\dot{I}_{\text{out}}\right) + I_{\text{o}}^2 I_{\text{out}}}. \tag{3.39}$$

When all currents I_{C_k} are expressed as functions of the output current, the overall transfer function, a fifth-order DE, is obtained by elimination of the intermediate currents from eqn (3.37), followed by substitution of the expressions for the capacitance currents I_{C_k}.

Implementation of the exponential transformations Apparently, the global analysis method is not very suitable for the analysis by manual calculation of large TL filters. The large equations involved are cumbersome and error prone. As discussed, a significant simplification can be obtained by using a state-space approach.

[2] In general, the capacitance currents are expressed in terms of both the input current and the output current (and their time derivatives). However, for an all-pole low-pass filter, only the output current is required to describe the capacitance currents.

Since the filter contains five capacitors, five currents I_{x_l}, where $l \in [1, \ldots, 5]$, have to be defined to represent the state of the filter. The type of circuitry required to introduce I_{x_l} is derived from an examination of the output section of the filter. At the output, the voltage across C_5 is expanded exponentially by means of Q_{20} into a current I_{out}. Transistor Q_{19} only serves as a level shift. The use of a single (compound) device to generate the output current reveals that the circuit shown in Fig. 3.10 is in fact a log-domain filter. Consequently, the same output structure has to be used to generate the currents I_{x_1} through I_{x_4}; I_{x_5} is most favourably chosen to equal I_{out}.

The voltages across the capacitances vary but a few milli-volts from ground potential. As a result, the parallel connection of a (fictitious) compound transistor with each of the capacitances C_1 through C_4 requires a level shift in order to satisfy the STL principle. Since level shifts are already connected to the capacitances in the shape of Q_3, Q_7, Q_{11} and Q_{15}, the additional compound transistors Q_{21} through Q_{24} can be connected directly to the NPN-base-terminals of these transistors. This is illustrated in Fig. 3.10 by the dotted components.

Translinear analysis of the state-space filter circuit By the connection of the four extra transistors, four additional fundamental TL loops are introduced, corresponding to the introduction of four new intermediate currents I_{x_l}. The set of fundamental TL loops is completed by the addition of the loops Q_{21}-Q_3-Q_6-Q_5-Q_7-Q_{22}, Q_{22}-Q_7-Q_{10}-Q_9-Q_{11}-Q_{23}, Q_{23}-Q_{11}-Q_{14}-Q_{13}-Q_{15}-Q_{24}, and Q_{24}-Q_{15}-Q_{18}-Q_{17}-Q_{19}-Q_{20}. The corresponding loop equations are given by:

$$I_{x_l} I_{\text{p}_l} = I_{\text{o}} I_{x_{l+1}}, \qquad l \in [1, \ldots, 4]. \tag{3.40}$$

Elimination of the intermediate currents I_{p_j} from eqns (3.37) and (3.40) is straightforward. Solving the remaining system of five polynomials for the capacitance currents yields:

$$I_{C_1} I_{x_1} = I_{\text{o}} I_{\text{in}} - I_{\text{os}} I_{x_1} - I_{\text{o}} I_{x_2}, \tag{3.41a}$$
$$I_{C_2} I_{x_2} = I_{\text{o}} \left(I_{x_1} - I_{x_3} \right), \tag{3.41b}$$
$$I_{C_3} I_{x_3} = I_{\text{o}} \left(I_{x_2} - I_{x_4} \right), \tag{3.41c}$$
$$I_{C_4} I_{x_4} = I_{\text{o}} \left(I_{x_3} - I_{x_5} \right), \tag{3.41d}$$
$$I_{C_5} I_{x_5} = I_{\text{o}} I_{x_4} - I_{\text{ol}} I_{x_5}. \tag{3.41e}$$

Now, the improvement provided by the state-space analysis method is the simplicity of the expressions for the capacitance currents. Equation (3.24) is applied to express I_{C_k} in terms of I_{x_k} and $\dot{I}_{x_k}$. For example, to obtain I_{C_1}, eqn (3.24) is applied to the loop C_1-Q_3-Q_{21}. The capacitance currents are thus

readily attained as:

$$I_{C_k} = 2C_k U_T \frac{\dot{I}_{x_k}}{I_{x_k}}, \qquad k \in [1, \ldots, 5]. \tag{3.42}$$

Finally, substitution of eqn (3.42) yields a current-mode linear state-space description of the filter:

$$2U_T \begin{pmatrix} C_1\dot{I}_{x_1} \\ C_2\dot{I}_{x_2} \\ C_3\dot{I}_{x_3} \\ C_4\dot{I}_{x_4} \\ C_5\dot{I}_{x_5} \end{pmatrix} = \begin{pmatrix} -I_{os} & -I_o & 0 & 0 & 0 \\ I_o & 0 & -I_o & 0 & 0 \\ 0 & I_o & 0 & -I_o & 0 \\ 0 & 0 & I_o & 0 & -I_o \\ 0 & 0 & 0 & I_o & -I_{ol} \end{pmatrix} \begin{pmatrix} I_{x_1} \\ I_{x_2} \\ I_{x_3} \\ I_{x_4} \\ I_{x_5} \end{pmatrix} + \begin{pmatrix} I_o I_{in} \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix},$$

$$I_{out} = I_{x_5}. \tag{3.43}$$

Figure 3.11 shows the corresponding signal flow graph.

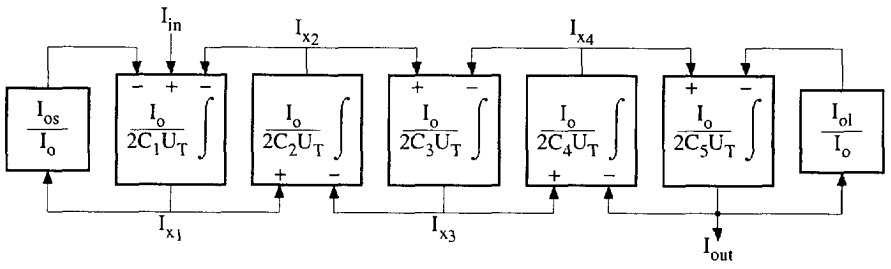

Figure 3.11: Signal flow graph corresponding to eqn (3.43).

3.2.3 Alternative analysis methods

Next to the analysis methods proposed in Sections 3.2.1 and 3.2.2, a number of alternative analysis methods for TL filters have been proposed in the literature. Since most publications on TL filters have been geared towards synthesis, the number of different analysis methods is smaller than the collection of synthesis techniques.

Since different points of view can provide complementary information, this section gives a short review of the various analysis methodologies. First of all, TL filters can be analysed using a voltage-mode instead of a current-mode approach. Both a *global* voltage-mode analysis method [1] and the corresponding *state-space* procedure are treated. Small-signal analysis of TL networks is described next, followed by the analysis of log-domain filters based on Bernoulli's DE [14].

Global voltage-mode analysis

In [1], Adams not only presented a synthesis method for log-domain filters, but also proposed an analysis method to calculate the non-linear error terms resulting from his synthesis procedure. The first step of the analysis method is to write down the node equations from the large-signal ac model of the filter. Next, the equations containing the derivative of a capacitance voltage are multiplied by an exponential term. Using the chain rule of differentiation, the isolated derivatives can be eliminated, as follows:

$$\dot{V}_{\text{cap}} \xrightarrow{\text{multiply by } \mathrm{e}^{\frac{V_{\text{cap}}}{U_T}}} \dot{V}_{\text{cap}}\mathrm{e}^{\frac{V_{\text{cap}}}{U_T}} = U_T \frac{\mathrm{d}}{\mathrm{d}t}\mathrm{e}^{\frac{V_{\text{cap}}}{U_T}}. \tag{3.44}$$

Now, the intermediate node voltages have to be eliminated from the system of equations, such that a single one results expressing the relation between the compressed input and output voltage. Unfortunately, according to Adams no systematic method might exist for this step [1]. In the last analysis step, a DE is obtained from this single equation by applying a logarithmic transformation; the inverse of the transformation used during synthesis.

Implicitly, the voltage-mode analysis method has been applied in numerous publications on log-domain filters to verify parts of transistor level implementations. In [15], an example can be found of the analysis of a complete second-order TL filter. Note that in most of these papers, the application of the voltage-mode analysis method is simplified by direct substitution of the overall V-I transfer function of prevalent building blocks, thus reducing the number of intermediate voltages and node equations.

An apparent drawback of voltage-mode analysis is the abundant usage of transcendental equations, hindering a clear understanding of the circuit. Furthermore, eqn (3.44) only applies to log-domain filters. Different functions are required for other types of DTL circuits, such as tanh and sinh filters. The transformation to be applied has to be derived from the circuit structure, which might be a complicated task in some situations.

As an example of the voltage-mode analysis procedure, consider the circuit shown in Fig. 3.5. The nodal equation for node ① is given by [1,3]:

$$C\dot{V}_{\text{cap}} = I_{\text{s}} \exp \frac{V'_{\text{in}} - V_{\text{cap}}}{U_T} - I_{\text{o}}, \tag{3.45}$$

where V_{cap} is the capacitance voltage and V'_{in} is the compressed input voltage, i.e., the output voltage of the input op amp.

Multiplication of eqn (3.45) by $\exp V_{\text{cap}}/U_T$ yields:

$$CU_T \frac{\mathrm{d}}{\mathrm{d}t}\mathrm{e}^{\frac{V_{\text{cap}}}{U_T}} = I_{\text{s}} \exp \frac{V'_{\text{in}}}{U_T} - I_{\text{o}} \exp \frac{V_{\text{cap}}}{U_T}. \tag{3.46}$$

Application of the logarithmic transformations $V'_{\text{in}} = U_T \ln (I_{\text{in}} + I_{\text{dc}})/I_{\text{s}}$ and $V_{\text{cap}} = U_T \ln (I_{\text{out}} + I_{\text{dc}})/I_{\text{o}}$, finally yields the linear DE given by (3.21).

State-space voltage-mode analysis

A considerable simplification of the voltage-mode analysis method can be obtained using a state-space approach. Eliminating all intermediate voltages with the exception of the capacitance voltages, a set of nodal equations results that can be transformed directly into a state-space representation of the filter using a logarithmic transformation. This method is the voltage-mode equivalent of the current-mode state-space analysis method described in Section 3.2.2.

Small-signal analysis

A very basic way to calculate the transfer function of a complete filter is to analyse the small-signal equivalent circuit, see, e.g., [5]. Since, by definition, a small-signal analysis results in a linear transfer function, this method yields the correct expression only when the overall transfer function of the TL circuit under consideration is theoretically linear for large signals. Obviously, it is a misconception to argue that large-signal linearity allows the use of a small-signal analysis method [90], as the large-signal linearity is not known *a priori*. Using small-signal analysis, the large-signal linearity cannot be proven and has to be verified in another way. Obviously, this method cannot be applied to TL circuits realising non-linear functions.

Analysis based on Bernoulli's differential equation

An alternative *current-mode* analysis method has been proposed by Drakakis *et al.* in [14]. This method can be used to analyse log-domain filters based on the generic structure shown in Fig. 3.12. The currents I_{u_k}, where $k \in [1, \ldots, n]$ and n denotes the order of the filter, determine the transfer function of the filter. The currents I_{o_k} are dc bias currents. For the moment, the dotted components can be ignored.

The analysis is based on the 'Bernoulli cell', shown in Fig. 3.13, which is a basic element of the generic structure shown in Fig. 3.12. The Bernoulli cell is described by a DE:

$$\dot{T}_k + \left(\dot{V}_{\mathrm{B}_k} + \frac{I_{u_k}}{C_k}\right)\frac{T_k}{U_T} = \frac{1}{CU_T}, \tag{3.47}$$

where V_{B_k} is a base voltage and $1/T_k$ a collector current, as shown in Fig. 3.13.

For the first cell, the derivative $\dot{V}_{\mathrm{B}_1}$ equals:

$$\dot{V}_{\mathrm{B}_1} = U_T \frac{\mathrm{d}}{\mathrm{d}t} \ln \frac{I_{\mathrm{in}}}{I_{\mathrm{s}}}, \tag{3.48}$$

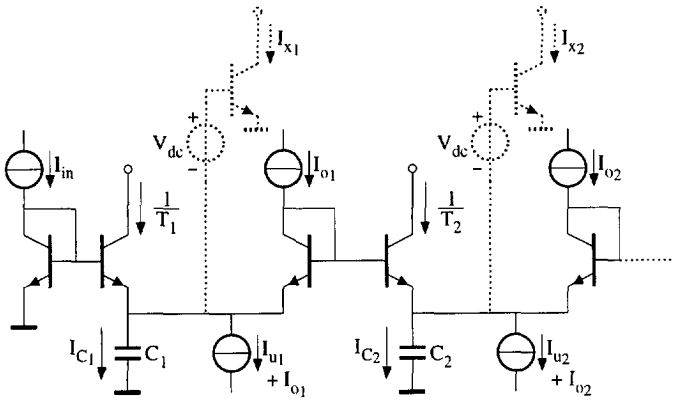

Figure 3.12: Generic structure that can be analysed with the analysis method based on Bernoulli's differential equation [14].

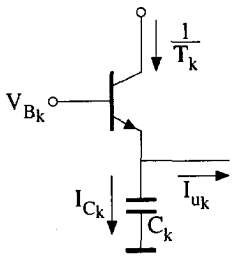

Figure 3.13: Bernoulli cell [14].

where I_{in} is the input current of the filter. Substitution of eqn (3.48) in (3.47) for $k = 1$ yields:

$$C_1 U_T \frac{\mathrm{d}}{\mathrm{d}t} \ln I_{\text{in}} T_1 + I_{u_1} = \frac{1}{T_1}. \tag{3.49}$$

Equation (3.49) can be generalised to:

$$C_k U_T \frac{\mathrm{d}}{\mathrm{d}t} \ln c_k I_{\text{in}} T_1 \ldots T_k + I_{u_k} = \frac{1}{T_k}, \tag{3.50}$$

where c_k is a constant with dimension $[\mathrm{A}^{k-1}]$. Note that the first term on the LHS represents the capacitance current I_{C_k}.

Definition of a current $I_{x_k} = c'_k I_{\text{in}} T_1 \ldots T_k$, where c'_k is a constant with dimension $[\text{A}^k]$, and substitution in eqn (3.50) yields:

$$C_k U_T \dot{I}_{x_k} + I_{u_k} I_{x_k} = \frac{c'_k}{c'_{k-1}} I_{x_{k-1}}. \tag{3.51}$$

By definition, I_{x_0} equals I_{in}.

Application of eqn (3.50) to all capacitors yields a set of n first-order DEs; a state-space description of the filter. It is interesting to note that the capacitance currents in terms of I_{x_k} are given by:

$$I_{C_k} = C_k U_T \frac{\text{d}}{\text{d}t} \ln \frac{c_k}{c'_k} I_{x_k}. \tag{3.52}$$

Elaboration of the logarithm yields an expression similar to eqn (3.42). Hence, it can be concluded that, although the derivation is different, the analysis method based on the Bernoulli DE is identical to the state-space analysis method described in Section 3.2.2. However, the method by Drakakis *et al.* has been derived only for log-domain filters. Finally, note that the currents I_{x_k} are the collector currents of the dotted components shown in Fig. 3.12.

3.3 Characteristics of different translinear filter classes

Several types of DTL networks can be distinguished within the overall class of DTL circuits, based on the variety of possible exponential-like relations between the voltages and currents. In a TL filter, the specific transconductance equation is reflected by the output stage. Here, the capacitor is considered to be a part of the output stage. Hence, the output stage converts a capacitance voltage into an output current. Alternatively speaking, from a current-mode point of view, the relation between the capacitance current and the output current is determined by a different capacitance-junction(s) loop.

This section is devoted to the analysis of the various types of TL filters. The characteristics of each particular class of DTL circuits are derived from the generic output stage and the corresponding expression for the capacitance current. The discussion is limited to those types of DTL networks that have been proposed in the literature: log-domain, tanh and sinh filters.[3] The characteristics of these three classes are treated in Sections 3.3.1, 3.3.2 and 3.3.3, respectively.

[3]Note that these names are not used consistently, for 'log' refers to an I-V transfer function, whereas 'tanh' and 'sinh' refer to a V-I transfer function. Therefore, the extension 'domain' is not used here for tanh and sinh filters, where the voltages are processed in the $\tanh^{-1}$ and $\sinh^{-1}$ domains, whereas in log-domain filters, the voltages are indeed processed in the log-domain.

3.3.1 log-domain filters

From the perspective of circuit implementation, the most simple relation between the collector currents and the capacitance voltages in a TL filter is the pure exponential function. Applying the exponential law describing the (bipolar) transistor, this relation can be implemented by a single transistor, a Common-Emitter (CE) stage, as illustrated in Fig. 3.14. This generic output stage is identical to the sub-circuit shown in Fig. 2.7, as the level shift shown in Fig. 2.7 does not have any influence on the capacitance current I_{cap}. Translinear filters based on the single transistor output stage are called 'log-domain filters', as the capacitance voltage V_{cap} is logarithmically related to the collector current.

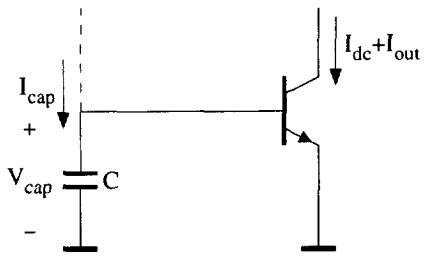

Figure 3.14: Generic output stage of a log-domain filter.

The exponential V-I relation of a CE stage is highly non-linear. Hence, this transconductance stage is not frequently applied in conventional filters to implement a 'linear' transconductance. Instead, a differential pair is more likely to be encountered as the differential operation implies the elimination of even-order distortion components and hence a better linearity of the V-I conversion. Linearity of the transconductances is not an issue for TL filters, as they are based on the theory of distortionless companding described in Chapter 2.

Class-A operation

The collector current of the output stage has to be strictly positive for the transistor to work in the active exponential region. Consequently, class-A operation is required to process a zero-mean output signal. That is, the actual bipolar-valued output current I_{out} is superposed on a dc bias current I_{dc}. For the output stage to operate correctly, the inequality $I_{\text{out}} > -I_{\text{dc}}$ has to be satisfied at all times. Lower values of I_{out} result in clipping distortion.

Instantaneous companding

The collector current of the log-domain output stage is exponentially related to the capacitance voltage:

$$I_{\mathrm{dc}} + I_{\mathrm{out}} = I_{\mathrm{s}} \exp \frac{V_{\mathrm{cap}}}{U_T}. \tag{3.53}$$

This exponential function can be identified with the output expansion function $E(x)$, depicted in the general schematic of an instantaneous companding linear integrator, see Fig. 3.17. Thus, the companding characteristics of log-domain filters are directly related to eqn (3.53).

Applying a strict definition of companding, the function $E(x)$ should be expanding. Without loss of generality, $x = 0$ is considered to be the quiescent point. Then, a genuine expansion function is characterised by an increasing value of the first-order derivative of $E(x)$ with respect to x for increasing values of $x > 0$. Consequently, the second-order derivative with respect to x is strictly positive for $x > 0$. For $x < 0$, the first-order derivative of $E(x)$ increases for decreasing values of x, the second-order derivative is therefore strictly negative.

Figure 3.15 shows a plot of the exponential function $\exp x$. Of course, the first-order and second-order derivatives with respect to x are equal to $\exp x$ as well. The quiescent point $x = 0$ complies with $V_{\mathrm{cap}} = U_T \ln I_{\mathrm{dc}}/I_{\mathrm{s}}$ in eqn (3.53). Now, a comparison of the second-order derivative, $\exp x$, with the general characteristics of a true expansion output stage, reveals that the generic output function (3.53) of a log-domain filter is indeed expanding for $x > 0$. However, for $x < 0$ the second-order derivative is positive as well. This implies a *compression* for $x < 0$.

For a symmetrical output current, the overall behaviour of the CE output stage implies a compression rather than an expansion of the peak-to-peak signal swings [90]. For example, a sinusoidal output current with an amplitude of 0.1 I_{dc} results in a peak-to-peak voltage swing of 0.20 U_T; an amplitude of 0.9 I_{dc} results in a voltage swing of 2.94 U_T. Hence, the voltage swing increases by a factor 14.7, whereas the current swing only increases by a factor 9.

Capacitance current

In correspondence with the current-mode nature of TL circuits, the expression for the capacitance current is even more interesting than the capacitance voltage. The capacitance current is related to the collector current of the output transistor and is given by:

$$I_{\mathrm{cap}} = C U_T \frac{\dot{I}_{\mathrm{out}}}{I_{\mathrm{dc}} + I_{\mathrm{out}}}. \tag{3.54}$$

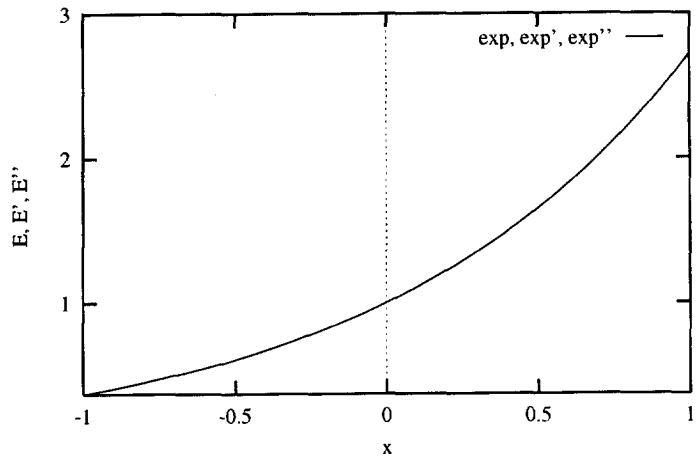

Figure 3.15: The normalised output-expansion function of log-domain filters.

The exponential transconductance of the log-domain output stage results in a non-linear dynamic relation between I_{cap} and I_{out}. Figure 3.16 illustrates this non-linear dynamic relation, eqn (3.54), under the assumption of a sinusoidal output current, given by:

$$I_{\text{out}} = mI_{\text{dc}} \sin \omega t, \tag{3.55}$$

where m is the modulation index. The numerical values of the relevant parameters used in Fig. 3.16 are: $C = 10$ pF, $U_T = 26$ mV and $\omega = 3.85$ Mrad/s.

As shown in Fig. 3.16, I_{cap} is nearly sinusoidal for low values of m. With reference to eqn (3.54), this linear behaviour can be explained through the denominator of (3.54), which is approximately constant. The non-linearity of I_{cap} increases when m approaches the value of one, as the minimum value of the denominator of eqn (3.54) then approaches zero. The denominator attains its minimum value when I_{out} is minimal. Hence, the maximal capacitance current swings are obtained symmetrically around $I_{\text{out}} = -mI_{\text{dc}}$. It is interesting to note that the increasing non-linearity is related to the class-A operation of the log-domain output stage. The characteristics of this mode of operation are thus retained in the denominator of eqn (3.54) for I_{cap}.

In a complete TL filter, the value of m is determined by the (modulus of the) filter transfer function.

Global linearisation

Despite the non-linear nature of the capacitance currents in a TL filter, an exactly linear transfer function can be realised in theory. The DTL principle

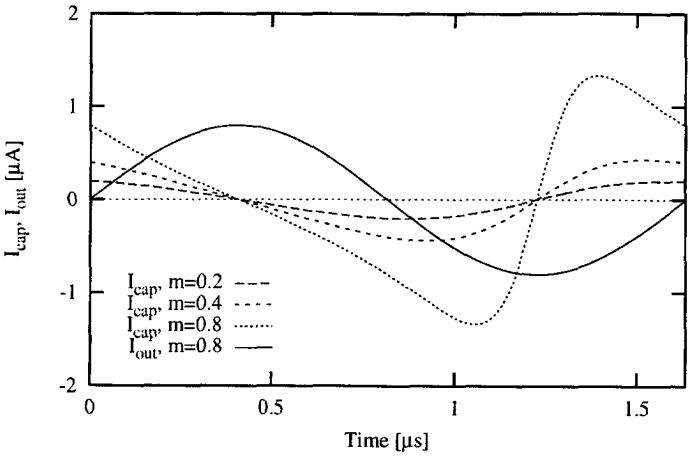

Figure 3.16: Generic capacitance current of a log-domain output stage.

states that a linear derivative can be obtained when a capacitance current is multiplied by some other currents. In the case of a log-domain filter, I_{cap} has to be multiplied by the collector current to which I_{cap} is related. Consequently, the capacitance current shown in Fig. 3.14 has to be multiplied by $I_{\text{dc}} + I_{\text{out}}$ to obtain a linear derivative $\dot{I}_{\text{out}}$, given by:

$$CU_T\dot{I}_{\text{out}} = I_{\text{cap}}\left(I_{\text{dc}} + I_{\text{out}}\right). \tag{3.56}$$

It is interesting to compare this result to the general schematic of a distortionless instantaneous companding integrator, see Fig. 3.17. Clearly, the capacitance C performs the integration function shown in Fig. 3.17. The resulting voltage $x = V_{\text{cap}}$ is expanded by the exponential law (3.53) into the output current $y = I_{\text{dc}} + I_{\text{out}}$. The derivative $\dot{y}$ represents the linear derivative $CU_T\dot{I}_{\text{out}}$. Now the input current $\dot{x} = I_{\text{cap}}$ to the integrator is generated by dividing $\dot{y} = CU_T\dot{I}_{\text{out}}$ by $\partial E(x)/\partial x = E(x)$, which simply equals $y = I_{\text{out}}$, owing to the characteristics of the exponential function. Hence, $\dot{x}$ is proportional to $\dot{I}_{\text{out}}/I_{\text{out}}$ in correspondence with eqn (3.54).

Linear damping

A favourable property of log-domain filters is that a linear damping term can be implemented by the connection of a dc current source I_{o} in parallel to a capacitor. This characteristic can be explained from eqns (3.54) and (3.56). The linear derivative $\dot{I}_{\text{out}}$ is obtained by multiplication of I_{cap} by $(I_{\text{dc}} + I_{\text{out}})$. If instead of I_{cap}, $(I_{\text{cap}} + I_{\text{o}})$ is multiplied by this current, two additional terms $(I_{\text{o}}I_{\text{dc}} + I_{\text{o}}I_{\text{out}})$ are generated at the LHS of eqn (3.56). The first term $I_{\text{o}}I_{\text{dc}}$

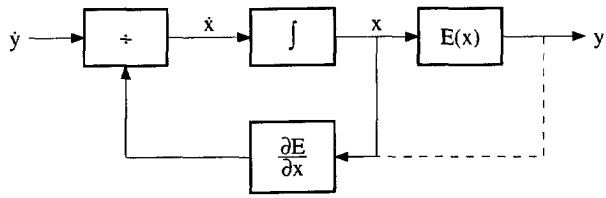

Figure 3.17: General block schematic of an instantaneous companding integrator.

represents a dc offset current. The second term $I_o I_{out}$ results in a finite negative pole.

The creation of a linear damping term by means of a dc current source is possible owing to the fact that the denominator of eqn (3.54) is a linear function of I_{out}. This property is not valid for TL filters in general. For example, the denominators of eqns (3.59) and (3.71), which are given by $I_{dc}^2 - I_{out}^2$ and $\sqrt{4I_{dc}^2 + I_{out}^2}$, respectively, are not linear in I_{out}. Consequently, for tanh and sinh filters a dc current source connected in parallel with a capacitor does not result in a linear damping term.

Since in practice a capacitance current does not have a dc term associated with it, and the collector currents in a TL circuit have to be strictly positive, a dc term has to be added to I_{cap} for biasing purposes. For example, regard the TL integrator shown in Fig. 3.8. To correctly bias Q_3, a current I_o is added to I_{cap}, which results in damping, as explained in the foregoing. To cancel this undesired effect, the current mirror Q_4-Q_5 provides positive feedback. As, in theory, the effects of I_o and Q_5 cancel out exactly, the ideal transfer function of this circuit is a loss-less integration. This effect can be deduced from the TL loop equation (3.33) as well: both sides contain a redundant term $I_o I_{out}$.

Class-AB operation

Typically, log-domain filters operate in class A. As a result, the output current is limited by $I_{out} > -I_{dc}$. This restriction on the output signal swing is only single-sided, which is advantageous if a-symmetrical wave forms have to be processed. This fact can be exploited to enable class (A)B operation [2, 91]. Naturally, not only the output stage, but all other parts of the complete filter have to be subject to the same single-sided limitation.

Figure 3.18 shows the general set-up for class-AB operation. In this set-up, a static non-linear current splitter is used at the input to divide the input current I_{in} into two currents I_{in_1} and I_{in_2}, which are both strictly positive. These signals are related to I_{in} by: $I_{in} = I_{in_1} - I_{in_2}$. The two parts of the input signal are now processed by two separate signal paths, with a transfer function F. The resulting output currents I_{out_1} and I_{out_2} are subtracted to obtain the overall

output current I_{out}, the linearly filtered version of I_{in}. If the signal path F only has a single-sided restriction with respect to the currents being processed, the dynamic range of the log-domain filter is no longer theoretically limited by a dc current I_{dc}. A more thorough treatment of class-AB operation is given in Section 4.7.

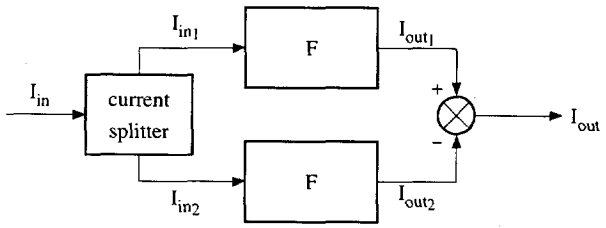

Figure 3.18: General set-up for class (A)B operation [91].

3.3.2 tanh filters

Instead of a single transistor in common-emitter configuration, the class of tanh filters is characterised by a differential pair output structure, see Fig. 3.19. The name of this class of filters is derived from the well-known hyperbolic tangent V-I transfer function of the differential pair. The capacitance voltage V_{cap} is the input voltage. The output current I_{out} is the difference of the two collector currents.

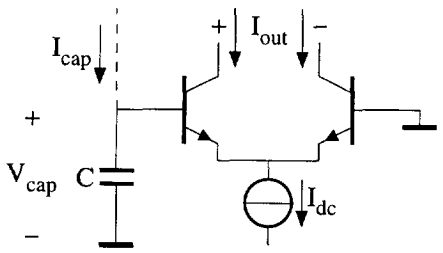

Figure 3.19: Generic output stage of tanh filters.

Class-A operation

The differential pair is biased by a dc current source I_{dc}. The limited tail current restricts the output current to the range $-I_{dc} < I_{out} < I_{dc}$. Since this interval is symmetrical, tanh filters cannot be operated in class AB.

In conventional filters, the differential pair is often used as a simple implementation of an Operational Transconductance Amplifier (OTA). Due to its symmetry, the transconductance of the differential pair is much more linear than the transconductance of a CE stage. Nevertheless, the remaining nonlinearity restricts the operating range of the OTA. A typical Total Harmonic Distortion (THD) level of -40 dB is obtained for a sinusoidal input voltage with an amplitude of only 0.7 U_T. The corresponding amplitude of I_{out} is 0.34 I_{dc}.

Whereas OTA-C filters based on the sub-circuit shown in Fig. 3.19 can only use 34% of the dc bias current, tanh filters can exploit the complete class-A operating range. The theoretically possible improvement of the dynamic range can be calculated for a specified distortion level, when the influence of the remaining circuitry of the tanh filter is neglected. For a THD level of -40 dB, the maximum improvement is 9.5 dB. This compares well with the 10 dB improvement reported in [10], based on 2.6% intermodulation distortion.

Instantaneous companding

The transcendental relation between I_{out} and V_{cap} is expressed by the hyperbolic tangent function:

$$I_{\text{out}} = I_{\text{dc}} \tanh \frac{V_{\text{cap}}}{2U_T}. \tag{3.57}$$

Figure 3.20 depicts the normalised hyperbolic tangent function $\tanh x$, as well as its first- and second-order derivatives. Obviously, the first-order derivative, representing the small-signal transconductance, decreases for x moving away from the quiescent point $x = 0$. Hence, the second-order derivative is strictly negative for $x > 0$ and strictly positive for $x < 0$. Identifying the differential pair with the output expansion stage $E(x)$ shown in Fig. 3.17 and applying the genuine definitions of compression and expansion, it is concluded that tanh filters are not companding [92]. The relative output current swing is smaller than the relative capacitance voltage swing.

This can be illustrated by a numerical example. For a sinusoidal output current, eqn (3.55), with $m = 0.1$ and 0.9, the amplitude of the capacitance voltage swing equals 0.20 and 2.94 U_T, respectively. Again, the voltage swing increases by a factor of 14.6, while the current swing increases only by a factor of 9.

Capacitance current

In the generic tanh output stage, the capacitance C forms a loop with the two transistors of the differential pair. Using eqn (3.24), the capacitance current

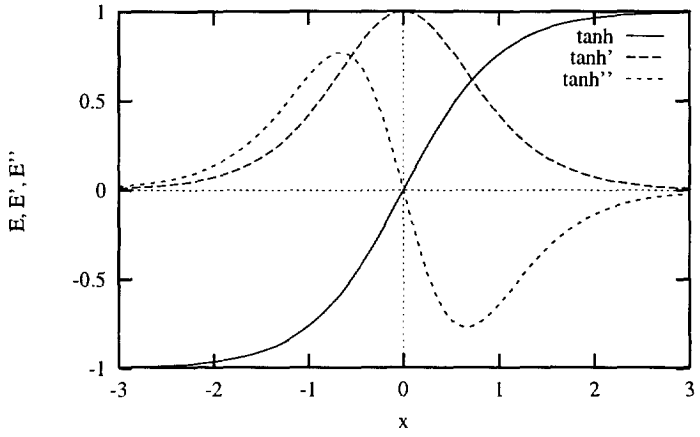

Figure 3.20: The (derivatives of the) normalised output-expansion function of tanh filters.

I_{cap} is found to be:

$$I_{\text{cap}} = CU_T \left(\frac{\dot{I}_{\text{out}}}{I_{\text{dc}} + I_{\text{out}}} - \frac{-\dot{I}_{\text{out}}}{I_{\text{dc}} - I_{\text{out}}} \right), \tag{3.58}$$

$$= 2CU_T \frac{I_{\text{dc}} \dot{I}_{\text{out}}}{I_{\text{dc}}^2 - I_{\text{out}}^2}. \tag{3.59}$$

Note that the class-A characteristics of tanh filters can be derived from the denominators of eqns (3.58) and (3.59).

Figure 3.21 illustrates the non-linear dynamic relation between I_{cap} and I_{out}. In this figure, I_{out} is given by eqn (3.55). Further, $C = 10$ pF, $U_T = 26$ mV and $\omega = 3.85$ Mrad/s. As could have been expected, the non-linearity of I_{cap} increases when the modulation index m approaches one. For values of m close to zero, the denominator of eqn (3.59) is approximately constant, resulting in a linear behaviour of I_{cap}. The denominator reaches its minimum value when $I_{\text{out}} = \pm m I_{\text{dc}}$, and therefore, the maximums of I_{cap} are found symmetrically around these two points. The compressing nature of the tanh output stage can also be derived from these plots of I_{cap}, as the total area under the plot $|I_{\text{cap}}|$ increases more than proportional to m.

Global linearisation

To obtain a linear tanh filter, I_{cap} has to be multiplied by the denominator $I_{\text{dc}}^2 - I_{\text{out}}^2$ of eqn (3.59). This polynomial represents the output of the feedback

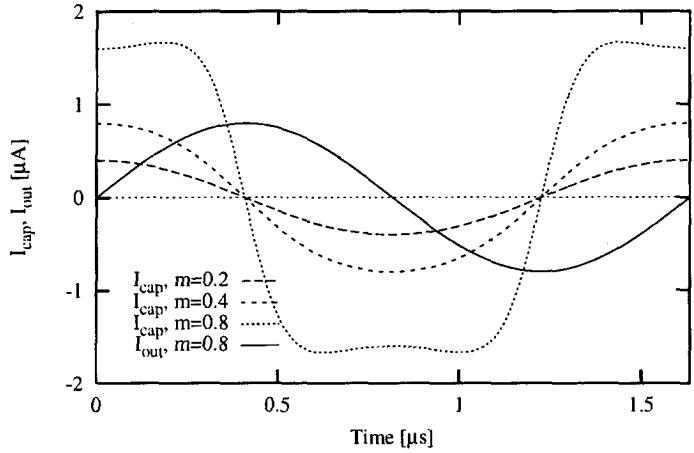

Figure 3.21: Generic capacitance current for a tanh output stage.

block $\partial E/\partial x = 1 - \tanh^2 x$, shown in Fig. 3.17. Thus, a linear derivative $\dot{I}_{\text{out}}$ is obtained:

$$2CU_T I_{\text{dc}} \dot{I}_{\text{out}} = I_{\text{cap}} \left(I_{\text{dc}} + I_{\text{out}}\right) \left(I_{\text{dc}} - I_{\text{out}}\right). \tag{3.60}$$

A comparison of eqns (3.56), (3.60) and (3.73) shows that the dimensions of these equations are [A^2], [A^3] and [A^2], respectively. This implies that a third-order polynomial is required to implement a linear derivative in a tanh filter, whereas only a second-order polynomial is required in log-domain and sinh filters. Consequently, the circuitry required to realise a tanh filter is in general more complex. In addition, a linear loss term cannot be implemented by the connection of a dc current source in parallel with a capacitance, as explained in Section 3.3.1.

Example: Analysis of a tanh first-order low-pass filter

Figure 3.22 shows an example of a tanh filter [4]. The output stage, see Fig. 3.19, is formed by transistors Q_9 and Q_{10}. A PNP current mirror is used to obtain a single-ended output current I_{out}.

Apart from the current mirrors, the tanh filter comprises three second-order TL loops. The first loop is formed by Q_1–Q_4. The other two loops are coupled and consist of Q_5–Q_8 and Q_6-Q_5-Q_9-Q_{10}, respectively.

To calculate the transfer function of the filter, first the KCLs are used to find expressions for the collector currents. Since the filter contains three TL loops, two intermediate currents have to be introduced. By definition, the collector currents of Q_5 and Q_8 are equated to I_{p_1} and I_{p_2}, respectively. Since the tail

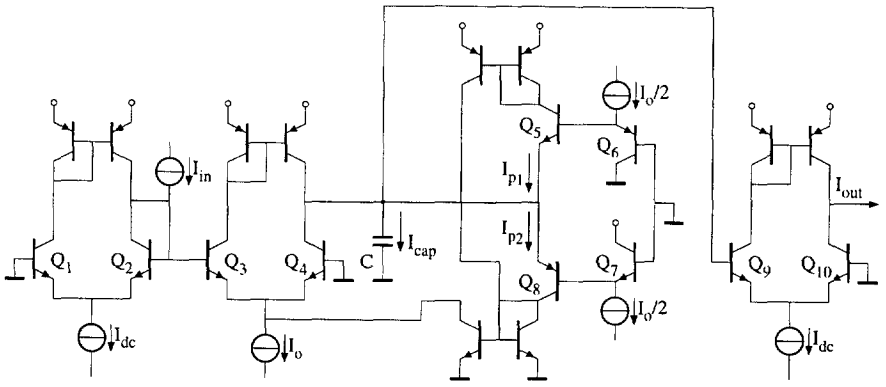

Figure 3.22: A tanh first-order low-pass filter [4].

current of the differential pair Q_3-Q_4 amounts to $I_o + I_{p_1} + I_{p_2}$, while its output equals $I_{cap} - I_{p_1} + I_{p_2}$, the collector currents I_3 and I_4 of Q_3 and Q_4 are given by:

$$I_3 = \tfrac{1}{2}\left(I_o + I_{cap} + 2I_{p_2}\right), \tag{3.61}$$

$$I_4 = \tfrac{1}{2}\left(I_o - I_{cap} + 2I_{p_1}\right). \tag{3.62}$$

Hence, the loop equations are readily found to be:

$$\left(I_{dc} - I_{in}\right)\left(I_o + I_{cap} + 2I_{p_2}\right) = \left(I_{dc} + I_{in}\right)\left(I_o - I_{cap} + 2I_{p_1}\right), \tag{3.63a}$$

$$I_o^2 = 4I_{p_1}I_{p_2}, \tag{3.63b}$$

$$I_o\left(I_{dc} - I_{out}\right) = 2I_{p_1}\left(I_{dc} + I_{out}\right). \tag{3.63c}$$

Elimination of I_{p_1} and I_{p_2} from the system of TL loop equations yields a third-order polynomial:

$$I_{cap}\left(I_{out} + I_{dc}\right)\left(I_{dc} - I_{out}\right) + 2I_oI_{dc}I_{out} = 2I_oI_{dc}I_{in}. \tag{3.64}$$

In accordance with eqn (3.60), the first term on the LHS of (3.64) equals $2CU_TI_{dc}\dot{I}_{out}$. Substitution of eqn (3.60) for I_{cap} finally yields the DE describing the linear filter transfer function:

$$CU_T\dot{I}_{out} + I_oI_{out} = I_oI_{in}. \tag{3.65}$$

3.3.3 sinh filters

The third type of TL filters treated in this section is the class of sinh filters [4,10,36,77,93]. The generic output structure of this class of TL filters, which is

depicted in Fig. 3.23, comprises a complete second-order TL loop, Q_1–Q_4. This loop implements the function:

$$I_{dc}^2 = I_{out_1} I_{out_2}, \tag{3.66}$$

where I_{out_1} and I_{out_2} are the collector currents of Q_2 and Q_3. The actual output current I_{out} is the difference of I_{out_1} and I_{out_2}.

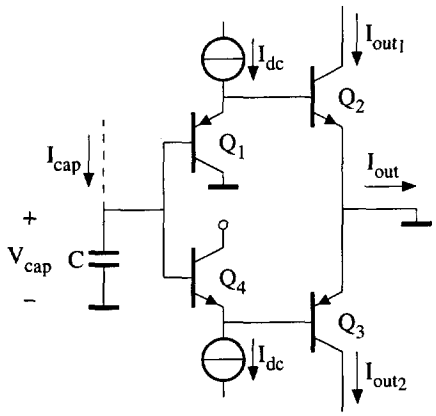

Figure 3.23: Generic output stage of sinh filters.

Class-AB operation

Transistors Q_2 and Q_3 can be considered as being two separate signal paths for the output current, similar to the set-up shown in Fig. 3.18. Equation (3.66) forces I_{out_1} and I_{out_2} to have a constant geometric mean. The relation between $I_{out_{1,2}}$ and the actual output current I_{out} is given by:

$$I_{out_{1,2}} = \tfrac{1}{2}\left(\sqrt{4I_{dc}^2 + I_{out}^2} \pm I_{out}\right). \tag{3.67}$$

Since the collector currents I_{out_1} and I_{out_2} are strictly positive, the sinh output stage operates in class AB. Naturally, for an entire sinh filter to operate in class AB, not only the output stage, but also the various other parts of the filter have to facilitate class-AB operation.

Instantaneous companding

The V-I transfer function of the sinh output structure is described by the hyperbolic sine function:

$$I_{out} = 2I_{dc} \sinh \frac{V_{cap}}{U_T}. \tag{3.68}$$

The normalised hyperbolic sine function $\sinh x$ is plotted in Fig. 3.24, along with the first-order derivative $\cosh x$. The expanding characteristics of the sinh output stage can be derived from the second-order derivative, which again equals $\sinh x$. Since the second-order derivative is strictly positive for $x > 0$ and strictly negative for $x < 0$, $x = 0$ being the quiescent point, the hyperbolic sine function is a genuine expansion function.

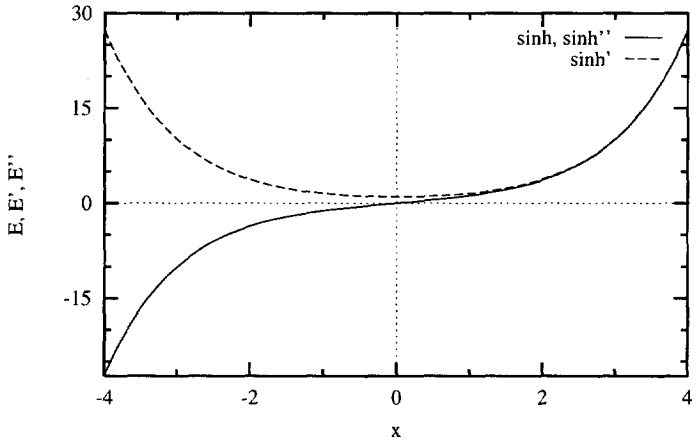

Figure 3.24: The (derivatives of the) normalised output-expansion function of sinh filters.

This can be illustrated by a numerical example. For a sinusoidal output current, eqn (3.55), with $m = 1$ and 9, the amplitude of the capacitance voltage swing equals 0.48 and 2.21 U_T, respectively. Consequently, whereas the current swing increases by a factor of 9, the voltage swing increases only by a factor of 4.59.

Capacitance current

Applying eqns (3.24) and (3.67), several equivalent expressions for the capacitance current I_{cap} associated with the sinh structure can be obtained:

$$I_{\text{cap}} = CU_T \frac{\dot{I}_{\text{out}_1}}{I_{\text{out}_1}}, \tag{3.69}$$

$$= -CU_T \frac{\dot{I}_{\text{out}_2}}{I_{\text{out}_2}}, \tag{3.70}$$

$$= CU_T \frac{\dot{I}_{\text{out}}}{\sqrt{4I_{\text{dc}}^2 + I_{\text{out}}^2}}, \tag{3.71}$$

$$= CU_T \frac{\dot{I}_{\text{out}}}{I_{\text{out}_1} + I_{\text{out}_2}}. \tag{3.72}$$

Figures 3.25 and 3.26 illustrate the relation between I_{cap} and I_{out}. In order to make a comparison possible between the capacitance currents of log-domain, tanh and sinh filters, in Fig. 3.25 the same values of the modulation index are used as in Figs 3.16 and 3.21. For the sinh output structure, even for a modulation index of $m = 0.8$, the denominator of eqn (3.71) does not vary much, and as a result, I_{cap} approximately equals a cosine function. Only for values of m well above one does the capacitance current become more non-linear, as shown in Fig. 3.26. The denominator of eqn (3.71) is minimal for $I_{\text{out}} = 0$ and I_{cap} therefore attains its maximum signal swing at this point.

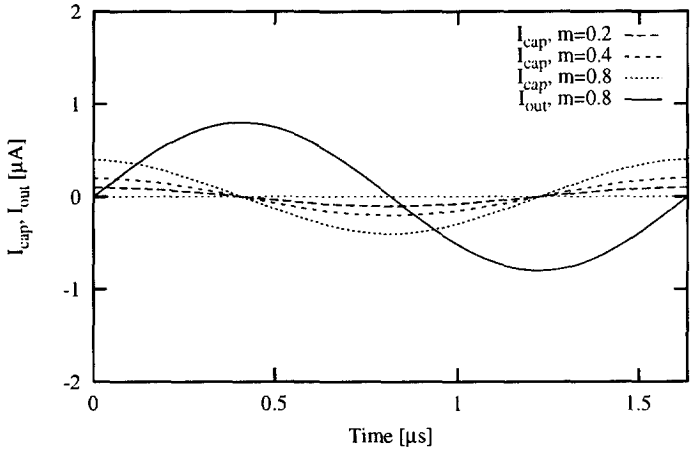

Figure 3.25: Generic capacitance current for a sinh output stage, for small signal swings.

Global linearisation

Application of the sinh output stage has also been proposed in the context of conventional filter implementations [94]. For conventional filters, the non-linearity of this transconductance implementation restricts the operating range. For a typical THD level of -40 dB, a maximal sinusoidal input voltage swing of 0.5 U_T can be applied. The corresponding amplitude of I_{out} is 1.0 I_{dc}.

Whereas only 1.0 times the dc bias current can be used in conventional filter implementations, in TL filters, a theoretically infinite dynamic range is possible. Equation (3.72) shows that a linear derivative $\dot{I}_{\text{out}}$ is obtained by multiplying

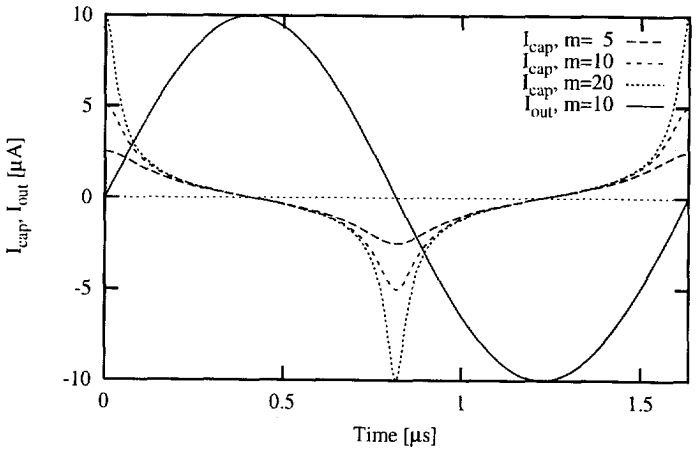

Figure 3.26: Generic capacitance current for a sinh output stage, for large signal swings.

I_{cap} by $I_{\text{out}_1} + I_{\text{out}_2}$:

$$CU_T \dot{I}_{\text{out}} = I_{\text{cap}} \left(I_{\text{out}_1} + I_{\text{out}_2} \right). \tag{3.73}$$

With respect to Fig. 3.17, for the sinh filter, $E(x)$ equals $\sinh x = I_{\text{out}}$. The derivative $\partial E / \partial x$ equals an hyperbolic cosine function, $\cosh x$. This cosh function represents the transfer function from V_{cap} to the denominator $I_{\text{out}_1} + I_{\text{out}_2}$ of eqn (3.72).

Example: Analysis of a sinh second-order band-pass filter

The generic sinh output structure, consisting of the compound transistors Q_{11}-Q_{12}-Q_{13}-Q_{14} and connected to capacitor C_1, is readily recognised in the sinh filter shown in Fig. 3.27 [10]. To facilitate a state-space analysis of this filter, a similar output structure, Q_{21}–Q_{24}, has been connected to C_2. Together, the currents I_{out} and I_x represent the state of the filter.

Including the additional circuitry, the dotted components, the sinh filter comprises nine fundamental TL loops. This number corresponds to the total number of unknown currents; the output and intermediate currents, denoted in Fig. 3.27 by I_{in_1}, I_{out_1}, I_{out_2}, I_{x_1}, I_{x_2}, I_{p_1}, I_{p_2}, I_{q_1} and I_{q_2}. Based on the KCL equations, all collector currents can be expressed in terms of the input currents and the nine unknowns. The states I_{out} and I_x are related to the nine unknowns by $I_{\text{out}} = I_{\text{out}_1} - I_{\text{out}_2}$ and $I_x = I_{x_1} - I_{x_2}$.

Apart from the two sinh output structures, the filter contains three other geometric mean TL loops: Q_1–Q_4, Q_5–Q_8, and Q_{15}–Q_{18}. The corresponding

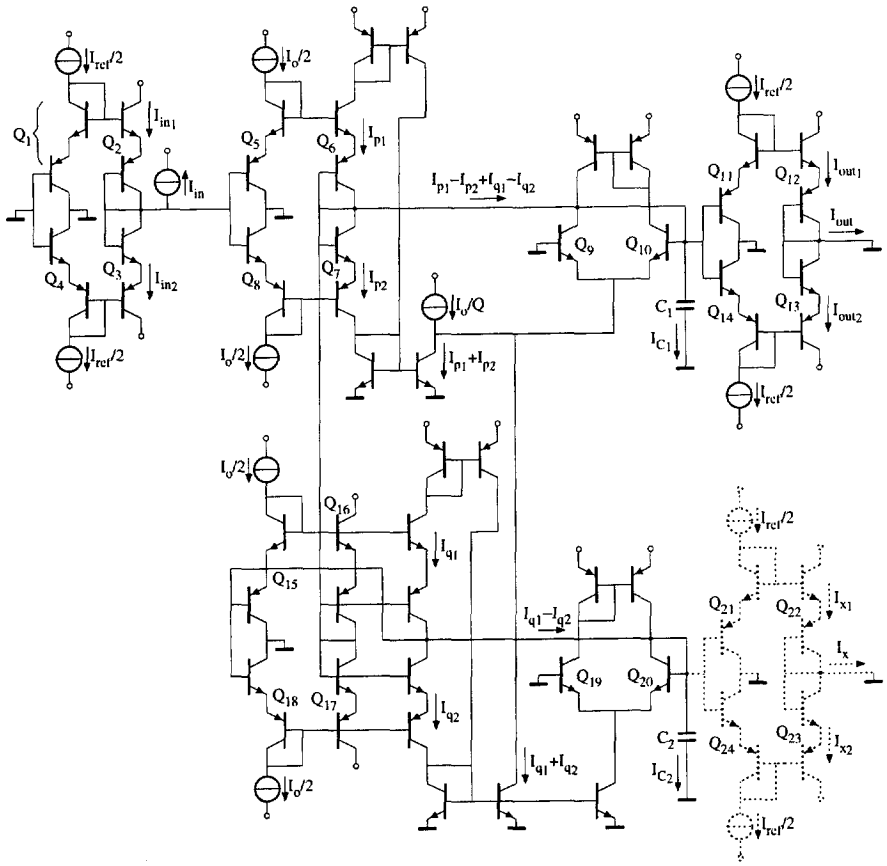

Figure 3.27: A sinh second-order band-pass filter [10].

five geometric mean TL loop equations are given by:

$$I_{\mathrm{in}_1} I_{\mathrm{in}_2} = 4I_{\mathrm{dc}}^2, \tag{3.74a}$$

$$I_{\mathrm{p}_1} I_{\mathrm{p}_2} = 4I_{\mathrm{o}}^2, \tag{3.74b}$$

$$I_{\mathrm{out}_1} I_{\mathrm{out}_2} = 4I_{\mathrm{dc}}^2, \tag{3.74c}$$

$$I_{\mathrm{q}_1} I_{\mathrm{q}_2} = 4I_{\mathrm{o}}^2, \tag{3.74d}$$

$$I_{x_1} I_{x_2} = 4I_{\mathrm{dc}}^2, \tag{3.74e}$$

where I_{dc} and I_{o} are dc currents.

These five loops and the differential pairs Q_9-Q_{10} and Q_{19}-Q_{20} are coupled by four other fundamental loops. The first loop comprises Q_1-Q_2-Q_5-Q_6-Q_{11}-Q_{12}. The second loop, Q_9-Q_{10}-Q_{11}-Q_{11}-Q_{12}-Q_{12}, is a little tricky as it contains both compound transistors, Q_{11} and Q_{12}, and single NPN transistors, Q_9 and Q_{10}. The slope of the exponential law differs by a factor of two for single and compound transistors. Consequently, in this context, the NPN and PNP transistors of Q_{11} and Q_{12} have to be treated as separate transistors, and therefore, their collector currents have to be included twice in the TL loop equation. The third loop, Q_{12}-Q_{11}-Q_{16}-Q_{15}-Q_{21}-Q_{22}, comprises only compound transistors. However, the fourth loop, Q_{19}-Q_{20}-Q_{21}-Q_{21}-Q_{22}-Q_{22}, is again a mixture of compound and single transistors. The four loop equations are respectively given by:

$$8I_{\mathrm{in}_1} I_{\mathrm{p}_1} I_{\mathrm{out}_1} = I_{\mathrm{o}} I_{\mathrm{dc}}^2, \tag{3.74f}$$

$$4I_9 I_{\mathrm{out}_1}^2 = I_{10} I_{\mathrm{dc}}^2, \tag{3.74g}$$

$$2I_{\mathrm{q}_1} I_{\mathrm{out}_1} = I_{\mathrm{o}} I_{x_1}, \tag{3.74h}$$

$$4I_{19} I_{x_1}^2 = I_{20} I_{\mathrm{dc}}^2, \tag{3.74i}$$

where I_9, I_{10}, I_{19} and I_{20} are given by:

$$I_{9,10} = \tfrac{1}{2}\left[I_{\mathrm{p}_1} + I_{\mathrm{p}_2} + I_{\mathrm{q}_1} + I_{\mathrm{q}_2} - \frac{I_{\mathrm{o}}}{Q} \pm (I_{\mathrm{p}_1} - I_{\mathrm{p}_2} + I_{\mathrm{q}_1} - I_{\mathrm{q}_2} - I_{C_1})\right],$$

$$I_{19,20} = \tfrac{1}{2}\left[I_{\mathrm{q}_1} + I_{\mathrm{q}_2} \pm (I_{C_2} - I_{\mathrm{q}_1} + I_{\mathrm{q}_2})\right].$$

The dynamic part of the filter transfer function is contained in the two expressions for the capacitance currents I_{C_1} and I_{C_2}. As indicated by eqns (3.69)–(3.72), several equivalent equations can be derived. Application of eqn (3.69), and $C_1 = C_2 = C$, yields:

$$I_{C_1} = 2CU_T \frac{\dot{I}_{\mathrm{out}_1}}{I_{\mathrm{out}_1}}, \tag{3.75a}$$

$$I_{C_2} = 2CU_T \frac{\dot{I}_{x_1}}{I_{x_1}}. \tag{3.75b}$$

To arrive at the state-space formulation of the filter transfer function, all variables except I_x, I_{out} and I_{in} have to be eliminated from the set of equations. To begin with, eqn (3.74h) yields an expression for I_{q_1} in terms of I_{x_1} and I_{out_1}. A similar expression can be found for I_{q_2} using eqns (3.74c), (3.74d) and (3.74e). Substitution of the expressions for $I_{\text{q}_{1,2}}$ and eqn (3.75b) in (3.74i) yields:

$$2CU_T\dot{I}_x = -I_{\text{o}}I_{\text{out}}. \tag{3.76a}$$

To obtain the second part of the state-space description, eqns (3.74f), (3.74a), (3.74b) and (3.74c) are used to obtain equations for I_{p_1} and I_{p_2} in terms of $I_{\text{in}_{1,2}}$ and $I_{\text{out}_{1,2}}$. The expressions for $I_{\text{p}_{1,2}}$ and $I_{\text{q}_{1,2}}$ along with eqn (3.75a) are substituted in (3.74g), which yields:

$$2CU_T\dot{I}_{\text{out}} = -\frac{I_{\text{o}}}{Q}I_{\text{out}} + I_{\text{o}}I_x - I_{\text{o}}I_{\text{in}}. \tag{3.76b}$$

The transfer function $H(s)$ of the sinh filter is easily derived from the state space description (3.76a) and (3.76b):

$$H(s) = \frac{-2sCU_TI_{\text{o}}}{4s^2C^2U_T^2 + 2sCU_T\frac{I_{\text{o}}}{Q} + I_{\text{o}}^2}. \tag{3.77}$$

This equation finally reveals that the filter shown in Fig. 3.27 implements a second-order band-pass transfer function.

4

Synthesis of translinear circuits

A structured design methodology for Static TransLinear (STL) circuits has been available for many years [50]. This chapter basically describes an extended version of this method, applicable to the design of both STL and Dynamic TransLinear (DTL) circuits [13,17,18,21,27,28,88]. The high level of similarity between STL and DTL circuits, which is evident from Chapter 3, is beneficially exploited. A major advantage resulting from this approach is that the existing theory and experience on STL circuits can be employed directly for the design of DTL circuits.

A general characteristic of synthesis methods is that they are divergent, and the method presented here is no exception. That is, many different circuit realisations, all implementing the desired electronic function, can result when following one and the same design trajectory, simply because many different design choices can be made during each stage of the synthesis procedure. The resulting realisations will all differ, more or less, with respect to properties like signal-to-noise ratio, dynamic range, bandwidth, minimum supply voltage, power consumption and sensitivity to component spread. These specifications are mainly determined by second-order effects, which are discussed in Chapters 5 and 6. Ideally, a structured synthesis method incorporates these effects in order to select the most favourable design choice at each stage of the design trajectory. However, at present only a limited amount of theory is available concerning this issue. Therefore, the aim of this chapter is to provide a *general* synthesis theory, based on ideal transistor models, encompassing *all* possible circuit solutions. The next step, the selection of the most suitable design choices, is mainly beyond the scope of this chapter. Further research in this direction

is required to obtain a completely structured theory on the synthesis of *high-performance* STL and DTL circuits.

For clarity, an overview of the current-mode synthesis method is given first, in Section 4.1, before the various design steps are treated in detail in Sections 4.2 through 4.5. In the literature, next to the method described in this chapter, several alternative synthesis methods for DTL circuits have been proposed. These are briefly reviewed in Section 4.6, and compared with the method presented in Sections 4.1 through 4.5. An issue closely related to synthesis is class-AB operation; this topic is discussed in Section 4.7.

4.1 Overview of the synthesis method

A considerable amount of theory on conventional, i.e., static, TransLinear (TL) circuits already exists in the open literature, ranging from a large number of circuit realisations to a complete formal analysis and synthesis theory [50]. Since DTL circuits are basically just a special kind of TL circuit, the aim of the synthesis method described in detail in Sections 4.2–4.5 is to unite the design of STL and DTL circuits in one all-encompassing theory. This way, the existing knowledge on STL circuits becomes directly applicable to DTL circuits, which obviously constitutes an important advantage.

A similar effort, but limited to the subclass of log-domain filters, is reported in [14], where Bernoulli's non-linear differential equation (DE) [95] is used as the basis of a current-mode synthesis method for DTL circuits. This method is briefly discussed in Section 4.6.3.

The design trajectory of both STL and DTL circuits is depicted in Fig. 4.1 and demonstrates the high level of similarity between these two classes of circuits.

The starting point of the synthesis method is an equation. Equations suitable for implementation by STL circuitry are polynomials $\mathcal{P}_m$, rational functions $\mathcal{P}_m/\mathcal{P}_n$ and n^{th}-order root ($\sqrt[n]{}$) functions. Transcendental equations can only be implemented after approximation by one of the former types of equations. For DTL circuits, the time derivative operator is added as a primitive function.

The function to be implemented can be described by a dimensionless equation. That is, all variables, parameters, and even time are represented by dimensionless quantities. This dimensionless equation first has to be transformed into an equation with the proper dimensions for a TL implementation to be possible. The possible transfer functions and the required signal transformations are discussed in Section 4.2.

After the appropriate signal transformations, the synthesis of STL circuits starts with a current-mode multivariable polynomial [50], representing the function to be implemented. The only difference between this polynomial and the current-mode DE, which is the starting point of DTL circuit design, is formed

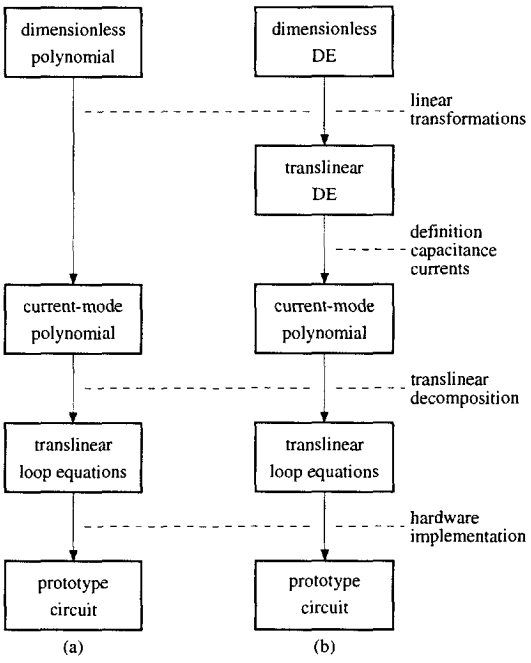

Figure 4.1: Synthesis path of (**a**) static and (**b**) dynamic translinear circuits.

by the time derivatives. To bridge this gap, all time derivatives are eliminated through the introduction of capacitance currents. This process is described in Section 4.3. From this point on, the design trajectory is largely identical for STL and DTL circuits, since both are now described by a current-mode multivariable polynomial.

The next synthesis step, treated in Section 4.4, is called 'translinear decomposition'. During this stage, the polynomial has to be rewritten as a difference between two products of collector currents. The resulting equation, given by (3.4), is called a 'translinear loop equation'.

Once a TL decomposition is found, it has to be projected onto a TL topology. Additionally, the circuit has to be biased, i.e., the required collector currents have to be enforced. The topic of hardware implementation is treated in Section 4.5. Once the prototype TL circuit is ready, the next design step, not shown in Fig. 4.1, is the analysis and elimination or reduction of second-order effects. This is the topic of Chapter 5.

4.2 Translinear transfer functions

The starting point of the design of a TL circuit is a dimensionless equation. Section 4.2.1 discusses the variety of functions suitable for implementation by STL circuits. Likewise, DTL circuit technology can be used to realise a variety of DEs, which is discussed in Section 4.2.2. Next to the types of functions, the dimensions of the signals have to allow for a TL implementation. As the starting point is a dimensionless equation, several dimension transformations are required to obtain a 'translinear equation'. A detailed treatment of the required transformations is given in Section 4.2.3.

4.2.1 Static transfer functions

Static translinear circuits can be used to realise a wide, yet limited, range of transfer functions. Not all types of equations can be integrated in a theoretically exact way by means of TL circuit technology. As TL circuits are described by products of current, the variety of transfer functions is restricted to algebraic equations.

More specifically, STL can be used to implement polynomials $\mathcal{P}_m$, rational functions $\mathcal{P}_m/\mathcal{P}_n$ and n^{th}-order roots ($\sqrt[n]{}$), each of which can have multiple inputs. Denoting the output signal by z and the inputs by x and y, some examples are respectively given by the squaring operation $z = x^2$, the divider $z = x/y$, and the geometric mean function $z = \sqrt{xy}$.

Approximations

Often the function to be realised is already given by an algebraic equation. Alternatively, a curve, a set of data points or a transcendental function can be specified, in which case the first step is to find an approximating algebraic function.

Several interpolation and approximation methods can be applied, and different accuracy criteria can be used. Often, simple methods, such as described in [50,96], suffice to find a suitable approximation. More sophisticated methods of approximation by polynomials and rational functions can be found in the literature, see, e.g., [97]. A treatment of the various approximation techniques is beyond the scope of this thesis.

Due to the non-idealities of the bipolar or weak inversion MOS transistor, which are treated in Chapter 5, the accuracy of TL circuits is limited, as a rule of thumb to 0.1 to 1%. Consequently, approximations usually do not have to be better than this.

Of primary importance is the simplicity of the approximating function. The coefficients in the approximating algebraic function must have a low number of significant digits, at most two, and preferably one.

Equally important, because of mismatch, is the sensitivity of the transfer function with respect to these coefficients. In this context, rational functions are known to perform better than polynomials. Unless a polynomial is a constant, it will always diverge rapidly outside the specified input signal range and it can be difficult to suppress this tendency within the interval [97]; this complies with a large sensitivity with respect to the coefficient values. Rational functions do not have this disadvantage.

Rational functions are also the better choice with respect to accuracy [97]. For a given degree of the numerator and denominator polynomials, $\mathcal{P}_m$ and $\mathcal{P}_n$, the total number of coefficients is larger than for a single polynomial function having the same degree as $\mathcal{P}_m$ or $\mathcal{P}_n$.

Multiple solutions

A general characteristic of polynomials and rational functions is that they can have several roots. Some roots may be physically impossible, but it is quite possible to have several physically correct roots. For example, before the square root function $z = \sqrt{x}$ can be implemented by a TL circuit, it has to be converted into a polynomial, i.e., $z^2 = x$. However, in squaring the original equation, information is lost. As a result, the new polynomial has two roots: $z = \pm\sqrt{x}$. To implement only the desired solution, the other root has to be made physically impossible by means of a suitable biasing arrangement.

Though only one solution can be correct at a certain point in time, it is possible to switch between different solutions. In principle, this method can be used to implement piece-wise linear or piece-wise polynomial functions [50, 98, 99]. For example, the absolute value function $z = |x|$ can be implemented this way. Squaring the equation results in a polynomial, $z^2 = x^2$. The two solutions of the polynomial are $z = \pm x$. A biasing arrangement has to be found such that $z = x$ for $x \geq 0$ and $z = -x$ for $x < 0$. A detailed treatment of biasing is given in Section 4.5.1.

Inverse realisations

A technique which can be used for the implementation of a strictly monotonous function is an inverse realisation. A TL circuit realising the inverse function is placed in the feedback path of a high-gain amplifier [98]. Alternatively, it is sometimes possible to exchange the input and output currents of a TL circuit [50]. An example of the former technique is the Wilson current mirror [100,101]. This circuit can be regarded as a simple two-transistor current mirror placed in the feedback path of an amplifier implemented by a single common-emitter (CE) stage.

Some care has to be taken when the inverse function F^{-1} is an approximation. Depending on the function and the accuracy measure used, the accuracy

of the approximation by F^{-1} can be very different from the accuracy of the resulting approximation by F.

4.2.2 Dynamic transfer functions

Polynomials, rational functions and n^{th}-order roots are the primitive functions of STL circuits. Adding the time derivative operator as a primitive function results in the class of DTL circuits. Thus, the DTL principle can be used to implement a wide variety of DEs, based on these primitive functions.

At present, most publications on DTL circuits are concerned with *linear* filters. However, application of the DTL principle is not limited to the implementation of linear filters, i.e., linear DEs. Using the STL principle it is possible to implement non-linear static transfer functions. Combining these non-linear static functions with the DTL principle, it is quite obvious that it is equally possible to realise *non-linear* DTL circuits, which are described by non-linear DEs.

In conventional designs, the dynamic and the non-linear part of a non-linear dynamic function are usually separated at system level, and the non-linear part is often implemented by STL circuits, see, e.g., [102, 103]. Using the DTL principle, it becomes possible to merge these functions into one functional block, see, e.g., [22–25], resulting in a high functional density.

Non-linear DTL circuits can be applied to perform non-linear filtering, such as phase-locked loops [26–28], adaptive filters [104], RMS-DC converters [22,23] and mixer-filter combinations [24,25], or for signal generation [19–21].

Linear filter transfer functions

For any filter implementation technique, the first design step is to obtain the filter transfer function. Depending on the application, the transfer function is usually determined by frequency-domain specifications, such as magnitude and phase response, or time-domain specifications, such as step and impulse response. The resulting transfer function is described by a linear DE, or equivalently, by a set of poles and zeros with a gain factor.

State-space descriptions

Another useful alternative for describing a filter transfer function is the state-space method. The original n^{th}-order DE is split up into n first-order DEs. The general state-space description of a linear filter is expressed by:

$$\dot{\vec{x}} = \mathbf{A}\vec{x} + \mathbf{B}\vec{u}, \tag{4.1a}$$

$$\vec{y} = \mathbf{C}\vec{x} + \mathbf{D}\vec{u}, \tag{4.1b}$$

where $\vec{x} = (x_1, \ldots, x_n)^T$ is the state vector, $\vec{u}$ and $\vec{y}$ are the input and output vectors, respectively, and $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$ and $\mathbf{D}$ are matrices.

The state-space description is often represented graphically by means of a signal-flow graph, which is completely equivalent.

Non-linear dynamic functions

Like linear filters, non-linear dynamic functions can be described by an n^{th}-order DE or by a set of n first-order DEs, the state-space description, which is in general given by:

$$\dot{\vec{x}} = \vec{F}(\vec{x}, \vec{u}), \tag{4.2a}$$

$$\vec{y} = \vec{G}(\vec{x}, \vec{u}), \tag{4.2b}$$

where $\vec{F}$ and $\vec{G}$ are, in general, non-linear vector functions of the states and the input signals.

4.2.3 Dimension transformations

In most cases, synthesis of a static or dynamic (transfer) function starts with a dimensionless equation. That is, all signals and parameters, and even the time variable in a DE, are dimensionless. However, as soon as the mathematical domain is left and an electronic implementation has to be found, quantities are bound to certain dimensions. These dimensions are dictated by the particular circuit technique employed. In order to find a TL implementation of a certain equation, transformations have to be applied to the dimensionless equation to arrive at an equation with the dimensions characteristic for the TL circuit technique.

A number of fundamental characteristics of TL networks are related to the required transformations, which are therefore treated explicitly in this section.

Time transformation

A static transfer function, characteristic for STL circuits, comprises only signals and parameters. In addition, the time variable τ is present in the dimensionless DE describing a DTL circuit. As the DE will be autonomous in most cases, τ will only be present implicitly through the derivative operator.

The dimensionless time variable τ has to be transformed into the time variable t with its usual dimension of seconds [s]. An important aspect of the time transformation is that some factors $(CU_T)^k$, where $k \in \mathbb{N}$, have to be introduced. Section 3.2 shows that these factors are always present in the DE describing a DTL circuit. Every term $(CU_T)^k$ in the DE is accompanied by a derivative operator $\mathrm{d}^k/\mathrm{d}t^k$, i.e., the power k of the factor CU_T equals the order of the

derivative, and the highest power of the term CU_T is equal to the degree n of the DE. Therefore, $k \in [1, \ldots, n]$. This indicates that the terms CU_T have to be brought into the properly dimensioned DE through the time transformation.

The dimension of the term CU_T being the coulomb [C], division by a dc current I_{o_1} results in a fraction CU_T/I_{o_1} having the required dimension [s]. Consequently, for DTL circuits a suitable time transformation from τ to t is given by the equivalence relation:

$$\frac{\mathrm{d}}{\mathrm{d}\tau} = \frac{CU_T}{I_{o_1}} \frac{\mathrm{d}}{\mathrm{d}t}. \tag{4.3}$$

Note that neither side of eqn (4.3) has dimension.

Several fundamental characteristics of DTL circuits can be derived from eqn (4.3). First of all, eqn (4.3) shows that time t is inversely proportional to I_{o_1}. This explains the excellent linear frequency tuning capabilities of TL filters. It is interesting to note that 'bipolar g_mC' filters, for which the transconductance g_m is implemented by bipolar transistors only, have identical tuning characteristics. In fact, these bipolar g_mC filters are characterised by the same time transformation.

Secondly, the frequency behaviour of a TL filter depends on the absolute temperature through U_T. However, eqn (4.3) shows that this temperature dependency can be cancelled by making I_{o_1} PTAT[1] [1].

Finally, though the variable I_{o_1} has the dimension [A], it does not necessarily have to be a physical current. It is possible to replace I_{o_1} by a more complex expression with the same dimension [A]. For example, in [105], $I_{o_1} = I_o I_y / I_x$.

Signal transformation

Translinear circuits are typical examples of current-mode signal processing. In both STL and DTL circuits, information is carried by currents, whereas voltages are only of secondary interest. This implies that all time-varying signals in the dimensionless equation have to be transformed into currents. This is again accomplished by introducing an equivalence relation. A dimensionless signal x is transformed into a signal current I_x through the equation:

$$x = \frac{I_x}{I_{o_2}}, \tag{4.4}$$

where I_{o_2} is a dc current. Again, note that neither side of eqn (4.4) has dimension.

In eqns (4.3) and (4.4), two different currents, I_{o_1} and I_{o_2}, are introduced as both transformations are independent. The dc currents I_{o_1} and I_{o_2} determine the absolute current levels of the DTL circuit to be realised. In principle, it is

[1] Proportional-To-Absolute-Temperature

possible to choose $I_{o_1} = I_{o_2}$. A disadvantage of this choice is the resulting dependence of the absolute signal swings on current I_{o_1} controlling the frequency characteristics. On the other hand, second-order effects, e.g., finite base currents, are more difficult to manage when large magnitude differences in current levels occur in a TL network. Further, it is often possible to restore the signal levels using a variable gain amplifier with a gain that is proportional to I_{o_2}/I_{o_1} [21].

Parameter transformation

Closely linked to the transformations is electronic controllability. In many situations, the equation to be realised contains some parameters that influence its behaviour. Next to the filter cut-off frequency already encountered, some interesting examples are the gain of an amplifier [44], the Q of a filter [5], the amplitude of a harmonic oscillation [21] or a bifurcation parameter in a chaotic DE.

A parameter in a dimensionless equation can either be transformed into a current, using eqn (4.4), or remain dimensionless. In the first case, the parameter becomes a signal and therefore will be tunable. Note that every interesting parameter can be made (linearly) current controlled this way. In the latter case, the parameter ends up as an area scale factor and will be fixed. Hence, during the transformation synthesis step the need for the controllability of certain parameters has to be considered.

Design example: A third-order elliptic low-pass filter

To illustrate the synthesis procedure proposed in this chapter, we consider the design of a third-order elliptic low-pass filter. A customary method in analogue filter design is to derive the transfer function and state-space description from a passive LC ladder filter. For this synthesis example, consider the third-order elliptic low-pass filter depicted in Fig. 4.2 [106]. All circuit elements are normalised. The cut-off frequency is one. The values of the (normalised) capacitances and inductance are: $c_1 = c_3 = 1.6876$, $l_2 = 0.5882$ and $c_2 = 0.8508$. Due to the presence of c_2, the filter possesses a transmission zero at a frequency of 1.4137. The pass-band ripple is 1.25 dB. The minimum attenuation is 20.41 dB and is first attained at a frequency of 1.2868.

Three state variables have to be chosen in order to derive a state-space description of the LC filter. Suitable state variables are the (normalised) capacitance voltages x_1 across c_1 and x_3 across c_3, and the inductance current x_2 flowing through l_2. The output signal y equals $2x_3$, where the factor two compensates for the loss due to the unity resistances.

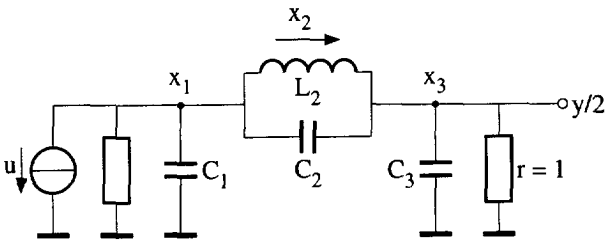

Figure 4.2: Prototype third-order elliptic *LC* filter.

Next, a state-space description is found by solving the system of two nodal equations and one mesh equation for the derivatives $\dot{x}_1$, $\dot{x}_2$ and $\dot{x}_3$. This yields:

$$\dot{x}_1 = -\frac{c_1\,(u + x_1 + x_2) + c_2\,(u + x_1 + x_3)}{c_1\,(c_1 + 2c_2)}, \tag{4.5a}$$

$$\dot{x}_2 = \frac{x_1 - x_3}{l_2}, \tag{4.5b}$$

$$\dot{x}_3 = \frac{c_1\,(x_2 - x_3) - c_2\,(u + x_1 + x_3)}{c_1\,(c_1 + 2c_2)}, \tag{4.5c}$$

where u is the input signal.

It is convenient to scale x_2 by a factor $(c_1 + c_2)/c_1$. This results in more coefficients of the **A**-matrix being equal, which, in turn, yields a simpler circuit implementation.

The state-space description comprises normalised signals. Application of eqn (4.4) transforms x_1, x_2, x_3, u and y into the currents I_{x_1}, I_{x_2}, I_{x_3}, I_{in} and I_{out}. It is interesting to note that the normalisation current I_{o_2} can be eliminated completely. Due to the fact that the filter is linear, each additive term in the state-space description contains only one of the signals x_1, x_2, x_3, u or y. Hence, in the transformed state-space description, I_{o_2} occurs exactly once in each additive term and can therefore be eliminated. Application of eqn (4.3), with $I_{\text{o}_1} = I_{\text{o}}$, finally yields a properly dimensioned state-space description:

$$2.25\; CU_T \dot{I}_{x_1} = -I_{\text{o}}\,(I_{x_1} + I_{x_2} + 0.335\; I_{x_3} + I_{\text{in}})\,, \tag{4.6a}$$

$$0.885\; CU_T \dot{I}_{x_2} = \;\; I_{\text{o}}\,(I_{x_1} - I_{x_3})\,, \tag{4.6b}$$

$$2.25\; CU_T \dot{I}_{x_3} = -I_{\text{o}}\,(0.335\; I_{x_1} - I_{x_2} + I_{x_3} + 0.335\; I_{\text{in}})\,, \tag{4.6c}$$

where the numerical values of c_1, c_2, c_3 and l_2 have been substituted; only three significant digits are shown. The example is continued on page 88.

4.3 Definition of capacitance currents

Capacitance currents are the key to DTL circuits. From a current-mode point of view, they bridge the gap between STL and DTL circuits. Whereas STL transfer functions are described by multivariable polynomials, in which the variables are formed by the input and output currents, DTL functions are described by DEs, containing not only currents, but also time derivatives of currents, as well as some terms CU_T. Obviously, the theory presented in this section is exclusively related to DTL circuits. Static translinear designs directly continue with the next step, TL decomposition, described in Section 4.4.

The DTL principle, explained in Section 2.2.2, states that a time derivative of a current can be implemented by means of a capacitance current. As illustrated in Fig. 4.1(b), through the introduction of capacitance currents, all derivatives can be eliminated from the DE, as well as the terms CU_T, resulting in a current-mode multivariable polynomial. The variables in this polynomial are the input, output, and capacitance currents. As both STL and DTL circuits are now described by a polynomial, from this point on the subsequent synthesis steps, starting with TL decomposition, are roughly the same for STL and DTL networks.

The capacitance currents are introduced by appropriately defining them. Section 4.3.1 gives a general model for a TL capacitance current, based on a state-space approach, and describes its properties. Obviously, valid capacitance current definitions have to satisfy these properties. The various classes of capacitance current definitions are treated in Sections 4.3.2, 4.3.3 and 4.3.4. These sections display an increasing degree of complexity in the capacitance current definitions. Basically, Section 4.3.2 is concerned with log-domain filters, Section 4.3.3 with definitions for TL filter classes like tanh and sinh filters, and Section 4.3.4 with the most general form of capacitance current definitions.

4.3.1 State-space approach

State-space methods form a very powerful and efficient approach in the synthesis of both conventional filters and TL filters [3]. In particular, for DTL circuits, capacitance current definitions can be derived from the states, which are represented by the vector of state currents $\vec{I}_x = (I_{x_1}, \ldots, I_{x_n})^T$.

The general state-space description of a linear single-output TL filter, obtained by applying transformations (4.3) and (4.4) to (4.1), is given by:

$$CU_T \dot{\vec{I}}_x = \mathbf{A}\vec{I}_x + \mathbf{B}\vec{I}_u, \tag{4.7a}$$

$$I_{\text{out}} = \mathbf{C}\vec{I}_x + \mathbf{D}\vec{I}_u, \tag{4.7b}$$

where $\dot{\vec{I}}_x = (\dot{I}_{x_1}, \ldots, \dot{I}_{x_n})^T$, $\vec{I}_u$ is the vector of input currents, I_{out} the output current, and $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$ and $\mathbf{D}$ are matrices. Note that the dimension of the

coefficients comprising **A** and **B** is now [A], whereas the coefficients of **C** and **D** are dimensionless.

The n first-order DEs have to be converted into n 'state-space polynomials'. Through application of the DTL principle, the n derivatives $CU_T\dot{\vec{I}}_x$, shown on the Left-Hand Side (LHS) of eqn (4.7a), have to be replaced by products of currents. To this end, n capacitance currents,[2] denoted by the vector $\vec{I}_{\rm cap} = [I_{C_1}, \ldots, I_{C_n}]^T$, have to be defined. As the capacitance currents are used to eliminate $\dot{\vec{I}}_x$, in the definition of $\vec{I}_{\rm cap}$ the derivatives present in the state-space description have to be used. Consequently, $\vec{I}_{\rm cap}$ is a vector function of the states and the first-order time derivatives of the states,[3] that is (compare with eqns (2.7) and (3.24)):

$$\vec{I}_{\rm cap} = \vec{I}_{\rm cap}\left(\vec{I}_x, \dot{\vec{I}}_x\right). \tag{4.8}$$

To eliminate $\dot{\vec{I}}_x$ from eqn (4.7a), (4.8) has to be solved to yield expressions for $\dot{\vec{I}}_x = \dot{\vec{I}}_x(\vec{I}_{\rm cap}, \vec{I}_x)$. Substitution of the resulting expressions in eqn (4.7a) yields a set of state-space polynomials.

Characteristics of the capacitance currents

In a TL filter, a capacitance always forms a closed loop with one or more base-emitter junctions, as illustrated in Fig. 3.6. Equation (3.24) gives the general expression for a TL capacitance current. It has two important characteristics. First, all denominators on the Right-Hand Side (RHS) are collector currents. This implies that these currents have to be strictly positive. Secondly, the numerators on the RHS are the time derivatives of the corresponding denominators. With these two characteristics in mind, eqn (3.24) can be used to define the capacitance currents.

Analogy with conventional filters

It is interesting to make a comparison between TL and conventional filters regarding the introduction of the memory elements. In conventional filters, equations for the capacitance currents and inductance voltages are used to implement the derivatives present in the state-space description. The only difference with respect to TL filters is that the capacitance currents and inductance voltages

[2] In principle, more than n capacitances can be used to implement an $n^{\rm th}$-order filter. However, this option requires more chip area than absolutely necessary and is therefore not explicitly considered here.

[3] The treatment given here is limited to instantaneous companding TL filters. In syllabic companding TL filters, see Section A.1, the gain control signals represent additional states, which have to be included at the RHS of eqn (4.8).

are now *linear* functions of the time derivatives of the states. As a consequence, elimination of the derivatives from the state-space description yields linear expressions. These KCL and KVL equations can be implemented directly by connecting linear circuit elements, possibly with the aid of some amplifiers.

State-space transformations

State-space descriptions are not unique. One single DE can be represented by infinitely many different, yet equivalent, state-space descriptions. From a given state-space description, alternative descriptions are obtained through the application of state-space transformations. In general, both linear and non-linear transformations can be used, which are represented by:

$$\vec{I}_y = \vec{I}_y\left(\vec{I}_x\right), \tag{4.9}$$

where $\vec{I}_y$ is the new state vector. This vector function can be used to rewrite eqns (4.7a) and (4.7b) in terms of $\vec{I}_y$ and $\dot{\vec{I}}_y$. An important condition is that the Jacobian of the vector function $\vec{I}_y$ is non-singular at all times.

Through the application of state-space transformations, it is possible to write each capacitance current as a function of only one state current and its first-order derivative, i.e.:

$$I_{C_k} = I_{C_k}\left(I_{y_k}, \dot{I}_{y_k}\right), \qquad k \in [1, \ldots, n]. \tag{4.10}$$

In particular, it is possible to make each capacitance current dependent on one single collector current I_{y_k}. In other words, all possible capacitance current definitions can be mapped onto the log-domain output structure. This is illustrated symbolically in Fig. 4.3. As the log-domain output structure is the most simple one, it is convenient to refer all possible capacitance current definitions to this structure. Hence, in general, the n capacitance currents can be expressed by:

$$I_{C_k} = C_k U_T \frac{\dot{I}_{y_k}}{I_{y_k}}, \qquad k \in [1, \ldots, n]. \tag{4.11}$$

Note that the capacitance value C_k denotes an additional degree of freedom in the definition.

An important consequence of this approach is that the state-space description in terms of $\vec{I}_y$ is to a certain extent related directly to a circuit topology. Likewise, this approach is used habitually in the design process of conventional filters, see, e.g., [80, 107]. Its advantages are that it enhances the designability and, even more importantly, the sensitivity and dynamic range properties of the particular state-space description are transferred, to a certain extent, to the final filter realisation.

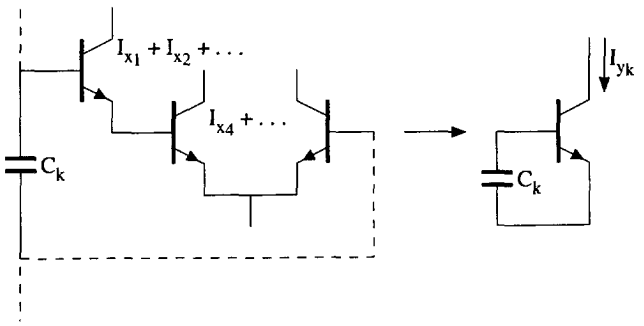

Figure 4.3: Using (non-linear) state-space transformations, all possible capacitance current definitions can be mapped onto the log-domain output structure.

4.3.2 Linear transformations

Linear transformations form an important class of state-space transformations. The new state vector $\vec{I}_y$ is now a linear function of the previous state vector $\vec{I}_x$:

$$\vec{I}_y = \mathbf{T}^{-1}\vec{I}_x, \tag{4.12}$$

where $\mathbf{T}$ is a non-singular matrix. The well-known process of scaling the state variables complies with a matrix $\mathbf{T}$ having only non-zero coefficients at its diagonal.

The state-space description, eqns (4.7a) and (4.7b), can be rewritten as:

$$CU_T\dot{\vec{I}}_y = \mathbf{A}'\vec{I}_y + \mathbf{B}'\vec{I}_u, \tag{4.13a}$$

$$I_{\text{out}} = \mathbf{C}'\vec{I}_y + \mathbf{D}\vec{I}_u, \tag{4.13b}$$

where

$$\mathbf{A}' = \mathbf{T}^{-1}\mathbf{A}\mathbf{T},$$
$$\mathbf{B}' = \mathbf{T}^{-1}\mathbf{B},$$
$$\mathbf{C}' = \mathbf{C}\mathbf{T}.$$

Referring to the log-domain output structure, shown in Fig. 3.14, the capacitance currents are now described by eqn (4.11).

Strictly positive state currents

The state currents $\vec{I}_y$ have to be strictly positive for eqn (4.11) to be a valid capacitance current definition. Assuming class-A operation, this implies that

appropriate dc bias currents have to be introduced. This can be accomplished easily. In this thesis, dc bias currents are considered to be a special type of input current to the circuit. Therefore, next to the actual input current I_{in}, the vector $\vec{I_u}$ contains the dc current I_{dc}. That is:

$$\vec{I_u} = \begin{bmatrix} I_{\text{in}} \\ I_{\text{dc}} \end{bmatrix}. \tag{4.14}$$

Now, choosing appropriate values for the coefficients in the second column of $\mathbf{B}'$ in eqn (4.13a) results in strictly positive currents $\vec{I_y}$ for a given input signal range of I_{in}.

A different but equivalent method is to use $\vec{I_u} = [I_{\text{in}}]$ and to include the dc bias currents I_{dc_k} in the capacitance current definitions:

$$I_{C_k} = C_k U_T \frac{\dot{I}_{y_k}}{I_{\text{dc}_k} + I_{y_k}}. \tag{4.15}$$

This approach can be more suitable when non-linear DEs have to be realised.

Sensitivity

Different state-space descriptions can represent one and the same transfer function, and therefore, there seems to be no particular reason to favour one description. However, in electronic filter design, it is customary to use a one-to-one mapping of the state-space description onto a certain filter topology. This approach enhances the designability, especially for higher-order filters.

Using this approach, the coefficients in the matrices $\mathbf{A}$, $\mathbf{B}$ and $\mathbf{C}$ are mapped directly onto component values in the final filter circuit. As a consequence, the sensitivity properties of the filter transfer function with respect to small deviations of the matrix coefficients are retained in the sensitivities with respect to mismatches of the component values. Hence, an electronic filter implementation preferably originates from a state-space description with low sensitivity characteristics. Note that the sensitivity properties are not always completely retained, but practice shows that the sensitivities to the component values are generally low [80, 81, 107]. Further, it is likely that the sensitivity optimum is close to the DR optimal network [80].

Another important aspect of state-space realisations is the sparsity of the matrix $\mathbf{A}$. Eventually, the coefficients are implemented by connections in the circuit. A matrix $\mathbf{A}$ without zero entries implies a fully-connected circuit, which is undesirable as it results in a structure too large and difficult to implement on a chip [80]. Therefore a sparse matrix is often preferable.

Simulation of *LC* ladder filters

An often used method is to derive the state-space description from a doubly terminated *LC* ladder filter. Figure 4.2 shows an example of an *LC* ladder filter. It is well-known that at the so-called attenuation zeros the first-order sensitivity of the transfer function of these filters to their component values is zero [108]. Choosing the inductance currents and capacitance voltages to represent the state of the filter, a state-space description with low sensitivity properties is obtained. Active simulation of this state-space description yields a low sensitivity filter implementation. In addition, the **A**-matrix is quite sparse as it is tri-diagonal. For these reasons, *LC* ladder filters have been used as prototypes in the design of many TL filter circuits [12, 89, 109].

Design example: A third-order elliptic low-pass filter

To illustrate the introduction of capacitance currents, we continue the design example from page 81. Equations (4.6a)–(4.6c), describing the third-order elliptic filter, have to be transformed into polynomials by defining three capacitance currents I_{C_1}, I_{C_2} and I_{C_3}. Different types of capacitance current expressions can be used to define I_{C_1} through I_{C_3}, corresponding to different TL filter classes, as explained in Section 3.3. The final network is at its most simple if a log-domain filter is designed. In practice, log-domain filters are probably the most relevant category of TL filters, and most TL filters described in the literature are in fact log-domain filters. For these reasons, we choose to implement the elliptic filter by a log-domain circuit.

Since the *LC* filter has a low-pass characteristic, the state currents I_{x_1}, I_{x_2} and I_{x_3} acquire a dc component when a dc current $-I_{\mathrm{dc}}$ is added to I_{in}. These dc components $I_{x_1}|_{\mathrm{dc}}$, $I_{x_2}|_{\mathrm{dc}}$ and $I_{x_3}|_{\mathrm{dc}}$ are given by:

$$I_{x_1}|_{\mathrm{dc}} = I_{x_3}|_{\mathrm{dc}} = \frac{I_{\mathrm{dc}}}{2}, \qquad I_{x_2}|_{\mathrm{dc}} = \frac{c_1 I_{\mathrm{dc}}}{2\,(c_1 + c_2)}. \tag{4.16}$$

The state currents being strictly positive, eqn (4.11) can be used directly to define I_{C_1}–I_{C_3}. Suitable definitions are:

$$I_{C_1} = 2.25\, CU_T \frac{\dot{I}_{x_1}}{I_{x_1}}, \tag{4.17a}$$

$$I_{C_2} = 0.885\, CU_T \frac{\dot{I}_{x_2}}{I_{x_2}}, \tag{4.17b}$$

$$I_{C_3} = 2.25\, CU_T \frac{\dot{I}_{x_3}}{I_{x_3}}. \tag{4.17c}$$

The capacitance currents implement the derivatives $\dot{I}_{x_1}$, $\dot{I}_{x_2}$ and $\dot{I}_{x_3}$. Substitution of eqns (4.17) in (4.6) yields a set of three TL polynomials:

$$(I_o + I_{C_1})\, I_{x_1} = -I_o \left(I_{x_2} + \tfrac{1}{3} I_{x_3} + I_{in}\right), \tag{4.18a}$$

$$I_{C_2} I_{x_2} = \; I_o \left(I_{x_1} - I_{x_3}\right), \tag{4.18b}$$

$$(I_o + I_{C_3})\, I_{x_3} = -I_o \left(\tfrac{1}{3} I_{x_1} - I_{x_2} + \tfrac{1}{3} I_{in}\right), \tag{4.18c}$$

where 0.335 has been approximated by $\frac{1}{3}$. Equations (4.18a) and (4.18c) demonstrate that the linear loss, due to the termination resistances shown in Fig. 4.2, can be implemented by a current I_o in parallel with capacitances C_1 and C_3.

The next synthesis step, translinear function decomposition, is described on page 106.

4.3.3 Single-state non-linear transformations

Next to the log-domain output structure, more complex output structures can be used to define the capacitance currents. Examples are the tanh and sinh output stages shown in Figs 3.19 and 3.23. With respect to the log-domain output structure, these choices comply with non-linear state-space transformations, described by:

$$I_{y_k} = I_{y_k}(I_{x_k}). \tag{4.19}$$

Note that in comparison with eqn (4.9), (4.19) does not represent the most general class of non-linear state-space transformations. Hence, the class of exponential state-space filters introduced in [4] can be generalised even further, as discussed in Section 4.3.4.

In principle, eqn (4.19) can be used to rewrite the state-space description terms of $\vec{I}_y$. However, in practice, this does not seem to be very useful as the resulting set of equations is further away from the eventual implementation. In practice, it is more likely that a new DTL output structure is derived in the first instance from a transistor structure than from the corresponding mathematical transformation.

Finally, it is interesting to note that the non-linear state-space transformations do not have an analogy for conventional filter implementations. In the latter class of filters, non-linear components are not available to implement the non-linear equations, which renders non-linear transformations useless.

Example: Non-linear transformation for tanh filters

To illustrate the non-linear state-space transformation resulting from a non-log-domain output structure, consider the application of a tanh output structure to

implement the derivative $\dot{I}_{\text{out}}$ in the integrator equation (3.36). The tanh sub-circuit can be mapped onto the log-domain structure having a collector current I_y defined by:

$$I_y = I_0 \frac{I_{\text{dc}} + I_{\text{out}}}{I_{\text{dc}} - I_{\text{out}}}. \tag{4.20}$$

Note that I_y is strictly positive for $|I_{\text{out}}| < I_{\text{dc}}$. Thus, eqn (3.36) can be rewritten as:

$$CU_T \dot{I}_y = \frac{I_{\text{in}} (I_0 + I_y)^2}{2I_{\text{dc}}}. \tag{4.21}$$

Clearly, the RHS of eqn (4.21) is non-linear.

4.3.4 General non-linear transformations

The non-linear transformations treated in Section 4.3.3 are characterised by the fact that each new state variable I_{y_k} is a function of exactly *one* previous state variable I_{x_k}, see eqn (4.19). However, eqn (4.9) shows that in general each new state variable can depend on *all* previous state variables. This is true for the linear transformations treated in Section 4.3.2, but it is equally valid for non-linear state-space transformations. These 'generalised' non-linear state-space transformations result in a class of TL filters more general than the class proposed in [4, 10].

As an example, for a second-order circuit characterised by the states I_{x_1} and I_{x_2}, two possible capacitance current definitions, denoted by I_{C_1} and I_{C_2}, are given by:

$$I_{C_1} = CU_T \left(\frac{\dot{I}_{x_1}}{I_{x_1}} - \frac{\dot{I}_{x_2}}{I_{x_2}} \right), \tag{4.22a}$$

$$I_{C_2} = CU_T \left(\frac{\dot{I}_{x_1}}{I_{x_1}} + \frac{\dot{I}_{x_2}}{I_{x_2}} \right). \tag{4.22b}$$

A condition for these definitions to be valid is that I_{x_1} and I_{x_2} are strictly positive, which can be assured using the methods described in Section 4.3.2. Figure 4.4 shows possible implementations of eqns (4.22a) and (4.22b).

With respect to the log-domain output structure, eqns (4.22a) and (4.22b) comply with non-linear state-space transformations. The transformed state-space is represented by the states I_{y_1} and I_{y_2}, given by:

$$I_{y_1} = I_0 \frac{I_{x_1}}{I_{x_2}}, \tag{4.23a}$$

$$I_{y_2} = \frac{I_{x_1} I_{x_2}}{I_0}, \tag{4.23b}$$

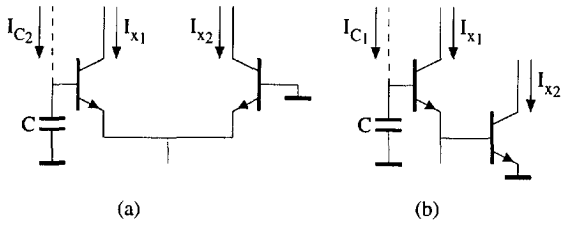

Figure 4.4: Two capacitance current definitions based on general non-linear state-space transformations.

where I_o is a dc bias current.

It is interesting to note that the *non-linear* transformations (4.23a) and (4.23b), in the *linear* domain of the state currents, are equivalent to *linear* transformations in the *non-linear* domain of the capacitance currents. Suppose the capacitance currents I'_{C_1} and I'_{C_2} are defined by eqn (4.11), i.e., based on the log-domain output stage:

$$I'_{C_1} = CU_T \frac{\dot{I}_{x_1}}{I_{x_1}}, \tag{4.24a}$$

$$I'_{C_2} = CU_T \frac{\dot{I}_{x_2}}{I_{x_2}}. \tag{4.24b}$$

Then, eqns (4.22a) and (4.22b) can be written as linear combinations of these currents:

$$I_{C_1} = I'_{C_1} - I'_{C_2}, \tag{4.25a}$$

$$I_{C_2} = I'_{C_1} + I'_{C_2}. \tag{4.25b}$$

A design example of a second-order TL filter based on eqns (4.22a) and (4.22b) is described in Section A.3.

4.4 Translinear function decomposition

For the STL design trajectory, shown in Fig. 4.1(a), the application of signal transformations has resulted in a current-mode multivariable polynomial. Similarly, for the DTL design trajectory, shown in Fig. 4.1(b), the introduction of capacitance currents has 'transformed' the DE into a current-mode multivariable polynomial. Consequently, the remaining part of the synthesis method is now basically identical for both STL and DTL circuits.

The next synthesis step to be performed is called 'translinear decomposition'. That is, the polynomial has to be mapped onto a TL loop equation, described by

eqn (3.4). This step is fundamentally non-linear, and therefore not the easiest part of the design trajectory.

Translinear decompositions can be divided into two main groups: non-parametric and parametric TL decompositions. In the former group, a polynomial is mapped onto a single TL loop equation. Non-parametric decompositions are discussed in Section 4.4.1 and an algorithm for the automatic generation of non-parametric decompositions is given in Section 4.4.2.

In the case of a parametric decomposition, the polynomial is mapped onto a set of two or more TL loop equations. This class of TL decompositions is dealt with in Section 4.4.3. An algorithm for the automatic generation of parametric decompositions unfortunately does not yet exist.

4.4.1 Non-parametric decomposition

Each STL or DTL circuit can be described by a current-mode multivariable polynomial. The variables comprising this polynomial are the input currents, the output current and, for DTL circuits only, the capacitance currents. A polynomial describing a TL circuit has a homogeneous degree r, i.e. the dimension of all the terms of the equation is $[\mathrm{A}^r]$, and is given by [110]:

$$\mathcal{P}_r(I_{x_1},\ldots,I_{x_n}) = \sum_{j_1+\cdots+j_n=r} a_{j_1,\ldots,j_n} I_{x_1}^{j_1}\ldots I_{x_n}^{j_n} = 0, \tag{4.26}$$

where I_{x_j}, $j \in [1,\ldots,n]$, are the n variables and $a_{j_1,\ldots,j_n}$ are the coefficients.

Translinear loop equation

In order to implement a multivariable polynomial by a TL circuit, a valid TL decomposition has to be found first. That is, the polynomial has to be rewritten as a single TL loop equation (*non-parametric* decomposition) or as a set of TL loop equations (*parametric* decomposition). For non-parametric decompositions, the TL loop equation is generally described by:

$$\begin{aligned}(c_{1,1}I_{x_1}+\cdots+c_{1,n}I_{x_n})\ldots(c_{2r'-1,1}I_{x_1}+\cdots+c_{2r'-1,n}I_{x_n})\\ -(c_{2,1}I_{x_1}+\cdots+c_{2,n}I_{x_n})\ldots(c_{2r',1}I_{x_1}+\cdots+c_{2r',n}I_{x_n})=0,\end{aligned} \tag{4.27}$$

where $c_{i,j}$, $i \in [1,\ldots,r']$, $j \in [1,\ldots,n]$, are the coefficients, and r' is the degree of the TL loop equation.

As an example of a non-parametric decomposition, consider the current squaring function (3.12). To implement this equation, a suitable TL decomposition has to be derived. A possible non-parametric decomposition is given by eqn (3.11).

The TL loop equation (4.27) does not have to be exactly identical to the polynomial (4.26). The crucial point is that the functionality of the polynomial

is retained in the TL loop equation. For example, multiplying eqn (4.26) by a number $\lambda(\neq 0)$ does not alter the functionality.

Although in most practical situations, the degree r' of the TL loop equation (4.27) is identical to the degree r of the polynomial (4.26), this is not a general characteristic of (4.27). It is possible to multiply (4.26) by a current-mode polynomial $\mathcal{P}_{r'-r}$ of homogeneous degree $r' - r > 0$ before the actual TL decomposition is performed. As long as $\mathcal{P}_{r'-r} = 0$ does not introduce any new physical solutions, the behaviour of the previous polynomial is exactly retained. An example is found in Section 8.1.3, where the current mirror function $I_{\text{in}} = I_{\text{out}}$ is implemented by $I_{\text{dc}} I_{\text{in}} = I_{\text{dc}} I_{\text{out}}$. A TL decomposition of the latter equation is given by eqn (8.3).

Positive collector currents

The linear terms between brackets in eqn (4.27) represent the collector currents of the transistors comprising the TL loop. Consequently, these factors have to remain strictly positive under all operating conditions. It is an important part of the TL decomposition process to guarantee this.

The factors in eqn (4.27) are linear combinations of the input, output and capacitance currents. As the function to be implemented and the input signal range are assumed to be known, it is straightforward to check whether a linear combination of input, output and capacitance currents is strictly positive. This is easiest for STL circuits, where the output current is determined only by the instantaneous value of the input currents. Therefore, it is sufficient to specify only the ranges of the input currents.

For DTL circuits, the situation is more complicated due to the frequency-dependency of the dynamic (transfer) function. Not only the instantaneous value of the input signals, but also the derivatives of the input signals come into play as they determine the capacitance currents. Therefore, the wave form and frequency range have to be specified as well.

To calculate the output current, the DE has to be solved. This is simple for filters, which are described by linear DEs. However, non-linear DEs will often require a numerical approach as there is no general method for solving a non-linear DE analytically.

The odds for finding a decomposition

For TL decomposition, an important question is whether a non-parametric decomposition can always be found for any polynomial with an arbitrary degree r and an arbitrary number of independent variables. The answer follows from a comparison of the degrees of freedom, i.e. the number of coefficients, available in the polynomial to be implemented and the TL loop equation onto which the polynomial is to be mapped.

An r^{th}-order TL loop contains $2r$ collector currents, each comprising a linear combination of v input, output and capacitance currents. Consequently, the number of coefficients in a TL loop equation, denoted by F_{TL}, is given by:

$$F_{TL} = 2rv. \tag{4.28}$$

For a general polynomial of homogeneous degree r in v variables, the number of coefficients $F_{\mathcal{P}}$ can be found from a recursive formula:

$$F_{\mathcal{P}}(v,r) = \begin{cases} 1 & \text{if } r = 0 \text{ or } v = 1, \\ \sum_{i=0}^{r} F_{\mathcal{P}}(v-1, r-i) & \text{otherwise.} \end{cases} \tag{4.29}$$

A comparison between the number of degrees of freedom can be made by calculating the ratio $F_{TL}(v,r)/F_{\mathcal{P}}(v,r)$. This results in the plots depicted in Fig. 4.5, where the number of variables v is plotted on the x-axis and the degree r is used as a parameter. The figure clearly shows that for both increasing v and r, F_{TL} is much smaller than $F_{\mathcal{P}}$. Note that the condition of strictly positive collector currents is not yet accounted for in this simplified comparison.

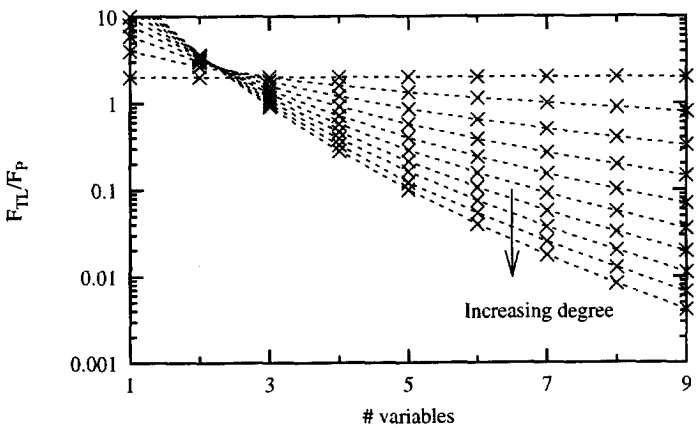

Figure 4.5: Comparison of the degrees of freedom in a polynomial and in a translinear loop equation.

The important conclusion that can be derived from Fig. 4.5 is that non-parametric decompositions are not likely to exist for polynomials of $r \geq 3$ and $v \geq 4$. This is illustrated by the fact that in the literature on STL circuits, the TL loop equations encountered are almost always second-order, see e.g. [50,61]. For polynomials with $r \geq 3$ and $v \geq 4$, parametric decompositions have to be used in most cases. A parametric TL decomposition consists of a set of TL loop

equations. As the number of coefficients in a set of equations is larger than for a single TL loop equation, a parametric decomposition can always be found.

The facts described above can be illustrated by comparing the number of TL loop equations that can be found for two different polynomials. The first polynomial describes a TL multiplier:

$$I_{\text{out}}I_{\text{o}} - I_{\text{in}_1}I_{\text{in}_2} = 0, \tag{4.30}$$

where I_{o} is a dc current, I_{in_1} and I_{in_2} are the input currents, and I_{out} is the output current. Equation (4.30) has a degree of two and contains four variables.

The second function is an approximation of the sine function, which can be used to design a TL sine shaper [43]:

$$I_{\text{out}}\left(I_{\text{o}}^2 + I_{\text{in}}^2\right) - \left(I_{\text{in}}I_{\text{o}}^2 - I_{\text{in}}^3\right) = 0, \tag{4.31}$$

where I_{o}, I_{in} and I_{out} denote, respectively, a dc current, the input current and the output current. Equation (4.31) has a degree of three and comprises three different variables.

If the input signal range of the multiplier is given by $|I_{\text{in}_1}, I_{\text{in}_2}| \leq I_{\text{o}}$, and the coefficients $c_{i,j}$ in the TL loop equation (4.27) are chosen from the set $[-1, 0, 1]$, nine non-parametric decompositions can be found. These are[4]:

$$(1-x-y+z)1 - (1-x)(1-y), \tag{4.32}$$
$$(1-x-y+z)(1+x) - (1-x)(1+x-y-z), \tag{4.33}$$
$$(1-x-y+z)(1+y) - (1-x+y-z)(1-y), \tag{4.34}$$
$$(1-x-y+z)(1+x+y+z) - (1-x+y-z)(1+x-y-z), \tag{4.35}$$
$$(1-x)(1+y) - (1-x+y-z)1, \tag{4.36}$$
$$(1-x)(1+x+y+z) - (1-x+y-z)(1+x), \tag{4.37}$$
$$(1-y)(1+x) - 1(1+x-y-z), \tag{4.38}$$
$$(1-y)(1+x+y+z) - (1+y)(1+x-y-z), \tag{4.39}$$
$$1(1+x+y+z) - (1+y)(1+x), \tag{4.40}$$

where 1, x, y and z represent the currents I_{o}, I_{in_1}, I_{in_2} and I_{out}, normalised with respect to I_{o}.

For eqn (4.31), with $|I_{\text{in}}| \leq I_{\text{o}}$, choosing the coefficients again from the set $[-1, 0, 1]$ now results in only one valid non-parametric decomposition:

$$(1+x)^2(1-x-z) - (1-x)^2(1+x+z), \tag{4.41}$$

where 1, x and z are the normalised currents.

[4]The algorithm described in Section 4.4.2 was used to generate these non-parametric decompositions.

Allowing a larger set of coefficients, e.g., $[-6,\ldots,6]$, results in only two additional decompositions:

$$(1-x-z)(2-x)(3-x)-(1-x)1(6-6x-5z), \tag{4.42}$$
$$(1+x+z)(2+x)(3+x)-(1+x)1(6+6x+5z). \tag{4.43}$$

In contrast, using the set $[-5,\ldots,5]$ of coefficient values for the multiplier already results in a total of 1300 different non-parametric decompositions.

These numbers clearly illustrate that although the degree is only one higher, it is much more difficult to find non-parametric decompositions for eqn (4.31) than for (4.30). Hence, it can be concluded that parametric decompositions are an absolute necessity.

4.4.2 An algorithm for non-parametric decomposition

Translinear decomposition is a fundamentally non-linear process and therefore not the easiest part of the design trajectory. For polynomials having a high degree and comprising a large number of independent variables in particular, it is rather difficult to derive valid TL decompositions heuristically. Automation of the TL decomposition process is the preferable solution for overcoming this problem. Unfortunately, an integral solution does not yet exist. However, as a start, this section describes an algorithm for the generation of *non-parametric* decompositions. An algorithm for the generation of *parametric* decompositions still remains to be developed.

In [50], considerable attention is paid to TL decomposition. In particular, some methods for finding TL decompositions are described. These are 'ratio manipulation' and 'differential forms' for non-parametric decompositions, and 'continued products', 'partial fractions' and 'continued fractions' for parametric decompositions. However, these methods do not provide a fundamental solution to the TL decomposition problem. They are either not generally applicable, or cannot generate all possible TL decompositions. Therefore, a different approach is used in this section.

Coefficients of the translinear loop equation

Ultimately, the coefficients $c_{i,j}$ in the TL loop equation (4.27) are implemented by transistor scaling factors, and possibly by scaling the capacitance values in DTL circuits. Matching of the transistors is an important aspect of TL circuits, as discussed in Section 5.6. In practical IC processes, relatively good matching can only be obtained when the transistors are scaled by integer values. Consequently, as accuracy is an important specification in most analogue designs and on-chip trimming is hardly ever available, the coefficients $c_{i,j}$ are restricted

to numbers in $\mathbb{Z}$.[5] This restriction does not completely exclude the use of irrational coefficients. For example, a current $I_{\sqrt{2}} = \sqrt{2}I_{\rm dc}$ can be generated from a TL circuit implementing $I_{\sqrt{2}}I_{\sqrt{2}} = 2I_{\rm dc}I_{\rm dc}$ [111]. The current $I_{\sqrt{2}}$ has to be regarded as an additional independent variable in the decomposition process. In fact, as a second TL loop is required to generate $I_{\sqrt{2}}$, this decomposition is a parametric decomposition, where $I_{\sqrt{2}}$ is an intermediate current.

In principle, all values in $\mathbb{Z}$ are allowed for the coefficients $c_{i,j}$. Large numbers, however, result in large scaling factors and hence a large chip area. A practical solution is to restrict the coefficient values to the set $[-N, \ldots, N]$, where N is a maximum scaling factor. In practice, the value of N is chosen well below 10. Most TL decompositions found in the literature, see, e.g., [50], comply with this condition.

Due to the limited set of coefficient values, the number of possible non-parametric TL decompositions is finite. Consequently, it becomes possible to develop an algorithm that can generate all of these TL decompositions.

Efficiency of the algorithm

An apparently simple algorithm would be to test each combination of coefficients for the TL loop equation (4.27) within the set $[-N, \ldots, N]$. Then a check should be made as to whether the resulting polynomial equals the original polynomial to be implemented, and whether all collector currents are strictly positive. However, even for a low value of N the number of combinations is huge and the required computation time unrealistic. For example, for $r = 3$, $v = 3$ and $N = 5$, $5.6 \cdot 10^{18}$ combinations have to be tested. Consequently, an *efficient* algorithm is required.

Overview of the developed algorithm

An algorithm has been developed that efficiently explores the finite space of potential solutions. The algorithm beneficially exploits important characteristics of the general TL loop equation (4.27). For clarity, a short overview is given before going into detail of the algorithm; this is illustrated in Fig. 4.6. The first characteristic of eqn (4.27) is the fact that the collector currents, which are linear combinations of the input and output currents, are strictly positive. This is used in the first stage of the algorithm to generate a set $\mathcal{T}_1$ of positive collector currents. Some elements of $\mathcal{T}_1$ cannot be part of a non-parametric decomposition. This is verified for each element using a division procedure, which is based on the fact that eqn (4.27) comprises two products of linear factors. The procedure results in a set $\mathcal{T}_2$, which is a subset of $\mathcal{T}_1$. Next, a recursive division procedure is applied to generate combinations of $2r$ elements from $\mathcal{T}_2$,

[5] Coefficients in $\mathbb{Q}$ are transformed to $\mathbb{Z}$ through multiplication by an appropriate integer number.

resulting in potential TL loop equations. This procedure is again based on the specific form of eqn (4.27). The recursive division procedure cannot exclude all erroneous combinations. Therefore, a final check is required to verify the consistency of the potential TL loop equations generated by the procedure.

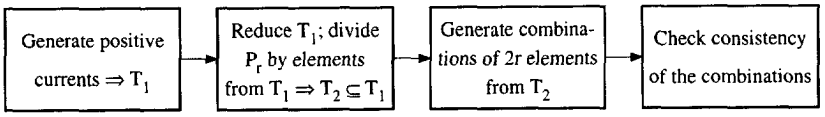

Figure 4.6: Overview of the non-parametric translinear decomposition algorithm.

Notation

A shorter notation is introduced to describe the decomposition algorithm. The polynomial to be decomposed is denoted by $\mathcal{P}_r$. The other polynomials encountered are, in general, described by:

$$\mathcal{P}_{r,a}, \tag{4.44}$$

where r is the degree of the polynomial $\mathcal{P}$ and different alphanumeric indices a are used to distinguish different polynomials.

Positive collector currents

It is favourable to use the characteristic of strictly positive collector currents first as this check has to be performed in any imaginable algorithm. Therefore, this check comprises the first stage of the developed algorithm and results in a set of positive collector currents, denoted by $\mathcal{T}_1$. As discussed in Section 4.4.1, generation of strictly positive linear combinations of the variables is straightforward. The number of coefficient combinations for a single collector current is much smaller than for a complete TL loop equation. Consequently, the computation time of this part of the algorithm is short.

Division by one collector current

The second stage of the algorithm removes all the collector currents from $\mathcal{T}_1$ which certainly cannot be part of a non-parametric decomposition. The result is a set $\mathcal{T}_2 \subseteq \mathcal{T}_1$. To this end, another characteristic of the TL loop equation is exploited.

Suppose that the polynomial $\mathcal{P}_r$, comprising n independent variables $I_{x_j} i$, $j \in [1, \ldots, n]$, has a valid TL decomposition given by[6] (compare with eqn (4.27)):

$$\lambda \mathcal{P}_r = \lambda_1 \mathcal{P}_{1,1} \ldots \mathcal{P}_{1,2r-1} - \lambda_2 \mathcal{P}_{1,2} \ldots \mathcal{P}_{1,2r}, \tag{4.45}$$

where λ, λ_1 and λ_2 are integers, and λ_1 and λ_2 have the same sign. The first product term on the RHS of eqn (4.45) represents the clockwise connected transistors; the last product represents the counter-clockwise connected transistors. The (linear) polynomials $\mathcal{P}_{1,i}$, where $i \in [1, \ldots, 2r]$, are members of the set $\mathcal{T}_1$ and represent the collector currents.

Then, division of eqn (4.45) by $\mathcal{P}_{1,1}$ and expansion with respect to one of the variables I_{x_j} yields:

$$\frac{\lambda \mathcal{P}_r}{\mathcal{P}_{1,1}} = \lambda_1 \mathcal{P}_{1,3} \ldots \mathcal{P}_{1,2r-1} - \lambda_2 \frac{\mathcal{P}_{1,2} \ldots \mathcal{P}_{1,2r}}{\mathcal{P}_{1,1}}, \tag{4.46}$$

$$= \mathcal{P}_{r-1,\mathrm{q}} + \frac{\mathcal{P}_{r,\mathrm{r}}}{\mathcal{P}_{1,1}}, \tag{4.47}$$

where $\mathcal{P}_{r-1,\mathrm{q}}$ and $\mathcal{P}_{r,\mathrm{r}}$ are the quotient ('q') and the remainder ('r') terms resulting from the division of $\mathcal{P}_r$ by $\mathcal{P}_{1,1}$.

Hence, owing to the form of the second product term on the RHS of eqn (4.46), the remainder $\mathcal{P}_{r,\mathrm{r}}$ in (4.47), resulting from an elaboration of the division, can be factored into r linear factors. This fact provides an interesting criterion for a selection procedure, illustrated in Fig. 4.7. The polynomial $\mathcal{P}_r$ is divided by each of the collector currents comprising $\mathcal{T}_1$. If the remainder of a particular division does not consist of r linear factors, that collector current cannot be a part of a non-parametric decomposition. Hence, that particular collector current is not added to $\mathcal{T}_2$. Obviously, $\mathcal{T}_2 \subseteq \mathcal{T}_1$.

An example can illustrate the above procedure. Consider the polynomial (eqn (4.31)):

$$\mathcal{P}_3 = I_{\mathrm{in}}^3 + I_{\mathrm{in}}^2 I_{\mathrm{out}} - I_{\mathrm{o}}^2 I_{\mathrm{in}} + I_{\mathrm{o}}^2 I_{\mathrm{out}}. \tag{4.48}$$

The currents $(I_{\mathrm{o}} - I_{\mathrm{in}})$ and $(I_{\mathrm{o}} - I_{\mathrm{out}})$ are two elements of $\mathcal{T}_1$. Division of $\mathcal{P}_3$ by $(I_{\mathrm{o}} - I_{\mathrm{out}})$ and expansion with respect to I_{o} yields:

$$\frac{\mathcal{P}_3}{I_{\mathrm{o}} - I_{\mathrm{out}}} = I_{\mathrm{o}} (I_{\mathrm{out}} - I_{\mathrm{in}}) - I_{\mathrm{out}} (I_{\mathrm{in}} - I_{\mathrm{out}}) + \frac{I_{\mathrm{in}}^3 + I_{\mathrm{in}}^2 I_{\mathrm{out}} - I_{\mathrm{in}} I_{\mathrm{out}}^2 + I_{\mathrm{out}}^3}{I_{\mathrm{o}} - I_{\mathrm{out}}}. \tag{4.49}$$

[6] It is assumed that the degree of the TL loop equation is equal to the degree of the polynomial.

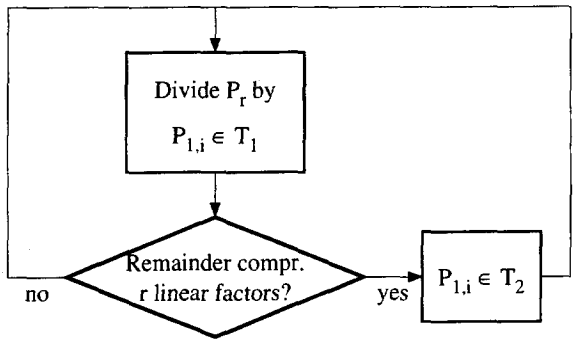

Figure 4.7: Generation of the set $\mathcal{T}_2$ from $\mathcal{T}_1$.

Since the remainder term is not factorable, $(I_o - I_{out})$ cannot be part of a valid non-parametric decomposition, i.e., $(I_o - I_{out}) \notin \mathcal{T}_2$.

On the contrary, division of $\mathcal{P}_3$ by $(I_o - I_{in})$ and expansion with respect to I_o yields:

$$\frac{\mathcal{P}_3}{I_o - I_{in}} = I_o\,(I_{out} - I_{in}) - I_{in}\,(I_{in} - I_{out}) + \frac{2I_{in}^2 I_{out}}{I_o - I_{in}}. \tag{4.50}$$

The remainder $I_{in} \cdot I_{in} \cdot I_{out}$ consists of three linear factors. Hence, $(I_o - I_{in}) \in \mathcal{T}_2$.

For eqn (4.48) with $N = 1$, $\mathcal{T}_1$ contains 9 elements: $\{(I_o - I_{in} - I_{out}), (I_o - I_{in}), (I_o - I_{in} + I_{out}), (I_o - I_{out}), I_o, (I_o + I_{out}), (I_o + I_{in} - I_{out}), (I_o + I_{in}), (I_o + I_{in} + I_{out})\}$. The second stage of the algorithm results in the set $\mathcal{T}_2$ containing 5 elements: $\{(I_o - I_{in} - I_{out}), (I_o - I_{in}), I_o, (I_o + I_{in}), (I_o + I_{in} + I_{out})\}$. The reduction of the set of possible collector currents considerably speeds up the remaining part of the algorithm.

Division by two collector currents

In the next stage of the decomposition algorithm, the polynomial $\mathcal{P}_r$ is divided by two collector currents from the set $\mathcal{T}_2$.

Suppose that the polynomial $\mathcal{P}_r$ has a valid TL decomposition given by eqn (4.45). Division by two collector currents from oppositely connected transistors then yields:

$$\frac{\lambda \mathcal{P}_r}{\mathcal{P}_{1,1}\mathcal{P}_{1,2}} = \frac{\lambda_1 \mathcal{P}_{1,3} \ldots \mathcal{P}_{1,2r-1}}{\mathcal{P}_{1,2}} - \frac{\lambda_2 \mathcal{P}_{1,4} \ldots \mathcal{P}_{1,2r}}{\mathcal{P}_{1,1}}, \tag{4.51}$$

$$= \mathcal{P}_{r-2,\mathrm{q}} + \frac{\mathcal{P}_{r-1,\mathrm{r1}}}{\mathcal{P}_{1,1}} + \frac{\mathcal{P}_{r-1,\mathrm{r2}}}{\mathcal{P}_{1,2}}, \tag{4.52}$$

where $\mathcal{P}_{r-2,\mathrm{q}}$ is the quotient term, and $\mathcal{P}_{r-1,\mathrm{r1}}$ and $\mathcal{P}_{r-1,\mathrm{r2}}$ are two remainder terms. The elaboration of the division described by eqn (4.51) is accomplished

by partial fraction expansion with respect to a variable I_{x_j} that the two currents $\mathcal{P}_{1,1}$ and $\mathcal{P}_{1,2}$ have in common. If no common variable exists, two different variables can be used to perform the expansion.

If $\mathcal{P}_{1,1}$ and $\mathcal{P}_{1,2}$ are indeed part of a valid TL decomposition, both $\mathcal{P}_{r-1,\mathrm{r1}}$ and $\mathcal{P}_{r-1,\mathrm{r2}}$ can be factored into $r-1$ first-order factors.

Furthermore, the two remainders in eqn (4.52) are polynomials of order $r-1$. There is no remainder term of order r. This attribute provides another important selection criterion, which is applied to each combination of two elements from $\mathcal{T}_2$. If a polynomial remainder term of order r does result from the division of $\mathcal{P}_r$ by two currents $\mathcal{P}_{1,1}$, $\mathcal{P}_{1,2} \in \mathcal{T}_2$, it can be concluded that $\mathcal{P}_{1,1}$ and $\mathcal{P}_{1,2}$ cannot (together) form two oppositely connected transistors of a valid non-parametric decomposition.

As an example, this characteristic is demonstrated for eqn (4.48). Division of $\mathcal{P}_3$ by $(I_\mathrm{o}+I_\mathrm{in})(I_\mathrm{o}-I_\mathrm{in}-I_\mathrm{out})$, two currents in $\mathcal{T}_2$, and expansion with respect to I_o, yields:

$$\frac{\mathcal{P}_3}{(I_\mathrm{o}+I_\mathrm{in})(I_\mathrm{o}-I_\mathrm{in}-I_\mathrm{out})} = I_\mathrm{out} - I_\mathrm{in} + \frac{I_\mathrm{out}^2(I_\mathrm{in}+I_\mathrm{out})}{(I_\mathrm{o}-I_\mathrm{in}-I_\mathrm{out})(2I_\mathrm{in}+I_\mathrm{out})} - \frac{2I_\mathrm{in}^2 I_\mathrm{out}}{(I_\mathrm{o}+I_\mathrm{in})(2I_\mathrm{in}+I_\mathrm{out})}. \quad (4.53)$$

Equation (4.53) contains third-order remainders. Hence, $(I_\mathrm{o}+I_\mathrm{in})$ cannot be combined with $(I_\mathrm{o}-I_\mathrm{in}-I_\mathrm{out})$ to form a part of a TL decomposition.

Conversely, division of $\mathcal{P}_3$ by another pair of currents, $(I_\mathrm{o}+I_\mathrm{in})(I_\mathrm{o}+I_\mathrm{in}+I_\mathrm{out})$, and expansion with respect to I_o, yields:

$$\frac{\mathcal{P}_3}{(I_\mathrm{o}+I_\mathrm{in})(I_\mathrm{o}+I_\mathrm{in}+I_\mathrm{out})} = I_\mathrm{out} - I_\mathrm{in} + \frac{2I_\mathrm{in}^2}{I_\mathrm{o}+I_\mathrm{in}} - \frac{I_\mathrm{out}(I_\mathrm{in}+I_\mathrm{out})}{I_\mathrm{o}+I_\mathrm{in}+I_\mathrm{out}}. \quad (4.54)$$

Equation (4.54) does not contain a third-order remainder. Therefore, the algorithm can continue with this pair of currents, as described in the next section.

Recursive division by two collector currents

The division by two collector currents can be applied recursively. This is illustrated in Fig. 4.8. The division procedure can be applied to the two remainder terms $\mathcal{P}_{r-1,\mathrm{r1}}$ and $\mathcal{P}_{r-1,\mathrm{r2}}$ in eqn (4.52). Note that the two fractions on the RHS of eqn (4.52) are similar to the fraction on the RHS of (4.47). However, the degree of $\mathcal{P}_{r-1,\mathrm{r1}}$ and $\mathcal{P}_{r-1,\mathrm{r2}}$ is lower than the degree of $\mathcal{P}_{r,\mathrm{r}}$. As the two remainders, $\mathcal{P}_{r-1,\mathrm{r1}}$ and $\mathcal{P}_{r-1,\mathrm{r2}}$, can be treated separately, the problem is effectively split up into two identical sub-problems.

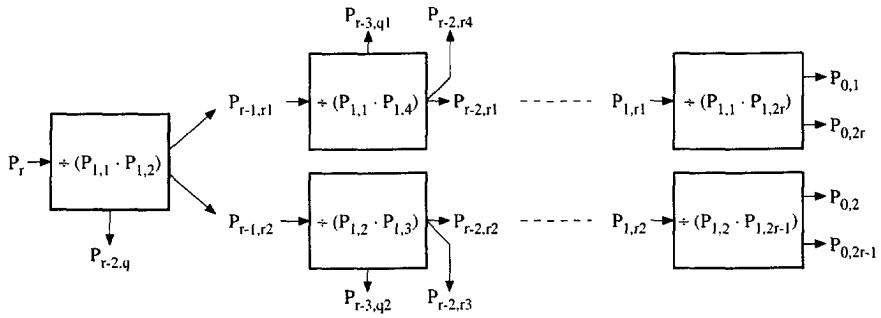

Figure 4.8: Recursive division procedure.

Suppose that the polynomial $\mathcal{P}_r$ has a valid TL decomposition given by eqn (4.45). Then, division of $\mathcal{P}_{r-1,\mathrm{r1}}$ by two currents $\mathcal{P}_{1,1},\ \mathcal{P}_{1,4} \in \mathcal{T}_2$ yields:

$$\frac{\mathcal{P}_{r-1,\mathrm{r1}}}{\mathcal{P}_{1,1}\mathcal{P}_{1,4}} = \mathcal{P}_{r-3,\mathrm{q1}} + \frac{\mathcal{P}_{r-2,\mathrm{r1}}}{\mathcal{P}_{1,1}} + \frac{\mathcal{P}_{r-2,\mathrm{r4}}}{\mathcal{P}_{1,4}}, \tag{4.55a}$$

where $\mathcal{P}_{r-3,\mathrm{q1}}$ is the quotient, and $\mathcal{P}_{r-2,\mathrm{r1}}$ and $\mathcal{P}_{r-2,\mathrm{r4}}$ are the two remainders. Both remainders can be factored into $r-2$ linear factors. Likewise, division of $\mathcal{P}_{r-1,\mathrm{r2}}$ by two currents $\mathcal{P}_{1,2}$ and $\mathcal{P}_{1,3}$ yields:

$$\frac{\mathcal{P}_{r-1,\mathrm{r2}}}{\mathcal{P}_{1,2}\mathcal{P}_{1,3}} = \mathcal{P}_{r-3,\mathrm{q2}} + \frac{\mathcal{P}_{r-2,\mathrm{r2}}}{\mathcal{P}_{1,2}} + \frac{\mathcal{P}_{r-2,\mathrm{r3}}}{\mathcal{P}_{1,3}}, \tag{4.55b}$$

where $\mathcal{P}_{r-3,\mathrm{q1}}$ is the quotient, and $\mathcal{P}_{r-2,\mathrm{r1}}$ and $\mathcal{P}_{r-2,\mathrm{r4}}$ are the two remainders.

Equations (4.55a) and (4.55b) do not contain a remainder term of order $r-1$. This is an important attribute, which is used to check whether $\mathcal{P}_{1,3}$ and/or $\mathcal{P}_{1,4}$ can be part of a valid TL decomposition in combination with $\mathcal{P}_{1,1}$ and $\mathcal{P}_{1,2}$.

Next, the division procedure is applied to the remainders $\mathcal{P}_{r-2,\mathrm{r1}}$ and $\mathcal{P}_{r-2,\mathrm{r2}}$, which are divided by $\mathcal{P}_{1,1} \cdot \mathcal{P}_{1,6}$ and $\mathcal{P}_{1,2} \cdot \mathcal{P}_{1,5}$, respectively.

During each recursive cycle of the algorithm, the degree of the two remainders is decreased by one. Ultimately, during the r^{th} cycle of the algorithm, two zero-degree polynomials, i.e. two integers, remain. To check whether the resulting set of $2r$ collector currents comprises a valid TL decomposition one final check has to be performed.

First, however, the recursive division procedure is illustrated by means of the eqn (4.48). Division of (4.48) by $\mathcal{P}_{1,1} = (I_\mathrm{o} - I_\mathrm{in})$ and $\mathcal{P}_{1,2} = (I_\mathrm{o} + I_\mathrm{in})$ yields:

$$\frac{2\mathcal{P}_3}{\mathcal{P}_{1,1}\mathcal{P}_{1,2}} = 2\,(I_\mathrm{out} - I_\mathrm{in}) + \frac{2I_\mathrm{in}I_\mathrm{out}}{I_\mathrm{o} - I_\mathrm{in}} - \frac{2I_\mathrm{in}I_\mathrm{out}}{I_\mathrm{o} + I_\mathrm{in}}. \tag{4.56}$$

Clearly, the two remainders $\mathcal{P}_{2,\mathrm{r1}} = 2I_\mathrm{in}I_\mathrm{out}$ and $\mathcal{P}_{2,\mathrm{r2}} = -2I_\mathrm{in}I_\mathrm{out}$ are second-order. The quotient is $\mathcal{P}_{1,\mathrm{q}} = 2(I_\mathrm{out} - I_\mathrm{in})$.

Next, division of $\mathcal{P}_{2,\mathrm{r1}}$ by $\mathcal{P}_{1,1}$ and $\mathcal{P}_{1,4} = (I_\mathrm{o} + I_\mathrm{in})$, and division of $\mathcal{P}_{2,\mathrm{r2}}$ by $\mathcal{P}_{1,2}$ and $\mathcal{P}_{1,3} = (I_\mathrm{o} - I_\mathrm{in})$, yields:

$$\frac{\mathcal{P}_{2,\mathrm{r1}}}{\mathcal{P}_{1,1}\mathcal{P}_{1,4}} = \frac{I_\mathrm{out}}{I_\mathrm{o} - I_\mathrm{in}} - \frac{I_\mathrm{out}}{I_\mathrm{o} + I_\mathrm{in}}, \tag{4.57a}$$

$$\frac{\mathcal{P}_{2,\mathrm{r2}}}{\mathcal{P}_{1,2}\mathcal{P}_{1,3}} = \frac{I_\mathrm{out}}{I_\mathrm{o} + I_\mathrm{in}} - \frac{I_\mathrm{out}}{I_\mathrm{o} - I_\mathrm{in}}. \tag{4.57b}$$

The remainders $\mathcal{P}_{1,\mathrm{r1}} = I_\mathrm{out}$, $\mathcal{P}_{1,\mathrm{r4}} = -I_\mathrm{out}$, $\mathcal{P}_{1,\mathrm{r2}} = I_\mathrm{out}$ and $\mathcal{P}_{1,\mathrm{r3}} = -I_\mathrm{out}$ are first-order. The quotients are $\mathcal{P}_{0,\mathrm{q1}} = 0$ and $\mathcal{P}_{0,\mathrm{q2}} = 0$.

Next, division of $\mathcal{P}_{1,\mathrm{r1}}$ by $\mathcal{P}_{1,1}$ and $\mathcal{P}_{1,6} = (I_\mathrm{o} - I_\mathrm{in} - I_\mathrm{out})$, and division of $\mathcal{P}_{1,\mathrm{r2}}$ by $\mathcal{P}_{1,2}$ and $\mathcal{P}_{1,5} = (I_\mathrm{o} + I_\mathrm{in} + I_\mathrm{out})$, yields:

$$\frac{\mathcal{P}_{1,\mathrm{r1}}}{\mathcal{P}_1\mathcal{P}_6} = \frac{-1}{I_\mathrm{o} - I_\mathrm{in}} + \frac{1}{I_\mathrm{o} - I_\mathrm{in} - I_\mathrm{out}}, \tag{4.58a}$$

$$\frac{\mathcal{P}_{1,\mathrm{r2}}}{\mathcal{P}_2\mathcal{P}_5} = \frac{1}{I_\mathrm{o} + I_\mathrm{in}} - \frac{1}{I_\mathrm{o} + I_\mathrm{in} + I_\mathrm{out}}. \tag{4.58b}$$

The remainders $\mathcal{P}_{0,\mathrm{r1}}$, $\mathcal{P}_{0,\mathrm{r2}}$, $\mathcal{P}_{0,\mathrm{r5}}$ and $\mathcal{P}_{0,\mathrm{r6}}$ equal -1, 1, -1, 1, respectively.

Final check

The steps of the algorithm described up to now result in one or more sets of $2r$ collector currents. Each set is a potential non-parametric TL decomposition. One final check is required to verify whether a certain set of $2r$ currents forms a TL decomposition. During the recursive procedure, illustrated in Fig. 4.8, some information is 'lost' for each cycle of the algorithm. Namely, the quotient polynomials and some of the remainder polynomials are not used during subsequent cycles of the algorithm. Therefore, the final check is required to verify whether these disregarded polynomials are consistent with the corresponding set of $2r$ currents.

Analytical elaboration of the TL decomposition algorithm for the second-order case easily yields an expression linking $\mathcal{P}_{0,\mathrm{q}}$, $\mathcal{P}_{0,\mathrm{r3}}$ and $\mathcal{P}_{0,\mathrm{r4}}$:

$$[\mathcal{P}_{0,\mathrm{q}}] - [\mathcal{P}_{0,\mathrm{r3}} + \mathcal{P}_{0,\mathrm{r4}}] = 0. \tag{4.59}$$

The first pair of square brackets contains the result of the first cycle of the algorithm; the second pair the result of the second cycle. Verification of whether eqn (4.59) is satisfied is given by the final stage of the algorithm. If the result is positive, it follows that $\lambda_1\mathcal{P}_{1,1}\mathcal{P}_{1,3}\mathcal{P}_{1,5} - \lambda_2\mathcal{P}_{1,2}\mathcal{P}_{1,4}\mathcal{P}_{1,6}$ is a valid non-parametric TL decomposition, see eqn (4.45). Further, $\mathcal{P}_{0,\mathrm{r1}}$ equals $-\lambda_2$, and $\mathcal{P}_{0,\mathrm{r2}}$ equals λ_1.

For third-order TL decompositions, the quotient and remainder polynomials are linked by:

$$[\mathcal{P}_{1,\mathrm{q}}] + [\mathcal{P}_{1,\mathrm{r3}} + \mathcal{P}_{1,\mathrm{r4}} + \mathcal{P}_{1,4}\mathcal{P}_{0,\mathrm{q1}} + \mathcal{P}_{1,3}\mathcal{P}_{0,\mathrm{q2}}] - [\mathcal{P}_{1,4}\mathcal{P}_{0,\mathrm{r1}} + \mathcal{P}_{1,3}\mathcal{P}_{0,\mathrm{r2}}] = 0. \quad (4.60)$$

For the example polynomial (4.48), verification of eqn (4.60) for the set of currents $\mathcal{P}_{1,1} = (I_\mathrm{o} - I_\mathrm{in})$, $\mathcal{P}_{1,2} = (I_\mathrm{o} + I_\mathrm{in})$, $\mathcal{P}_{1,3} = (I_\mathrm{o} - I_\mathrm{in})$, $\mathcal{P}_{1,4} = (I_\mathrm{o} + I_\mathrm{in})$, $\mathcal{P}_{1,5} = (I_\mathrm{o} + I_\mathrm{in} + I_\mathrm{out})$ and $\mathcal{P}_{1,6} = (I_\mathrm{o} - I_\mathrm{in} - I_\mathrm{out})$, yields a positive result. Further, $\lambda_1 = \lambda_2 = 1$ and $\lambda = 2$. Hence:

$$2\mathcal{P}_3 = (I_\mathrm{o} - I_\mathrm{in})^2 (I_\mathrm{o} + I_\mathrm{in} + I_\mathrm{out}) - (I_\mathrm{o} + I_\mathrm{in})^2 (I_\mathrm{o} - I_\mathrm{in} - I_\mathrm{out}). \quad (4.61)$$

The algorithm developed has been implemented in C and works satisfactorily. Nevertheless, improvements are likely to be possible and further research in this direction, also with a view to the development of an algorithm for parametric TL decomposition, is highly recommended.

4.4.3 Parametric decomposition

In the case of a parametric TL decomposition, the polynomial (4.26) is mapped onto a set of two or more TL loop equations. This is accomplished through the introduction of one or more parameters I_{p_j}, called intermediate currents, which are non-linearly related to the input and output currents. As discussed in Section 4.4.1, parametric decompositions are an absolute requirement simply because non-parametric decompositions do not always exist. A set of two TL loop equations contains twice as many coefficients as a single TL loop equation and the chances of finding a suitable decomposition are therefore increased significantly.

The introduction of one intermediate current I_p is accomplished by equating the polynomial $\mathcal{P}_r(I_{x_1}, \ldots, I_{x_n})$ to be implemented to another polynomial containing the parameter I_p. That is:

$$\begin{cases} \mathcal{P}_r(I_{x_1}, \ldots, I_{x_n}) & = \mathcal{P}_r(I_{x_1}, \ldots, I_{x_n}, I_\mathrm{p}), \\ \mathcal{P}_r(I_{x_1}, \ldots, I_{x_n}, I_\mathrm{p}) & = 0. \end{cases} \quad (4.62)$$

Now, both equations have to be implemented by a valid TL loop equation. The parameter I_p, introduced by eqn (4.62), represents a physical current. Therefore, I_p must be real, which forms an important condition for the possible polynomials $\mathcal{P}_r(I_{x_1}, \ldots, I_{x_n}, I_\mathrm{p})$. Further, for polynomials of higher-order in I_p, care has to be taken that multiple physical solutions for I_p do not occur. This is partly a biasing problem, as discussed in Section 4.5.1.

An important characteristic of a parametric decomposition is that the intermediate currents are not uniquely determined. A certain parametric decomposition can be described by different, yet equivalent, sets of equations. Linear transformations (within the set of all input, output, capacitance and intermediate currents) applied to an intermediate current I_p, e.g., $I'_\mathrm{p} = 2I_\mathrm{p} + I_\mathrm{in}$, do not fundamentally change a parametric decomposition.

As an example, consider the frequency-doubling circuit depicted in Fig. 3.4. This circuit is described by eqn (3.15), which is based on the definition $I_\mathrm{p} = I_4$. The definition of I_p is in fact quite arbitrary. Defining instead $I'_\mathrm{p} = I_3$, an alternative, yet equivalent, description is obtained, given by:

$$I_{\mathrm{in}_1}^2 = I'_\mathrm{p}\left(2I'_\mathrm{p} - I_\mathrm{out}\right), \tag{4.63a}$$

$$I_{\mathrm{in}_2}^2 = \left(I'_\mathrm{p} - I_\mathrm{out}\right)\left(2I'_\mathrm{p} - I_\mathrm{out}\right). \tag{4.63b}$$

The two intermediate currents I_p and I'_p are related by the transformation $I'_\mathrm{p} = \frac{1}{2}(I_\mathrm{p} + I_\mathrm{out})$.

In non-parametric TL decompositions, all transistor currents are linear combinations of the input, output and capacitance currents. This is not true for parametric TL decompositions, where the transistor currents are, in general, linear combinations of the input, output, capacitance and intermediate currents. Since the values of the intermediate currents are not known in advance, the decomposition algorithm described in Section 4.4.2 cannot be used for the generation of parametric TL decompositions. Lacking a proper algorithm, the most systematic approach remaining is the application of the 'continued products', 'partial fractions' and 'continued fractions' methods described in [50].

Parametric decomposition for dynamic translinear circuits

As described in Section 4.3, the state-space approach is a powerful tool for the synthesis of linear filters. Factually, a state-space description is already a form of parametric decomposition since the state currents are intermediate currents.

Next to the TL loops, a second type of loop, occurring in DTL circuits only, is the capacitance-junction(s) loop. The junctions in this loop are represented by a product of linear factors, the collector currents. In principle, this factorisation is unique. However, different factorisations can be constructed through the definition of intermediate currents.

An example can illustrate this. In [112], a first-order high-pass log-domain filter is described. The capacitance current in this filter is derived from the second-order polynomial $(I_\mathrm{in} + I_\mathrm{dc})(I_\mathrm{o} + I_{\mathrm{o}_1}) - I_\mathrm{out} I_\mathrm{o}$. Through the introduction of an intermediate current I_p, this polynomial is factored as $I_\mathrm{p} \cdot I_\mathrm{out}$. As a result, the capacitance-junctions loop contains one transistor biased at a current I_p and

one transistor biased at I_{out}, i.e.:

$$I_{cap} = CU_T \left(\frac{\dot{I}_{\text{p}}}{I_{\text{p}}} + \frac{\dot{I}_{\text{out}}}{I_{\text{out}}} \right), \tag{4.64}$$

$$= CU_T \frac{\dot{I}_{\text{in}} \left(I_{\text{o}} + I_{\text{o}_1} \right) - \dot{I}_{\text{out}} I_{\text{o}}}{\left(I_{\text{in}} + I_{\text{dc}} \right) \left(I_{\text{o}} + I_{\text{o}_1} \right) - I_{\text{out}} I_{\text{o}}}. \tag{4.65}$$

Design example: A third-order elliptic low-pass filter

On page 88, a set of three current-mode polynomials (4.18a)–(4.18c) was obtained for the elliptic log-domain filter to be designed. Translinear decomposition is the next synthesis step to be performed. Suitable TL decompositions have to be derived for each of the polynomials. In fact, eqns (4.18a) and (4.18c) are already valid TL loop equations. A non-parametric TL decomposition of eqn (4.18b) can be obtained through the addition of a term $I_{\text{o}} I_{x_2}$ to both sides of the equation. Biasing of the three TL loop equations thus obtained results in an interconnection of linear first-order filter sub-circuits, comparable to the network arrangements found in conventional filter implementations.

As well as the interconnection of linear sub-circuits, there are additional possibilities for implementing TL filters. Most of the log-domain filters presented in the literature are based on the set-up shown in Fig. 4.35 [9,10,12,14,15,89,90, 109,113]. In this arrangement, I_{in} forms the collector current of a transistor to implement current-to-voltage logarithmic compression. Exponential expansion from voltage to current is only performed at the output. Hence, the state currents I_{x_1} and I_{x_2} are not physically present within the so-called 'log-filter'.

For illustrative purposes, we design the elliptic filter in accordance with the set-up shown in Fig. 4.35. To accomplish this, *parametric* TL decompositions have to be derived for each of the polynomials (4.18a)–(4.18c). These decompositions need to have a special form in order to comply with the set-up shown in Fig. 4.35. In particular, in any TL loop equation each of the currents I_{x_1}, I_{x_2}, I_{x_3} and I_{in} is only allowed to form a linear factor *by itself*. Only this way can a biasing arrangement be derived where I_{x_1} and I_{x_2} do not have to be implemented physically. Note that I_{x_1} and I_{x_2} can be sensed using the analysis method described in Section 3.2.2.

The RHS of eqn (4.18a) comprises three variables: I_{x_2}, I_{x_3} and I_{in}. Hence, two intermediate currents, I_{p_1} and I_{p_2}, have to be introduced to arrive at a suitable decomposition. This is accomplished by equating the RHS of eqn (4.18a) to:

$$\left(I_{\text{p}_1} + I_{\text{o}} + I_{C_1} \right) I_{x_1} - \left(I_{\text{p}_1} - I_{\text{p}_2} \right) I_{x_1} - I_{\text{p}_2} I_{x_1}. \tag{4.66}$$

A parametric TL decomposition is obtained from a comparison of eqn (4.66)

with the RHS of (4.18a):

$$(I_{p_1} + I_o + I_{C_1})\, I_{x_1} = -I_o I_{in}, \tag{4.67a}$$
$$(I_{p_1} - I_{p_2})\, I_{x_1} = I_o I_{x_2}, \tag{4.67b}$$
$$3 I_{p_2} I_{x_1} = I_o I_{x_3}. \tag{4.67c}$$

Note that I_{x_1}, I_{x_2}, I_{x_3} and I_{in} only occur as linear factors by themselves.

Likewise, decompositions of (4.18b) and (4.18c) are obtained by equating the RHS of these polynomials respectively to:

$$(I_q + I_{C_2})\, I_{x_2} - I_q I_{x_2}, \tag{4.68}$$

and

$$(I_{r_1} + I_o + I_{C_3})\, I_{x_3} - (I_{r_1} + I_{r_2})\, I_{x_3} + I_{r_2} I_{x_3}, \tag{4.69}$$

where I_q, I_{r_1} and I_{r_2} are intermediate currents.

A comparison of eqn (4.68) with the RHS of (4.18b) yields the second parametric decomposition:

$$(I_q + I_{C_2})\, I_{x_2} = I_o I_{x_1}, \tag{4.70a}$$
$$I_q I_{x_2} = I_o I_{x_3}. \tag{4.70b}$$

A comparison of eqn (4.69) with the RHS of (4.18c) yields the third parametric decomposition:

$$3\,(I_{r_1} + I_o + I_{C_3})\, I_{x_3} = -I_o I_{in}, \tag{4.71a}$$
$$3\,(I_{r_1} + I_{r_2})\, I_{x_3} = I_o I_{x_1}, \tag{4.71b}$$
$$I_{r_2} I_{x_3} = I_o I_{x_2}. \tag{4.71c}$$

An implementation of the parametric TL decomposition thus obtained is designed on page 116.

4.5 Hardware implementation

Hardware implementation is the last synthesis task to be accomplished in order to obtain a prototype TL circuit. The TL loop equation has to be mapped onto a TL topology and the network has to be biased. In the context of TL circuits, biasing means that currents have to be supplied to a network of TL loops such that all transistors are forced to conduct the collector currents corresponding to the TL decomposition. Convenient currents to be supplied to the network have to be found by judicious addition and subtraction of the transistor currents.

Involving only the operations of addition and subtraction, biasing is merely a linear problem, in contrast to the issue of TL decomposition. Nevertheless, the extensive number of possible solutions for a specific TL decomposition adds to the complexity of this design step. Furthermore, the complexity increases with the number of TL loop equations and independent variables involved.

A general description of the issues involved in topology selection and biasing is given in Section 4.5.1. The theory is explained mainly in terms of NPN transistors, which are the most prevalent TL devices. Nevertheless, several alternative devices can be used to implement a TL loop. The additional possibilities opened up by these TL devices are discussed in Section 4.5.2.

4.5.1 Topology selection and biasing

The linear factors in a TL loop equation, see eqn (3.4), correspond to the collector currents and therefore with the base-emitter junctions of the transistors comprising the loop. Biasing means that the transistors are forced to conduct the required collector currents, which are each linear combinations of the input, output, capacitance and intermediate currents. Obviously, the node voltages also have to be biased such that all transistors operate in the active region.

Figure 4.9 shows the three basic ways to force a collector current through a transistor. The bias current source I_{bias} is connected either to the emitter or to the collector terminal. The emitter is an active terminal as its voltage directly controls the collector current. Hence, in Fig. 4.9(a), the transistor is forced to conduct I_{bias}. In contrast, the collector is not an active terminal; to a first-order approximation the collector does not control the transistor current. Therefore, a nullor has to be used to control the emitter or the base, which does control the collector current, and thus, forces the transistor to conduct I_{bias}. The nullor shown in Fig. 4.9(b) can, in principle, be replaced by a wire, resulting in a diode connection.

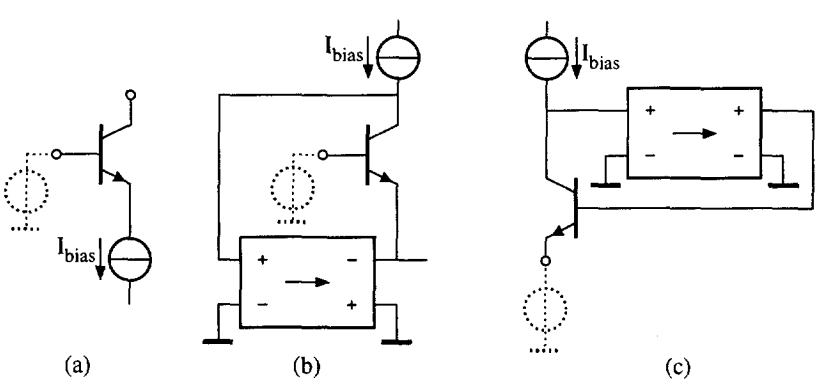

Figure 4.9: Three basic ways of current biasing of a transistor.

The three basic ways of biasing depicted in Fig. 4.9 can also be used to bias the transistors in a complete TL loop. To this end, currents are supplied to the circuit nodes of the loop. In principle, these nodes comprise the base and emitter terminals. However, as indicated by the possibility of diode-connected transistors, some collectors can also be connected to these nodes. Consequently, the currents to be supplied to the nodes of the TL loop are linear combinations of emitter and collector currents (base currents are assumed to be negligible). The process of biasing entails several degrees of freedom to manipulate these linear combinations and biasing thus becomes a quest for 'convenient' node currents; currents that are easily realised as current sources. An obvious example of a convenient node current is a dc current.

The collector terminals

A first degree of freedom in the biasing process is formed by the collector terminals. First of all, not all collector terminals are required to bias the transistors. This is illustrated by Fig. 4.9(a). These collectors are available to modify the node currents of the TL loop. The only restriction is of course that this should not result in saturation of one of the transistors. Judicious choices for the collector connections result in convenient node currents.

Secondly, for a diode-connected transistor, the collector is connected to the base of the same transistor. In a complete TL loop, this is not the only option. The collector terminal can often be connected to a different circuit node, as long as the voltage gain from that circuit node to the base terminal is positive.

Those collectors not connected to a circuit node, in one of the above ways, have to be connected to a suitable voltage source.

In principle, the biasing strategy of using the collector terminals to obtain convenient node currents does not require any additional circuitry. Hence, it results in efficient designs.

The ground connection

As a TL loop is not allowed to float completely, one (and only one) of the nodes of the loop has to be connected to ground or another voltage source. In principle, the designer is free to choose which node to connect to ground. Since the ground node does not have to be biased by a current source, the current flowing into the ground connection does not need to be convenient.

Arrangement of currents in the loop and the loop equation

The arrangement of the linear factors, i.e. the collector currents, in the TL loop constitutes a third degree of freedom with respect to the biasing procedure. The TL loop equation only determines the direction, clockwise or counter-clockwise,

of the base-emitter junctions. However, within each product of currents, the commutative properties of multiplication can be used to rearrange the linear factors. Different arrangements result in different node currents in the TL circuit implementation.

The topology of a translinear loop

Translinear loops can be implemented according to different topologies. The two basic topologies, 'folded' and 'stacked', are depicted in Fig. 4.10.[7] The choice of a particular topology is part of the biasing process. Different loop topologies result in different possibilities for the construction of node currents.

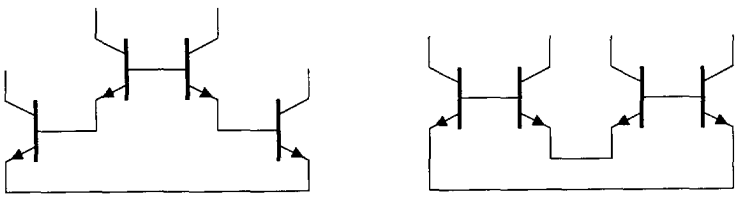

Figure 4.10: Two basic translinear loop topologies: (a) stacked and (b) folded.

For the stacked TL loop, shown in Fig. 4.10(a), the TL loop equation can be mapped onto the topology in four different ways. The emitter currents of the two emitter-connected transistors are added. Their combined current cannot be influenced by one of the collector currents. In contrast, the other node currents can be influenced. The collectors of the emitter-connected transistors can be connected to the emitters of the base-connected transistors to manipulate the corresponding node currents. Obviously, the stacked topology facilitates subtraction points. The base node of the upper transistors however only provides addition of currents since only collectors can be connected to it.

The folded topology, shown in Fig. 4.10(b), is more symmetrical than the stacked topology. It entails two axes of symmetry. As a consequence, folded topologies are less versatile when it comes to biasing. For a start, a second-order TL loop equation can be mapped on a second-order folded topology in two different ways only. Secondly, the structure only provides addition of transistor currents. The node currents of the two nodes formed by the emitters cannot be influenced by the collector currents. The nodes formed by the bases only facilitate the addition of (collector) currents.

[7] In higher-order loops, mixtures of folding and stacking are possible resulting in more than two topologies. For example, nine different fourth-order TL loop topologies exist [50].

In general, it can be concluded that the stacked topology is more easily biased using the methods discussed thus far. This is evidenced by the fact that most known TL circuits are based on the stacked topology, see e.g. [50, 61].

The choice for a stacked or folded topology depends not only on the possibilities for biasing. When low-voltage operation is required, e.g. a supply voltage of 1 volt is specified, the folded topology is often the only option.

Current mirrors

The absence of subtraction points in folded topologies is not a fundamental limitation. It can be overcome by additional circuitry in the form of current mirrors. These provide inversion and hence generate subtraction points. Both PNP and NPN current mirrors are applicable. In many designs, current mirrors are a valuable means for finding a proper biasing scheme. Some different applications of current mirrors to provide subtraction points are illustrated in Fig. 4.11.

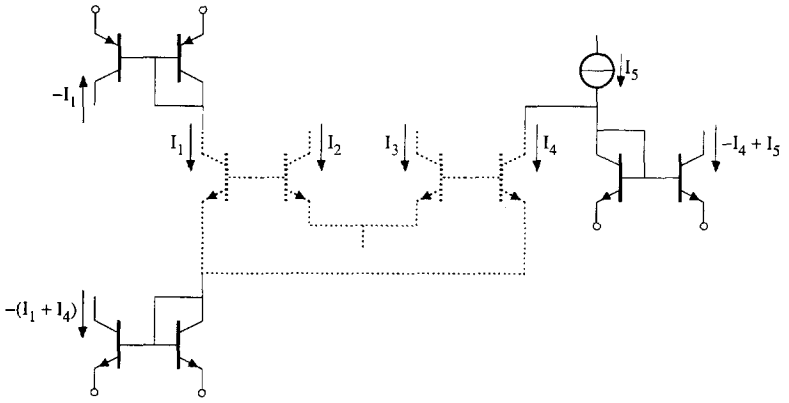

Figure 4.11: Current mirrors provide subtraction points in folded loop topologies.

Scaling of currents and emitter areas

Another biasing option is scaling of the collector currents. The base-emitter voltage is not changed if the collector current and the emitter area are both scaled by the same factor. Through this simple means, the node currents can be influenced so as to find different biasing solutions.

Level shifts and redundant transistors

In general, a pair of equal-valued oppositely-connected voltage sources can be inserted in the loop without changing the TL loop equation. These level shifts

can be used to change the circuit node voltages. Thus, collector connections become possible, which were not allowed in the original loop due to the requirement of operation in the active region of all transistors. Obviously, insertion of level shifts is a form of stacking, and therefore not suitable for low-voltage applications.

A possible implementation of the voltage sources is the insertion of redundant pairs of transistors into the TL loop. A redundant pair comprises two oppositely connected transistors with an equal collector current density and hence does not alter the TL loop equation. The redundant pair of transistors need not necessarily be biased at a dc current. Figure 4.12 shows an arrangement in which the current I_p is one of the factors in the original TL loop equation [14,44,114]. The collector current of both redundant transistors equals $I_{bias} - I_p$. The exact wave form of this current is irrelevant as long as its value is guaranteed to be strictly positive at all times. If I_p constitutes an inconvenient node current to be sunk, this structure can beneficially solve the bias problem. Note that the arrangement shown in Fig. 4.12 does alter the TL loop equation. It adds the solution $I_p = I_{bias}$, but this is not a stable solution.

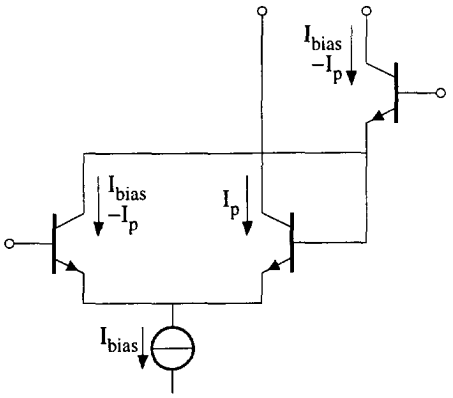

Figure 4.12: Redundant pair of transistors in a translinear loop [44].

Nullor implementations

Feedback is frequently used in TL circuits for the purpose of biasing as it introduces new possibilities. This is illustrated by Fig. 4.9(b,c), where nullors are used to force the collector currents. In Fig. 4.9(c), the output current of the nullor functions as a node current source. Now, the biasing process is simplified by the fact that the output current does not need to have a convenient value as it is determined by negative feedback.

Practical nullor implementations for TL circuits are often as simple as a single stage, e.g. a CE stage, a CC stage or a differential pair. In a complete TL circuit, some transistors comprising the loops can also function as nullor implementations. This is illustrated in Fig. 4.13.

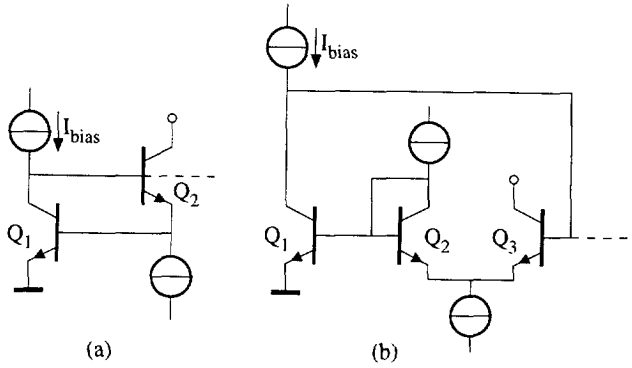

Figure 4.13: Part of the translinear loop functioning as a nullor implementation.

Figure 4.14 shows an example of the application of nullors to enable biasing of a DTL circuit [115]. The TL filter consists of two coupled second-order loops in folded topology. The voltage V_{ref} is a dc bias voltage; the 'ground' connection of this circuit. Denoting the collector current of Q_3 as the intermediate current I_{p}, the two loop equations are described by:

$$I_{\text{in}_1} I_{\text{o}} = (I_{\text{p}} - I_{\text{cap}})\, I_{\text{out}}, \tag{4.72a}$$

$$I_{\text{in}_2} I_{\text{o}} = I_{\text{p}} I_{\text{out}}. \tag{4.72b}$$

The tail currents of the three differential pairs equal $(I_{\text{in}_1} + I_{\text{p}} - I_{\text{cap}})$, $(I_{\text{in}_2} + I_{\text{p}})$ and $(I_{\text{o}} + I_{\text{out}})$. Obviously, these currents cannot be supplied by bias current sources. However, the inconvenient tail currents are readily realised by means of negative feedback. The nullors are implemented by the common-source stages M_1, M_2 and M_3.

Implementation of functions having multiple solutions

In Section 4.2.1, functions with multiple solutions were discussed. Implementation of the correct solution, or switching between different solutions dependent on the input signal is a biasing issue. The biasing arrangement has to be made so that only one solution is physically possible at each instant of time. The characteristic used to realise this is the fact that a transistor can only conduct positive currents. This is explained by means of an example circuit.

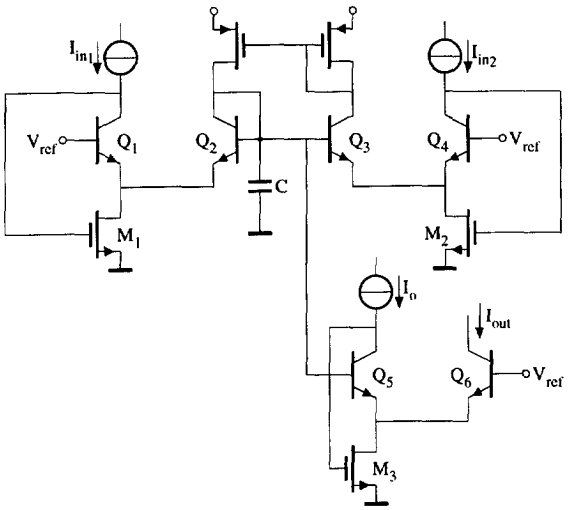

Figure 4.14: Biasing of a translinear integrator with the aid of nullor implementations [115].

Consider the modulus circuit depicted in Fig. 4.15. The TL loop equation is given by:

$$(I_o + I_{in})(I_o - I_{in}) = (I_o + I_{out})(I_o - I_{out}). \tag{4.73}$$

The solutions of eqn (4.73) are $I_{out} = \pm I_{in}$. The key to a proper biasing arrangement for eqn (4.73) is transistor Q_7. Its collector current I_7 equals I_{out}. Since I_7 can only have positive values, I_{out} necessarily switches between the solutions $I_{out} = I_{in}$, for $I_{in} \geq 0$, and $I_{out} = -I_{in}$, for $I_{in} < 0$, resulting in the absolute value function.

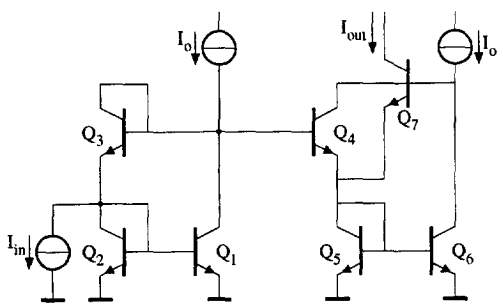

Figure 4.15: Modulus circuit [50].

Implementation of parametric translinear decompositions

Until now, this section has only been concerned with the biasing properties of a single TL loop circuit. For parametric decompositions, however, multiple TL loops are necessarily involved. These loops interact by means of the intermediate currents, as illustrated in Fig. 3.2.

In this context, the term 'topology' has to be placed in a wider context. A distinction can be made between disjunct and coupled TL loops, see Fig. 3.1. Parametric decompositions that have certain collector currents in common can be implemented both by coupled and disjunct TL loops. However, recall from Section 3.1 that the set of fundamental TL loops is not uniquely defined. Different sets of independent loop equations exist, which result in different biasing arrangements when an implementation by means of disjunct loops is designed. As an example, consider the parametric decomposition given by [116]:

$$2I_{\text{out}}\,(I_{C_1} + I_{\text{o}})\,I_{\text{p}} = I_{\text{in}} I_{\text{o}}^2, \tag{4.74a}$$

$$2\,(I_{\text{p}} - I_{C_2})\,(I_{C_1} + I_{\text{o}}) = I_{\text{o}}^2, \tag{4.74b}$$

which can be rewritten as:

$$I_{\text{out}} I_{\text{p}} = I_{\text{in}}\,(I_{\text{p}} - I_{C_2})\,, \tag{4.75a}$$

$$2\,(I_{\text{p}} - I_{C_2})\,(I_{C_1} + I_{\text{o}}) = I_{\text{o}}^2. \tag{4.75b}$$

Implementation of eqn (4.74a) by means of disjunct loops yields a circuit other than the implementation of (4.75a).

Biasing of dynamic translinear circuits

The fundamental difference between STL and DTL circuits is, respectively, the absence and presence of capacitance currents. In the context of biasing, the capacitance currents can be considered to be a special kind of current source. Naturally, the voltage across a capacitor is fixed since the capacitance voltage determines the capacitance current. This voltage is generated by the collector currents occurring in the definitions of the capacitance currents, see Section 4.3.

In most published TL filters, the capacitors are connected to nodes of the TL loops. However, this is not necessary, as evidenced, e.g. by the substructure C-Q_5 shown in Fig. 8.10. The TL loop, comprising Q_1–Q_4, generates the current I_{cap}, which is supplied to the capacitor. Integration of I_{cap} yields the output current I_{out}, which is again fed back to the TL loop by means of a current mirror.

Implementation of non-parametric decompositions using multiple translinear loops

Multiple TL loop circuits are not exclusively related to parametric decompositions. It is equally possible to implement a non-parametric decomposition by means of multiple loops. These loops are described by equal or different non-parametric TL loop equations. All loop equations represent the same transfer function and are therefore linearly dependent. To bias the circuit, convenient node currents have to be derived for all loops simultaneously, using the methods described earlier in connection with single TL loop circuits. Since more collector terminals are available, additional possibilities arise to find convenient node currents.

An example is the well-known 'six-pack' four-quadrant multiplier shown in Fig. 4.16 [45]. This circuit contains two fundamental TL loops, Q_1–Q_4 and Q_1-Q_5-Q_6-Q_4, described by eqns (4.33) and (4.37). Since eqns (4.33) and (4.37) do not contain intermediate currents, this is obviously a non-parametric decomposition. This is evidenced further by the linear dependence of eqns (4.33) and (4.37) and the fact that all collector currents can be expressed as linear combinations of I_o, I_{in_1}, I_{in_2} and I_{out}. In this circuit, the output current is obtained from a judicious interconnection of the collectors of Q_3 through Q_6.

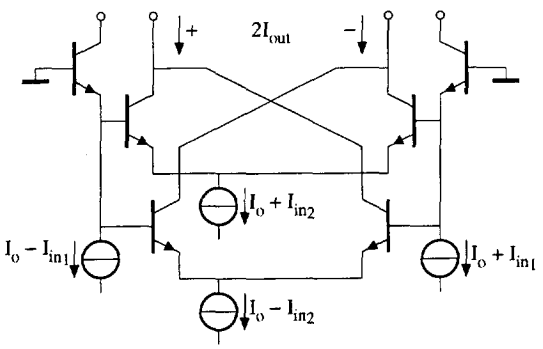

Figure 4.16: The 'six-pack' four-quadrant multiplier [45].

Design example: A third-order elliptic low-pass filter

Biasing is the last design step to be performed in order to obtain a prototype TL circuit implementation of the third-order elliptic filter. As discussed on page 106, it is possible to find a biasing arrangement of the parametric TL decomposition, comprising eqns (4.67a)–(4.67c) and (4.70a)–(4.71c), based on the set-up shown in Fig. 4.35. Each of the currents I_{x_1}, I_{x_2}, I_{x_3} and I_{in} is implemented by a single collector current. Figure 4.17 shows a realisation of

the fractions $I_{\text{out}}/I_{\text{o}}$ $(= 2I_{x_3}/I_{\text{o}})$, $I_{\text{in}}/I_{\text{o}}$, I_{x_1}/I_{o} and I_{x_2}/I_{o}. The tail current of each differential pair is sunk by a CE transistor stage. The bases of all the transistors biased at a current I_{o} are connected to a dc voltage V_{dc}. The capacitance voltages are denoted by V_{C_1}, V_{C_2} and V_{C_3}. Since I_{x_1} and I_{x_2} are not physically required, the dotted transistors do not have to be implemented physically. They can be used however to sense I_{x_1} and I_{x_2}, as explained in Section 3.2.2.

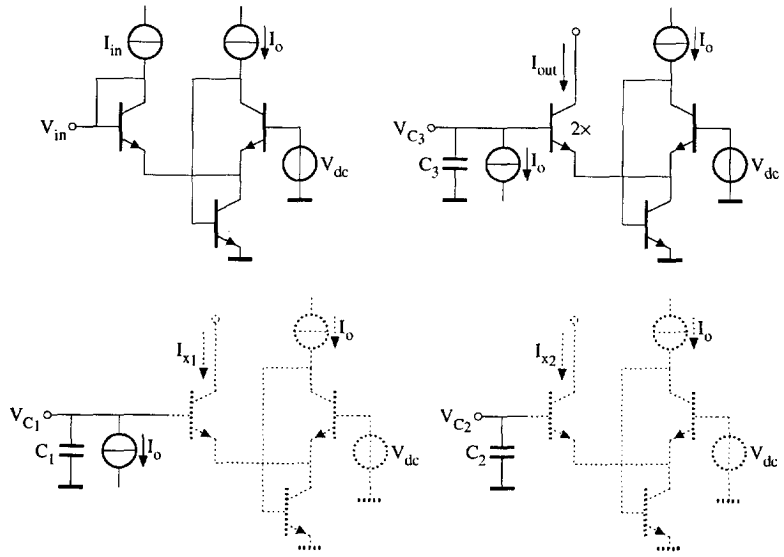

Figure 4.17: Implementation of the input compression, the output expansion and the state currents I_{x_1} and I_{x_2}. The dotted components are fictitious; they do not have to be implemented physically.

Figure 4.18 shows a biasing arrangement for the elliptic filter based on the stages depicted in Fig. 4.17. The interconnection wires between the various sub-circuits are not depicted for convenience. The current $(I_{\text{o}} + I_{C_1})$, see eqn (4.18a), is formed by the collector currents of Q_1 and Q_3 and the emitter current of Q_6, which equal I_{p_2}, $(I_{\text{p}_1} - I_{\text{p}_2})$ and $(I_{\text{p}_1} + I_{\text{o}} + I_{C_1})$, respectively; compare with eqns (4.18a) and (4.66). In accordance with eqn (4.67c), Q_2 is scaled by a factor of three. The transistor currents of Q_{11}, Q_{14}, Q_2, Q_{23} and Q_{26} are equal to I_{q}, $(I_{\text{q}} + I_{C_2})$, I_{r_2}, $(I_{\text{r}_1} + I_{\text{r}_2})$ and $(I_{\text{r}_1} + I_{\text{o}} + I_{C_3})$, respectively. Transistors Q_{24} and Q_{25} are scaled by a factor three as well.

Simulations verify the correct operation of the elliptic filter. Transistor non-idealities are beyond the scope of this chapter; they are dealt with in Chapter 5.

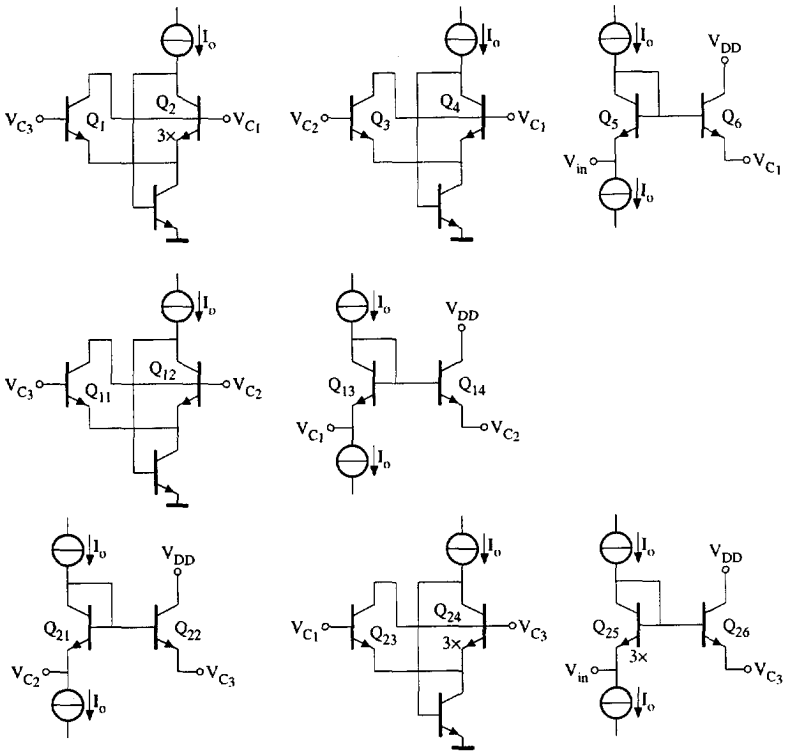

Figure 4.18: Biasing arrangement for the third-order elliptic low-pass filter.

Therefore, ideal transistor models are used in the simulations. Figure 4.19 shows the small-signal ac transfer function. With $I_o = 1$ μA, $C_1 = C_3 = 22.5$ pF and $C_2 = 8.85$ pF, the simulated cut-off frequency is 642 kHz. The transmission zero is located at 872 kHz. The maximum pass-band ripple of 1.25 dB is attained at 358 kHz. The minimum attenuation of -20.5 dB is realised at 1.35 MHz.

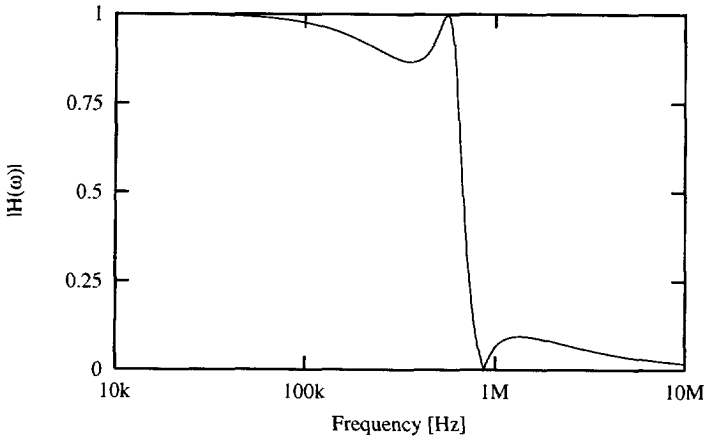

Figure 4.19: Small-signal transfer function of the third-order elliptic low-pass filter.

Due to the companding nature of TL filters, correct operation of the designed log-domain filter cannot be proven by small-signal analysis. The transient simulations of I_{out} depicted in Fig. 4.20 do demonstrate the externally linear behaviour of the TL filter. Simulations are shown for different frequencies f of the input signal $I_{in} = -I_{dc}(1 + 0.25 \sin 2\pi ft)$. The x-axis is normalised. For sinusoidal signals, the maximum amplitude of the input signal is 0.30 I_{dc}, due to the maximum internal gain of 3.4 from u to x_2. An amplitude of 0.25 I_{dc} corresponds to 85% of this maximum.

4.5.2 Translinear devices

Next to the NPN transistor, several other devices are characterised by an exponential V-I relation. This section discusses the TL devices depicted in Fig. 4.21.

Diodes

In principle, TL loops can be constructed using only diodes. However, the limited number of terminals of the diode severely restricts the possibilities for biasing a TL loop comprising only diodes. Both terminals of each diode being

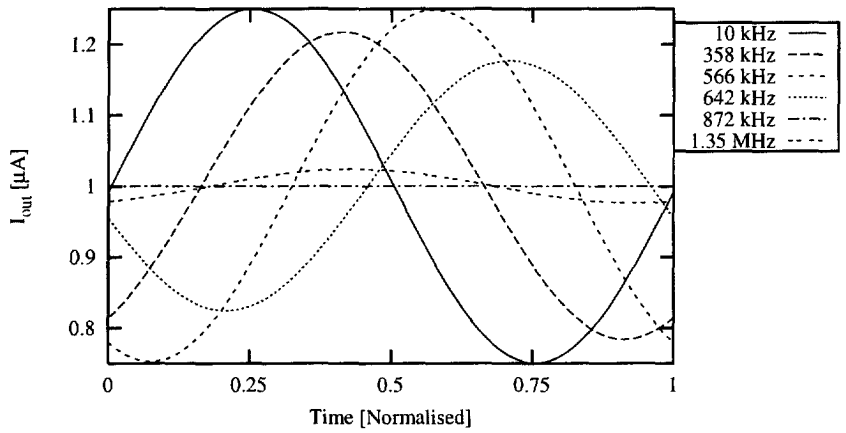

Figure 4.20: Transient analysis of the third-order elliptic low-pass filter for different frequencies.

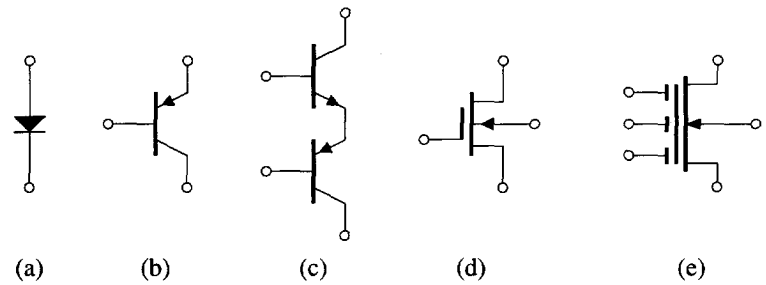

Figure 4.21: Translinear devices: (**a**) diode, (**b**) PNP transistor, (**c**) compound transistor, (**d**) subthreshold MOS transistor, and (**e**) floating-gate MOS transistor.

connected to the nodes of the TL loop, no collector terminals are available to manipulate the node currents.

Due to this limitation, a proper biasing scheme can often only be found by the application of additional circuitry. In particular, including a diode in the feedback path of a nullor results in a virtual device with more than two terminals, and hence additional biasing options. An example of this approach is formed by the TL filter shown in Fig. 3.5, where D_1 and D_3 are connected in the feedback path of two op amps.

Lateral and vertical PNP transistors

New topologies arise when mixtures of NPN and PNP transistors are used to create TL loops. An example of such a mixed loop is the well-known class-AB output stage used in many op amp realisations. In modern processes, where vertical PNP transistors are available, high-frequency operation of the TL circuit is not impeded. The use of lateral PNP transistors in the TL loops is restricted mainly to low-frequency applications.

Since the saturation currents of NPN and PNP transistors cannot be expected to match, in a single TL loop, both the NPN and the PNP transistors have to satisfy the STL principle in order to obtain a process and temperature-independent loop equation. That is, both for the NPN and the PNP transistors, the number of clockwise and counter-clockwise oriented transistors have to be equal.

For second-order TL loops, five mixed topologies can be derived; two folded topologies, depicted in Fig. 4.22, and three stacked topologies, depicted in Fig. 4.23. These mixed topologies allow different biasing arrangements in comparison with the all-NPN topologies depicted in Fig. 4.10. Hence, the availability of (high-frequency) PNP transistors provides additional biasing possibilities.

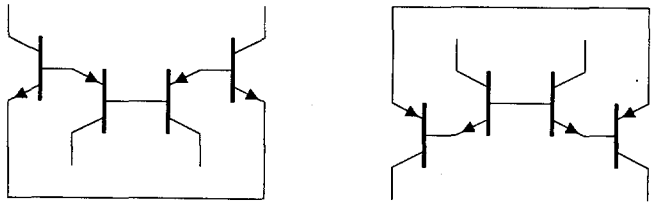

Figure 4.22: Mixed translinear loops in folded topology.

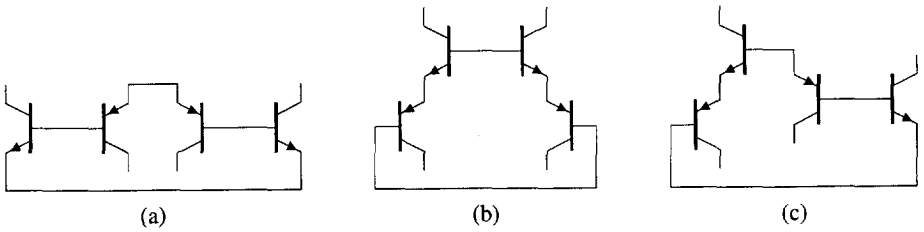

Figure 4.23: Mixed translinear loops in stacked topology.

The MOS transistor in weak inversion

In the subthreshold region, the MOS transistor is often characterised by an exponential V-I relation. In the saturation region, the drain current I_{DS} is given by [86,117]:

$$I_{\mathrm{DS}} = I_0 \exp \frac{V_{\mathrm{GS}}}{nU_T} \exp \frac{(n-1)V_{\mathrm{BS}}}{nU_T}, \tag{4.76}$$

where n is a constant representing the process-dependent subthreshold slope. Recently, the exponential behaviour in the subthreshold region has led to a strong revival of TL circuits in the context of MOS analogue VLSI (neural) networks, where the high functional density offered by TL technology is very much welcome, see, e.g., [65,66].

For DTL circuits, some care has to be taken with respect to the subthreshold slope factor as it influences the capacitance current expressions. For a capacitance connected to the gate terminal, the 'equivalent thermal voltage' $U_{\mathrm{T_{eq}}}$, to be used in eqn (3.24), equals nU_T. The connection of a capacitance to the source and back-gate respectively yields $U_{\mathrm{T_{eq}}} = U_T$ and $U_{\mathrm{T_{eq}}} = nU_T/(n-1)$.

Additionally, the different process-dependence of the subthreshold slope for NMOS and PMOS devices prohibits the application of most mixed TL loops. An exception is the loop depicted in Fig. 5.10(b).

Application of the back-gate

A simple way to design a subthreshold TL circuit is to translate a bipolar circuit design, replacing the base-emitter junctions by gate-source voltages. However, the MOS device finds wider use in TL technology.

In weak inversion, the body terminal can be used as an active gate as well as the front gate [118,119]. As a result, many new TL loop topologies become feasible. First of all, consider the circuit depicted in Fig. 4.24. Instead of the usual loop of gate-source voltages, this TL network comprises a second-order (folded) loop of gate-bulk voltages.

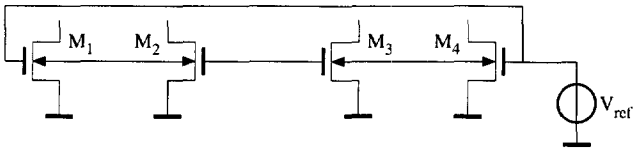

Figure 4.24: Translinear loop of gate-bulk voltages.

The gate-bulk voltage V_{GB} can be found from eqn (4.76):

$$V_{GB} = nU_T \ln \frac{I_{DS}}{I_0} - nV_{BS}. \tag{4.77}$$

Due to the TL loop configuration, the sum of the gate-bulk voltages is zero. Using (4.77), the circuit can be described by:

$$nU_T \left(\ln \frac{I_1}{I_0} - \ln \frac{I_2}{I_0} + \ln \frac{I_3}{I_0} - \ln \frac{I_4}{I_0} \right) - n \left(V_{BS_1} - V_{BS_2} + V_{BS_3} - V_{BS_4} \right) = 0. \tag{4.78}$$

Note that the voltage V_{ref}, depicted in Fig. 4.24, does not influence eqn (4.78). The constants n and I_0 can be dropped from eqn (4.78). The back-gate voltages can be eliminated as well, since the back-gates of M_2 and M_3, and of M_1 and M_4, are connected, resulting in:

$$\frac{I_1 I_3}{I_2 I_4} = \exp \frac{V_{S_2} - V_{S_1} + V_{S_4} - V_{S_3}}{U_T}. \tag{4.79}$$

In Fig. 4.24, all sources are connected to ground. Consequently, the RHS of eqn (4.79) equals 1 and (4.79) simply reduces to (2.14), with $\lambda = 1$.

The fact that all sources of the MOS transistors are connected to the same voltage is advantageous in low-voltage low-power environments. A difference with respect to bipolar transistor TL loops is that the MOS circuit needs a gate or back-gate voltage to be biased. In the circuit shown in Fig. 4.24, two gates are biased at a voltage V_{ref}. In theory, this can be done without power consumption, since the gate and back-gate draw no current.

An application of the circuit is described in [118], where it is used in the feedback path of an amplifier to realise a $\sqrt{x}$-function. A DTL application is proposed in [105], where a TL integrator is described.

Figure 4.25 depicts another MOS TL loop. The loop is constructed from gate-source voltages; the back gates have not been connected yet.

Applying eqn (4.76), the loop satisfies:

$$\frac{I_1 I_3}{I_2 I_4} = \exp \frac{V_{BS_1} - V_{BS_2} + V_{BS_3} - V_{BS_4}}{\eta U_T}, \tag{4.80}$$

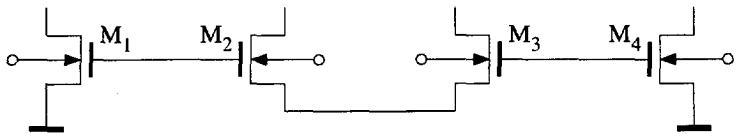

Figure 4.25: A folded loop of gate-source voltages with floating back-gates.

where $1/\eta = 1 - 1/n$. The source voltages of M_1 and M_4, and of M_2 and M_3, are identical. As a consequence, they cancel out and an equation very similar to (4.79) is obtained. Instead of connecting all the back-gates together, which would again result in eqn (2.14), it is also possible to add the back-gate voltages of M_1 and M_3, and of M_2 and M_4, simply by connecting them. Equation (4.80) thus becomes:

$$\frac{I_1 I_3}{I_2 I_4} = \exp \frac{2V_{B_1} - 2V_{B_2}}{\eta U_T}. \tag{4.81}$$

Now, if the back-gates of M_1 and M_4 are connected to the back-gates of two supplementary MOS transistors, M_5 and M_6, respectively, and M_5 and M_6 have the same gate voltage, a theoretically process and temperature-independent transfer is obtained. The resulting circuit, depicted in Fig. 4.26, is described by an equation structure containing two squared currents:

$$\frac{I_1 I_3}{I_2 I_4} = \frac{I_5^2}{I_6^2}. \tag{4.82}$$

This equation structure is different from the equations that can be realised with bipolar TL networks. An application of eqn (4.82) is described in Section 8.1.2.

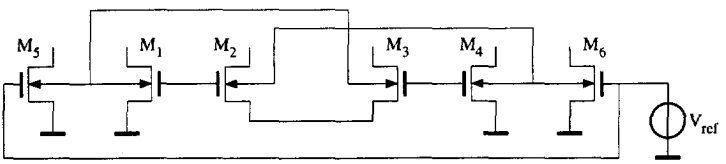

Figure 4.26: Circuit realising equation structure (4.82).

The topology of the circuit shown in Fig. 4.26 actually consists of two loops of gate-bulk voltages. The first loop is formed by M_1-M_2-M_6-M_5; the second by M_3-M_4-M_6-M_5.

A more complex equation structure with four squared currents can be obtained by inserting a bulk-connected pair between the gates of M_5 and M_6, grounding the sources of these two extra transistors. The resulting topology is

described by:

$$\frac{I_1 I_3}{I_2 I_4} = \frac{I_5^2 I_7^2}{I_6^2 I_8^2}. \tag{4.83}$$

An equation structure with two cubed currents is also possible, starting with a loop of six gate-source voltages in folded configuration. If the back-gates of the transistors with the same orientation in the loop are tied together and the two remaining back-gate voltages are connected to the bulk voltages of two extra transistors M_7 and M_8 with the same gate voltage, the resulting topology is described by:

$$\frac{I_1 I_3 I_5}{I_2 I_4 I_6} = \frac{I_7^3}{I_8^3}. \tag{4.84}$$

As a conclusion, using the back-gate in MOS TL circuits, new equation structures are realised. In theory, these additional equations might result in more area-efficient realisations. However, in practice, TL decompositions will hardly ever require the full functionality offered by these equations.

Triode region operation

In the triode region, in weak inversion, the voltage at the drain terminal is exponentially related to the drain current:

$$I_{\mathrm{DS}} = I_0 \exp \frac{V_{\mathrm{GB}}}{nU_T} \left(\exp \frac{-V_{\mathrm{SB}}}{U_T} - \exp \frac{-V_{\mathrm{DB}}}{U_T} \right). \tag{4.85}$$

Consequently, the gate-drain voltage V_{GD} can be employed as well as V_{GS} as part of a TL loop [120]. This results in new TL loop topologies.

In [121], an MOS differential pair is described based on triode region operation. Figure 4.27 depicts both the conventional and the triode region differential pair. In Fig. 4.27(b), transistor $M_{2,3}$ operates in the triode region. The transfer function from the input voltage V_{in} to the single-ended output current I_{out} is exactly equivalent to the V-I transfer function of the conventional differential pair, provided that the back-gates of M_1 and $M_{2,3}$ are both grounded. The tail current of the new differential pair is controlled by the bias voltage V_{bias}. In addition, the tail current can be altered by connecting a current source to the source of M_1.

Folded TL loops are essentially built up from series-connected differential pairs. Hence, new TL topologies can be derived by the series connection of new and conventional MOS differential pairs. For NMOS second-order TL loops, this results in three new topologies, depicted in Fig. 4.28. Note that for each triode region operated MOS transistor, one source terminal remains floating.

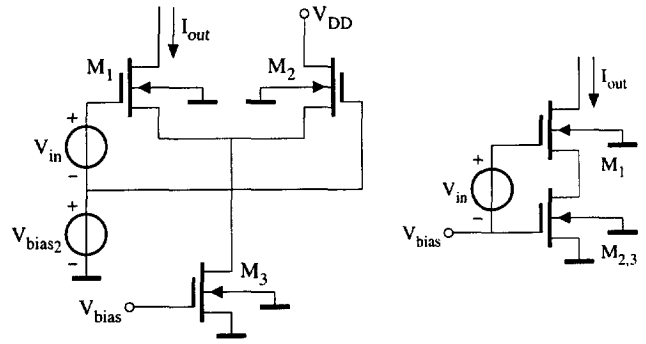

Figure 4.27: (a) Conventional and (b) triode region single-ended differential pair.

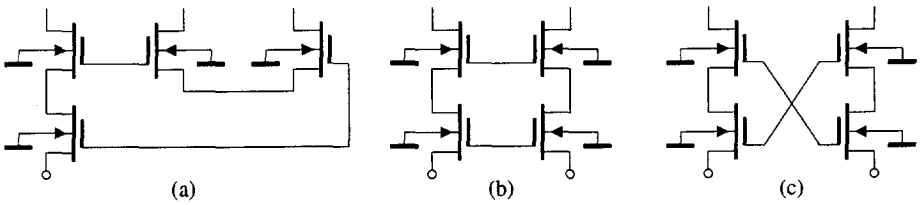

Figure 4.28: Translinear loops based on triode region operation of (some of) the NMOS transistors.

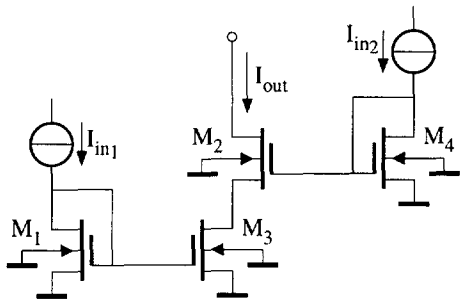

Figure 4.29: A harmonic mean circuit [65,122].

Connection of these terminals to an appropriate voltage is part of the biasing process.

The TL topologies shown in Fig. 4.28 can be described by current-mode loop equations, based on the fact that the drain current, see eqn (4.85), can be split up into a forward current I_F, which is a function of V_S, and a reverse current, determined by V_D:

$$I_{DS} = I_F - I_R. \tag{4.86}$$

In the resulting TL loop equations, the triode region operated transistors are not represented by their drain current, but by their reverse current I_R.

Figure 4.29 shows an example of a TL circuit using the topology depicted in Fig. 4.28(a) [65,122]. The floating source terminal is connected to the common-source node of the conventional differential pair. Moreover, this is the ground connection of the loop. Transistors M_1 and M_4 are biased by the input signals I_{in_1} and I_{in_2}, respectively. The drain current of M_2, and M_3, is the output current I_{out}. Translinear analysis of the circuit reveals that I_{out} is given by:

$$I_{out} = \frac{I_{in_1} I_{in_2}}{I_{in_1} + I_{in_2}}. \tag{4.87}$$

Hence, the circuit calculates the harmonic mean of I_{in_1} and I_{in_2}.

An application of the loop depicted in Fig. 4.28(b) is described in Section 8.1.3. The circuit described in [120] is based on the topology shown in Fig. 4.28(c).

Compound transistors

The number of terminals per transistor can effectively be increased using compound transistors. Figure 4.30 depicts a bipolar compound transistor, comprising an anti-series connection of a PNP and an NPN transistor, as well as the

(subthreshold) MOS equivalent. A compound transistor can be regarded as a single equivalent transistor, albeit one with four terminals, which can be used to implement TL loop equations.

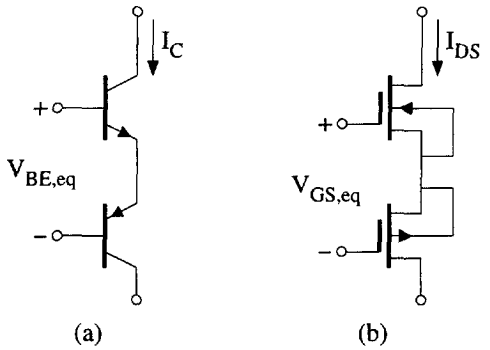

Figure 4.30: Compound transistors: (**a**) bipolar and (**b**) MOS.

The equivalent collector current I_C of a compound bipolar transistor is given by:

$$I_C = \sqrt{I_{s_n} I_{s_p}} \exp \frac{V_{B_n} - V_{B_p}}{2U_T}, \tag{4.88}$$

where I_{s_n} and I_{s_p} are the saturation currents of the NPN and PNP transistor, respectively, and V_{B_n} and V_{B_p} are the base voltages. As a result, the compound transistor can be regarded as a single transistor with an equivalent base-emitter voltage $V_{B_n} - V_{B_p}$, an equivalent saturation current $I_{s_{eq}} = \sqrt{I_{s_n} I_{s_p}}$ and an equivalent thermal voltage $U_{T_{eq}} = 2U_T$.

If the back-gate terminals of both the NMOS and PMOS are connected to the common source, a similar equation can be derived for the subthreshold MOS compound transistor, based on eqn (4.76), which yields:

$$I_{DS} = I_{0_{eq}} \exp \frac{V_{G_n} - V_{G_p}}{n_{eq} U_T}, \tag{4.89}$$

where

$$I_{0_{eq}} = I_{0_n}^{\frac{n_n}{n_{eq}}} I_{0_p}^{\frac{n_p}{n_{eq}}},$$
$$n_{eq} = n_n + n_p,$$

and n_n, n_p and n_{eq} are the NMOS, PMOS and equivalent subthreshold slope factors; I_{0_n}, I_{0_p} and $I_{0_{eq}}$ are the respective zero-bias currents. The equivalent thermal voltage is given by $U_{T_{eq}} = (n_n + n_p)U_T$.

The different equivalent thermal voltage of the compound transistor has no influence on the TL loop equations. However, it does influence eqn (3.24) for the capacitance currents. The capacitance currents are increased by a factor $U_{T_{eq}}/U_T$.

In TL loops comprising compound transistors, two collector terminals per transistor are available for biasing purposes. This represents an increase in the degrees of freedom in comparison with single transistor implementations. In conventional STL circuits, compound transistors have hardly ever been employed due to important disadvantages: the hardware is doubled; the required voltage room is doubled; using lateral PNPs, the frequency performance is severely degraded. In contrast, many DTL circuits comprising compound transistors have been presented in the literature, despite the disadvantages [5, 10]. Some synthesis methods even rely completely on the application of compound transistors [12,89,113]. This is entirely due to the fact that the biasing of DTL circuits is, in general, more complex than the biasing of STL circuits, as explained in Section 4.5.1. If the use of nullors is excluded, some biasing arrangements can only be realised using compound transistors. For example, compare the two differential pairs depicted in Fig. 4.31. To bias the differential pair shown in Fig. 4.31(a), the tail current has to be supplied by a current source. An inconvenient value of this tail current source can frustrate this biasing arrangement. This problem is not encountered for the differential pair shown in Fig. 4.31(b), as both transistors can be biased individually.

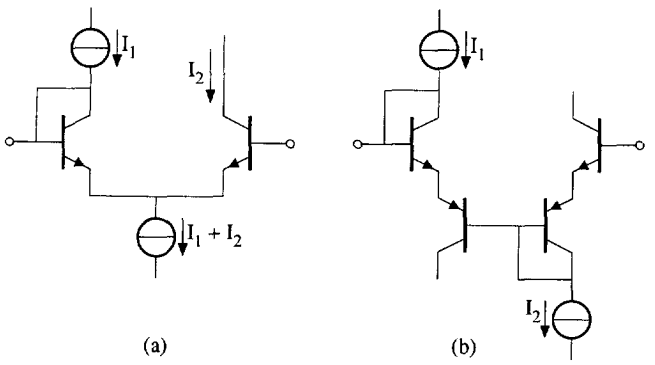

Figure 4.31: Biasing of a differential pair: (**a**) based on single transistors, (**b**) based on compound transistors.

Floating-gate MOS transistors

The multiple-input Floating-Gate MOS (FG-MOS) transistor, depicted in Fig. 4.32, is the 'centipede' of these devices, having lots of terminals. In the sub-

threshold region, the FG-MOS transistor behaves exponentially and can therefore be used to implement TL loops [65, 123].

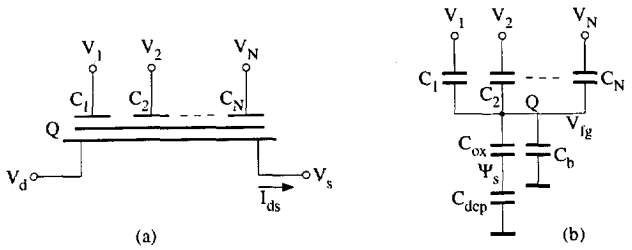

Figure 4.32: A floating-gate MOS transistor: (**a**) symbol and (**b**) capacitive model [65, 123].

The drain current is determined by the floating gate voltage, which is in turn determined by the N gates. The N gate-source voltages V_i are capacitively coupled into the floating gate, as illustrated by the capacitive model shown in Fig. 4.32(b). In the subthreshold region, ignoring parasitic capacitances and other second-order effects, the drain current in the saturation region is given by [123]:

$$I_{\mathrm{DS}} = \lambda I_0 \exp\left(\frac{1}{nU_T}\frac{\sum_{i=1}^{N} C_i V_i}{C_{\mathrm{T}}}\right), \tag{4.90}$$

where n is the subthreshold slope factor, C_i are the gate capacitances, I_0 is zero-bias current and λ accounts for the aspect ratio W/L and for the net charge stored on the floating-gate. The source and back-gate are connected to each other. The capacitance C_{T} equals:

$$C_{\mathrm{T}} = \frac{C_{\mathrm{ox}} C_{\mathrm{c}}}{C_{\mathrm{ox}} + C_{\mathrm{c}}} + \sum_{i=1}^{N} C_i, \tag{4.91}$$

where C_{ox} is the gate-oxide capacitance and C_{c} the capacitance of the bulk.

Since additions in the voltage domain, which are evident from eqn (4.90), are equivalent to powers in the current-domain, these devices can be used to generate powers in TL circuits.

To analyse a TL circuit comprising FG-MOS transistors, it is convenient to rewrite eqn (4.90) into a current-mode expression [65]:

$$I_{\mathrm{DS}} = \lambda \prod_{i=1}^{N} I_i^{1/N}, \tag{4.92}$$

where:

$$I_i = I_0 \exp \frac{C_i V_i}{n C_T U_T}.$$

Equation (4.92) facilitates the current-mode analysis of FG-MOS TL circuits [65]. For example, consider the circuit shown in Fig. 4.33. Nodes ① and ② are associated with the currents I_{n_1} and I_{n_2}, respectively. Hence, the drain currents of M_1, M_2 and M_3 can be written as:

$$I_{ref} = \lambda_1 I_{n_1}, \tag{4.93a}$$

$$I_{in} = \lambda_2 I_{n_1}^{\frac{1}{2}} I_{n_2}^{\frac{1}{2}}, \tag{4.93b}$$

$$I_{out} = \lambda_3 I_{n_1}^{\frac{1}{4}} I_{n_2}^{\frac{3}{4}}. \tag{4.93c}$$

Solving the set of equations for I_{out}, by eliminating I_{n_1} and I_{n_2}, yields:

$$I_{out} = \frac{\sqrt{\lambda_1}\lambda_3}{\lambda_2\sqrt{\lambda_2}} \frac{I_{in}\sqrt{I_{in}}}{\sqrt{I_{ref}}}, \tag{4.94}$$

for $I_{in}, I_{ref} > 0$.

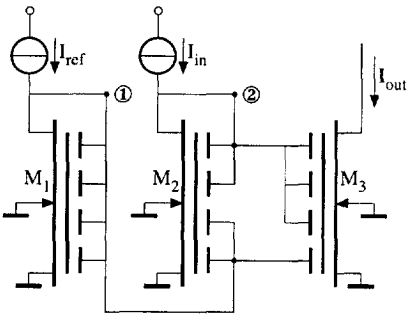

Figure 4.33: A subthreshold floating-gate MOS translinear circuit [123].

It is interesting to note that certain compound transistor structures, combining the voltage-mode additive properties of the FGMOS transistor with the superior exponential characteristics of the bipolar transistor, allow the operation of FGMOS TL circuits at higher current levels and hence at higher frequencies [124].

Non-translinear elements

In some special cases, it can be interesting to insert non-translinear elements into a TL loop. In low-voltage applications, the supply voltage is often made

part of the TL loop, see e.g. [125]. Since a supply voltage is, in general, not PTAT, another voltage source has to track the supply voltage source, so that the remaining net voltage is zero or PTAT. The tracking voltage source can be implemented, e.g., by a resistor biased by an appropriate current.

Resistors can be included in TL loops for yet another reason. If a TL decomposition is insensitive to parasitic resistances, intentional resistors can be added to improve the noise and matching performance. A well-known example is the emitter degeneration applied to a current mirror.

4.6 Alternative synthesis methods for dynamic translinear circuits

As well as the synthesis method for STL and DTL circuits described in Sections 4.1 through 4.5, several alternative synthesis methods for DTL networks have been proposed in the literature.

Frey proposed a synthesis method based on exponential mappings applied to linear state-space descriptions [3]. This method is a generalisation to higher-order filters of the method initially proposed by Adams [1]. Additionally, Frey described a general class of exponential transformations in [10].

Several researchers have proposed the use of component substitution based methods to synthesise TL filters from LC or g_mC prototype filters [6,11,12,126].

Finally, Drakakis *et. al.* proposed a synthesis method based on Bernoulli's DE [14]. Whereas the two former design methods use a *voltage*-mode approach, Drakakis' synthesis method uses a *current*-mode approach, thus emphasising the TL nature of DTL circuits.

As all of these synthesis method yield DTL circuits, they have to be similar to a certain extent. Consequently, it is interesting to make a comparison between the design steps required in each of these methods. In Section 4.6.1, the method described in Sections 4.1–4.5 is compared with the method based on exponential mappings. Likewise, comparisons with the component substitution based methods and the method based on Bernoulli's DE are described in Sections 4.6.2 and 4.6.3, respectively.

4.6.1 Synthesis based on exponential transformations

Synthesis of first-order TL filters based on exponential transformations was introduced by Adams in [1]. Using a state-space approach, Frey was able to generalise this synthesis method to filters of arbitrary order [3]. In addition, Frey generalised this method to allow different exponential-like transformations [4]. This section gives a short overview of the synthesis method based on exponential-like transformations.

Figure 4.34 shows the design trajectory. The starting point is a state-space description of the filter to be realised, see eqn (4.7). The general synthesis theory as proposed in the literature [10] does not incorporate the design of non-linear DTL circuits and this review therefore only deals with the synthesis of linear filters.

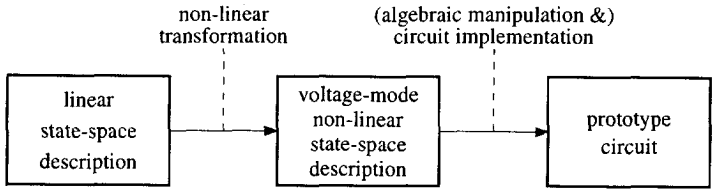

Figure 4.34: Design trajectory of the synthesis method based on exponential transformations.

Instead of the collector currents I_{x_i}, the voltages V_{C_i} across the capacitances C_i are used to represent the state of the filter. To arrive at a voltage-mode state-space description, an exponential-like transformation is applied to the states and to the input signal I_{in}. In general, this transformation is described by:

$$I_{x_k} = f_k(V_{C_k}), \qquad k \in [1, \ldots, n], \tag{4.95a}$$

$$I_{\text{in}} = f(V_{\text{in}}), \tag{4.95b}$$

where the functions f_k and f are strictly monotonous. Different choices can be made for the functions f_k. Those published are [10]:

$$I_{x_k} = I_{\text{st}} \exp \alpha V_{C_k}, \tag{4.96a}$$

$$I_{x_k} = I_{\text{st}} \tanh \tfrac{1}{2}\alpha V_{C_k}, \tag{4.96b}$$

$$I_{x_k} = I_{\text{st}} \sinh \alpha V_{C_k}, \tag{4.96c}$$

where I_{st} and α are constants with dimensions [A] and [V^{-1}], respectively. These three functions comply with the classes of log-domain, tanh and sinh filters, respectively.

The choice of the functions f_k corresponds to the definition of the capacitance currents, described in Section 4.3. Note that the form of f_k, eqn (4.95a), is not as general as the corresponding form of (4.8). Consequently, eqn (4.95a) does not cover the complete class of TL filters.

For log-domain filters, the states I_{x_k} have to be strictly positive at all times. This is accomplished first of all by adding a dc current to I_{in} and restricting the ac input signal swing. The latter limitation is also necessary for tanh filters. However, for an arbitrary state-space description, these measures cannot guarantee the states I_{x_k} are strictly positive at all times. The solution proposed

in [127] is to use another state-space description, which can be obtained through linear transformations, eqn (4.13). An additional option is formed by the introduction of a second dc input current [10]. The latter option is also described in Section 4.3.2, where it is shown that linear state-space transformations are never fundamentally required to solve the problem of negative collector currents I_{x_k}. Hence, *any* state-space description can be used to design a TL filter.

Based on eqns (4.95a) and (4.95b), the next synthesis step is to rewrite the state-space description in terms of V_{C_k} and V_{in}. This yields a non-linear state-space description:

$$C\dot{V}_{C_k} = \sum_{l=1}^{n} \mathbf{a_{kl}} \frac{f(V_l)}{f'(V_k)U_T} + \mathbf{b_k} \frac{f(V_{\text{in}})}{f'(V_k)U_T}, \qquad k \in [1, \ldots, n], \tag{4.97}$$

where $\mathbf{a_{kl}}$ and $\mathbf{b_k}$ represent the elements of the matrices $\mathbf{A}$ and $\mathbf{B}$, and $f'(V_{C_k})$ is the first-order derivative of $f(V_{C_k})$ with respect to V_{C_k}.

Next, eqn (4.97) is interpreted as a set of nodal equations. The LHS of eqn (4.97) equals the current flowing through the capacitance C_i. Each of the terms on the RHS of eqn (4.97) takes the form of a controlled exponential-like transconductance. These controlled transconductances are mapped directly onto a circuit implementation, resulting in the prototype filter circuit. Often, standard building blocks are used to implement eqn (4.97) [4, 10, 12, 90]. For example, E^+, E^-, T, S and $S2$ blocks are introduced in [10]. By comparing the known V-I transfer functions of these building blocks with the terms on the RHS of eqn (4.97), a circuit implementation is derived.

It is sometimes difficult to implement the non-linear transconductance terms directly. Then, it is required to rewrite the RHS of (4.97) using algebraic manipulations [4, 10].

With respect to the synthesis method described in Sections 4.1 through 4.5, mapping the RHS of eqn (4.97) onto a circuit implementation corresponds to both TL decomposition and biasing. Rewriting the RHS of eqn (4.97) corresponds to TL decomposition. An important disadvantage is that transcendental equations have to be manipulated, which is more difficult and hinders clear insight into the behaviour of the circuit designed.

4.6.2 Synthesis based on component substitution

Another approach to the synthesis of TL filters is based on component substitution of prototype LC [12, 15, 89] or g_mC filters [109, 113]. The general idea is to replace elements from a prototype filter by parts of TL loops. Within the general class of TL filters, only methods for the design of log-domain filters have been published.

All of these synthesis methods are based on the set-up depicted in Fig. 4.35, consisting of three essential parts. At the input, a single transistor is used to

compress the input current I_{in}, resulting in a logarithmically related voltage V_{in}. Next, this voltage is filtered by means of a so-called 'log-filter'. The resulting output voltage V_{out} is expanded exponentially, again by a single transistor, into the output current I_{out}.

Figure 4.35: Prevalent log-domain filter set-up.

Most of the design effort goes into the design of a 'log-integrator'. Basically, the first-order building blocks to be designed are an inverting and a non-inverting integrator, which are then used as substitutes for the integrator elements in the signal-flow graph. Within a higher-order filter network, the internal compression and expansion stages of the first-order building blocks cancel, and hence, these can be omitted [89], leaving only a single compression stage at the input and an expansion stage at the output of the complete filter. Linear losses, i.e. resistances, can simply be implemented by a dc current source in parallel with a capacitor, as explained in Section 3.3.1.

Application of these component substitution based design methods is simple. Yet, an important disadvantage seems that the designer cannot make any choices along the synthesis path. In general, for each LC or g_mC prototype filter, exactly one TL filter results. Therefore, the applicability of these methods is restricted.

4.6.3 Synthesis based on Bernoulli's differential equation

The synthesis method for log-domain filters proposed in [14] is based on the generic circuit structure shown in Fig. 3.12. The analysis of the structure has shown that it is described by the state-space description (3.51). To synthesise a TL filter, eqn (3.51) is simply compared with a state-space description of the filter to be realised. This yields the necessary form of the currents I_{u_k}. The task of the designer is to find ways to generate the currents I_{u_k} using conventional TL techniques.

In comparison with the synthesis theory outlined in Sections 4.1–4.5, the method proposed in [14] starts with the TL decomposition and hardware implementation of a part of the TL filter circuit, i.e., the structure depicted in Fig. 3.12. This sub-circuit implicitly 'defines' the capacitance currents as well. Next, the generation of the currents I_{u_k} corresponds to the design stages of TL decomposition and hardware implementation. A disadvantage of the method

described in [14] is that it introduces restrictions that are not fundamental. These restrictions arise from the choice for the sub-circuit depicted in Fig. 3.12. In addition, the method is limited to the design of log-domain filters.

4.7 Class-AB operation

Parallel signal processing arrangements can yield very elegant analogue circuit solutions in many situations. Some examples are differential filters, multi-path op amp implementations [128], full-flash or folding analogue-to-digital converters [129], multi-tanh transconductance cells [130, 131] and analogue VLSI neural networks [65, 66]. In the area of TL circuits, class-AB operation is another example of parallel processing, which enables the signal currents to be much larger than the dc quiescent currents. This, in turn, entails a larger dynamic range and a reduced average current consumption. The price paid is often an increase in circuit complexity.[8]

Generic class-AB set-up

Figure 3.18 shows a general set-up for class-AB operation [91]. In this set-up, a current splitter is used at the input to divide the input current I_{in} into two currents I_{in_1} and I_{in_2}, which are both strictly positive. These signals are related to I_{in} by:

$$I_{\text{in}} = I_{\text{in}_1} - I_{\text{in}_2}. \tag{4.98}$$

The two parts of the input signal are now processed by two separate signal paths, denoted by F_1 and F_2. The resulting output currents I_{out_1} and I_{out_2} are subtracted to obtain the overall output current I_{out}.

In TL circuits operated in class A, the signal current swings are limited directly by some dc bias currents. However, this restriction being single-sided only in many (but not all) TL circuits, asymmetrical wave forms can advantageously be processed. This fact is exploited in class-AB operated circuits. The current splitter, shown in Fig. 3.18, generates two asymmetrical output currents I_{in_1} and I_{in_2}, both strictly positive. On condition that the two signal paths F_1 and F_2 can process signals in the range $< 0, \infty >$, the dynamic range of the class-AB set-up is theoretically infinite.

In general, there are several possibilities for defining the two functions F_1 and F_2. Naturally, the restriction is that the overall transfer function of the system equals the desired input-output transfer function. For linear transfer

[8] Note though that class-AB processing is not restricted to genuine TL circuits. Interesting examples of non-TL forms of class-AB operation are also found in the area of conventional filter implementation techniques [81, 132].

functions F, a very simple solution is to choose F_1 and F_2 equal to F [91]. This choice is possible both for static and dynamic linear transfer functions.

Static translinear circuits

For STL circuits, class-AB operation is simply a special kind of parametric TL decomposition. Strangely enough, in the past class-AB operation has never been widely used for the realisation of STL circuits. Only a limited number of examples, such as op amp output stages, or class-AB current mirrors [133] can be found in the literature. Nonetheless, class-AB operation can yield very elegant and interesting circuit solutions for STL circuits. As an example, Fig. 4.36 shows a four-quadrant multiplier comprising four one-quadrant multipliers and operated in class AB by means of two input current splitters.

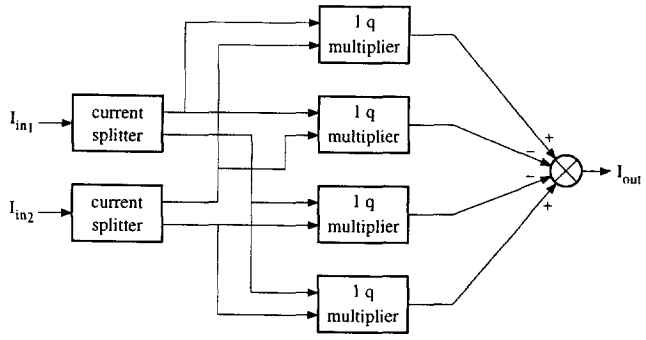

Figure 4.36: A class-AB four-quadrant multiplier.

Dynamic translinear circuits

An interesting example of class-AB operation in DTL circuits is formed by the integrator depicted in Fig. 4.37 [2]. In this circuit, the two signal paths are both described by non-linear DEs:

$$CU_T\dot{I}_{\text{out}_1} + I_{\text{out}_1}I_{\text{out}_2} = I_0 I_{\text{in}_1}, \tag{4.99a}$$

$$CU_T\dot{I}_{\text{out}_2} + I_{\text{out}_1}I_{\text{out}_2} = I_0 I_{\text{in}_2}, \tag{4.99b}$$

where $C_1 = C_2 = C$, $I_{\text{out}} = I_{\text{out}_1} - I_{\text{out}_2}$ and $I_{\text{in}} = I_{\text{in}_1} - I_{\text{in}_2}$. Clearly, subtraction of eqns (4.99a) and (4.99b) results in the DE describing a linear integrator, see (3.36).

The two signal paths F_1 and F_2 comprising the integrator exhibit interaction due to the non-linear term $I_{\text{out}_1}I_{\text{out}_2}$ in eqns (4.99a) and (4.99b). This product results from the subtraction of a current I_{out_1} from the capacitance current I_{C_2}

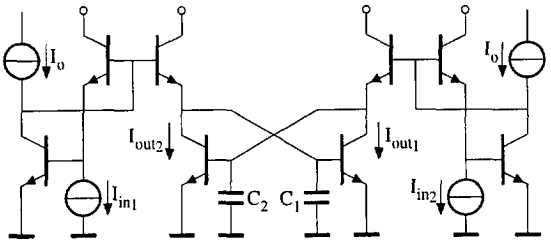

Figure 4.37: A class-AB translinear integrator [2].

and I_{out_2} from I_{C_1}. These subtractions have been implemented to obtain strictly positive collector currents. To verify this for a given input signal, it is necessary to revert to numerical investigations as the wave forms of I_{out_1} and I_{out_2} result from non-linear DEs.

Current splitters

Several equations can be applied to implement the input current splitter function in the class-AB set-up shown in Fig. 3.18. Three different current splitter functions have been proposed in the literature: the class B current splitter, the splitter based on a constant geometric mean and the splitter based on a constant harmonic mean.

The two output currents $I_{in_{1,2}}$ of a class B current splitter are given by:

$$\begin{cases} I_{in_1} = I_{in}, & I_{in_2} = 0, & \text{for } I_{in} \geq 0, \\ I_{in_1} = 0, & I_{in_2} = -I_{in}, & \text{for } I_{in} < 0. \end{cases} \tag{4.100}$$

The relation between the actual input current I_{in} and $I_{in_{1,2}}$ is illustrated in Fig. 4.38. All currents are normalised with respect to a dc current I_{dc}. For reference, the situation of class-A operation is also depicted.

An important disadvantage of class B operation is that one of the currents $I_{in_{1,2}}$ is always zero. This results in a turn-on delay and distortion during the zero-crossings of I_{in}. The class B splitter is even less suitable for DTL circuits, as the resulting capacitance currents can become quite large, as suggested by Fig. 3.26.

The geometric mean control law, or product law, is used more often to implement the current splitter. This control law forces the currents I_{in_1} and I_{in_2} to have a constant geometric mean, equal to I_{dc}. That is:

$$I_{dc}^2 = I_{in_1} I_{in_2}. \tag{4.101}$$

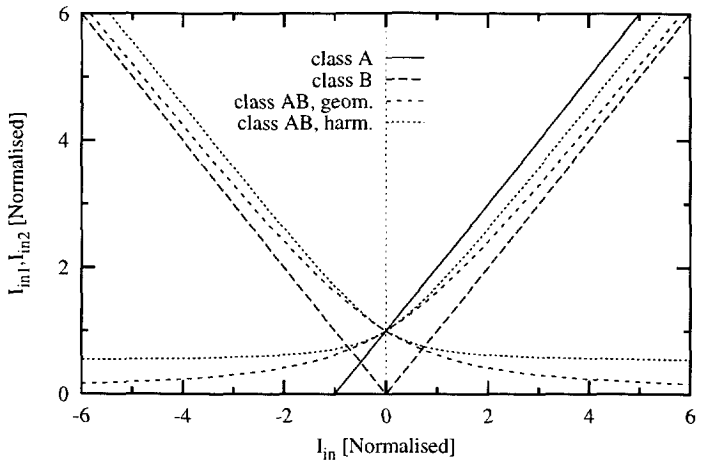

Figure 4.38: The currents resulting from different current splitters.

Using the geometric mean control, the two currents $I_{\text{in}_{1,2}}$, given by:

$$I_{\text{in}_{1,2}} = \tfrac{1}{2}\left(\sqrt{4I_{\text{dc}}^2 + I_{\text{in}}^2} \pm I_{\text{in}}\right), \tag{4.102}$$

are never turned off completely, as illustrated in Fig. 4.38.

An even better alternative is an implementation based on the harmonic mean function [55]:

$$I_{\text{dc}}\left(I_{\text{in}_1} + I_{\text{in}_2}\right) = 2I_{\text{in}_1} I_{\text{in}_2}, \tag{4.103}$$

which forces $I_{\text{in}_{1,2}}$ to have a constant harmonic mean equal to I_{dc}. Just like eqn (4.101), (4.103) is already a valid TL decomposition. In an implementation of this TL loop equation, the transistors conducting $I_{\text{in}_{1,2}}$, which are given by:

$$I_{\text{in}_{1,2}} = \tfrac{1}{2}\left(\sqrt{I_{\text{dc}}^2 + I_{\text{in}}^2} + I_{\text{dc}} \pm I_{\text{in}}\right), \tag{4.104}$$

are always biased at a minimum current $\frac{1}{2}I_{\text{dc}}$, as illustrated in Fig. 4.38. Consequently, the transit frequency f_{T} of these transistors does not tend to zero for large signal swings, which reduces an important source of distortion in class-AB circuits.

5

Device non-idealities

The analysis and synthesis methods discussed in the previous chapters are based on the exact exponential behaviour of the circuit elements. Nonetheless, many second-order effects influence the accuracy of a TransLinear (TL) circuit and in general result in distortion. Fortunately, many techniques have been developed in the past to overcome these problems. For example, this is demonstrated by the TL multiplier reported in [49], which provides a total harmonic distortion level of -95 dB.

This chapter discusses the second-order effects associated with the bipolar and the MOS transistor and gives an overview of methods for reducing the influence of these device non-idealities. The discussion in this chapter is limited to circuit level techniques. The designer should be aware, however, that very elegant solutions can often be found at the system level. A well-known example is the use of differential operation, which results in a significant reduction of even-order distortion components.

The most important error sources in bipolar designs are the finite current gain and the parasitic base and emitter resistances associated with the bipolar transistor. These error sources are discussed in Sections 5.1 and 5.2, respectively. The body effect, which is discussed in Section 5.3, is an error source in subthreshold MOS designs. The next three second-order effects discussed in this chapter apply both to the bipolar and the subthreshold MOS transistor. In Section 5.4, the Early effect is discussed. Next, the influence of parasitic capacitances is treated in Section 5.5. Finally, device mismatches are the topic of Section 5.6.

5.1 Base currents

The finite current gain of the bipolar transistor is one of the major error sources in TL circuits; especially in networks exhibiting large differences in the collector current levels, such as class-AB operated circuits or high-gain TL amplifiers. In general, without the application of appropriate measures, the finite current gain reduces the useful current range from approximately eight to only one or two decades of collector current. However, the exact nature of B_F-induced deviations strongly depends on the topology of the TL loop, the TL loop equation and the specific biasing arrangement.

In this respect, subthreshold MOS designs obviously have a fundamental advantage over bipolar designs, as the gate current of the MOS transistor is negligible at low frequencies. Likewise, in BiCMOS designs, current mirrors and nullor implementations can be implemented beneficially using MOS transistors, while bipolar transistors are used to implement the TL loops [9].

The finite base current I_B of the bipolar transistor is modelled by the current gain factor B_F:

$$I_B = \frac{I_C}{B_F}, \tag{5.1}$$

where I_C is the collector current. In modern IC processes, B_F is relatively constant over many decades of current. This is illustrated by Fig. 5.1, showing a measurement of the Gummel plot for a minimum-sized NPN transistor in the DIMES02 process, and Fig. 5.2 showing the corresponding plot of B_F versus I_C. The temperature-dependence of B_F is small and has a negligible influence in most TL circuit designs [50]. The matching of B_F between adjacent devices is generally better than $\pm$ 5% [61].

The analysis of the influence of finite base currents is straightforward. The base current directly fits into the current-mode analysis methods discussed in Chapter 3. The analysis can often be simplified using the assumption that B_F is equal for all transistors. For Static TransLinear (STL) circuits, the distortion can be examined analytically. In case of Dynamic TransLinear (DTL) circuits, large-signal analysis frequently results in a non-linear Differential Equation (DE), and a numerical approach is therefore often the only remaining option to gain insight.

Several techniques can be applied to reduce the influence of finite B_F. A well-known method is compensation, which is illustrated in Fig. 5.3. This method relies on the matching properties of B_F. Transistor Q_2 senses the collector current of Q_1. The base current of Q_2 is fed back to the base of Q_1 by means of a current mirror and approximately compensates the base current of Q_1. Especially the bandwidth of the PNP current mirror is of crucial importance for this technique to work at high frequencies.

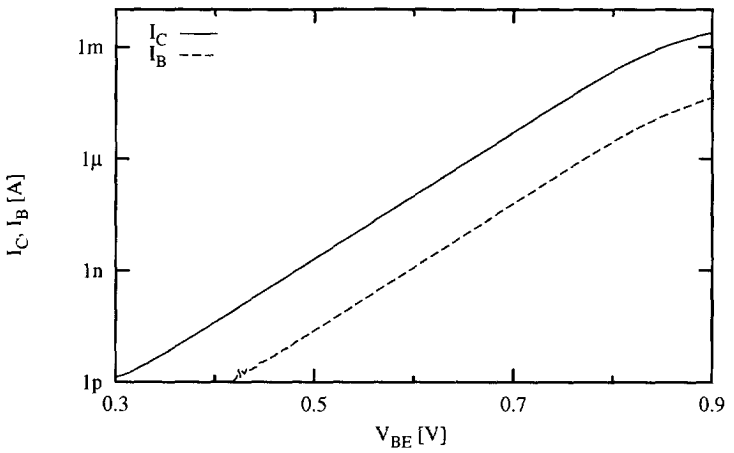

Figure 5.1: Gummel plot of a minimum-sized NPN transistor.

For some TL circuit structures, depending on the specific TL decomposition implemented, compensation by means of small independent dc current sources is possible [50]. A major advantage over the aforementioned methods is the wide-band character of this technique.

Finally, a generally applicable technique is the use of nullors to provide the base currents, which is described in Section 4.5.1.

5.2 Parasitic resistances

At the upper end of the collector current range, the validity of the exponential law is deteriorated by the parasitic base resistance R_B and the emitter resistance R_E. The resulting deviations increase exponentially as a function of the collector current. Hence, these parasitic resistances can easily become the dominant error sources and introduce gross distortion. For small transistors, typical values of R_E and R_B are in the region of some ohms and some hundreds of ohms, respectively. In addition, the parasitic collector resistance can sometimes cause saturation of the bipolar transistor at high current levels [50].

To analyse the effect of R_B and R_E, an equivalent resistance R'_E in the emitter lead can be used [40, 50, 134]:

$$R'_E = R_E + \frac{R_B}{B_F}. \tag{5.2}$$

This simplified equation assumes constant values of B_F, R_E and R_B. For a single transistor, the influence of R'_E on the base-emitter voltage is negligible when

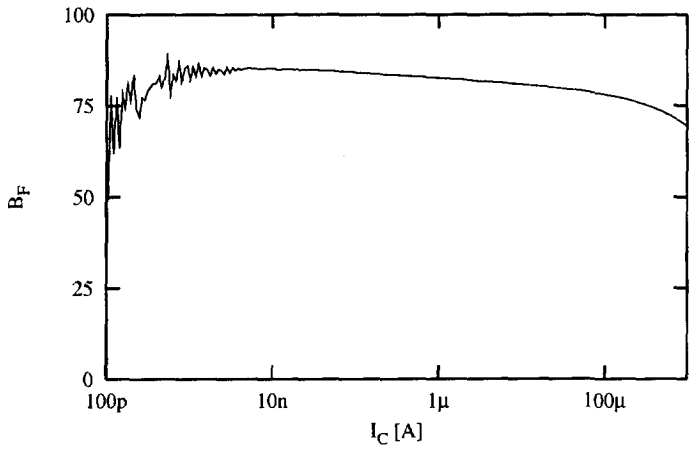

Figure 5.2: Current gain factor as a function of the collector current.

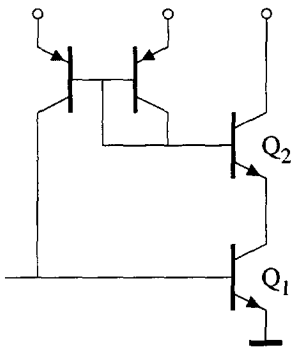

Figure 5.3: Base current compensation.

$I_C \ll U_T/R'_E$. Using large transistors, this condition can always be accomplished. However, the use of large transistors to prevent R'_E-induced distortion often conflicts with high-frequency demands.

In subthreshold MOS TL circuits, parasitic resistances are not an issue due to the low current levels employed.

In a TL circuit, the effect of R'_E is determined by the contribution of all transistors comprising the loop. The emitter and base resistances scale in inverse proportion to the emitter area λ_i. The TL loop equation, including the influence of R'_E, is thus given by:

$$\frac{\prod_i \lambda_{2i} I_{2i}}{\prod_i \lambda_{2i-1} I_{2i-1}} = \exp \frac{\left(\sum_i \frac{I_{2i-1}}{\lambda_{2i-1}} - \sum_i \frac{I_{2i}}{\lambda_{2i}}\right) R'_E}{U_T}. \tag{5.3}$$

By definition, eqn (5.3) can be written as:

$$\lambda \frac{\prod_i I_{2i}}{\prod_i I_{2i-1}} = \exp \frac{\Delta I R'_{\mathrm{E}}}{U_T}, \tag{5.4}$$

where λ is the area ratio $\prod_i \lambda_{2i} / \prod_i \lambda_{2i-1}$ of the TL loop. Equation (5.4) is transcendental, which frustrates the analysis. However, if $\Delta I R'_{\mathrm{E}} \ll U_T$, a first-order Taylor approximation yields a more accessible expression:

$$\lambda \frac{\prod_i I_{2i}}{\prod_i I_{2i-1}} = 1 + \frac{\Delta I R'_{\mathrm{E}}}{U_T}. \tag{5.5}$$

To a certain extent, the exact deviations introduced by R'_{E} depend on the TL decomposition implemented. For some TL loop equations, the voltage drops over the parasitic resistances are even cancelled out completely. A trivial example is a current mirror with emitter degeneration resistors. A second example is eqn (4.103), which implements a harmonic mean current splitter. For this circuit, ΔI amounts to I_{dc} assuming equally-sized transistors. Hence, only the quiescent current is affected, but the two output currents I_{out1} and I_{out2} are not distorted. A final example, is the 'six-pack' four-quadrant multiplier, depicted in Fig. 4.16 [45].

In a TL circuit, the individual emitter areas λ_i of the transistors are not important; only the area ratios of the complete loops comprising the circuit are found back in the transfer function of the circuit. This fact provides some freedom with respect to the scaling of the individual emitter areas. Different values can result in the same λ, and hence do not influence the Left-Hand Side (LHS) of eqn (5.3). Nevertheless, they do influence the error term on the Right-Hand Side (RHS) of eqn (5.3). A proper choice of the individual λ_i values can minimise ΔI across the input signal range [56].

Using other circuit techniques, the influence of R'_{E} can even be eliminated in a theoretically exact fashion. A possible method is described by Schmook in [48]. A resistance R_{e}, equal to R'_{E}, is introduced in the loop and biased by the current ΔI. As a result, the voltage drops across R_{e} and R'_{E} cancel exactly. It is important that R_{e} tracks R'_{E} over wide variations of temperature and IC process variables.

An alternative method, reported by Opris in [134], uses three transistors to emulate a single transistor with zero emitter-resistance. The principle is illustrated in Fig. 5.4. The voltage drops across the three emitter resistances cancel exactly. The equivalent base-emitter voltage $V_{\mathrm{BE,eq}}$ equals:

$$V_{\mathrm{BE,eq}} = U_T \ln \frac{I_{\mathrm{C}}}{4 I_{\mathrm{s}}}. \tag{5.6}$$

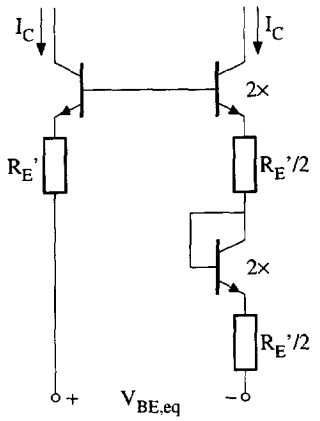

Figure 5.4: Emulation of a single transistor with zero emitter-resistance [134].

Dynamic translinear circuits

Next to the TL loops, the capacitance-junction(s) loops in DTL circuits are affected as well by R'_{E}. For example, for the log-domain output stage, the distorted capacitance current I_{cap} is given by:

$$I_{\mathrm{cap}} = C\dot{I}_{\mathrm{C}}\left(\frac{U_T}{I_{\mathrm{C}}} + \frac{1}{R'_{\mathrm{E}}}\right). \tag{5.7}$$

Both the methods of Schmook [48] and Opris [134] can be used to eliminate R'_{E}-induced errors in the capacitance-junction(s) loops.

5.3 Body effect

In the subthreshold region, the drain current I_{DS} of the MOS transistor approximately exhibits an exponential relation with respect to the gate voltage V_{G}. A measurement of the V_{G} versus $\ln I_{\mathrm{DS}}$ plot is shown in Fig. 5.5. The measurement shows that the MOS transistor is approximately exponential across 3 to 4 decades of drain current. In the measurement, the source voltage V_{S} and the back-gate voltage V_{B} are fixed. The dimensions of the measured transistor, from a 2 μm CMOS process, are $W = 108$ μm/μm and $L = 7$ μm/μm.

Often the drain current is approximated by a pure exponential model, see eqn (4.76). However, even when the MOS transistor is operated well below the moderate inversion region, it only behaves approximately exponentially. Therefore, some attention has to be paid to the differences in large signal behaviour between the bipolar and the weak inversion MOS transistor.

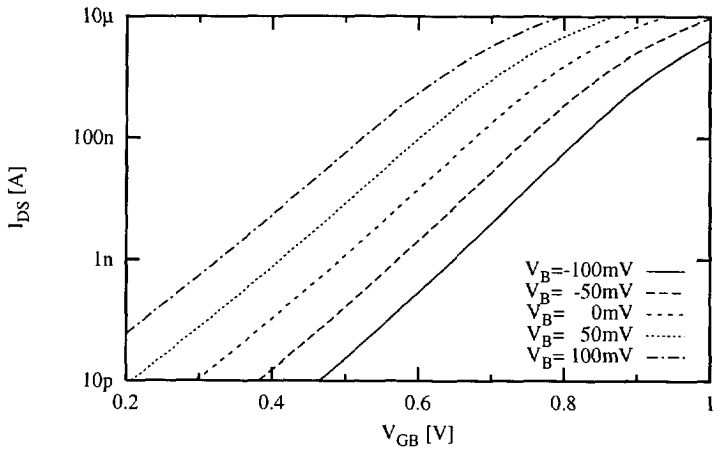

Figure 5.5: Measurement of the drain current as a function of the gate voltage.

The derivative of the V_G-ln I_{DS} plot is often modelled by $1/n$, where n is the subthreshold slope factor. Figure 5.6 shows a measurement of $1/n$ for different values of V_B. The figure shows that it is only approximately constant, even within the subthreshold region. However, in general, the distortion introduced by this body effect is overshadowed by the deviations resulting from the poor matching characteristics of the MOS transistors in the weak inversion region. For reference, Fig. 5.7 depicts a measurement of the normalised derivative of the V_{BE}-ln I_C relation, corresponding to Fig. 5.1. A comparison of Figs 5.6 and 5.7 furthermore shows that the slope of the V_{GS}-ln I_{DS} plot is less steep than the slope of the V_{BE}-ln I_C plot.

In a more complex subthreshold MOS model, the slope factor is weakly dependent on the gate-bulk voltage V_{GB}. When a positive gate-bulk voltage V_{GB} is applied to an n-channel MOS transistor, a positive charge $-Q_C$ accumulates on the gate. This charge is balanced by a negative charge Q_C in the substrate. The substrate charge can be divided into the depletion charge Q_B, resulting from ionised acceptor atoms, and the inversion charge Q_I, resulting from free electronics in a thin layer close to the oxide-silicon interface. In subthreshold, the surface channel potential ψ_s, found at the oxide-semiconductor interface, is constant along the channel due to the fact that $Q_I \ll Q_B$ [135]. The drain current, which results from a diffusion process, is determined by the difference of the inversion charge at the source and the inversion charge at the drain. These inversion charges are (exactly) exponentially related to the voltage differences $V_S - \psi_s$ and $V_D - \psi_s$, respectively. Due to the negligible influence of Q_I, the voltage ψ_s can be said to be generated by the capacitive voltage divider formed by the oxide capacitance C_{ox} and the bulk semiconductor capacitance

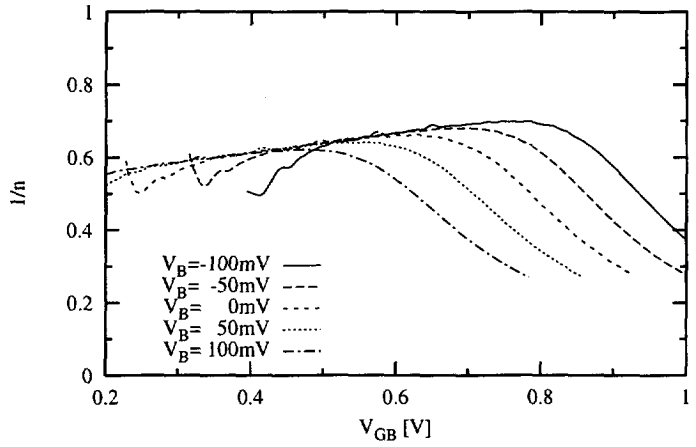

Figure 5.6: Measurement of the subthreshold slope factor.

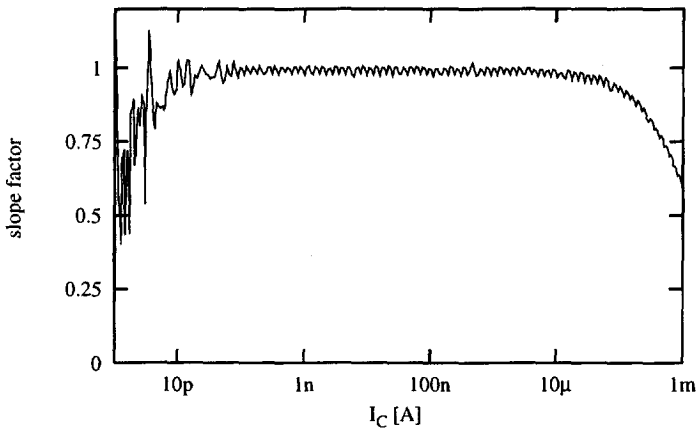

Figure 5.7: Measurement of the normalised derivative of the V_{BE}-ln I_C relation of a bipolar transistor.

C_c. Consequently, deep in weak inversion, the subthreshold slope factor is given by [117, 136]:

$$\frac{1}{n} = \frac{C_{ox}}{C_{ox} + C_c}, \tag{5.8}$$

$$= 1 - \frac{\gamma/2}{\sqrt{\gamma^2/4 + V_{GB} - V_{FB} - U_T}}, \tag{5.9}$$

where V_{FB} is the flat band voltage. The slope factor of the back-gate is given by $(1 - 1/n)$. An intuitive, though physically not completely correct model of the subthreshold MOS transistor is depicted in Fig. 5.8, illustrating that the weak inversion MOS transistor is a 'bipolar transistor in disguise' [137]. A zero base current is assumed for the bipolar transistor.

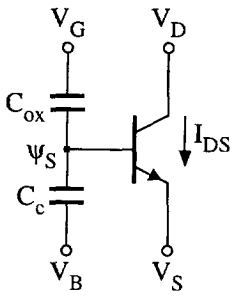

Figure 5.8: Intuitive model of the subthreshold MOS transistor.

By integration of eqn (5.9) with respect to V_{GB}, a more accurate expression than (4.76) can be obtained for I_{DS}:

$$I_{DS} = I_0 \exp \frac{V_{GB} - \gamma\sqrt{\gamma^2/4 + V_{GB} - V_{FB} - U_T}}{U_T} \exp \frac{V_{BS}}{U_T}, \tag{5.10}$$

where I_0 is the integration constant introduced.

The subthreshold slope factor n does not vary strongly with V_{GB} and the voltage swings in a TL circuit are small. Nonetheless, the factor n is present in the argument of an exponential function. Hence, even a small difference in n between transistors in a TL loop can result in significant deviations over the entire input signal range. Manual calculations are difficult due to the voltage-mode dependence of n. This results in transcendental equations. Unfortunately, simulation might be a problem as well, since most circuit simulators simply model the weak inversion region by an exact exponential function [138].

Folded topologies

Fortunately, some TL topologies are fundamentally insensitive to the body effect. Equation (5.9) shows that in the weak inversion region the subthreshold slope factor n is only dependent on the voltage V_{GB}. The exact dependence is different for devices with ion implantation, but the V_{GB} dependence and V_S independence are preserved [117]. Due to this fact, the body effect can be eliminated completely by choosing the right TL topologies. Figure 5.9 shows combinations of two transistors with equal V_{GB} voltages. At the unconnected source and drain terminals, these structures provide an exact exponential relation, equal to the exponential law of the bipolar transistor. This is due to the equal V_{GB} voltage and hence the equal subthreshold slope factor n of the devices. Using the structures shown in Fig. 5.9 to construct complete TL loops results in body effect independent topologies. Necessarily, these are all folded loops, which complies very well with low-voltage operation. Figure 5.10 shows some possible second-order TL loops. Note that the back-gate voltages of the two parts of each loop do not have to be equal.

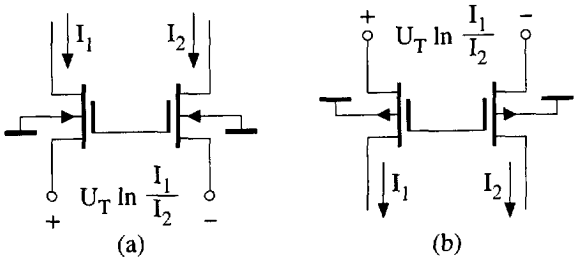

Figure 5.9: Body effect independent structures.

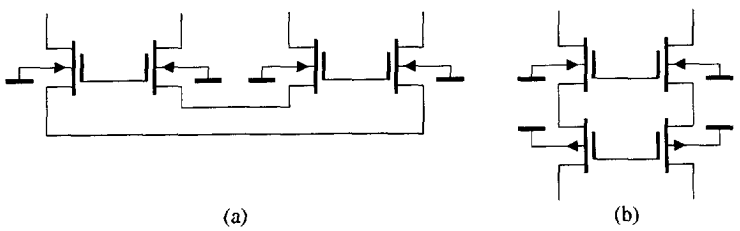

Figure 5.10: Body effect independent translinear loops.

In contrast, all stacked TL topologies are vulnerable to the body effect. In these loops, the body effect can be minimised by connecting the back-gate of each transistor to its source. This however has a frequency penalty due to the well capacitance. If two transistors have the same gate potential, the

back-gates can both be connected to the source of only one transistor. This might be interesting for DTL circuits if the back-gates can be connected to a node where an intended capacitor is already present. A final alternative is to connect the back-gates to a bias voltage, generated by diode-connected and dc biased transistors. Nevertheless, these methods are not fundamentally exact and distortion analysis is difficult for the reasons given above.

Capacitance currents

In DTL circuits, the subthreshold slope factor influences the capacitance currents as well. The three different subthreshold slope factors for the gate, the back-gate, the source, and/or the drain determine the equivalent thermal voltage $U_{T,\mathrm{eq}}$ in eqn (3.24). The capacitance current is process-independent and $U_{T,\mathrm{eq}}$ equals U_T only when a capacitor is connected to a source or drain terminal.

5.4 Early effect

The collector current of the bipolar transistor is influenced by base-width modulation; the Early effect. Owing to the small voltage swings, the influence of the Early effect is relatively small in TL circuits.

The Early effect is modelled by the forward and reverse Early voltages, denoted by V_{AF} and V_{AR}, respectively [139]:

$$I_{\mathrm{C}} = I_{\mathrm{s}} \left(1 - \frac{V_{\mathrm{BC}}}{V_{\mathrm{AF}}} - \frac{V_{\mathrm{BE}}}{V_{\mathrm{AR}}}\right) \exp \frac{V_{\mathrm{BE}}}{U_T}. \tag{5.11}$$

A similar equation is often used to model channel-length modulation for subthreshold MOS transistors.

Typical values of V_{AF} for high-frequency transistors are in the range of 5 to 50 V [61]; V_{AR} takes on values in the order of several volts [139]. The Early voltage is essentially independent of temperature [61].

For the moment assuming that the effect of V_{AR} is negligible, the effect of V_{AF} on a TL loop is described by:

$$\frac{\prod_i I_{2i}}{\prod_i I_{2i-1}} = \lambda \frac{\prod_i \left(1 - \frac{V_{\mathrm{BC},2i-1}}{V_{\mathrm{AF}}}\right)}{\prod_i \left(1 - \frac{V_{\mathrm{BC},2i}}{V_{\mathrm{AF}}}\right)}. \tag{5.12}$$

Equation (5.12) reveals that V_{AF} results in a modulation of the area factor λ. Pair-wise matching of the V_{BC} voltages is the most obvious solution to counteract the Early effect. Nullor implementations can be used to accomplish this. However, exact pair-wise matching cannot always be (easily) achieved.

For small values of the collector-base voltages, with respect to V_{AF}, the condition of exact pairs-wise matching can be relaxed as eqn (5.12) can be approximated by [50]:

$$\frac{\prod_i I_{2i}}{\prod_i I_{2i-1}} = \lambda \left[1 - \frac{1}{V_{AF}} \left(\sum_i V_{BC2i-1} - \sum_i V_{BC_{2i}} \right) \right]. \tag{5.13}$$

Hence, the influence of V_{AF} is minimised if the sums of the V_{BC} voltages in both directions of the loop are made equal.

The modulation of λ can be divided into a dc term and an ac term. In TL circuits, the voltage swings are often very small. Of course, considerable care has to be taken if the output consists of a resistive load. Due to the small voltage swings, the ac modulation of λ is often negligible. For example, a voltage swing of 50 mV of V_{BC} is required for 1% ac modulation of λ for $V_{AF} = 5$ V. This translates into a current swing of a factor of 6.8. Hence, the ac part of the Early effect is only important for high-precision applications. The effect of the dc part of the modulation of λ is similar to the effect of mismatch. The exact influence of a mismatch of λ on the transfer function of the TL circuit depends very much on the specific TL loop equation employed.

The reverse Early voltage V_{AR} is typically lower than V_{AF}. As the V_{BE} voltage swings are small, the modulation of λ can be approximated by eqn (5.13), exchanging V_{BC} by V_{BE} and V_{AF} by V_{AR}. Since a TL circuit, by definition, comprises closed loops of base-emitter junctions, the sum of V_{BE} voltages in both directions of the loop are always exactly equal. Hence, the effect of V_{AR} is nearly always negligible.

5.5 Parasitic capacitances

Translinear circuits operate at fundamentally the lowest impedance possible at a given bias current level. This low-impedance characteristic facilitates high-frequency operation, see, e.g., [24,44], and an almost complete freedom of slew-rate limitations [61]. Further, due to the small voltage gains in TL circuits, the Miller effect with respect to the base-collector capacitance C_μ is small [50,61]. However, operation of TL circuits not well below the f_T frequency can easily give rise to significant distortion.

As the parasitic capacitances of the transistors comprising a TL loop influence the bandwidth, the relative bandwidth of the circuit is optimised when the transistors have the same value of f_T [50]. This is accomplished by biasing the transistors at equal current densities. Obviously, the lateral PNP transistor is a harmful dissonant. It goes without saying that the availability of a complementary-bipolar process constitutes an important advantage. This is especially true for low-voltage (< 1 V), class-AB operated circuits, in which PNP

current mirrors, which require stacked TL loops [140, 141], cannot be applied and class-A biased NPN mirrors are also not an alternative.

In an absolute sense, the bandwidth is optimised by biasing the transistors at high current levels. Unfortunately, the accuracy of the exponential relation deteriorates in this biasing range due to the parasitic base and emitter resistance. Consequently, the design of TL circuits with a high absolute bandwidth is a serious challenge. Note that the exponential behaviour is not important for transistors outside the TL loops. Consequently, these transistors can be biased at higher current densities, and hence a higher f_T, than the transistors comprising the actual TL loop. As a result, amplifiers can often be used beneficially to buffer (some of) the parasitic capacitances of the TL core.

In MOS technology, subthreshold operation of the transistors is restricted to low current levels. Since the f_T is low at low current levels, application of subthreshold MOS TL circuits is necessarily restricted to low-frequency applications.

Analysis

In principle, the general analysis method presented in Section 3.2.1 can be used to calculate the influence of the parasitic capacitances. The voltage-dependence of the junction capacitances is negligible due to the small voltage swings. The signal dependence of the diffusion capacitance is easily accommodated in the analysis method.

Nevertheless, the merits of large-signal analysis methods with respect to parasitic capacitances are small. In general, the analyses result in non-linear DEs, see, e.g., eqn (2.16) for the current mirror. This hampers insight and is not very useful for design purposes. Hence, small-signal and numerical analyses are better alternatives to gain insight into the influence of parasitic capacitances. Further, methods are being studied to analyse the behaviour of non-linear dynamic circuits using a linear time-varying approach [142, 143].

In DTL circuits, those parasitic capacitances connected in parallel with the intended capacitor do not significantly influence the circuit operation. In fact, it has even been proposed to use parasitic capacitances as the effective capacitances in DTL circuits [19, 144]. However, in practice, this method results in a large spread of the absolute capacitance values and can only be used when appropriate tuning circuits are used.

5.6 Mismatch

Mismatch is an important and often dominant source of errors in TL circuits. The mismatch of the bipolar transistor can be modelled by a mismatch of the saturation current I_s. Typically, values of I_s match within 1% [61]. The MOS

transistor suffers from two sources of mismatch: mismatch of the threshold voltage V_{th} and of the transconductance factor β, which are almost uncorrelated in practice [145]. Due to the (approximately) exponential behaviour in the weak inversion region, both effects can be modelled as a mismatch of the zero-bias current I_0 [146, 147].

In general, the matching properties of MOS transistors are inferior to those of bipolar transistors. This is a major disadvantage of subthreshold MOS TL circuits. Typical values of 2 to 4% mismatch are reported for 20/20 μm/μm NMOS devices, scaling inversely proportional to the square-root of the transistor area [146–148]. The matching of PMOS devices is generally worse due to the additional threshold adjust implant [145]. Fortunately, since V_{th} mismatch decreases for thinner gate oxide [148], it can be expected that the matching properties of MOS devices will improve in the future.

In the weak inversion region, the V_{th}-mismatch is dominant [147]. This can be exploited in MOS current mirrors by operating the transistors in the moderate or strong inversion region to minimise the current mirror mismatch [149].

In TL circuits, the matching of all transistors comprising the loops is relevant. The total mismatch can be modelled by a mismatch of the area ratio λ. Optimum matching can be achieved by following the well-known rules summarised in Table 5.1 [150]. The common-centroid arrangement also effectively reduces the effect of mismatch caused by thermal gradients on the chip [50].

Table 5.1: Rules for optimum matching [150].

Same structure
Same temperature
Same shape, same size
Minimum distance
Common-centroid geometries
Same orientation
Same surroundings
Non-minimum size

The effect of mismatch on the transfer function of a TL circuit depends on the particular TL decomposition used. This criterion can be used to select those TL decompositions that are least sensitive to variations of λ, or for which mismatch does not result in harmonic distortion, but, e.g., in scaling errors.

It is interesting to note that transistor mismatch does not influence the expressions for the capacitance currents, see eqn (3.24).

For high-precision applications, the measures summarised in Table 5.1 are not sufficient and the only option left at circuit level is trimming. Elimination

of mismatch across a wide temperature range is accomplished by trimming a PTAT voltage source connected in series in the TL loop. This PTAT source can be approximated by an aluminium resistor biased at a temperature-stable current [61]. Highly specialised trimming methods are required to obtain ultimate precision [49]. More exotic forms of trimming include programmable MOS transistor structures [151] or charging of the floating-gate of floating-gate MOS transistors [152].

Class-AB operation

The possibility of class-AB operation is an important characteristic of TL circuits. In general, mismatch between the separate signal paths, shown in Fig. 3.18, results in harmonic distortion of the overall transfer function. To a lesser extent this effect also occurs in differential (TL) circuits [153, 154]. As an illustrative example, Fig. 5.11 shows the simulated THD of a class-AB current amplifier as a function of a mismatch $\Delta\lambda$ between the gains of the two signal paths. The figure also shows that for an increasing value of the modulation index m of the input signal, the THD saturates.

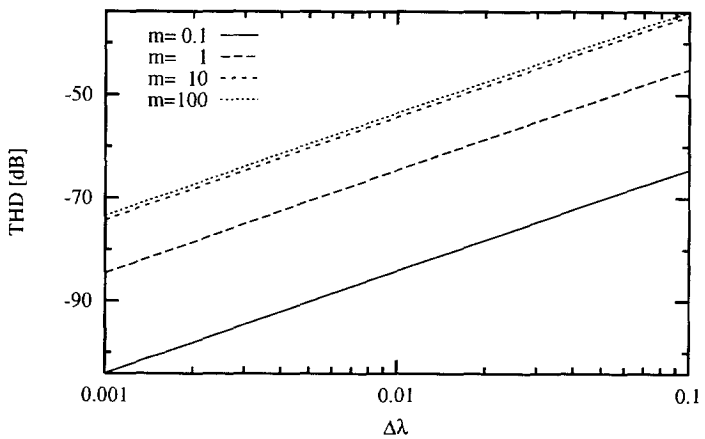

Figure 5.11: Distortion in a class-AB amplifier due to a mismatch factor $\Delta\lambda$.

Mismatch of capacitors

In DTL circuits, another error source is mismatch of the capacitors. The matching of passive components is generally better than of active components. A typical value is 0.2% mismatch for 20/20 μm/μm capacitors [155], which can be improved further by clever layout techniques [156].

It is important to note that mismatch of capacitors in TL filters most often only results in a deviation of the linear transfer function, but does not result in harmonic distortion. An exception is class-AB operated log-domain filters, where two capacitors are used for the implementation of the same pole.

6

Noise

Noise is an important non-ideal aspect in most electronic circuits. A discussion of the noise properties of TransLinear (TL) circuits is therefore of fundamental importance. Furthermore, Static TransLinear (STL) circuits do not have a particularly good reputation when it comes to noise [47,81] and it is likely that Dynamic TransLinear (DTL) circuits inherit these noise characteristics.

The Dynamic Range (DR) and the maximum Signal-to-Noise-Ratio (SNR) are important measures for describing the noise behaviour of analogue circuits. To avoid ambiguity, the exact definitions of the DR and SNR used throughout this thesis are given in Section 6.1.

The analysis of noise in TL circuits is not trivial. Since TL circuits are explicitly based on the exponential behaviour of the transistor, they are inherently non-linear, even when they exhibit an externally-linear transfer function. This results in intermodulation of the signals being processed with noise and interference [9, 24, 31–33].

The situation is further complicated by the fact that the internal noise sources, dealt with in Section 6.2, are non-stationary. The transistor currents in a TL circuit are signal-dependent. As a consequence, the transistor shot noise sources are modulated by the signals being processed [126, 157].

A number of noise analysis methods for STL and DTL circuits have been proposed previously [32,50,158]. However, since the approach used in these publications is quasi-linear and quasi-stationary, these methods cannot adequately account for the non-linear and non-stationary properties of noise in TL circuits. It is also important to note that most circuit simulators do not facilitate non-linear noise analysis.

In the area of non-linear signal processing theory, a lot of effort has been devoted to the topic of noise analysis. Results from this field of research can be applied to the analysis of noise in TL circuits as well. Section 6.3 provides

a short review of some important results, which have been used to develop a non-linear noise analysis method for STL circuits, dealt with in Section 6.4, and DTL circuits, dealt with in Section 6.5 [33,35,38]. The noise analysis method for DTL circuits is however limited to linear TL filters. The analysis of noise in non-linear DTL circuits is beyond the scope of this thesis. The interested reader is referred to [34].

6.1 Definitions of dynamic range and signal-to-noise ratio

In the literature, several definitions for the DR and the maximum SNR are in common use. Therefore, to clarify the discussion, this section explicitly defines these quantities.

By definition:

- The (maximum) SNR equals the (maximum) ratio of the signal power to the noise power *at the same time*;
- The DR equals the ratio of the maximum signal power to the minimum acceptable signal power; the latter is usually taken to be equal to the noise power in the absence of any signals, and this convention is adopted in this thesis.

In conventional amplifiers and filters, based on linear circuit elements, the DR and the maximum SNR are equal since the noise floor is constant. Hence, the maximum SNR is obtained for the maximum value of the signal power, which is determined by a certain specification of the distortion level, e.g. $< 1\%$ total harmonic distortion.

As pointed out in [31], a single noise figure cannot adequately describe the noise behaviour of TL filters, or companding filters in general. Due to signal $\times$ noise intermodulation, the maximum SNR can be much smaller than the DR.

In TL circuits a complication arises with respect to the definition of the SNR. Due to non-stationary noise sources and signal $\times$ noise intermodulation, the equivalent input noise spectrum is time-dependent. The easiest way to define the SNR of a circuit with a non-stationary noise spectrum is to give a stationary interpretation to the noise spectrum. Several possibilities can be thought of. A logical and practical choice is to use the average noise spectrum to define the SNR [159] and this convention is adopted in this thesis. The use of an average spectrum complies with the results obtained from common measurement instruments.

Occasionally, special weighting functions have to be applied to the noise spectrum, e.g., in audio applications, where the physiological properties of the human ear play an important role. However, these aspects are beyond the scope of this thesis.

6.2 Transistor noise sources

Although both the bipolar transistor and the MOS transistor in the subthreshold region are characterised by an exponential V-I transfer function, there are some important differences between these two devices regarding their application in TL circuits. This applies both to the 'ideal' operation and to the noise properties of these transistors.

In Sections 6.2.1 and 6.2.2, the noise sources of the bipolar and the MOS transistor in subthreshold are reviewed briefly and the relative influence of the various noise sources in TL circuits is discussed. The convention used throughout this thesis is to preserve the lower case letter 'i' for noise currents and the upper case letter 'I' for signal currents. Indices are used to distinguish between different noise or signal currents.

6.2.1 Bipolar transistor

The noise behaviour of the bipolar transistor is characterised mainly by four statistically independent noise sources. First, the collector current is accompanied by a current shot noise source i_C, connected between the collector and emitter terminals. The double-sided power spectral density function S_{i_C} of the collector shot noise, which is flat since i_C consists of white noise, is given by:

$$S_{i_C}(\omega, t) = qI_C(t), \tag{6.1}$$

where q is the unity charge.

The second and third noise sources are often described in one equation, as both are connected between the base and emitter terminals. The base current I_B causes a current shot noise source, which has a flat frequency spectrum. The $1/f$ noise, or flicker noise, which is the product of a process-dependent noise mechanism, is usually characterised by a frequency f_l at which its contribution equals the contribution of the white noise. For decreasing values of I_B, f_l decreases [160]. The combined power spectral density function S_{i_B} of the white noise and the $1/f$ noise is given by:

$$S_{i_B}(\omega, t) = qI_B(t)\left(1 + \frac{2\pi f_l}{\omega}\right). \tag{6.2}$$

Normally, with respect to noise calculations, the collector and base currents are approximated as dc currents. In that case, all noise sources are stationary. However, this approximation is not accurate for TL circuits, where the transistor currents are often strongly signal-dependent. Therefore, the shot noise sources in a TL circuit are principally non-stationary, which explains the time variable t in eqns (6.1) and (6.2). The non-stationary representation of the $1/f$ noise lacks

a sound theoretical and experimental foundation, but is commonly adopted in the absence of an established alternative [161, 162].

For noise analysis purposes, it is convenient to represent each non-stationary collector (or base) noise current source $i_C(t)$, as a modulated stationary noise source, i.e.:

$$i_C(t) = a(t)n(t), \tag{6.3}$$

where $n(t)$ is a stationary noise source and $a(t)$ is the modulation function [162–164]. This way, the modulation of the noise spectral density function can be absorbed into the circuit equations. If, by definition, the spectral density of $n(t)$ equals:

$$S_n(\omega) = qI_o, \tag{6.4}$$

where I_o is a dc current, the modulation function $a(t)$ is given by:

$$a(t) = \sqrt{\frac{I_C(t)}{I_o}}. \tag{6.5}$$

The fourth noise source is the thermal noise generated by the base resistance R_B of the bipolar transistor. By good approximation, this voltage noise source v_{R_B} has a white spectrum. Its power spectral density function S_{R_B} is given by:

$$S_{R_B}(\omega) = 2kTR_B, \tag{6.6}$$

where k is Boltzman's constant and T is the absolute temperature.

Comparison of the noise sources

By comparing the three noise sources, it is possible to determine their relative influence in TL circuits under various operating conditions.

Both the base and the collector shot noise are represented by current sources. Since TL circuits are most elegantly described in terms of currents, these two noise sources can be compared directly. Translinear circuits are characterised by the collector currents flowing through the transistors. The collector currents are forced through the transistors using either diode-like connections or (simple) amplifier implementations, as illustrated in Fig. 6.1. In the diode connected transistor, shown in Fig. 6.1(a), i_B and i_C are connected in parallel. Since the noise power of i_C is B_F times higher than the noise power of i_B, the latter is negligible. If an amplifier is used to force the collector current, as illustrated in Fig. 6.1(b), the influence of i_B is further decreased, since the noise source i_B is divided by the current gain G of the amplifier when transformed to the collector terminal. The amplifier is assumed to have an infinite transconductance gain.

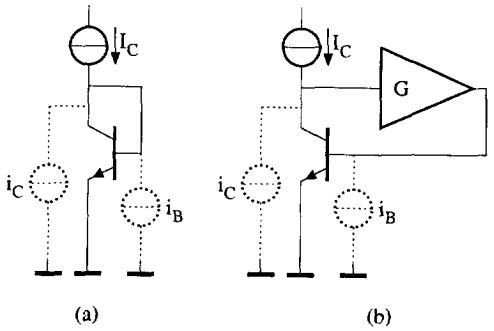

Figure 6.1: Biasing of a transistor in a translinear circuit using (a) a diode connection or (b) an amplifier.

Some simple amplifier implementations often encountered in TL circuits are the common-collector (CC) stage and the differential pair. Often, the CC stage is simply just another transistor in the TL loop, thus having a double functionality.

The only situation in which i_B can become important in a TL circuit is when large magnitude differences of the collector currents exist, of at least a factor β_F. However, in practice, the errors introduced by the finite base currents in such a situation will be very large and will have to be eliminated. If amplifiers are used to this end, the influence of i_B is likewise eliminated. Only when feed-forward error compensation methods are used instead of negative feedback to cancel the influence of finite base currents can i_B become important.

The flicker noise of the bipolar transistor is characterised by the corner frequency f_l. In common bipolar IC processes, f_l is usually quite low, typically a few hertz, and decreases when the base current decreases. Due to the very small influence of base current shot noise in TL circuits, the relative influence of $1/f$ noise in a TL circuit is characterised by a much lower corner frequency of about f_l/β_F. Consequently, in most applications the flicker noise will have a negligible influence. It is interesting to note though that in TL circuits the $1/f$ noise is not only situated at low frequencies, but is copied to other frequency bands due to signal $\times$ noise intermodulation.

The influence of the thermal noise generated by the base resistance cannot be compared directly to the shot noise sources. The noise voltage v_{R_B} first has to be transformed to a noise current source in parallel with i_C.[1] Since $v_{R_B} \ll U_T$, the (small-signal) transconductance $g_m = I_C/U_T$ can be applied to transform v_{R_B} to i_C. Note that in TL circuits, the signal-dependence of I_C often cannot be

[1] In principle, this transformation of v_{R_B} yields besides a noise current source between the collector and emitter terminals also a noise voltage source in series with the collector terminal. However, the influence of the latter on the collector current is negligible, due to the high transistor output impedance.

ignored. The power spectral density $S_{i_{R_B}}$ of i_{R_B}, which has been transformed to the collector terminal, is thus found to be:

$$S_{i_{R_B}}(\omega, t) = qI_C(t)\,\frac{2R_B I_C(t)}{U_T}. \tag{6.7}$$

Comparing eqns (6.1) and (6.7), it can be concluded that v_{R_B} is negligible when the transistor is operated at low current levels, where $I_C \ll \frac{1}{2}U_T/R_B$. Conversely, at high current levels, where $I_C \gg \frac{1}{2}U_T/R_B$, v_{R_B} is the dominant source of noise. For moderate current levels, both noise sources have to be included in the noise calculations.

Signal-to-noise ratio

Some conclusions regarding the maximum SNR of a TL circuit can be derived by calculating the SNR of a single bipolar transistor. The signal power that can be processed by a single transistor is proportional to the square of I_C. For simplicity here, the dc value of I_C is considered to be the processed signal, in which case all noise sources become stationary. Division of the signal power by the noise power in an equivalent noise bandwidth B (in [Hz]) yields the SNR of a single bipolar transistor. The SNR is thus given by:

$$\mathrm{SNR} = \frac{I_C}{2qB\,(1 + 2R_B I_C/U_T)}. \tag{6.8}$$

Figure 6.2 shows a plot of eqn (6.8) for $R_B = 600\ \Omega$ and $B = 1$ MHz. For low current levels, the SNR increases linearly proportional to the collector current. At high current levels, the SNR saturates to 78.3 dB, due to the thermal noise of the base resistance, to the asymptote given by:

$$\lim_{I_C \to \infty} \mathrm{SNR} = \frac{U_T}{4qR_B B}. \tag{6.9}$$

A TL circuit consists of one or several TL loops. Each of these loops can often, but not always, be regarded as a cascade of transistors. In such a TL loop, as a rule of thumb, the SNR of the complete loop is limited to the SNR of the transistor with the lowest (average) collector current, assuming that the equivalent noise bandwidth is the same for all noise sources. If all the transistors operate at high current levels, i.e. $I_C \gg \frac{1}{2}U_T/R_B$, the SNR of the circuit is fundamentally limited to the value expressed by eqn (6.9).

6.2.2 Subthreshold MOS transistor

The symmetry of the MOS transistor is re-discovered in its noise properties [165]. The drain current shot noise can be modelled by two statistically independent

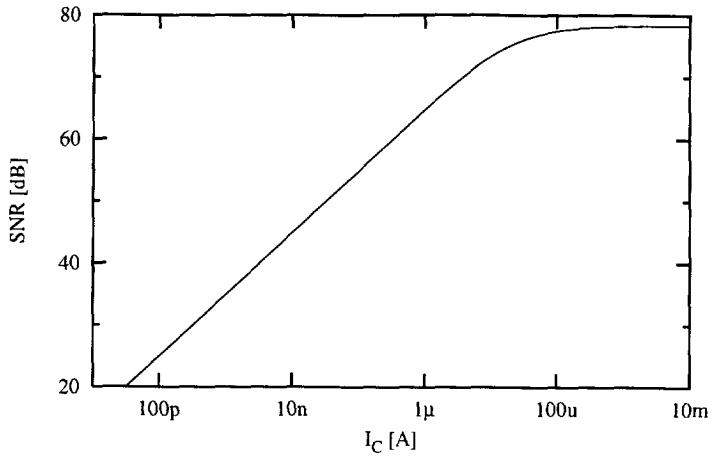

Figure 6.2: The signal-to-noise-ratio of a bipolar transistor, for $R_B = 600\ \Omega$ and $B = 1$ MHz.

noise sources in parallel, characterised by the forward and reverse current components respectively, I_F and I_R in eqn (4.86). The power spectral density function $S_{i_{DS}}$ is given by:

$$S_{i_{DS}}(\omega, t) = q\left[I_F(t) + I_R(t)\right], \tag{6.10}$$

$$= qI_F(t)\left[1 + e^{-V_{DS}(t)/U_T}\right]. \tag{6.11}$$

If the MOS transistor is operated in the saturation region, which is, as yet, the most prevalent situation for TL circuits, $S_{i_{DS}}$ simplifies to $S_{i_{DS}} = qI_{DS}$ [166]. However, for TL circuits comprising MOS transistors operating in the triode region, both noise sources, accompanying I_F and I_R, have to be considered.

Next to the white noise, the MOS transistor exhibits yet another noise component: the $1/f$ noise. It is shown in [166], that $1/f$ noise is negligible at low current levels. Consequently, only white noise has to be considered in TL circuits based on the exponential behaviour of the MOS transistor in the subthreshold region. Note, though, that the signal $\times$ noise intermodulation copies the $1/f$ noise to other frequency bands.

6.3 Noise in non-linear circuits

To calculate the noise behaviour of an electronic circuit, it is customary to transform the internal noise sources to the input or output. An equivalent output noise source can be calculated, which can be compared with the signal

being processed to obtain the SNR. In linear systems, the transformations to be applied are relatively simple. Owing to the superposition principle, the noise sources and signals can be analysed individually. There is no mutual influence. All transfer functions of the internal noise sources to the output are linear. For example, in an amplifier, each noise source is transformed by a gain factor. As another example, in linear filters, the state-space description, used to analyse the signal behaviour of the filter, can also be applied to calculate the linear frequency-dependent gain of each noise source to the output.

The situation is more complicated in non-linear circuits. The superposition principle no longer applies, therefore the noise sources cannot be treated separately from the signals being processed. Intermodulation between signals, noise and interference results in aliasing effects. The noise and interference are transformed to other frequency bands due to this modulation.

Intermodulation effects not only occur in systems with a non-linear transfer function, but also in circuits with a linear transfer function, which behave non-linear internally. Here, we distinguish two important classes of such circuits.

First, in discrete-time circuits, e.g., switched-capacitor (SC) filters, the noise sources are multiplied by the clock signal causing *clock* $\times$ *noise* intermodulation. Noise analysis techniques for SC circuits are based on the fact that the clock is known *a priori*, see, e.g., [167–169].

The second class is linear circuits based on non-linear devices. An important example is the class of TL circuits. Due to the fundamental dependence on the exponential characteristic of the transistor, TL circuits exhibit a strongly non-linear behaviour, causing *signal* $\times$ *noise* intermodulation. Whereas the clock is known in a discrete-time circuit, the signals being processed in a TL circuit are not known *a priori*. This constitutes a fundamental difference with respect to noise analysis. For TL circuits, an extra complication is the non-stationary nature of the transistor noise sources.

A combination of the characteristics of these two classes is also possible. For example, switched-current filters are both discrete-time and based on non-linear devices. Moreover, these circuits also exhibit non-stationary noise sources.

Non-stationary processes

The Wiener-Khintchine theorem relates the autocorrelation function $R(\tau)$ to the power spectral density function $S(\omega)$ via the Fourier transformation, defined by:

$$S(\omega) = \int_{-\infty}^{\infty} R(\tau) \mathrm{e}^{-j\omega\tau} \mathrm{d}\tau. \tag{6.12}$$

When dealing with non-stationary processes, the autocorrelation function becomes a function of the absolute time t and can only be calculated using ensemble averages. In [159], Lampard showed that the Wiener-Khintchine theorem can be generalised to non-stationary processes. By calculating the Fourier

transform of an autocorrelation function $R(\tau, t)$ with respect to the variable τ, a time-dependent frequency spectrum $S(\omega, t)$ is obtained. That is:

$$S(\omega, t) = \int_{-\infty}^{\infty} R(\tau, t) \mathrm{e}^{-j\omega\tau} \mathrm{d}\tau. \tag{6.13}$$

As a consequence of this generalised theorem, non-stationary processes can also be described in terms of (time-varying) frequency spectra.

6.4 Noise in static translinear circuits

Large-signal analysis methods for TL circuits are required to be able to utilise the results described in Section 6.3 for the calculation of signal × noise intermodulation in TL circuits. A structured large-signal analysis method for STL circuits was described in [50]; see Section 3.1 for a brief review. This method has been used to develop a noise analysis method for STL circuits, described in Section 6.4.1. Several illustrative analysis examples are discussed in Section 6.4.2.

6.4.1 Noise analysis method

The non-linear behaviour of TL circuits is due to the exponential nature of the transistor. Since the properties of the exponential function are used in a very specific way, the non-linear properties of TL circuits can be made more explicit. In fact, four different appearances of non-linear behaviour can be distinguished, which all result from the exponential device characteristics. First, the multiplication of collector currents, see eqn (2.14), introduces signal × noise intermodulation. Secondly, the signal-dependent transformation of the base resistance thermal noise introduces a multiplicative non-linearity, see eqn (6.7). Thirdly, the noise current sources are, in general, non-stationary. Finally, in DTL circuits, the incorporation of capacitances may result in non-linear dynamic (transfer) functions.

Using an approach in the current domain, TL loops are described by products of collector currents. These collector currents consist of both signals and noise components. The collector current shot noise sources are already 'current-mode' and are easily incorporated into the TL loop equation. For example, consider the second-order TL loop shown in Fig. 6.3. It is supposed that the four transistors are somehow biased at the currents I_1 through I_4. Each of these collector currents is accompanied by shot noise, the sources i_1 through i_4. For the moment, the base resistance noise voltage sources v_5–v_8 are ignored. The power spectral density of each of the shot noise sources is determined by the instantaneous value of I_1–I_4, respectively. In principle, additional noise sources might exist, originating from current source implementations or interference.

These noise sources can be considered to be part of i_1–i_4. Including i_1–i_4, the TL loop equation is given by:

$$(I_1 + i_1)(I_3 + i_3) - (I_2 + i_2)(I_4 + i_4) = 0. \tag{6.14}$$

This equation contains both signals and noise, and is the basis for the non-linear noise analysis. It is important to note that the noise behaviour of a circuit to be designed can already be evaluated (approximately) once a TL decomposition is derived. Consequently, the synthesis path does not have to be completed before the noise performance of a potential circuit can be calculated.

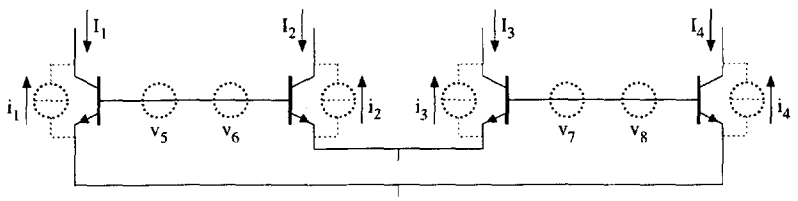

Figure 6.3: A translinear loop in the presence of noise.

The presence of i_1–i_4 in the TL loop equation results in products of signals and noise. Elaboration of eqn (6.14) results in a second-order polynomial. In general, an n^{th}-order polynomial is obtained for an n^{th}-order TL loop. Each separate term of the fully expanded loop equation comprises signal and/or noise components. As long as the noise is much smaller than the signals, products of noise components are negligible. Hence, only those product terms containing at most one noise component are relevant. Expansion of eqn (6.14) thus yields:

$$I_1 I_3 - I_2 I_4 + I_1 i_3 + I_3 i_1 - I_2 i_4 - I_4 i_2 = 0. \tag{6.15}$$

An interesting result of this simplification is that the noise sources have no mutual influence. Therefore, in principle, the transfer function of uncorrelated noise sources to the output can be calculated individually.

The next step is to solve eqn (6.15) for the output current I_{out} of the circuit, which is present in (some of) the currents I_1–I_4. The resulting equation for I_{out} is a polynomial, a rational function or an expression containing n^{th}-order root functions.

Next, a first-order Taylor series approximation is made with respect to all the noise sources, which is allowed as the noise is assumed to be always much smaller than the signals. It is important to note that this approximation preserves the signal-dependence of the noise.

Now, the expression for I_{out} can be divided into a noise-free part, comprising a deterministic component $C(t)$:

$$C(t) = \mathrm{E}[I_{\text{out}}(t)]_{\vec{s},\vec{n}}, \tag{6.16a}$$

and a signal component $\mathcal{S}(t)$:

$$\mathcal{S}(t) = \mathrm{E}[I_{\mathrm{out}}(t)|\vec{s}(t)]_{\vec{n}} - \mathcal{C}(t), \tag{6.16b}$$

and a part $\mathcal{T}(t)$ representing the total output noise [170]:

$$\mathcal{T}(t) = I_{\mathrm{out}}(t) - \mathcal{S}(t) - \mathcal{C}(t), \tag{6.16c}$$

where $\vec{s}(t)$ denotes the vector of input signals, $\vec{n}(t)$ is the vector of stationary noise sources, see eqn (6.3), and $\mathrm{E}[\cdot]$ denotes the mathematical expectation, i.e., the ensemble average at a certain time t, with respect to $\vec{s}(t)$ and/or $\vec{n}(t)$, as denoted by the indices. The signals $\mathcal{C}(t)$, $\mathcal{S}(t)$ and $\mathcal{T}(t)$ are completely uncorrelated. Hence, from these time-domain expressions, the autocorrelation functions $R_{\mathcal{C}}(\tau,t)$, $R_{\mathcal{S}}(\tau,t)$ and $R_{\mathcal{T}}(\tau,t)$, and the power spectral density functions $S_{\mathcal{C}}(\omega,t)$, $S_{\mathcal{S}}(\omega,t)$ and $S_{\mathcal{T}}(\omega,t)$ can be computed directly.

In principle, $\mathcal{T}(t)$ can be separated further into a signal-independent noise term $\mathcal{N}(t)$ and a signal-dependent noise term $\mathcal{I}(t)$ [170]. However, due to the signal-dependent nature of the noise current sources in TL circuits, the calculations involved are cumbersome and do not provide additional insight into the noise behaviour.

Due to the first-order Taylor approximation with respect to all noise sources, each separate noise term in $\mathcal{T}(t)$ consists of a noise current source $i_i(t)$ multiplied by a noise-free factor $G_i(t)$. Using the modulated noise source representation, see eqn (6.3), the term $\mathcal{T}_i(t) = i_i(t)G_i(t)$ can be split into two statistically independent factors:

$$\mathcal{T}_i(t) = i_i(t)G_i(t), \tag{6.17}$$

$$= n_i(t) \cdot [a_i(t)G_i(t)]. \tag{6.18}$$

Equation (6.18) shows that the functions $a_i(t)$ and $G_i(t)$ have an equivalent influence on the noise behaviour of a circuit. In STL circuits, the noise vector $\vec{n}$ comprises only uncorrelated zero-mean noise sources. Hence, the autocorrelation functions $R_{\mathcal{T}_i}(\tau,t)$ of the terms $\mathcal{T}_i(t)$ can be calculated individually. As $n_i(t)$ and $[a_i(t)G_i(t)]$ are independent, and $n_i(t)$ is a white noise process, $R_{\mathcal{T}_i}(\tau,t)$ equals:

$$R_{\mathcal{T}_i}(\tau,t) = R_{n_i}(\tau) \cdot [a_i(t)G_i(t)]^2. \tag{6.19}$$

The term $a_i(t)G_i(t)$ being independent of τ, the power spectral density function $S_{\mathcal{T}_i}(\omega,t)$ of $R_{\mathcal{T}_i}(\tau,t)$ is found to be:

$$S_{\mathcal{T}_i}(\omega,t) = S_{n_i}(\omega)[a_i(t)G_i(t)]^2, \tag{6.20}$$

$$= qI_{\mathrm{C}_i}(t)G_i(t)^2. \tag{6.21}$$

Base resistance thermal noise

In the above discussion, the thermal noise generated by the base resistance was omitted. As mentioned earlier, this is in fact the second source of signal × noise intermodulation in TL circuits, next to the multiplications of currents.

In a TL circuit, see Fig. 6.3, the base-emitter junctions are connected in series. Consequently, the noise voltages v_5–v_8 are series connected and can be combined into one equivalent noise source v_n. This resulting noise source can be placed freely in series with one of the base terminals of the transistors comprising the TL loop. Next, eqn (6.7) is used to transform v_n into an equivalent noise current source i_n. Equation (6.7) shows that v_n is multiplied by $I_C(t)$. Thus, another non-linear characteristic, responsible for signal × noise intermodulation is identified. In principle, the collector current $I_C(t)$ in eqn (6.7) is signal-dependent. However, as v_n can be shifted freely through the TL loop, it is possible to choose which transistor, and hence which collector current is used in eqn (6.7) to calculate i_n. Obviously, the simplest choice is to use a transistor biased at a constant current, which is a prevalent situation.

6.4.2 Analysis examples

In this section, the proposed noise analysis method is applied to some generic STL circuits. Except for the noise sources all transistor non-idealities are ignored in the analyses. The simplest example is the current mirror. Although no collector currents are multiplied in a current mirror, signal × noise intermodulation is introduced due to the base resistance thermal noise. Two examples of second-order TL loops, analysed next, are the square circuit and the square root circuit. The last circuit analysed is the geometric mean current splitter. Its noise behaviour is very relevant, since the current splitter is used in many TL filters to increase the DR through class-AB operation.

Current mirror

The current mirror is the simplest TL circuit. In fact, it is a trivial example. Whereas, in general, TL circuits are described by products of currents, the current mirror is described by a first-order polynomial, which contains no multiplications. Previously, two mechanisms of signal × noise intermodulation in STL circuits have been identified. Since no multiplications of collector currents are present, the only source of signal × noise intermodulation in the current mirror is the transformation of the noise voltage v_{R_B} into an equivalent noise current i_{R_B}.

Figure 6.4 shows a two-transistor current mirror, biased in class A by a dc current I_{dc}. The zero-mean input current I_{in} and output current I_{out} are superposed on I_{dc}. Three relevant noise sources are present within the circuit.

These are the shot noise sources i_1 and i_2, and the thermal noise source v_3, which represents the sum of the noise power of the base resistance thermal noise sources of Q_1 and Q_2.

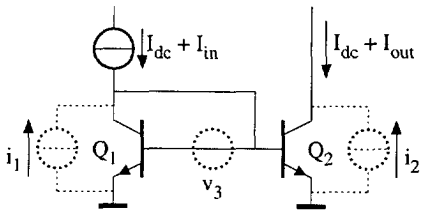

Figure 6.4: The relevant noise sources in a current mirror.

To find a current-mode description of the current mirror, the voltage source v_3 first has to be transformed into an equivalent noise current source. The transconductance g_{m_1} of Q_1 can be applied to calculate an equivalent noise source i_3 in parallel with i_1. The transconductance is not determined by the quiescent current $I_{\rm dc}$, but by the time-varying collector current of Q_1. Thus, g_{m_1} equals $(I_{\rm dc} + I_{\rm in})/U_T$, and i_3 is found to be:

$$i_3 = (I_{\rm dc} + I_{\rm in})\frac{v_3}{U_T}. \tag{6.22}$$

Equation (6.22) clearly demonstrates the occurrence of intermodulation. The noise source i_3 comprises two uncorrelated terms. The first term, $I_{\rm dc}v_3/U_T$, only depends on the statistics of v_3. However, the second term, the multiplication of $I_{\rm in}$ by v_3, represents the signal $\times$ noise intermodulation.

The collector currents I_1 and I_2 of transistors Q_1 and Q_2 are directly found from the currents applied at the collector nodes. Neglecting all transistor non-idealities, the TL loop equation states that the collector currents are equal, i.e., $I_1 = I_2$. An expression for the output current is obtained simply by rearranging the terms. This yields:

$$I_{\rm out} = I_{\rm in} + i_1 - i_2 + (I_{\rm dc} + I_{\rm in})\,\frac{v_3}{U_T}. \tag{6.23}$$

The output current of the current mirror can be divided into three components using the method described in the previous section [170]. Application of eqns (6.16a)–(6.16c) is straightforward and yields:

$$\mathcal{C} = 0, \tag{6.24a}$$

$$\mathcal{S}(t) = I_{\rm in}, \tag{6.24b}$$

$$\mathcal{T}(t) = i_1 - i_2 + v_3\frac{I_{\rm dc} + I_{\rm in}}{U_T}. \tag{6.24c}$$

Due to the absence of multiplications of collector currents in the current mirror, i_1 and i_2 do not introduce any signal $\times$ noise intermodulation. Alternatively, this is intuitively clear since i_1 and i_2 are situated at the input and output, respectively, and the overall transfer function of the circuit is linear.

To calculate the power spectral density of the total output noise, first the autocorrelation function $R_{\mathcal{T}}$ has to be derived. Application of eqn (6.19) yields:

$$R_{\mathcal{T}}(\tau,t) = R_{n_1}(\tau)\frac{I_{\rm dc}+I_{\rm in}(t)}{I_{\rm o}} + R_{n_2}(\tau)\frac{I_{\rm dc}+I_{\rm out}(t)}{I_{\rm o}} + R_{v_3}(\tau)\frac{[I_{\rm dc}+I_{\rm in}(t)]^2}{U_T^2}, \quad (6.25)$$

where $R_{n_1}(\tau)$, $R_{n_2}(\tau)$ and $R_{v_3}(\tau)$ are the autocorrelation functions of n_1, n_2 and v_3, respectively.

The power spectral density function of the total noise component $\mathcal{T}$ can be found by applying the Fourier transform to eqn (6.25). Using expression (6.21), we find:

$$S_{\mathcal{T}}(\omega,t) = 2q\,[I_{\rm dc}+I_{\rm in}(t)] + \frac{4kTR_{\rm B}[I_{\rm dc}+I_{\rm in}(t)]^2}{U_T^2}. \quad (6.26)$$

As explained in Section 6.1, to define the SNR the time averaged power spectral density function, denoted by $\overline{S_{\mathcal{T}}}$, is used. Let $I_{\rm in}$ be a sine wave at frequency $\omega_{\rm o}$, given by:

$$I_{\rm in} = mI_{\rm dc}\sin(\omega_{\rm o}t+\phi), \quad (6.27)$$

where m is the modulation index with respect to the dc bias current $I_{\rm dc}$, and ϕ is a uniformly distributed stochastic variable, representing the arbitrary choice of the origin of the time axis. Then, $\overline{S_{\mathcal{T}}}$ is found to be:

$$\overline{S_{\mathcal{T}}} = 2q\left[I_{\rm dc}+\frac{2R_{\rm B}(I_{\rm dc}^2+P_{I_{\rm in}})}{U_T}\right], \quad (6.28)$$

$$= 2qI_{\rm dc}\left[1+\frac{2R_{\rm B}I_{\rm dc}}{U_T}\left(1+\tfrac{1}{2}m^2\right)\right]. \quad (6.29)$$

Note that the term including the input power $P_{I_{\rm in}}$ in eqn (6.28) would not have been obtained if the equivalent output noise was calculated from the small-signal equivalent circuit of the current mirror at its quiescent point. Expression (6.29) shows that at high current levels, where the noise contribution of $R_{\rm B}$ is dominant, the total output noise can increase by up to 1.8 dB (a factor of 1.5) for $m = 1$, when a sinusoidal input signal is applied. At low current levels, only linear noise can be observed.

Square circuit

Next, consider the square circuit depicted in Fig. 6.5, which can be applied, e.g., as a frequency doubler. Each of the four transistors contributes a noise source, i_1–i_4. The collector currents of Q_1 and Q_2 consist of a dc bias current on which the input current is superposed.

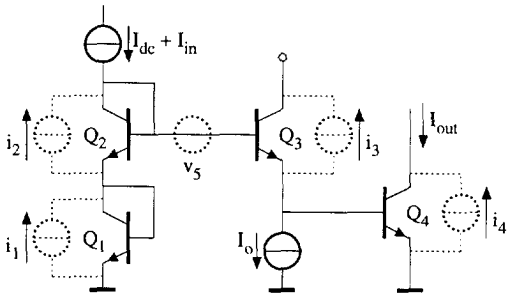

Figure 6.5: Translinear square circuit with internal noise sources.

The four base resistance noise sources can be combined into one source v_5. In this case, transformation of v_5 into an equivalent noise current source in parallel with i_3 is very simple. Transistor Q_3 is biased at a constant current I_o. Therefore, this transformation does not introduce signal × noise intermodulation. In the following calculations, to simplify the equations and without loss of generality, v_5 will be assumed to be negligible.

Including i_1–i_4, the TL loop equation reads:

$$(I_{dc} + I_{in} + i_1)(I_{dc} + I_{in} + i_2) = (I_o + i_3)(I_{out} + i_4). \tag{6.30}$$

To calculate the equivalent output noise, the output current I_{out} has to be isolated from eqn (6.30). Solving for I_{out}, the cross-products of noise sources can be ignored. The factor $(I_o + i_3)$ on the Right-Hand Side (RHS) of eqn (6.30) ends up in the denominator of the expression for I_{out}. The noise source i_3 can be brought to the numerator by applying a first-order Taylor series approximation: $(I_o + i_3)^{-1} \approx (I_o - i_3)/(I_o^2)$. Hence, the expression for I_{out} becomes:

$$I_{out} = \frac{(i_1 + i_2)(I_{dc} + I_{in})}{I_o} + (I_o - i_3)\frac{(I_{dc} + I_{in})^2}{I_o^2} - i_4. \tag{6.31}$$

Since the transfer function of a square circuit is non-linear, all sources, except i_4 which is already at the output, cause signal × noise intermodulation. An input signal has to be chosen to calculate the equivalent output noise. We choose the sine function, eqn (6.27). Hence, $E[\cdot]_{\bar{s}} = E[\cdot]_{\phi}$. Equations (6.16a)–

(6.16c) can be applied to divide I_{out} into three components. This yields:

$$\mathcal{C} = \frac{I_{\text{dc}}^2}{I_{\text{o}}}\left(1 + \tfrac{1}{2}m^2\right), \tag{6.32a}$$

$$\mathcal{S}(t) = \frac{mI_{\text{dc}}^2}{2I_{\text{o}}}\left[4\sin\left(\omega_{\text{o}}t + \phi\right) - m\cos\left(2\omega_{\text{o}}t + 2\phi\right)\right], \tag{6.32b}$$

$$\mathcal{T}(t) = (i_1 + i_2)\frac{I_{\text{dc}} + I_{\text{in}}}{I_{\text{o}}} - i_3\frac{(I_{\text{dc}} + I_{\text{in}})^2}{I_{\text{o}}^2} - i_4. \tag{6.32c}$$

Equation (6.32c) reveals that i_1 and i_2 are modulated only by the fundamental frequency, whereas i_3 is also modulated by the second harmonic frequency component. Note that the dc level of the output transistor, equal to $\mathcal{C}$, see eqn (6.32a), is a function of the modulation index m.

Calculation of the autocorrelation functions and application of the Fourier transformation yields the power spectral density functions of $\mathcal{C}$, $\mathcal{S}$ and $\mathcal{T}$:

$$S_{\mathcal{C}}(\omega) = \frac{2\pi I_{\text{dc}}^4}{I_{\text{o}}^2}\left(1 + \tfrac{1}{2}m^2\right)^2\delta(\omega), \tag{6.33a}$$

$$\begin{aligned} S_{\mathcal{S}}(\omega) = \frac{m^2 I_{\text{dc}}^4}{4I_{\text{o}}^2}\Big\{&8\pi\left[\delta(\omega + \omega_{\text{o}}) + \delta(\omega - \omega_{\text{o}})\right] \\ &+ \tfrac{1}{2}m^2\pi\left[\delta(\omega + 2\omega_{\text{o}}) + \delta(\omega - 2\omega_{\text{o}})\right]\Big\}, \end{aligned} \tag{6.33b}$$

$$S_{\mathcal{T}}(\omega, t) = \frac{2q(I_{\text{dc}} + I_{\text{in}})^3}{I_{\text{o}}^2} + \frac{q(I_{\text{dc}} + I_{\text{in}})^4}{I_{\text{o}}^3} + \frac{q(I_{\text{dc}} + I_{\text{in}})^2}{I_{\text{o}}}. \tag{6.33c}$$

The SNR can be derived from the above equations. The average output noise spectrum is given by:

$$\overline{S_{\mathcal{T}}} = \frac{qI_{\text{dc}}^2}{I_{\text{o}}}\left[\left(1 + \tfrac{1}{2}m^2\right) + \frac{I_{\text{dc}}}{I_{\text{o}}}\left(2 + 3m^2\right) + \frac{I_{\text{dc}}^2}{8I_{\text{o}}^2}\left(8 + 24m^2 + 3m^4\right)\right]. \tag{6.34}$$

Suppose the bandwidth of interest is $[-B, B]$, $B \geq 2\omega_{\text{o}}/\pi$. Integration of eqn (6.33b) and (6.34), followed by a division yields the SNR:

$$\text{SNR} = \frac{I_{\text{o}}}{2Bq} \cdot \frac{I_{\text{dc}}^2 m^2(m^2 + 16)}{I_{\text{dc}}^2(3m^4 + 24m^2 + 8) + 8I_{\text{dc}}I_{\text{o}}(3m^2 + 2) + 4I_{\text{o}}^2(m^2 + 2)}. \tag{6.35}$$

An interesting conclusion can be reached if the SNR is calculated in the limit $I_{\text{dc}} \to \infty$:

$$\lim_{I_{\text{dc}} \to \infty} \text{SNR} = \frac{I_{\text{o}}}{2Bq}\,\frac{m^2(m^2 + 16)}{3m^4 + 24m^2 + 8}. \tag{6.36}$$

The second fraction on the RHS remains less than 1 for all possible values of m. As I_{dc} increases, the power of the collector currents of Q_1, Q_2 and Q_4 increases. Only the collector current of Q_3 remains fixed to I_o. Hence eqn (6.36) illustrates that when the input power is increased, the output SNR becomes proportional to the SNR of Q_3, which has the lowest collector current, see eqn (6.8).

A major advantage of the availability of symbolic expressions for the noise behaviour is the possibility of performing optimisations. As an example, consider the relation between I_o and I_{dc}, which can be optimised for a given input signal. If $m = \frac{1}{2}$, it follows from the derivative of eqn (6.35) with respect to I_o that the optimum value of I_o equals $I_{dc}\sqrt{227}/12$.

Square-root circuit

Polynomials, rational functions and functions containing n^{th}-order roots can be realised using the STL principle. For polynomial transfer functions, an example of which is the square circuit, the different components $\mathcal{C}$, $\mathcal{S}$ and $\mathcal{T}$ in the output current can be identified directly. This is more complicated for rational or n^{th}-order root transfer functions. Therefore, as an example, the noise of a square-root circuit, shown in Fig. 6.6, is now analysed.

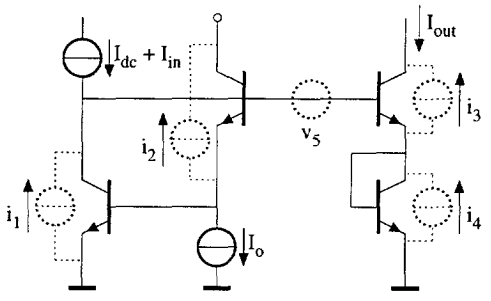

Figure 6.6: Translinear square-root circuit in the presence of noise.

An expression for the output current can be derived from the TL loop equation. The noise currents i_1 and i_2 can be isolated from the resulting square-root, using a first-order Taylor approximation. This yields:

$$I_{out} = \sqrt{(I_{dc} + I_{in})I_o} + \frac{1}{2}\left(i_1\sqrt{\frac{I_o}{I_{dc} + I_{in}}} + i_2\sqrt{\frac{I_{dc} + I_{in}}{I_o}} - i_3 - i_4\right). \tag{6.37}$$

A complication arises if eqns (6.16a)–(6.16c) are applied directly to (6.37). It is not possible, or at least very cumbersome, to find an analytical expression

for $\mathcal{C}$. However, it is directly clear from eqn (6.37) that the first term on the RHS equals $\mathcal{C} + \mathcal{S}$ and the second term represents the total noise $\mathcal{T} = \mathcal{N} + \mathcal{I}$.

Using the proposed analysis method, the spectrum of the total equivalent output noise is found:

$$S_{\mathcal{T}} = \frac{q}{4}\left[I_o + I_{dc} + I_{in} + 2I_{out}\right]. \tag{6.38}$$

For the purpose of noise calculation, the average of the output current can be approximated by $\sqrt{I_o I_{dc}}(1 - \frac{1}{16}m^2)$. Thus, $\overline{S_{\mathcal{T}}}$ becomes:

$$\overline{S_{\mathcal{T}}} = \frac{q}{4}\left[I_o + I_{dc} + 2\sqrt{I_o I_{dc}}\left(1 - \tfrac{1}{16}m^2\right)\right]. \tag{6.39}$$

Class-AB current splitters

The current flowing through a transistor is always restricted to positive values. To facilitate the processing of signals of both negative and positive polarity, some kind of biasing is required. One possible solution is class-A operation, where the actual signal is superposed on a dc bias current. The maximum negative current signal swing is now limited to the dc value of the bias current.

Another option is class-B or class-AB operation, as explained in Section 4.7. Often, the geometric mean function is used to split the input current I_{in} into two strictly positive currents I_{in_1} and I_{in_2}, which can be implemented by the circuit shown in Fig. 6.7. As class-AB operation can increase the DR of a TL filter, the noise behaviour of the current splitter is very relevant.

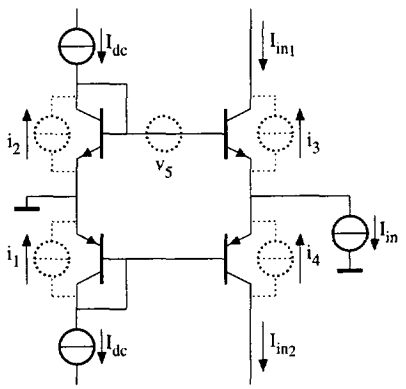

Figure 6.7: A geometric mean current splitter in the presence of noise.

Ignoring all transistor non-idealities, the output current of the splitter equals the difference of I_{in_1} and I_{in_2}. Looking at the node at which the input current source is connected, it is clear that the output current equals I_{in}, irrespective

of the noise sources. This means that the splitter depicted in Fig. 6.7 does not add any noise. The noise sources present in the TL loop equation of the geometric mean circuit only result in common-mode noise in I_{in_1} and I_{in_2}, which is irrelevant. Note that not all possible current splitter implementations possess this favourable property.

6.5 Noise in translinear filters

This section discusses the DR and SNR characteristics of TL filters. Though DTL circuits find wider application than the implementation of linear differential equations (DEs), the discussions in this section are restricted to linear TL filters. The analysis of noise in non-linear DTL networks is described in [34].

In Section 6.5.1, the DR properties of TL filters are compared with respect to conventional filter implementation techniques.

The large-signal analysis method for STL circuits described in [50] has been generalised to the examination of DTL circuits in [13, 16–18]. Both a global and a state-space analysis method have been developed, which are described in Sections 3.2.1 and 3.2.2, respectively. Using these methods, the theory reviewed in Section 6.3 can be applied to the analysis of TL filters. The resulting noise analysis method is presented in Section 6.5.2. Some illustrative analysis examples are discussed in Section 6.5.3.

6.5.1 Dynamic range considerations

Since STL circuits have a poor reputation with respect to noise [47, 81], it is interesting to compare the DR properties of g_mC and opamp-MOSFET-C filters, the most popular implementation techniques to date [171–173], with the DR specifications of TL filters. The comparisons are made under the practically relevant restriction of a low supply voltage. Note that a comparison is made with respect to the DR and not to the maximum SNR, thus, due to the definition of the DR, excluding the signal × noise intermodulation. This intermodulation is the topic of Sections 6.5.2 and 6.5.3.

To obtain an indication of the DR properties of TL, g_mC and opamp-MOSFET-C filters, we compare the RC and the diode-C sub-circuits shown in Fig. 6.8. The DR of a complete filter is strongly related to the DR of these elementary building blocks. The low-pass transfer function $I_{\text{in}} \rightarrow I_{\text{out}}$ is considered for both filter sections. Under certain assumptions, discussed later, the circuit shown in Fig. 6.8(a) is representative of opamp-MOSFET-C filters. The circuit shown in Fig. 6.8(b) represents both TL filters and 'bipolar g_mC' filters, for which the transconductances comprise bipolar transistors only. The DR properties of the two filter sections are compared first based on a simplified approach. The influence of low-voltage implementation issues, tunability,

low-power operation, high-frequency performance and class-AB operation is discussed next.

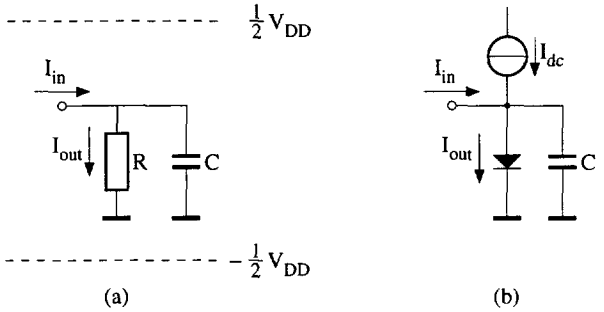

Figure 6.8: Comparison of the dynamic range properties of (**a**) RC and (**b**) diode-C filter sections.

For the RC filter section, the current signal swing is limited, due to the supply voltages, to $V_{\rm DD}/(2R)$. Assuming class-A operation, the signal swing in the diode-C filter is limited by the dc bias current $I_{\rm dc}$.

The only noise source in the RC filter is due to the resistor R. The double-sided noise current power spectral density is given by $2kT/R$. The noise bandwidth of the filter equals $1/(2RC)$. Hence, the equivalent noise power is found to be $kT/(CR^2)$.

In the diode-C circuit, when the signal $\times$ noise intermodulation is neglected, the power spectral density of the shot noise in the bias point equals $qI_{\rm dc}$. In comparing the two filters, both the capacitance value and the bandwidth of the filter are assumed to be equal. As a result, the relation between R and $I_{\rm dc}$ is given by: $RI_{\rm dc} = U_T$, where U_T is the thermal voltage. Hence, the noise bandwidth of the TL filter equals $I_{\rm dc}/(2CU_T)$, and the equivalent noise power is found to be $qI_{\rm dc}^2/(2CU_T)$.

Dividing the maximum signal swing by the total amount of noise, we find the dynamic ranges DR_{RC} and DR_{g_mC} for the RC and the diode-C filter section, respectively. This yields:

$$\mathrm{DR}_{RC} = \frac{CV_{\rm DD}^2}{4kT}, \tag{6.40}$$

$$\mathrm{DR}_{g_mC} = \frac{2CU_T}{q}. \tag{6.41}$$

Equations (6.40) and (6.41) represent upper limits of the DR. In practice, these

values have to be divided by the square of the crest factor[2] of the specific signal being processed.

To compare the dynamic range properties, we divide DR_{RC} by DR_{g_mC}:

$$\frac{\mathrm{DR}_{RC}}{\mathrm{DR}_{g_mC}} = \frac{V_{\mathrm{DD}}^2}{8U_T^2}. \tag{6.42}$$

Obviously, in principle, application of filters based on linear resistors yields a much better DR. For example, even for a low supply voltage of 1 V, and U_T = 26 mV, DR_{RC} and DR_{g_mC} differ by a factor of 185, or equivalently, 22.7 dB. Since the minimum power consumption of a filter is fundamentally related to the desired DR [172], the voltage swings should preferably be rail-to-rail [172, 174]. This is realised in the RC section, but not in the diode-C sub-circuit, where the voltage swing is only U_T, corresponding to a current swing of I_{dc}. This explains the large difference between DR_{RC} and DR_{g_mC}.

The conclusion drawn from eqn (6.42) is not absolute though. Many adventitious factors that affect the DR are not incorporated in eqns (6.40) and (6.41). Their influence is discussed next.

Opamp-MOSFET-C filters

The opamp-MOSFET-C technique is the only method for realising filters with rail-to-rail signal swings and low noise levels [172]. In opamp-MOSFET-C filters, large voltage swings are possible, due to the fact that the quadratic behaviour of the MOS transistor in strong inversion can be approximated quite accurately by a first-order Taylor polynomial. Thus, the sub-circuit shown in Fig. 6.8(a) can be used to represent this class of filters. Based on the simple MOS square law equation, it is even possible, in theory, to obtain a perfectly linear transconductance that extends the voltage swings [175]. Consequently, these filters can be made to approach the fundamental limit regarding the minimum power consumption for a certain specified DR [172].

Unfortunately, at low supply voltages, opamp-MOSFET-C filters become difficult to implement [171–173], resulting in a lower DR than indicated by eqn (6.40). Due to the requirement for strong inversion operation, very low voltage operation only becomes possible by using an on-chip charge pump to drive the gate voltages high. In addition, the tuning range of these filters is quite limited; it is only just enough to cope with process tolerances [171].

MOS g_mC filters

The class of transistor-only g_mC filters can be divided into the categories of 'MOS g_mC' and 'bipolar g_mC', based on MOS and bipolar transistor-only

[2]The crest factor of a signal is defined as the ratio between the peak value and the root-mean-square value.

transconductances, respectively. With respect to opamp-MOSFET-C filters, the excess noise of the transconductors in MOS g_mC filters results in a factor 2 to 3 lower DR. Since most of the other characteristics of MOS g_mC filters are very similar to opamp-MOSFET-C filters, MOS g_mC filters will not be discussed here.

Bipolar g_mC filters

The circuit shown in Fig. 6.8(b) can be used to represent bipolar transistor-only g_mC filters, since the bipolar transistor is an exponential device. Equation (6.42) shows that the DR of bipolar g_mC filters is generally worse in comparison to opamp-MOSFET-C filters, since the voltage swings are limited to U_T. In practice, however, the voltage swings are even smaller due to the strongly non-linear nature of the bipolar transistor. Therefore, most often, the differential pair is used instead of a single transistor to eliminate even order distortion. Nevertheless, the voltage swings remain limited to only 0.7 U_T for a THD of 1%. Application of emitter degeneration resistors is often not allowed as this severely reduces the tuning range.

Transconductance linearisation techniques using linear combinations of collector currents are not as effective for bipolar as for MOS transconductors and cannot increase the maximum voltage swings above 100 $\mathrm{mV_{pp}}$ [130]. Whereas, exact linearisation is possible for MOS transconductors, as the square law is a polynomial, exact linearisation of a bipolar transconductance, using only exponential devices, is fundamentally impossible, since the exponential function is transcendental.

Although the small voltage swings in bipolar g_mC have a negative influence on the DR properties, on the other hand, it makes them very suitable for operation at low supply voltages [130, 171, 173]. The DR is, at the first order, independent of the supply voltage. Further, bipolar g_mC filters exhibit very wide tuning ranges and potential for high frequency and low-power operation.

Translinear filters

Since the diode-C circuit shown in Fig. 6.8(b) represents both bipolar g_mC and TL filters, these two types of filters have many characteristics in common, e.g., excellent tunability and potential for low voltage, low power and high frequency operation.

A major difference is the possible signal swings. Owing to the application of the DTL principle, in theory, TL filters offer a perfectly linear current-mode transfer function. Hence, the maximum signal swings in TL filters are larger than in bipolar g_mC filters. A DR comparison between a bipolar g_mC, a log-domain and a tanh filter, reported in [10], shows that the latter two outperform the g_mC filter by 13 dB and 10 dB, respectively.

A very important aspect of log-domain filters is the possibility of class-AB operation, which can be used to increase the DR. For example, in [9], a DR of 65 dB is reported, in connection with a maximum SNR of 52.5 dB. Class-AB operation is possible due to the fact that the linearisation mechanism of TL filters is theoretically exact. Since the two different signal paths only have to process unipolar signals, no dc bias current is needed. Hence, the noise floor is de-coupled from the maximum current signal swings, in contrast to the class-A set-up shown in Fig. 6.8(b).

Summary

To conclude, in principle, opamp-MOSFET-C filters are the best choice for a large DR in the area of tunable continuous-time filters. However, in low voltage environments, or for applications where a large tuning range is required, TL filters and bipolar g_mC are more suitable.

Owing to the theoretically exact linearisation mechanism, TL filters are an interesting and competitive alternative to g_mC filters. Particularly when class-AB operation is applied, the DR of TL filters, which is theoretically unlimited, exceeds the DR obtainable with g_mC filters. At low supply voltages, the DR of (class-AB) TL filters can even exceed the DR of practical opamp-MOSFET-C filters.

6.5.2 Noise analysis method

To a large extent, the noise analysis method for DTL circuits is identical to the method described in Section 6.4.1 for STL circuits. However, some complications arise due to the frequency-dependence of the capacitance currents.

The TL loop equation (6.14) is representative both for STL and DTL circuits. The only difference is the presence of capacitance currents. To find the DE describing the transfer function of a DTL circuit, the expressions for the capacitance currents have to be derived and substituted in the TL loop equation. Since the capacitance currents are related to collector currents incorporating noise, the resulting capacitance current expressions will include these noise sources *and their derivatives*. These derivatives of noise sources are additional elements in the noise vector $\vec{n}$, which are correlated to the noise sources from which they originate [170].

The DE obtained through substitution of the capacitance current expressions can contain complicated noise terms. Again a first-order Taylor approximation is applied to simplify the expressions. The approximation is performed with respect to all noise sources, thus including the time derivatives of noise sources that are additional elements in $\vec{n}$.

Since correlated noise sources, with a coloured frequency spectrum, are introduced in DTL circuits, each autocorrelation function $R_{\mathcal{T}_i}$ now has to be

computed collectively for an entire group of correlated noise sources. Often, a complete group of correlated noise sources can be rewritten into one single expression of the form $i_i G_i$, where i_i represents a white noise source and G_i contains no noise sources. If this situation is accomplished, eqns (6.19)–(6.21) can be used once more to calculate the noise frequency spectrum.

In the DE, not all noise terms will be situated at the output of the filter. Hence, once the power spectral density of a noise term is calculated, it has to be transformed to the output of the filter through multiplication by a certain frequency-dependent transfer function. For example, a noise term at the input of the filter is transformed to the output through multiplication by $|H(\omega)|^2$, where $H(\omega)$ describes the transfer function of the filter.

Base resistance thermal noise

In DTL circuits, a complication arises concerning the influence of the base resistance thermal noise sources. A capacitance connected in a TL loop divides the TL loop in two capacitance-junction(s) loops. As a result, only the noise voltage sources within each of the two resulting loops are series connected and can be combined into an equivalent noise source.

6.5.3 Analysis examples

In this section, some illustrative analyses of the non-linear noise properties of TL filters are presented. First, a first-order class-A filter is analysed, which shows that the influence of signal × noise intermodulation is quite small when class-A operation is assumed. Secondly, the corresponding class-AB filter is examined. In this mode of operation, the signal × noise intermodulation dominates for large values of the input power. Finally, Seevinck's class-AB filter circuit is dealt with.

Class-A translinear filter

Figure 6.9 shows an already well-known DTL circuit. This first-order low-pass filter operates in class A. Its cut-off frequency can be tuned by the current I_o. Basically, the filter consists of a second-order TL loop, comprising Q_1–Q_4, and a capacitance C.

The filter can be described by its TL loop equation [16], including i_1–i_6:

$$(I_{dc} + I_{in} + i_1 + i_5)I_o = (I_o + I_{cap} + i_2)(I_{dc} + I_{out} + i_{3,eq} + i_4 + i_6), \tag{6.43}$$

where i_5 and i_6 are the equivalent input and output noise currents originating from the base resistance noise of Q_1-Q_2 and Q_3-Q_4, respectively, represented by v_5 and v_6, shown in Fig. 6.9. Due to the presence of C in the TL loop, v_5 and

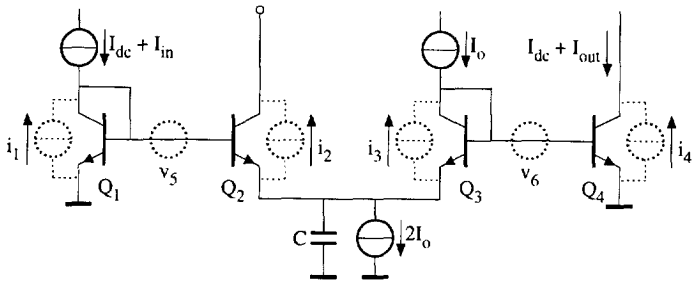

Figure 6.9: Noise in a translinear first-order low-pass filter.

v_6 cannot be combined into one equivalent noise voltage. The shot noise source i_3 is transformed to an equivalent noise source $i_{3,\mathrm{eq}} = -i_3 \cdot (I_{\mathrm{dc}} + I_{\mathrm{out}})/I_{\mathrm{o}}$ at the output. This way, the capacitance current is only determined by the current $I_{\mathrm{dc}} + I_{\mathrm{out}} + i_{3,\mathrm{eq}} + i_4 + i_6$ through Q_4, which avoids the production of correlated noise components in the equations.

Equation (2.20) can be used to eliminate I_{cap}, resulting in a DE. Ignoring products of noise sources yields:

$$\frac{CU_T}{I_{\mathrm{o}}}\left[\dot{I}_{\mathrm{out}} + \frac{\mathrm{d}}{\mathrm{d}t}\left(i_{3,\mathrm{eq}} + i_4 + i_6\right)\right] + I_{\mathrm{out}} + i_{3,\mathrm{eq}} + i_4 + i_6 = I_{\mathrm{in}} + i_1 + i_5 - i_2\frac{I_{\mathrm{dc}} + I_{\mathrm{out}}}{I_{\mathrm{o}}}. \quad (6.44)$$

Equation (6.44) shows that i_1, i_2 and i_5 are situated at the input of the filter, whereas $i_{3,\mathrm{eq}}$, i_4 and i_6 are located at the output. Hence, two noise spectra $S_{\mathcal{T}_{\mathrm{in}}}(\omega, t)$ and $S_{\mathcal{T}_{\mathrm{out}}}(\omega, t)$ can be distinguished, which are given by:

$$S_{\mathcal{T}_{\mathrm{in}}}(\omega, t) = q\Bigg[\underbrace{I_{\mathrm{dc}} + I_{\mathrm{in}}}_{i_1} + \underbrace{\frac{(I_{\mathrm{o}} + I_{\mathrm{cap}})(I_{\mathrm{dc}} + I_{\mathrm{out}})^2}{I_{\mathrm{o}}^2}}_{i_2} + \underbrace{\frac{4R_{\mathrm{B}}(I_{\mathrm{dc}} + I_{\mathrm{in}})^2}{U_T}}_{v_5}\Bigg], \quad (6.45a)$$

$$S_{\mathcal{T}_{\mathrm{out}}}(\omega, t) = q\Bigg[\underbrace{\frac{(I_{\mathrm{dc}} + I_{\mathrm{out}})^2}{I_{\mathrm{o}}}}_{i_3} + \underbrace{I_{\mathrm{dc}} + I_{\mathrm{out}}}_{i_4} + \underbrace{\frac{4R_{\mathrm{B}}(I_{\mathrm{dc}} + I_{\mathrm{out}})^2}{U_T}}_{v_6}\Bigg]. \quad (6.45b)$$

The horizontal braces indicate the origin of the different terms.

To calculate the equivalent output noise, $S_{\mathcal{T}_{\mathrm{in}}}(\omega, t)$ has to be transformed to the output. In principle, to obtain the resulting non-stationary output noise spectrum, the application of two-dimensional Fourier transformations is required, instead of the one-dimensional transformation introduced in eqn (6.13).

However, in the definition of the SNR the time-averaged spectrum is used. Since the filter under consideration is linear, the sequence of the operations of filtering and averaging can be exchanged, which simplifies the calculations. Hence, the contribution of $S_{\mathcal{T}_{\rm in}}(\omega,t)$ to the average output noise spectrum $\overline{S_{\mathcal{T}}}(\omega)$ is equal to $\overline{S_{\mathcal{T}_{\rm in}}}(\omega)|H(\omega)|^2$. Thus, $\overline{S_{\mathcal{T}}}(\omega)$ is given by:

$$\overline{S_{\mathcal{T}}}(\omega) = q\left(I_{\rm dc} + \frac{I_{\rm dc}^2 + P_{I_{\rm out}}}{I_{\rm o}} + \frac{4R_{\rm B}I_{\rm dc}^2}{U_T}\right)\left(1+|H(\omega)|^2\right) + \frac{4qR_{\rm B}}{U_T}\left(P_{I_{\rm out}} + P_{I_{\rm in}}\,|H(\omega)|^2\right). \quad (6.46)$$

Equation (6.46) shows that intermodulation of the noise sources with both the input and the output signal occurs. It is important to note that the input signal does not have to be in the pass-band of the filter to increase the noise level. Consequently, a large out-of-band-signal will deteriorate the SNR of a small in-band-signal at the output of the filter. The intermodulation noise is higher for in-band signals as for out-of-band signals, though.

Using eqn (6.46) and applying the noise bandwidth of the filter to $i_{3,\rm eq}$, i_4 and i_6 as well, the SNR of the class-A TL filter can now be determined. Considering a sinusoidal input current within the pass-band of the filter, see eqn (6.27), the SNR as a function of m plotted in Fig. 6.10 is obtained. In this figure, $C = 10$ pF, $R_{\rm B} = 0\ \Omega$, $I_{\rm dc} = 5\ \mu$A and $I_{\rm o} = 1\ \mu$A.

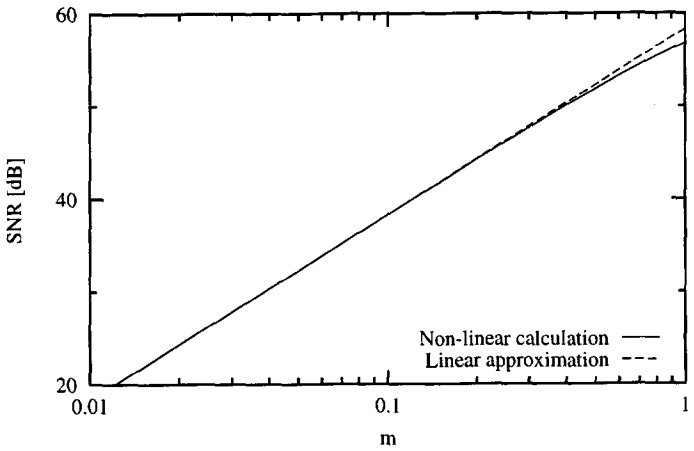

Figure 6.10: Signal-to-noise-ratio for a translinear filter operated in class A.

Since $m < 1$ for a class-A filter, the influence of signal × noise intermodulation is very small. The difference between the non-linear calculation and the linear approximation, shown for reference in Fig. 6.10, equals only 1.51 dB

for $m = 1$. Hence, for class-A TL filters, the noise floor in the absence of any signals can be used as a very good estimate of the noise. This is not the case in class-AB filters, as is shown in the following section.

Class-AB translinear filter

To benefit from the DR improvement companding can provide, class-AB operation is required. A possible way to realise a class-AB first-order low-pass filter is to use the geometric mean current splitter, shown in Fig. 6.7, and, with the aid of some current mirrors, apply the currents I_{in_1} and I_{in_2} to the inputs of two class-A log-domain filters, shown in Fig. 6.9. The dc bias current I_{dc} becomes obsolete and is omitted. The output currents of the two class-A filters are denoted by I_{out_1} and I_{out_2}. The SNR of the resulting class-AB filter is calculated next. A sine wave input is assumed, see eqn (6.27).

It was shown in Section 6.4.2 that the current splitter does not contribute any noise. Assuming the current mirrors between the splitter and two class-A filters do not have a significant noise contribution, the equivalent output noise power equals two times the equivalent output noise power of the class-A filter. Neglecting the influence of R_{B}, computation of the (average) spectrum $\overline{S_{\mathcal{T},I_{\text{in}_1}}}(\omega)$ yields:

$$\overline{S_{\mathcal{T},I_{\text{in}_1}}}(\omega) = q\left(\frac{P_{I_{\text{out}_1}}}{I_{\text{o}}} + \overline{I_{\text{out}_1}}\right)\left(1 + |H(\omega)|^2\right), \tag{6.47}$$

where $\overline{I_{\text{out}_1}} (= \overline{I_{\text{in}_1}})$ is the dc average value of I_{out_1}, $P_{I_{\text{out}_1}}$ is the power of I_{out_1} and $H(\omega)$ is the transfer function of the filter.

In class-AB TL filters, the noise floor increases due to two effects. First, the signal $\times$ noise intermodulation causes the SNR to saturate. Second, the noise level rises due to the increase of $\overline{I_{\text{out}_1}}$. The latter effect is less strong, however, and cannot cause saturation of the SNR.

To calculate the SNR for a single signal in the pass band of the filter, $P_{I_{\text{out}_1}}$, see eqn (6.47), can be replaced by $P_{I_{\text{in}_1}}$. In other words, the transfer function is approximated as being frequency-independent. Using a geometric mean current splitter, the power $P_{I_{\text{in}_1}}$ is given by:

$$P_{I_{\text{in}_1}} = \overline{I_{\text{in}_1}^2} = I_{\text{dc}}^2\left(1 + \tfrac{1}{4}m^2\right). \tag{6.48}$$

An exact expression for the average value $\overline{I_{\text{in}_1}}$ for the sine wave input, see eqn (6.27), cannot be computed. However, for noise purposes, $\overline{I_{\text{in}_1}}$ can be approximated by:

$$\overline{I_{\text{in}_1}} = \begin{cases} I_{\text{dc}} & \text{if } m \ll 1, \\ \frac{mI_{\text{dc}}}{\pi} & \text{if } m \gg 1. \end{cases} \tag{6.49}$$

The exact value of $\overline{I_{\text{in}_1}}$ and the approximations, eqn (6.49), are illustrated in Fig. 6.11.

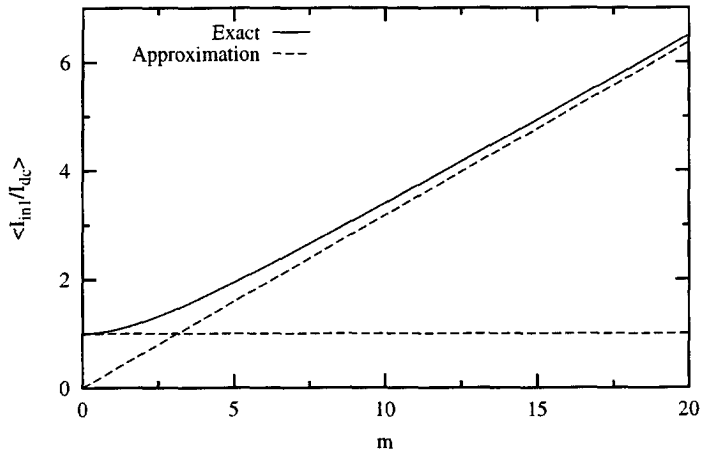

Figure 6.11: The dc output level of a geometric mean splitter.

The total output noise power of the class-AB filter is found by integration of eqn (6.47) over ω, and multiplication by a factor 2 to account for the two class-A filters. The noise bandwidth of the filter, which equals $I_o/(2CU_T)$ for a double-sided spectrum, is also applied to i_3 and i_4, shown in Fig. 6.9. For large values of m, the SNR is given by:

$$\text{SNR} = \frac{\frac{1}{2}m^2 I_{\text{dc}}^2}{\frac{2qI_{\text{dc}}}{CU_T}\left[\frac{mI_o}{\pi} + I_{\text{dc}}\left(1 + \frac{1}{4}m^2\right)\right]}. \tag{6.50}$$

The SNR is a function of the modulation index m of the input signal. Figure 6.12 displays the SNR, using the exact value of $\overline{I_{\text{in}_1}}$. The parameter values used in this plot are: $I_{\text{dc}} = aI_o$, where $a = [0.1,\ 1,\ 10]$, $I_o = 1\ \mu$A, $C = 10$ pF and $U_T = 26$ mV. The corresponding cut-off frequency is 612 kHz. The x-axis variable, equal to $m \cdot a$, represents the amplitude of I_{in}, normalised to I_o. For low values of $m \cdot a$, the SNR increases linearly, by 20 dB per decade. Eventually, the SNR saturates to a value of 62.1 dB.

A higher value of the quiescent current I_{dc} constitutes a higher noise floor, and hence, a lower SNR, as illustrated in Fig. 6.12. Whereas a low value of I_{dc} decreases the output noise, it also increases the distortion at a certain input power level. These two effects will have to be mutually weighted during design.

For reference, we mention the DR at $m = 15$, which is an estimation of the practical upper limit of the signal swing. For $m = 15$, and $a = [0.1,\ 1,\ 10]$, the DR equals [79.2, 86.6, 89.2] dB, respectively. The differences of [17.1, 24.5, 27.1]

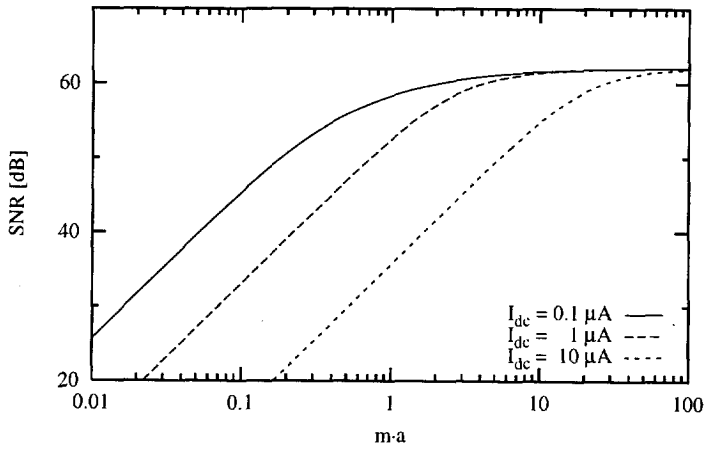

Figure 6.12: Signal-to-noise-ratio of a class-AB translinear filter.

dB, respectively, between the DR and the SNR demonstrates the beneficial influence of companding.

Maximum signal-to-noise ratio

The maximum value of the SNR equals the limit of eqn (6.50) for $m \to \infty$:

$$\lim_{m\to\infty} \text{SNR} = \frac{CU_T}{q}. \tag{6.51}$$

This limit leads to an interesting conclusion. The maximum SNR not only increases linearly with the capacitance C, but also with the absolute temperature T. This effect can be explained as follows. On the one hand, the shot noise power is independent of the temperature. On the other hand, eqn (3.23) shows that the capacitance voltage swings increase proportionally to T, which is beneficial with respect to the SNR. Note that, except for a constant factor, the result of eqn (6.51) complies with (6.8), when $R_B = 0$, $I_C = I_o$ (the lowest collector current value in the class-AB filter), and B is equal to the noise bandwidth, $I_o/(2CU_T)$.

For high current levels, where the base resistance thermal noise dominates, the same conclusion is reached. In this region, for the class-AB filter the maximum SNR is given by:

$$\lim_{m\to\infty} \text{SNR} = \frac{CU_T}{q}\,\frac{U_T}{4R_B I_o}. \tag{6.52}$$

The first fraction on the RHS corresponds with eqn (6.51). The second fraction is temperature independent, since I_o has to be a PTAT current to compensate for the temperature dependence of the low-pass cut-off frequency [1,2].

The limited value of the maximum SNR can be explained intuitively from the first-order TL filter depicted in Fig. 6.9, assuming class-AB operation. Figure 6.13 shows that this filter can be re-drawn as a cascade of two-ports. It is obvious that the SNR of a chain of two-ports is limited by the element(s) having the lowest SNR. A translation of this fact to the circuit shown in Fig. 6.13 indicates that the maximum SNR of the class-AB TL filter is limited by the transistors with the lowest SNR value, defined in Section 6.2.

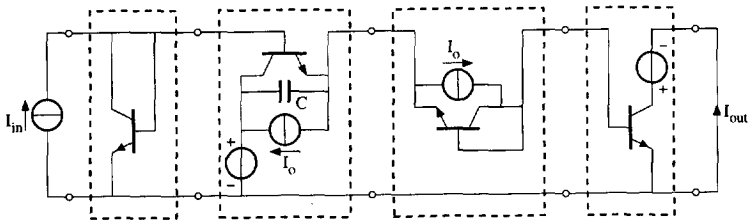

Figure 6.13: A translinear filter consisting of a cascade of two-ports.

In Fig. 6.9, for increasing input signal swings, and class-AB operation, the average collector currents of Q_1 and Q_4 increase accordingly. Hence, the SNR of Q_1 and Q_4 increases. The average collector currents of Q_2 and Q_3, however, remain equal to I_o. Thus, for large signals, the SNR of these two transistors dictates the maximum SNR value of the complete filter. For Q_3, P_{I_C} equals I_o^2. The (double-sided) power spectral density of i_C is equal to qI_o, and the noise bandwidth of the filter equals $I_o/(2CU_T)$. Hence, P_{i_C} becomes $qI_o^2/(2CU_T)$, and the SNR of Q_3 is found to be $2CU_T/q$. Since Q_2 and Q_3 have the same SNR, the overall SNR is reduced by a factor of two. This again yields:

$$\mathrm{SNR}_{\max} = \frac{CU_T}{q}. \tag{6.53}$$

Noise due to out-of-band signals

A major advantage of the proposed analysis method is its comprehensiveness. For example, eqn (6.47) incorporates the different influence of in-band versus out-of-band signals being processed by the filter. Figure 6.14 displays the noise power spectrum for a sinusoidal input signal, with $m = 10$, at the frequencies $\omega = [\frac{1}{10}, 1, 10]\omega_c$, ω_c being the cut-off frequency of the filter. For reference, the noise level in the absence of any signals is also depicted.

The co-existence of a large signal and a small signal in a companding TL filter is an interesting situation. Suppose the small signal is the desired output

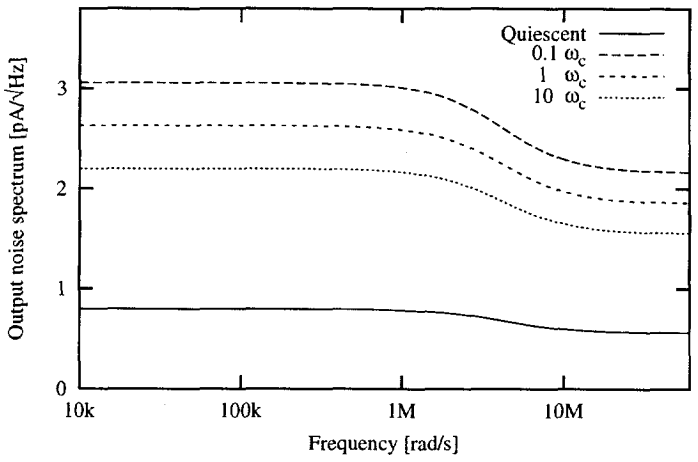

Figure 6.14: Influence of signal × noise intermodulation on the noise spectrum.

signal and the large signal is outside the pass-band. Now, in conventional filters, the large signal will limit the maximum SNR at the output as it occupies a large part of the available DR of the filter. Naturally, the same effect applies to companding filters. However, in these filters, the SNR at the output will be further decreased, as the large out-of-band signal will increase the internal noise level [31]. This effect makes companding filters less suitable, e.g., for intermediate-frequency filtering [172], unless some form of linear pre-filtering is used [31].

Figure 6.15 displays the resulting SNR for an in-band signal as a function of the amplitude of an out-of-band signal. The applied input signal equals $I_{dc}(m \sin \omega_1 t + n \sin \omega_2 t)$, where ω_1 and ω_2 are the in-band and out-of-band frequencies, respectively. The modulation index m of the in-band signal equals $[0.1, 1, 10]$, and n denotes the modulation index of the out-of-band signal. The figure demonstrates the expected behaviour. Clearly, the effect is more pronounced for in-band signals with a small amplitude, i.e. a low value of m.

Seevinck's class-AB integrator

Although exhibiting an externally-linear transfer function, the class-AB integrator proposed by Seevinck in [2], and shown in Fig. 6.16, is a non-linear DTL circuit in a way as it implements two non-linear DEs, see eqns (4.99a) and (4.99b). In Fig. 6.16, two current sources I_0 have been added in parallel to the capacitances to give the circuit the same low-pass transfer function as the filter shown in Fig. 6.9.

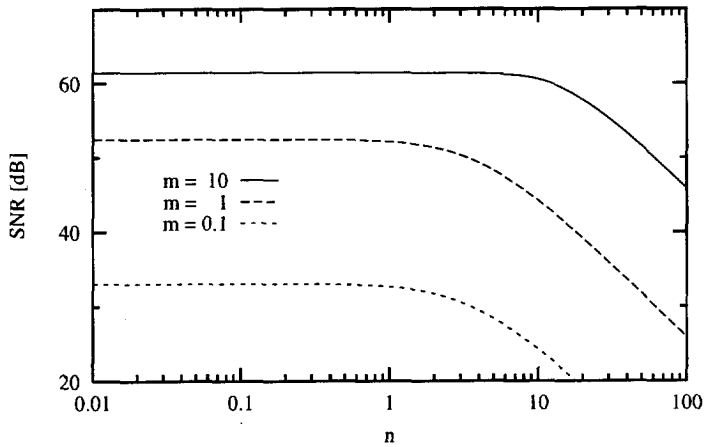

Figure 6.15: Signal-to-noise-ratio in the presence of an out-of-band signal.

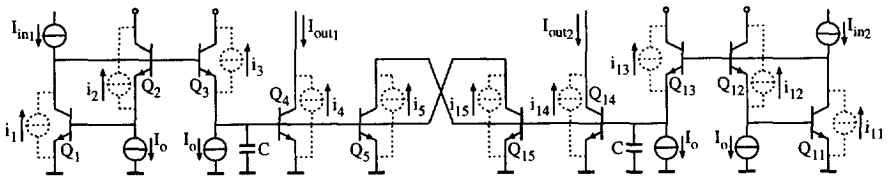

Figure 6.16: Seevinck's class-AB translinear filter in the presence of noise [2].

With respect to the class-AB filter treated previously, the most important change is the addition of the output currents I_{out_1} and I_{out_2} to the collector currents of Q_{13} and Q_3, respectively. This addition ensures that these collector currents are strictly positive when the circuit is used as an integrator, i.e., without the current sources I_o connected in parallel to the capacitors, introduced here.

The circuit basically comprises two TL loops, the inputs I_{in_1} and I_{in_2} of which are obtained from a (geometric mean) current splitter. The difference of I_{out_1} and I_{out_2} is the actual output current I_{out}. In the presence of shot noise, the overall DE is found to be:

$$\frac{CU_T}{I_o}\left(\dot{I}_{out} + \frac{di_4}{dt} - \frac{di_{14}}{dt}\right) + I_{out} + i_4 - i_{14} = I_{in} + i_1 - i_{11} + i_2\frac{I_{in_1}}{I_o} - i_{12}\frac{I_{in_2}}{I_o} + (i_{15} - i_3)\frac{I_{out_1}}{I_o} + (i_{13} - i_5)\frac{I_{out_2}}{I_o}. \quad (6.54)$$

Taking into account the symmetry of the filter, when I_{in} is stationary and symmetrical, the average power spectral density function $\overline{S_T}$ of the total output

noise can be expressed as:

$$\overline{S_T}(\omega) = 2q\left(\overline{I_{\text{in}_1}} + \frac{P_{I_{\text{in}_1}} - P_{I_{\text{out}_1}} + 2\overline{I_{\text{in}_1} I_{\text{out}_1}}}{I_o}\right) \cdot |H(\omega)|^2 + 2q\overline{I_{\text{out}_1}}. \tag{6.55}$$

Since $\overline{S_T}$ is partly determined by $\overline{I_{\text{out}_1}}$ and $\overline{I_{\text{in}_1} I_{\text{out}_1}}$, to evaluate the exact noise spectrum for a given input signal, the DEs (4.99a) and (4.99b) have to be solved. Unfortunately, as these DEs are non-linear, there is no general way of doing so. The only solution is to apply a numerical approach, i.e. to use a circuit simulator. Common simulation programs can be used to find $\overline{I_{\text{out}_1}}$ and $\overline{I_{\text{in}_1} I_{\text{out}_1}}$.

7

Voltage-translinear circuits

TransLinear (TL) circuits are based on the exponential law describing the bipolar transistor. Based on the square law model for the strong inversion MOS transistor, a different type of TL circuits can be realised [67–70]. The formal definition of the general principle behind these 'Voltage-TransLinear'[1] (VTL) circuits was published by Seevinck and Wiegerink in [67], see Section 2.3.

This chapter discusses the practical relevance of the VTL design principles, and in particular of Dynamic Voltage-TransLinear (DVTL) circuits, the strong inversion MOS analogue of Dynamic TransLinear (DTL) circuits. With the possible exception of specialised non-demanding applications, it is concluded that VTL circuits do not have much practical value.

Section 7.1 first discusses the validity of the square law model for the drain current. Another important aspect, the designability of VTL circuits, is dealt with in Section 7.2. Section 7.3 describes the general large-signal analysis of DVTL circuits. Based on this analysis method, finally, in Section 7.4, a comparison is made between three possible DVTL output stages, the analogs of the log-domain, tanh and sinh DTL output stages described in Section 3.3.

7.1 Square law conformance

The square law model of the drain current in the strong inversion region, eqn (2.25), is a rough approximation of the MOS transistor's behaviour in practice [117]. Whereas the exponential law, describing the bipolar transistor, is valid across a current range of six to ten decades, the square law model is only valid over approximately 1.5 decades of current [70]. This current range is even

[1]The term 'Voltage-Translinear' proposed in [63, 64] is used throughout this thesis as it clearly distinguishes between TL principles based on the exponential law and VTL principles based on the square law, as opposed to the term 'MOS Translinear' proposed in [67].

smaller for modern CMOS processes, due to down-scaling of the gate oxide thickness. As a consequence, the square law region will ultimately vanish, and with it the sole foundation of the VTL design principles.

The validity of the square law is further degraded by the body effect. This second-order effect can be cancelled out by connecting the back-gate of each transistor to its source, but this implies an important speed penalty. In folded topologies, the effect is less pronounced but nonetheless present.

7.2 Designability

Another disadvantageous property of VTL circuits concerns the designability. In principle, the synthesis path of VTL circuits [70,73] is very similar to the TL design trajectory shown in Fig. 4.1. However, severe problems are encountered at the stage of VTL decomposition.

In comparison with the TL loop equations, the VTL loop equations are much more complicated and mathematically awkward. Hence decomposition is very difficult for VTL. To date, the only existing structural method for finding VTL decompositions is a numerical one, which can only be applied to four-transistor single-loop circuits, having one input, one output and one bias current [70].

Furthermore, VTL circuits are far less versatile than TL circuits. An illustration of this fact is given by the very limited number of different VTL loop equations that can be found in literature, see, e.g., [70] for an overview.

In addition, the design of VTL circuits with true class AB VTL behaviour, that is, having theoretically unlimited signal swings, is difficult. This is again a consequence of the fundamentally different characteristics of TL and VTL loop equations.

7.3 Analysis of dynamic voltage-translinear circuits

In Section 2.3.2, the DVTL principle is explained with respect to the class of $\sqrt{\cdot}$-domain filter networks. This class of DVTL circuits is characterised by the subcircuit depicted in Fig. 2.11, where the capacitance C forms a closed loop with one gate-source voltage. In general, however, a capacitance in a DVTL circuit is connected in series with a number of gate-source junctions, as illustrated by Fig. 7.1, compare with Fig. 3.6. The corresponding capacitance current I_{cap} is given by:

$$I_{\text{cap}} = C \sum_i \pm \frac{\dot{I}_{\text{DS},M_i}}{\sqrt{2\beta_i I_{\text{DS},M_i}}}, \tag{7.1}$$

where I_{DS,M_i} and β_i are the drain currents and transconductance factors, respectively, of the transistors comprising the loop. The sign of each fraction in eqn (7.1) is dependent on the orientation of the transistor in the loop.

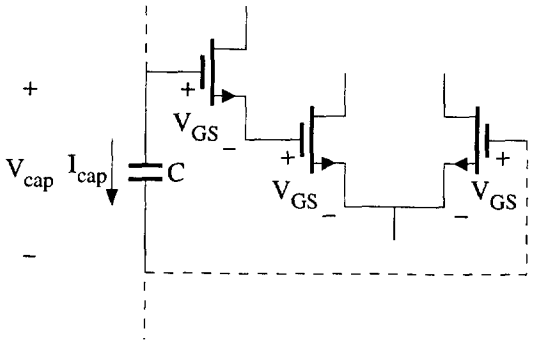

Figure 7.1: A capacitance in (a part of) a voltage-translinear loop.

In combination with the VTL loop equations, see eqn (2.27), (7.1) is the key to the large-signal analysis of DVTL circuits. The resulting analysis method is used next in Section 7.4 to investigate the characteristics of three possible DVTL output stages.

7.4 Characteristics of different voltage-translinear filter classes

Replacing the bipolar transistors in the DTL output stages shown in Figs 3.14, 3.19 and 3.23 by strong inversion MOS transistors results in three possible DVTL output stages, see Fig. 7.2.

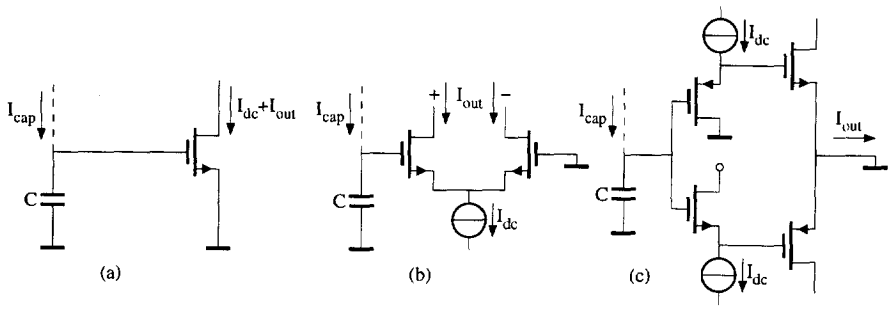

Figure 7.2: Three possible dynamic voltage-translinear output stages.

$\sqrt{}$-domain circuits

The first DVTL output stage, the common-source stage, is characteristic for the class of $\sqrt{}$-domain filters [29, 30, 73, 176]. This sub-circuit can be used to implement the derivative $\dot{I}_{\text{out}}$, given by eqn (2.32) with $I_{\text{DS}} = I_{\text{out}}$. A comparison of the log-domain and the $\sqrt{}$-domain output structures, based on eqns (3.56) and (2.32), shows that the latter class needs more circuitry to implement the derivative $\dot{I}_{\text{out}}$. Only four (bipolar) transistors are required to implement a log-domain low-pass filter. On the other hand, the implementation of the $\sqrt{}$-domain integrator described in Section 8.5.2 requires a square-root circuit and a multiplier. The multiplier again comprises two square circuits. The $\sqrt{}$-domain integrator published in [176] is a little more efficient as it requires a square-root circuit and only one square circuit. Nevertheless, it is clear that $\sqrt{}$-domain circuits require significantly more circuitry than log-domain circuits.

Differential pair output stage

Even more hardware is required to implement a linear derivative $\dot{I}_{\text{out}}$ based on the differential pair output stage, shown in Fig. 7.2(b). The capacitance current I_{cap} is now given by:

$$I_{\text{cap}} = \frac{C}{\sqrt{2\beta}} \dot{I}_{\text{out}} \left(\frac{1}{\sqrt{I_{\text{dc}} + I_{\text{out}}}} + \frac{1}{\sqrt{I_{\text{dc}} - I_{\text{out}}}} \right), \tag{7.2}$$

where β is the transconductance factor of the transistors comprising the differential pair.

The question arises whether the differential pair is a useful DVTL output stage. The MOS differential pair is often used in conventional filter implementations. In these circuits, a total harmonic distortion of 1% in I_{out} is obtained for a sinusoidal input voltage swing of 1.8 V_p (for $\beta = 50\ \mu\text{A/V}^2$, $V_{th} = 0.7$ V and $I_{dc} = 1\text{mA}$). This is equivalent to an output current modulation index $m = 0.53$. Hence, application of the DVTL principle can yield a theoretical improvement of the Dynamic Range (DR) of only 5.5 dB. However, the large amount of additional circuitry required introduces additional noise and distortion, and will reduce this 5.5 dB DR improvement.

Analog of the sinh output stage

More interesting is the output stage shown in Fig. 7.2(c), which is a direct translation of the sinh DTL output stage. The capacitance current is now given by:

$$I_{\text{cap}} = \frac{C}{4\sqrt{2\beta I_{\text{dc}}}} \dot{I}_{\text{out}}. \tag{7.3}$$

Note that I_{cap} and $\dot{I}_{\mathrm{out}}$ are *linearly* related. As a consequence, no additional circuitry is required to linearise this output stage; it is already linear. Additionally, this stage allows a kind of class-AB behaviour as the maximum current swing of I_{out} is four times as large as I_{dc}.

The above comparison of the three possible DVTL output stages shows that the two circuits shown in Fig. 7.2(a,b) are not practically useful, and only interesting from an academic point of view. They require a significant amount of additional hardware for linearisation purposes, which is not required at all for the output stage shown in Fig. 7.2(c).

In fact, the output stage shown in Fig. 7.2(c) is a well-known circuit [69], and many related implementations have been published, see, e.g., [68,177,178]. The linear V-I relation is possible owing to the fact that the MOS square law is a polynomial function. An analog principle for DTL circuits is fundamentally impossible since the exponential law is not a polynomial, but a transcendental function.

8

Realisations

This chapter describes realisations of both Static TransLinear (STL) and Dynamic TransLinear (DTL) circuits. In addition, one realisation of a Dynamic Voltage-TransLinear (DVTL) circuit is described.

As STL circuits have been around for many years, the accent of this chapter lies on DTL circuits. The STL circuits described in Section 8.1 [119, 179] are not conventional in that they use properties of the subthreshold MOS transistor not available in TL designs using bipolar transistors.

Sections 8.2 [180] and 8.3 [93] discuss linear TransLinear (TL) filters. These filters have been designed to operate at a low supply voltage down to 1 volt. The filter described in Section 8.2 is operated in class A, the filter described in Section 8.3 in class AB.

A non-linear application of the DTL principle is RMS-DC conversion, which is the topic of Section 8.4 [22, 42, 181].

The last design example, discussed in Section 8.5 [73], is a current-controlled oscillator, based on the DVTL principle.

Two other design examples demonstrating the application of the synthesis theory proposed in Chapter 4, an oscillator and a phase-locked loop, can be found in [21] and [27, 28], respectively.

8.1 Subthreshold MOS translinear circuits

Application of the subthreshold MOS transistor opens up some extra possibilities for the implementation of TL circuits, as described in Section 4.5.2. This section describes realisations of STL circuits based on these additional options.

First, the application of the back gate-as an active terminal is used in Section 8.1.1 to implement a low-voltage current mirror. Another application of the back-gate terminal is reported in Section 8.1.2, describing the design of a sine

shaping circuit. Finally, operation of the MOS transistor in the triode region is exploited in the cascoded current mirror dealt with in Section 8.1.3.

8.1.1 Bulk current-mirror

In a conventional current mirror, see Fig. 8.1(a), the input current I_{in} forces the gate voltage, while the back-gate is connected to the source. However, it is equally possible to bias the gates at a constant voltage V_{ref} and use the back-gate to mirror the input current, as shown in Fig. 8.1(b). This principle can also be applied in strong inversion [182]. For an NMOS mirror in a p-substrate process, a double-well process will be necessary. The bulk-source junction is biased slightly forwards. As a consequence, the input voltage V_{in} is restricted to about 350 mV to keep the back-gate leakage current small in comparison with I_{in}. The input voltage has to be higher than about 100 mV for the input transistor to remain saturated. The input voltage of the bulk current-mirror is lower than the gate-source voltage of the conventional current mirror. Hence, the bulk current-mirror might be useful for low-voltage applications.

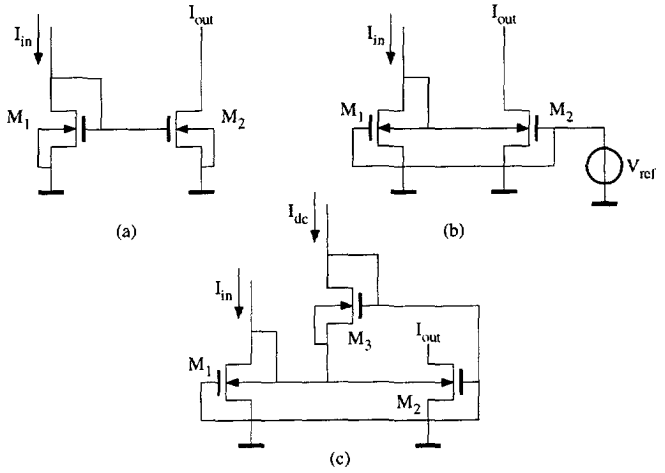

Figure 8.1: (**a**) Conventional current mirror. (**b**) Bulk current-mirror. (**c**) Improved bulk current-mirror.

The current mirrors were implemented using transistor arrays. The aspect ratio of the NMOS transistors used is 108/7 μm/μm. The gates are biased at 350 mV. The measured and ideal output current I_{out} of the bulk current-mirror are depicted in Fig. 8.2. For $I_{\text{in}} < 100$ pA, the bulk voltage is less than 100 mV, causing a deviation from the ideal transfer function. Above $I_{\text{in}} = 100$ nA, the

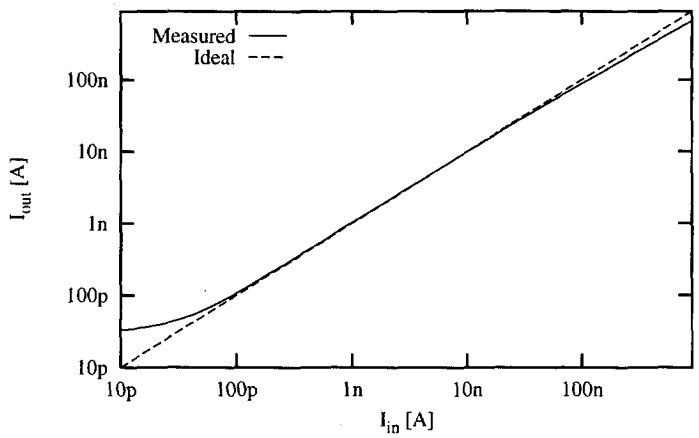

Figure 8.2: Measured and ideal output current of the bulk current-mirror.

bulk voltage is greater than 420 mV and the resulting leakage current reduces the accuracy of the bulk current-mirror.

The main disadvantage of the bulk current-mirror is the small input current range with respect to a conventional current mirror. First, this is caused by the relatively small input voltage range of about 250 mV. Secondly, the slope of the V_{BS} versus $\ln I_{DS}$ characteristic is usually about twice as steep as the slope of the V_{GS}-$\ln I_{DS}$ plot. The second effect can be cancelled out by driving the gate as well as the back-gate, connecting them by a voltage source. Figure 8.1(c) shows the resulting current mirror, where M_3 is a simple realisation of the voltage source. The drain current I_{dc} of M_3 is added to I_{in}. Therefore, I_{dc} has to be much smaller than I_{in}. Another possibility is to compensate for I_{dc} by subtracting I_{dc} from I_{out}. The derivative of V_{in}-$\ln I_{in}$ of this mirror is the same as the derivative for a bipolar transistor current mirror, which is 59 mV/decade, as shown by the measurements depicted in Fig. 8.3, where V_{in} is plotted against I_{in} for the current mirrors shown in Fig. 8.1. The increase of the derivative of V_{in}-$\ln I_{in}$ for the improved bulk current-mirror around 100 nA is due to a protection diode between the gate and the back-gate, which causes latch-up for higher bulk voltages.

The bandwidth of the bulk current-mirror is about four times lower than the bandwidth of a conventional mirror. Both the input resistance and the input capacitance are about twice as large. Hence, the price paid for low-voltage operation is a reduction of the bandwidth.

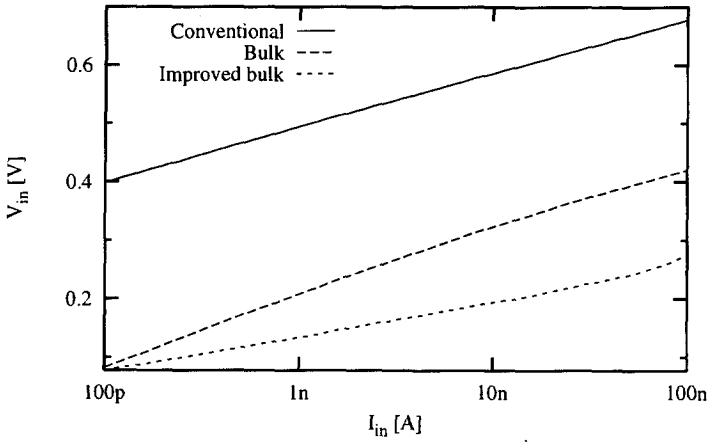

Figure 8.3: Measured input voltages of the conventional mirror, the bulk current-mirror, and the improved bulk current-mirror.

8.1.2 A $\sin x$-circuit in MOS technology using the back-gate

A trivial application of the topology shown in Fig. 4.26, described by the new equation structure (4.82), is the construction of a square-root circuit. A bread-board version of the circuit, depicted in Fig. 8.4, was built using transistor arrays to verify eqn (4.82). The drain currents of transistors M_2, M_3, M_4 and M_6 are all 1 nA ($= I_{dc}$), and are supplied by the two current mirrors, implemented by M_9 through M_{16}. The drain currents of M_1 and M_5 are the input current I_{in} and the output current I_{out}, respectively. The gates of M_5 and M_6 are biased at $V_{ref} = 550$ mV. Transistors M_7 and M_8 are two simple floating voltage sources, which are used to keep M_3 and M_6 in saturation for bulk voltages of less than 100 mV. The supply voltages V_{DD} and V_{SS} are ± 1 V. The aspect ratios of the used NMOS and PMOS transistors are 108/7 and 108/7.5 μm/μm, respectively.

Measurements were performed using an HP4142B Modular DC Source / Monitor. In Fig. 8.5, the 'transfer function' I_{out}^2/I_{in} of the square-root circuit is plotted. The large errors at low and high values of the input current are caused by leakage currents of the measurement set-up and by the transition into the moderate inversion region, respectively. The main cause of error for intermediate current values is mismatch, which is quite large due to the bread-board realisation. The average mismatch between the drain currents of two transistors at the same gate-source voltage is about 9%. As a consequence, the influence of the restricted validity of the simple drain current model (4.76) could

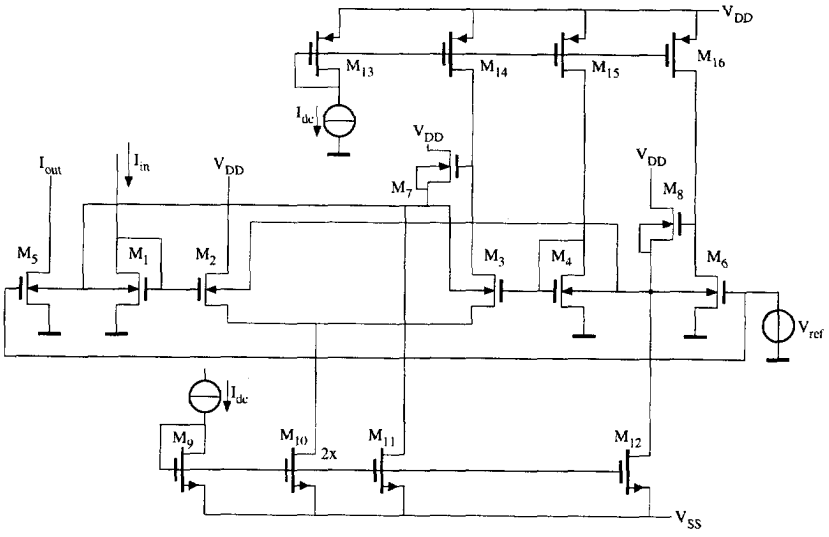

Figure 8.4: Application of the back-gate in a square-root circuit.

not be measured. Nevertheless, it is clear that the circuit will be quite accurate when the transistors are properly matched.

Based on these results, a sine shaping circuit was designed using the general topology shown in Fig. 4.26. The sine function cannot be implemented directly using TL circuits. First, an approximation by a polynomial or rational function has to be derived. The sine function can be approximated by a rational function, eqn (4.31). Another way of writing this sine approximation is eqn (4.41), which can easily be fitted on equation structure (4.82) by choosing $I_2 = (I_o - I_{out} - I_{in})$, $I_3 = (I_o + I_{out} + I_{in})$, $I_5 = (I_o + I_{in})$, $I_6 = (I_o - I_{in})$ and $I_1 = I_4$, where I_{in} and I_{out} are the input and output current, and I_o is a dc bias current. The sine shaped output current is obtained by:

$$2I_{out} = I_3 - I_2 - 2I_{in}. \tag{8.1}$$

The complete circuit is depicted in Fig. 8.6. Since the circuit is differential, a gain cell, implemented by M_9–M_{12} [44], is used to convert the input signal into a differential signal. Current mirrors are used to supply the currents to the actual $\sin x$-circuit.

The measured output current is shown in Fig. 8.7. The gates of M_5 and M_6 in Fig. 8.6 are biased at 350 mV, the bias current I_o is 1 nA and the input current I_{in} varies from 0 to 2 nA. The drains of M_2 and M_3 are loaded by two 500 mV voltage sources. Despite the rather large mismatch due to the breadboard realisation, causing offset, asymmetry, amplitude, phase and frequency errors, the result is clearly a sine function.

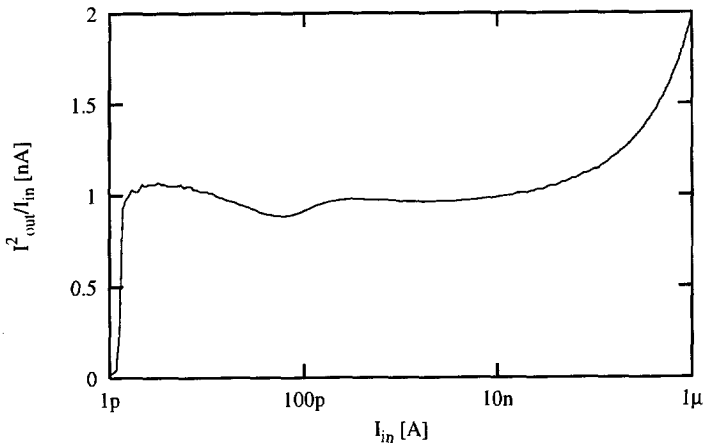

Figure 8.5: Transfer function $I^2_{\text{out}}/I_{\text{in}}$ of the square-root circuit.

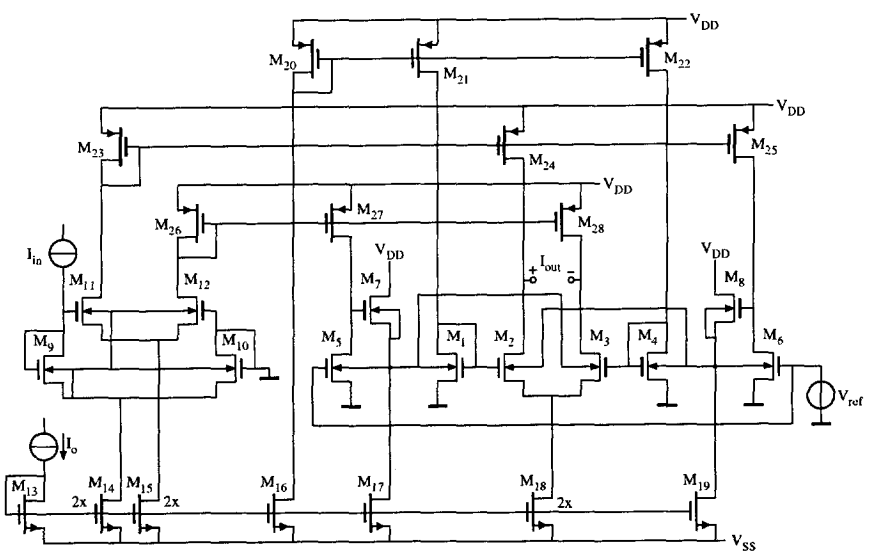

Figure 8.6: A $\sin x$-circuit.

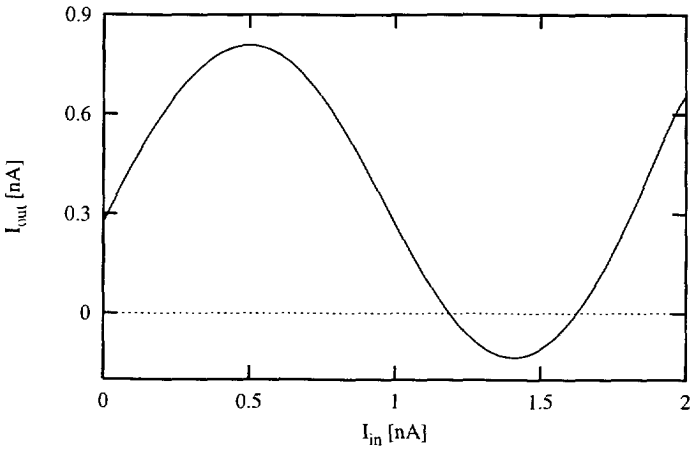

Figure 8.7: Measured output current of the $\sin x$-circuit.

8.1.3 High-swing cascode MOS current mirror

Due to the trend towards lower supply voltages in modern VLSI systems, many well-known conventional circuit techniques are no longer applicable. An important example is the current mirror, a common basic building block. Especially for high-performance implementations, like the cascode, the standard Wilson [100] and the improved Wilson current mirrors [183], the output voltage swing is severely reduced.

A number of low-voltage high-swing cascode current mirrors have been proposed, e.g., [184,185]. In these designs, voltage room is gained by operating the grounded MOS transistors at the verge of saturation. An even higher output voltage swing is obtained when the grounded MOS transistors are operated in the triode region, as was recently proposed in [186].

In this section, another triode-region high-swing cascode current mirror is presented. The proposed current mirror is shown in Fig. 8.8(a). Transistors M_3 and M_4 are operated in the triode region. The operation of the circuit becomes intuitively clear if M_3 and M_4 are regarded as active resistances, biased at a constant gate voltage through the diode-connected transistor M_5. Then the circuit resembles a simple current mirror, comprising M_1 and M_2, with source degeneration. The degeneration resistors increase the output resistance of the current mirror. As M_4 operates in the triode region, the mirror provides cascode-type output resistance for output voltages even lower than twice the subthreshold MOS saturation voltage $V_{DS_{sat}}$. The output resistance r_{out} of the

circuit is approximately given by:

$$r_{\text{out}} = g_{m_2} r_{o_2} \left(\frac{1}{g_{m,\text{D}_4}} \parallel r_{o_4} \right), \tag{8.2}$$

where g_{m_2} is the gate transconductance of M_2, g_{m,D_4} is the drain transconductance of M_4, and r_{o_2} and r_{o_4} denote the output conductance of M_2 and M_4.

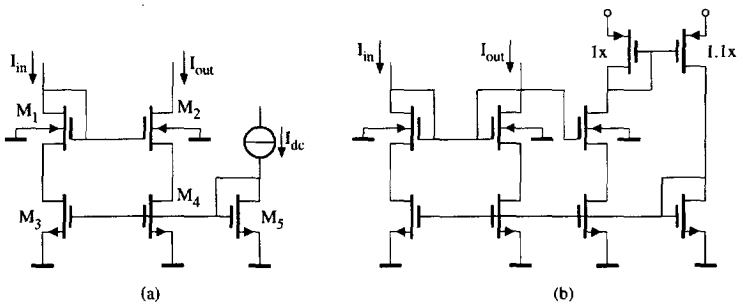

Figure 8.8: Cascode current-mirrors using triode-region MOSTs.

An exact description of the circuit's operation is obtained from a large-signal analysis. A TL analysis can be performed by recognising that the current mirror basically consists of a TL loop, comprising two MOS transistors operating in the saturation region, M_1 and M_2, and two MOS transistors operating in the triode region, M_3 and M_4. The drain currents of I_{DS_1} and I_{DS_2} equal I_{in} and I_{out}, respectively. The forward currents I_{F_3} and I_{F_4} both equal $I_{\text{DS}_5} = I_{\text{dc}}$. As the drain currents of M_3 and M_4 equal I_{in} and I_{out}, respectively, their reverse currents are found from eqn (4.86): $I_{\text{R}_3} = I_{\text{dc}} - I_{\text{in}}$ and $I_{\text{R}_4} = I_{\text{dc}} - I_{\text{out}}$. Hence, the TL loop equation becomes:

$$I_{\text{in}} \left(I_{\text{dc}} - I_{\text{out}} \right) = I_{\text{out}} \left(I_{\text{dc}} - I_{\text{in}} \right). \tag{8.3}$$

The solution of eqn (8.3) is indeed $I_{\text{out}} = I_{\text{in}}$.

The deviation from the ideal transfer function of the current mirror shown in Fig. 8.8(a) was measured using a transistor array. The aspect ratio of the used MOS transistors is $W/L = 108/7\ \mu\text{m}/\mu\text{m}$. The bias current is $I_{\text{dc}} = 100$ nA. The results are shown in Fig. 8.9.

The input current of the current mirror shown in Fig. 8.8(a) is limited. As the reverse current I_{R} of an MOS transistor is positive by definition, eqn (8.3) shows that $I_{\text{in}} < I_{\text{dc}}$. This limitation can be overcome by using an adaptive biasing method [184,185], which is illustrated in Fig. 8.8(b). By exchanging I_{dc} in eqn (8.3) with $A \cdot I_{\text{out}}$, where $A > 1$, I_{R_3} and I_{R_4} remain positive for all values of I_{in}. Correct operation was verified by simulation.

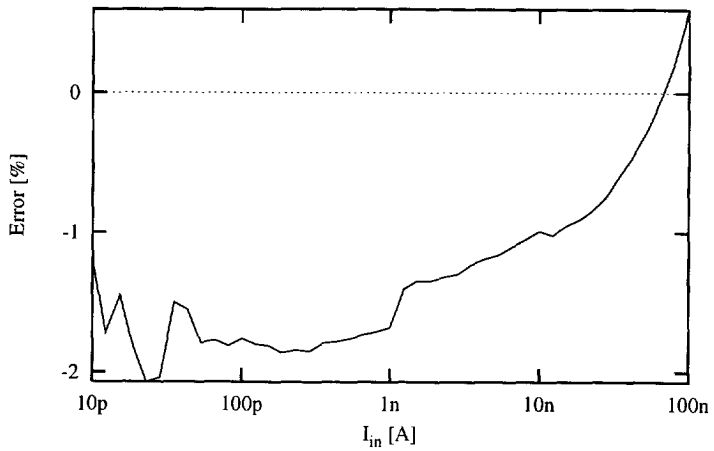

Figure 8.9: Measured error in the transfer function of the current mirror shown in Fig. 8.8(a).

The operation of the proposed current mirrors is not restricted to the weak inversion region. The circuits only exploit the symmetric property of the triode-region MOS transistor, which is equally valid in the moderate and strong inversion region. Correct operation in the strong inversion region is easily validated through a Voltage-TransLinear (VTL) analysis [70] and was verified by measurements for the circuit shown in Fig. 8.8(a).

8.2 A translinear integrator for audio filter applications

Especially in a low-voltage environment, the limited Dynamic Range (DR) of electronic filters is a problem, see, e.g., [80]. If a (frequency) controllable transfer function is also required and resistor values become too large for integration, which is the penalty for going to lower and lower currents, the situation becomes even more complicated [187].

In this section, a systematic approach to the design of a 1 volt, 'ultra-low-power', i.e. resistorless, TL integrator, which can be considered to be a basic building block of log-domain filters, is presented. Section 8.2.1 deals with the implementation in a low-voltage environment. As an application example, Section 8.2.2 presents a controllable second-order low-pass filter for hearing instruments, of which the measurements are given in Section 8.2.3.

Much of the material in this section has been developed by, and in co-operation with, Martijn Broest and Wouter Serdijn [180].

8.2.1 Design of the integrator

The starting point of the discussion is the TL integrator, as mentioned by Seevinck in [2], see Fig. 3.8. The circuit basically consists of a second-order TL loop that implements eqn (3.34). Although Seevinck's integrator contains only six NPN transistors, thus indicating its potential to operate up to high frequencies, it also suffers from some major drawbacks. First, the integrator dc gain A_{dc} is a function of the current gain factor β_{F} of the output transistors and the ratio $I_{\mathrm{o}}/I_{\mathrm{in}}$:

$$A_{\mathrm{dc}} = \frac{\mathrm{d}I_{\mathrm{out}}}{\mathrm{d}I_{\mathrm{in}}} \approx \frac{\beta_{\mathrm{F}}}{\sqrt{8\beta_{\mathrm{F}}\frac{I_{\mathrm{in}}}{I_{\mathrm{o}}}+16}}. \tag{8.4}$$

Equation (8.4) shows that the dc gain is small for small values of β_{F} and non-linear for variations of the input current I_{in}.

Secondly, because of the two base-emitter voltages connected in series between the two supply rails, this integrator is not able to operate at very low supply voltages.

The first disadvantage can be overcome by connecting a voltage follower in series with the input of the output transistors. Overcoming the other disadvantage implies the use of a different TL topology.

A different TL decomposition was derived to realise the low-voltage TL integrator. Instead of eqn (3.33), a possible decomposition of (3.34) is:

$$I_{\mathrm{o}}\left(I_{\mathrm{out}}+I_{\mathrm{in}}\right) = I_{\mathrm{out}}\left(I_{\mathrm{o}}+I_{\mathrm{cap}}\right). \tag{8.5}$$

At a supply voltage of one volt, four topologies can be used to implement eqn (8.5). Either an all-NPN folded topology, see Fig. 4.10, or a mixed folded topology, see Fig. 4.22, is used.

Of the various possible ways to implement eqn (8.5), the TL loop depicted in Fig. 4.22(a) has been chosen as it requires only one additional floating voltage source, is symmetrically biased and — according to simulations, using realistic transistor models — has a satisfying high-frequency behaviour. The resulting circuit diagram, including the above-mentioned voltage follower, is depicted in Fig. 8.10. The floating voltage source prevents transistor Q_1 from saturating. The PNP current mirror with two outputs delivers the two output currents with the correct sign to the TL loop. It can be seen that I_{o} no longer determines the maximum signal current the integrator can handle. These currents are determined in the complete filter structure, as described in Section 8.2.2.

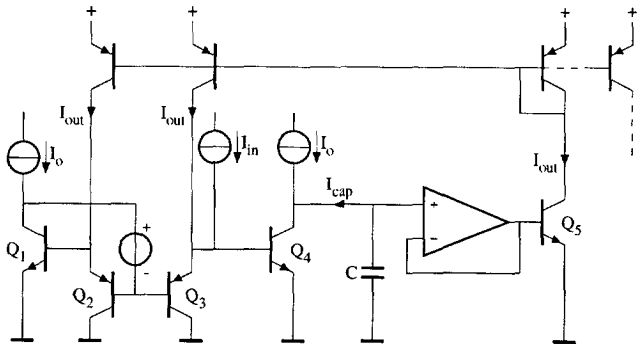

Figure 8.10: Signal path of the 1-V translinear integrator with an ideal floating voltage source and an ideal voltage follower.

Voltage follower

A suitable implementation of the voltage follower is an ordinary differential pair of which the positive output and the negative input have been connected to each other.

To be able to drive the output transistor Q_5 (and possible additional parallel-connected output transistors), the collector bias currents, I_{bias}, of the differential pair should be larger than the maximum base current of the output transistor(s). However, the base currents of the differential pair should be smaller than the collector current I_o of Q_4. A very convenient value is the geometric mean of these two boundaries which equals the geometric mean of the collector bias currents of Q_4 and Q_5. Hence:

$$I_{\text{bias}} = \sqrt{I_o I_{\text{out}}}. \tag{8.6}$$

Floating voltage source

A suitable embodiment of the floating voltage source, which additionally reduces the influence of base currents in the divider, is an ordinary emitter follower. Again, for the value of its biasing current, I_{ef}, the geometric mean of I_o and I_{out} is a suitable value. To create some room for the bias source of this emitter follower and for the tail current source of the voltage follower, an additional voltage source, V_{dc}, has been connected in series with the emitters of Q_1, Q_4 and Q_5. Note that the absolute value of this voltage source is not important since it does not appear in the TL loop equation. A convenient value is 200 mV. The circuit diagram of the complete 1-V TL integrator is depicted in Fig. 8.11.

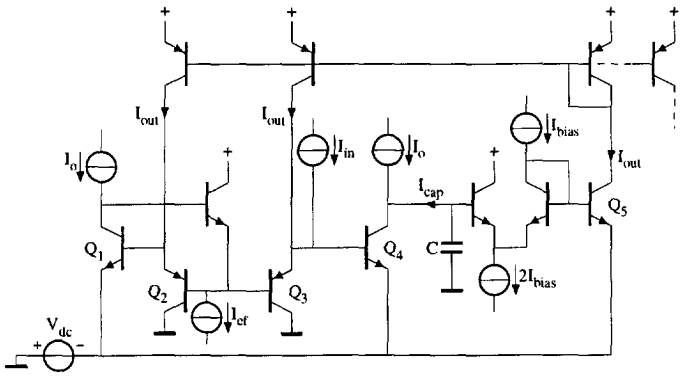

Figure 8.11: The complete signal path of the 1-V translinear integrator.

8.2.2 An application example for hearing instruments

Subsequently, the TL integrator is adopted for the design of a second-order Butterworth low-pass filter for hearing instruments. In this filter, the requirements shown in Table 8.1 have to be fulfilled [188].

Table 8.1: Filter requirements.

Quantity	Value	Comment
Supply voltage	1.1–1.6 V	
Bandwidth	100 Hz–8 kHz	-3 dB
Cut-off frequency	1.6 kHz–8 kHz	linearly adjustable in octaves
Dynamic range	> 56 dB	THD < 2%
Total capacitance:	< 200 pF	

The starting point is the second-order low-pass leapfrog filter as depicted in Fig. 8.12. This filter operates in the current domain and consists of two integrators. The input-output relation H_F of the filter is given by:

$$H_F = \frac{2H_I^2}{1 + 2H_I + 2H_I^2}, \tag{8.7}$$

H_I being the transfer function of the integrator. With $H_I = I_o/(sCU_T)$, this yields a Butterworth low-pass filter with cut-off frequency $f_c = I_o/(\pi\sqrt{2}CU_T)$. The filter circuit diagram is depicted in Fig. 8.13.

Only one bias current source, I_X, is necessary to ensure the correct biasing of the complete filter. Its value determines the maximum signal current the filter can handle and its DR. Since the circuit is biased in class A, the noise

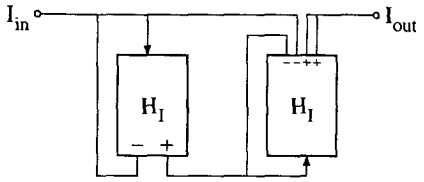

Figure 8.12: Second-order low-pass leapfrog filter operating in the current domain, consisting of two integrators (H_I).

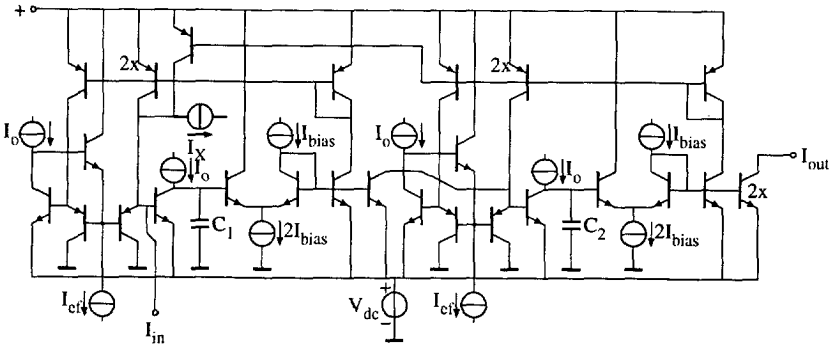

Figure 8.13: Circuit diagram of the second-order low-pass filter.

sources inside the circuit can be considered to be almost independent of the signal levels inside the filter. To estimate the DR of the filter, the major noise sources inside the filter, i.e., the collector shot noise sources, are shifted to the output. Then, the equivalent output noise power density spectrum is integrated over the total frequency range (from 100 Hz to 8 kHz) and compared to the maximum signal power. For sinusoidal signals, with $I_X = 400$ nA, $I_{bias} = 80$ nA, $V_{dc} = 200$ mV, $I_{in,max} = 180$ nA (peak value), $C_A = C_B = 50$ pF, $T = 308$ K (35 °C) and $I_o = 47$ nA ($f_c = 8$ kHz), this yields a DR of 59 dB. This value has been confirmed by simulation. With respect to the 56 dB DR requirement, this means that the bias sources are not permitted to produce more noise than the signal path of the complete filter. Even in low-voltage applications this requirement is easily met [189].

8.2.3 Measurement results

The control current I_o is realised by a PTAT[1] current source with a scaled indirect output [187]. The scaled output is generated by a controllable volt-

[1] Proportional-To-Absolute-Temperature

age source in series with the emitter of the output transistor. This results in the desired exponential relation between the control quantity and the cut-off frequency of the filter.

All the other biasing currents are derived from two scaled current mirrors with indirect outputs. The embodiment of the voltage source V_{dc} was inspired by the one used in [190] and adapted for our purpose. Its circuit diagram is depicted in Fig. 8.14. Three saturated transistors, Q_{V1}, Q_{V2} and Q_{V3}, generate a PTAT voltage of approximately 200 mV. Transistors Q_{V4}, Q_{V5} and Q_{V6} are connected in voltage-follower configuration, to generate a low-impedance version of this voltage. A PNP current mirror with multiple outputs delivers the necessary bias currents. Note that since, in general, a saturation voltage is a function of the ratio of the collector and the base current [189], the output voltage V_{dc} does not depend on the value of I_V. Also noise originating from I_V does not penetrate into V_{dc}. For $I_V = 0.5$ μA, the noise production of the voltage source itself appears to be sufficiently small.

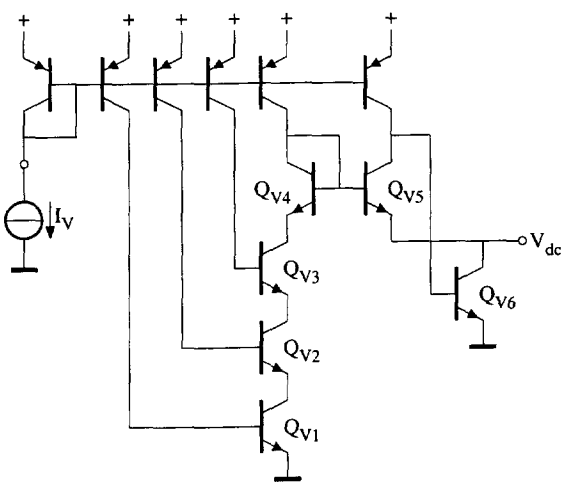

Figure 8.14: Realisation of the voltage source V_{dc}. The output voltage is independent of the value of I_V.

A semi-custom version of the active circuitry of the complete filter has been integrated in a standard 2-μm, 7-GHz process, fabricated at the Delft Institute of MicroElectronics and Submicron technology (DIMES). Typical transistor parameters are: $B_{F,NPN} \approx 100$, $f_{T,NPN} \approx 7$ GHz, $B_{F,LPNP} \approx 80$ and $f_{T,LPNP} \approx 40$ MHz. Experiments proved the correct operation of the filter. The filter characteristic is second-order Butterworth with the specifications shown in Table 8.2.

Table 8.2: Filter specifications.

Quantity	Value	Comment
Supply voltage	down to 1 V	
Bandwidth	0–80 kHz	
Pass-band transfer	+ 1.6 dB	
Stop-band attenuation	30 dB	
Cut-off frequency	1.6–8 kHz	linearly adjustable in octaves
Maximum signal current	220 nA_p	THD < 2%, 100 Hz–8 kHz
Dynamic range	57 dB	THD < 2%, 100 Hz–8 kHz
Supply current	6 μA	
PSRR	> 120 dBΩ	100 Hz–8 kHz
Total capacitance	100 pF	

Figure 8.15 depicts the measured output frequency spectrum with and without a 1 kHz, 70 nA (peak value) sine wave input signal. The cut-off frequency and supply voltage equal 8 kHz and 1.3 V, respectively. The plot clearly indicates that since the integrator is biased in class A, the output noise is not a function of the integrator input signal level.

Figure 8.16 depicts the measured output frequency spectrum for a 1 kHz, 220 nA (peak value) sine wave input signal using the same settings. The Total Harmonic Distortion (THD) mainly results from the second-order harmonic and equals 1.3%. Over the complete frequency range, i.e. from 100 Hz to 8 kHz, the THD remains below 2%.

8.3 A 1-volt class-AB translinear integrator

An important feature of TL circuits is the possibility of class-AB operation, which yields a larger dynamic range and a reduced average current consumption. As discussed in Section 3.3.3, class-AB operation is an inherent characteristic of sinh filters. The sinh output stage shown in Fig. 3.23 is not suitable for low-voltage operation due to the stacked topology of the TL loop. This section describes the design of a 1 volt sinh integrator, which is necessarily based on folded topologies. The integrator can be used as an elementary building block for the design of higher-order filters.

In Section 8.3.1, the block schematic of the integrator is described. Section 8.3.2 treats the design of the individual blocks. Finally, measurement results are presented in Section 8.3.3.

Much of the material in this section has been developed by, and in cooperation with, Paul Poort (1965–1997) and Wouter Serdijn [93].

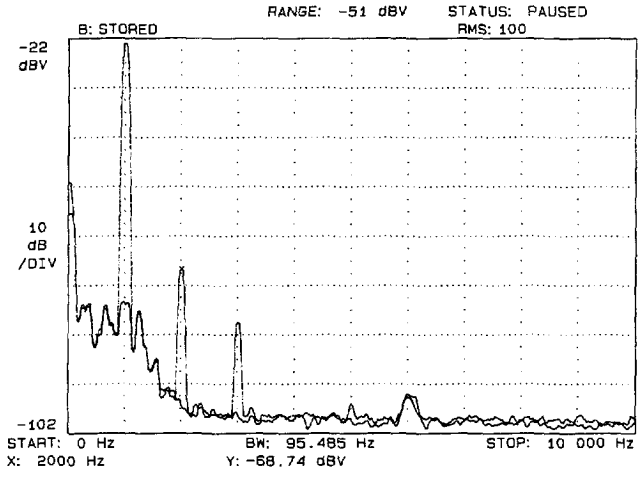

Figure 8.15: Measured output frequency spectrum with and without a 1 kHz, 70 nA (peak value) sine-wave input signal. The cut-off frequency and supply voltage equal 8 kHz and 1.3 V, respectively.

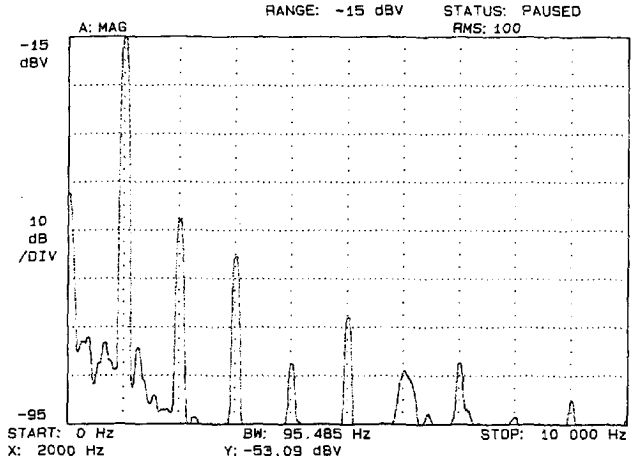

Figure 8.16: Measured output frequency spectrum for a 1-kHz, 220-nA (peak value) sine-wave input signal. The cut-off frequency and supply voltage equal 8 kHz and 1.3 V, respectively.

8.3.1 Block schematic of the integrator

Equation (3.36) describes the transfer function of a TL integrator. In sinh filters, the derivative $\dot{I}_{out}$ of the output current is implemented by eqn (3.72), which yields a current-mode polynomial:

$$I_{\text{cap}}\,(I_{\text{out}_1} + I_{\text{out}_2}) = I_{\text{o}} I_{\text{in}}. \tag{8.8}$$

The current I_{cap} to be supplied to the capacitance C is thus given by:

$$I_{\text{cap}} = \frac{I_{\text{o}} I_{\text{in}}}{I_{\text{out}_1} + I_{\text{out}_2}}. \tag{8.9}$$

A two-quadrant multiplier/divider is required to implement the Right-Hand Side (RHS) of eqn (8.9). Since a class-AB implementation is pursued, this two-quadrant multiplier/divider has to be realised by two one-quadrant multiplier/dividers. This is realised by splitting the input current into two strictly positive signals I_{in_1} and I_{in_2}, the difference of which equals I_{in}. Rewriting eqn (8.9) yields:

$$I_{\text{cap}} = \frac{I_{\text{o}} I_{\text{in}_1}}{I_{\text{out}_1} + I_{\text{out}_2}} - \frac{I_{\text{o}} I_{\text{in}_2}}{I_{\text{out}_1} + I_{\text{out}_2}}. \tag{8.10}$$

Equation (8.10) is the basis for the block schematic of the sinh integrator depicted in Fig. 8.17. At the input, a current splitter generates I_{in_1} and I_{in_2} from I_{in}. Subsequently, the currents I_{in_1} and I_{in_2} are divided by $I_{\text{out}_1} + I_{\text{out}_2}$ in two separate circuits. The current $I_{\text{out}_1} + I_{\text{out}_2}$ is obtained from the sinh output stage, a geometric mean current splitter. The output currents of the two multiplier/dividers are denoted by I_{cap1} and I_{cap2} and are respectively equal to the first and the second term on the RHS of eqn (8.10). Hence, the current supplied to the capacitance equals $I_{cap1} - I_{cap2}$. The use of a single capacitor is an advantage over the class-AB integrator proposed in [2] as it eliminates the necessity of matched capacitors. Finally, the capacitance voltage V_{cap} is applied to the sinh output stage via a voltage buffer to prevent interaction between the capacitance and the output stage.

8.3.2 Design of the individual blocks

The system blocks can be implemented by TL circuits, except of course the voltage buffer. To facilitate low-voltage operation, only folded TL loop topologies are allowed. A bipolar IC technology is used to implement the individual blocks.

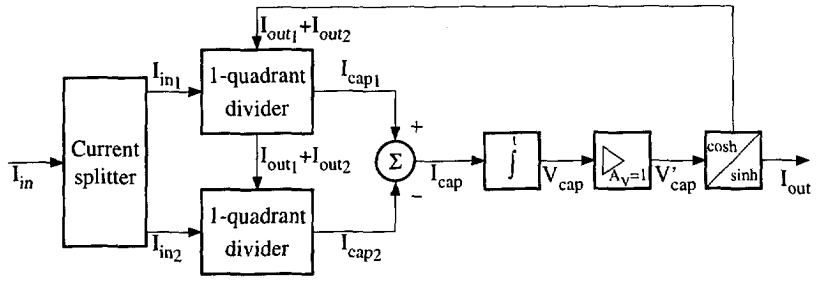

Figure 8.17: Block schematic of the class-AB translinear integrator.

Design of the input current splitter

A current splitter generates the currents I_{in_1} and I_{in_2} at the input of the integrator. In principle, the type of current splitter to be used at the input is not dictated by eqn (8.10). Hence, all possibilities discussed in Section 4.7 are valid choices. As the output stage is a geometric mean current splitter, the same function was chosen for the input current splitter.

The TL loop equation to be implemented is (4.101). Figure 8.18 depicts a 1 volt realisation of this equation. The core of the circuit is the TL loop formed by Q_1 through Q_4. Transistors Q_1 and Q_3 are biased by a dc current I_{dc_1}. Transistor Q_2 conducts I_{in_2}. This current is inverted by a PNP current mirror and added to I_{in}. The resulting current I_{in_1} is conducted by Q_4, which is enforced by the Common-Collector (CC) stage Q_5. Biasing of Q_5 by means of a dc tail current source of the differential pair Q_2-Q_3 requires a relatively high dc current. This is disadvantageous with respect to the quiescent current consumption. A solution is dynamic biasing. The tail current of Q_2-Q_3 is generated by Q_6, Q_7 and Q_9, and equals $3I_{\text{dc}_1} + I_{\text{in}_2}$. Hence, Q_5 is biased at a dc current equal to only $2I_{\text{dc}_1}$.

The voltage source V_{dc_1} is necessary to ensure that the Q_7 does not saturate. Note that this voltage source has no effect on the TL loop. A convenient value for V_{dc_1} is 200 mV.

Design of the multiplier/divider

Once the bipolar input current I_{in} is decomposed into two positive currents $I_{\text{in}_{1,2}}$, such that the difference of these currents equals I_{in}, the two-quadrant multiplication of I_{in} can now be performed by the individual division of I_{in_1} and I_{in_2} by $I_{\text{out}_1} + I_{\text{out}_2}$, by means of two one-quadrant multiplier/dividers. The output currents of the one-quadrant multiplier/dividers satisfy:

$$I_{\text{cap}_{1,2}} = \frac{I_o I_{\text{in}_{1,2}}}{I_{\text{out}_1} + I_{\text{out}_2}}. \tag{8.11}$$

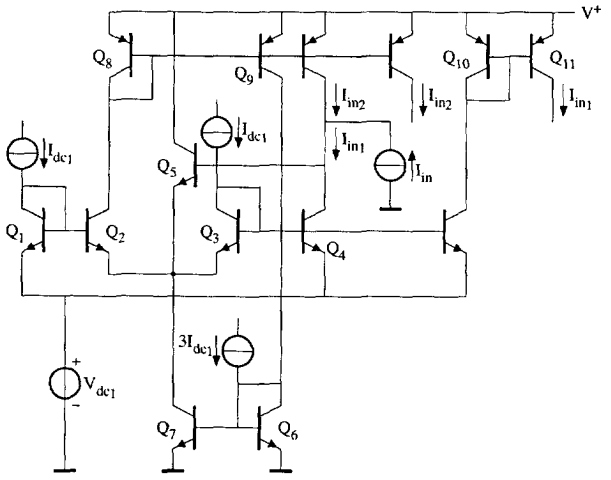

Figure 8.18: Implementation of the input current splitter.

As all linear factors in eqn (8.11) are strictly positive, it is a valid TL decomposition.

The 1 volt implementation of eqn (8.11) is shown in Fig. 8.19. The second-order TL loop comprises Q_{12}–Q_{15}. Transistors Q_{13} and Q_{14} are biased by supplying respectively the currents $I_{\text{out}_1} + I_{\text{out}_2}$ and $I_{\text{in}_{1,2}}$ to the emitters of these devices. The collector current I_o of Q_{12} is enforced by the CC stage Q_{16}, which is biased by a dc current I_{b_1}.

A voltage source V_{dc_2} is necessary to ensure that the base voltages of Q_{13} and Q_{14} are always positive. Again, 200 mV is a convenient value.

The output of the multiplier/divider is the collector current of Q_{15}. Subtraction of I_{cap_1} and I_{cap_2} is performed by a PNP current mirror inverting I_{cap_2}.

Design of the voltage buffer

The current $I_{\text{cap}_1} - I_{\text{cap}_2}$ is supplied to the capacitor resulting in the voltage V_{cap}. A voltage buffer is used to minimise the interaction between the capacitor and the sinh output stage. The principle of the buffer amplifier is depicted in Fig. 8.20(a). Ideally, the buffering is performed by the nullor. A level-shift between the input and the output of the buffer, represented by the voltage source V_{dc_3}, is necessary to avoid saturation of Q_{15} in the first multiplier/divider circuit. The output voltage is denoted by V'_{cap}.

The practical implementation of the nullor and the voltage source V_{dc_3} is shown in Fig. 8.20(b). The nullor is implemented by two Common-Emitter (CE) stages, Q_{19} and Q_{20}. The level-shift is realised by the base-emitter voltage of

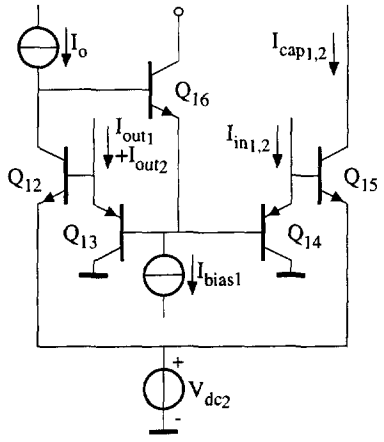

Figure 8.19: Implementation of the one-quadrant multiplier/divider.

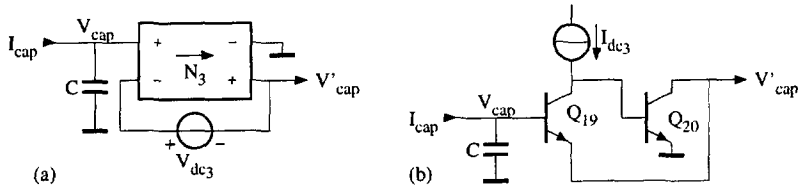

Figure 8.20: (a) Principle and (b) implementation of the voltage buffer.

Q_{19}. The output transistor Q_{20} must be able to sink the input current of the sinh output stage.

Design of the sinh output stage

The output stage has two functions. First, it enforces a geometric mean relation between the two output currents I_{out_1} and I_{out_2}. Secondly, it must provide the current $I_{\text{out}_1} + I_{\text{out}_2}$ to each of the multiplier/dividers, as shown in Fig. 8.17.

The 1 volt realisation of the output stage is depicted in Fig. 8.21. The TL loop comprising Q_{21}–Q_{24} implements the sinh function given by:

$$I_{\text{out}} = 2I_{\text{dc}_2} \sinh \frac{V'_{\text{cap}} - V_{\text{dc}_4}}{U_T}, \tag{8.12}$$

where I_{dc_2} is a dc current. Note that eqn (8.12) is equivalent to the geometric mean function $I^2_{\text{dc}_2} = I_{\text{out}_1} I_{\text{out}_2}$.

The current $I_{\text{out}_1} + I_{\text{out}_2}$ is supplied to the multiplier/dividers by means of PNP current mirrors. The output current I_{out} is generated by additional NPN

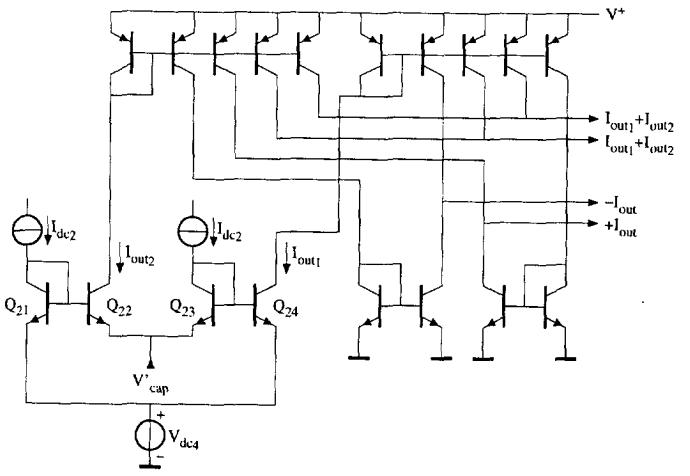

Figure 8.21: Implementation of the sinh output stage.

current mirrors. The inverted output current $-I_{\text{out}}$ is added to easily enclose the integrator in a unity-feedback configuration by connecting $-I_{\text{out}}$ to the input of the integrator, which results in a first-order low-pass filter.

The voltage source V_{dc_4} is necessary to ensure that the emitter voltages of Q_{22} and Q_{23} are always positive. Once again, 200 mV is a convenient value.

8.3.3 Measurement results

Now that all the individual system blocks have been designed at circuit level, the sub-circuits can be linked together to form the integrator as depicted in Fig. 8.17. For biasing purposes, the integrator is enclosed in a unity-feedback configuration, as discussed previously. This results in a first-order low-pass filter. Application of this filter in a hearing instrument was pursued. This leads to the required filter specifications shown in Table 8.3 [187]. For measurement purposes, the biasing current sources I_{dc_1}, I_{dc_2}, I_{b_1} and I_{b_2} are realised by simple current mirrors and high-valued resistors. The frequency control current I_{o} is realised with a PTAT current source.

To verify the operation of the filter in practice, a semi-custom version of the active circuitry of the complete filter has been integrated in the DIMES02 process. The dc currents are set to $I_{\text{dc}_1} = I_{\text{dc}_2} = I_{\text{b}_2} = 45$ nA, and $I_{\text{bias}_1} = 135$ nA.

The capacitor has a value of 100 pF and is connected externally. The voltage sources $V_{\text{dc}_{1,2,4}}$ equal 200 mV and are implemented by a resistive voltage divider.

Table 8.3: Filter requirements.

Quantity	Value	Comment
Supply voltage	down to 1 V	
Current consumption	$< 5\ \mu$A	$I_{\text{in,max}} = 180\ \text{nA}_\text{p}$
Cut-off frequency (f_c) range	1.6–8 kHz	controllable
Dynamic range	68 dB	100 Hz–8 kHz
Total harmonic distortion	$< 2\%$	$f = 1$ kHz, $f_\text{c} = 1.6$ kHz, $I_\text{in} < 130\ \text{nA}_\text{p}$
	$< 7\%$	$f = 1$ kHz, $f_\text{c} = 1.6$ kHz, $I_\text{in} > 130\ \text{nA}_\text{p}$

The measurement results are summarised in Table 8.4 and are in good agreement with the expectations.

Table 8.4: Filter specifications.

Quantity	Value	Comment
Minimal supply voltage	0.95 V	
Supply current	1.9 μA	$I_\text{in} = 180\ \text{nA}_\text{p}$
Quiescent supply current	1.6 μA	
Cut-off frequency range	1– > 8 kHz	
Dynamic range	73 dB	100 Hz–8 kHz
Total harmonic distortion	2.7%	$f_\text{in} = 1$ kHz, $f_\text{c} = 1.6$ kHz, $I_\text{in} = 180\ \text{nA}_\text{p}$

8.4 A dynamic translinear RMS-DC converter

In the literature, the DTL principle has been used mainly to implement filters, i.e. *linear* DEs. However, conventional (static) TL circuits are well-known for the wide variety of non-linear functions they can implement. Obviously, the DTL principle can be applied just as well to the implementation of *non-linear* DEs, thus extending the applicability of the DTL principle.

A simple example of a non-linear dynamic transfer function is RMS-DC conversion, which is a basic function used in many signal processing applications [191]. The RMS-DC function is used in this section to demonstrate the applicability of the DTL principle to the implementation of non-linear DEs.

The design of an RMS-DC converter based on the DTL principle is treated in Section 8.4.1. Measurement results of a semicustom IC realisation are presented in Section 8.4.2.

8.4.1 Design of the RMS-DC converter

The STL principle already plays a key role in conventional implementations of RMS-DC converters [62, 191]. A well-known block schematic of an RMS-DC converter is shown in Fig. 8.22. The system consists of two separate functions: a squarer-divider and a low-pass filter.

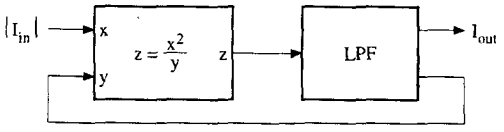

Figure 8.22: Block schematic of a conventional RMS-DC converter.

The core of the implementation of the squarer-divider is a second-order TL loop. This loop calculates the current $I_{\text{in}}^2/I_{\text{out}}$, where I_{in} and I_{out} are the input and output current of the RMS-DC converter, respectively. The output current I_{out} equals the mean value of $I_{\text{in}}^2/I_{\text{out}}$:

$$I_{\text{out}} = \left\langle \frac{I_{\text{in}}^2}{I_{\text{out}}} \right\rangle, \tag{8.13}$$

where $< \cdots >$ represents the averaging operation, i.e., the low-pass filter shown in Fig. 8.22. By dividing I_{in}^2 by I_{out}, instead of applying a square-root function to the mean of I_{in}^2, the requirements on the offsets in the system are relaxed [191, 192].

In most implementations of the system shown in Fig. 8.22, a squarer-divider facilitating one-quadrant operation is used. In that case, the TL loop is preceded by a full-wave rectifier.

The low-pass filter function is often just first-order. In most cases, it is implemented by means of a simple RC section.

The key role of the TL technique could be enlarged by realising the low-pass filter by a TL filter. However, as in that case both system functions are implemented in the 'translinear domain', there is actually no reason why these two functions have to be treated as separate system blocks. By merging the two functions into one system block, a higher functional density can be obtained. To this end, we start at a higher hierarchical level, describing the RMS-DC function by means of a DE.

The current-mode description of a TL first-order low-pass filter is given by:

$$CU_T\dot{I}_y + I_o I_y = I_o I_x, \tag{8.14}$$

where I_o is a dc bias current and the current I_y is the low-pass filtered version of I_x. For low frequencies, the transfer of this filter equals one. The cut-off frequency ω_c of the filter is given by:

$$\omega_c = \frac{I_o}{CU_T}. \tag{8.15}$$

In the RMS-DC conversion given by eqn (8.13), the filtering operation is not performed on the input signal I_{in}, but on the current I_{in}^2/I_{out}. That is, the variable I_x in eqn (8.14) equals I_{in}^2/I_{out}. The output current I_y of the filter equals the output current I_{out} of the RMS-DC converter. Applying these two substitutions to eqn (8.14), the DE describing a first-order RMS-DC conversion is found:

$$CU_T \dot{I}_{out} I_{out} + I_o I_{out}^2 = I_o I_{in}^2. \tag{8.16}$$

Obviously, this is a *non-linear* DE.

Higher-order RMS-DC converters can be designed by choosing a higher-order low-pass filter, instead of eqn (8.14).

Definition of the capacitance current

According to the DTL principle, the derivative of a current can be replaced by a product of currents. In other words, by introducing a capacitance current, the derivative $\dot{I}_{out}$ can be eliminated from eqn (8.16). The capacitance current is introduced through the circuit shown in Fig. 8.23, which is a slightly modified version of the circuit shown in Fig. 2.7. In Fig. 8.23, the capacitance $\frac{1}{2}C$ is connected in a loop with two base-emitter junctions. The two transistors have a collector current equal to I_{out}. The capacitance current shown in Fig. 8.23, which is described by eqn (2.20) with $I_C = I_{out}$, can be used to eliminate $\dot{I}_{out}$ from eqn (8.16). The result is a current-mode polynomial:

$$(I_{cap} + I_o)\, I_{out}^2 = I_o I_{in}^2. \tag{8.17}$$

Translinear decomposition and implementation

Since all factors in eqn (8.17) are positive, if the input current is full-wave rectified, which is common practice [191], they can be mapped directly onto the collector currents of a third-order TL loop, comprising six transistors. Two possible implementations are shown in Fig. 8.24,[2] where C' equals $\frac{1}{2}C$. In both circuits, the TL loop is formed by transistors Q_1–Q_6. In Fig. 8.24(a), the quadratic factor I_{out}^2 is implemented by Q_5-Q_6. The structure C'-Q_4-Q_5-Q_6 is

[2]The circuit shown in Fig. 8.24(a) was invented independently by Frey [23].

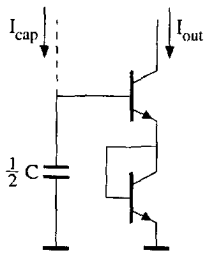

Figure 8.23: Output stage of the dynamic translinear RMS-DC converter introducing I_{cap}.

identical to the sub-circuit shown in Fig. 8.23, except for Q_4. Since Q_4 is biased by a dc current, it acts as a dc voltage source and consequently does not change the capacitance current introduced in Fig. 8.23.

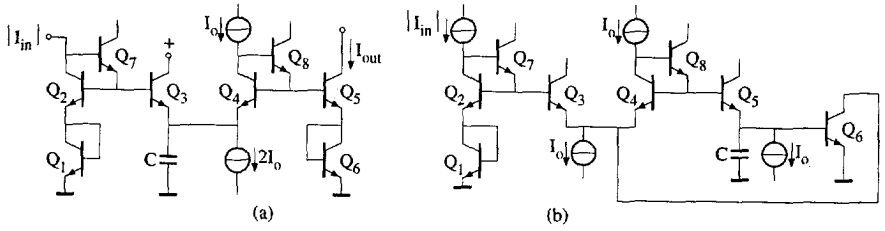

Figure 8.24: Two implementations of a dynamic translinear RMS-DC converter.

Dynamic translinear circuits not only inherit the advantages of STL circuits, but also the disadvantages and error sources. An important error source is the finite current gain of the bipolar transistor. With respect to this problem, the most sensitive point of the circuit shown in Fig. 8.24(a) is the node connecting the bases of Q_2 and Q_3. The collector current $(I_o + I_{cap})$ of Q_3 can be much larger than $|I_{in}|$. Using a diode connection to force $|I_{in}|$ through Q_2 would result in significant errors, as the base current of Q_3 is not always negligible with respect to $|I_{in}|$. The problem can be solved by using a buffer amplifier. In Fig. 8.24(a), Q_7 is a simple implementation of this buffer. The other CC stage, transistor Q_8, buffers the bases of Q_4 and Q_5.

8.4.2 Measurement results

The RMS-DC converter shown in Fig. 8.24(a) was implemented on a semi-custom IC in DIMES02, a 7 GHz bipolar process. The bias current sources I_o are implemented by simple current mirrors.

Full-wave rectification and voltage-to-current conversion is accomplished by means of the set-up shown in Fig. 8.25. An HP33120A Arbitrary Wave-form Generator is programmed to supply a full-wave rectified output voltage, thus excluding the non-idealities of the alternative, an on-chip full-wave rectifier. The output voltage of the generator is converted to a current using a 47 kΩ resistor. The combination of a discrete op amp and a discrete PNP transistor is used as a current buffer. The output current of this buffer is the input current $|I_{in}|$ of the RMS-DC converter. The output current of the RMS-DC converter is measured across a 47 kΩ resistor. To facilitate a sufficient voltage range across the output resistor, a supply voltage of 4 V is used for the RMS-DC converter, though its minimum supply voltage is only 2 V. The bias current I_o has a value of 85 μA.

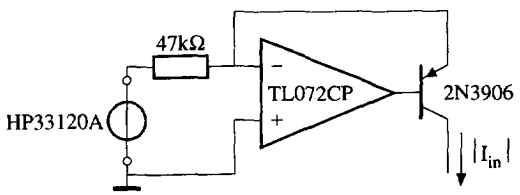

Figure 8.25: Measurement set-up.

In Fig. 8.26, the relevant currents flowing in the RMS-DC converter are shown. The figure illustrates the non-linear relation between the capacitance current I_{cap} and the output current I_{out}. Further, it shows that I_{cap} can have much larger values than $|I_{in}|$. In this figure, C' is 47 nF, which yields a cut-off frequency of 5.5 kHz. The input frequency is only 12 kHz, which explains the ripple on I_{out}. The capacitance current is measured across a 4.7 kΩ resistor. The output voltage of the generator is 2 V_p.

For the next two measurements, a capacitor of 4.7 μF is used, which yields a cut-off frequency of 55 Hz. Figure 8.27 shows the measured relative error for a rectified sine wave at a frequency of 100 kHz, as a function of the amplitude. In this figure, V_{in} is the voltage supplied by the generator. For low values of V_{in}, the error curve is dominated by offsets in the measurement set-up and the RMS-DC converter, and by the limited bandwidth of the transistors at low current levels. For intermediate input levels, the curve shows a scaling error due to mismatches of the source and load resistors and of the transistors in the TL loop. For values of V_{in} above 4 V, the output transistor of the RMS-DC converter starts to saturate.

The error of the output of the RMS-DC converter as a function of the frequency is shown in Fig. 8.28 for various values of the input voltage V_{in}.

The -3 dB cut-off frequency of the transfer function could not be measured due to the limited frequency range (5 MHz) of the signal generator.

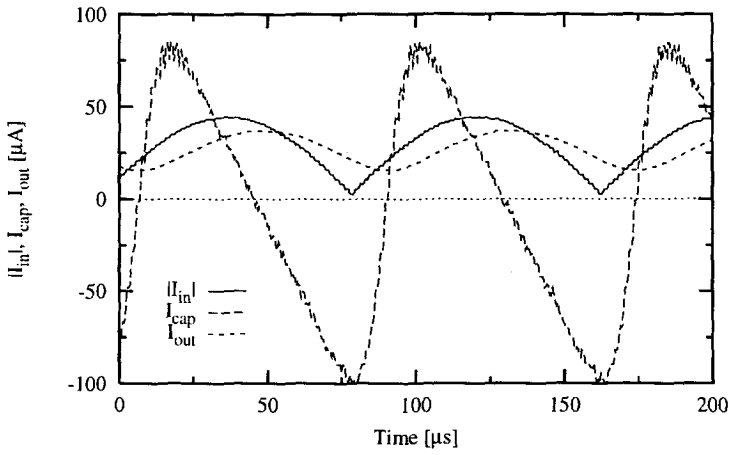

Figure 8.26: Measurement of the currents $|I_{\text{in}}|$, I_{cap} and I_{out}.

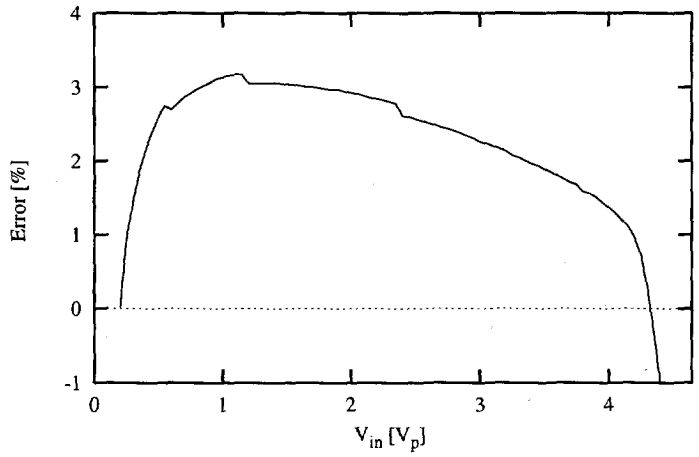

Figure 8.27: Measured error versus input voltage.

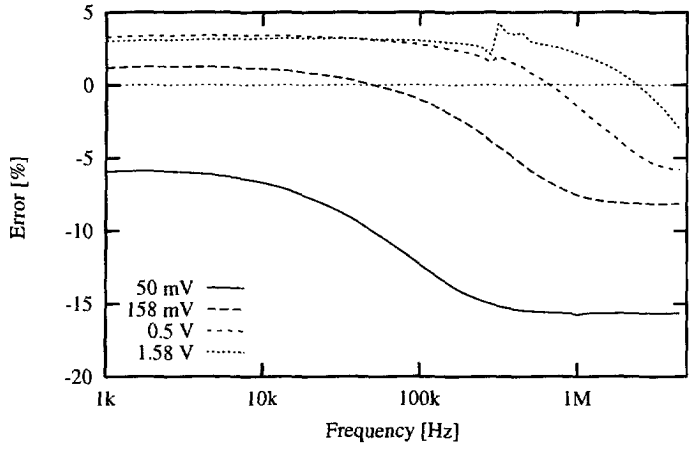

Figure 8.28: Measured frequency response.

The worst-case wave form for an RMS measurement is a rectangular pulse train, where all energy is contained in the pulses. The collector current of Q_3, shown in Fig. 8.24(a), takes its maximum value $I_{3,\max}$ during the peaks of the input signal. The value of $I_{3,max}$ can be derived from eqn (8.17), and is given by:

$$I_{3,\max} = CF^2\, I_o, \tag{8.18}$$

where CF is the crest factor, the ratio between the peak value and the RMS value of the input signal.

For high crest factors, $I_{3,\max}$ becomes quite large, and as a consequence, transistor Q_3, which is minimum-sized, no longer behaves exponentially during the peaks, due to parasitic resistances and β_F high-current roll-off. Therefore, to perform a measurement of the error as a function of the crest factor, the current I_o is scaled down to 850 nA. The input resistor, shown in Fig. 8.25, and the output resistor are scaled up by a factor 100. The input voltage V_{in} switches between a bias level of 0.15 V and a certain peak voltage V_{peak}. The duty cycle and the peak voltage V_{peak} are varied to obtain different crest factors at a constant RMS value of 0.4 V. The pulse width of the peak is constant and equals 200 μs. Figure 8.29 shows the measured additional error as a function of the crest factor. The error remains below 1% for crest factors up to 10.

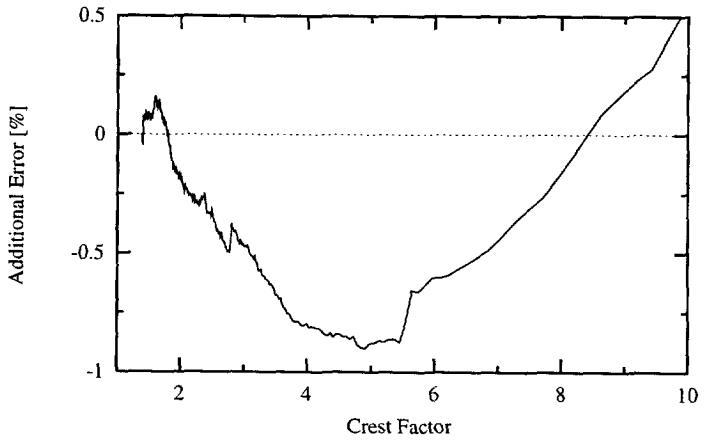

Figure 8.29: Additional error versus crest factor.

8.5 A 3.3-volt current-controlled voltage-translinear oscillator

In MOS IC processes, TL filters can be realised by operating the MOS transistors in the subthreshold region, see, e.g., [5]. However, subthreshold operation is limited to low frequencies. Fortunately, the general companding principle on which TL filters are based can be generalised to MOS transistors operating in strong inversion, as discussed in Section 2.3.2.

In this section, the design of a $\sqrt{}$-domain current-controlled oscillator is described. In Section 8.5.1, the square law conformance is verified for the MOS transistors in the process used to the design the oscillator. Section 8.5.2 treats the design of a VTL integrator. Based on the integrator, a current-controlled harmonic oscillator is designed, described in Section 8.5.3. An experimental prototype of the oscillator was realised in the DiMOS process. The measurement results are presented in Section 8.5.4.

8.5.1 Square law conformance

Both the static and dynamic voltage-translinear principles, described in Section 2.3, rely on the quadratic behaviour of the MOS transistor operating in strong inversion. However, the square law is quite a coarse simplification [117], as discussed in Section 7.1. It is only valid across approximately 1.5 decades of current [70]. At the low end, the square law is limited by the moderate inversion region. At the high end, it is limited by carrier mobility reduction. The square law is far less exact than the exponential law, describing the bipolar transistor,

on which the TL principle is based. Therefore, it is advisable to check the range of validity of the square law model beforehand.

Some measurements were performed on the DiMOS CMOS process, which was used to implement the $\sqrt{}$-domain oscillator described in this section. In Fig. 8.30, a measurement is shown for an MOS transistor having dimensions $W = L = 20$ μm. The drain current was measured for gate voltages from 0.7 V to 3 V; higher gate voltages are not very interesting for low-voltage operation. The measured drain current was fitted on the ideal square law, eqn (2.25). To emphasise the difference between the measured and the fitted curve in the moderate inversion region, the drain current is plotted on a logarithmic scale. The fitted parameters are $V_{\text{th}} = 0.815$ V and $\beta = 56.8$ μA/V^2. The corresponding error curve, depicted on the second y-axis, shows that the fit is accurate to within 1 % for drain currents ranging from 5.6 μA to more than 135 μA, which corresponds to more than 1.4 decades of drain current. Although this range is much smaller than the validity of the exponential law for the bipolar transistor, which is valid across approximately six to ten decades, it is sufficient to justify the application of the simple square law model.

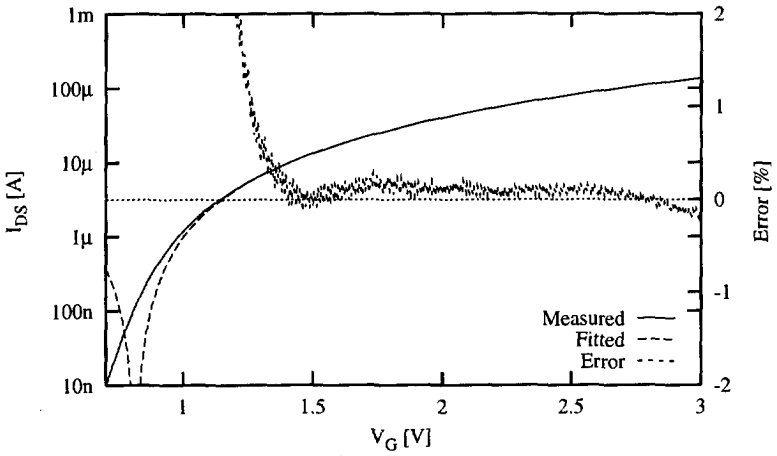

Figure 8.30: Measured and fitted drain current, and the error between the measurement and the fitted square law.

8.5.2 Design of a voltage-translinear integrator

Any integrator can be described by the dimensionless DE:

$$\dot{z} = x, \tag{8.19}$$

where the dot represent differentiation with respect to the dimensionless time τ and x and z represent the input and output signal, respectively.

In order to implement an integrator using the design principles discussed in Section 2.3, eqn (8.19) has to be transformed into a DE with the proper dimensions. As both the Static Voltage-TransLinear (SVTL) principle and the DVTL principle are basically current-mode, it is obvious that x and z have to be transformed into currents. This is accomplished by defining the equivalence relations, see eqn (4.4):

$$x = \frac{I_{\text{in}}}{I_{\text{o}}}, \qquad z = \frac{I_{\text{out}}}{I_{\text{o}}}, \tag{8.20}$$

where I_{in} and I_{out} are the input and output current of the integrator, respectively, and I_{o} is an arbitrary dc current.

The dimensionless time τ implicitly present in eqn (8.19) has to be transformed into the usual time t with dimension $[s]$. This can be done by applying the transformation:

$$\frac{\mathrm{d}}{\mathrm{d}\tau} = \frac{C\sqrt{I_{\text{o}_1}}}{\sqrt{2\beta}I_{\text{o}_2}}\frac{\mathrm{d}}{\mathrm{d}t}, \tag{8.21}$$

where I_{o_1} and I_{o_2} are dc bias currents. From this equation, it follows directly that frequency, the inverse of time t, is linearly controllable through I_{o_2}.

Applying the above transformations, a DE is obtained having the proper dimensions for a DVTL implementation to be possible:

$$\frac{C\sqrt{I_{\text{o}_1}}}{\sqrt{2\beta}}\dot{I}_{\text{out}} = I_{\text{o}_2}I_{\text{in}}. \tag{8.22}$$

The derivative $\dot{I}_{\text{out}}$ in eqn (8.22) can be eliminated by introducing a capacitance current I_{cap} according to eqn (2.32) with $I_{\text{DS}} = I_{\text{out}}$, corresponding to Fig. 2.11. Using eqn (2.32) to eliminate the derivative $\dot{I}_{\text{out}}$ from (8.19) an algebraic equation is obtained:

$$\sqrt{I_{\text{out}}I_{\text{o}_1}}I_{\text{cap}} = I_{\text{o}_2}I_{\text{in}}. \tag{8.23}$$

If we are able to implement this equation, we have actually implemented the integrator described by eqn (8.22). To implement eqn (8.23), the SVTL principle can be used. Equation (8.23) has to be mapped onto one or more VTL loop equations, see (2.27). Unfortunately, no analytical synthesis methods for mapping algebraic equations onto VTL loop equations exist [70]. The numerical method described in [70] cannot be used either, since it is limited to single-loop four-transistor circuits having one input, one output and one bias current. In eqn (8.23), an input current, and output current, two bias currents I_{o_1} and

I_{o_2}, and a capacitance current are present. The only alternative is to split eqn (8.23) into several simpler parts, which can be realised by existing VTL circuits. The term $\sqrt{I_{\text{out}} I_{o_1}}$ can be realised by a square-root circuit [67]. Next, a multiplier/divider can be used to realise the product $I_{o_2} I_{\text{in}}$ and divide it by the output of the square-root circuit [69,70]. Then the output of the multiplier is the capacitance current I_{cap}. The output stage shown in Fig. 2.11 defines the relation between I_{cap} and I_{out}. A block schematic of the solution thus obtained is shown in Fig. 8.31.

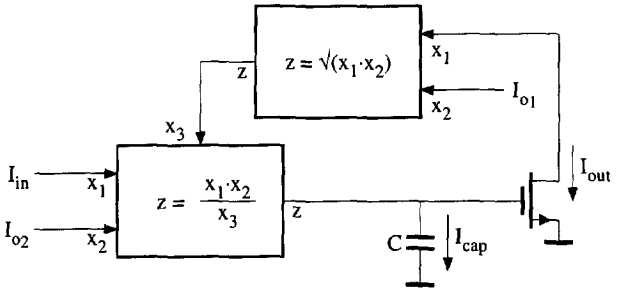

Figure 8.31: Block schematic of a voltage-translinear integrator.

Square-root circuit

An SVTL square-root circuit was published in [67,70]. The circuit is depicted in Fig. 8.32. Its loop equation is given by:

$$\sqrt{I_{x_1}} + \sqrt{I_{x_2}} = 2\sqrt{\frac{I_{x_1} + I_{x_2}}{4} + I_z}, \tag{8.24}$$

where I_{x_1} and I_{x_2} are two input currents and $I_z = \frac{1}{2}\sqrt{I_{x_1} I_{x_2}}$ is the output current of the square-root circuit. The relation between these currents and Fig. 8.31 is given by: $I_{x_1} = I_{\text{out}}$, $I_{x_2} = I_{o_1}$ and $I_z = \frac{1}{2}\sqrt{I_{o_1} I_{\text{out}}}$.

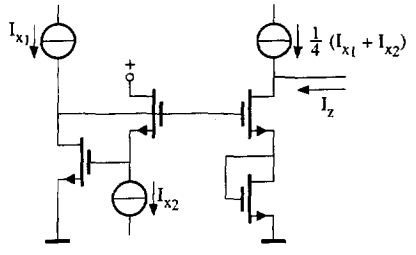

Figure 8.32: Square-root circuit, stacked topology [67,70].

A disadvantage of the circuit shown in Fig. 8.32 is that it is based on a stacked VTL loop, which is sensitive to body effect [70]. Due to the body effect, the threshold voltages of the MOS transistors in a stacked loop differ. As a consequence, errors are introduced in the general equation (2.27) unless all transistors have individual wells connected to their sources, which is disadvantageous with respect to bandwidth.

In folded topologies, the influence of the body effect is much smaller. Therefore, a new square-root circuit is designed by mapping eqn (8.24) onto a VTL loop in folded topology. The resulting circuit is shown in Fig. 8.33. Transistors M_1–M_4 make up the VTL core. The dimensions chosen for M_1 through M_4 are $W = 10$ μm and $L = 12$ μm. The current mirror M_5-M_6 is used to supply both M_2 and M_3 with the output current I_z, see eqn (8.24). The aspect ratio of the current mirror transistors is chosen to be quite large, to gain some voltage room for the transistors of the VTL core at low supply voltages. The dimensions of M_5 and M_6 are $W = 200$ μm and $L = 8$ μm.

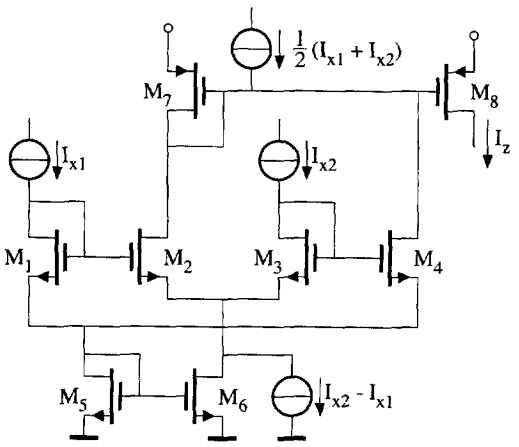

Figure 8.33: Square-root circuit, folded topology.

Multiplier

Multiplier circuits are often based on the well-known quarter-square principle: $(a+b)^2 - (a-b)^2 = 4ab$. Using this expression, a multiplier can be constructed from two square circuits. In [69, 70], four-quadrant VTL multipliers are presented, which are based on the quarter-square principle. The resulting circuits have a kind of 'differential difference' input structure.

The multiplier described in [70] is based on VTL loops in folded topology, which are insensitive to the body effect. This circuit is shown in Fig. 8.34. The VTL core of the two square circuits is formed by M_1–M_4 and M_{11}–M_{14}.

The output currents of the square circuits are subtracted by means of a PMOS current mirror, yielding the output current I_z of the four-quadrant multiplier, which is given by $I_z = I_{x_1} I_{x_2}/(2I_{x_3})$. This current is supplied to the capacitor shown in Fig. 8.31. The relations between the input currents I_{x_1}, I_{x_2} and I_{x_3} and the output current I_z of the multiplier shown in Fig. 8.34, and the currents in the block schematic shown in Fig. 8.31 are given by: $I_{x_1} = I_{\text{in}}$, $I_{x_2} = I_{o_2}$, $I_{x_3} = \frac{1}{2}\sqrt{I_{o_1} I_{\text{out}}}$ and $I_z = I_{\text{cap}}$.

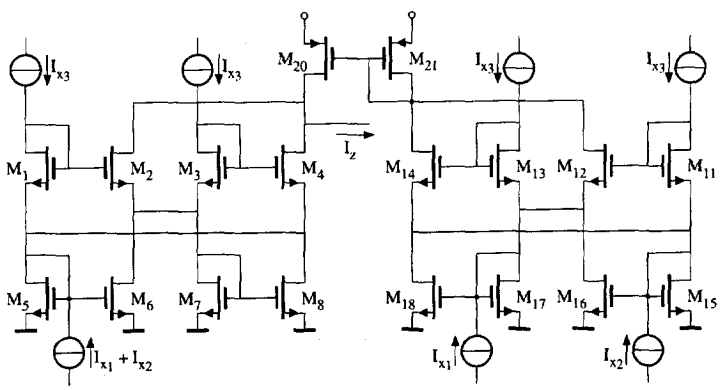

Figure 8.34: Four-quadrant multiplier/divider [70].

For reasons of voltage compatibility between the PMOS current mirror load of the multiplier and the integrator output transistor, a PMOS output transistor is used for the integrator. By choosing equal dimensions for the output PMOS transistor as for the PMOS transistors comprising the current mirror, the two output voltages of the square circuits, comprising the multiplier, are identical, thus reducing the even-order distortion of the multiplier.

Complete voltage-translinear integrator

Employing the square-root circuit, shown in Fig. 8.33, and the multiplier, depicted in Fig. 8.34, in the block schematic, shown in Fig. 8.31, the complete $\sqrt{}$-domain integrator thus obtained is depicted in Fig. 8.35. Note that the $\sqrt{}$-domain output structure is not part of any VTL loop. The output of the integrator has to be class-A biased. Therefore, a dc bias current source is connected from the drain of the output transistor of the integrator to ground.

8.5.3 Design of the oscillator

The integrator described in the previous section was used to design a current-controlled harmonic oscillator. By applying negative feedback to a cascade of

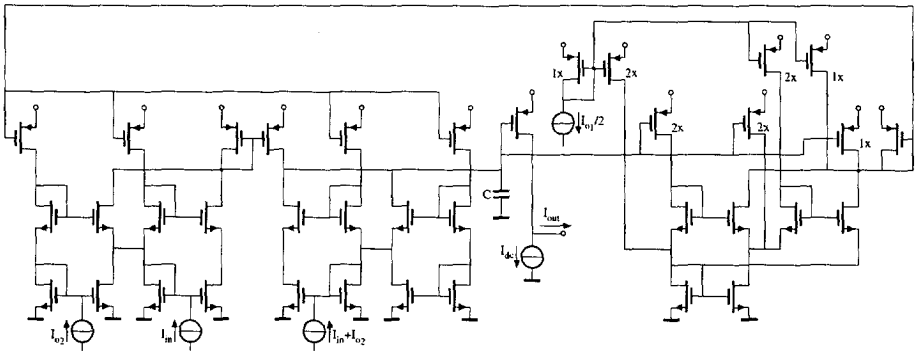

Figure 8.35: A $\sqrt{}$-domain integrator.

two integrators, a two-integrator oscillator is obtained. The block schematic of the realised oscillator is shown in Fig. 8.36. The oscillation frequency of the loop equals the unity-gain frequency of the integrators, which is given by:

$$\omega_c = \frac{\sqrt{2\beta} I_{o_2}}{C\sqrt{I_{o_1}}}. \tag{8.25}$$

The oscillation frequency can be tuned linearly by means of I_{o_2}.

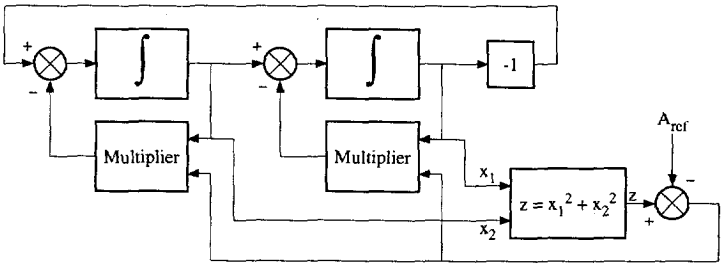

Figure 8.36: Two-integrator oscillator.

A loop of two integrators and an inverter is described by a linear DE, which cannot posses a unique limit cycle. In other words, an amplitude control circuit is required, which is also depicted in Fig. 8.36. A fixed amplitude is maintained by controlling the amount of local feedback of the integrators. Negative feedback causes a decrease of the oscillation amplitude, positive feedback causes an increase. To be able to apply both positive and negative feedback to the integrators, a four-quadrant multiplier is required in the local feedback paths. The VTL multiplier shown in Fig. 8.34 is used to this end.

The integrator, shown in Fig. 8.35, has a differential input structure. Therefore, it is not necessary to convert the output of the multiplier to a single output current by means of the PMOS current mirror shown in Fig. 8.34. Since the output voltage levels of M_4 and M_{14}, shown in Fig. 8.34, are not compatible with the input voltage levels of the integrator, it is necessary to load the two square circuits, comprising the multiplier, with two PMOS current mirrors. The differential output current of these two current mirrors is supplied to the differential input of the integrator.

The amplitude is measured by adding the squares of the two quadrature outputs of the oscillator, yielding the square of the amplitude [103]. Two VTL square circuits, which were also employed in the multiplier shown in Fig. 8.34, can be used to this end. The output currents of the square circuits are added by connecting the output terminals. The square of the oscillation amplitude, thus obtained, is compared with a reference current. The difference is applied to the second input of the feedback multipliers, thus controlling the local feedback of the integrators.

In the set-up shown in Fig. 8.36, the amplitude and the frequency can be tuned independently [103], by means of I_{o_2} and A_{ref}, respectively.

8.5.4 Measurement results

To verify the DVTL principle, the current-controlled $\sqrt{}$-domain oscillator was realised in DiMOS, a 1.6 μm n-well CMOS process, fabricated at the Delft Institute of MicroElectronics and Submicron Technology. For measurement purposes, the two capacitors of the oscillator are connected externally. All dc bias and control currents are supplied externally as well. The oscillator occupies a chip area of 0.65 mm^2. Most of the area is consumed by the current mirrors, which are operated in the moderate inversion region to gain some voltage room. The oscillator is designed for a supply voltage of 3.3 V.

Figure 8.37 shows the quadrature output currents of the oscillator. The output currents of the two integrators are measured across two 100 kΩ resistors. The dc current used to bias the integrators in class A is 5 μA. The oscillation amplitude is 3.6 μA, which is 72% of the class-A bias current. The capacitors have a value of 82 pF. The control currents I_{o_1} and I_{o_2} are 5 μA and 3.1 μA, respectively. With eqn (8.25), this amounts to an oscillation frequency of 28 kHz. The measured oscillation frequency is 22 kHz.

Figure 8.38 shows the measured output spectrum of the oscillator. To prevent distortion caused by the output voltage swing across the load resistor in relation to the output conductance of the output MOS transistor, an external common-base stage is used to buffer the output current. The harmonic distortion is mainly caused by the second and third harmonics at -46 dB and -45 dB, respectively.

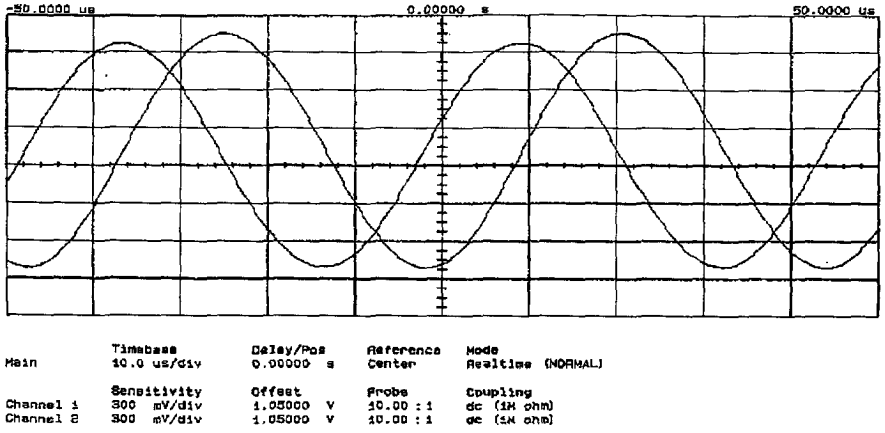

Figure 8.37: Measured output currents of the oscillator.

The frequency tunability as a function of I_{o_2} was measured for the same values of the capacitors and the bias currents. The results are shown in Fig. 8.39. The figure shows that the oscillator is linearly tunable from about 2.6 kHz to 53 kHz. For large values of the control current I_{o_2}, correct operation of the VTL integrator is prohibited by the limited supply voltage.

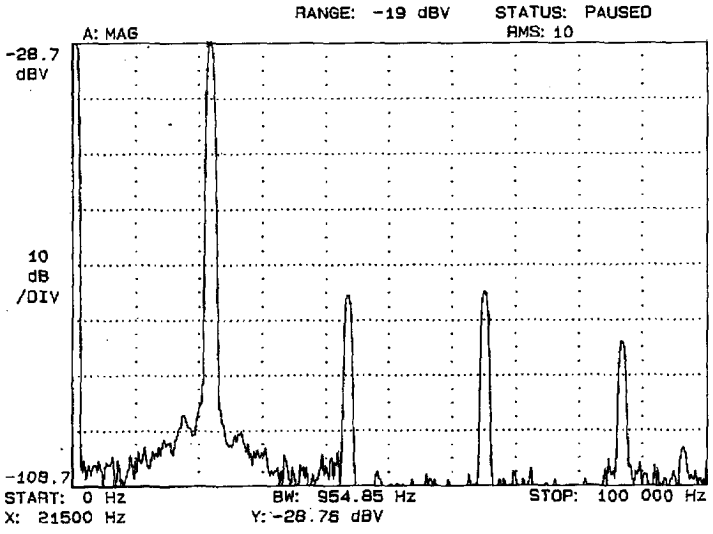

Figure 8.38: Frequency spectrum of the oscillator.

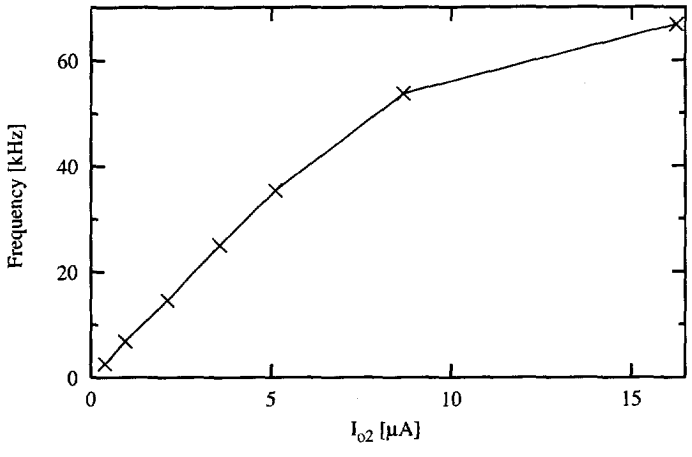

Figure 8.39: Frequency control of the oscillator.

9

Conclusions

The introduction of the capacitance as a basic TransLinear (TL) network element significantly extends the applicability of these circuits. As a result, next to the static transfer functions, both linear and non-linear, facilitated by conventional 'Static TransLinear' (STL) technology, a wide variety of frequency-dependent (transfer) functions can be realised. The resulting class of 'Dynamic TransLinear' (DTL) circuits implements differential equations; both linear differential equations, describing linear filters, and non-linear differential equations, describing, e.g. oscillators, RMS-DC converters and PLLs can be realised.

Translinear filters are especially suitable for those applications that do require a large dynamic range, but do not need a high signal-to-noise ratio. Most specifications obtainable with bipolar-transistor TL filters are comparable to the specifications of bipolar-transistor-only g_mC filters. This applies, e.g., to the signal-to-noise ratio, the bandwidth, the power consumption and the tunability characteristics. However, a significantly better dynamic range specification can be realised owing to the theoretical (external) linearity of TL filters. The dynamic range of TL filters can even exceed the dynamic range of opamp-MOSFET-C filters, especially at low supply voltages. Subthreshold MOS implementations are particularly useful in the area of analogue VLSI (neural) networks owing to the high versatility of TL technology, offering both linear and non-linear, static and dynamic (transfer) functions, and the high functional density.

Translinear circuits are typical examples of current-mode signal processing. Information is carried primarily by currents, whereas voltages are only of secondary interest. As a consequence, TL networks are best described in terms of currents. This applies both to STL and DTL circuitry. The current-mode approach has the additional major advantage that the existing theory on STL circuits becomes directly applicable to DTL circuits. In particular, the existing

design methodology for STL circuits has to be supplemented by only one additional step, the definition of capacitance currents, to facilitate synthesis of DTL circuits. This extension is based on the 'Dynamic Translinear Principle'. As well as the conventional STL principle, the DTL principle is a *current-mode* formulation of the underlying fundamental design principle. It relates the capacitance currents to the currents representing the memory of the circuit. The resulting structured synthesis methodology is more general than alternative methods proposed in the literature and covers the design of both linear and non-linear, STL and DTL circuits.

A powerful synthesis method must go together with a general analysis method in the same domain. Current-mode analysis of DTL circuits is simple. It is based on current-mode expressions for the capacitance currents. Both a global and a state-space approach can be applied. The state-space method is less general, but has the advantage of a limited intermediate expression swell.

The analysis method developed even facilitates the analysis of noise in both STL and DTL circuits, which is non-trivial due to the exponential transistor characteristics and the non-stationary nature of the transistor noise sources. The resulting signal $\times$ noise intermodulation causes the noise level to increase with the processed signal power.

In MOS technology, in weak inversion, additional design options arise from the application of the back-gate, operation in the triode region and application of floating-gate MOS transistors. On the other hand, the poor matching characteristics and the low drain current levels restrict the utilisation of MOS designs to non-demanding applications.

In the strong inversion region, the square law behaviour of the MOS transistor can be used to implement 'Voltage-Translinear' circuits. In addition to the conventional (static) voltage-translinear principle, a 'Dynamic Voltage-Translinear Principle' can be formulated. Though of academic interest, voltage-translinear circuits are not very relevant in practice.

Dynamic translinear circuits are a promising and challenging approach for overcoming the dynamic range and bandwidth limitations that conventional analogue electronics techniques are facing due to ever lower supply voltages, low power consumption and high-frequency demands. As a consequence, the literature demonstrates an increasing interest for this rapidly developing circuit paradigm. In recent years, the emphasis in the literature has been on synthesis methods. At present, research efforts are shifted towards the investigation of the specific merits and demerits of (D)TL circuits. In particular, many papers appear on the investigation of noise and other second-order effects.

Ultimately, and this is the main recommendation for further research, the results of these efforts have to be combined so as to result in an even more powerful synthesis method. Disclosing the relations between important specifications, such as noise, bandwidth and power consumption, and the possible

choices along the design trajectory will provide feedback to the electronics designer at an early stage of the design. This, in turn, will speed up the synthesis process. In addition, this issue is of crucial importance for automation of (part of) the design process. As evidenced by this thesis, the current-mode approach is best suited to meet these challenges.

A

Additional design examples

This appendix presents three additional design examples of Dynamic TransLinear (DTL) circuits. As opposed to the realisations presented in Chapter 8, the circuits described in this appendix have been verified only through simulation and are not supported by measurements.

Section A.1 presents a TransLinear (TL) filter that uses syllabic companding to increase the dynamic range [78,83]. A theoretically distortionless companding scheme is implemented. Section A.2 shows that sinh filters are not necessarily based on the geometric mean output stage. A sinh integrator based on a harmonic mean output stage is designed. Finally, Section A.3 presents the synthesis of a second-order low-pass filter to illustrate the generalised class of DTL circuits proposed in Section 4.3.4.

A.1 A syllabic companding translinear filter

Since the voltages in a TL filter are logarithmically related to the currents, these filters are inherently *instantaneous* companding. At current level, TL filters are not companding; the input current I_{in} is directly processed by the filter. As a consequence, the current signal swing is limited by the dc bias current I_{dc} for class-A operated TL filters, such as log-domain and tanh filters. For TL filters operating in class AB, e.g., sinh filters, the current signal swing is limited, in practice, by second-order effects, such as the finite transistor current gain factor, the parasitic emitter resistance and the low value of f_{T} at low current levels.

For both class-A and class-AB TL filters, the current signal swing, and hence the dynamic range, can be enlarged through the application of *syllabic* companding. The nature of syllabic companding is different from the instantaneous companding inherently present. In a syllabic companding set-up, the input current I_{in} is compressed by multiplying it by a non-negative signal g, re-

sulting in a compressed current I_{in}^*. This compressed current is supplied to the core TL filter. When the signal g is a suitable function of the average strength of I_{in}, the core TL filter will only have to process relatively small signals, i.e., I_{in}^*, irrespective of the amplitude of I_{in}.

In Section 2.1, it is shown that (syllabic) companding can be accomplished theoretically without introducing distortion. To accomplish this, the state variables have to be 'updated' by a certain compensation signal as a function of the compression signal g [76, 79]. The particular appearance of the compensation signal is basically independent of the filter implementation used [75]. Only the impact of the required compensation signal on the companding circuit is different for different filter implementation techniques. For example, in g_mC filters, (some of) the transconductances have to be tuned by this compensation term [82].

This section describes the design of a (theoretically distortionless) syllabic companding TL filter. Section A.1.1 explains the principle of distortionless syllabic companding in the context of TL filters. The TL filter implementation is described next, in Section A.1.2. Finally, Section A.1.3 presents simulation results.

A.1.1 Distortionless syllabic companding

Figure A.1 depicts a simple TL first-order low-pass filter, which is described by the Differential Equation (DE):

$$CU_T\dot{I}_{\text{out}} + I_{\text{o}}I_{\text{out}} = I_{\text{o}}I_{\text{in}}, \tag{A.1}$$

where C is a capacitance, U_T is the thermal voltage kT/q, I_{in}, I_{out} and I_{o} are respectively the filter input current, the output current and a dc current. The dot represents differentiation with respect to time.

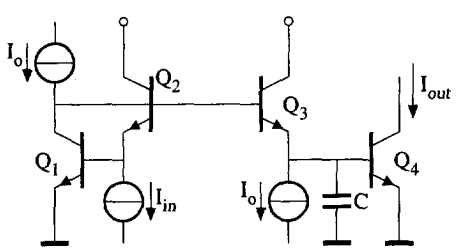

Figure A.1: A first-order low-pass filter.

In a syllabic companding filter set-up, the input current I_{in} is divided by a (dimensionless) compression signal $g \neq 0$ and the resulting compressed input current I_{in}^* is applied to the actual filter. The output current I_{out} is obtained

by multiplying the compressed output I^*_{out} by the same factor g. The relation between I_{in} and I^*_{in} and between I_{out} and I^*_{out} is described by:

$$gI^*_{\text{in}} = I_{\text{in}}, \tag{A.2}$$

$$gI^*_{\text{out}} = I_{\text{out}}. \tag{A.3}$$

If the filter shown in Fig. A.1 is used in a syllabic companding set-up, the uncompressed currents I_{in} and I_{out} are no longer available to this filter. Therefore, eqn (A.1) has to be rewritten in terms of the compressed currents. Eqns (A.2) and (A.3) can be used directly to eliminate I_{in} and I_{out}, respectively. An expression for the derivative $\dot{I}_{\text{out}}$ can be found from the time derivative of eqn (A.3), given by:

$$\dot{I}_{\text{out}} = g\dot{I}^*_{\text{out}} + \dot{g}I^*_{\text{out}}. \tag{A.4}$$

In terms of the compressed currents, eqn (A.1) becomes:

$$CU_T\dot{I}^*_{\text{out}} + \left(I_{\text{o}} + CU_T\frac{\dot{g}}{g}\right)I^*_{\text{out}} = I_{\text{o}}I^*_{\text{in}}. \tag{A.5}$$

The term $I^*_{\text{out}}CU_T\dot{g}/g$ is in fact the compensation signal that ensures *distortionless* companding. Without this term, significant intermodulation distortion results when the frequency of the compression signal g is not well beneath the signal frequency band.

Note that the compensation signal has the dimension of a current. Therefore, we denote this signal by the current I_{C_g}:

$$I_{C_g} = CU_T\frac{\dot{g}}{g}. \tag{A.6}$$

In eqn (A.1), the term $I_{\text{o}}I_{\text{out}}$ accounts for the loss of the integrator shown in Fig. A.1. This loss term is implemented by the current source I_{o} in parallel with the capacitor C. Comparing eqns (A.1) and (A.5), we see that the current I_{C_g} has to be added to the current source I_{o} to establish distortionless companding.

Higher-order filters

The above description can be generalised to filters of n^{th}-order. In the general case of an n^{th}-order filter, the state-space description is multiplied by a time-varying $n \times n$ matrix $\mathbf{G}$, of which all n^2 elements can, in principle, be different functions [75]. An implementation of the general principle will however result in a considerable overhead. The result will be a fully connected filter topology, requiring n^2 multipliers, dividers and generators of the different elements of G. Furthermore, at present, the benefits of such an elaborate implementation

over less general ones are not clear. Therefore, we will restrict ourselves to the situation in which one multiplier is placed in front of the core TL filter. This is equivalent to a matrix $G = gI$, where g is a single compression function and I is the identity matrix of order n. For TL filters, in this special case, the same compensation current I_{C_g} has to be distributed to all the capacitors in the n^{th}-order filter.

Class-A operation

In TL filters operating in class A, the actual ac input current I_{in} is always superposed on a dc bias current I_{dc}. This bias current limits the maximum input signal level, and hence, the dynamic range of the filter. The dynamic range can be enlarged by compressing I_{in} before entering the filter. Obviously, I_{dc} should not be compressed. Otherwise, the input modulation index m does not change, and hence the dynamic range does not improve. Consequently, the compressed input current I^*_{in}, instead of I_{in}, should be superposed on I_{dc}.

However, companding introduces local non-linear behaviour. As a consequence, the superposition principle cannot be applied if I_{in} is compressed, but I_{dc} is not. If a current $I_{\text{dc}} + I^*_{\text{in}}$ is applied to Q_2, shown in Fig. A.1, the compressed output current I^*_{out} will contain an error term. In particular, the relation between I^*_{in} and I^*_{out} is now described by:

$$CU_T\dot{I}^*_{out} + I^*_{out}(I_o + I_{C_g}) + I_{C_g}I_{dc} = I_oI^*_{in}. \tag{A.7}$$

A comparison of eqns (A.5) and (A.7) reveals the error: the term $I_{C_g}I_{\text{dc}}$ on the left-hand side of (A.7).

The error term depends on the compression signal g, but not on the input signal I_{in}. Therefore, in a differential filter set-up, which is common practice, the error term is a common mode signal and is eliminated in the differential mode output current.

A.1.2 Translinear implementation

Next, we apply the above theory on syllabic companding to the TL filter shown in Fig. A.2. The circuit comprises two TL loops, Q_1–Q_6 and Q_7–Q_{10} and is described by the DE:

$$C^2U_T^2\ddot{I}_{\text{out}} + \tfrac{1}{2}CU_TI_o\dot{I}_{\text{out}} + I_o^2I_{\text{out}} = I_o^2I_{\text{in}}. \tag{A.8}$$

This equation describes a second-order low-pass filter with a cut-off frequency given by $\omega_c = I_o/(CU_T)$ and a Q of two.

The filter shown in Fig. A.2 was used in the differential set-up shown in Fig. A.3.

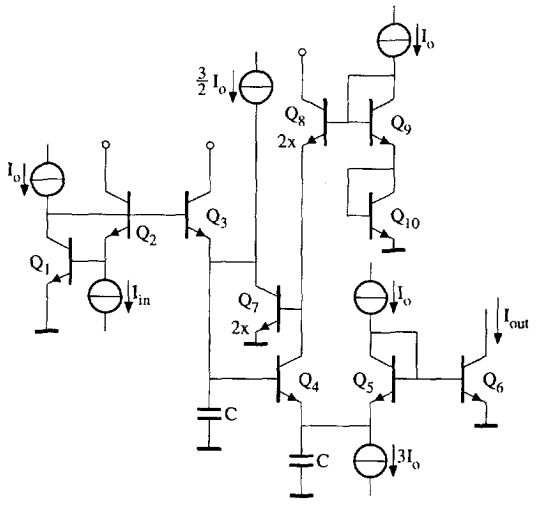

Figure A.2: A second-order low-pass translinear filter.

Multiplication

Multiplication and division by g can be performed by TL circuits, if g is equated to a ratio of currents, see eqn (4.4):

$$g = \frac{I_g}{I_{og}}, \tag{A.9}$$

where I_{og} is a dc current.

The dynamic range of the multipliers and dividers are of crucial importance with respect to the dynamic range of the complete companding filter. Therefore, these circuits have to operate in class AB, see, e.g., Fig. 4.36. The second-order effects of the multipliers and dividers introduce distortion and will therefore limit the dynamic range of the companding filter. The set-up shown in Fig. A.3 is favourable in comparison with class-AB TL filters or dynamically biased class-A filters [84], as the requirements on the core TL filter are substantially relaxed. In addition, the multipliers and dividers are simple static TL circuits and therefore, the influence of second-order effects can be decreased more easily by careful design.

Generation of the compression signal

The compression signal current I_g has to be some measure of average strength of the input signal. A possible implementation is depicted in Fig. A.3, where I_g is the output of a low-pass filter acting on the absolute value of I_{in}.

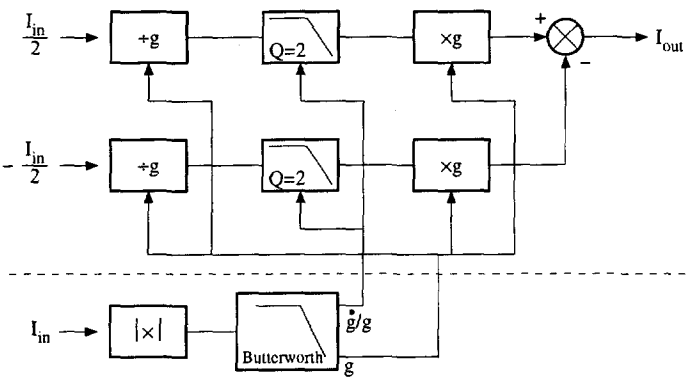

Figure A.3: Block schematic of a syllabic companding differential filter.

The accuracy of the circuit generating I_g does not have to be high [82]. The only constraint is that the relation between I_g and I_{C_g} is accurate. Hence, the design of the absolute value circuit and the low-pass filter is not difficult. The low-pass filter was implemented by cascading two of the low-pass sections shown in Fig. A.1 and applying unity negative feedback, resulting in a second-order Butterworth low-pass filter, shown in Fig. A.4.

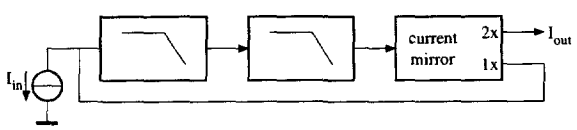

Figure A.4: A second-order Butterworth filter.

Generation of the compensation current

The compensation current I_{C_g} can be obtained from the TL sub-circuit shown in Fig. A.5. If the collector current in this figure is I_g, and the base current is negligible, the capacitance current is given by:

$$I_{C_g} = CU_T \frac{\dot{I}_g}{I_g}, \tag{A.10}$$

which is exactly the required compensation current.

Since the current I_g is the output current of the Butterworth filter and the sub-circuit shown in Fig. A.5 equals the output structure of the Butterworth filter, see Fig. A.1, no additional hardware is required to generate I_{C_g}. Current mirrors can be used to distribute the current $(I_{C_g} + I_o)$, flowing through Q_3,

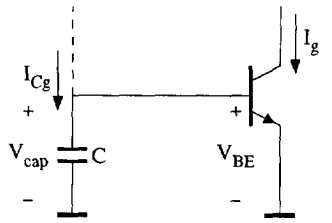

Figure A.5: Generation of the compensation current.

shown in Fig. A.1, to all the capacitors in the actual TL filter. A constraint is, of course, that the capacitor shown in Fig. A.1 is matched to the capacitors in the actual TL filter depicted in Fig. A.2.

In [82], it is shown that the same compensation current $I_{C_g} = CU_T\dot{g}/g$ is required in syllabic companding g_mC filters, where it is used to tune (some of) the transconductances. Hence, the substructure shown in Fig. A.5 can be used for companding g_mC filters as well.

A.1.3 Simulation results

Simulations using realistic IC transistor models were performed to verify the correct operation of the syllabic companding set-up shown in Fig. A.3. The value of the capacitors in the filters shown in Fig. A.2 and in Fig. A.1 is chosen to be 1.2 nF.

For the bias current I_o in the core filter, shown in Fig. A.2, a value of 2 μA is used, resulting in a cut-off frequency of 10 kHz. A dc current of 2 μA is added to the input of the filter to facilitate class-A operation. Since the filter has a Q of 2 and a differential set-up is used, the input current swing is limited to 2 μA.

The cut-off frequency of the Butterworth filter is designed to equal 5 kHz, which is only a factor two below the cut-off frequency of the companding filter. As a consequence, the envelope of the input current can be tracked very quickly. A dc current of 0.5 μA is added to the input to prevent I_g from becoming zero when no input is applied to the filter.

The value of I_{og} in eqn (A.9) is 0.7 μA. Thus, the amplification of very small input signals is limited to 1.4; this is the ratio of I_{og} and the dc input current of the Butterworth filter. An ideal divider and multiplier are used in the simulations.

First, the second-order filter shown in Fig. A.2 was simulated outside the companding set-up. Without syllabic companding, the third-order harmonic distortion of the filter, used in a differential set-up, is -76 dB at ω_c, with an input amplitude of 0.8 μA.

To demonstrate the beneficial influence of the compensation current I_{C_g}, a large-signal ac analysis was performed with and without the addition of I_{C_g} to the capacitors in the filter. The results are shown in Fig. A.6. The input amplitude is again 0.8 μA. Figure A.6(a) depicts the situation without compensation. Clearly, the output current contains a very large third-order harmonic. When I_{C_g} is added to all capacitors in the filter, the result shown in Fig. A.6(b) is obtained. The improvement with respect to Fig. A.6(a) is obvious.

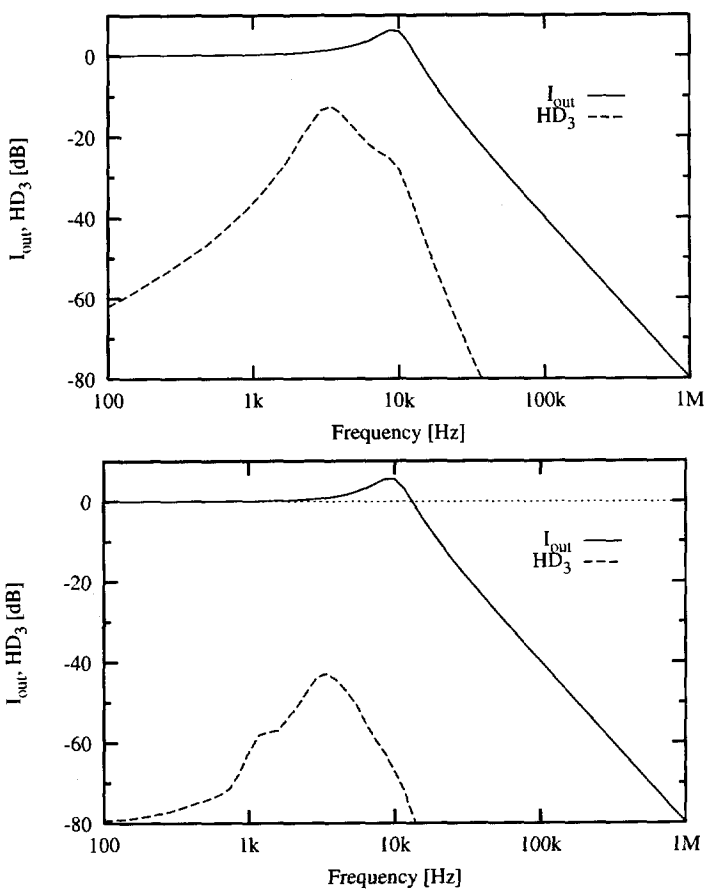

Figure A.6: Syllabic companding (**a**) without and (**b**) with compensation for distortion.

A transient simulation demonstrates the increase of the input current swing due to syllabic companding. The input current used in the simulations shown in Fig. A.7 is a sine wave with a switching amplitude. The input frequency is

10 kHz. For reference, Fig. A.7(a) shows the output current without syllabic companding. The amplitude of the input sine wave switches from 20 nA to 100 nA. In Fig. A.7(b), the amplitude switches from 20 μA to 100 μA. Although this is a factor of 50 beyond the original input signal range, the same response as shown in Fig. A.7(a) is obtained, except for some Q degradation, which illustrates the significant improvement in DR range obtainable from applying (theoretically distortionless) syllabic companding. The Q degradation is caused by the finite β_F of the circuit generating the compensation current, depicted in Fig. A.5. For large input signals, I_g becomes large. This is illustrated by Fig. A.8, which corresponds to the simulation of Fig. A.7(b). Consequently, the base current added to I_{C_g} is no longer negligible. For $I_g = 40$ μA, approximately 200 nA is added to I_{C_g}. This extra current is distributed to all the capacitors in the actual TL filter, where it causes deviations of Q and ω_c. A voltage buffer might be used to improve the relation between I_g and I_{C_g} for large input currents.

A.2 A harmonic mean class-AB integrator

The general class of DTL circuits comprises several sub-classes, based on different output stages, see Section 3.3. Three types of output structures have been published to date, which are named after their V-I transfer functions. These are: log-domain, tanh and sinh filters [10].

In sinh filters, the output current I_{out} is split into two strictly positive currents I_{out_1} and I_{out_2}, the difference of which equals the actual output current, i.e.:

$$I_{out} = I_{out_1} - I_{out_2}. \tag{A.11}$$

A second equation is required to determine I_{out_1} and I_{out_2} so that they are strictly positive. The geometric mean control law, or product law, can be used to this end:

$$I_{out_1} I_{out_2} = I_{dc_1}^2, \tag{A.12}$$

where I_{dc_1} is the dc quiescent current. That is, when I_{out} is zero, both I_{out_1} and I_{out_2} equal I_{dc_1}.

Figure A.9(a) shows an implementation of eqn (A.12) by means of a TL loop comprising transistors Q_1 through Q_4. Transistors Q_1 and Q_2 are biased at I_{dc_1}, whereas Q_3 and Q_4 conduct I_{out_2} and I_{out_1}, respectively. The value of I_{out} is determined by the capacitance voltage V_{cap} via a hyperbolic sine relation. The voltage follower sinks the emitter current of Q_3.

Unfortunately, the geometric mean control law exhibits a serious disadvantage. For $|I_{out}| \gg I_{dc_1}$, either I_{out_1} or I_{out_2} tends to zero. As a result, the circuit becomes more vulnerable to second-order effects: the transit frequency

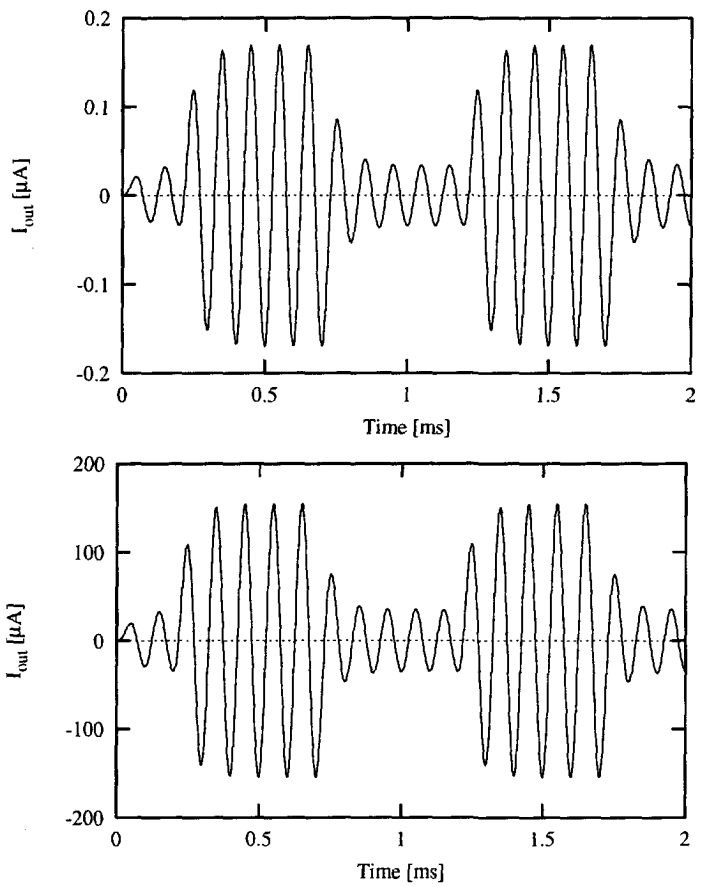

Figure A.7: Transient simulation (**a**) without and (**b**) with syllabic companding.

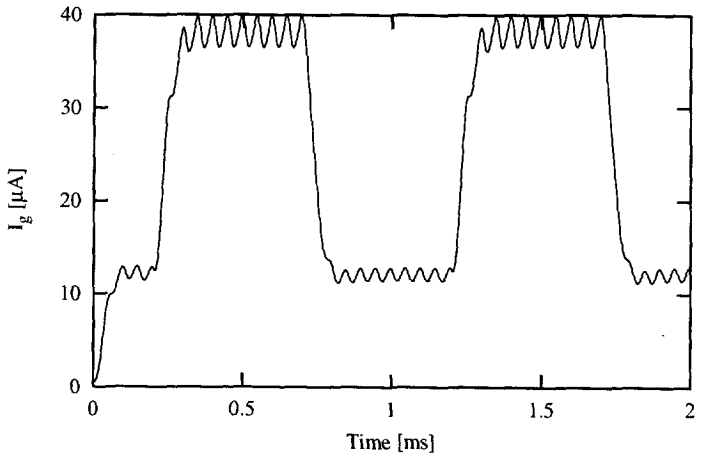

Figure A.8: Compression signal I_g for a large input current.

f_T of Q_4 or Q_3 decreases drastically and the influence of finite base currents becomes more pronounced.

An interesting alternative is to use the harmonic mean control law instead. In op amp circuits, this solution has proven to be very effective [55]. Instead of eqn (A.12), a harmonic mean output stage is characterised by:

$$2I_{\text{out}_1} I_{\text{out}_2} = (I_{\text{out}_1} + I_{\text{out}_2})\, I_{\text{dc}_1}. \tag{A.13}$$

For large values of $|I_{\text{out}}|$, I_{out_1} or I_{out_2} now asymptotically approach the value of $\frac{1}{2}I_{\text{dc}_1}$ instead of zero. The harmonic mean function thus provides fundamentally better performance.

A possible implementation of eqn (A.13) is depicted in Fig. A.9(b). The collector currents of Q_1–Q_4, which form a TL loop, are respectively given by I_{dc_1}, $(I_{\text{out}_1} + I_{\text{out}_2})$, I_{out_2} and I_{out_1}. The doubled emitter area of Q_1 implements the factor 2 shown in eqn (A.13).

A.2.1 Capacitance currents

Using the current-mode approach, the output stages of the different DTL subclasses are characterised by their generic expressions for the capacitance currents. For sinh filters, the capacitance current I_{cap} is derived from I_{out_1}, as shown in Fig. A.9(a), and is given by eqns (3.69)–(3.69).

Using the harmonic instead of the geometric mean output stage, the question arises how to define I_{cap}. One might be tempted to derive I_{cap} from I_{out_1} as in eqn (3.69). In practice, this will work when $|I_{\text{out}}|$ is not much greater than I_{dc_1}.

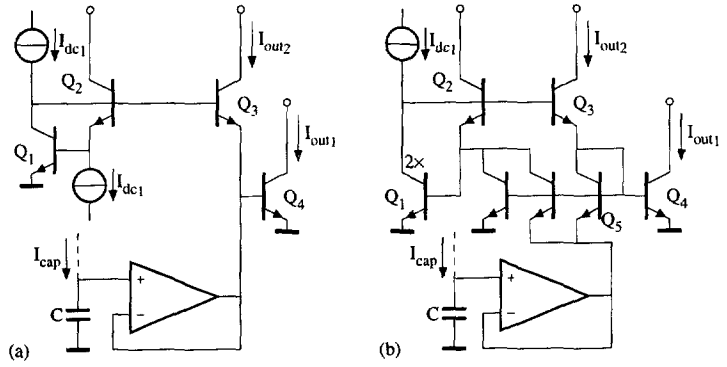

Figure A.9: Two sinh output stages: (**a**) based on the geometric mean, and (**b**) based on the harmonic mean.

However, for $|I_{\text{out}}| \gg I_{\text{dc}_1}$, the corresponding capacitance voltage V_{cap} becomes constant and will fail to control I_{out} effectively.

A more suitable (and symmetric) definition of I_{cap} is given by:

$$I_{\text{cap}} = CU_T \left(\frac{\dot{I}_{\text{out}_1}}{I_{\text{out}_1}} - \frac{\dot{I}_{\text{out}_2}}{I_{\text{out}_2}} \right). \tag{A.14}$$

This definition is implemented in the output stage shown in Fig. A.9(b) by the loop C-Q_5-Q_4. Note that Q_5 is not part of the TL loop. Elaboration of eqn (A.14) in terms of $\dot{I}_{\text{out}}$, using (A.11) and (A.13), yields:

$$I_{\text{cap}} = CU_T \frac{\dot{I}_{\text{out}}}{I_{\text{out}_1} + I_{\text{out}_2} - I_{\text{dc}_1}}. \tag{A.15}$$

Using a voltage-mode approach to analyse the output stage, it is easily verified that V_{cap} and I_{out} are related by a hyperbolic sine function. Hence, the circuit shown in Fig. A.9(b) is in fact also a sinh output stage, but now based on the harmonic mean control law.

A.2.2 Design of the integrator

A possible application of the proposed output stage principle is a current-mode integrator, which can be used for the construction of higher-order filters. Here, we present the design of such an integrator for a 1-volt supply V_{DD}.

The DE of a TL integrator is given by:

$$CU_T \dot{I}_{\text{out}} = I_o I_{\text{in}}, \tag{A.16}$$

where I_{in} denotes the integrator input current. Using eqn (A.15) to implement the derivative $CU_T\dot{I}_{\text{out}}$, a current-mode polynomial is obtained:

$$I_{\text{cap}}\,(I_{\text{out}_1} + I_{\text{out}_2} - I_{\text{dc}_1}) = I_{\text{o}} I_{\text{in}}. \tag{A.17}$$

Since $(I_{\text{out}_1} + I_{\text{out}_2} - I_{\text{dc}_1})$ and I_{o} are strictly positive, while I_{cap} and I_{in} take on bipolar values, a two-quadrant multiplier is required to implement eqn (A.17). To facilitate class-AB operation of the complete integrator, the multiplier has to operate in class AB as well. Class-AB two-quadrant multiplication can be accomplished using two one-quadrant multipliers. To this end, using a current splitter, I_{in} is split into two strictly positive currents I_{in_1} and I_{in_2}, where $I_{\text{in}} = I_{\text{in}_1} - I_{\text{in}_2}$. The currents $I_{\text{in}_{1,2}}$ are applied to two one-quadrant multipliers, the output currents of which equal I_{C_1} and I_{C_2}, respectively. The latter currents are related to I_{cap} by $I_{\text{cap}} = I_{C_1} - I_{C_2}$. Hence, the one-quadrant multipliers are described by the TL loop equations:

$$I_{C_1}\,(I_{\text{out}_1} + I_{\text{out}_2} - I_{\text{dc}_1}) = I_{\text{o}} I_{\text{in}_1}, \tag{A.18a}$$

$$I_{C_2}\,(I_{\text{out}_1} + I_{\text{out}_2} - I_{\text{dc}_1}) = I_{\text{o}} I_{\text{in}_2}. \tag{A.18b}$$

To implement the complete class-AB integrator, the blocks to be realised are: the output stage, described by eqns (A.13) and (A.14), two one-quadrant multipliers, described by (A.18a) and (A.18b), and an input current splitter.

Output stage

The circuit shown in Fig. A.9 is unsuitable for low-voltage environments due to the stacked nature of the TL loop Q_1–Q_4. Figure A.10 shows an implementation based on a folded TL loop, which does enable 1-volt operation. Transistors Q_1 through Q_4 implement a second-order TL loop. The bases of Q_1 and Q_4 are connected to a dc voltage V_{dc}. The collector currents of Q_1–Q_4 are respectively given by $(I_{\text{out}_1} + I_{\text{out}_2})$, I_{out_2}, I_{dc_1} and I_{out_1}. Biasing of Q_1 and Q_3 is accomplished by means of simple nullor constructions. That is, the two common-emitter (CE) stages, which sink the tail currents of the differential pairs Q_1-Q_2 and Q_3-Q_4. The value of I_{out} is determined by V_{cap}. Transistor Q_5 conducts I_{out_2}. The collector currents of Q_4 and Q_5 are added and supplied to Q_1 by means of PNP current mirrors. The loop formed by Q_5, Q_4 and the capacitor C implements eqn (A.14). Since C is connected to a base terminal, in principle, a voltage follower, as shown in Fig. A.9(b) is not required.

Second-order effects introduce distortion and noise. Several techniques can be applied to reduce their influence [50]. For example, it is better in practice to connect the capacitor between the bases of Q_5 and Q_4. In that case, V_{dc} is not part of the capacitance-junctions loop and therefore noise and disturbances of V_{dc} do not influence I_{cap}. In addition, the parasitic capacitance of C may help to improve the quality of V_{dc}.

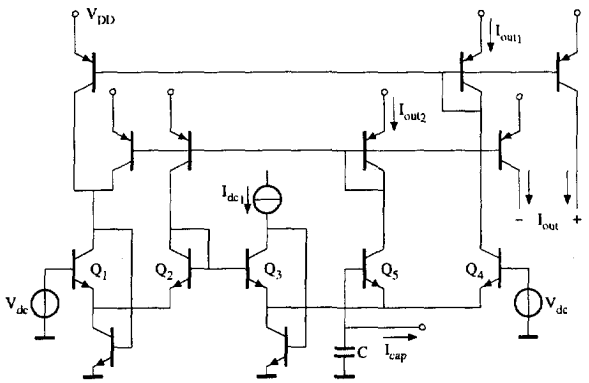

Figure A.10: Low-voltage implementation of the sinh output stage based on the harmonic mean control law.

The finite current gain factor β_F of the transistors constitutes another (dominant) source of errors. In particular, the collector current of Q_3 is corrupted by the base current of the CE stage. The error can be reduced by increasing both the collector current and the emitter area of Q_3 by the same factor. Alternatively, two stage nullor implementations are an adequate means for reducing β_F-induced errors.

When the circuit specifications demand both 1-volt and class-AB operation, the use of PNP current mirrors is inevitable. Obviously, the availability of a fully complementary bipolar process or a BiCMOS process is a major advantage in this situation. In processes where only lateral PNP devices are available, their limited f_T will confine the bandwidth of the circuit. The bandwidth of the PNP mirrors can be improved using an NPN buffer amplifier instead of a diode-connection to drive the base terminals. This also helps to reduce the gain error introduced by the finite base currents.

Two-quadrant multiplier

Figure A.11 depicts a 1-volt implementation of the class-AB two-quadrant multiplier. The circuit comprises two coupled TL loops: Q_1–Q_4 and Q_1-Q_2-Q_5-Q_6. Again, CE stages are used to sink the currents of the differential pairs. The common factors I_o and $(I_{out_1} + I_{out_2} - I_{dc_1})$ are implemented respectively by Q_2 and Q_1. The latter current is obtained from the output stage, shown in Fig. A.10, by means of the PNP current mirrors. Likewise, I_{in_1} and I_{in_2} are copied from the input splitter, described next. The subtraction of I_{C_1} and I_{C_2}, required to generate I_{cap}, is accomplished by means of a PNP current mirror.

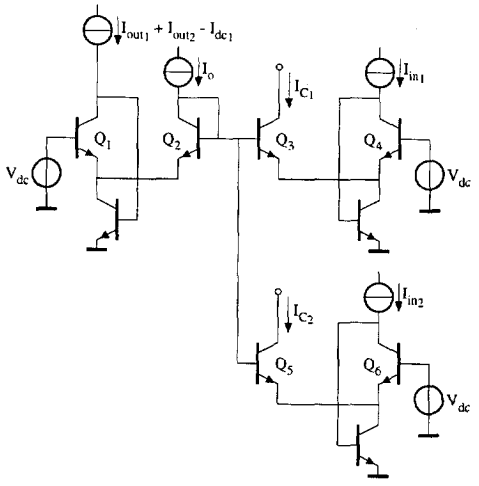

Figure A.11: Low-voltage implementation of the class-AB two-quadrant multiplier.

Input current splitter

The type of current splitter used to generate I_{in_1} and I_{in_2} has not been considered yet, but is of key importance for the performance of the integrator. In a complete filter, the relation between the input and output signals of the integrator is determined by the complete filter structure. As a consequence, it is possible that I_{out} is large while I_{in} is zero. In that situation, $I_{\text{in}_{1,2}}$ equal the quiescent current level I_{dc_2}, while $I_{\text{out}_1} + I_{\text{out}_2} - I_{\text{dc}_1} \gg I_{\text{dc}_1}$. Then, as can be deduced from eqns (A.18a) and (A.18b), either I_{C_1} or I_{C_2} approaches zero, which is clearly disadvantageous.

A possible solution is adaptive biasing of I_{dc_2}. While this method is not a suitable option for the (geometric mean) sinh output stage (it distorts I_{cap} [84], unless severe low-frequency filtering requirements are fulfilled), it can be applied in the input current splitter. Adaptive biasing of I_{dc_2} only results in common-mode signals in $I_{\text{in}_{1,2}}$ and in theory does not affect the circuit operation at all. When I_{dc_2} is derived from the average value of $(I_{\text{out}_1} + I_{\text{out}_2} - I_{\text{dc}_1})$, $I_{\text{in}_{1,2}}$ will never tend to zero. Since I_{dc_2} does not affect the circuit operation, the filtering requirements are very modest; significant ripple and noise can be tolerated.

Figure A.12 shows a 1-volt embodiment of the input current splitter. Due to the adaptive biasing arrangement, $|I_{\text{in}}|$ will not become much greater than I_{dc_2} and therefore both a geometric and a harmonic mean current splitter can be used. The circuit shown in Fig. A.12 is based on the geometric mean function, which results in a more simple circuit realisation. Transistors Q_1–Q_6 comprise a TL loop, where Q_2, Q_4, Q_5 and Q_6 are biased at I_{dc_2}. A folded TL loop does not provide subtraction points as the collectors cannot be connected to emitter

nodes. The subtraction required in the equation $I_{\text{in}} = I_{\text{in}_1} - I_{\text{in}_2}$ is implemented by the current mirror Q_7-Q_8. The input current is connected to the emitters of Q_1 and Q_2. The collector current of Q_1 equals I_{in_1}. Hence, Q_7 conducts $(I_{\text{dc}_2} + I_{\text{in}_2})$. This is exactly the current needed at the common emitter node of Q_3 and Q_4. This current is copied by Q_8. Due to the 1-volt supply, it is not possible to use a conventional current mirror having a diode-connected input transistor. Instead, Q_7 is connected as a CE stage, controlled by the collector voltage of Q_2.

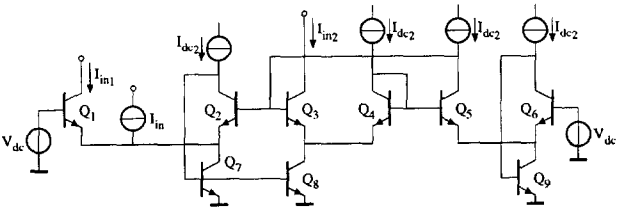

Figure A.12: Low-voltage implementation of the input current splitter based on the geometric mean control law.

Interconnection of the input current splitter, the two-quadrant multiplier and the output stage yields the complete TL integrator. Correct operation has been verified through simulation using realistic IC transistor models.

A.3 A second-order low-pass filter

As discussed in Section 4.3.4, the class of 'Exponential State-Space' (ESS) filters proposed in [10] can be generalised. As an illustration of the general class of DTL circuits, this section treats the design of a second-order filter that does not fit into the class of ESS filters proposed in [10]. Section A.3.1 describes the synthesis of a second-order Butterworth low-pass filter. Simulation results are presented next in Section A.3.2.

A.3.1 Design of the filter

A possible state-space description of a Butterworth second-order low-pass filter is given by:

$$2CU_T\dot{I}_{\text{out}} = I_{\text{o}}\left(I_x - 2I_{\text{out}}\right), \tag{A.19a}$$

$$CU_T\dot{I}_x = I_{\text{o}}\left(I_{\text{in}} - I_{\text{out}}\right), \tag{A.19b}$$

where I_{o} is a dc current, I_{in} is the input current and I_{out} the output current. The currents I_x and I_{out} are state variables.

The cut-off frequency ω_c equals $I_o/(\sqrt{2}CU_T)$. It is assumed that I_{in} contains a dc component $I_{in,dc}$. As a result, I_{out} and I_x contain dc components equal to $I_{in,dc}$ and $2I_{in,dc}$, respectively.

Possible definitions within the generalised class of DTL circuits of two capacitance currents I_{C_1} and I_{C_2} are given by:

$$I_{C_1} = CU_T \left(\frac{\dot{I}_x}{I_x} + \frac{\dot{I}_{out}}{I_{out}} \right), \tag{A.20a}$$

$$I_{C_2} = CU_T \left(\frac{\dot{I}_x}{I_x} - \frac{\dot{I}_{out}}{I_{out}} \right). \tag{A.20b}$$

Figure A.13 shows a possible implementation of eqns (A.20a) and (A.20b). Obviously, eqns (A.20a) and (A.20b) do not fit into the framework suggested by (4.19) as both I_{C_1} and I_{C_2} are functions of both state currents I_x and I_{out}. Eqns (A.20a) and (A.20b) can be implemented by the structures depicted in Figs A.13(b) and A.13(a), respectively.

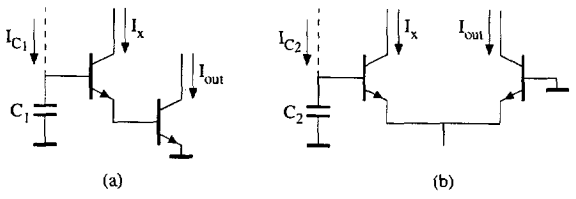

Figure A.13: Two capacitance current definitions.

The capacitance current definitions (A.20a) and (A.20b) are used to implement the derivatives $\dot{I}_{out}$ and $\dot{I}_x$. Solving eqns (A.20a) and (A.20b) for $\dot{I}_{out}$ and $\dot{I}_x$ and substitution in eqns (A.19a) and (A.19b) yields two current-mode polynomials:

$$I_{out}\,(I_{C_1} - I_{C_2}) = I_o\,(I_x - 2I_{out})\,, \tag{A.21a}$$

$$I_x\,(I_{C_1} + I_{C_2}) = 2I_o\,(I_{in} - I_{out})\,. \tag{A.21b}$$

To implement eqns (A.21a) and (A.21b) using TL circuit techniques, suitable TL decompositions have to be derived. Addition of a redundant term $2I_oI_{out}$ to both sides of eqn (A.21a) yields a valid TL loop equation:

$$I_{out}\,(2I_o + I_{C_1} - I_{C_2}) = I_oI_x. \tag{A.22a}$$

The second TL loop equation is derived as follows: a term $2I_oI_x$ is added to both sides of (A.21b); next, (A.22a) is solved for I_x; the resulting expression for I_x is substituted for I_x appearing at the left-hand side of (A.21b). This yields:

$$I_{out}\,(2I_o + I_{C_1} - I_{C_2})\,(2I_o + I_{C_1} + I_{C_2}) = 2I_o^2\,(I_{in} - I_{out} + I_x)\,. \tag{A.22b}$$

The linear factors in eqns (A.22a) and (A.22b) are strictly positive and represent collector currents. Figure A.14 depicts a possible implementation of these equations. In order of appearance, the linear factors in eqns (A.22a) and (A.22b) are implemented by transistors Q_6–Q_2–Q_1–Q_{10} and Q_6–Q_2–Q_3–Q_1–Q_4–Q_5. The factor 2 at the right-hand side of eqn (A.22b) is realised by the scale factor of Q_3. All other NPN transistors constitute simple nullor implementations. The PNP transistors implement current mirrors. The dc current $I_{\rm dc}$ equals 0.5 μA. In accordance with eqns (A.20a) and (A.20b), I_{C_1} is derived from the collector currents of Q_6 and Q_7, whereas I_{C_2} is derived from the collector currents of Q_6 and Q_{10}. The supply voltages are +2/-1.3 V.

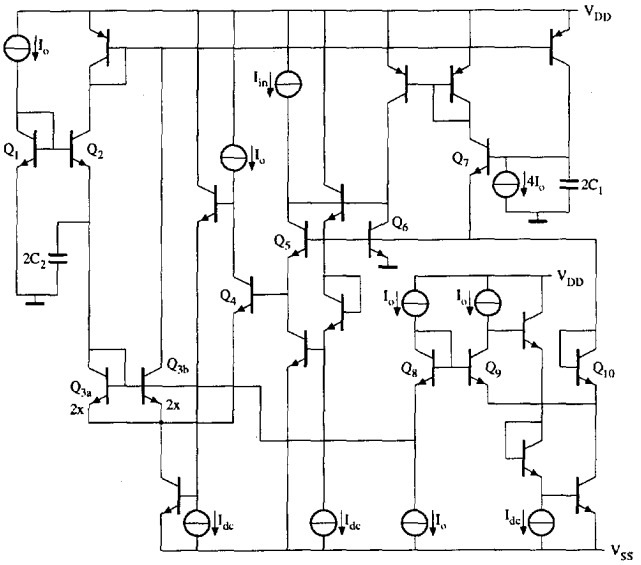

Figure A.14: A Butterworth second-order low-pass filter.

A.3.2 Simulation results

Correct operation of the circuit was verified by means of simulation using realistic transistor models. Figure A.15 shows a transient simulation at 40 kHz. The amplitude of the input signal is 90% of $I_{\rm in,dc}$, which equals 1 μA. With $C = C_1 = C_2 = 100$ pF, $U_T = 26$ mV and $I_{\rm o} = 1$ μA, $\omega_{\rm c}$ equals 43.3 kHz. Clearly, the relation between $I_{\rm in}$ and $I_{\rm out}$ is linear, despite the strongly nonlinear behaviour of I_{C_1} and I_{C_2}.

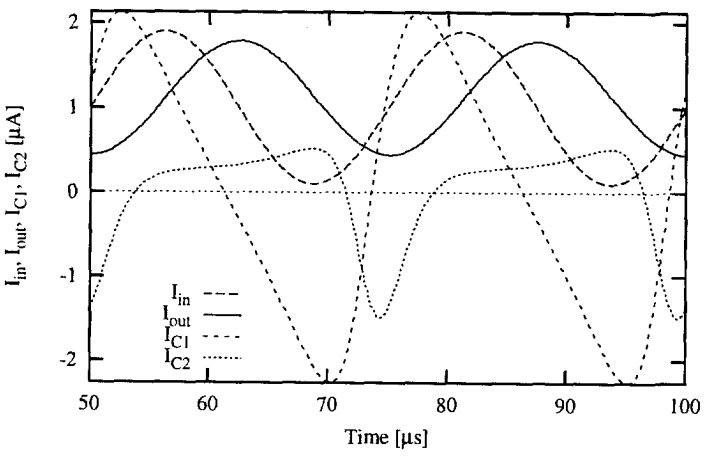

Figure A.15: Transient simulation of the Butterworth filter.

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Summary

The introduction of the capacitance as a basic TransLinear (TL) network element significantly extends the applicability of these circuits. The resulting class of 'Dynamic Translinear' networks, also known as 'log-domain' circuits, can be used to implement both linear and non-linear frequency-dependent signal processing functions. In the area of analogue continuous-time filters, which is facing serious challenges due to ever more stringent low-voltage, low-power and high-frequency demands, the theoretically linear transfer function offered by TL filters provides a useful alternative for those applications that do require a large dynamic range, but do not need a high signal-to-noise ratio. Most specifications obtainable with bipolar-transistor TL filters are comparable to the specifications of bipolar-transistor-only g_mC filters. This applies, e.g., to the signal-to-noise ratio, the bandwidth, the power consumption and the tunability characteristics. However, a significantly better dynamic range specification can be realised owing to the theoretical (external) linearity of TL filters. The dynamic range of TL filters can even exceed the dynamic range of opamp-MOSFET-C filters, especially at low supply voltages. Due to the promising expectations and encouraging results obtained thus far, research efforts have rapidly increased and dynamic translinear circuit design has become a trend.

This thesis describes the structured analysis and synthesis of both Static (i.e., conventional) TransLinear (STL) and Dynamic TransLinear (DTL) circuits. It is shown that log-domain filters, and DTL networks in general, are closely related to the conventional class of STL circuits. Having established this relation, it follows that a current-mode point of view is the most suitable approach to the design of DTL circuitry. The current-mode approach has the additional advantage that the existing theory and experience on STL circuits becomes directly applicable to the analysis and synthesis of DTL networks.

After the general introduction of Chapter 1, Chapter 2 starts with a discussion of the design principles that form the foundation of the thesis. In a general context, companding networks are considered that exhibit a theoretically linear frequency-dependent transfer function even though the signal path contains non-linear processing blocks. A general model is developed, includ-

ing both instantaneous and syllabic companding systems. Dynamic translinear and Dynamic Voltage-TransLinear (DVTL) filters can be considered as special cases of externally-linear internally-non-linear companding networks. Next to the DTL and DVTL principles, the (conventional) STL principles are reviewed.

Although synthesis is more powerful than analysis, a synthesis method must go together with a generally applicable analysis method in the same domain. This is a prerequisite for structured electronic design. Chapter 3 therefore deals with the analysis of TL circuits before synthesis is considered in Chapter 4. The analysis of STL networks has been well established and is briefly reviewed in Chapter 3. On the contrary, analysis methods for DTL circuits have not been reported extensively in the literature. Large-signal analysis methods are however of crucial importance as small-signal analyses cannot prove the externally-linear transfer function of TL filters nor reveal the functionality of non-linear DTL networks. The existing STL analysis method uses a current-mode approach and Chapter 3 shows that this approach is best suited to DTL circuit analysis as well. The capacitance currents form the key to a general large-signal analysis method. Identifying loops of capacitors and junctions, simple current-mode expressions for the capacitance currents can be derived, which compose a supplement to the KCL (Kirchhoff's Current Law) equations and the TL loop equations. Two methods have been developed for finding expressions for the capacitance currents. Using a global method, the final result of the calculations is a higher-order DE describing the network. Alternatively, a state-space method can be applied, which yields a set of first-order DEs, a state-space description, and diminishes the intermediate expression swell. The latter method uses fictitious transistors to convert the capacitance voltages to (collector) currents, which are chosen to represent the state of the circuit. In addition, Chapter 3 explores the characteristics of three different classes of DTL networks proposed in the literature. These are log-domain, tanh and sinh filters.

Chapter 4 constitutes the core of this thesis. A structured synthesis methodology is developed for the design of both STL and DTL networks. Basically, the method is a generalisation and extension of the existing synthesis method for STL circuits and beneficially exploits the high level of similarity between STL and DTL circuits. Synthesis takes off with a normalised, i.e., dimensionless, polynomial, rational function, n^{th}-order root function or differential equation. Next, dimension transformations are applied to arrive at an equation having the proper dimensions to allow for a TL implementation. Several circuit characteristics can be derived from the applied transformations. The subsequent synthesis step is required only for DTL networks: the time derivatives are implemented by means of capacitance currents, which are introduced by definition, using state-space techniques. The possible definitions of the capacitance currents are linked to a classification of DTL circuits. The resulting framework is found to be more general than the classifications described in the literature. As

a result of this synthesis step, both STL and DTL designs are now described by a current-mode multivariable polynomial and the succeeding design trajectory is roughly identical. To implement the multivariable polynomial, it has to be mapped onto one or more TL loop equations. This process is called 'translinear decomposition', which can be divided into non-parametric and parametric decomposition. Next to a description of the characteristics of both types of decompositions, an efficient algorithm is developed for the automatic generation of non-parametric decompositions. Once a TL decomposition has been found, the final design stage is the hardware implementation of the TL loop equations. This process entails numerous different synthesis options and even more possibilities arise from the employment of alternative exponential devices, such as compound transistors and floating-gate MOS transistors, from operation of the MOS transistor in the triode region, and from the application of the back-gate. Next to the synthesis method developed in this thesis, several alternative methods have been proposed in the literature for the design of TL filters. Hence, a comparison is made to elucidate the differences and similarities. The chapter is concluded by a treatment of class-AB operation, which is an important issue closely related to synthesis.

The analysis and synthesis methods dealt with in Chapters 3 and 4 are based on ideal exponential devices. However, in practice, device non-idealities introduce distortion. Chapter 5 treats the second-order effects involved with the bipolar and the subthreshold MOS transistor. Methods are described to reduce the distortion introduced by finite current gain, parasitic resistances, body effect, Early effect, parasitic capacitances and mismatch. Nevertheless, in general, considerable design efforts are usually required to realise a *high-performance* TL circuit.

Noise is of fundamental importance in electronic circuits. Chapter 6 is concerned with the analysis of noise in both STL and DTL circuits. Noise analysis is not trivial due to the non-linear nature of the devices employed. Even for externally-linear circuits, the exponential device characteristics give rise to intermodulation between signals and noise. The situation is further complicated by the fact that the internal noise sources are non-stationary. For these reasons, small-signal noise analysis methods do not suffice. Once again, it is shown that the current-mode approach, in combination with known results from non-linear circuit theory, facilitates an elegant solution to the challenge of large-signal noise analysis.

Chapter 7 discusses the usefulness of VTL circuits and in particular of dynamic VTL networks. The conclusion is that VTL circuits are interesting from an academic point of view, however, their practical value is very limited. The decreasing validity of the square law in modern IC processes eliminates the sole foundation of VTL circuits. Moreover, even for a perfect square law device, the design of VTL networks is frustrated by the mathematically awkward equa-

tions involved, which also diminish the versatility of these circuits. In the area of DVTL, considerable amounts of hardware are required to linearise common-source and differential pair output stages. In contrast, the strong inversion MOS analogue of the sinh does not require any additional hardware for linearisation purposes. The circuit is already linear and is in fact a well-known circuit. Its linearisation is based on properties of the polynomial character of the square law.

Chapter 8 describes several realisations, which illustrate and verify the developed theory. The emphasis is placed on DTL circuits. Some non-conventional STL circuits have been designed as well; they are based on properties of the subthreshold MOS transistor not available in bipolar designs. Two low-voltage low-power TL filters are described next. The first filter, having a second-order Butterworth low-pass characteristic, is operated in class A. The second filter, an integrator, uses class-AB operation to increase the dynamic range. Next, a non-linear application of the DTL principle is treated: an RMS-DC converter. Starting from the DE describing the RMS-DC function, a suitable network is synthesised. The final realisation example illustrates the design of (dynamic) voltage-translinear circuits. A 3.3-V current-controlled oscillator is designed in an IC process exhibiting a reasonable square law conformance.

Finally, Chapter 9 presents the conclusions of this thesis.

Samenvatting

Het ontwerp van dynamische translineaire en log-domein circuits heeft zich ontwikkeld tot een duidelijke nieuwe trend binnen de analoge elektronica. Het gebruik van de capaciteit als een basis translineair-netwerkelement leidt namelijk tot een aanzienlijke toename van de potentiële functionaliteit van translineaire circuits. Dynamische translineaire schakelingen kunnen worden toegepast voor de realisatie van zowel lineaire als niet-lineaire frequentie-afhankelijke signaalbewerkingsfuncties. Met name op het gebied van de analoge tijdcontinue filters, dat zich gesteld ziet voor serieuze uitdagingen door de steeds strengere eisen ten aanzien van voedingsspanning, vermogensconsumptie en bandbreedte, vormen translineaire (TL) filters een interessant en uitermate geschikt alternatief voor die toepassingen die wèl een groot dynamisch bereik vereisen, maar niet noodzakelijk een hoge signaalruisverhouding. Zo kan bij lage voedingsspanningen het dynamisch bereik van TL filters gemakkelijk groter zijn dan het dynamisch bereik haalbaar met opamp-MOSFET-C filters. Bandbreedte, vermogensconsumptie en regelbaarheid van TL filters zijn vergelijkbaar met de specificaties van g_mC filters die opgebouwd zijn uit enkel bipolaire transistoren. Het is dan ook niet verwonderlijk dat de onderzoeksactiviteiten op het gebied van TL filters de laatste jaren snel zijn toegenomen!

Dit proefschrift beschrijft de analyse en synthese van zowel statische translineaire (STL) als dynamische translineaire (DTL) schakelingen. Hierbij wordt veelvuldig gebruik gemaakt van de grote overeenkomsten die bestaan tussen conventionele (statische) en dynamische translineaire netwerken. Eén van de conclusies van dit proefschrift is dat voor de analyse en synthese van DTL schakelingen het best gebruik kan worden gemaakt van beschrijvingen in termen van stromen. Een bijkomend voordeel van deze methode is dat de bestaande theorie en ervaring op het gebied van STL circuits direct toepasbaar zijn op DTL netwerken.

Na de algemene introductie in hoofdstuk 1 worden in hoofdstuk 2 de ontwerpprincipes besproken die in dit proefschrift aan bod komen. Allereerst wordt een algemeen model opgesteld voor dynamische circuits die opgebouwd zijn uit *niet-lineaire* functies, maar die toch een *lineaire* frequentie-afhankelijke overdracht

van ingang naar uitgang hebben. Het model omvat zowel 'syllabic companding' als 'instantaneous companding' filters. Dynamische translineaire en dynamische spannings-translineaire filters zijn speciale gevallen binnen dit model. De ontwerpprincipes van deze filters worden vervolgens behandeld op circuitniveau. Daarnaast worden de conventionele TL principes kort beschreven.

Een gestructureerde synthesemethode kan niet zonder een bijbehorende analysemethode. Hoofdstuk 3 behandelt derhalve eerst de analyse van TL schakelingen, waarna hoofdstuk 4 ingaat op het eigenlijke ontwerpproces. Na een korte samenvatting van de bestaande analysemethode voor STL circuits, worden nieuwe methoden beschreven voor de analyse van DTL schakelingen. Deze methoden zijn gebaseerd op grootsignaalmodellen omdat kleinsignaalmodellen onbruikbaar zijn om de grootsignaallineariteit van een TL filter te bewijzen dan wel om de functionaliteit van niet-lineaire DTL circuits bloot te leggen. De sleutel tot de analyse van DTL schakelingen wordt gevormd door de capaciteitsstromen. Uitdrukkingen voor de capaciteitsstromen in termen van de collectorstromen kunnen worden afgeleid uit de lussen die iedere capaciteit vormt met een aantal transistorjuncties in serie. Twee nieuwe analysemethoden worden beschreven. De eerste methode resulteert direct in een hogere-orde differentiaalvergelijking die de schakeling beschrijft. Bij de tweede methode worden fictieve transistoren aan het netwerk toegevoegd, waarna een toestandsbeschrijving van het circuit kan worden gevonden. Voordeel van de laatstgenoemde methode is een lagere rekenintensiteit. Tenslotte worden in hoofdstuk 3 de karakteristieken geanalyseerd van een aantal typen DTL schakelingen die in de literatuur zijn beschreven: log-domein, tanh en sinh filters.

Hoofdstuk 4 vormt de kern van dit proefschrift en behandelt het gestructureerd ontwerp van zowel STL als DTL schakelingen. De ontwikkelde synthesemethode kan gezien worden als een generalisatie van de bestaande ontwerpmethode voor STL circuits. Het ontwerp begint met een dimensieloze wiskundige vergelijking: een polynoom, een rationele functie, een wortelfunctie of een differentiaalvergelijking. Door de toepassing van eenvoudige transformaties wordt een vergelijking gevonden met de juiste dimensies om een TL realisatie mogelijk te maken. Een aantal eigenschappen van het uiteindelijke circuit zijn direct terug te voeren op de gebruikte transformaties. Aangezien STL schakelingen al beschreven worden door een polynoom is de volgende ontwerpstap alleen van toepassing op DTL circuits. Deze stap betreft het vertalen van de tijdafgeleiden in de differentiaalvergelijking naar capaciteitsstromen. Om deze capaciteitsstromen te definiëren wordt een toestandsbeschrijving gebruikt. De verschillende vormen van definities geven een klassificatie van TL filters die breder is dan de bestaande klassificaties die bekend zijn uit de literatuur. Door het vervangen van de tijdafgeleiden door capaciteitsstromen wordt de differentiaalvergelijking herleid tot een polynoom in meerdere variabelen. In dit stadium van het ontwerpproces worden zowel de STL als de DTL functies door een poly-

noom beschreven. Het resterende ontwerptraject is daarom vrijwel identiek voor zowel STL als DTL schakelingen. De eerstvolgende stap is TL decompositie; het polynoom wordt afgebeeld op een (set van) TL lusvergelijking(en), waarbij onderscheid gemaakt wordt in niet-parametrische en parametrische decomposities. Beide typen worden beschreven en een algoritme voor de automatische generatie van niet-parametrische decomposities wordt ontwikkeld. Voor parametrische decomposities ontbreekt tot nu toe een dergelijk algoritme. Wanneer een decompositie gevonden is, volgt de 'hardware'-implementatie van de TL lusvergelijkingen. Dit proces bevat vele keuzemogelijkheden, zoals de lus-topologie en het gebruik van alternatieve exponentiële devices. Vervolgens vergelijkt hoofdstuk 4 de ontwikkelde methode met alternatieve synthesemethoden die beschreven zijn in de literatuur. Ook worden in dit hoofdstuk klasse-AB implementaties behandeld.

De theorie gepresenteerd in hoofdstuk 3 and 4 is gebaseerd op ideale exponentiële devices. In de praktijk resulteren de diverse niet-idealiteiten van de componenten in distorsie. Hoofdstuk 5 beschrijft de effecten van eindige stroomversterking, parasitaire weerstanden en capaciteiten, 'body effect', 'Early effect' en 'mismatch'. Tevens worden methoden behandeld die de invloed van deze niet-idealiteiten reduceren.

Hoofdstuk 6 gaat in op de ruiseigenschappen van zowel STL als DTL netwerken. Translineaire circuits staan niet bepaald bekend om hun goede ruiseigenschappen. In klasse-AB schakelingen kan de *signaalruisverhouding* nog verder verslechteren door signaal-ruis-intermodulatie, die het gevolg is van het exponentiële gedrag van de transistoren. Dit neemt niet weg dat het *dynamisch bereik* van klasse-AB implementaties uitstekend kan zijn. De analyse van ruis in TL schakelingen is niet-triviaal. Grootsignaalanalyses zijn nodig om de signaal-ruis-intermodulatie en het niet-stationaire karakter van de interne ruisbronnen mee te kunnen nemen in de berekeningen. Dit hoofdstuk beschrijft een elegante ruisanalysemethode die gebruik maakt van de ontwikkelde TL analysemethoden enerzijds en resultaten uit de niet-lineaire ruistheorie anderzijds.

Het gebruik van MOS transistoren in het sterke-inversiegebied, dat beschreven wordt door een kwadratisch model, leidt tot de verwante klasse van spannings-translineaire circuits. Ook hier kan een onderscheid worden gemaakt tussen statische en dynamische schakelingen. Hoofdstuk 7 bediscussieert het praktisch nut van deze schakelingen, waarbij de nadruk ligt op dynamische spannings-translineaire netwerken. Geconcludeerd kan worden dat spanningstranslineaire circuits weliswaar interessant zijn vanuit een academisch standpunt, maar vrijwel onbruikbaar zijn in de praktijk. Allereerst is dit te wijten aan de zeer beperkte geldigheid van het kwadratische MOS-model. Daarnaast wordt synthese bemoeilijkt door de onhandelbare wiskundige vergelijkingen. Verder vereist de linearisatie van mogelijke dynamische spannings-translineaire uitgangstrappen veel hardware, terwijl de theoretische toename van het dy-

namisch bereik minimaal is. Het equivalent van de DTL 'sinh'-uitgangstrap vormt hierop een uitzondering. Dit circuit, feitelijk een welbekende schakeling, is zelf reeds lineair en maakt gebruik van het feit dat het MOS-model een polynoom is, en geen transcendente functie zoals het exponentiële transistormodel.

Om de ontwikkelde theorie te illustreren en te verifiëren worden in hoofdstuk 8 een aantal realisaties beschreven. De nadruk ligt hierbij op DTL circuits. Eerst worden echter een aantal niet-conventionele STL circuits behandeld. Deze maken gebruik van enkele specifieke eigenschappen van de MOS-transistor in het zwakke-inversiegebied. Vervolgens worden twee TL filters beschreven die ontworpen zijn voor een voedingsspanning van 1 volt en een minimale vermogensconsumptie. Het eerste filter heeft een tweede-orde overdracht en werkt in klasse A, het tweede filter (een integrator) werkt in klasse AB en realiseert dan ook een aanzienlijk betere specificatie van het dynamisch bereik. De toepassing van het DTL principe voor niet-lineaire dynamische functies wordt geïllustreerd middels het ontwerp van een RMS-DC converter. Als laatste voorbeeld wordt een spannings-translineaire oscillator beschreven.

Hoofdstuk 9 bevat de conclusies van dit proefschrift.

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Finally, thanks and love go to my wife Arjanne.

Jan Mulder

Biography

Jan Mulder was born in Medemblik, The Netherlands, on July 7, 1971. After completing the VWO Wiringherlant in Wieringerwerf in 1989, he started his study of electrical engineering at the Delft University of Technology and received his M.Sc. in 1994. Subsequently, he did his Ph.D. research at the Electronics Research Laboratory of the same university. He is now with Philips Research Laboratories, Eindhoven, The Netherlands.

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