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Passive Techniques to Reduce Supply Sensitivity in an LC Oscillator Achieving 46-dB Suppression

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***Abstract*—This paper proposes two fully passive techniques to reduce the supply sensitivity of an LC oscillator. An RC low-pass filter is employed to reduce the supply sensitivity of coarse-tuning switched capacitors stemming from code-dependent parasitic capacitance. To cancel the remaining supply sensitivity, the supply variations are scaled and coupled to polarity-switchable varactor pairs, which are introduced in the resonator to provide a frequency tuning gain that is reverse to the supply sensitivity. A programmable capacitive divider is used to scale the supply variations by a proper ratio. The proposed techniques are applied in a 5.83–6.99 GHz class-B LC oscillator. Prototyped in 65-nm CMOS, the oscillator occupies 0.24 mm^2 and consumes 6.8 mW from 1 V. With supply perturbations in the 0.1–50 MHz frequency range, the measured reduction of the supply sensitivity is 20–46.2 dB, which is the highest reported over a wide frequency range. Benefiting from the fully passive implementation, the proposed techniques do not consume extra power or degrade the phase noise.**

***Index Terms*—Supply sensitivity, voltage-controlled oscillator (VCO), varactor, switchable capacitors, spur reduction**

I. INTRODUCTION

Radio-frequency oscillators are among the most sensitive circuits in communication systems. Their high supply sensitivity makes them vulnerable to unavoidable supply variations, such as noise and ripples [1]. Typically, an oscillator must rely on a dedicated low-dropout (LDO) regulator to clean up its supply voltage. This sets stringent requirements on the power supply rejection and output noise of LDOs, especially in the cases of low-noise oscillators. As a consequence, these LDOs may consume large power and chip area. To avoid these penalties, it is desirable to have oscillators with low supply sensitivity.

Several techniques have been proposed in the literature to reduce the supply sensitivity of RF oscillators [2], [3], [4], [5], [6], [7], [8], [9]. In [2], two constant-g_m circuits with different supply sensitivities were utilized to provide a stable current for a ring oscillator. A calibration loop was employed to optimize the current ratio between the two constant-g_m stages. However, due to mismatches in the current mirroring ratio, the reduction of supply sensitivity was limited to 10 dB within a narrow frequency range (below 1 MHz). In [8], the supply ripples were replicated with a proper amplification ratio to the gate bias of a PMOS current source to stabilize the current. However, this technique is only applicable to current-biased oscillators. The replication circuits can also introduce extra noise that degrades the phase noise performance. Also, they cannot suppress the supply sensitivity of the switchable capacitors in the oscillator. In [5], spurious patterns from supply ripple were detected and reconstructed within a PLL, then subtracted from the DCO's frequency control word to compensate for the frequency variations. However, the detection loop parameters limit the maximum cancellable supply variation frequency. A more generic and wideband supply sensitivity reduction method is thus sought to protect the RF oscillators of various topologies from the supply ripples and noise.

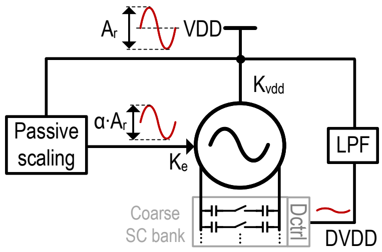

Fig. 1. The proposed concept of supply sensitivity reduction in an oscillator.

In this paper, we propose two fully passive techniques to reduce the supply sensitivity of LC oscillators. They exploit 1) an RC low-pass filter and 2) polarity-switchable varactors with a reversed frequency tuning gain to mitigate the supply sensitivity. They do not introduce any extra power consumption and are broadly applicable across various oscillator topologies.

II. PROPOSED TECHNIQUES TO REDUCE THE SUPPLY SENSITIVITY

In an LC oscillator, there are three main root causes of supply sensitivity: code-dependent nonlinear parasitic capacitance in the switchable capacitors (SCs), nonlinear parasitic capacitance in negative-g$_m$ transistors, and out-of-phase harmonic mixing (Groszkowski's effect). The polarity of the supply sensitivity varies with different designs and at different frequencies. This paper proposes to exploit a low-pass filter (LPF) and a dual-polarity varactor to suppress the supply sensitivity in the oscillator, as illustrated in Fig. 1.

A. LPF for Supply Sensitivity Reduction of SCs

Switchable capacitors are widely used for coarse frequency tuning of LC oscillators in both analog and digital PLLs. As

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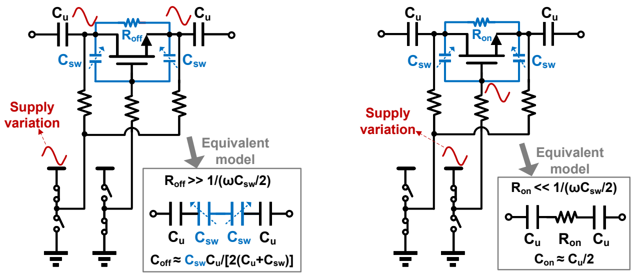

(a) (b)

Fig. 2. Schematic of the switched capacitor in (a) OFF and (b) ON states.

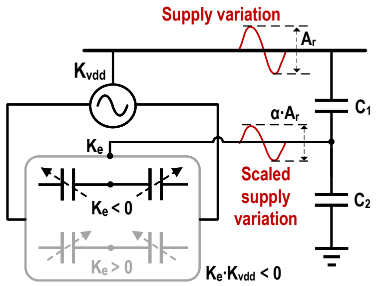

Fig. 3. Conceptual diagram of the proposed supply sensitivity reduction technique using varactors with reverse frequency tuning gain.

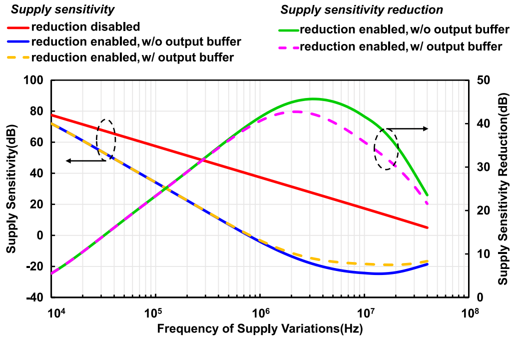

Fig. 4. Simulated supply sensitivity of the oscillator with/without the two proposed techniques when half of the SCs are off.

shown in Fig. 2(a), the equivalent capacitance of the SC in the off state is modulated by the supply voltage of the preceding control logic (typically an inverter or two), causing frequency-dependent supply sensitivity. It is a major contributor to the supply sensitivity, especially when most of the SCs are off.

In this work, low-pass filtering is applied on the supply voltage of the inverter drivers of SCs to attenuate the supply disturbances arriving at the SCs. Due to the small static current of the inverter drivers here (maximum 5 uA in this design), an on-chip RC low-pass filter is used to clean up the supply of control logic. A large R can be used in the LPF to achieve a narrow bandwidth with acceptable capacitance. With a 20-kΩ resistor and 100-pF capacitor inserted onto V_{DD}, a low-pass filter (LPF) with a 79-kHz cutoff frequency is achieved, while the IR drop on the local supply voltage is kept low. In this way, any noise or ripples above 79 kHz on the supply line will be attenuated before reaching the local V_{DD} of the driving inverters and modulating the parasitic capacitance of the SCs.

While SCs are also used for fine frequency tuning in digital PLLs, their contribution to the supply sensitivity is small. Thereby, we only apply this technique on coarse-tuning SCs. To adopt this technique in a practical PLL, the LPF can be disabled by shorting the R during the locking process, and enabled after the PLL is locked.

B. Reverse-Polarity Varactors for Supply Sensitivity Cancellation

Instead of *isolating* the oscillator from supply disturbances, an alternative solution is to cancel K_{vdd} by introducing an auxiliary component that has the reversed supply sensitivity. Fig. 3 presents the proposed concept. Auxiliary varactors are introduced into the oscillator to provide a frequency tuning gain of K_e, whose polarity is opposite to that of the supply sensitivity (i.e., $K_e \cdot K_{vdd} < 0$). The supply variation is scaled by a proper ratio (α) and then fed to the varactors. To avoid extra noise and power penalties, the scaling of supply variation is achieved with a capacitive divider (C_1 and C_2), thereby $0 < \alpha < 1$. If $\alpha \cdot K_e + K_{vdd} = 0$, the supply sensitivity can (ideally) be completely cancelled.

K_{vdd} is evidently frequency-dependent and sensitive to PVT variations. Even its polarity may flip. The scaling ratio α and polarity of K_e must thus be adjusted accordingly. To furnish K_e of different polarities, two pairs of varactors are employed and connected in opposite polarities to the LC resonator. The varactors are designed so that $|K_e| > |K_{\mathrm{vdd}}|$ over the PVT variations. By enabling one of the varactor pairs, K_e can be programmed to be either positive or negative. The scaling ratio α realized by the capacitive voltage divider is $\alpha = C_1/(C_1 + C_2)$. The value of C_1 and C_2 is digitally programmed to achieve the optimal α. In a typical case, the supply variation is small, allowing K_e and K_{vdd} to be considered nearly constant for a given oscillation frequency and supply voltage. Hence, by choosing the correct polarity of K_e and optimal value for α, the supply sensitivity of the oscillator can almost disappear.

The simulated supply sensitivity of the oscillator with and without the proposed techniques is presented in Fig. 4. After applying the proposed techniques, the supply sensitivity is reduced by approximately 45 dB at 5MHz. This demonstrates the effectiveness of the proposed techniques to reduce the oscillator's supply sensitivity. Since the techniques do not suppress the amplitude modulation on the oscillator, a concern of the AM-PM conversion at the output buffer may arise. To address that, the effect of supply sensitivity reduction is examined in simulations with and without the output buffer. As shown in Fig. 4, there is little difference (< 5 dB) in the supply sensitivity reduction between these two cases. It proves that the AM-PM conversion is not severe and its adverse effect on the proposed techniques is small.

III. Circuit implementation

To demonstrate the efficacy of the proposed techniques in a generalized and representative manner, we have chosen a class-B LC oscillator with a 2-turn spiral inductor in the LC tank and a tail resistor R_T. Coarse frequency tuning is provided by a switchable-capacitor bank with 12 SC units. The two types of techniques described in Section II are applied here.

As discussed, a low-bandwidth RC LPF is desired on the supply line of the buffering inverters for the SCs in the LC tank. As a tradeoff between the bandwidth, maximum voltage drop and area, a 20-kΩ resistor and 100-pF capacitor are used in the LPF. The achieved cutoff frequency is 79 kHz. With the maximum observed static current consumption of 5 uA in the buffering inverters, the voltage drop on the supply line is limited to a maximum of 100 mV. This creates an unnoticeable impact on the Q-factor of the SCs.

The two pairs of varactors are implemented with identical MOSCAPs but flipped terminal connections. The varactor_P and varactor_N provide negative and positive K_e, respectively. The varactors are DC biased with resistors R_b, R_P and R_N. The DC bias of the varactors is optimized to maximize their frequency tuning gain K_e. The varactors are sized to cover the largest possible supply sensitivity over PVT variations.

Capacitive voltage dividers with switched-capacitor banks are utilized to realize the tunable scaling ratio α. The capacitances C_1 and C_2 are programmed with 7-bit and 2-bit switchable capacitors, respectively. The value of α can be tuned in the range between 0 and 0.81. The R_P and the capacitance $(C_1 + C_2)$ comprise a high-pass filter (HPF) in the achieved scaling ratio for the supply variations

$$\alpha = \frac{j\omega C_1 \cdot R_P}{1 + j\omega \left(C_1 + C_2\right) \cdot R_P} \tag{1}$$

To avoid an extra attenuation and phase shift by the HPF, its cutoff frequency is designed to be low (100 kHz) by using large resistors R_P and R_N of 200 kΩ. At frequencies above the cutoff, $\alpha \approx C_1 / \left(C_1 + C_2\right)$. At very high frequencies (>10 MHz), the ON resistance of the switches in the capacitive divider becomes comparable to or larger than the impedance of the capacitors. Hence, α starts to deviate from the optimal value, affecting the supply sensitivity reduction.

In this design, each pair of the varactors is connected to a separate capacitive divider. The polarity selection of the K_e is accomplished by setting the capacitive scaling ratio of the unused varactor pair to 0.

Although not implemented herein, the calibration of K_e polarity and α value can be done within a PLL. By injecting a predefined supply ripple (e.g., a modulating current drawn from V_{DD}), the correlation between the detected phase error in the PLL and the ripple can provide information for the calibration.

IV. Measurement results

The oscillator with the proposed supply sensitivity reduction techniques was prototyped in a 65-nm 1P9M CMOS process. Fig. 6(a) shows the chip micrograph. The chip area is $0.24\,\mathrm{mm}^2$. It consumes 6.8 mW from a 1V supply. The frequency tuning range spans from 5.83 to 6.99 GHz. The measured phase noise at different oscillation frequencies is plotted in Fig. 6(b). At a 10 MHz offset, the phase noise is -137.2 $\sim$ -139.4 dBc/Hz across the frequency tuning range. Biasing the varactors in low-gain or high-gain regions results in a negligible difference in phase noise. This proves that the proposed techniques do not impair the phase noise performance.

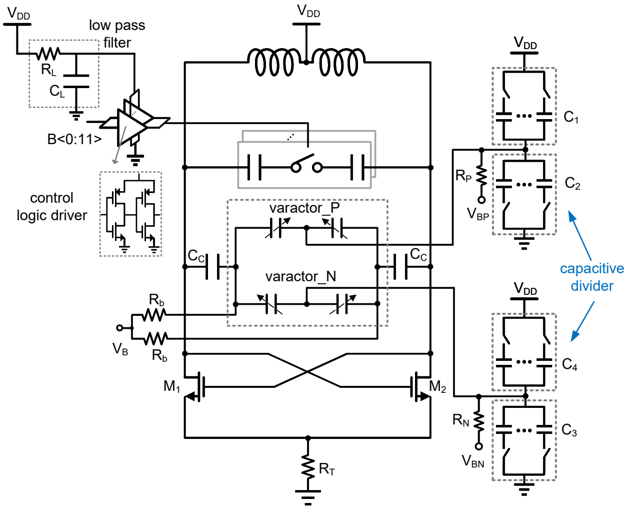

Fig. 5. Schematic of the LC oscillator with the proposed supply sensitivity reduction techniques.

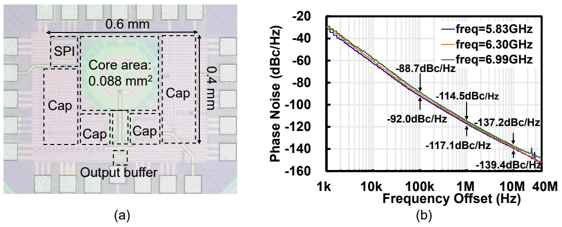

Fig. 6. (a) Chip micrograph of the LC oscillator with supply sensitivity reduction. (b) Measured phase noise at different oscillation frequencies.

To examine the efficacy of the proposed techniques, the spur level at the oscillator output in the presence of a supply ripple is measured as an indicator of supply sensitivity. A 15-mV$_{\mathrm{pp}}$ 5-MHz sinusoidal ripple is first injected on the supply voltage of the oscillator. With the RC LPF enabled and α tuned from 0 up to 0.81, the measured spur level at 5.83 GHz across the different α value is shown in Fig. 7(a). When α is set to the optimal value (0.63 in this case), the spur level is reduced from -34 dBc to -77.5 dBc, demonstrating a 43.5 dB reduction of the supply sensitivity. The measured output frequency spectrum at 5.83 GHz before and after enabling the proposed techniques is shown in Fig. 7(b). Performance of the supply sensitivity reduction is measured across the whole frequency tuning range of the oscillator with the same supply

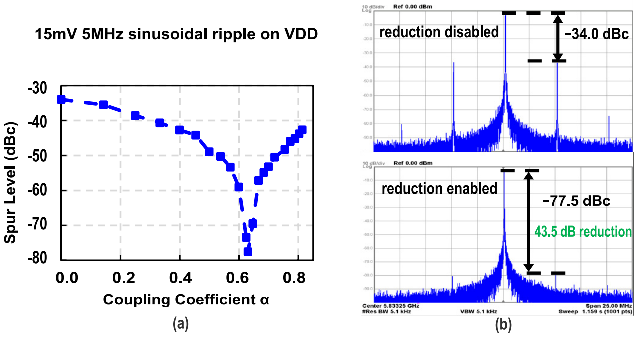

Fig. 7. (a) Measured spur level induced by the supply ripple across the range of α; (b) measured spectrum before/after enabling the two proposed techniques.

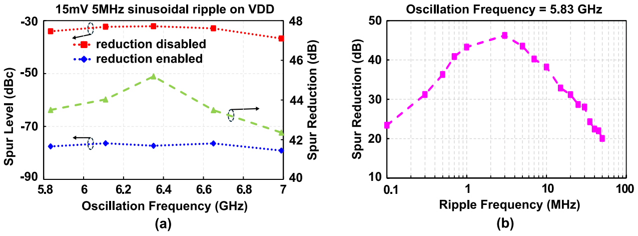

Fig. 8. Measured supply sensitivity reduction (a) across the frequency tuning range and (b) at different supply ripple frequencies.

ripple at 5 MHz. As shown in Fig. 8(a), the achieved reduction of supply sensitivity is higher than 42 dB over the frequency tuning range. When altering the ripple frequency in the range of 0.1-50 MHz, the achieved reduction of supply sensitivity is always higher than 20 dB, as shown in Fig. 8(b).

Performance of the proposed oscillator system is compared with the relevant state-of-the-art in Table I. The proposed techniques achieve the highest reduction of the supply sensitivity. Moreover, they provide a reduction of $>$ 20 dB in the supply sensitivity between 0.1-50 MHz, which is the widest frequency range reported. Benefiting from the fully passive circuit realizations, the proposed techniques introduce no degradation of the phase noise. Compared to the other class-B LC oscillators in the same frequency range, our oscillator maintains the best-in-class figure-of-merit, which proves the aforementioned advantage.

V. CONCLUSION

This paper proposes two fully passive methods to reduce the supply sensitivity of LC oscillators. An RC low-pass filter on the supply voltage of their controlling drivers protects the switched capacitors from supply perturbations. Polarity-switchable varactors are employed to cancel the remaining supply sensitivity. By selecting the correct polarity and coupling the properly scaled supply fluctuations to varactors via capacitive dividers, accurate cancellation of the supply sensitivity is achieved. The proposed techniques are showcased in a 6-GHz class-B oscillator and prototyped in 65-nm CMOS. They achieve 20–46.2 dB reduction of supply sensitivity with supply variations in the 0.1-50 MHz frequency range. Owing to the fully passive realization, no extra power overhead or phase noise degradation is introduced. Moreover, the proposed techniques are generically applicable to both voltage- and current-biased oscillator topologies.

TABLE I
PERFORMANCE COMPARISON WITH THE STATE-OF-THE-ART WORKS.

		This work	JSSC'19 [8]	ESSCIRC'16 [5]	ISSCC'16 [2]	TCAS-I'22 [9]
Techniques		**Passive supply sensitivity reduction**	Feed-forward compensation	PLL compensation	Constant-g_m biasing	Supply noise cancellation
Osc. Type		**LC**	LC	LC	Ring	Ring
CMOS Tech. (nm)		**65**	40	65	40	28
VDD(V)		**1**	1	1	1.1	1
Frequency (GHz)		**5.83 - 6.99**	4.90	3.57	3.2	4
PN@10M (dBc/Hz)		**-139.4**	-130.5	NA	NA	-109.8
Supply sensitivity reduction (dB)	@100kHz	**23.4**	NA	NA	13	NA
	@1MHz	**43.8**	24	15	10	29
	@3MHz	**46.2**	NA	16	7	35*
	@5MHz	**43.5**	30	12	8	38
	@10MHz	**38.2**	25.6	17	8	26
	@50MHz	**20.1**	NA	NA	NA	18
Frequency range of reduction (MHz)		**0.1 - 50**	0.5-20	0.555-10*	0.01-20	1-100*
Power of Osc. (mW)		**6.8**	0.8	18.9$^+$	2.95$^+$	6.65$^+$
Power consumed by supply sensitivity reduction (mW)		**0**	0.2	2.4	NA	2.4
FoM**@10MHz		**186.4**	185.2	NA	NA	NA
Chip area (mm^2)		**0.24**	0.23	0.63	0.0216	0.088

+: power consumption of PLL *: estimated from measured results **: FOM = - PN + $20\log_{10}(f_o/\Delta f)$ $-10\log_{10}(P_{DC}/1\text{mW})$

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